THE DATASHEET OF

ADP3181JRQZ-RL

5-Bit or 6-Bit Programmable 2-,3-,4-Phase Synchronous Buck Controller

ADP3181

FEATURES

- **Selectable 2-, 3- or 4-phase operation at up to 1 MHz per phase**
- **±14.5 mV worst-case mV differential sensing error over temperature**
- **Logic-level PWM outputs for interface to external high power drivers**
- **Active current balancing between all output phases**
- **Built-in power good/crowbar blanking supports on-the-fly VID code changes**
- **Digitally programmable output can be switched between VRM 9 (5-bit) and VRD 10 (6-bit) VID codes**
- **Programmable short-circuit protection with programmable latch-off delay**

APPLICATIONS

Desktop PC power supplies for:

- **Next-generation Intel® processors**
- **VRM modules**

GENERAL DESCRIPTION

The ADP3181 is a highly efficient multiphase synchronous buck-switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 6-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage. The CPUID input selects whether the DAC codes match the VRM 9 or VRD 10 specifications. It uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, or 4-phase operation, allowing for the construction of up to four complementary buck-switching stages.

The ADP3181 also includes programmable no-load offset and slope functions to adjust the output voltage as a function of the load current so that it is always optimally positioned for a system transient. The ADP3181 provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power good output that accommodates on-the-fly output voltage changes requested by the CPU.

The device is specified over the commercial temperature range of 0°C to +85°C and is available in a 28-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM

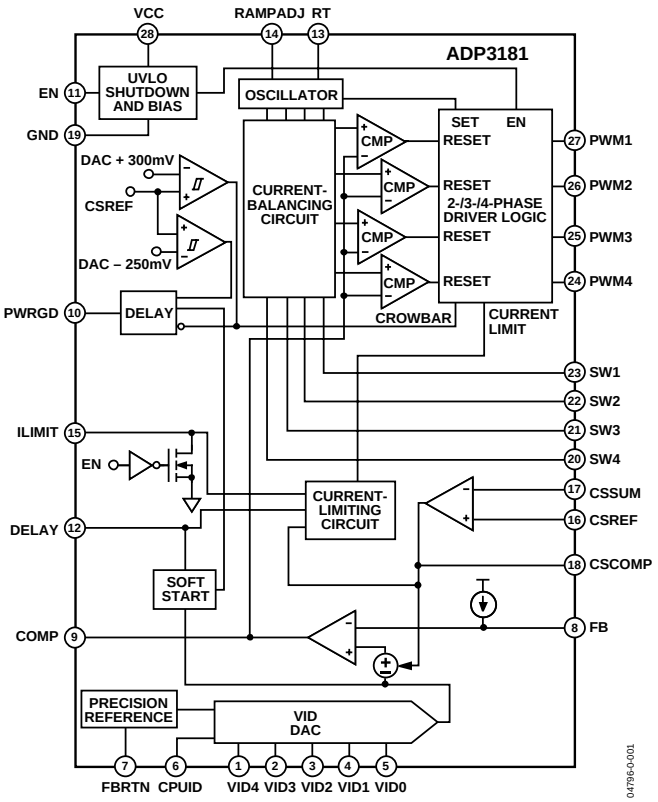

Figure 1.

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REVISION HISTORY

5/04—Revision 0: Initial Version

SPECIFICATIONS

VCC = 12 V, FBRTN = GND, T_A = 0°C to +85°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER						
Output Voltage Range[2]	V_{COMP}		0.7		3.1	V
Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN, CSSUM = CSCOMP. See Figure 2.	−14.5		+14.5	mV
Line Regulation	ΔV_{FB}	VCC = 10 V to 14 V		0.05		%
Input Bias Current	I_{FB}		14	15.5	17	µA
FBRTN Current	I_{FBRTN}			100	140	µA
Output Current	$I_{O(ERR)}$	FB forced to V_{OUT} – 3%		500		µA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		C_{COMP} = 10 pF		25		V/µs
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$	CPUID > 4.5 V			0.8	V
		CPUID < 4.0 V			0.4	V
Input High Voltage	$V_{IH(VID)}$	CPUID > 4.5 V	2.0			V
		CPUID < 4.0 V	0.8			V
Input Current	I_{VID}	VID(x) = 0 V, CPUID > 4.5 V		40	70	µA
		VID(x) = 0 V, CPUID < 4.0 V		20	35	µA
Pull-up Resistance	R_{VID}		40	60		kΩ
Internal Pull-up Voltage		CPUID > 4.5 V	2.25	2.5	2.75	V
		CPUID < 4.0 V	1.1	1.25	1.4	V
VID Transition Delay Time[2]		VID code change to FB change	400			ns
No CPU Detection Turn-off Delay Time[2]		VID code change to 11111 to PWM going low	400			ns
CPUID INPUT						
Input Low Voltage	$V_{IL(CPUID)}$				0.4	V
Input High Voltage	$V_{IH(CPUID)}$		0.8		4.0	V
VR 9 Detection Threshold Voltage			4.0		4.5	V
Input Current	I_{CPUID}	CPUID = 0 V		20	3.5	µA
Pull-up Resistance	R_{CPUID}		4.0	60		kΩ
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.25		4	MHz
Frequency Variation	f_{PHASE}	T_A = 25°C, R_T = 250 kΩ, 4-phase	155	200	245	kHz
		T_A = 25°C, R_T = 115 kΩ, 4-phase		400		kHz
		T_A = 25°C, R_T = 75 kΩ, 4-phase		600		kHz
Output Voltage	V_{RT}	R_T = 100 kΩ to GND	1.9	2.0	2.1	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ – FB	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		0		100	µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM – CSREF. See Figure 3.	−3		+3	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		−50		+50	nA
Gain Bandwidth Product	$GBW_{(CSA)}$			10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/µs
Input Common-Mode Range		CSSUM and CSREF	0		2.7	V
Positioning Accuracy	ΔV_{FB}	See Figure 4.	−77	−80	−83	mV
Output Voltage Range			0.05		2.7	V
Output Current	I_{CSCOMP}			500		µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT BALANCE CIRCUIT						
Common-Mode Range	$V_{SW(X)CM}$		−600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0 V	20	30	40	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0 V	4	7	10	μA
Input Current Matching	$\Delta I_{SW(X)}$	SW(X) = 0 V	−5		+5	%
CURRENT LIMIT COMPARATOR						
Output Voltage						
Normal Mode	$V_{ILIMIT(NM)}$	EN > 0.8 V, R_{ILIMIT} = 250 kΩ	2.9	3	3.1	V
In Shutdown	$V_{ILIMIT(SD)}$	EN < 0.4 V, I_{ILIMIT} = −100 μA			400	mV
Output Current, Normal Mode	$I_{ILIMIT(NM)}$	EN > 0.8 V, R_{ILIMIT} = 250 kΩ		12		μA
Maximum Output Current[2]			60			μA
Current Limit Threshold Voltage	V_{CL}	$V_{CSREF} - V_{CSCOMP}$, R_{ILIMIT} = 250 kΩ	105	125	145	mV
Current Limit Setting Ratio		V_{CL}/I_{ILIMIT}		10.4		mV/μA
DELAY Normal Mode Voltage	$V_{DELAY(NM)}$	R_{DELAY} = 250 kΩ	2.9	3	3.1	V
DELAY Overcurrent Threshold	$V_{DELAY(OC)}$	R_{DELAY} = 250 kΩ	1.7	1.8	1.9	V
Latch-off Delay Time	t_{DELAY}	R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF		1.5		ms
SOFT START						
Output Current, Soft-start Mode	$I_{DELAY(SS)}$	During start-up, DELAY < 2.4 V	15	20	25	μA
Soft-start Delay Time	$t_{DELAY(SS)}$	R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF, VID code = 011111		1		ms
ENABLE INPUT						
Input Low Voltage	$V_{IL(EN)}$				0.4	V
Input High Voltage	$V_{IH(EN)}$		0.8			V
Input Current, Input Voltage Low	$I_{IL(EN)}$	EN = 0 V	−1		1	μA
Input Current, Input Voltage High	$I_{IH(EN)}$	EN = 1.25 V		10	25	μA
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal DAC output	−180	−250	−320	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to nominal DAC output	230	300	370	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 4 mA		225	400	mV
Power Good Delay Time						
During Soft Start[2]		R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF, VID Code = 011111	1			ms
VID Code Changing			100	250		μs
VID Code Static				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to nominal DAC output	230	300	370	mV
Crowbar Reset Point		Relative to FBRTN	630	700	770	mV
Crowbar Delay Time	$t_{CROWBAR}$	Overvoltage to PWM going low				
VID Code Changing			100	250		μs
VID Code Static				400		ns
PWM OUTPUTS						
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = −400 μA		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400 μA	4.0	5		V
SUPPLY						
DC Supply Current				5	10	mA
UVLO Threshold Voltage	V_{UVLO}	VCC rising	6.5	6.9	7.3	V
UVLO Hysteresis			0.7	0.9	1.1	V

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or bench characterization, not tested in production.

TEST CIRCUITS

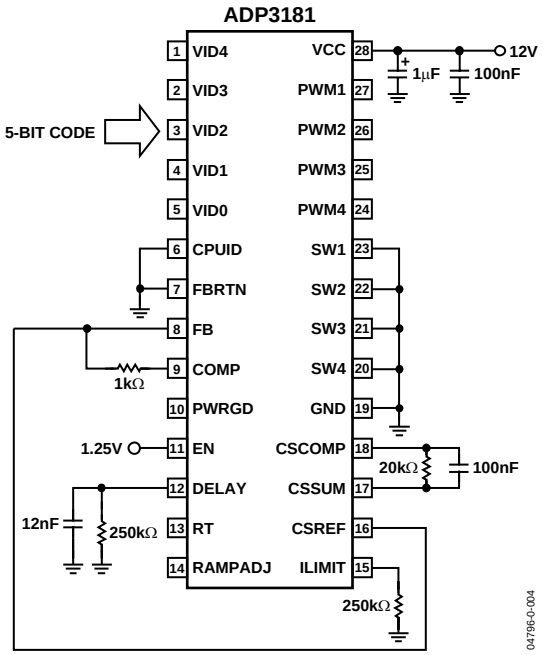

Figure 2. Closed-Loop Output Voltage Accuracy

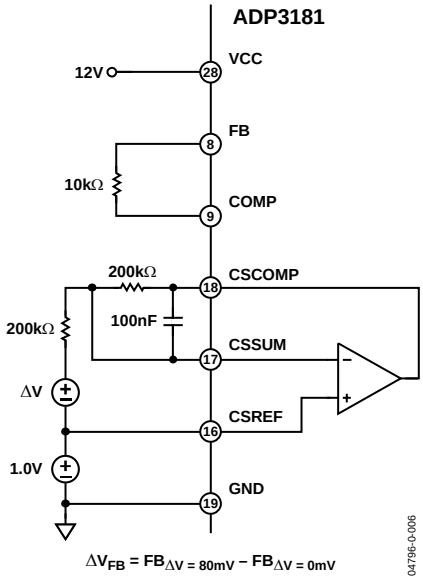

Figure 4. Positioning Voltage

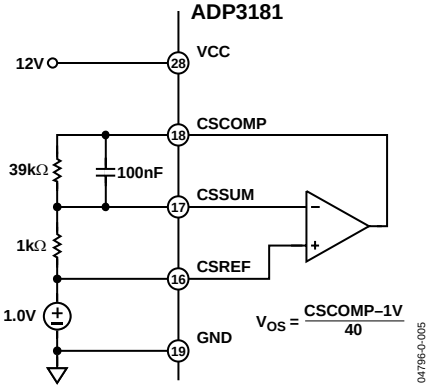

Figure 3. Current Sense Amplifier V_{OS}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +15 V
FBRTN	−0.3 V to +0.3 V
VID0 to VID4, CPUID, EN, DELAY, ILIMIT, CSCOMP, RT, PWM1 to PWM4, COMP	−0.3 V to +5.5 V
SW1 to SW4	−5 V to +25 V
All other inputs and outputs	−0.3 V to VCC +0.3 V
Storage temperature	−65°C to +150°C
Operating ambient temperature range	0°C to 85°C
Operating junction temperature	125°C
Thermal impedance (θ_{JA})	100°C/W
Lead temperature	
Soldering (10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

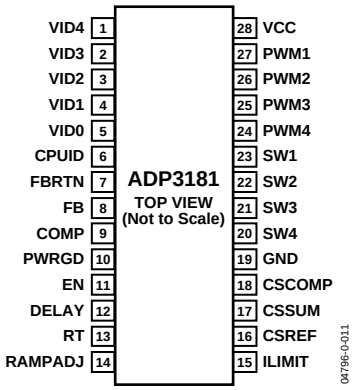

Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Name	Description
1 to 5	VID4 to VID0	Voltage Identification DAC Inputs. These five pins are pulled up to an internal reference, providing a Logic 1 if left open. When in normal mode, the DAC output programs the FB regulation voltage based on the condition of the CPUID pin (see Table 4 and Table 5). Leaving VID4 through VID0 open results in the ADP3181 going into a "no CPU" mode, shutting off its PWM outputs.
6	CPUID	CPU DAC Code Selection Input. When this pin is pulled > 4.5 V, the internal DAC reads its inputs based on the VR 9 VID table (see Table 4). When this pin is < 4 V, the DAC reads its inputs based on the VR 10 VID table (see Table 5) and treats CPUID as the VID5 input.
7	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
8	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no-load offset point.
9	COMP	Error Amplifier Output and Compensation Point.
10	PWRGD	Power Good Output. Open-drain output that signals when the output voltage is outside of the proper operating range.
11	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs.
12	DELAY	Soft-start Delay and Current Limit Latch-off Delay Setting Input. An external resistor and capacitor connected between this pin and GND sets the soft-start ramp-up time and the overcurrent latch-off delay time.
13	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
14	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
15	ILIMIT	Current Limit Setpoint/Enable Output. An external resistor from this pin to GND sets the current limit threshold of the converter. This pin is actively pulled low when the ADP3181 EN input is low, or when VCC is below its UVLO threshold, to signal to the driver IC that the driver high-side and low-side outputs should go low.
16	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power good and crowbar functions. This pin should be connected to the common point of the output inductors.
17	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
18	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determine the slope of the load line and the positioning loop response time.
19	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
20 to 23	SW4 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
24 to 27	PWM4 to PMW1	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3413 or ADP3418. Connecting the PWM3 and/or PWM4 outputs to GND causes that phase to turn off, allowing the ADP3181 to operate as a 2-, 3-, or 4-phase controller.
28	VCC	Supply Voltage for the Device.

TYPICAL PERFORMANCE CHARACTERISTICS

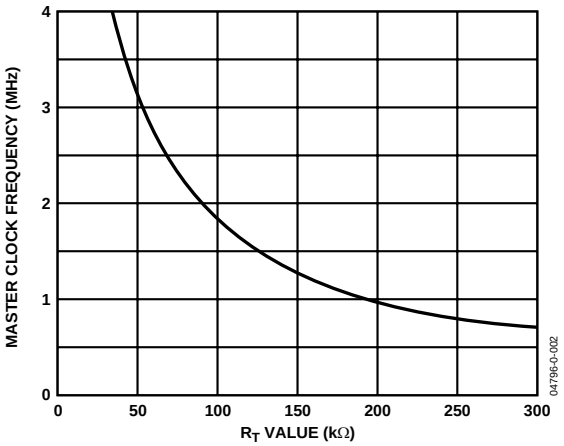

Figure 6. Master Clock Frequency vs. R_T

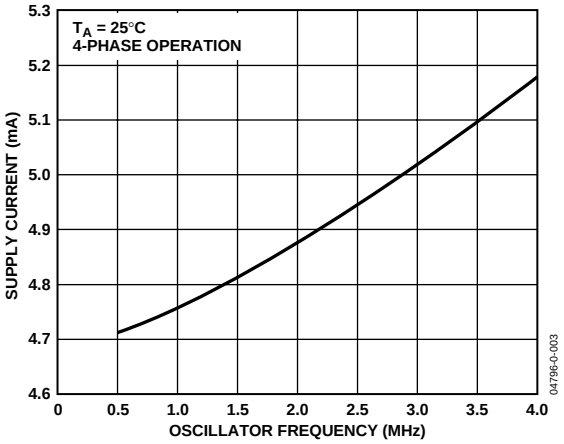

Figure 7. Supply Current vs. Oscillator Frequency

THEORY OF OPERATION

The ADP3181 combines a multimode, fixed-frequency PWM control with multiphase logic outputs for use in 2-, 3-, and 4-phase synchronous buck CPU core supply power converters. The internal VID DAC can be used in the Intel 5-bit VRM 9 or 6-bit VRD/VRM 10 designs, depending on the setting of the CPUID pin. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter places high thermal demands on the components in the system such as the inductors and MOSFETs. The multimode control of the ADP3181 ensures a stable, high performance topology for

- Balancing currents and thermals between phases.
- High speed response at the lowest possible switching frequency and output decoupling.
- Minimizing thermal switching losses due to lower frequency operation.
- Tight load line regulation and accuracy.
- High current output from 4-phase operational design.
- Reduced output ripple due to multiphase cancellation.
- PC board layout noise immunity.
- Ease of use and design due to independent component selection.
- Flexibility in operation for tailoring design to low cost or high performance.

START-UP SEQUENCE

Two functions are set during the start-up sequence: the number of active phases and the VID DAC configuration. The number of operational phases and their phase relationship is determined by internal circuitry that monitors the PWM outputs. Normally, the ADP3181 operates as a 4-phase PWM controller. Grounding the PWM4 pin programs 3-phase operation, and grounding the PWM3 and PWM4 pins programs 2-phase operation.

When the ADP3181 is enabled, the controller outputs a voltage on PWM3 and PWM4 that is approximately 675 mV. An internal comparator checks each pin's voltage versus a threshold of 300 mV. If the pin is grounded, it is below the threshold and the phase is disabled. The output resistance of the PWM pin is approximately 5 kΩ during this detection time. Any external pull-down resistance connected to the PWM pin should not be less than 25 kΩ to ensure proper operation.

PWM1 and PWM2 are disabled during the phase detection interval, which occurs during the first two clock cycles of the internal oscillator. After this time, if the PWM output was not grounded, the 5 kΩ resistance is removed and it switches between 0 V and 5 V. If the PWM output was grounded, it remains off.

The PWM outputs are logic-level devices intended for driving external gate drivers such as the ADP3418. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at a time for overlapping phases.

The VID DAC configuration is determined by the voltage at the CPUID pin. If this pin is pulled up to > 4.5 V, the VID DAC operates with five inputs and generates the VR 9 output voltage range as shown in Table 4. If CPUID is < 4 V, the VID DAC treats CPUID as the VID5 input of VR 10, and operates as a 6-bit DAC using the output voltage range given in Table 5.

Table 4. VR 9 VID Codes for the ADP3181, CPUID > 4.25

VID4	VID3	VID2	VID1	VID0	Output
1	1	1	1	1	No CPU
1	1	1	1	0	1.100 V
1	1	1	0	1	1.125 V
1	1	1	0	0	1.150 V
1	1	0	1	1	1.175 V
1	1	0	1	0	1.200 V
1	1	0	0	1	1.225 V
1	1	0	0	0	1.250 V
1	0	1	1	1	1.275 V
1	0	1	1	0	1.300 V
1	0	1	0	1	1.325 V
1	0	1	0	0	1.350 V
1	0	0	1	1	1.375 V
1	0	0	1	0	1.400 V
1	0	0	0	1	1.425 V
1	0	0	0	0	1.450 V
0	1	1	1	1	1.475 V
0	1	1	1	0	1.500 V
0	1	1	0	1	1.525 V
0	1	1	0	0	1.550 V
0	1	0	1	1	1.575 V
0	1	0	1	0	1.600 V
0	1	0	0	1	1.625 V
0	1	0	0	0	1.650 V
0	0	1	1	1	1.675 V
0	0	1	1	0	1.700 V
0	0	1	0	1	1.725 V
0	0	1	0	0	1.750 V
0	0	0	1	1	1.775 V
0	0	0	1	0	1.800 V
0	0	0	0	1	1.825 V
0	0	0	0	0	1.850 V

Table 5. VR 10 VID Codes for the ADP3181, CPUID Used as a VID5 Input

VID4	VID3	VID2	VID1	VID0	CPUID	Output	VID4	VID3	VID2	VID1	VID0	CPUID	Output
1	1	1	1	1	1	No CPU	1	1	0	1	0	0	1.2125 V
1	1	1	1	1	0	No CPU	1	1	0	0	1	1	1.2250 V
0	1	0	1	0	0	0.8375 V	1	1	0	0	1	0	1.2375 V
0	1	0	0	1	1	0.8500 V	1	1	0	0	0	1	1.2500 V
0	1	0	0	1	0	0.8625 V	1	1	0	0	0	0	1.2625 V
0	1	0	0	0	1	0.8750 V	1	0	1	1	1	1	1.2750 V
0	1	0	0	0	0	0.8875 V	1	0	1	1	1	0	1.2875 V
0	0	1	1	1	1	0.9000 V	1	0	1	1	0	1	1.3000 V
0	0	1	1	1	0	0.9125 V	1	0	1	1	0	0	1.3125 V
0	0	1	1	0	1	0.9250 V	1	0	1	0	1	1	1.3250 V
0	0	1	1	0	0	0.9375 V	1	0	1	0	1	0	1.3375 V
0	0	1	0	1	1	0.9500 V	1	0	1	0	0	1	1.3500 V
0	0	1	0	1	0	0.9625 V	1	0	1	0	0	0	1.3625 V
0	0	1	0	0	1	0.9750 V	1	0	0	1	1	1	1.3750 V
0	0	1	0	0	0	0.9875 V	1	0	0	1	1	0	1.3875 V
0	0	0	1	1	1	1.0000 V	1	0	0	1	0	1	1.4000 V
0	0	0	1	1	0	1.0125 V	1	0	0	1	0	0	1.4125 V
0	0	0	1	0	1	1.0250 V	1	0	0	0	1	1	1.4250 V
0	0	0	1	0	0	1.0375 V	1	0	0	0	1	0	1.4375 V
0	0	0	0	1	1	1.0500 V	1	0	0	0	0	1	1.4500 V
0	0	0	0	1	0	1.0625 V	1	0	0	0	0	0	1.4625 V
0	0	0	0	0	1	1.0750 V	0	1	1	1	1	1	1.4750 V
0	0	0	0	0	0	1.0875 V	0	1	1	1	1	0	1.4875 V
1	1	1	1	0	1	1.1000 V	0	1	1	1	0	1	1.5000 V
1	1	1	1	0	0	1.1125 V	0	1	1	1	0	0	1.5125 V
1	1	1	0	1	1	1.1250 V	0	1	1	0	1	1	1.5250 V
1	1	1	0	1	0	1.1375 V	0	1	1	0	1	0	1.5375 V
1	1	1	0	0	1	1.1500 V	0	1	1	0	0	1	1.5500 V
1	1	1	0	0	0	1.1625 V	0	1	1	0	0	0	1.5625 V
1	1	0	1	1	1	1.1750 V	0	1	0	1	1	1	1.5750 V
1	1	0	1	1	0	1.1875 V	0	1	0	1	1	0	1.5875 V
1	1	0	1	0	1	1.2000 V	0	1	0	1	0	1	1.6000 V

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3181 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 6. To determine the frequency per phase, the clock is divided by the number of phases in use. If PWM4 is grounded, then divide the master clock by 3 for the frequency of the remaining phases. If PWM3 and 4 are grounded, divide by 2. If all phases are in use, divide by 4.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3181 combines differential sensing with a high accuracy VID DAC and reference and a low offset error amplifier to maintain a worst-case specification of ±14.5 mV differential sensing error over its full operating output voltage and temperature ranges. The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN should be connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

OUTPUT CURRENT SENSING

The ADP3181 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning versus load current and for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low-side MOSFET. This amplifier can be configured several ways depending on the objectives of the system:

- Output inductor ESR sensing without a thermistor for lowest cost.
- Output inductor ESR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output inductors) to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor to set the load line required by the microprocessor. The current information is then given as the difference of CSREF – CSCOMP. This difference signal is used internally to offset the VID DAC for voltage positioning and as a differential input for the current limit comparator.

To provide the best accuracy for the sensing of current, the CSA has been designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors so that it can be made extremely accurate.

ACTIVE IMPEDANCE CONTROL MODE

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the CSCOMP pin can be scaled to equal the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This differs from previous implementations and allows enhanced feed-forward response.

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3181 has individual inputs for each phase, which are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for the positioning described previously.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It is also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. Detailed information about programming the ramp is given in the Application Information section.

If desired, external resistors can be placed in series with individual phases to create an intentional current imbalance if desired, such as when one phase may have better cooling and can support higher currents. Resistors RSW1 through RSW4 (see the typical application circuit in Figure 10) can be used for adjusting thermal balance. It is best to have the ability to add these resistors during the initial design, so make sure placeholders are provided in the layout.

To increase the current in any phase, make R_{SW} for that phase larger (make $R_{SW} = 0$ for the hottest phase; do not change during balancing). Increasing R_{SW} to only 500 Ω makes a substantial increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

VOLTAGE CONTROL MODE

A high gain bandwidth voltage mode error amplifier is used for the voltage-mode control loop. The control input voltage to the positive input is set via the VID logic. This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with a resistor, RB, and is used for sensing and controlling the output voltage at this point. A current source from the FB pin flowing through RB is used for setting the no-load offset voltage from the VID voltage. The no-load voltage is negative with respect to the VID DAC. The main loop compensation is incorporated in the feedback network between FB and COMP.

SOFT START

The power-on ramp-up time of the output voltage is set with a capacitor and resistor in parallel from the DELAY pin to ground. The RC time constant also determines the current limit latch off time as explained in the following section. In UVLO or when EN is a logic low, the DELAY pin is held at ground. After the UVLO threshold is reached and EN is a logic high, the DELAY capacitor is charged with an internal 20 µA current source. The output voltage follows the ramping voltage on the DELAY pin, limiting the in-rush current. The soft-start time depends on the value of VID DAC and C_{DLY}, with a secondary effect from R_{DLY}. Refer to the Application Information section for detailed information on setting C_{DLY}.

If either EN is taken low or VCC drops below UVLO, the DELAY capacitor is reset to ground to be ready for another soft-start cycle. Figure 8 shows the typical start-up waveforms for the ADP3181.

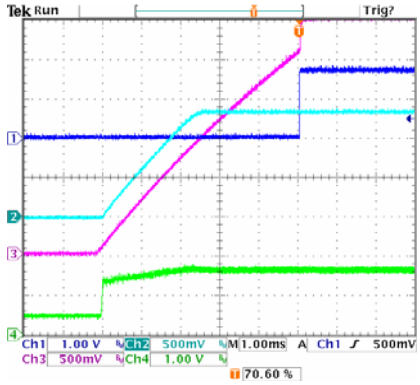

Figure 8. Typical Start-up Waveforms
Channel 1: PWRGD, Channel 2: CSREF,
Channel 3: DELAY, Channel 4: COMP

CURRENT LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3181 compares a programmable current-limit setpoint to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3 V. The current through the external resistor is internally scaled to give a current-limit threshold of 10.4 mV/µA. If the difference in voltage between CSREF and CSCOMP rises above the current-limit threshold, the internal current-limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

After the limit is reached, the 3 V pull-up on the DELAY pin is disconnected, and the external delay capacitor is discharged through the external resistor. A comparator monitors the DELAY voltage and shuts off the controller when the voltage drops below 1.8 V. The current-limit latch-off delay time is thus set by the RC time constant discharging from 3 V to 1.8 V. The Application Information section discusses the selection of C_{DLY} and R_{DLY}.

Because the controller continues to cycle the phases during the latch-off delay time, if the short is removed before the 1.8 V threshold is reached, the controller returns to normal operation. The recovery characteristic depends on the state of PWRGD. If the output voltage is within the PWRGD window, the controller resumes normal operation. However, if short circuit has caused the output voltage to drop below the PWRGD threshold, a soft-start cycle is initiated.

The latch-off function can be reset either by removing and reapplying VCC to the ADP3181, or by pulling the EN pin low for a short time. To disable the short-circuit latch-off function, the external resistor to ground should be left open, and a high value (>1 MΩ) resistor should be connected from DELAY to VCC. This prevents the delay capacitor from discharging so the 1.8 V threshold is never reached. The resistor has an impact on the soft-start time because the current through it adds to the internal 20 µA current source.

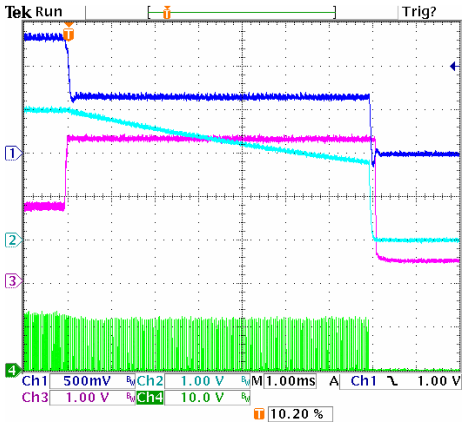

Figure 9. Overcurrent Latch-off Waveforms
Channel 1: CSREF, Channel 2: DELAY,
Channel 3: COMP, Channel 4: Phase 1 Switch Node

During start-up when the output voltage is below 200 mV, a secondary current limit is active because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 2 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry.

There is also an inherent per phase current limit that protects individual phases if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

DYNAMIC VID

The ADP3181 incorporates the ability to dynamically change the VID input while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF event can occur under either light load or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be either positive or negative.

When a VID input changes state, the ADP3181 detects the change and ignores the DAC inputs for a minimum of 400 ns. This time is to prevent a false code due to logic skew while the five VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 250 µs to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

POWER GOOD MONITORING

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if all of the VID DAC inputs are high, or whenever the EN pin is pulled low. PWRGD is blanked during a VIDOTF event for a period of 250 µs to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn-on delay time based on the DELAY ramp. The PWRGD pin is held low until the DELAY pin reaches 2.8 V. The time between when the PWRGD undervoltage threshold is reached and when the DELAY pin reaches 2.8 V provides the turn-on delay time. This time is incorporated into the soft-start ramp. To ensure a 1 ms delay time on PWRGD, the soft-start ramp must also be > 1 ms. Refer to the Application Information section for detailed information on setting C_{DLY}.

OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of about 700 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short of the high-side MOSFET, this action current-limits the input supply or blows its fuse, protecting the microprocessor from destruction.

OUTPUT ENABLE AND UVLO

The input supply (VCC) to the controller must be higher than the UVLO threshold and the EN pin must be higher than its logic threshold for the ADP3181 to begin switching. IF UVLO is less than the threshold or the EN pin is a logic low, the device is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the ILIMIT pin at ground.

In the application circuit, the ILIMIT pin should be connected to the OD pins of the ADP3418 drivers. Because ILIMIT is grounded, this disables the drivers such that both DRVH and DRVL are grounded. This feature is important to prevent discharging of the output capacitors when the controller is shut off. If the driver outputs were not disabled, a negative voltage could be generated on the output due to the high current discharge of the output capacitors through the inductors.

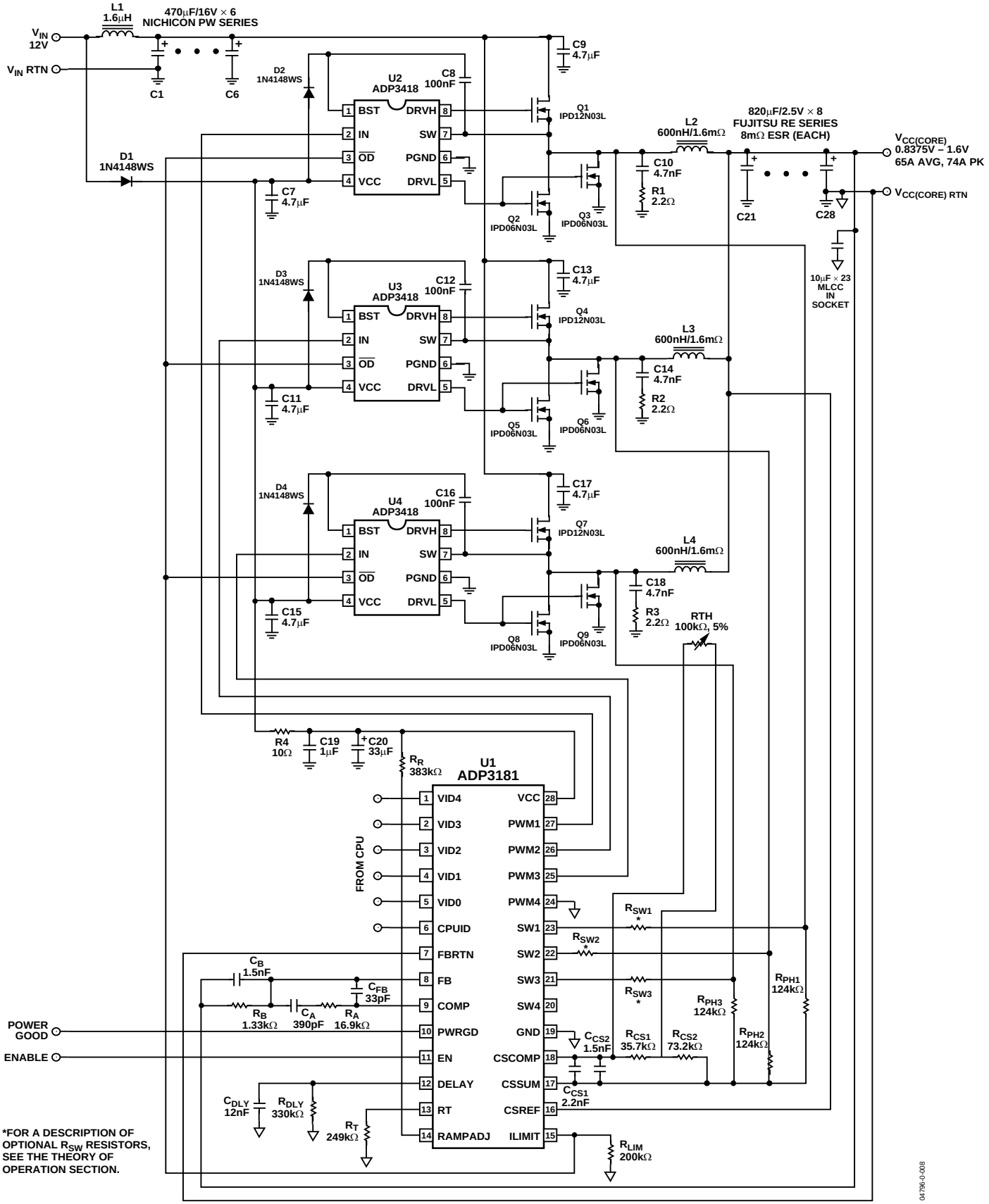

Figure 10. Typical VR 10 Application Circuit

APPLICATION INFORMATION

The design parameters for a typical ADP3181 CPU application are as follows:

- Input voltage (V_{IN}) = 12 V
- VID setting voltage (V_{VID}) = 1.500 V
- Duty cycle (D) = 0.125
- Nominal output voltage at no load (V_{ONL}) = 1.480 V
- Nominal output voltage at 65 A load (V_{OFL}) = 1.3825 V
- Static output voltage drop based on a 1.5 mΩ load line (R_O) from no load to full load:
  $V\Delta = V_{ONL} - V_{OFL} = 1.480\ V - 1.3825\ V = 97.5\ mV$
- Maximum output current (I_O) = 65 A
- Number of phases (n) = 3
- Switching frequency per phase (f_{SW}) = 330 kHz

SETTING THE CLOCK FREQUENCY

The ADP3181 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors and input and output capacitors. With n = 3 for three phases, a clock frequency of 990 kHz sets the switching frequency, f_{SW}, of each phase to 330 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. Figure 6 shows that to achieve a 990 kHz oscillator frequency, the correct value for R_T is 200 kΩ. For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

SOFT-START AND CURRENT-LIMIT LATCH-OFF DELAY TIMES

Because the soft-start, PWRGD delay, and current-limit latch-off delay functions all share the DELAY pin, these three parameters must be considered together. The first step is to set C_{DLY} for the PWRGD delay ramp. This ramp is generated with a 20 μA internal current source. The value of R_{DLY} has a second-order impact on the soft-start time because it sinks part of the current source to ground. However, as long as R_{DLY} is kept greater than 200 kΩ, this effect is minor. The value for C_{DLY} can be approximated using

$$C_{DLY} = \left(20\ \mu A - \frac{2.8\ V - V_{VID} - V_{PWRGD(UV)}}{2 \times R_{DLY}}\right) \times \frac{t_{PWRGD}}{2.8\ V - V_{VID} - V_{PWRGD(UV)}} \quad (1)$$

where t_{PWRGD} is the desired PWRGD delay time and $V_{PWRGD(UV)}$ is the undervoltage threshold for the PWRGD comparator.

Assuming an R_{DLY} of 250 kΩ and a desired a PWRGD delay time of 1 μs, C_{DLY} is 12 nF. The soft-start delay time can then be calculated using

$$t_{ss} = \frac{C_{DLY} \times V_{VID}}{20\ \mu A - \frac{V_{VID}}{2 \times R_{DLY}}} \quad (2)$$

Once C_{DLY} has been chosen, R_{DLY} can be calculated for the current limit latch off time using:

$$R_{DLY} = \frac{2 \times t_{DELAY}}{C_{DLY}} \quad (3)$$

If the result for R_{DLY} is less than 200 kΩ, a smaller soft-start time should be considered by recalculating the equation for C_{DLY}, or a longer latch-off time should be used. In no case should R_{DLY} be less than 200 kΩ. In this example, a delay time of 2 ms gives R_{DLY} = 333 kΩ. The closest standard 5% value is 330 kΩ. Substituting 330 kΩ back into Equations 1 and 2 shows that the PWRGD delay and soft-start times do not change significantly.

INDUCTOR SELECTION

The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs, but allows using smaller size inductors and, for a specified peak-to-peak transient deviation, less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. In any multiphase converter, a practical value for the peak-to-peak inductor ripple current is less than 80% of the maximum dc current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current in the inductor. Equation 4 determines the minimum inductance based on a given output ripple voltage:

$$I_{RIPPLE} = \frac{V_{VID}\ (1-D)}{f_{SW} \times L} \quad (4)$$

$$L \geq \frac{V_{VID} \times R_O \times (1-D) \times (1-(n \times D))}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

Intel recommends that the ripple voltage should not exceed 10 mV peak-to-peak at the socket. Solving Equation 4 for a 12 mV peak-to-peak output ripple voltage at the regulator's output to allow for drops through the PCB traces yields

$$L \geq \frac{1.5\ V \times 1.5\ m\Omega \times 0.875 \times (1-0.375)}{330\ kHz \times 12\ mV} = 310\ nH \quad (6)$$

If the ripple voltage is less than that designed for, the inductor can be made smaller until the ripple value is met. This allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. A 300 nH inductor is a good choice to start, and it gives a calculated ripple current of 13.3 A, which is 61% of the full load current of 21.7 A. The inductor should not saturate at the peak current of 29 A, and should be able to handle the sum of the power dissipation caused by the average current of 22 A in the winding and the core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the phase currents. A large DCR causes excessive power losses, while too small a value leads to increased measurement error. A good rule is to have the DCR be about 1 to 1½ times the droop resistance (R_O).

DESIGNING AN INDUCTOR

Once the inductance and DCR are known, the next step is to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to keep the accuracy of the system controlled. Using 15% for the inductance and 8% for the DCR (at room temperature) are reasonable tolerances that most manufacturers can meet.

The first decision in designing the inductor is to choose the core material. Several possibilities for providing low core loss at high frequencies include the powder cores (Kool-Mμ® from Magnetics, Inc. or Micrometals) and the gapped soft ferrite cores (3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

The best choice for a core geometry is a closed-loop types, such as potentiometer cores, PQ, U, and E cores, or toroids. A good compromise between price and performance are cores with a toroidal shape. There are many useful references for quickly designing a power inductor, such as

- Magnetic Designer Software Intusoft (http://www.intusoft.com)
- Designing Magnetic Components for High Frequency DC-DC Converters, McLyman, Kg Magnetics, ISBN 1-883107-00-08

Selecting a Standard Inductor

The companies listed in Table 6 can provide design consultation and deliver power inductors optimized for high power applications upon request.

Table 6. Power Inductor Manufacturers

Company	Contact	Website
Coilcraft	(847) 639-6400	http://www.coilcraft.com
Coiltronics	(561) 752-5000	http://www.coiltronics.com
Sumida Electric Company	(510) 668-0660	http://www.sumida.com
Vishay	(402) 563-6506	http://www.vishay.com

OUTPUT DROOP RESISTANCE

The design requires that the regulator output voltage measured at the CPU pins drops when the output current increases. The specified voltage drop corresponds to a dc output resistance (R_O).

The output current is measured by summing together the voltage across each inductor and then passing the signal through a low-pass filter. This summer-filter is the CS amplifier configured with resistors $R_{PH(X)}$ (summers) and R_{CS} and C_{CS} (filter). The output resistance of the regulator is set by these equations, where R_L is the DCR of the output inductors:

$$R_O = \frac{R_{CS}}{R_{PH(X)}} \times R_L \quad (7)$$

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \quad (8)$$

One has the flexibility of choosing either R_{CS} or $R_{PH(X)}$. It is best to start with $R_{PH(X)}$ in the range of 100 kΩ to 200 kΩ, and then solve for R_{CS} by rearranging Equation 7. Using 100 kΩ for $R_{PH(X)}$:

$$R_{CS} = \frac{R_O}{R_L} \times R_{PH(X)}$$

$$R_{CS} = \frac{1.5\ \text{m}\Omega}{1.6\ \text{m}\Omega} \times 100\ \text{k}\Omega = 93.8\ \text{k}\Omega$$

Next, use equation 8 to solve for C_{CS}:

$$C_{CS} = \frac{300\ \text{nH}}{1.6\ \text{m}\Omega \times 93.8\ \text{k}\Omega} = 2.0\ \text{nF}$$

The closest standard value for C_{CS} is 1.8 nF. If the calculated value is not a standard value, recalculate for the closest 1% resistor values for R_{CS} and $R_{PH(X)}$ using the final value selected for C_{CS}. This can be quickly calculated by multiplying the original values of R_{CS} and $R_{PH(X)}$ by the ratio of the calculated C_{CS} to the actual value used. For best accuracy, C_{CS} should be a 5% or 10% NPO capacitor. For this example, the actual values used for R_{CS} and $R_{PH(X)}$ are 104.2 kΩ and 111.1 kΩ. The closest standard 1% value for $R_{PH(X)}$ is 110 kΩ. R_{CS} is used later and should not be rounded yet.

INDUCTOR DCR TEMPERATURE CORRECTION

With the inductor's DCR being used as the sense element, and copper wire being the source of the DCR, one needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage change in resistance to that of the wire, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, Resistors R_{CS1} and R_{CS2} are needed (see Figure 11) to linearize the NTC and produce the desired temperature tracking.

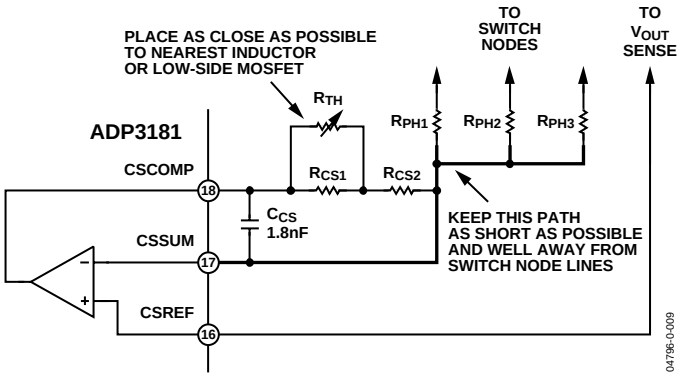

Figure 11. Temperature Compensation Circuit Values

The following procedure yields values to use for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on type and value. Because there is not a value yet, start with a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.

2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. We call these resistance values A (A is $R_{TH}(50°C)/R_{TH}(25°C)$) and B (B is $R_{TH}(90°C)/R_{TH}(25°C)$). The NTC's relative value is always 1 at 25°C.

3. Find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage change needed, which can be 0.39%/°C initially. These values are r_1 (r_1 is $1/(1+ TC \times (T1 - 25))$) and r_2 (r_2 is $1/(1 + TC \times (T2 - 25))$) where TC = 0.0039, T1 = 50°C, and T2 = 90°C.

4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH}:

$$R_{CS2} = \frac{(A-B)\times r_1 \times r_2 - A\times(1-B)\times r_2 + B\times(1-A)\times r_1}{A\times(1-B)\times r_1 - B\times(1-A)\times r_2 - (A-B)} \quad (9)$$

$$R_{CS1} = \frac{(1-A)}{\frac{1}{1-r_{CS2}} - \frac{A}{r_1 - r_{CS2}}}$$

$$R_{TH} = \frac{1}{\frac{1}{1-r_{CS2}} - \frac{1}{r_{CS1}}}$$

Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (10)$$

Calculate values for R_{CS1} and R_{CS2} using the following:

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \quad (11)$$

$$R_{CS2} = R_{CS} \times ((1-k) + (k \times r_{CS2}))$$

For this example, R_{CS} has already been calculated in the previous section to be 104.2 kΩ, so a thermistor value of 100 kΩ is started with. In available 0603 size thermistors, there is a Vishay NTHS0603N01N1003JR NTC thermistor with A = 0.3602 and B = 0.09174. From these, r_{CS1} = 0.3796, r_{CS2} = 0.7195 and r_{TH} = 1.0751 can be computed. Solving for R_{TH} yields 112.05 kΩ, so when 100 kΩ is chosen, k = 0.8925. Finally, R_{CS1} and R_{CS2} are found to be 35.30 kΩ and 78.11 kΩ. Selecting the closest 1% resistor values yields a choice of 35.7 kΩ or 78.7 kΩ.

OUTPUT OFFSET

The Intel specification requires that, at no load, the nominal output voltage of the regulator be offset to a lower value than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing out of the FB pin (I_{FB}) and flowing through R_B. The value of R_B can be found using Equation 12. The closest standard 1% resistor value is 1.33 kΩ.

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}} \quad (12)$$

$$R_B = \frac{1.5\ V - 1.480\ V}{15\ \mu A} = 1.33\ k\Omega$$

C_{OUT} SELECTION

The required output decoupling for the regulator is typically recommended by Intel for various processors and platforms. One can also use some simple design guidelines to determine what is required. These guidelines are based on having both bulk and ceramic capacitors in the system.

The first thing is to select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramics is inside the socket, with 12 to 18 of size 1206 being the physical limit. Others can be placed along the outer edge of the socket as well.

The combined ceramic values of 200 µF to 300 µF are recommended, made of multiple 10 µF or 22 µF capacitors. Select the number of ceramics and find the total ceramic capacitance (C_Z).

Next, there is an upper limit imposed on the total amount of bulk capacitance (C_X) when one considers the VID on-the-fly voltage stepping of the output (voltage step V_V in time t_V), and a lower limit based on meeting the critical capacitance for load release for a given maximum load step I_{MAX}:

$$C_{X(MIN)} \geq \left(\frac{L \times I_{STEP}}{n \times R_O \times V_{VID}} - C_Z \right) \quad (13)$$

$$C_{X(MAX)} \leq \frac{L}{nK^2 R_O^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_v \frac{V_{VID}}{V_V} \times \frac{nKR_O}{L} \right)^2} - 1 \right) - C_Z$$

$$\text{where } K = 1n\left(\frac{V_{ERR}}{V_V} \right) \quad (14)$$

where R_X is the ESR of the bulk capacitor bank. To meet the transient specification, R_X cannot be greater than 3 times R_O. If the $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system does not meet the VID on-the-fly specification and may require the use of a smaller inductor or more phases (and may have to increase the switching frequency to keep the output ripple the same).

In this example, there are twelve 22 µF 1206 MLC capacitors (CZ = 264 µF). The VID-on-the-fly step change is 12.5 mV in 5 µs. Solving for the bulk capacitance, assuming that $R_X = R_O$, and where $k = 4.6$, yields

$$C_{X(MIN)} \geq \left(\frac{600\text{ nH} \times 60\text{ A}}{3 \times 1.3\text{ m}\Omega \times 1.5\text{ V}} - 230\text{ µF} \right) = 5.92\text{ mF}$$

$$C_{X(MAX)} \leq \frac{600\text{ nH} \times 250\text{ mV}}{3 \times 4.6^2 \times 1.3\text{ m}\Omega^2 \times 1.5\text{ V}} \times \left(\sqrt{1 + \left(\frac{150\text{ µs} \times 1.5\text{ V} \times 3 \times 4.6 \times 1.3\text{ m}\Omega}{450\text{ mV} \times 320\text{ nH}} \right)^2} - 1 \right) - 230\text{ µF}$$

$$= 23.9\text{ mF}$$

Using ten 560 µF OSCONs with an ESR of 12 mΩ each yields C_X = 5.6 mF with an R_X = 1.2 mΩ (making the new limits on C_X 2.4 mF to 8.8 mF, which is still within the acceptable range).

One last check should be made to ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the initial high frequency transient spike. This can be tested using

$$L_X \leq C_Z \times R_O{}^2$$
$$L_X \leq 230\text{ µF} \times 1.3\text{ m}\Omega^2 = 389\text{ pH} \quad (15)$$

In this example, L_X is 400 pH for the ten OSCSON capacitors, which satisfies this limitation. If the L_X of the chosen bulk capacitor bank is too large, the number of MLC capacitors must be increased.

Note that for this multimode control technique, all ceramic designs can be used as long as the conditions of Equations 11, 12, and 13 are satisfied.

POWER MOSFETS

For this example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G , C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3418) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} ~10 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are recommended.

The maximum output current, I_O, determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. In the ADP3181, currents are balanced between phases, so the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following expression shows the total power being dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O).

$$P_{SF} = (1 - D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (16)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, one can find the required $R_{DS(ON)}$ for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for P_{SF} is 1 W (assuming 2 D-paks) at 120°C junction temperature. Here, for example (65 A maximum), $R_{DS(SF)}$ (per MOSFET) < 8.7 mW. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C, so this must be accounted for this when making this selection.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the non-overlap dead time of the MOSFET driver (40 ns typical for the ADP3418). The output impedance of the driver is about 2 Ω, and the typical MOSFET input gate resistances are about 1 Ω – 2 Ω, so a total gate capacitance of less than 6000 pF should be adhered to. Because there are two MOSFETs in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000 pF.

The high-side (main) MOSFET has to be able to handle two main power dissipation components: conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET, where n_{MF} is the total number of main MOSFETs:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad (17)$$

Here, R_G is the total gate resistance (2 Ω for the ADP3418 and about 1 Ω for typical high speed switching MOSFETs, making R_G = 3 Ω), and C_{ISS} is the input capacitance of the main MOSFET. It is interesting to note that adding more main MOSFETs (n_{MF}) does not really help the switching loss per MOSFET because the additional gate capacitance slows down switching. The best thing to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following, where $R_{DS(MF)}$ is the on resistance of the MOSFET:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (18)$$

Typically, for main MOSFETs, one wants the highest speed (low C_{ISS}) device, but these usually have higher on resistance. One must select a device that meets the total power dissipation (about 1.5 W for a single D-PAK) when combining the switching and conduction losses.

For this example, an Infineon IPD12N03L was selected as the main MOSFET (three total; n_{MF} = 3), with a C_{ISS} = 1460 pF (max) and $R_{DS(MF)}$ = 14 mΩ (max at T_J = 120°C), and an Infineon IPD06N03L as the synchronous MOSFET (six total; n_{SF} = 6), with C_{ISS} = 2370 pF (max) and $R_{DS(SF)}$ = 8.3 mΩ (max at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 3000 pF, satisfying that requirement. Solving for the power dissipation per MOSFET at I_O = 65 A and I_R = 13 A yields 900 mW for each synchronous MOSFET and 1.6 W for each main MOSFET. These numbers work well considering that there is usually more PCB area available for each main MOSFET versus each synchronous MOSFET.

One last thing to consider is the power dissipation in the driver for each phase. This is best described in terms of the Q_G for the MOSFETs and is given by the following, where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad (19)$$

Also shown is the standby dissipation factor ($I_{CC} \times V_{CC}$) for the driver. For the ADP3418, the maximum dissipation should be less than 400 mW. For example, with I_{CC} = 7 mA, Q_{GMF} = 22.8 nC and Q_{GSF} = 34.3 nC, 260 mW is found in each driver, which is below the 400 mW dissipation limit.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. The following expression is used for determining the optimum value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad (20)$$

$$R_R = \frac{0.2 \times 600 \text{ nH}}{3 \times 5 \times 4.2 \text{ m}\Omega \times 5 \text{ pF}} = 381 \text{k}\Omega$$

where A_R is the internal ramp amplifier gain, A_D is the current balancing amplifier gain, R_{DS} is the total low-side MOSFET on resistance, and C_R is the internal ramp capacitor value. The closest standard 1% resistor value is 226 kΩ.

The internal ramp voltage magnitude can be calculated using

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (21)$$

$$V_R = \frac{0.2 \times (1 - 0.125) \times 1.5 \text{ V}}{383 \text{ k}\Omega \times 5 \text{ pF} \times 267 \text{ kHz}} = 0.51 \text{ mV}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response improve, but thermal balance degrades. Likewise, if the ramp is made smaller, thermal balance improves at the sacrifice of transient response and stability. The factor of 3 in the denominator of Equation 20 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

CURRENT LIMIT SETPOINT

To select the current limit setpoint, it is necessary to find the resistor value for R_{LIM}. The current limit threshold for the ADP3181 is set with a 3 V source (V_{LIM}) across R_{LIM} with a gain of 10 mV/μA (A_{LIM}). R_{LIM} can be found using the following:

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{I_{LIM} \times R_O} \quad (22)$$

where I_{LIM} is the average current limit for the output of the supply. For example, using 90 A for I_{LIM}, R_{LIM} is 222.2 kΩ and for which 221 kΩ can be chosen as the nearest 1% value.

The per phase current limit described earlier has its limit determined by the following:

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} + \frac{I_R}{2} \quad (23)$$

where the maximum COMP voltage ($V_{COMP(MAX)}$) is 3.3 V, the COMP pin bias voltage (V_{BIAS}) is 1.2 V, and the current balancing amplifier gain (A_D) is 5. Using V_R of 0.7 V, and $R_{DS(MAX)}$ of 5.3 mΩ (low-side on resistance at 150°C), there is a per-phase limit of 52 A.

This limit can be adjusted by changing the ramp voltage V_R, but make sure not to set the per-phase limit lower than the average per-phase current ($I_{LIM/n}$).

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3181 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion to the load current at any load current slew rate; this ensures optimal positioning and allows the minimization of the output decoupling.

With the multimode feedback structure of the ADP3181, one needs to set the feedback compensation to make the converter's output impedance working in parallel with the output decoupling meet this goal. Several poles and zeros created by the output inductor and decoupling capacitors (output filter) need to be compensated for.

A type-three compensator on the voltage feedback is adequate for proper compensation of the output filter. The following equations are intended to yield an optimal starting point for the design; some minor adjustments may be necessary to account for PCB and component parasitic effects.

Using equations 24 to 28, the first step is to compute the time constants for all of the poles and zeros in the system, where, for the ADP3181, R is the PCB resistance from the bulk capacitors to the ceramics and where R_{DS} is approximately the total low-side MOSFET on resistance per phase at 25°C. For this example, A_D is 5, V_R equals 1 V, R' is approximately 0.6 mΩ (assuming a 4-layer motherboard) and L_X is 400 pH for the 10 OSCSON capacitors.

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - n \times D) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}} \quad (24)$$

$$R_E = 3 \times 1.3\ \text{m}\Omega + 5 \times 4.2\ \text{m}\Omega + \frac{1.6\ \text{m}\Omega \times 0.63\ \text{V}}{1.5\ \text{V}} + \frac{2 \times 600\ \text{nH} \times (1 - 0.375) \times 0.63\ \text{V}}{3 \times 6.56\ \text{mF} \times 1.3\ \text{m}\Omega \times 1.5\ \text{V}} = 37.9\ \text{m}\Omega$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} = 6.56\ \text{mF} \times (1.3\ \text{m}\Omega - 0.6\ \text{m}\Omega) + \frac{375\ \text{pH}}{1.3\ \text{m}\Omega} \times \frac{1.3\ \text{m}\Omega - 0.6\ \text{m}\Omega}{1.0\ \text{m}\Omega} = 4.79\ \mu\text{s} \quad (25)$$

$$T_B = (R_X + R' - R_O) \times C_X = (1.0\ \text{m}\Omega + 0.6\ \text{m}\Omega - 1.3\ \text{m}\Omega) \times 6.56\ \text{mF} = 1.97\ \text{ns} \quad (26)$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}}\right)}{V_{VID} \times R_E} = \frac{0.63\ \text{V} \times \left(600\ \text{nH} - \frac{5 \times 4.2\ \text{m}\Omega}{2 \times 267\ \text{kHz}}\right)}{1.5\ \text{V} \times 37.9\ \text{m}\Omega} = 6.2\ \mu\text{s} \quad (27)$$

$$T_D = \frac{C_X \times C_Z \times R_O^2}{C_X \times (R_O - R') + C_Z \times R_O} = \frac{6.56\ \text{mF} \times 230\ \mu\text{F} \times 1.3\ \text{m}\Omega^2}{6.56\ \text{mF} \times (1.3\ \text{m}\Omega - 0.6\ \text{m}\Omega) + 230\ \mu\text{F} \times 1.3\ \text{m}\Omega} = 521\ \text{ns} \quad (28)$$

The compensation values can be solved using the following:

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} \quad (29)$$

$$C_A = \frac{3 \times 1.3\ \text{m}\Omega \times 4.79\ \mu\text{s}}{3.79\ \text{m}\Omega \times 1.33\ \text{k}\Omega} = 371\ \text{pF}$$

$$R_A = \frac{T_C}{C_A} = \frac{6.2\ \mu\text{s}}{371\ \text{pF}} = 16.7\ \text{k}\Omega \quad (30)$$

$$C_B = \frac{T_B}{R_B} = \frac{1.97\mu\text{s}}{1.33\,\text{k}\Omega} = 1.48\,\text{nF} \quad (31)$$

$$C_{FB} = \frac{T_D}{R_A} = \frac{521\,\text{ns}}{16.7\ \text{k}\Omega} = 31.2\ \text{pF} \quad (32)$$

Choosing the closest standard values for these components yields C_A = 820 pF, R_A = 7.87 kΩ, C_B = 1.2 nF, and CFB = 100 pF. These make a good starting point.

Using the design spreadsheet yields more optimal compensation values; from the spreadsheet, C_A = 680 pF, R_A = 5.49 kΩ, C_B = 1.2 nF, and C_{FB} = 68 pF.

C_{IN} SELECTION AND INPUT CURRENT di/dt REDUCTION

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to n × V_{OUT}/V_{IN} and an amplitude of one-nth of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{N \times D}} \quad (33)$$

$$I_{CRMS} = 0.125 \times 65\,\text{A} \times \sqrt{\frac{1}{3 \times 0.125} - 1} = 10.5\ \text{A}$$

Note that the capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 2200 µF, 16 V Nichicon capacitors with a ripple current rating of 3.5 A each.

To reduce the input-current di/dt to below the recommended maximum of 0.1 A/µs, note that an additional small inductor (L > 1 µH @ 15 A) should be inserted between the converter and the supply bus. This inductor also acts as a filter between the converter and the primary power source.

BUILDING A SWITCHABLE VR9/VR10 DESIGN

Some designs may require the ability to work with either a VR9- or a VR10-based CPU, because both processors are available in the same package/pin count. To accomplish this, the voltage regulator must detect which processor is present and set the VID DAC and load line accordingly. This can accomplished using the BOOTSELECT output from the CPU. Figure 12 shows how this signal is used to modify the load line and set the CPUID pin of the ADP3181 appropriately.

To determine the values of x and y, start with the two load lines; R_{OL} (smaller slope) and R_{OH} (larger slope). First, follow the standard design procedure, which gives the values for R_{CS1}, R_{CS2}, and C_{CS} for R_{OL}. Tune R_{PH} and C_{CS}. Next, compute the values for R_{CS3} and C_{CS3} using the following:

$$R_{CS3} = \left(\frac{R_{OH}}{R_{OL}} - 1 \right) \times R_{CS} \quad (34)$$

$$C_{CS3} = \frac{C_{CS}}{\left(\frac{R_{OH}}{R_{OL}} - 1 \right)} \quad (35)$$

where R_{OL} is 1.5 mΩ and R_{OH} is 3 mΩ.

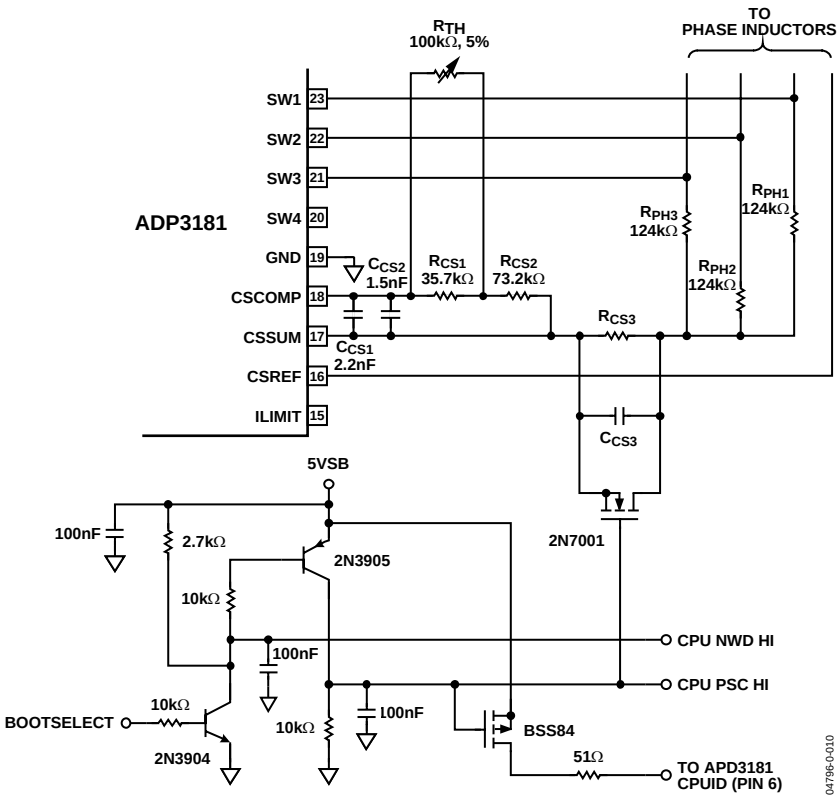

Figure 12. Connections to Allow Automatic Switching between VR9 and VR10 Operation

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

GENERAL RECOMMENDATIONS

For good results, at least a 4-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mW at room temperature.

Whenever high currents must be routed between PCB layers, use vias liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3181) must cross through the power circuitry, it is best if a signal ground plane is interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making the signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3181 for referencing the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing in it.

The components around the ADP3181 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins.

The output capacitors should be connected as closely as possible to the load (or connector) that receives the power (for example, a microprocessor core). If the load is distributed, the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop as described next.

Power Circuitry

The switching power path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path because it minimizes the inductance in the switching loop, which can cause high energy ringing, and because it accommodates the high current demand with minimal voltage loss.

Whenever a power-dissipating component (for example, a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias, and improved thermal perform-ance from vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heat sink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

Signal Circuitry

The output voltage is sensed and regulated between the FB pin and the FBRTN pin (which connects to the signal ground at the load). To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus the FB and FBRTN traces should be routed adjacent to each other atop the power ground plane back to the controller.

Connect the feedback traces from the switch nodes as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

OUTLINE DIMENSIONS

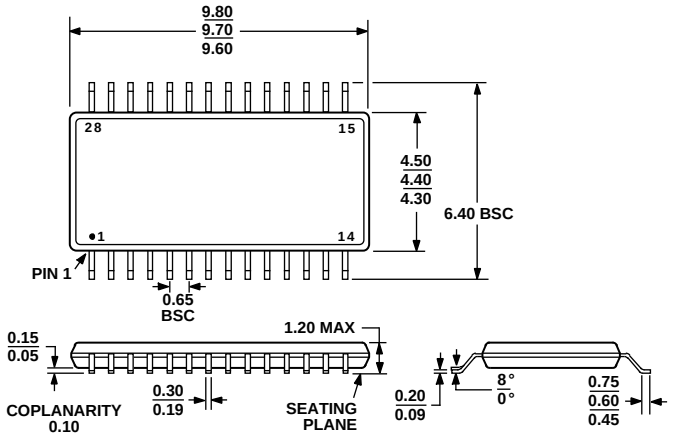

Figure 13. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Quantity per Reel
ADP3181JRUZ-REEL[1]	0°C to +85°C	Thin Shrink SO—13″ Reel	RU-28	2500

[1] Z = PB-free part.

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