# THE DATASHEET OF

# ADP3186JRUZ

www.win-source.net 0086-755-83957316

# 5-Bit Programmable 2-/3-/4-Phase Synchronous Buck Controller

# ADP3186

## FEATURES

**Selectable 2-, 3-, or 4-phase operation at up to 1 MHz per phase**

**±1% worst-case differential sensing error over temperature**

**Logic-level PWM outputs for interface to external high power drivers**

**Active current balancing between all output phases**

**Built-in power good/crowbar blanking supports on-the-fly VID code changes**

**5-bit digitally programmable 0.8 V to 1.55 V output**

**Programmable short-circuit protection with programmable latch-off delay**

## APPLICATIONS

**Desktop PC power supplies for**

**AMD Opteron™ processors**

**VRM modules**

## GENERAL DESCRIPTION

The ADP3186 is a highly efficient multiphase synchronous buck switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance AMD processors. It uses an internal 5-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.8 V and 1.55 V. It uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, or 4-phase operation, allowing the construction of up to four complementary buck switching stages.

The ADP3186 includes programmable no-load offset and slope functions to adjust the output voltage as a function of the load current, so that it is always optimally positioned for a system transient. The ADP3186 also provides accurate and reliable short-circuit protection, adjustable current limiting, and a power good output that accommodates on-the-fly output voltage changes requested by the CPU.

The ADP3186 is specified over the commercial temperature range of 0°C to 85°C and is available in 28-lead TSSOP and QSOP packages.

## FUNCTIONAL BLOCK DIAGRAM

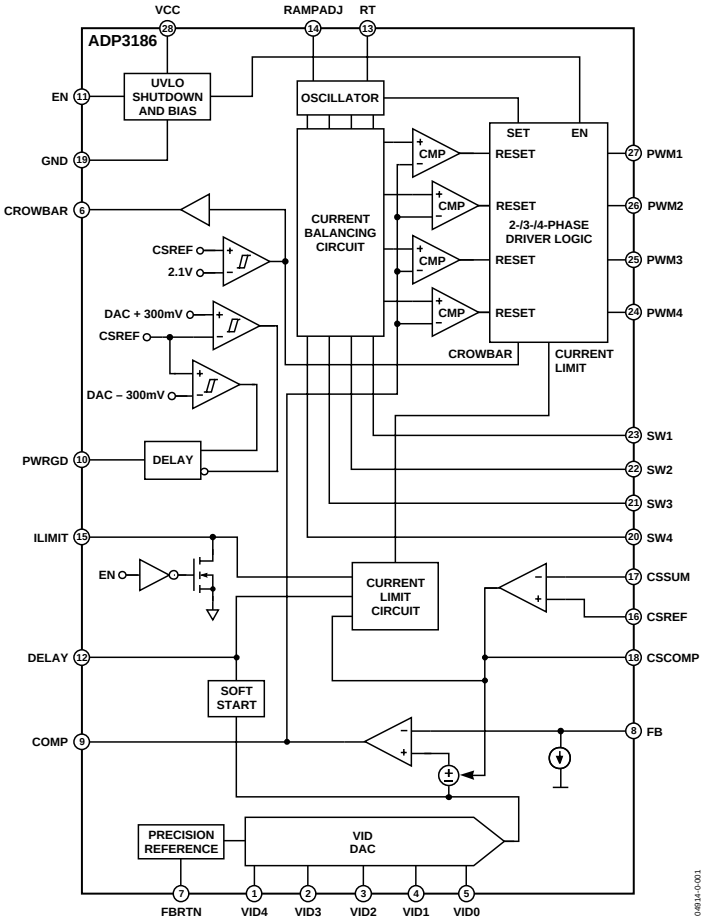


*Figure 1.*

**Rev. A**

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## REVISION HISTORY

**3/06—Rev. 0 to Rev. A**

Updated ADP3110 to ADP3110A ... Universal
Changes to Table 1 ... 3
Added QSOP Package ... 24
Updated Ordering Guide ... 24

**8/04—Revision Sp0: Initial Version**

# SPECIFICATIONS

VCC = 12 V, FBRTN = GND, $T_A$ = 0°C to 85°C, unless otherwise specified.[1]

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ERROR AMPLIFIER | | | | | | |
| Output Voltage Range[2] | $V_{COMP}$ | | 0.5 | | 3.5 | V |
| Accuracy | $V_{FB}$ | | | | | |
| 0.8 V Output | | Referenced to FBRTN, CSSUM = CSCOMP, Figure 2 | | | | |
| | | TSSOP | 0.7920 | | 0.8080 | V |
| | | QSOP | 0.7880 | | 0.8120 | V |
| 1.175 V Output | | Referenced to FBRTN, CSSUM = CSCOMP, Figure 2 | | | | |
| | | TSSOP | 1.1633 | | 1.1868 | V |
| | | QSOP | 1.1574 | | 1.1926 | V |
| 1.55 V Output | | Referenced to FBRTN, CSSUM = CSCOMP, Figure 2 | | | | |
| | | TSSOP | 1.5345 | | 1.5655 | V |
| | | QSOP | 1.5268 | | 1.5733 | V |
| Line Regulation | $\Delta V_{FB}$ | VCC = 10 V to 14 V | | 0.05 | | % |
| Input Bias Current | $I_{FB}$ | | −13 | −15.5 | −17 | μA |
| FBRTN Current | $I_{FBRTN}$ | | | 100 | 200 | μA |
| Output Current | $I_{O(ERR)}$ | FB Forced to $V_{OUT}$ − 3% | | 500 | | μA |
| Gain Bandwidth Product | $GBW_{(ERR)}$ | COMP = FB | | 20 | | MHz |
| Slew Rate | | $C_{COMP}$ = 10 pF | | 25 | | V/μs |
| VID INPUTS | | | | | | |
| Input Low Voltage | $V_{IL(VID)}$ | | | | 0.8 | V |
| Input High Voltage | $V_{IH(VID)}$ | | 1.5 | | | V |
| Input Current, Input Voltage Low | $I_{IL(VID)}$ | VID(X) = 0 V | | 20 | 26 | μA |
| Pull-Up Resistance | $R_{VID}$ | | 100 | 120 | | kΩ |
| Internal Pull-Up Voltage | | | 2.0 | 2.4 | 2.65 | V |
| VID Transition Delay Time[2] | | VID code change to FB change | 400 | | | ns |
| No CPU Detection Turn-Off Delay Time[2] | | VID code change to 11111 to PWM going low | 400 | | | ns |
| OSCILLATOR | | | | | | |
| Frequency Range[2] | $f_{OSC}$ | | 0.25 | | 4 | MHz |
| Frequency Variation | $f_{PHASE}$ | $T_A$ = 25°C, $R_T$ = 250 kΩ, 4-phase | 155 | 200 | 245 | kHz |
| | | $T_A$ = 25°C, $R_T$ = 115 kΩ, 4-phase | | 400 | | kHz |
| | | $T_A$ = 25°C, $R_T$ = 75 kΩ, 4-phase | | 600 | | kHz |
| Output Voltage | $V_{RT}$ | $R_T$ = 100 kΩ to GND | 1.9 | 2.0 | 2.1 | V |
| Timing Resistor Value | | | | | 500 | kΩ |
| RAMPADJ Output Voltage | $V_{RAMPADJ}$ | RAMPADJ − FB | −50 | | +50 | mV |
| RAMPADJ Input Current Range | $I_{RAMPADJ}$ | | 0 | | 50 | μA |
| CURRENT SENSE AMPLIFIER | | | | | | |
| Offset Voltage | $V_{OS(CSA)}$ | CSSUM − CSREF, Figure 3 | | | | |
| | | TSSOP | −3 | | +3 | mV |
| | | QSOP | −3.5 | | +3.5 | mV |
| Input Bias Current | $I_{BIAS(CSSUM)}$ | | −50 | | +50 | nA |
| Gain Bandwidth Product | $GBW_{(CSA)}$ | | | 10 | | MHz |
| Slew Rate | | $C_{CSCOMP}$ = 10 pF | | 10 | | V/μs |
| Input Common-Mode Range | | CSSUM and CSREF | 0 | | 2.7 | V |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Positioning Accuracy | $\Delta V_{FB}$ | Figure 4 | −77 | −80 | −83 | mV |
| Output Voltage Range | | | 0.05 | | 2.7 | V |
| Output Current | $I_{CSCOMP}$ | | | 500 | | μA |
| CURRENT BALANCE CIRCUIT | | | | | | |
| Common-Mode Range | $V_{SW(X)CM}$ | | −600 | | +200 | mV |
| Input Resistance | $R_{SW(X)}$ | SW(X) = 0 V | 20 | 30 | 40 | kΩ |
| Input Current | $I_{SW(X)}$ | SW(X) = 0 V | 4 | 7 | 10 | μA |
| Input Current Matching | $\Delta I_{SW(X)}$ | SW(X) = 0 V | −5 | | +5 | % |
| CURRENT LIMIT COMPARATOR | | | | | | |
| Output Voltage | | | | | | |
| Normal Mode | $V_{ILIMIT(NM)}$ | EN > 2.0 V, $R_{ILIMIT}$ = 250 kΩ | 2.9 | 3 | 3.1 | V |
| Shutdown Mode | $V_{ILIMIT(SD)}$ | EN < 0.8 V, $I_{ILIMIT}$ = −100 μA | | | 400 | mV |
| Output Current, Normal Mode | $I_{ILIMIT(NM)}$ | EN > 2.0 V, $R_{ILIMIT}$ = 250 kΩ | | 12 | | μA |
| Maximum Output Current[2] | | | 60 | | | μA |
| Current Limit Threshold Voltage | $V_{CL}$ | $V_{CSREF} - V_{CSCOMP}$, $R_{ILIMIT}$ = 250 kΩ | 105 | 125 | 145 | mV |
| Current Limit Setting Ratio | | $V_{CL}/I_{ILIMIT}$ | | 10.4 | | mV/μA |
| DELAY Normal Mode Voltage | $V_{DELAY(NM)}$ | $R_{DELAY}$ = 250 kΩ | 2.9 | 3 | 3.1 | V |
| DELAY Overcurrent Threshold | $V_{DELAY(OC)}$ | $R_{DELAY}$ = 250 kΩ | 1.7 | 1.8 | 1.9 | V |
| Latch-Off Delay Time | $t_{DELAY}$ | $R_{DELAY}$ = 250 kΩ, $C_{DELAY}$ = 12 nF | | 1.5 | | ms |
| SOFT START | | | | | | |
| Output Current, Soft Start Mode | $I_{DELAY(SS)}$ | During startup, DELAY < 2.8 V | 15 | 20 | 25 | μA |
| Soft Start Delay Time | $t_{DELAY(SS)}$ | $R_{DELAY}$ = 250 kΩ, $C_{DELAY}$ = 12 nF, VID code = 011111 | | 1 | | ms |
| ENABLE INPUT | | | | | | |
| Input Low Voltage | $V_{IL(EN)}$ | | | | 0.8 | V |
| Input High Voltage | $V_{IH(EN)}$ | | 2.0 | | | V |
| Input Current, Input Voltage Low | $I_{IL(EN)}$ | EN = 0 V | −1 | | +1 | μA |
| POWER GOOD COMPARATOR | | | | | | |
| Undervoltage Threshold | $V_{PWRGD(UV)}$ | Relative to nominal DAC output | −200 | −300 | −400 | mV |
| Overvoltage Threshold | $V_{PWRGD(OV)}$ | Relative to nominal DAC output | 200 | 300 | 400 | mV |
| Output Low Voltage | $V_{OL(PWRGD)}$ | $I_{PWRGD(SINK)}$ = 4 mA | | 150 | 400 | mV |
| OFF_State Leakage Current | | $V_{CSREF} = V_{DAC}$ | | | 50 | μA |
| Power Good Delay Time | | | | | | |
| VID Code Changing | | | 100 | 250 | | μs |
| VID Code Static | | | | 200 | | ns |
| Crowbar Trip Point | $V_{CROWBAR}$ | | 2.0 | 2.1 | 2.2 | V |
| Crowbar Reset Point | | | 300 | 400 | 500 | mV |
| Crowbar Delay Time | $t_{CROWBAR}$ | Overvoltage to PWM going low | | | | |
| VID Code Changing | | | 100 | 250 | | μs |
| VID Code Static | | | | 400 | | ns |
| PWM OUTPUTS | | | | | | |
| Output Low Voltage | $V_{OL(PWM)}$ | $I_{PWM(SINK)}$ = −400 μA | | 160 | 500 | mV |
| Output High Voltage | $V_{OH(PWM)}$ | $I_{PWM(SOURCE)}$ = +400 μA | 4.0 | 5 | | V |
| SUPPLY | | | | | | |
| DC Supply Current | | | | 5 | 10 | mA |
| UVLO Threshold Voltage | $V_{UVLO}$ | VCC rising | 6.5 | 6.9 | 7.3 | V |
| UVLO Hysteresis | | | 0.7 | 0.9 | 1.1 | V |

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or bench characterization, not production tested.

# TEST CIRCUITS

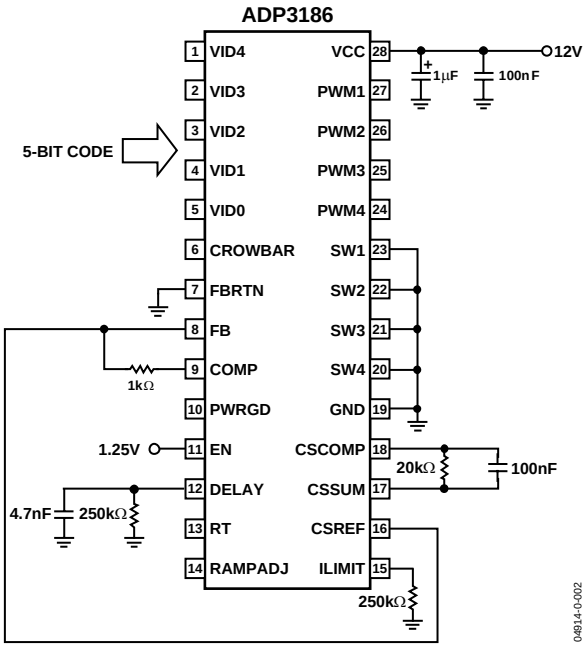



*Figure 2. Closed-Loop Output Voltage Accuracy*

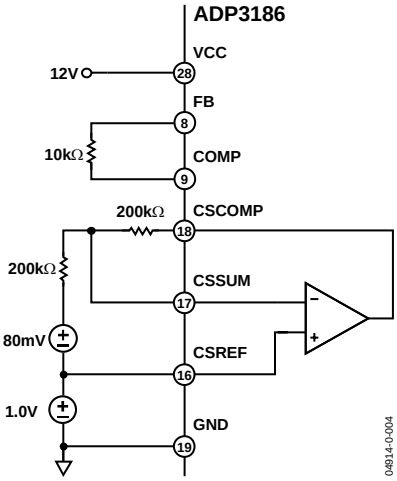



*Figure 4. Positioning Voltage*

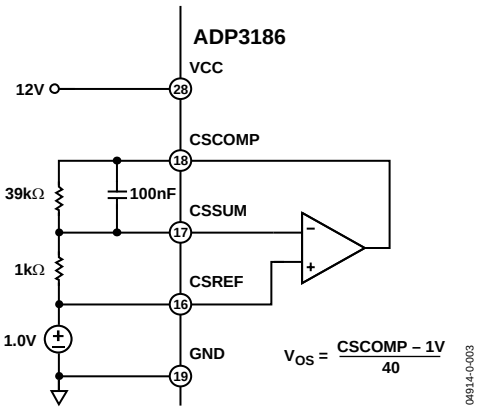



*Figure 3. Current Sense Amplifier, $V_{OS}$*

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| VCC | −0.3 V to +15 V |
| FBRTN | −0.3 V to +0.3 V |
| VID0 – VID4, EN, DELAY, ILIMIT, CSCOMP, RT, PWM1–PWM4, COMP, CROWBAR | −0.3 V to +5.5 V |
| SW1–SW4 | −5 V to +25 V |
| All Other Inputs and Outputs | −0.3 V to VCC + 0.3 V |
| Storage Temperature | −65°C to +150°C |
| Operating Ambient Temperature Range | 0°C to 85°C |
| Operating Junction Temperature | 125°C |
| Thermal Impedance ($\theta_{JA}$) | 100°C/W |
| Lead Temperature | |
| Soldering (10 sec) | 300°C |
| Infrared (15 sec) | 260°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages re referenced to GND.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

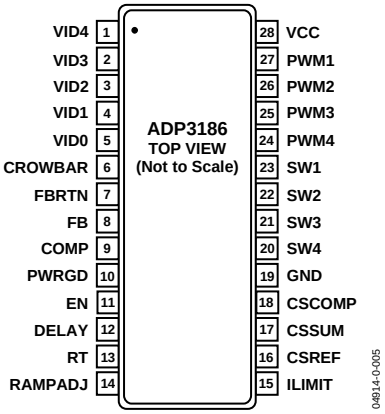



*Figure 5. Pin Configuration*

**Table 3. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 to 5 | VID4 to VID0 | Voltage Identification DAC Inputs. These five pins are pulled up to an internal reference, providing a Logic 1, if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.8 V to 1.55 V (see Table 4). Leaving all the VID pins open results in the ADP3186 going into No CPU mode, shutting off its PWM outputs and pulling the PWRGD output low. |
| 6 | CROWBAR | Crowbar Output. This logic-level output can be used to control an external device to short the 12 V supply to ground to protect the CPU from overvoltage, if CSREF exceeds 2.1 V. |
| 7 | FBRTN | Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage. |
| 8 | FB | Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no-load offset point. |
| 9 | COMP | Error Amplifier Output and Compensation Point. |
| 10 | PWRGD | Power Good Output. Open-drain output that signals when the output voltage is outside the proper operating range. |
| 11 | EN | Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low. |
| 12 | DELAY | Soft Start Delay and Current Limit Latch-Off Delay Setting Input. An external resistor and capacitor connected between this pin and GND sets the soft start ramp-up time and the overcurrent latch-off delay time. |
| 13 | RT | Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device. |
| 14 | RAMPADJ | PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp. |
| 15 | ILIMIT | Current Limit Setpoint/Enable Output. An external resistor from this pin to GND sets the current limit threshold of the converter. This pin is actively pulled low when the ADP3186 EN input is low, or when VCC is below its UVLO threshold, to signal to the driver IC that the driver high-side and low-side outputs should go low. |
| 16 | CSREF | Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power good and crowbar functions. This pin should be connected to the common point of the output inductors. |
| 17 | CSSUM | Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current. |
| 18 | CSCOMP | Current Sense Compensation Point. A resistor and a capacitor from this pin to CSSUM determine the slope of the load line and the positioning loop response time. |
| 19 | GND | Ground. All internal biasing and the logic output signals of the device are referenced to this ground. |
| 20 to 23 | SW4 to SW1 | Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open. |
| 24 to 27 | PWM4 to PMW1 | Logic-Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3110A. Connecting the PWM3 and/or PWM4 outputs to GND causes that phase to turn off, allowing the ADP3186 to operate as a 2-, 3-, or 4-phase controller. |
| 28 | VCC | Supply Voltage for the Device. |

# TYPICAL PERFORMANCE CHARACTERISTICS

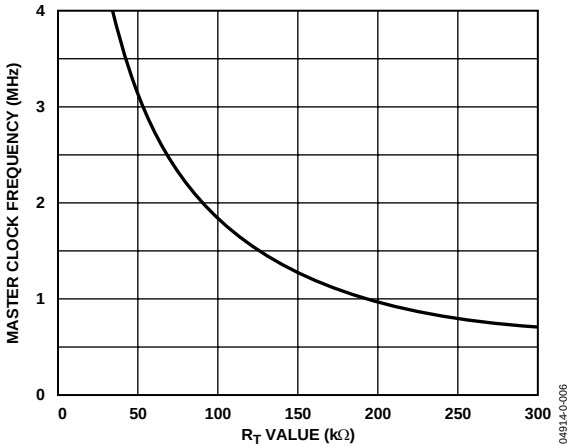



*Figure 6. Master Clock Frequency vs. $R_T$*

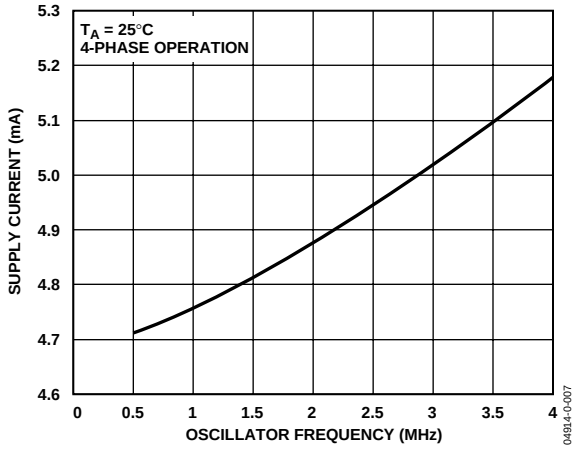



*Figure 7. Supply Current vs. Oscillator Frequency*

# THEORY OF OPERATION

The ADP3186 combines a multimode, fixed frequency PWM control with multiphase logic outputs for use in 2-, 3-, and 4-phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with AMD Opteron CPUs. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter places high thermal demands on the components in the system such as the inductors and MOSFETs.

The multimode control of the ADP3186 ensures a stable, high performance topology for

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses due to lower frequency operation
- Tight loadline regulation and accuracy
- High current output for up to 4-phase operation
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

## START-UP SEQUENCE

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP3186 operates as a 4-phase PWM controller. Grounding the PWM4 pin programs 3-phase operation and grounding the PWM3 and PWM4 pins programs 2-phase operation.

When the ADP3186 is enabled, the controller outputs a voltage on PWM3 and PWM4 that is approximately 675 mV. An internal comparator checks each pin's voltage versus a threshold of 300 mV. If the pin is grounded, it is below the threshold and the phase is disabled. The output resistance of the PWM pin is approximately 5 kΩ during this detection time. Any external pull-down resistance connected to the PWM pin should not be less than 25 kΩ to ensure proper operation. PWM1 and PWM2 are disabled during the phase detection interval, which occurs during the first two clock cycles of the internal oscillator. After this time, if the PWM output is not grounded, the 5 kΩ resistance is removed and it switches between 0 V and 5 V. If the PWM output was grounded, it remains off.

The PWM outputs are logic-level devices intended for driving external gate drivers such as the ADP3110A. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at the same time for overlapping phases.

## MASTER CLOCK FREQUENCY

The clock frequency of the ADP3186 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 6. To determine the frequency per phase, the clock is divided by the number of phases in use. If PWM4 is grounded, then divide the master clock by 3 for the frequency of the remaining phases. If PWM3 and PWM4 are grounded, then divide by 2. If all phases are in use, divide by 4.

## OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3186 combines differential sensing with a high accuracy VID DAC and reference and a low offset error amplifier. This maintains a worst-case specification of ±1% differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN should be connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

## OUTPUT CURRENT SENSING

The ADP3186 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning versus load current and for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low-side MOSFET. This amplifier can be configured several ways depending on the objectives of the system:

- Output inductor DCR sensing without a thermistor for lowest cost
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature
- Sense resistors for highest accuracy measurements

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output inductors) to the inverting input, CSSUM.

The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor to set the load line required by the microprocessor. The current information is then given as the difference of CSREF minus CSCOMP. This difference signal is used internally to offset the VID DAC for voltage positioning and as a differential input for the current limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors so that it can be made extremely accurate.

## ACTIVE IMPEDANCE CONTROL MODE

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the CSCOMP pin can be scaled to equal the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This differs from previous implementations and allows enhanced feed-forward response.

## CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3186 has individual inputs for each phase, which are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system, which has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning described previously.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. Detailed information about programming the ramp is given in the Application Information section.

External resistors can be placed in series with individual phases to create, if desired, an intentional current imbalance such as when one phase may have better cooling and can support higher currents. Resistors RSW1 through RSW4 (see the typical application circuit in Figure 10) can be used for adjusting thermal balance. It is best to have the ability to add these resistors during the initial design, so make sure that placeholders are provided in the layout.

To increase the current in any given phase, make $R_{SW}$ for that phase larger (make $R_{SW}$ = 0 for the hottest phase and do not change during balancing). Increasing $R_{SW}$ to only 500 Ω substantially increases the phase current. Increase each $R_{SW}$ value by small amounts to achieve balance, starting with the coolest phase first.

## VOLTAGE CONTROL MODE

A high gain-bandwidth voltage-mode error amplifier is used for the voltage-mode control loop. The control input voltage to the positive input is set via the VID logic, according to the voltages listed in Table 4. This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with a resistor ($R_B$) and is used for sensing and controlling the output voltage at this point. A current source from the FB pin flowing through $R_B$ is used for setting the no-load offset voltage from the VID voltage. The no-load voltage is positive with respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP.

## SOFT START

The power-on ramp-up time of the output voltage is set with a capacitor and resistor in parallel from the DELAY pin to ground. The RC time constant also determines the current limit latch-off time, as explained in the Current Limit, Short-Circuit, and Latch-Off Protection section. In UVLO or when EN is a logic low, the DELAY pin is held at ground. After the UVLO thresh-hold is reached and EN is a logic high, the DELAY capacitor is charged with an internal 20 μA current source. The output voltage follows the ramping voltage on the DELAY pin, limiting the inrush current. The soft start time depends on the value of VID DAC and $C_{DLY}$, with a secondary effect from $R_{DLY}$. See the Application Information section for details on setting $C_{DLY}$.

If EN is taken low or VCC drops below UVLO, the DELAY capacitor is reset to ground to be ready for another soft start cycle. Figure 8 shows a typical soft start sequence for the ADP3186.

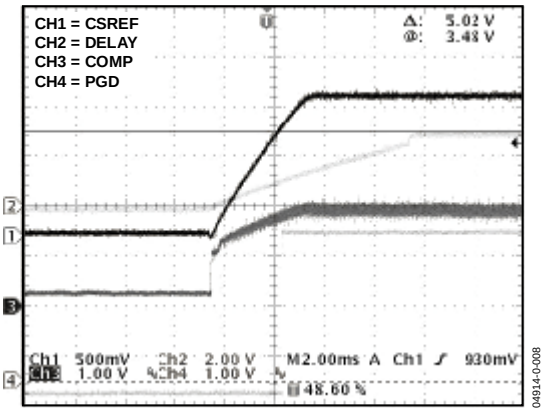



*Figure 8. Typical Start-Up Waveforms—Channel 1: PWRGD, Channel 2: CSREF, Channel 3: DELAY, Channel 4: COMP*

## CURRENT LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3186 compares a programmable current-limit setpoint to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3 V. The current through the external resistor is internally scaled to give a current limit threshold of 10.4 mV/μA. If the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

After the limit is reached, the 3 V pull-up on the DELAY pin is disconnected and the external delay capacitor is discharged through the external resistor. A comparator monitors the DELAY voltage and shuts off the controller when the voltage drops below 1.8 V. The current limit latch-off delay time is, therefore, set by the RC time constant discharging from 3 V to 1.8 V. The Application Information section discusses the selection of $C_{DLY}$ and $R_{DLY}$.

Because the controller continues to cycle the phases during the latch-off delay time, if the short is removed before the 1.8 V threshold is reached, the controller returns to normal operation. The recovery characteristic depends on the state of PWRGD. If the output voltage is within the PWRGD window, the controller resumes normal operation. However, if short circuit has caused the output voltage to drop below the PWRGD threshold, a soft start cycle is initiated.

The latch-off function can be reset by either removing and reapplying VCC to the ADP3186, or by pulling the EN pin low for a short time. To disable the short circuit latch-off function, the external resistor to ground should be left open, and a high-value (>1 MΩ) resistor should be connected from DELAY to VCC. This prevents the DELAY capacitor from discharging, so the 1.8 V threshold is never reached.

The resistor has an impact on the soft start time, because the current through it adds to the internal 20 μA current source.

During startup when the output voltage is below 200 mV, a secondary current limit is active. This is necessary, because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 2 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry.

An inherent per phase current limit protects individual phases, if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

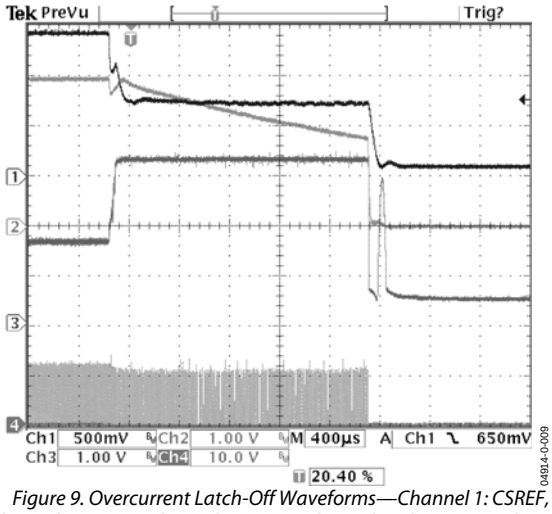



*Figure 9. Overcurrent Latch-Off Waveforms—Channel 1: CSREF, Channel 2: DELAY, Channel 3: COMP, Channel 4: Phase 1 Switch Node*

## DYNAMIC VID

The ADP3186 has the ability to dynamically change the VID input while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID input changes state, the ADP3186 detects the change and ignores the DAC inputs for a minimum of 400 ns. This time prevents a false code due to logic skew while the five VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 100 μs to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

**Table 4. VID Codes for the ADP3186**

| VID4 | VID3 | VID2 | VID1 | VID0 | Output |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | No CPU |
| 1 | 1 | 1 | 1 | 0 | 0.800 V |
| 1 | 1 | 1 | 0 | 1 | 0.825 V |
| 1 | 1 | 1 | 0 | 0 | 0.850 V |
| 1 | 1 | 0 | 1 | 1 | 0.875 V |
| 1 | 1 | 0 | 1 | 0 | 0.900 V |
| 1 | 1 | 0 | 0 | 1 | 0.925 V |
| 1 | 1 | 0 | 0 | 0 | 0.950 V |
| 1 | 0 | 1 | 1 | 1 | 0.975 V |
| 1 | 0 | 1 | 1 | 0 | 1.000 V |
| 1 | 0 | 1 | 0 | 1 | 1.025 V |
| 1 | 0 | 1 | 0 | 0 | 1.050 V |
| 1 | 0 | 0 | 1 | 1 | 1.075 V |
| 1 | 0 | 0 | 1 | 0 | 1.100 V |
| 1 | 0 | 0 | 0 | 1 | 1.125 V |
| 1 | 0 | 0 | 0 | 0 | 1.150 V |
| 0 | 1 | 1 | 1 | 1 | 1.175 V |
| 0 | 1 | 1 | 1 | 0 | 1.200 V |
| 0 | 1 | 1 | 0 | 1 | 1.225 V |
| 0 | 1 | 1 | 0 | 0 | 1.250 V |
| 0 | 1 | 0 | 1 | 1 | 1.275 V |
| 0 | 1 | 0 | 1 | 0 | 1.300 V |
| 0 | 1 | 0 | 0 | 1 | 1.325 V |
| 0 | 1 | 0 | 0 | 0 | 1.350 V |
| 0 | 0 | 1 | 1 | 1 | 1.375 V |
| 0 | 0 | 1 | 1 | 0 | 1.400 V |
| 0 | 0 | 1 | 0 | 1 | 1.425 V |
| 0 | 0 | 1 | 0 | 0 | 1.450 V |
| 0 | 0 | 0 | 1 | 1 | 1.475 V |
| 0 | 0 | 0 | 1 | 0 | 1.500 V |
| 0 | 0 | 0 | 0 | 1 | 1.525 V |
| 0 | 0 | 0 | 0 | 0 | 1.550 V |

## POWER GOOD MONITORING

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the specifications in Table 4 based on the VID voltage setting. PWRGD goes low if the output voltage is outside this specified range, if all the VID DAC inputs are high, or whenever the EN pin is pulled low. PWRGD is blanked during a VID OTF event for a period of 100 μs to prevent false signals during the time the output is changing.

## OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) and the CROWBAR logic output goes high when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 400 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output over-voltage is due to a short in the high-side MOSFET, this action current-limits the input supply or blows its fuse, protecting the microprocessor from destruction.

The CROWBAR output can be used to signal an external input crowbar or other protection circuit.

## OUTPUT ENABLE AND UVLO

For the ADP3186 to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold, and the EN pin must be higher than its logic threshold. If UVLO is less than the threshold or the EN pin is a logic low, the ADP3186 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the ILIMIT pin at ground.

In the application circuit, the ILIMIT pin should be connected to the $\overline{OD}$ pins of the ADP3110A. The ILIMIT being grounded disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs were not disabled, a negative voltage could be generated during output due to the high current discharge of the output capacitors through the inductors.

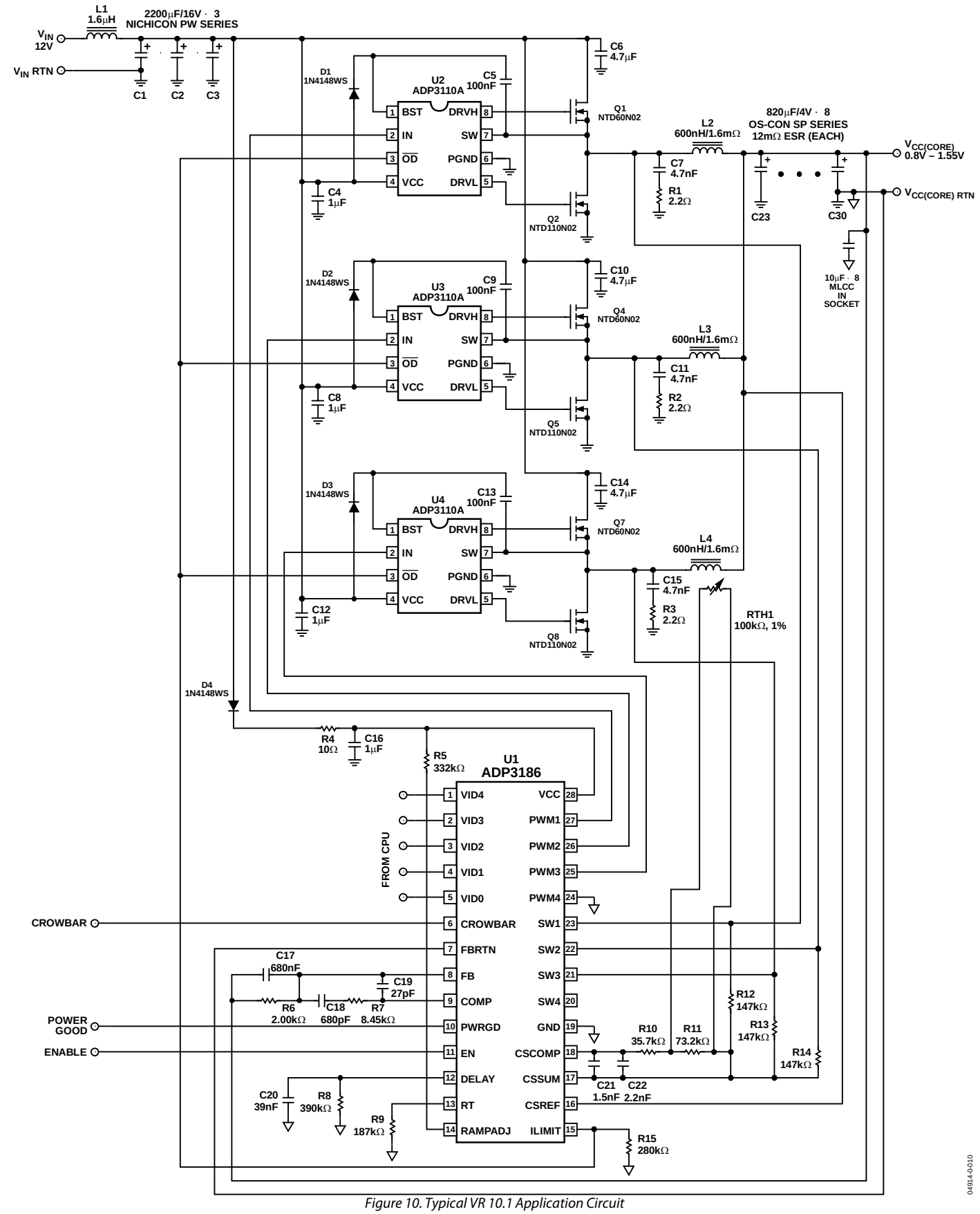



*Figure 10. Typical VR 10.1 Application Circuit*

# APPLICATION INFORMATION

The design parameters for a typical AMD Opteron CPU application are as follows:

- Input voltage ($V_{IN}$) = 12 V
- VID setting voltage ($V_{VID}$) = 1.500 V
- Duty cycle (D) = 0.125
- Maximum static output voltage error ($\pm V_{SRER}$) = ±50 mV
- Maximum dynamic output voltage error ($\pm V_{DRER}$) = ±70 mV
- Error voltage allowed for controller and ripple ($\pm V_{RERR}$) = ±20 mV
- Maximum output current ($I_O$) = 56 A
- Maximum output current step ($\Delta I_O$) = 24 A
- Static output drop resistance ($R_O$) based on
  1. No load output voltage set at upper output voltage limit.
     $V_{ONL} = V_{VID} + V_{SERR} - V_{RERR} = 1.530$ V
  2. Full load output voltage set at lower output voltage limit.
     $V_{OFL} = V_{VID} - V_{SERR} + V_{RERR} = 1.470$ V
  3. $R_O = (V_{ONL} - V_{OFL})/I_O = (1.53\text{ V} - 1.47\text{ V})/56\text{ A} = 1.1\text{ m}\Omega$
- Dynamic output drop resistance ($R_{OD}$) based on
  1. Output current step to no load with output voltage set at upper output dynamic voltage limit.
     $V_{ONLD} = V_{VID} + V_{DERR} - V_{RERR} = 1.550$ V
  2. Output voltage prior to load change (at $I_{OUT} = \Delta I_O$).
     $V_{OL} = V_{ONL} - (\Delta I_O \times R_O) = 1.504$ V
  3. $R_{OD} = (V_{ONLD} - V_{OL})/\Delta I_O = (1.55\text{ V} - 1.504\text{ V})/24\text{ A} = 1.9\text{ m}\Omega$
- Number of phases (n) = 3
- Switching frequency per phase ($f_{SW}$) = 330 kHz

## SETTING THE CLOCK FREQUENCY

The ADP3186 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor ($R_T$). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses, and the sizes of the inductors, and the sizes of the input and output capacitors. With n = 3 for three phases, a clock frequency of 990 kHz sets the switching frequency ($f_{SW}$) of each phase to 330 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. Figure 6 shows that, to achieve an 990 kHz oscillator frequency, the correct value for $R_T$ is 187 kΩ.

Alternatively, the value for $R_T$ can be calculated using

$$R_T = \frac{1}{n \times f_{SW} \times 4.7\text{ pF}} - 27\text{ k}\Omega \quad (1)$$

where 4.7 pF and 27 kΩ are internal IC component values. For good initial accuracy and frequency stability, a 1% resistor is recommended.

## SOFT START AND CURRENT LIMIT LATCH-OFF DELAY TIMES

Because the soft start and current limit latch-off delay functions share the DELAY pin, these two parameters must be considered together. The first step is to set $C_{DLY}$ for the soft start ramp. This ramp is generated with a 20 µA internal current source. The value of $R_{DLY}$ has a second-order impact on the soft start time, because it sinks part of the current source to ground. However, as long as $R_{DLY}$ is kept greater than 200 kΩ, this effect is minor. The value for $C_{DLY}$ can be approximated using

$$C_{DLY} = \left(20\ \mu\text{A} - \frac{V_{VID}}{2 \times R_{DLY}}\right) \times \frac{t_{SS}}{V_{VID}} \quad (2)$$

where $t_{SS}$ is the desired soft start time. Assuming an $R_{DLY}$ of 390 kΩ and a desired soft start time of 3 ms, $C_{DLY}$ is 36 nF. The closest standard value for $C_{DLY}$ is 39 nF. Once $C_{DLY}$ is chosen, $R_{DLY}$ can be calculated for the current limit latch-off time using

$$R_{DLY} = \frac{1.96 \times t_{DELAY}}{C_{DLY}} \quad (3)$$

If the result for $R_{DLY}$ is less than 200 kΩ, a smaller soft start time should be considered by recalculating the equation for $C_{DLY}$, or a longer latch-off time should be used. $R_{DLY}$ should never be less than 200 kΩ. In this example, a delay time of 8 ms results in $R_{DLY}$ equal to 402 kΩ. The closest standard 5% value is 390 kΩ.

## INDUCTOR SELECTION

The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs, but allows using smaller inductors and, for a specified peak-to-peak transient deviation, less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger inductors and more output capacitance for the same peak-to-peak transient deviation. In any multiphase converter, a practical value for the peak-to-peak inductor ripple current is less than 50% of the maximum dc current in the same inductor. Equation 4 shows the relationships among the inductance, oscillator frequency, and peak-to-peak ripple current in the inductor.

Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times (1 - D)}{f_{SW} \times L} \quad (4)$$

$$L \geq \frac{V_{VID} \times R_{OD} \times (1 - (n \times D))}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

Solving Equation 5 for a 10 mV p-p output ripple voltage yields

$$L \geq \frac{1.5\ \text{V} \times 1.9\ \text{m}\Omega \times (1 - 0.375)}{330\ \text{kHz} \times 10\ \text{mV}} = 540\ \text{nH}$$

If the resulting ripple voltage is less than that designed for, the inductor can be made smaller until the ripple value is met. This allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 600 nH inductor is a good starting point and gives a calculated ripple current of 6.6 A. The inductor should not saturate at the peak current of 22 A and should be able to handle the sum of the power dissipation caused by the average current of 18.7 A in the winding and core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the phase currents. A large DCR can cause excessive power losses, while too small a value can lead to increased measurement error. A good rule is to have the DCR be about 1 to 1½ times the droop resistance ($R_O$). The example uses an inductor with a DCR of 1.6 mΩ.

## DESIGNING AN INDUCTOR

Once the inductance and DCR are known, the next step is to either design an inductor or to find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to control the accuracy of the system. 20% inductance and 8% DCR (at room temperature) are reasonable tolerances that most manufacturers can meet.

The first decision in designing the inductor is to choose the core material. Several possibilities for providing low core loss at high frequencies include the powder cores (for example, Kool-Mμ® from Magnetics, Inc. or from Micrometals) and the gapped soft ferrite cores (for example, 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

The best choice for a core geometry is a closed-loop type such as a potentiometer core, PQ, U, E core, or toroid. A good compromise between price and performance is a core with a toroidal shape.

Many useful magnetics design references are available for quickly designing a power inductor, such as

- Magnetic Designer Software
  Intusoft (www.intusoft.com)
- *Designing Magnetic Components for High-Frequency DC-DC Converters*, by William T. McLyman, Kg Magnetics, Inc., ISBN 1883107008

### *Selecting a Standard Inductor*

The following power inductor manufacturers can provide design consultation and deliver power inductors optimized for high power applications upon request:

- Coilcraft
  (847) 639-6400
  www.coilcraft.com
- Coiltronics
  (561) 752-5000
  www.coiltronics.com
- Sumida Corporation
  (510) 668-0660
  www.sumida.com
- Vishay
  (402) 563-6866
  www.vishay.com

## OUTPUT DROOP RESISTANCE

The design requires that the regulator output voltage measured at the CPU pins drop when the output current increases. The specified voltage drop corresponds to the static output droop resistance ($R_O$).

The output current is measured by summing the voltage across each inductor and passing the signal through a low-pass filter. This summer filter is the CS amplifier configured with resistors $R_{PH(X)}$ (summers), and $R_{CS}$ and $C_{CS}$ (filter). The output resistance of the regulator is set by the following equations, where $R_L$ is the DCR of the output inductors:

$$R_O = \frac{R_{CS}}{R_{PH(x)}} \times R_L \quad (6)$$

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \quad (7)$$

One has the flexibility of choosing either $R_{CS}$ or $R_{PH(X)}$. It is best to select $R_{CS}$ equal to 100 kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 6:

$$R_{PH(x)} = \frac{R_L}{R_O} \times R_{CS}$$

$$R_{PH(x)} = \frac{1.6\ \text{m}\Omega}{1.1\ \text{m}\Omega} \times 100\ \text{k}\Omega = 145.5\ \text{k}\Omega$$

Next, use Equation 6 to solve for $C_{CS}$.

$$C_{CS} = \frac{600\ \text{nH}}{1.6\ \text{m}\Omega \times 100\ \text{k}\Omega} = 3.75\ \text{nF}$$

It is best to have a dual location for $C_{CS}$ in the layout, so that standard values can be used in parallel to get as close as possible to the value desired. For best accuracy, $C_{CS}$ should be a 5% or 10% NPO capacitor. This example uses a 5% combination for $C_{CS}$ of 1.5 nF and 2.2 nF in parallel. Recalculating $R_{PH(X)}$ using this capacitor combination yields a 1% value of 147 kΩ.

## INDUCTOR DCR TEMPERATURE CORRECTION

When the inductor's DCR is used as the sense element and copper wire is the source of the DCR, one needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If $R_{CS}$ is designed to have an opposite and equal percentage change in resistance to that of the wire, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, resistors $R_{CS1}$ and $R_{CS2}$ are needed. See Figure 11 to linearize the NTC and produce the desired temperature tracking.

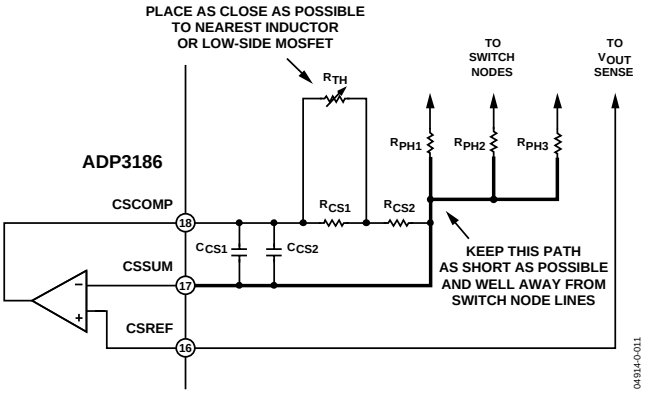



*Figure 11. Temperature Compensation Circuit Values*

The following procedure and expressions yield values to use for $R_{CS1}$, $R_{CS2}$, and $R_{TH}$ (the thermistor value at 25°C) for a given $R_{CS}$ value:

1. Select an NTC based on type and value. Because the value has not yet been found, start with a thermistor with a value close to $R_{CS}$. The NTC should also have an initial tolerance of better than 5%.
2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. These resistance values are called A ($R_{TH(50°C)}/R_{TH(25°C)}$) and B ($R_{TH(90°C)}/R_{TH(25°C)}$). Note that the NTC's relative value is always 1 at 25°C.
3. Find the relative value of $R_{CS}$ required for each of these temperatures. This is based on the percentage change needed, which in this example is initially 0.39%/°C. These are called $r_1$ (1/(1 + TC × ($T_1$ – 25))) and $r_2$ (1/(1 + TC × ($T_2$ – 25))), where TC = 0.0039 for copper. $T_1$ = 50°C and $T_2$ = 90°C are chosen. From this, one can calculate that $r_1$ = 0.9112 and $r_2$ = 0.7978.
4. Compute the relative values for $R_{CS1}$, $R_{CS2}$, and $R_{TH}$ using

$$r_{CS2} = \frac{(A-B) \times r_1 \times r_2 - A \times (1-B) \times r_2 + B \times (1-A) \times r_1}{A \times (1-B) \times r_1 - B \times (1-A) \times r_2 - (A-B)}$$

$$r_{CS1} = \frac{(1-A)}{\dfrac{1}{1-r_{CS2}} - \dfrac{A}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{1}{\dfrac{1}{1-r_{CS2}} - \dfrac{1}{r_{CS1}}} \qquad (8)$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \qquad (9)$$

6. Calculate values for $R_{CS1}$ and $R_{CS2}$ using Equation 10:

$$R_{CS1} = R_{CS} \times k \times r_{CS1}$$

$$R_{CS2} = R_{CS} \times \left((1-k) + \left(k \times r_{CS2}\right)\right) \qquad (10)$$

For this example, $R_{CS}$ has been calculated to be 100 kΩ, so start with a thermistor value of 100 kΩ. Looking through available 0603 size thermistors, one finds a Vishay NTHS0603N01N1003JR NTC thermistor with A = 0.3602 and B = 0.09174. From these, one can compute $r_{CS1}$ = 0.3796, $r_{CS2}$ = 0.7195, and $r_{TH}$ = 1.0751. Solving for $R_{TH}$ yields 107.51 kΩ, so 100 kΩ is chosen, making k = 0.9302. Finally, one finds that $R_{CS1}$ and $R_{CS2}$ are 35.3 kΩ and 73.9 kΩ. Choosing the closest 1% resistor values yields a choice of 35.7 kΩ and 73.2 kΩ.

## OUTPUT OFFSET

The AMD specification requires that at no load the nominal output voltage of the regulator be offset to a value higher than the nominal voltage corresponding to the VID code.

The offset is set by a constant current source flowing into of the FB pin ($I_{FB}$) and flowing through $R_B$. The value of $R_B$ can be found using Equation 11:

$$R_B = \frac{V_{ONL} - V_{VID}}{I_{FB}}$$

$$R_B = \frac{1.53\ \text{V} - 1.5\ \text{V}}{15\ \mu\text{A}} = 2.00\ \text{k}\Omega \quad (11)$$

The closest standard 1% resistor value is 2 kΩ.

## $C_{OUT}$ SELECTION

The required output decoupling for the regulator is typically recommended by AMD for various processors and platforms. One can also use some simple design guidelines to determine what is required. These guidelines are based on having both bulk and ceramic capacitors in the system.

First select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramics is inside the socket. Others can be placed along the outer edge of the socket as well.

Combined ceramic values of 30 µF to 100 µF are recommended, usually made up of multiple 10 µF or 22 µF capacitors. Select the number of ceramics and find the total ceramic capacitance ($C_Z$).

Next, there is an upper limit imposed on the total amount of bulk capacitance ($C_X$) when one considers the VID on-the-fly voltage stepping of the output (voltage step $V_V$ in time $t_V$ with error of $V_{ERR}$). A lower limit is based on meeting the capacitance for load release for a given maximum load step $\Delta I_O$ and a maximum allowable overshoot. The total amount of load release voltage is given as $\Delta V_O = \Delta I_O \times R_{OD}$.

$$C_{x(MIN)} \geq \left( \frac{L \times \Delta I_O}{n \times R_{OD} \times V_{VID}} - C_z \right) \quad (12)$$

$$C_{x(MAX)} \leq \frac{L}{nK^2 R_O^2} \times \frac{V_V}{V_{VID}} \times \left( \sqrt{1 + \left( t_v \times \frac{V_{VID}}{V_V} \times \frac{nKR_O}{L} \right)^2} - 1 \right) - C_Z \quad (13)$$

$$\text{where } K = ln\left( \frac{V_{ERR}}{V_V} \right)$$

To meet the conditions of these expressions and transient response, the ESR of the bulk capacitor bank ($R_X$) should be less than or equal to the dynamic droop resistance ($R_{OD}$). If the $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system cannot meet the VID on-the-fly specification and might require the use of a smaller inductor or more phases (and might have to increase the switching frequency to keep the output ripple the same).

This example uses a combination of MLC capacitors ($C_Z$ = 80 µF). The VID on-the-fly step change is from 1.5 V to 0.8 V (making $V_V$ = 700 mV) in 100 µs with a setting error of 3%. Solving for the bulk capacitance yields

$$C_{x(MIN)} \leq \left( \frac{600\ \text{nH} \times 24\ \text{A}}{3 \times 1.9\ \text{m}\Omega \times 1.5\ \text{V}} - 80\ \mu\text{F} \right) = 1.6\ \text{mF}$$

$$C_{x(MAX)} \leq \frac{600\ \text{nH} \times 700\ \text{mV}}{3 \times 3.5^2 \times 1.1\text{m}\Omega \times 1.5\ \text{V}} \times$$

$$\left( \sqrt{1 + \left( \frac{100\ \mu\text{s} \times 1.5\ \text{V} \times 3 \times 3.5 \times 1.1\ \text{m}\Omega}{700\ \text{mV} \times 600\ \text{nH}} \right)^2} - 1 \right) - 80\ \mu\text{F} = 20.4\ \text{mF}$$

where k = 3.5.

Using eight 820 µF OS-CON capacitors with a typical ESR of 12 mΩ each yields $C_X$ = 6.56 mF with an $R_X$ = 1.5 mΩ.

One last check should be made to ensure that the ESL of the bulk capacitors ($L_X$) is low enough to limit the high frequency ringing during a load change. This is tested using

$$L_x \leq Q^2 \times C_z \times R_{OD}{}^2$$
$$L_x \leq 2 \times 80\ \mu\text{F} \times (1.9\ \text{m}\Omega)^2 = 580\ \text{pH} \quad (14)$$

where Q is limited to the square root of 2 to ensure a critically damped system. In this example, $L_X$ is approximately 500 pH for the eight OS-CON capacitors, which satisfies this limitation. If the $L_X$ of the chosen bulk capacitor bank is too large, the number of ceramic capacitors might need to be increased, if there is excessive ringing.

One should note that for this multimode control technique, all ceramic designs can be used as long as the conditions of Equations 11, 12, and 13 are satisfied.

## POWER MOSFETS

For this example, the N channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, $Q_G$, $C_{ISS}$, $C_{RSS}$, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3110A) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With $V_{GATE}$ ~10 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are recommended.

The maximum output current ($I_O$) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With the ADP3186, currents are balanced between phases, therefore the current in each low-side MOSFET is the output current divided by the total number of MOSFETs ($n_{SF}$).

With conduction losses being dominant, the following expression shows the total power being dissipated in each synchronous MOSFET in terms of the ripple current per phase ($I_R$) and average total output current ($I_O$):

$$P_{SF} = (1-D) \times \left[ \left( \frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left( \frac{n\, I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (15)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, one can find the required $R_{DS(ON)}$ for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for $P_{SF}$ is 1 W to 1.5 W at 120°C junction temperature. Thus, for this example (56 A maximum), $R_{DS(SF)}$ < 4.8 mΩ. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C, so one needs to make sure to account for this when making this selection. This example uses one low-side MOSFET at 4.8 mΩ at 120°C.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the nonoverlap dead time of the MOSFET driver (40 ns typical for the ADP3110A). The output impedance of the driver is approximately 2 Ω, and the typical MOSFET input gate resistances are about 1 Ω to 2 Ω, so a total gate capacitance of less than 6000 pF should be adhered to. Because there is one MOSFET, the input capacitance for the synchronous MOSFET should be limited to 6000 pF.

The high-side (main) MOSFET must be able to handle two main power dissipation components: conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET, where $n_{MF}$ is the total number of main MOSFETs:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad (16)$$

where:

$R_G$ is the total gate resistance (2 Ω for the ADP3110A and about 1 Ω for typical high speed switching MOSFETs, making $R_G$ = 3 Ω).
$C_{ISS}$ is the input capacitance of the main MOSFET.

It is interesting to note that adding more main MOSFETs ($n_{MF}$) does not help the switching loss per MOSFET, because the additional gate capacitance slows switching. The best way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation, where $R_{DS(MF)}$ is the on resistance of the MOSFET:

$$P_{C(MF)} = D \times \left[ \left( \frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left( \frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (17)$$

Typically, for main MOSFETs, the highest speed (low $C_{ISS}$) device is preferred, but these usually have higher on resistance. Select a device that meets the total power dissipation (about 1.5 W for a single D-PAK) when combining the switching and conduction losses.

For this example, an NTD60N02 was selected as the main MOSFET (three total; $n_{MF}$ = 3), with a $C_{ISS}$ = 948 pF (max), and $R_{DS(MF)}$ = 11.2 mΩ (max at $T_J$ = 120°C), and an NTD110N02 was selected as the synchronous MOSFET (three total; $n_{SF}$ = 3), with $C_{ISS}$ = 2710 pF (max), and $R_{DS(SF)}$ = 4.8 mΩ (max at $T_J$ = 120°C). The synchronous MOSFET $C_{ISS}$ is less than 6000 pF, satisfying that requirement. Solving for the power dissipation per MOSFET at $I_O$ = 56 A and $I_R$ = 6.6 A yields 913 mW for each synchronous MOSFET and 1.48 W for each main MOSFET.

One last issue to consider is the power dissipation in the driver for each phase. This is best described in terms of the $Q_G$ for the MOSFETs and is given by the following equation, where $Q_{GMF}$ is the total gate charge for each main MOSFET and $Q_{GSF}$ is the total gate charge for each synchronous MOSFET:

$$P_{DRV} = \left[ \frac{f_{SW}}{2 \times n} \times \left( n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad (18)$$

Also shown is the standby dissipation factor ($I_{CC} \times V_{CC}$) for the driver. For the ADP3110A, the maximum dissipation should be less than 400 mW. In this example, with $I_{CC}$ = 7 mA, $Q_{GMF}$ = 16 nC, and $Q_{GSF}$ = 48 nC, one finds 211 mW in each driver, which is below the 400 mW dissipation limit. See the ADP3110A data sheet for more details.

## RAMP RESISTOR SELECTION

The ramp resistor ($R_R$) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. The following expression is used for determining the optimum value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R}$$

$$R_R = \frac{0.2 \times 600\ \text{nH}}{3 \times 5 \times 4.8\ \text{m}\Omega \times 5\ \text{pF}} = 333\ \text{k}\Omega \tag{19}$$

where:

$A_R$ is the internal ramp amplifier gain.
$A_D$ is the current balancing amplifier gain.
$R_{DS}$ is the total low-side MOSFET on resistance.
$C_R$ is the internal ramp capacitor value.
The closest standard 1% resistor value is 332 kΩ.

The internal ramp voltage magnitude can be calculated by using

$$V_R = \frac{A_R \times (1-D) \times V_{VID}}{R_R \times C_R \times f_{SW}}$$

$$V_R = \frac{0.2 \times (1-0.125) \times 1.5\ \text{V}}{332\ \text{k}\Omega \times 5\ \text{pF} \times 330\ \text{kHz}} = 480\ \text{m V} \tag{20}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response improve, but thermal balance degrades. Likewise, if the ramp is made smaller, thermal balance improves at the sacrifice of transient response and stability. The factor of three in the denominator of Equation 19 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

## COMP PIN RAMP

A ramp signal on the COMP pin is due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{(R_O + R_{OD}) \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O \times R_{OD}}\right)} \tag{21}$$

In this example, the overall ramp signal is 560 mV.

## CURRENT LIMIT SETPOINT

To select the current limit setpoint, first find the resistor value for $R_{LIM}$. The current limit threshold for the ADP3186 is set with a 3 V source ($V_{LIM}$) across $R_{LIM}$ with a gain of 10.4 mV/µA ($A_{LIM}$). $R_{LIM}$ can be found using

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{I_{LIM} \times R_O} \tag{22}$$

For values of $R_{LIM}$ greater than 500 kΩ, the current limit might be lower than expected, so some adjustment of $R_{LIM}$ might be needed. Here, $I_{LIM}$ is the average current limit for the output of the supply.

In this example, choosing a peak current limit of 100 A for $I_{LIM}$ results in $R_{LIM}$ = 284 kΩ, for which 280 kΩ is chosen as the nearest 1% value.

The per-phase current limit described in the Current Limit, Short-Circuit, and Latch-Off Protection section is determined by

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_{RT} - V_{BIAS}}{A_D \times R_{DS(MAX)}} - \frac{I_R}{2} \tag{23}$$

For the ADP3186, the maximum COMP voltage ($V_{COMP(MAX)}$) is 3.3 V, the COMP pin bias voltage ($V_{BIAS}$) is 1.2 V, and the current balancing amplifier gain ($A_D$) is 5. Using $V_R$ of 560 mV and $R_{DS(MAX)}$ of 4.8 mΩ (low-side on resistance at 150°C), one finds a per-phase peak current limit of 61 A. Although this number may seem high, this current level can be reached only with an absolute short at the output, and the current limit latch-off function shuts down the regulator before overheating can occur.

This limit can be adjusted by changing the ramp voltage ($V_R$), but make sure not to set the per-phase limit lower than the average per-phase current ($I_{LIM}$/n).

The per-phase initial duty cycle limit is determined by

$$D_{MAX} = D \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_{RT}} \tag{24}$$

In this example, the maximum duty cycle is 0.47.

## FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3186 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and equal to the droop resistances ($R_O$ and $R_{OD}$). With the resistive output impedance, the output voltage droops in proportion to the load current at any load current slew rate. This ensures optimal positioning and helps to minimize the output decoupling.

With the multimode feedback structure of the ADP3186, the feedback compensation must be set so that the converter's output impedance works in parallel with the output decoupling to meet this goal. Several poles and zeros created by the output inductor and decoupling capacitors (output filter) need to be compensated for.

A type-three compensator on the voltage feedback is adequate for proper compensation of the output filter. Equations 25 to 29 are intended to yield an optimal starting point for the design; some adjustments might be necessary to account for PCB and component parasitic effects.

The first step is to compute the time constants for all the poles and zeros in the system:

$$R_e = n \times R_{OD} + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{(R_O + R_{OD}) \times L \times (1 - n \times D) \times V_{RT}}{n \times C_X \times R_O \times R_{OD} \times V_{VID}}$$

$$R_e = 3 \times 1.9\,\text{m}\Omega + 5 \times 4.8\,\text{m}\Omega + \frac{1.6\,\text{m}\Omega \times 0.56\,\text{V}}{1.5\,\text{V}} + \frac{(1.1\,\text{m}\Omega + 1.9\,\text{m}\Omega) \times 600\,\text{nH} \times (1 - 0.375) \times 0.56\,\text{V}}{3 \times 6.56\,\text{mF} \times 1.1\,\text{m}\Omega \times 1.9\,\text{m}\Omega \times 1.5\,\text{V}} = 40.5\,\text{m}\Omega \quad (25)$$

$$T_a = C_X \times (R_{OD} - R') + \frac{L_X}{R_{OD}} \times \frac{R_{OD} - R'}{R_X} = 6.56\,\text{mF} \times (1.9\,\text{m}\Omega - 0.6\,\text{m}\Omega) + \frac{500\,\text{pH}}{1.9\,\text{m}\Omega} \times \frac{1.9\,\text{m}\Omega - 0.6\,\text{m}\Omega}{1.5\,\text{m}\Omega} = 8.76\,\mu\text{s} \quad (26)$$

$$T_b = (R_X + R' - R_{OD}) \times C_X = (1.5\,\text{m}\Omega + 0.6\,\text{m}\Omega - 1.9\,\text{m}\Omega) \times 6.56\,\text{mF} = 1.31\,\mu s \quad (27)$$

$$T_c = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}}\right)}{V_{VID} \times R_e} = \frac{0.56\,\text{V} \times \left(600\,\text{nH} - \frac{5 \times 4.8\,\text{m}\Omega}{2 \times 330\,\text{kHz}}\right)}{1.5\,\text{V} \times 40.5\,\text{m}\Omega} = 5.2\,\mu\text{s} \quad (28)$$

$$T_d = \frac{C_X \times C_Z \times R_{OD}^2}{C_X \times (R_{OD} - R') + C_Z \times R_{OD}} = \frac{6.56\,\text{mF} \times 80\,\mu\text{F} \times (1.9\,\text{m}\Omega)^2}{6.56\,\text{mF} \times (1.9\,\text{m}\Omega - 0.6\,\text{m}\Omega) + 80\,\mu\text{F} \times 1.9\,\text{m}\Omega} = 218\,\text{ns} \quad (29)$$

where, for the ADP3186, R' is the PCB resistance from the bulk capacitors to the ceramics and where $R_{DS}$ is the total low-side MOSFET on resistance per phase. In this example, $A_D$ is 5, $V_{RT}$ equals 0.56 V, R' is approximately 0.6 mΩ (assuming a 4-layer, 1 oz motherboard), and $L_X$ is 500 pH for the eight OS-CON capacitors.

The compensation values can then be solved using

$$C_A = \frac{n \times R_{OD} \times T_a}{R_e \times R_B}$$

$$C_A = \frac{3 \times 1.9\,\text{m}\Omega \times 8.76\,\mu\text{s}}{40.5\,\text{m}\Omega \times 2\,\text{k}\Omega} = 616\,\text{pF} \quad (30)$$

$$R_A = \frac{T_c}{C_A} = \frac{5.2\,\mu\text{s}}{616\,\text{pF}} = 8.44\,\text{k}\Omega \quad (31)$$

$$C_B = \frac{T_b}{R_B} = \frac{1.31\,\mu s}{2\,\text{k}\Omega} 655\,\text{pF} \quad (32)$$

$$C_{FB} = \frac{T_d}{R_A} = \frac{218\,\text{ns}}{8.44\,\text{k}\Omega} = 25.8\,\text{pF} \quad (33)$$

These are the starting values prior to tuning the design to account for layout and other parasitic effects (see the Tuning Procedure section). The final values selected after tuning are

$C_A$ = 680 pF
$R_A$ = 8.45 kΩ
$D_B$ = 860 pF
$C_{FB}$ = 27 pF

## $C_{IN}$ SELECTION AND INPUT CURRENT di/dt REDUCTION

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to n × $V_{OUT}/V_{IN}$ and an amplitude of 1 nth the maximum output current. To prevent large voltage transients, a low ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by

$$I_{Crms} = D \times I_O \times \sqrt{\frac{1}{N \times D} - 1}$$

$$I_{Crms} = 0.125 \times 56\,\text{A} \times \sqrt{\frac{1}{3 \times 0.125} - 1} = 9.05\,\text{A} \quad (34)$$

Note that the capacitor manufacturer's ripple current ratings are often based on only 2,000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors can be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 2,200 µF, 16 V aluminum electrolytic capacitors with a ripple rating of 3.5 A each.

To reduce the input current di/dt to a level below the recommended maximum of 0.1 A/µs, an additional small inductor (L > 1 µH @ 15 A) should be inserted between the converter and the supply bus. That inductor also acts as a filter between the converter and the primary power source.

## TUNING PROCEDURE

To tune the AD3186, follow these steps:

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Hook up the dc load to circuit, turn it on, and verify its operation. Also check for jitter at no-load and full-load.

### *DC Loadline Setting*

3. Measure the output voltage at no-load ($V_{NL}$). Verify that it is within tolerance.
4. Measure the output voltage at full-load cold ($V_{FLCOLD}$). Let the board sit for ~10 minutes at full-load, and then measure the output ($V_{FLHOT}$). If there is a change of more than a few mV, adjust $R_{CS1}$ and $R_{CS2}$ using Equations 35 and 37.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad (35)$$

5. Repeat Step 4 until the cold and hot voltage measurements remain the same.
6. Measure the output voltage from no-load to full-load using 5 A steps. Compute the loadline slope for each change, and then average them to determine the overall loadline slope ($R_{OMEAS}$).
7. If $R_{OMEAS}$ is off from $R_O$ by more than 0.05 mΩ, use the following to adjust the $R_{PH}$ values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad (36)$$

8. Repeat Steps 6 and 7 to check the loadline, and repeat adjustments, if necessary.
9. Once dc loadline adjustment is complete, do not change $R_{PH}$, $R_{CS1}$, $R_{CS2}$, or $R_{TH}$ for the remainder of the procedure.
10. Measure the output ripple at no-load and full-load with a scope, and make sure that it is within specifications.

### AC Loadline Setting

11. Remove the dc load from the circuit and hook up the dynamic load.
12. Hook up the scope to the output voltage and set it to dc coupling with the time scale at 100 µs/div.
13. Set the dynamic load for a transient step of about 24 A at 1 kHz with 50% duty cycle.
14. Measure the output waveform (you might have to use dc offset on scope to see the waveform). Try to use a vertical scale of 100 mV/div or finer. This waveform should look similar to Figure 12.
15. Use the horizontal cursors to measure $V_{ACDRP}$ and $V_{DCDRP}$ as shown. Do not measure the undershoot or overshoot that happens immediately after the step.
16. If $V_{ACDRP}$ and $V_{DCDRP}$ are different by more than a few mV, use Equation 38 to adjust $C_{CS}$. You might need to parallel different values to get the right one, because the standard capacitor values available are limited. It is a good idea to have locations for two capacitors in the layout for this.

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad (38)$$

17. Repeat Steps 11 to 13 and repeat the adjustments, if necessary. Once complete, do not change $C_{CS}$ for the remainder of the procedure.
18. Set the dynamic load step to the maximum step size (do not use a step size larger than needed) and verify that the output waveform is square, which means that $V_{ACDRP}$ and $V_{DCDRP}$ are equal.

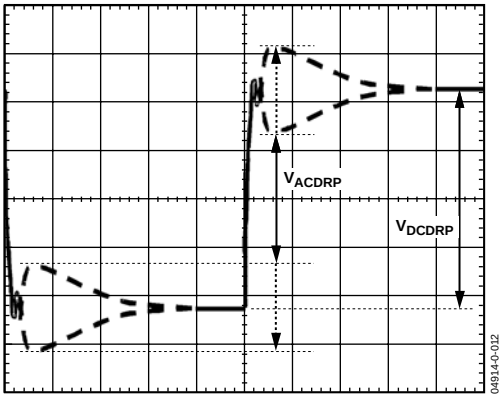



*Figure 12. AC Loadline Waveform*

$$R_{CS1(NEW)} = \frac{1}{\dfrac{R_{CS1(OLD)} + R_{TH(25°C)}}{R_{CS1(OLD)} \times R_{TH(25°C)} + \left(R_{CS1(OLD)} - R_{CS2(NEW)}\right) \times \left(R_{CS1(OLD)} - R_{TH(25°C)}\right)} - \dfrac{1}{R_{TH(25°C)}}} \quad (37)$$

### *Initial Transient Setting*

19. With the dynamic load still set at the maximum step size, expand the scope time scale to see 2 µs/div to 5 µs/div. The waveform may have two overshoots and one minor undershoot (see Figure 13). Here, $V_{DROOP}$ is the final desired value.

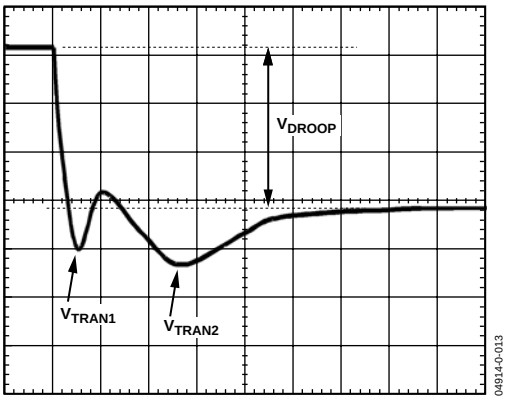



*Figure 13. Transient Setting Waveform*

20. If both overshoots are larger than desired, try making the following adjustments. Note that, if these adjustments do not change the response, you are limited by the output decoupling. Check the output response each time you make a change as well as the switching nodes to make sure that the response is still stable.

21. Make the ramp resistor larger by 25% ($R_{RAMP}$).

22. For $V_{TRAN1}$, increase $C_B$ or increase the switching frequency.

23. For $V_{TRAN2}$, increase $R_A$ and decrease $C_A$ by 25%.

24. For load release (see Figure 14), if $V_{TRANREL}$ is larger than $V_{TRAN1}$ (see Figure 13), there is not enough output capacitance. You need more capacitance or you have to make the inductor values smaller. (If you change inductors, you need to start the design again using the spreadsheet and this tuning procedure.)

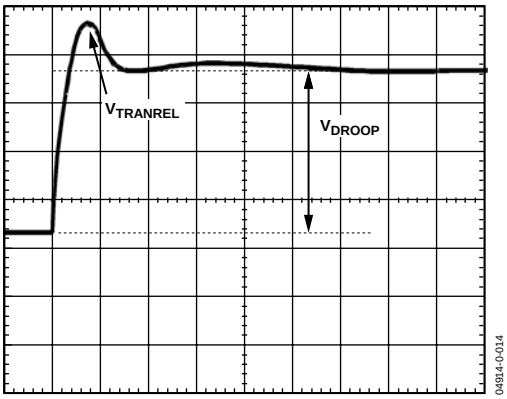



*Figure 14. Transient Setting Waveform*

Because the ADP3186 turns off all the phases (switches inductors to ground), there is no ripple voltage present during load release. Therefore, you do not have to add headroom for ripple, allowing your load release $V_{TRANREL}$ to be larger than $V_{TRAN1}$ by the amount of ripple, and still meet specifications.

If $V_{TRAN1}$ and $V_{TRANREL}$ are less than the desired final droop, this implies that capacitors can be removed. When removing capacitors, check the output ripple voltage as well to make sure that it is still within specifications.

## LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

### *General Recommendations*

For good results, a PCB with at least four layers is recommended. This provides the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input, and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths, so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3186) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3186 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing in it.

The components around the ADP3186 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins. The output capacitors should be connected as close as possible to the load (or connector), for example, a microprocessor core, that receives the power. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop, described in the Power Circuitry Recommendations section.

### *Power Circuitry Recommendations*

The switching power path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry.

The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.

Whenever a power dissipating component, for example, a power MOSFET, is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air.

Make a mirror image of any pad being used to heat sink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

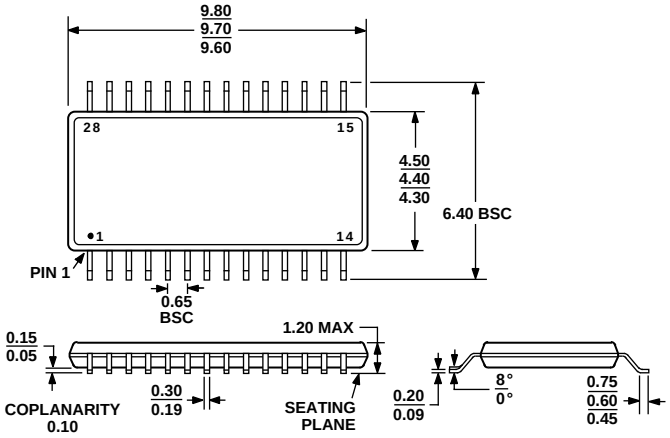
For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

### *Signal Circuitry Recommendations*

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Therefore, the FB and FBRTN traces should be routed adjacent to each other on top of the power ground plane back to the controller.

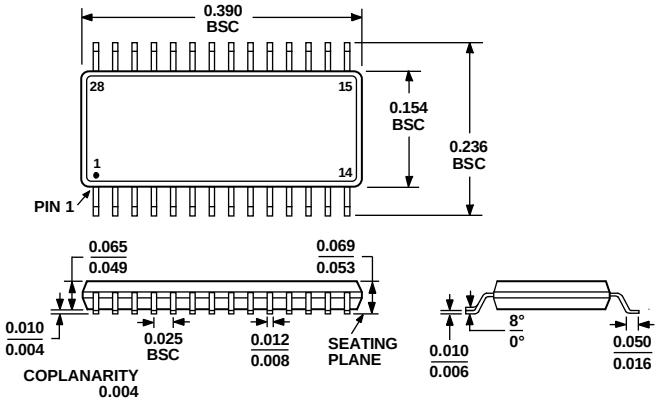
The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-153AE

*Figure 15. 28-Lead Thin Shrink Small Outline Package [TSSOP] (RU-28)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-137-AF

*Figure 16. 28-Lead Shrink Small Outline Package [QSOP] (RQ-28)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Quantity per Reel |
|---|---|---|---|---|
| ADP3186JRUZ-REEL[1] | 0°C to 85°C | 28-Lead TSSOP | RU-28 | 2500 |
| ADP3186JRQZ-REEL[1] | 0°C to 85°C | 28-Lead QSOP | RQ-28 | 2500 |

[1] Z = Pb-free part.

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D04914-0-3/06(A)

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