THE DATASHEET OF

ADP3209JCPZ-RL

ON Semiconductor®

5-Bit, Programmable, Single-Phase, Synchronous Buck Controller

ADP3209

FEATURES

- **Single-chip solution**
  - **Fully compatible with the Intel® GMCH chipset voltage regulator specifications**
  - **Integrated MOSFET drivers**
- **±8 mV worst-case differentially sensed core voltage error over temperature**
- **Automatic power-saving modes maximize efficiency during light load operation**
- **Soft transient control reduces inrush current and audio noise**
- **Independent current limit and load line setting inputs for additional design flexibility**
- **Built-in power-good masking supports voltage identification (VID) on-the-fly transients**
- **5-bit, digitally programmable DAC with 0.4 V to 1.25 V output**
- **Short-circuit protection with programmable latch-off delay**
- **Output power or current monitor options**
- **32-lead LFCSP**

APPLICATIONS

- **Notebook power supplies for next-generation Intel chipsets**

GENERAL DESCRIPTION

The ADP3209 is a highly efficient, single-phase, synchronous buck switching regulator controller. With its integrated drivers, the ADP3209 is optimized for converting the notebook battery voltage to render the supply voltage required by high performance Intel chipsets. An internal 5-bit DAC is used to read a VID code directly from the chipset and to set the GMCH core voltage to a value within the range of 0.4 V to 1.25 V.

The ADP3209 uses a multimode architecture. It provides programmable switching frequency that can be optimized for efficiency depending on the output current requirement. In addition, the ADP3209 includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The ADP3209 also provides accurate and reliable current overload protection and a delayed power-good output. The IC supports on-the-fly output voltage changes requested by the chipset.

The ADP3209 is specified over the extended commercial temperature range of 0°C to 100°C and is available in a 32-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

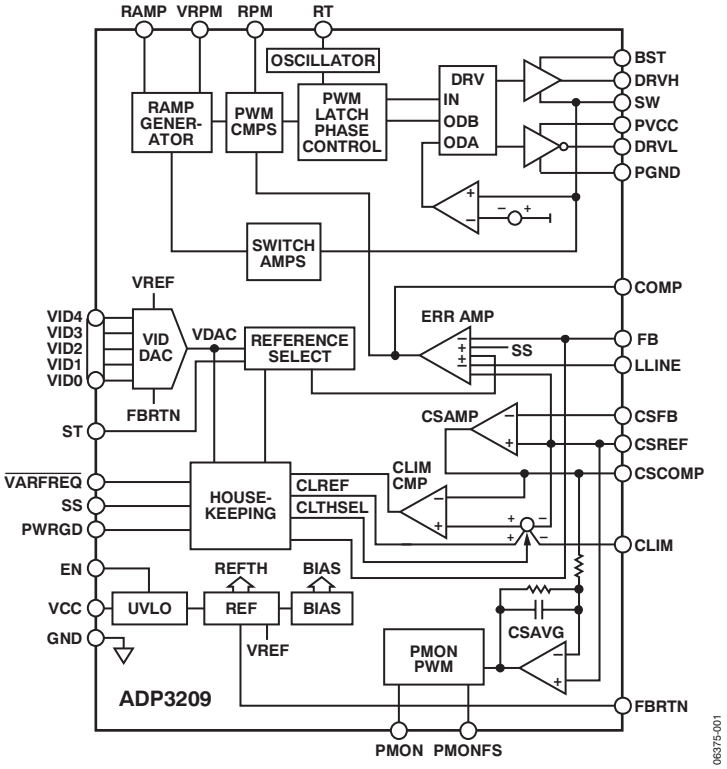

Figure 1.

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REVISION HISTORY

01/08 - Rev 2: Conversion to ON Semiconductor

9/07—Rev. Sp0 to Rev. SpA

Changes to Absolute Maximum Ratings 7
Change to Table 3 8
Change to the Setting the Clock Frequency for PWM Section 22
Changes to Ordering Guide 32

10/06—Revision Sp0: Initial Version

SPECIFICATIONS

VCC = 5 V, FBRTN = GND, $\overline{\text{VARFREQ}}$ = low, V_{VID} = 1.25 V, T_A = 0°C to 100°C, unless otherwise noted.[1] Current entering a pin (sunk by the device) has a positive sign.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOLTAGE ERROR AMPLIFIER						
Output Voltage Range[2]	V_{COMP}		0.8		3.6	V
COMP Clamp	V_{COMP}	CSREF < 0.2 V		1.6		V
DC Accuracy	V_{FB}	Relative to nominal V_{VID}, LLINE = CSREF, V_{VID} range = 0.4000 V to 1.25000 V	−8		+8	mV
Load Line Positioning Accuracy	ΔV_{FB}	LLINE − CSREF = −80 mV	76	80	83	mV
		LLINE − CSREF = −200 mV	190	200	210	mV
LLINE Input Bias Current	I_{LLINE}		−80		+80	nA
Differential Nonlinearity			−1		+1	LSB
VCC Line Regulation	ΔV_{FB}	VCC = 4.75 V to 5.25 V		0.05		%
Input Bias Current	I_{FB}		−1		+1	µA
FBRTN Current	I_{FBRTN}			200	400	µA
Output Current	I_{COMP}	FB forced to V_{VID} − 3%		500		µA
Gain Bandwidth Product[2]	$GBW_{(ERR)}$	COMP = FB, C_{COMP} = 0 pF		20		MHz
Slew Rate[2]		C_{COMP} = 10 pF		25		V/µs
VID DAC INPUTS						
Input Low Voltage	V_{IL}	VID(x)			0.5	V
Input High Voltage	V_{IH}	VID(x)	2.2			V
Input Current	$I_{IN(VID)}$	Sink current		1		µA
VID Transition Delay Time[2]		VID code change to FB change	400			ns
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.3		3	MHz
Oscillator Frequency	f_{OSC}	$\overline{\text{VARFREQ}}$ = high, RT = 250 kΩ		550		kHz
		$\overline{\text{VARFREQ}}$ = high, RT = 125 kΩ		1		MHz
RT Output Voltage	V_{RT}	$\overline{\text{VARFREQ}}$ = low, V_{VID} = 1.250 V	1.09	1.125	1.2	V
		$\overline{\text{VARFREQ}}$ = high (forced PWM mode)	1.6	1.7	1.8	V
VRPM Reference Voltage	V_{VRPM}	I_{VRPM} = 0 µA	0.95	1	1.05	V
		I_{VRPM} = 120 µA	0.95	1	1.05	V
RPM Output Current	I_{RPM}	V_{VID} = 1.250 V, R_T = 250 kΩ		−5		µA
RPM Comparator Offset	$V_{OS(RPM)}$	$V_{OS(RPM)} = V_{COMP} - V_{RPM}$		−11		mV
RAMP Input Voltage	V_{RAMP}		0.9	1.0	1.1	V
RAMP Input Current Range	I_{RAMP}	EN = high	1		50	µA
RAMP Input Current in Shutdown		EN = low or in UVLO, RAMP = 19 V		1		µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSFB − CSREF	−1.2		+1.2	mV
Input Bias Current	$I_{BIAS(CSFB)}$		−65		+65	nA
Gain Bandwidth Product[2]	$GBW_{(CSA)}$			6		MHz
Slew Rate[2]		C_{CSCOMP} = 10 pF		10		V/µs
Input Common-Mode Range[2]		CSFB and CSREF	0		3.5	V
Output Voltage Range	V_{CSCOMP}		0.05		2.7	V
Output Current	I_{CSCOMP}	Sink current	400	1000		µA
		Source current		−15	−8	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SWITCH AMPLIFIER						
Common-Mode Range[2]	V_{SW}		−400		+200	mV
Input Resistance	R_{SW}		30	45	60	kΩ
Input Current	I_{SW}	SW = 0 V		−4		µA
Zero Current Switching Threshold	$V_{ZCS(SW)}$			−6		mV
DCM Minimum Off Time Masking	$t_{OFFMASK}$	SW falling		475		ns
CURRENT LIMIT COMPARATOR						
Output Voltage Range[2]	V_{CLIM}		0.5		3	V
Output Current	I_{CLIM}	V_{CLIM} = 1.25 V		−10		µA
Current Limit Threshold Voltage	V_{CLTH}	$V_{CSREF} - V_{CSCOMP}$, R_{CLIM} = 125 kΩ	105	125	145	mV
Current Limit Setting Ratio		V_{CL}/V_{CLIM}		0.1		
SOFT START/LATCH-OFF TIMER						
Output Current	I_{SS}	During startup, V_{SS} < 1.7 V	−11	−7.5	−5	µA
		In normal mode, V_{SS} > 1.7 V		−48		µA
		In current limit, V_{SS} > 1.7 V	1.5	2	2.5	µA
Termination Threshold Voltage	$V_{TH(SS)}$	During startup	1.6	1.7	1.8	V
Normal Mode Operating Voltage		After PWRGD goes high		2.9		V
Current Limit Latch-Off Voltage	$V_{ILO(SS)}$	Current limit or PWRGD failure, SS falling	1.6	1.7	1.8	V
SOFT TRANSIENT CONTROL						
ST Sourcing Current	$I_{SOURCE(ST)}$	ST = V_{DAC} − 0.3 V		−7.5		µA
ST Sinking Current	$I_{SINK(ST)}$	ST = V_{DAC} + 0.3 V		2.5		µA
ST Offset Voltage	$V_{OS(ST)}$	|ST − V_{VID}| at the end of PWRGD masking	−10		+35	mV
Minimum Capacitance	C_{ST}		100			pF
Extended PWRGD Masking Comparator Threshold	$V_{TH(ST)}$	|ST − V_{VID}|, ST falling		150		mV
SYSTEM LOGIC INPUTS						
Input Low Voltage	V_{IL}	$\overline{\text{VARFREQ}}$			0.7	V
		EN			1.0	V
Input High Voltage	V_{IH}	$\overline{\text{VARFREQ}}$	4			V
		EN	2.3			V
Input Current	I_{IN}	EN, $\overline{\text{VARFREQ}}$		20		nA
	I_{IN}	EN = V_{TH}, high-to-low or low-to-high		60		µA
POWER GOOD						
CSREF Undervoltage Threshold	$V_{UV(CSREF)}$	Relative to V_{VID} = 0.4 V to 1.25 V		−300		mV
CSREF Overvoltage Threshold	$V_{OV(CSREF)}$	Relative to V_{VID} = 0.4 V to 1.25 V		200	250	mV
CSREF Crowbar (Overvoltage Protection) Threshold	$V_{CB(CSREF)}$	Relative to FBRTN	1.65	1.7	1.75	V
CSREF Reverse Voltage Detection Threshold	$V_{RVP(CSREF)}$	Relative to FBRTN				
		CSREF falling	−425	−300		mV
		CSREF rising		−60		mV
PWRGD Output Low Voltage	$V_{OL(PWRGD)}$	$I_{SINK(PWRGD)}$ = 4 mA		60	100	mV
PWRGD Output Leakage Current		V_{PWRDG} = 5 V			3	µA
PWRGD Masking Time				100		µs
POWER MONITOR						
PMON Output Resistance		I_{SINK} = 2 mA		15		Ω
PMON Leakage Current		PMON = 5 V		5		nA
PMON Oscillator Frequency		PMONFS = 2 V		320		kHz
PMONFS Voltage Range[2]			1.5		4	V
PMONFS Output Current		PMONFS = 2 V		−10		µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH-SIDE MOSFET DRIVER						
Output Resistance, Sourcing Current		BST − SW = 4.6 V		1.6	3.3	Ω
Output Resistance, Sinking Current		BST − SW = 4.6 V		1.3	2.8	Ω
Transition Times	$tr_{DRVH,}$	BST − SW = 4.6 V, C_L = 3 nF, Figure 2		15	35	ns
	tf_{DRVH}	BST − SW = 4.6 V, C_L = 3 nF, Figure 2		13	31	ns
Dead Delay Times	$tpdh_{DRVH}$	BST − SW = 4.6 V, Figure 2		10	30	ns
BST Quiescent Current		EN = low, shutdown		5	15	μA
		EN = high, no switching		200		μA
LOW-SIDE MOSFET DRIVER						
Output Resistance, Sourcing Current				1.4	3.0	Ω
Output Resistance, Sinking Current				1	2.7	Ω
Transition Times	$tr_{DRVL,}$	C_L = 3 nF, Figure 2		15	35	ns
	tf_{DRVL}	C_L = 3 nF, Figure 2		14	35	ns
Propagation Delay Times	$tpdh_{DRVL}$	C_L = 3 nF, Figure 2		10	30	ns
SW Transition Timeout	$t_{TO(SW)}$	BST − SW = 4.6 V	85	130	200	ns
Zero-Crossing Threshold	V_{ZC}			2.2		V
PVCC Quiescent Current		EN = low, shutdown		14	50	μA
		EN = high, no switching		170		μA
SOFT STOP						
CSREF Resistance to GND		EN = low or latch off		70		Ω
SUPPLY						
Supply Voltage Range[2]	V_{CC}		4.5		5.5	V
Supply Current		Normal mode		5	9	mA
		EN = 0 V		6	40	μA
VCC OK Threshold Voltage	V_{CCOK}	VCC rising		4.4	4.5	V
VCC UVLO Threshold Voltage	V_{CCUVLO}	VCC falling	4.0	4.2		V
UVLO Hysteresis[2]			150			mV

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or bench characterization, not production tested.

TIMING DIAGRAM

Timing is referenced to the 90% and 10% points, unless otherwise noted.

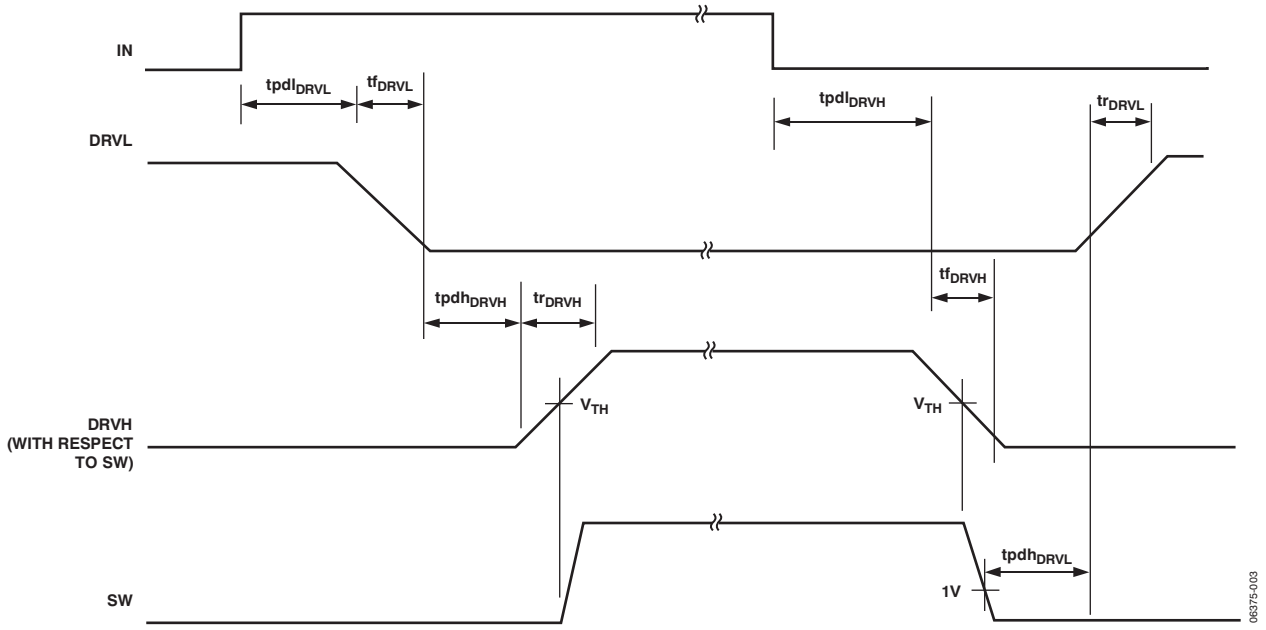


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +6 V
FBRTN, PGND	−0.3 V to +0.3 V
BST	
DC	−0.3 V to +25 V
t < 200 ns	−0.3 V to +30 V
DRVH, SW	
DC	−5 V to +20 V
t < 200 ns	−10 V to +25 V
DRVL to PGND	
DC	−0.3 V to +6 V
t < 200 ns	−5 V to +6 V
RAMP (in Shutdown)	
DC	−0.3 V to +20 V
t < 200 ns	−0.3 V to +25 V
All Other Inputs and Outputs	−0.3 V to +6 V
Storage Temperature	−65°C to +150°C
Operating Ambient Temperature Range	0°C to 100°C
Operating Junction Temperature	125°C
Thermal Impedance (θ_{JA}) 2-Layer Board	32.6°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

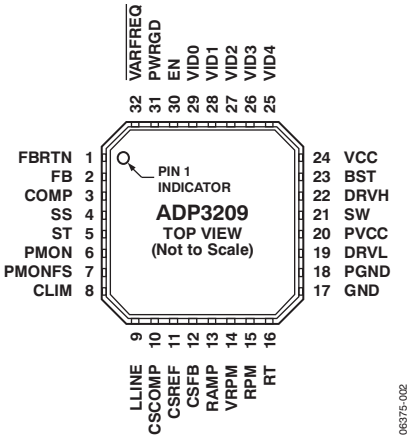


Figure 3. LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FBRTN	Feedback Return Input/Output. This pin remotely senses the GMCH voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
2	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
3	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
4	SS	Soft Start and Latch-Off Delay Setting Input/Output. An external capacitor from this pin to GND sets the soft start ramp-up time and the current limit latch-off delay ramp-down time.
5	ST	Soft Transient Slew Rate Timing Input/Output. A capacitor from this pin to GND sets the slew rate of the output voltage when it transitions from one VID setting to another.
6	PMON	Power Monitor Output. Open-drain output. A pull-up resistor from PMON to CSREF provides a duty cycle–modulated power output signal. An external RC network can be used to convert the digital signal stream to an averaged power analog output voltage.
7	PMONFS	Power Monitor Full-Scale Setting Input/Output. A resistor from this pin to GND sets the full-scale value of the PMON output signal.
8	CLIM	Current Limit Setting Input/Output. An external resistor from this pin to GND sets the current limit threshold of the converter.
9	LLINE	Load Line Programming Input. The center point of a resistor divider connected between CSREF and CSCOMP can be tied to this pin to set the load line slope.
10	CSCOMP	Current Sense Amplifier Output and Frequency Compensation Point.
11	CSREF	Current Sense Reference Input. This pin must be connected to the opposite side of the output inductor.
12	CSFB	Noninverting Input of the Current Sense Amplifier. The combination of a resistor from the switch node to this pin and the feedback network from this pin to the CSCOMP pin sets the gain of the current sense amplifier.
13	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp.
14	VRPM	RPM Mode Reference Voltage Output.
15	RPM	Ramp Pulse Modulation Current Source Output. A resistor between this pin and VRPM sets the RPM comparator upper threshold.
16	RT	PWM Oscillator Frequency Setting Input. An external resistor from this pin to GND sets the PWM oscillator frequency.
17	GND	Analog and Digital Signal Ground.
18	PGND	Low-Side Driver Power Ground. This pin should be connected close to the source of the lower MOSFET(s).
19	DRVL	Low-Side Gate Drive Output.
20	PVCC	Power Supply Input/Output of Low-Side Gate Driver.

Pin No.	Mnemonic	Description
21	SW	Current Return For High-Side Gate Drive.
22	DRVH	High-Side Gate Drive Output.
23	BST	High-Side Bootstrap Supply. A capacitor from this pin to SW holds the bootstrapped voltage while the high-side MOSFET is on.
24	VCC	Power Supply Input/Output of the Controller.
25 to 29	VID4 to VID0	Voltage Identification DAC Inputs. A 5-bit word (the VID code) programs the DAC output voltage, the reference voltage of the voltage error amplifier without a load (see the VID code table, Table 4). In normal operation mode, the VID DAC output programs the output voltage to a value within the 0 V to 1.25 V range. The input is actively pulled down.
30	EN	Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, and pulls PWRGD low.
31	PWRGD	Power-Good Output. Open-drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
32	$\overline{\text{VARFREQ}}$	Variable Frequency Enable Input. Pulling this pin to ground sets the normal RPM mode of operation. Pulling this pin to 5 V sets the fixed-frequency PWM mode of operation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

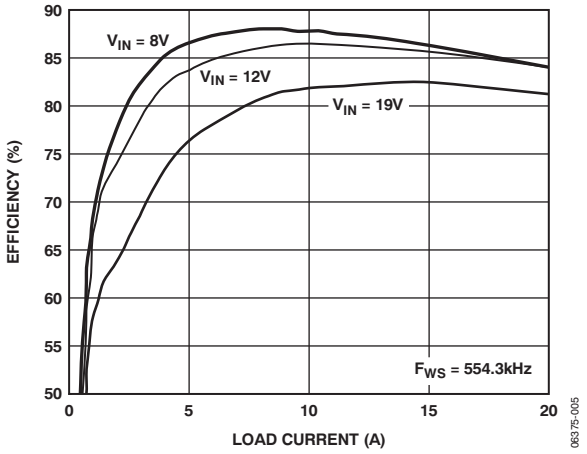


Figure 4. PWM Mode Efficiency vs. Load Current

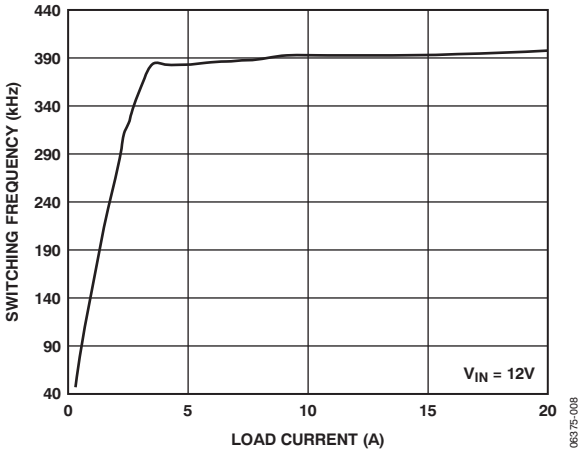


Figure 7. Switching Frequency vs. Load Current in RPM Mode

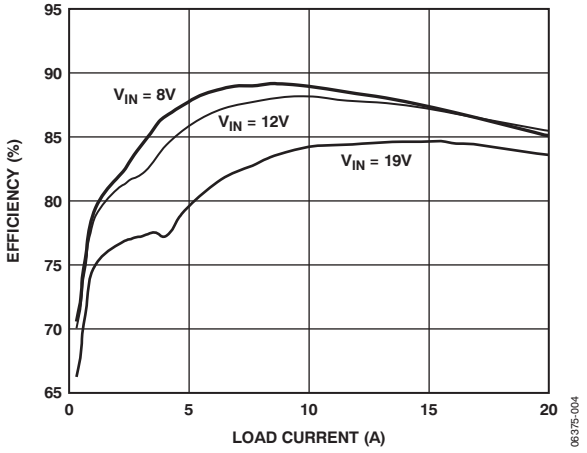


Figure 5. RPM Mode Efficiency vs. Load Current

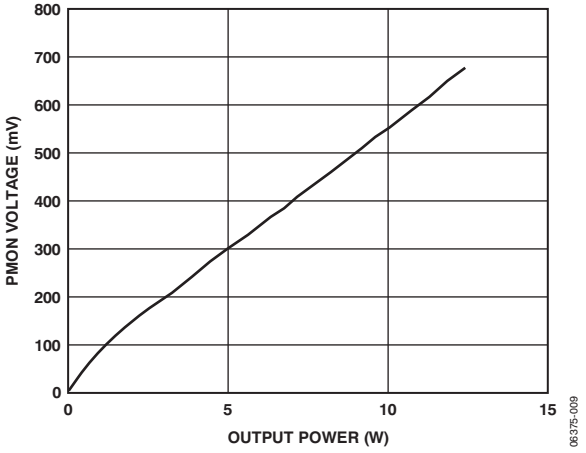


Figure 8. PMON Voltage vs. Output Power

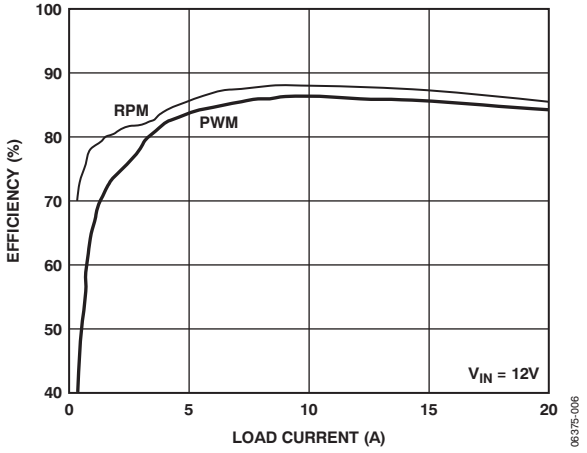


Figure 6. Efficiency vs. Load Current in All Modes

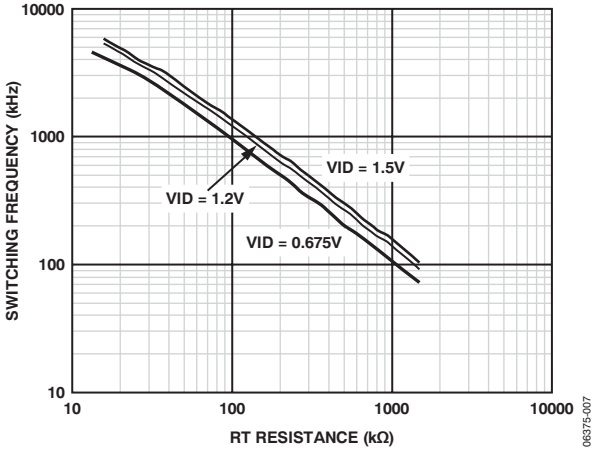


Figure 9. Switching Frequency vs. RT Resistance

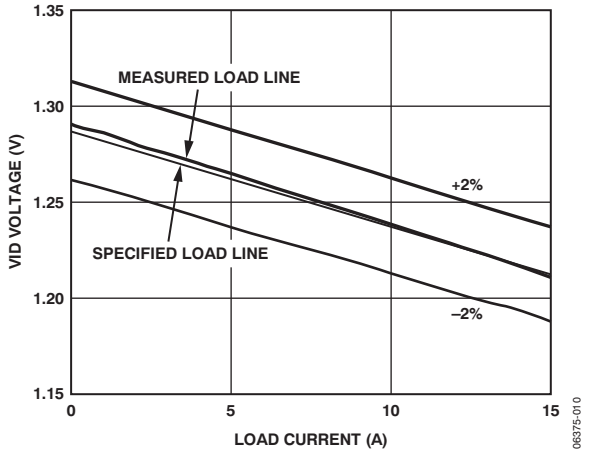


Figure 10. Load Line Accuracy

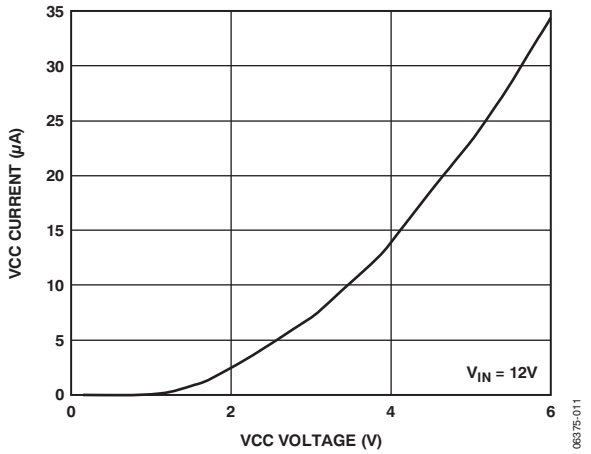


Figure 11. VCC Current vs. VCC Voltage with Enable Low

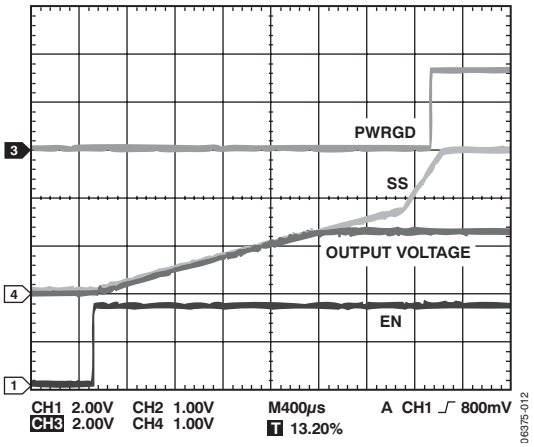


Figure 12. Start-Up Waveforms

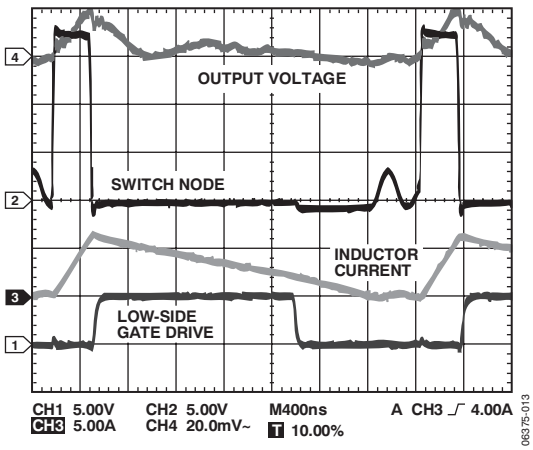


Figure 13. DCM Waveforms, 3 A Load Current

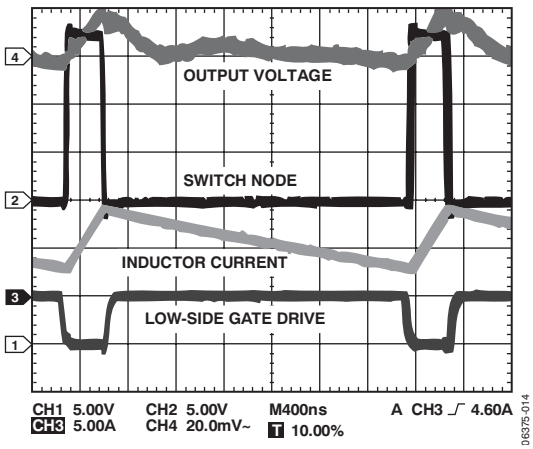


Figure 14. CCM Waveforms, 6 A Load Current

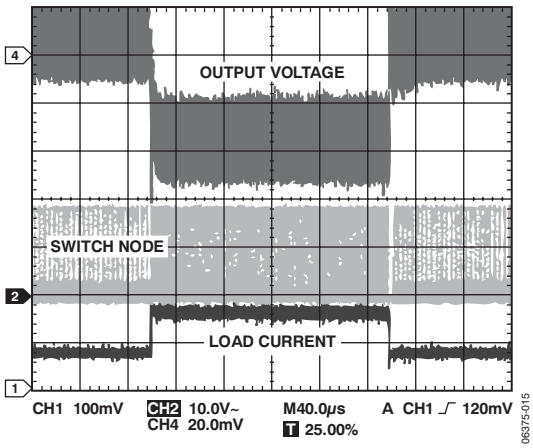


Figure 15. Load Transient, 2 A to 10 A, V_{IN} = 19 V

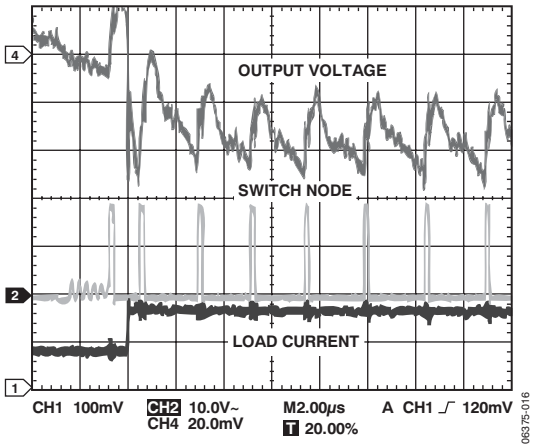


Figure 16. Load Transient, 2 A to 10 A, V_{IN} = 19 V

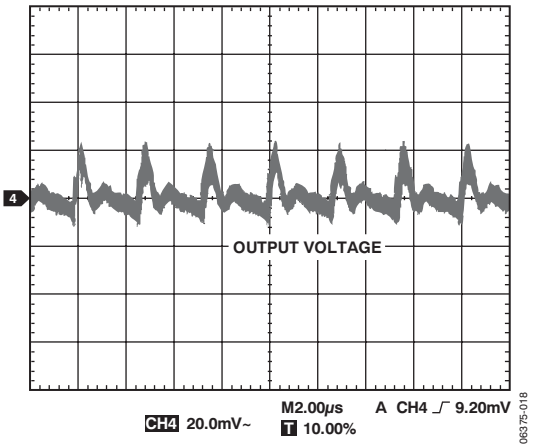


Figure 18. Output Ripple, 15 A Load, C_X = 470 µF, C_Z = 44 µF

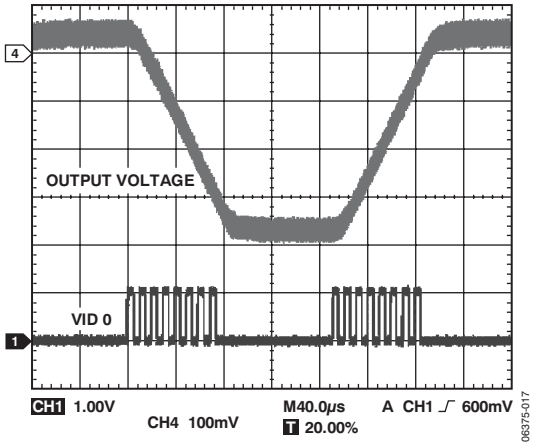


Figure 17. VID on the Fly, 1.25 V to 0.825 V

THEORY OF OPERATION

The ADP3209 is a ramp-pulse-modulated (RPM) controller for synchronous buck Intel GMCH core power supply. The internal 5-bit VID DAC conforms to the Intel IMVP-6+ specifications. The ADP3209 is a stable, high performance architecture that includes

- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors
- Minimized thermal switching losses due to lower frequency operation
- High accuracy load line regulation
- High power conversion efficiency with a light load by automatically switching to DCM operation

OPERATION MODES

The ADP3209 runs in RPM mode for the purpose of fast transient response and high light load efficiency. During the following transients, the ADP3209 runs in PWM mode:

- Soft start
- Soft transient: the period of 100 µs following any VID change
- Current overload

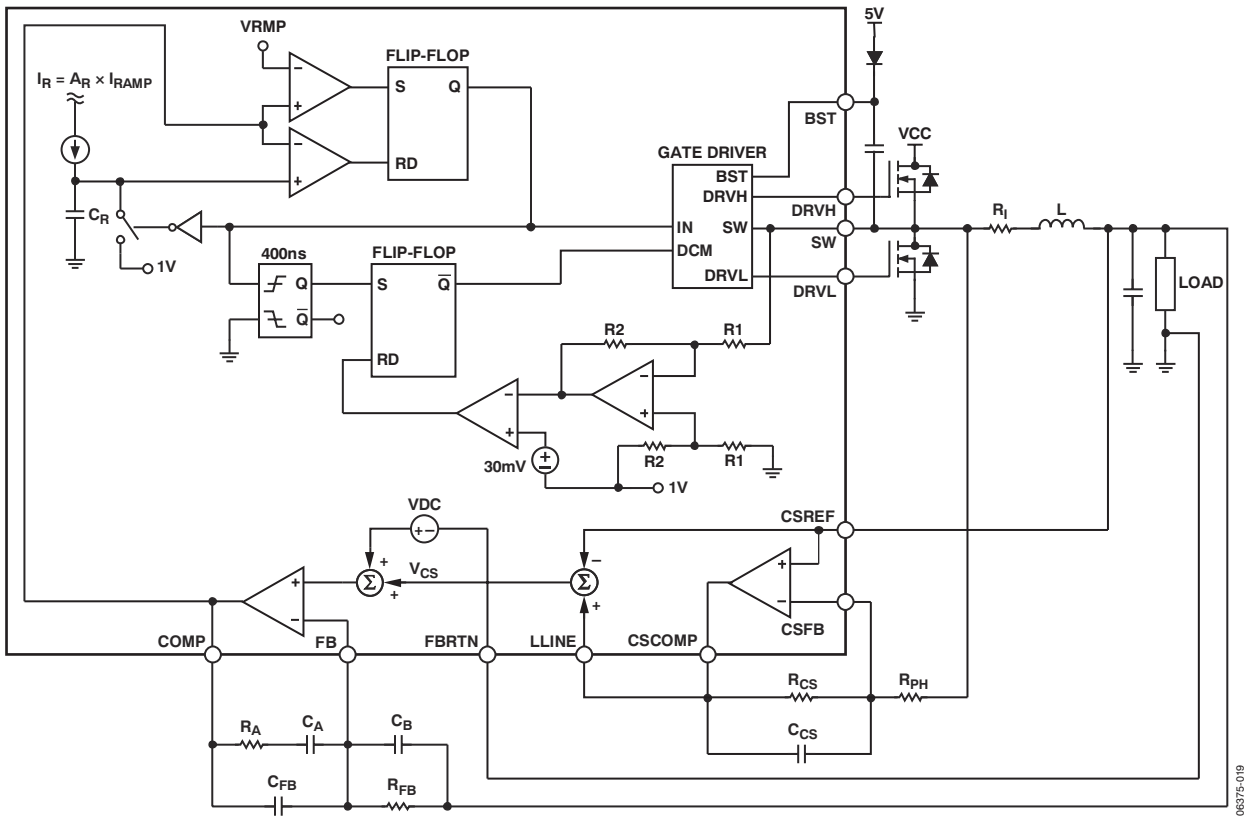


Figure 19. RPM Mode Operation

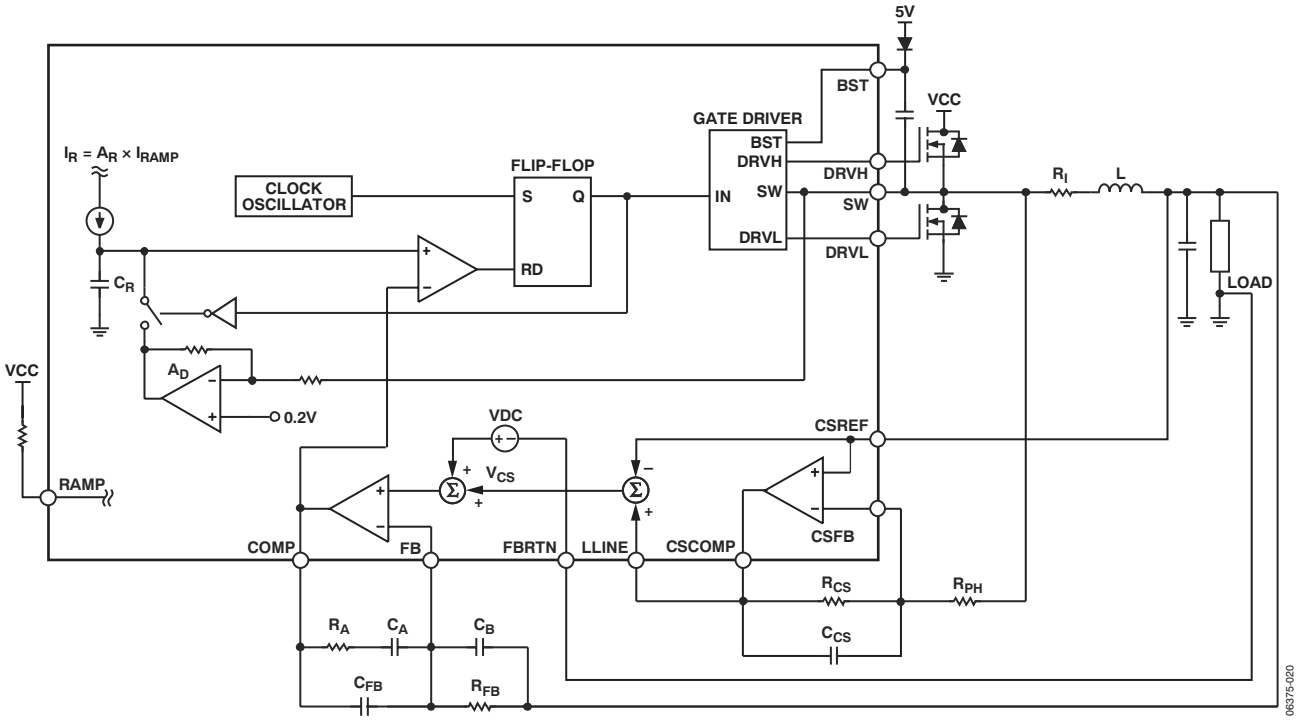


Figure 20. PWM Mode Operation

Setting Switch Frequency

Master Clock Frequency in PWM Mode

When the ADP3209 runs in PWM, the clock frequency is set by an external resistor connected from the RT pin to GND. The frequency varies with the VID voltage: the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage maintains constant V_{CCGFX} ripple and improves power conversion efficiency at lower VID voltages. Figure 9 shows the relationship between clock frequency and VID voltage, parameterized by RT resistance.

Switching Frequency in RPM Mode

When the ADP3209 operates in RPM mode, its switching frequency is controlled by the ripple voltage on the COMP pin. Each time the COMP pin voltage exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor connected between RPM and VRPM, an internal ramp signal is started and DRVH is driven high. The slew rate of the internal ramp is programmed by the current entering the RAMP pin. One-third of the RAMP current charges an internal ramp capacitor (5 pF typical) and creates a ramp. When the internal ramp signal intercepts the COMP voltage, the DRVH pin is reset low.

In continuous current mode, the switching frequency of RPM operation is almost constant. While in discontinuous current conduction mode, the switching frequency is reduced as a function of the load current.

DIFFERENTIAL SENSING OF OUTPUT VOLTAGE

The ADP3209 combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to meet the rigorous accuracy requirement of the Intel IMVP-6+ specification. In steady-state mode, the combination of the VID DAC and error amplifier maintain the output voltage for a worst-case scenario within ±8 mV of the full operating output voltage and temperature range.

The V_{CCGFX} output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point—the VCC remote sensing pin of the GMCH. FBRTN should be connected directly to the negative remote sensing point—the V_{SS} sensing point of the GMCH. The internal VID DAC and precision voltage reference are referenced to FBRTN and have a typical current of 200 μA for guaranteed accurate remote sensing.

OUTPUT CURRENT SENSING

The ADP3209 includes a dedicated current sense amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current and for overcurrent detection. Sensing the current delivered to the load is an inherently more accurate method than detecting peak current or sampling the current across a sense element, such as the low-side MOSFET. The current sense amplifier can be configured several ways, depending on system optimization objectives, and the current information can be obtained by

- Output inductor ESR sensing without the use of a thermistor for the lowest cost
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy
- Discrete resistor sensing for the highest accuracy

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that is, the CSFB pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are connected with a resistor. The feedback resistor between the CSCOMP and CSFB pins sets the gain of the current sense amplifier, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line required by the GMCH specification. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independent from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

ACTIVE IMPEDANCE CONTROL MODE

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning setpoint. The arrangement results in an enhanced feedforward response.

VOLTAGE CONTROL MODE

A high-gain bandwidth error amplifier is used for the voltage mode control loop. The noninverting input voltage is set via the 5-bit VID DAC. The VID codes are listed in Table 4. The noninverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using R_B, a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

POWER-GOOD MONITORING

The power-good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output that can be pulled up through an external resistor to a voltage rail—not necessarily the same VCC voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of this range.

Following the GMCH specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. To prevent a false alarm, the power-good circuit is masked during any VID change and during soft start. The duration of the PWRGD mask is set to approximately 100 µs by an internal timer. In addition, for a VID change from high to low, there is an additional period of PWRGD masking before the voltage of the ST pin drops within 200 mV of the new lower VID DAC output voltage, as shown in Figure 21.

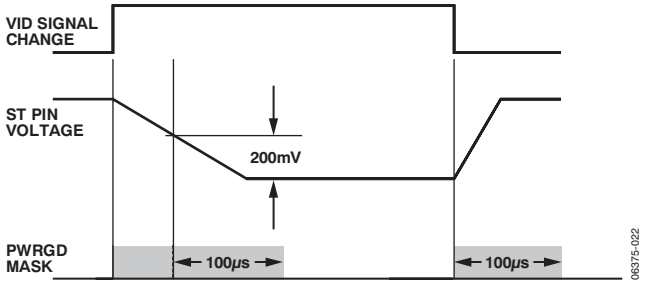


Figure 21. PWRGD Masking for VID Change

POWER-UP SEQUENCE AND SOFT START

The power-on ramp-up time of the output voltage is set with a capacitor tied from the SS pin to GND. The capacitance on the SS pin also determines the current limit latch-off time, as explained in the Current Limit, Short-Circuit, and
Latch-Off Protection section. The power-up sequence, including the soft start is illustrated in Figure 22.

In VCC UVLO or shutdown mode, the SS pin is held at zero potential. When VCC ramps to a value greater than the upper UVLO threshold while EN is asserted high, the ADP3209 enables the internal bias and starts a reset cycle of about 50 µs to 60 µs. When the initial reset is complete, the chip signals to ramp up the SS voltage. During soft start, the external SS capacitor is charged by an internal 8 µA current source. The V_{CCGFX} voltage follows the ramping SS voltage up to the VID code. While the V_{CCGFX} is regulated at the VID code voltage, the SS capacitor continues to rise. When the SS pin voltage reaches 1.7 V, the ADP3209 completes its soft start, PWRGD asserts high, and the chip switches to normal operation.

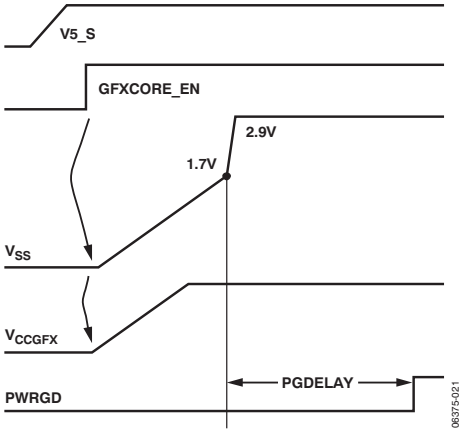


Figure 22. Power-Up Sequence of ADP3209

If EN is taken low or VCC drops below the lower VCC UVLO threshold, the SS capacitor is reset to ground to prepare the chip for a subsequent soft start cycle.

VID CHANGE AND SOFT TRANSIENT

When a VID input changes, the ADP3209 detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 5-bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

The ADP3209 provides a soft transient function to reduce inrush current during VID transitions. Reducing the inrush current helps decrease the acoustic noise generated by the MLCC input capacitors and inductors.

The soft transient feature is implemented with an ST buffer amplifier that outputs constant sink or source current on the ST pin that is connected to an external capacitor. The capacitor is used to program the slew rate of V_{CCGFX} voltage during a VID voltage transient. During steady-state operation, the reference inputs of the voltage error amplifier and the ST amplifier are connected to the VID DAC output. Consequently, the ST voltage is a buffered version of VID DAC output. When a VID change triggers a soft transition, the reference input of the voltage error amplifier switches from the DAC output to the ST output while the input of the ST amplifier

remains connected to the DAC. The ST buffer input recognizes the almost instantaneous VID voltage change and tries to track it. However, tracking is not instantaneous because the slew rate of the buffer is limited by the source and sink current capabilities (7.5 µA and 2.5 µA, respectively) of the ST output. Therefore, the V_{CCGFX} voltage slew rate is controlled. When the transient period is complete, the reference input of the voltage amplifier reverts to the VID DAC output to improve accuracy.

Charging/discharging the external capacitor on the ST pin programs the voltage slew rate of the ST pin and consequently of the V_{CCGFX} output.

CURRENT LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3209 has an adjustable current limit set by the R_{CLIM} resistor. This resistor is connected from the CLIM pin to GND, and the CLIM pin outputs a 10 µA current. The voltage created by 10 µA through R_{CLIM} is divided by 10 and then level shifted and connected in series with CSCOMP to form a current limit threshold. The current sense amplifier sets an output voltage between CSREF and CSCOMP that is proportional to the output current. When the difference in voltage between CSREF and CSCOMP is greater than the current limit threshold, there is a current overload.

Normally, the ADP3209 operates in RPM mode. During a current overload, the ADP3209 switches to PWM mode.

With low impedance loads, the ADP3209 operates in a constant current mode to ensure that the external MOSFETs and inductor function properly and to protect the GPU. With a low constant impedance load, the output voltage decreases to supply only the set current limit. If the output voltage drops below the power-good limit, the PWRGD signal transitions. After the PWRGD single transitions, the SS capacitor begins to discharge with a 2 µA internal constant current sink. When the SS capacitor has discharged voltage from 2.9 V to 1.65 V, the ADP3209 latches off. The current limit latch-off delay time is therefore set by the SS pin capacitance. Figure 23 shows how the ADP3209 reacts to a current overload.

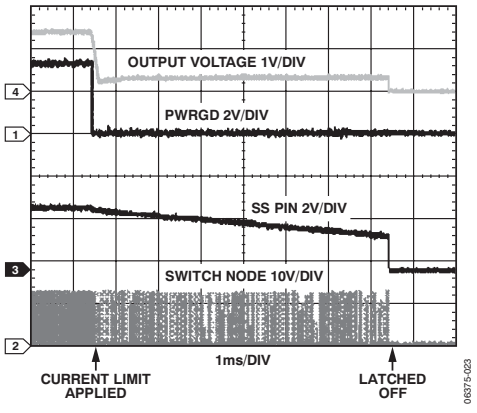


Figure 23. Current Overload

The latch-off function can be reset either by removing and reapplying VCC or by briefly pulling the EN pin low. To disable the current limit latch-off function, an external resistor pulls the SS pin to the VCC voltage to override the 2 µA sink current. This pull-up prevents the SS capacitor from discharging to the 1.65 V latch-off threshold.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot extend below ground. This secondary current limit clamp controls the minimum internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry.

Light Load RPM DCM Operation

The ADP3209 operates in RPM mode. With higher loads, the ADP3209 operates in continuous conduction mode (CCM), and the upper and lower MOSFETs run synchronously and in complementary phase. See Figure 24 for the typical waveforms of the ADP3209 running in CCM with a 7 A load current.

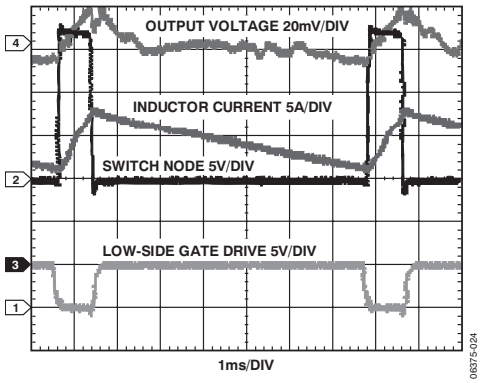


Figure 24. Single-Phase Waveforms in CCM

With lighter loads, the ADP3209 enters discontinuous conduction mode (DCM). Figure 25 shows a typical single-phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 26 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 27 the high-side FET is off and the low-side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high- and low-side FETs are off and no current flows into the inductor (see Figure 28). Figure 29 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the ADP3209 monitors the switch node voltage to determine when to turn off the low-side FET. Figure 30 shows a typical waveform in DCM with a 1 A load current. Between t_1 and t_2, the inductor current ramps down. The current flows through the source drain of the low-side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the

switch voltage approaches 0 V, as seen just before t_2. When the switch voltage is approximately −6 mV, the low-side FET is turned off.

Figure 29 shows a small, dampened ringing at t_2. This is caused by the LC created from capacitance on the switch node, including the C_{DS} of the FETs and the output inductor. This ringing is normal.

The ADP3209 automatically goes into DCM with a light load. Figure 30 shows the typical DCM waveform of the ADP3209 with a 1 A load current. As the load increases, the ADP3209 enters into CCM. In DCM, frequency decreases with load current, and switching frequency is a function of the inductor, load current, input voltage, and output voltage.

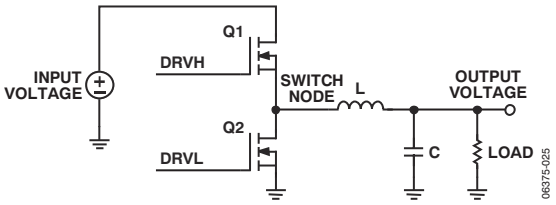


Figure 25. Buck Topology

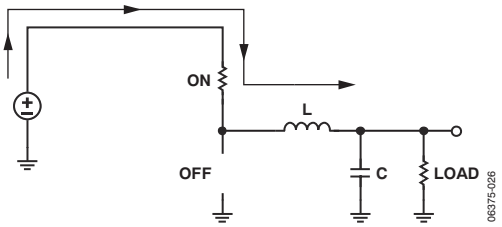


Figure 26. Buck Topology Inductor Current During t_0 and t_1

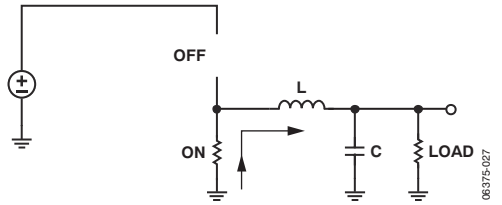


Figure 27. Buck Topology Inductor Current During t_1 and t_2

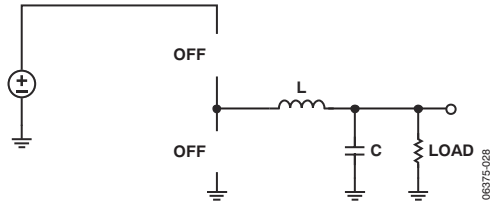


Figure 28. Buck Topology Inductor Current During t_2 and t_3

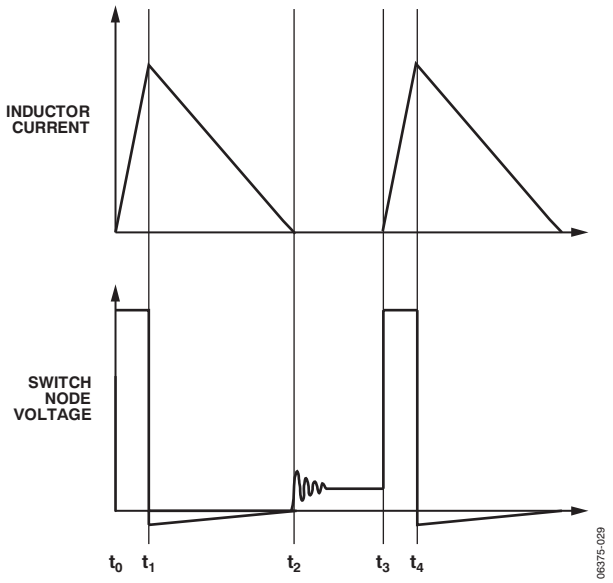


Figure 29. Inductor Current and Switch Node in DCM

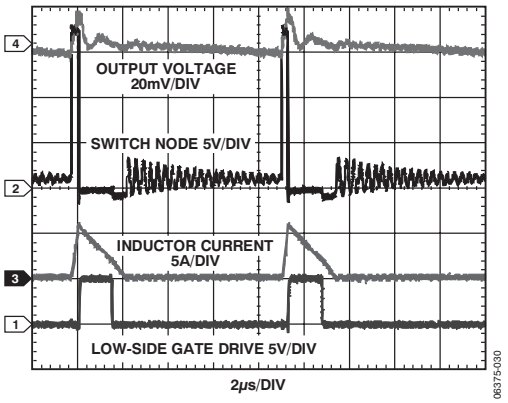


Figure 30. Single-Phase Waveforms in DCM with 1 A Load Current

OUTPUT CROWBAR

To protect the load and output components of the supply, the DRVL output is driven high (turning the low-side MOSFETs on) and DRVH is driven low (turning the high-side MOSFETs off) when the output voltage exceeds the GMCH OVP threshold.

Turning on the low-side MOSFETs forces the output capacitor to discharge and the current to reverse due to current build up in the inductors. If the output overvoltage is due to a drain-source short of the high-side MOSFET, turning on the low-side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the GMCH chipset from destruction.

When the OVP feature is triggered, the ADP3209 is latched off. The latch-off function can be reset by removing and reapplying VCC to the ADP3209 or by briefly pulling the EN pin low.

REVERSE VOLTAGE PROTECTION

Very large reverse current in inductors can cause negative V_{CCGFX} voltage, which is harmful to the chipset and other output components. The ADP3209 provides a reverse voltage

protection (RVP) function without additional system cost. The V_{CCGFX} voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than −300 mV, the ADP3209 triggers the RVP function by setting both DRVH and DRVL low, thus turning off all MOSFETs. The reverse inductor currents can be quickly reset to 0 by discharging the built-up energy in the inductor into the input dc voltage source via the forward-biased body diode of the high-side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns to greater than −100 mV.

Sometimes the crowbar feature inadvertently results in negative V_{CCGFX} voltage because turning on the low-side MOSFETs results in a very large reverse inductor current. To prevent damage to the chipset caused from negative voltage, the ADP3209 maintains its RVP monitoring function even after OVP latch-off. During OVP latch-off, if the CSREF pin voltage drops to less than −300 mV, the low-side MOSFETs is turned off by setting DRVL low. DRVL will be set high again when the CSREF voltage recovers to greater than −100 mV.

Figure 31 shows the reverse voltage protection function of the ADP3209. The CSREF pin is disconnected from the output voltage and pulled negative. As the CSREF pin drops to less than −300 mV, the low-side and high-side FETs turn off.

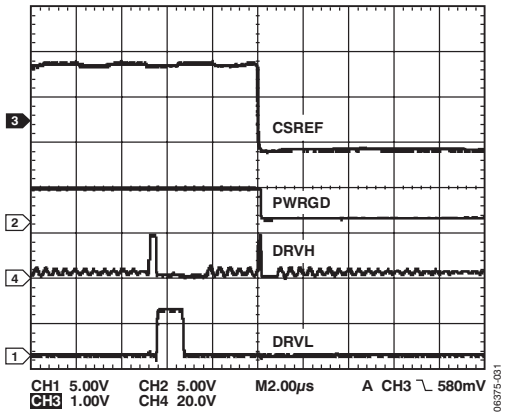


Figure 31. ADP3209 RVP Function

OUTPUT ENABLE AND UVLO

For the ADP3209 to begin switching, the VCC supply voltage to the controller must be greater than the V_{CCOK} threshold and the EN pin must be driven high. If the VCC voltage is less than the V_{CCUVLO} threshold or the EN pin is logic low, the ADP3209 shuts off. In shutdown mode, the controller holds DRVH and DRVL low, shorts the capacitors of the SS and PGDELAY pins to ground, and drives PWRGD to low.

The user must adhere to proper power-supply sequencing during startup and shutdown of the ADP3209. All input pins must be at ground prior to removing or applying VCC, and all output pins should be left in high impedance state while VCC is off.

POWER MONITOR FUNCTION

The ADP3209 includes a power monitor function. The PMON pin is an open-drain MOSFET. A pull-up resistor is required on PMON. PMON switches at a duty cycle proportional to the load current. The full-scale duty cycle of PMON at the maximum load current is set by a resistor, R_{PMONFS}, connected from PMONFS to GND. R_{PMONFS} also sets the switching frequency of the PMON open-drain transistor.

Connecting an RC to PMON will average the PMON voltage. If the PMON pull-up resistor is connected to a dc voltage, the average PMON voltage is proportional to the load current. Figure 32 shows the PMON function used to monitor load current.

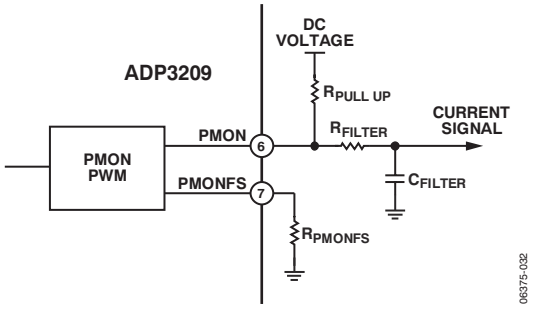


Figure 32. PMON Current Monitor Configuration

Because the output voltage of the ADP3209 can vary in the same application, the average PMON voltage is proportional to the load current, but not to the output power. Connecting the PMON pull-up resistor to V_{CCGFX} results in a PMON average voltage that is proportional to the output power.

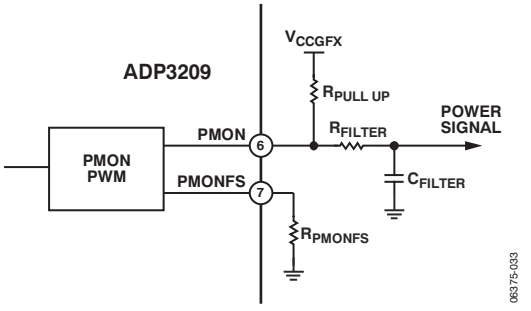


Figure 33. PMON Power Monitor Configuration

Table 4. VID Codes

Enable	VID4	VID3	VID2	VID1	VID0	Nominal V_{CCGFX} (V)
1	0	0	0	0	0	1.250
1	0	0	0	0	1	1.225
1	0	0	0	1	0	1.200
1	0	0	0	1	1	1.175
1	0	0	1	0	0	1.150
1	0	0	1	0	1	1.125
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.075
1	0	1	0	0	0	1.050
1	0	1	0	0	1	1.025
1	0	1	0	1	0	1.000
1	0	1	0	1	1	0.975
1	0	1	1	0	0	0.950
1	0	1	1	0	1	0.925
1	0	1	1	1	0	0.900
1	0	1	1	1	1	0.875
1	1	0	0	0	0	0.850
1	1	0	0	0	1	0.825
1	1	0	0	1	0	0.800
1	1	0	0	1	1	0.775
1	1	0	1	0	0	0.750
1	1	0	1	0	1	0.725
1	1	0	1	1	0	0.700
1	1	0	1	1	1	0.675
1	1	1	0	0	0	0.650
1	1	1	0	0	1	0.625
1	1	1	0	1	0	0.600
1	1	1	0	1	1	0.575
1	1	1	1	0	0	0.550
1	1	1	1	0	1	0.525
1	1	1	1	1	0	0.500
1	1	1	1	1	1	0.400
0	X	X	X	X	X	0.000

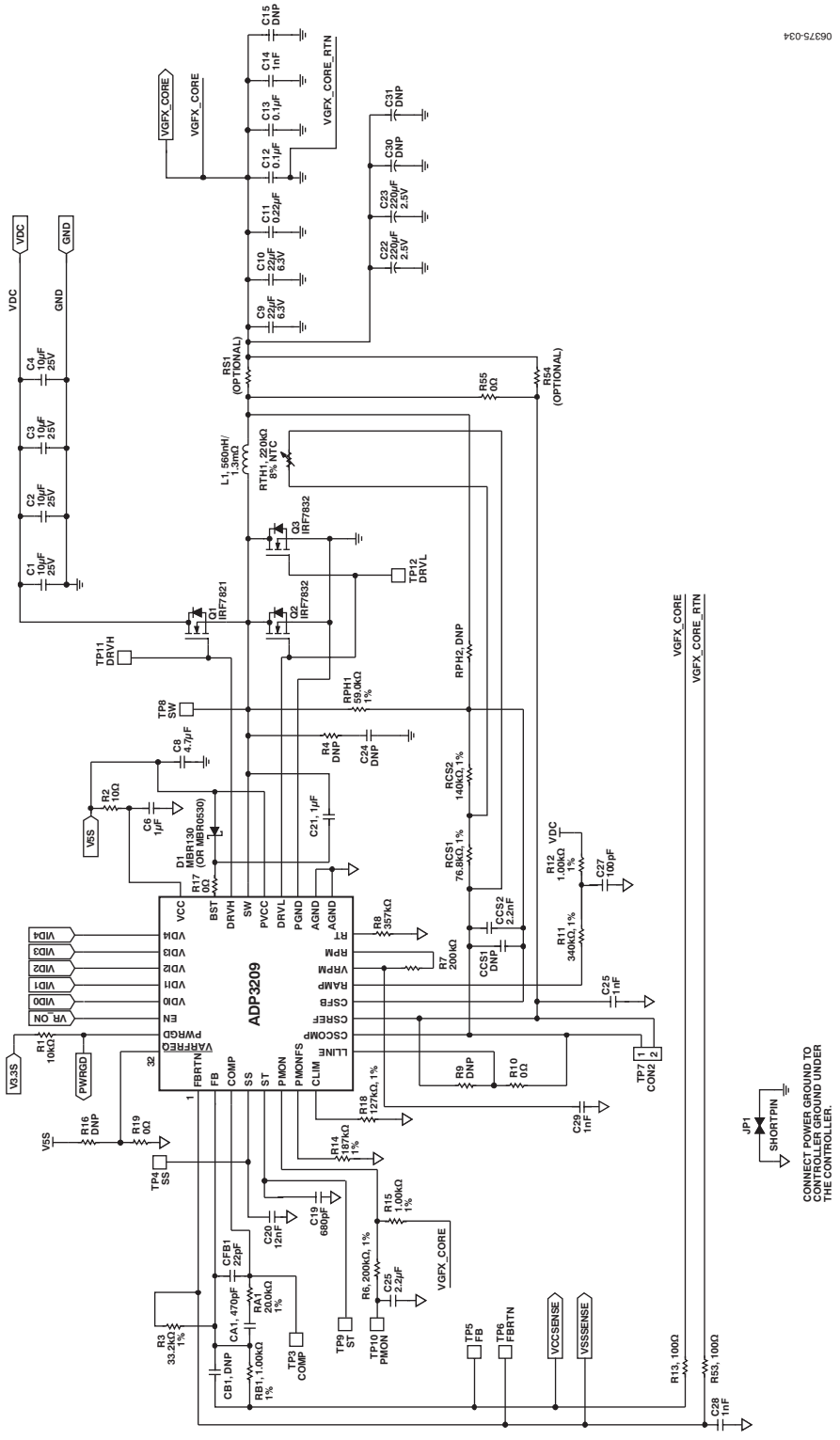


Figure 34. Typical Application Circuit

APPLICATION INFORMATION

The design parameters for a typical IMVP-6+-compliant GPU core VR application are as follows:

- Maximum input voltage (V_{INMAX}) = 19 V
- Minimum input voltage (V_{INMIN}) = 8 V
- Output voltage by VID setting (V_{VID}) = 1.25 V
- Maximum output current (I_O) = 15 A
- Droop resistance (R_O) = 5.1 mΩ
- Nominal output voltage at 15 A load (V_{OFL}) = 1.174 V
- Static output voltage drop from no load to full load (ΔV) = $V_{ONL} - V_{OFL}$ = 1.25 V − 1.174 V = 76 mV
- Maximum output current step (ΔI_O) = 8 A
- Number of phases (n) = 1
- Switching frequency (f_{SW}) = 390 kHz
- Duty cycle at maximum input voltage (D_{MAX}) = 0.15 V
- Duty cycle at minimum input voltage (D_{MIN}) = 0.062 V

SETTING THE CLOCK FREQUENCY FOR PWM

In PWM operation, the ADP3209 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (RT). The clock frequency determines the switching frequency, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For example, a clock frequency of 300 kHz sets the switching frequency to 300 kHz. This selection represents the trade-off between the switching losses and the minimum sizes of the output filter components. To achieve a 300 kHz oscillator frequency at a VID voltage of 1.2 V, RT must be 452 kΩ. Alternatively, the value for RT can be calculated by using the following equation:

$$RT = \frac{V_{VID} + 1.0\ \text{V}}{2 \times f_{SW} \times 7.2\ \text{pF}} - 35\ \text{k}\Omega \quad (1)$$

where:
7.2 pF and 35 kΩ are internal IC component values.
V_{VID} is the VID voltage in volts.
f_{SW} is the switching frequency in hertz.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

With $\overline{\text{VARFREQ}}$ pulled above 4 V, the ADP3209 operates with a constant switching frequency. The switching frequency does not change with VID voltage, input voltage, or load current. In addition, the DCM operation at light load is disabled, so the ADP3209 operates in CCM. The value of RT can be calculated by using the following equation:

$$RT = \frac{1.6\ \text{V}}{f_{SW} \times 7.2\ \text{pF}} - 35\ \text{k}\Omega$$

SETTING THE SWITCHING FREQUENCY FOR RPM OPERATION

During the RPM operation, the ADP3209 runs in pseudoconstant frequency if the load current is high enough for continuous current mode. While in DCM, the switching frequency is reduced with the load current in a linear manner. To save power with light loads, lower switching frequency is usually preferred during RPM operation. However, the V_{CCGFX} ripple specification of IMVP-6+ sets a limitation for the lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM can be equal to, greater than, or less than its counterpart in PWM.

A resistor between the VRPM and RPM pins sets the pseudoconstant frequency as follows:

$$R_{RPM} = \frac{4 \times RT}{(V_{VID} + 1.0\ \text{V})} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (2)$$

where:
A_R is the internal ramp amplifier gain.
C_R is the internal ramp capacitor value.
R_R is an external resistor on the RAMP pin to set the internal ramp magnitude (see the Ramp Resistor Selection section for information about the design of R_R resistance).

If R_R = 340 kΩ, the following resistance results in 390 kHz switching frequency in RPM operation.

$$R_{RPM} = \frac{4 \times 357\ \text{k}\Omega}{1.174\ \text{V} + 1.0\ \text{V}} \times \frac{0.2 \times (1 - 0.062) \times 1.174}{390\ \text{k}\Omega \times 5\ \text{pF} \times 390\ \text{kHz}} = 218\ \text{k}\Omega$$

SOFT START AND CURRENT LIMIT LATCH-OFF DELAY TIMES

The soft start and current limit latch-off delay functions share the SS pin; consequently, these parameters must be considered together. First, set C_{SS} for the soft start ramp. This ramp is generated with an 8 μA internal current source. The value for C_{SS} can be calculated as

$$C_{SS} = \frac{8\ \mu\text{A} \times t_{SS}}{V_{VID}} \quad (3)$$

where t_{SS} is the desired soft start time and is recommended in IMVP-6+ to be less than 3 ms.

Therefore, assuming a desired soft start time of 2 ms, C_{SS} is 13.3 nF, and the closest standard capacitance is 12 nF.

After C_{SS} is set, the current limit latch-off time can be calculated by using the following equation:

$$t_{DELAY} = \frac{1.2\ \text{V} \times C_{SS}}{2\ \mu\text{A}} \quad (4)$$

where C_{SS} is 7.2 ms.

INDUCTOR SELECTION

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller-size inductors, and for a specified peak-to-peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. For a buck converter, the practical value for peak-to-peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 5 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current. Equation 6 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times (1 - D_{MIN})}{f_{SW} \times L} \quad (5)$$

$$L \geq \frac{V_{VID} \times R_O \times (1 - D_{MIN})}{f_{SW} \times V_{RIPPLE}} \quad (6)$$

In this example, R_O is assumed to be the ESR of the output capacitance, which results in an optimal transient response. Solving Equation 6 for a 16 mV peak-to-peak output ripple voltage yields

$$L \geq \frac{1.174\ \text{V} \times 5.1\ \text{m}\Omega \times (1 - 0.062)}{390\ \text{kHz} \times 16\ \text{mV}} = 901\ \text{nH}$$

If the resultant ripple voltage is less than the initially selected value, the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling. In this example, the iteration showed that a 560 nH inductor was sufficient to achieve a good ripple.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 560 nH inductor is a good choice for a starting point, and it provides a calculated ripple current of 6.6 A. The inductor should not saturate at the peak current of 18.3 A, and it should be able to handle the sum of the power dissipation caused by the winding's average current (15 A) plus the ac core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the inductor current. Too large of a DCR causes excessive power losses, whereas too small of a value leads to increased measurement error. For this example, an inductor with a DCR of 1.3 mΩ is used.

Selecting a Standard Inductor

After the inductance and DCR are known, select a standard inductor that best meets the overall design goals. It is also important to specify the inductance and DCR tolerance to maintain the accuracy of the system. Using 20% tolerance for the inductance and 15% for the DCR at room temperature are reasonable values that most manufacturers can meet.

Power Inductor Manufacturers

The following companies provide surface-mount power inductors optimized for high power applications upon request.

- Vishay Dale Electronics, Inc.
  (605) 665-9301
- Panasonic
  (714) 373-7334
- Sumida Electric Company
  (847) 545-6700
- NEC Tokin Corporation
  (510) 324-4110

Output Droop Resistance

The design requires that the regulator output voltage measured at the chipset pins decreases when the output current increases. The specified voltage drop corresponds to the droop resistance (R_O).

The output current is measured by low-pass filtering the voltage across the inductor or current sense resistor. The filter is implemented by the CS amplifier that is configured with R_{PH}, R_{CS}, and C_{CS}. The output resistance of the regulator is set by the following equations:

$$R_O = \frac{R_{CS}}{R_{PH}} \times R_{SENSE} \quad (7)$$

$$C_{CS} = \frac{L}{R_{SENSE} \times R_{CS}} \quad (8)$$

where R_{SENSE} is the DCR of the output inductors.

Either R_{CS} or R_{PH} can be chosen for added flexibility. Due to the current drive ability of the CSCOMP pin, the R_{CS} resistance should be greater than 100 kΩ. For example, initially select R_{CS} to be equal to 200 kΩ, and then use Equation 8 to solve for C_{CS}:

$$C_{CS} = \frac{560\ \text{nH}}{1.3\ \text{m}\Omega \times 200\ \text{k}\Omega} = 2.2\ \text{nF}$$

If C_{CS} is not a standard capacitance, R_{CS} can be tuned. In this case, the required C_{CS} is a standard value and no tuning is required. For best accuracy, C_{CS} should be a 5% NPO capacitor.

Next, solve for R_{PH} by rearranging Equation 7 as follows:

$$R_{PH} \geq \frac{1.3\ \text{m}\Omega}{5.1\ \text{m}\Omega} \times 200\ \text{k}\Omega = 51.0\ \text{k}\Omega$$

The standard 1% resistor for R_{PH} is 51.1 kΩ.

Inductor DCR Temperature Correction

If the DCR of the inductor is used as a sense element and copper wire is the source of the DCR, the temperature changes associated with the inductor's winding must be compensated for. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite but equal percentage of change in resistance, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, series resistors R_{CS1} and R_{CS2} (see Figure 35) are needed to linearize the NTC and produce the desired temperature coefficient tracking.

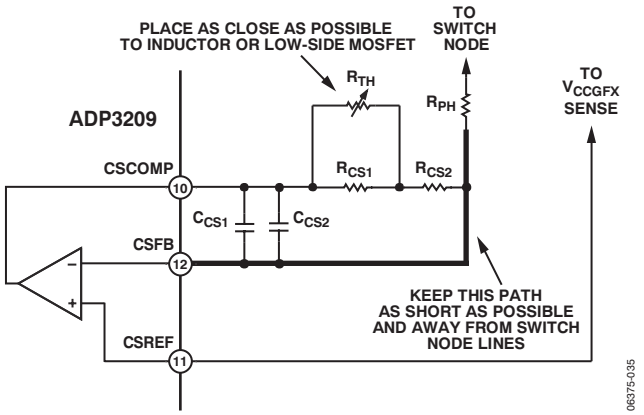


Figure 35. Temperature-Compensation Circuit Values

The following procedure and expressions yield values for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on its type and value. Because the value needed is not yet determined, start with a thermistor with a value close to R_{CS} and an NTC with an initial tolerance of better than 5%.
2. Find the relative resistance value of the NTC at two temperatures. The appropriate temperatures will depend on the type of NTC, but 50°C and 90°C have been shown to work well for most types of NTCs. The resistance values are called A (A is $R_{TH}(50°C)/R_{TH}(25°C)$) and B (B is $R_{TH}(90°C)/R_{TH}(25°C)$). Note that the relative value of the NTC is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of the two temperatures. The relative value of R_{CS} is based on the percentage of change needed, which is initially assumed to be 0.39%/°C in this example. The relative values are called r_1 (r_1 is $1/(1+ TC \times (T_1 - 25))$) and r_2 (r_2 is $1/(1 + TC \times (T_2 - 25))$), where TC is 0.0039, T_1 is 50°C, and T_2 is 90°C.
4. Compute the relative values for r_{CS1}, r_{CS2}, and r_{TH} by using the following equations:

$$r_{CS2} = \frac{(A-B)\times r_1 \times r_2 - A\times(1-B)\times r_2 + B\times(1-A)\times r_1}{A\times(1-B)\times r_1 - B\times(1-A)\times r_2 - (A-B)} \quad (9)$$

$$r_{CS1} = \frac{(1-A)}{\frac{1}{1-r_{CS2}} - \frac{A}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{1}{\frac{1}{1-r_{CS2}} - \frac{1}{r_{CS1}}}$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, and then select a thermistor of the closest value available. In addition, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (10)$$

6. Calculate values for R_{CS1} and R_{CS2} by using the following equations:

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \quad (11)$$

$$R_{CS2} = R_{CS} \times ((1-k) + (k \times r_{CS2}))$$

For example, if a thermistor value of 100 kΩ is selected in Step 1, an available 0603-size thermistor with a value close to R_{CS} is the Vishay NTHS0603N04 NTC thermistor, which has resistance values of A = 0.3359 and B = 0.0771. Using the equations in Step 4, r_{CS1} is 0.359, r_{CS2} is 0.729, and r_{TH} is 1.094. Solving for r_{TH} yields 219 kΩ, so a thermistor of 220 kΩ would be a reasonable selection, making k equal to 1.005. Finally, R_{CS1} and R_{CS2} are found to be 72.2 kΩ and 146 kΩ. Choosing the closest 1% resistor values yields a choice of 71.5 kΩ and 147 kΩ.

C_{OUT} SELECTION

The required output decoupling for processors and platforms is typically recommended by Intel. For systems containing both bulk and ceramic capacitors, however, the following guidelines can be a helpful supplement.

Select the number of ceramics and determine the total ceramic capacitance (C_Z). This is based on the number and type of capacitors used. Keep in mind that the best location to place ceramic capacitors is inside the socket; however, the physical limit is twenty 0805-size pieces inside the socket. Additional ceramic capacitors can be placed along the outer edge of the socket. A combined ceramic capacitor value of 40 µF to 50 µF is recommended and is usually composed of multiple 10 µF or 22 µF capacitors.

Ensure that the total amount of bulk capacitance (C_X) is within its limits. The upper limit is dependent on the VID on-the-fly output voltage stepping (voltage step, V_V, in time, t_V, with error of V_{ERR}); the lower limit is based on meeting the critical capacitance for load release at a given maximum load step, ΔI_O. The current version of the IMVP-6+ specification allows a maximum V_{CCGFX} overshoot (V_{OSMAX}) of 10 mV more than the VID voltage for a step-off load current.

$$C_{X(MIN)} \geq \left(\frac{L \times \Delta I_O}{\left(R_O + \frac{V_{OSMAX}}{\Delta I_O} \right) \times V_{VID}} - C_Z \right) \quad (12)$$

$$C_{X(MAX)} \leq \frac{L}{k^2 \times R_O^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_v \frac{V_{VID}}{V_V} \times \frac{k \times R_O}{L} \right)^2} - 1 \right) - C_Z$$

$$\text{where } k = -\ln\left(\frac{V_{ERR}}{V_V} \right) \quad (13)$$

To meet the conditions of these expressions and the transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance, R_O. If the $C_{X(MIN)}$ is greater than $C_{X(MAX)}$, the system does not meet the VID on-the-fly specifications and may require less inductance. In addition, the switching frequency may have to be increased to maintain the output ripple.

For example, if two pieces of 22 µF, 0805-size MLC capacitors (C_Z = 44 µF) are used during a VID voltage change, the V_{CCGFX} change is 220 mV in 22 µs with a setting error of 10 mV. If k = 3.1, solving for the bulk capacitance yields

$$C_{X(MIN)} \geq \left(\frac{560\text{ nH} \times 8\text{ A}}{\left(5.1\text{ m}\Omega + \frac{10\text{ mV}}{8\text{ A}} \right) \times 1.174\text{ V}} - 44\text{ µF} \right) = 256\text{ µF}$$

$$C_{X(MAX)} \leq \frac{560\text{ nH} \times 220\text{ mV}}{3.1^2 \times (5.1\text{ m}\Omega)^2 \times 1.174\text{ V}} \times$$

$$\left(\sqrt{1 + \left(\frac{22\text{ µs} \times 1.174\text{ V} \times 3.1 \times 5.1\text{ m}\Omega}{220\text{ mV} \times 560\text{ nH}} \right)^2} - 1 \right) - 44\text{ µF}$$

= 992 µF

Using two 220 µF Panasonic SP capacitors with a typical ESR of 7 mΩ each yields C_X = 440 µF and R_X = 3.5 mΩ.

Ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change. This is tested using

$$L_X \leq C_Z \times R_O{}^2 \times Q^2 \quad (14)$$

$$L_X \leq 44\text{ µF} \times (5.1\text{ m}\Omega)^2 \times 2 = 2.3\text{ nH}$$

where:
Q is limited to the square root of 2 to ensure a critically damped system.
L_X is about 450 pH for the two SP capacitors, which is low enough to avoid ringing during a load change. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased to prevent excessive ringing.

For this multimode control technique, an all ceramic capacitor design can be used if the conditions of Equations 12, 13, and 14 are satisfied.

POWER MOSFETS

For typical 15 A per phase applications, the N-channel power MOSFETs are selected for one high-side switch and one low-side switch. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. Because the voltage of the gate driver is 5 V, logic-level threshold MOSFETs must be used.

The maximum output current, I_O, determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With conduction losses being dominant, the following expression shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and the average total output current (I_O):

$$P_{SF} = (1-D)\times\left[\left(\frac{I_O}{n_{SF}}\right)^2 + \frac{1}{12}\times\left(\frac{I_R}{n_{SF}}\right)^2\right]\times R_{DS(SF)} \quad (15)$$

where:
D is the duty cycle and is approximately the output voltage divided by the input voltage.
I_R is the inductor peak-to-peak ripple current and is approximately

$$I_R = \frac{(1-D)\times V_{OUT}}{L\times f_{SW}}$$

Knowing the maximum output current and the maximum allowed power dissipation, the user can calculate the required $R_{DS(ON)}$ for the MOSFET. For an 8-lead SOIC or 8-lead SOIC-compatible MOSFET, the junction-to-ambient (PCB) thermal impedance is 50°C/W. In the worst case, the PCB temperature is 70°C to 80°C during heavy load operation of the notebook, and a safe limit for P_{SF} is about 0.8 W to 1.0 W at 120°C junction temperature. Therefore, for this example (15 A maximum), the $R_{DS(SF)}$ per MOSFET is less than 18.8 mΩ for the low-side MOSFET. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C; therefore, the $R_{DS(SF)}$ per MOSFET should be less than 13.3 mΩ at room temperature, or 18.8 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input must be small (less than 10% is recommended) to prevent accidentally turning on the synchronous MOSFETs when the switch node goes high.

The high-side (main) MOSFET must be able to handle two main power dissipation components: conduction losses and switching losses. Switching loss is related to the time for the main MOSFET to turn on and off and to the current and voltage that are being switched. Basing the switching speed on the rise and fall times of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET:

$$P_{S(MF)} = 2\times f_{SW}\times\frac{V_{DC}\times I_O}{n_{MF}}\times R_G\times n_{MF}\times C_{ISS} \quad (16)$$

where:
n_{MF} is the total number of main MOSFETs.
R_G is the total gate resistance.
C_{ISS} is the input capacitance of the main MOSFET.

The most effective way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D\times\left[\left(\frac{I_O}{n_{MF}}\right)^2 + \frac{1}{12}\times\left(\frac{I_R}{n_{MF}}\right)^2\right]\times R_{DS(MF)} \quad (17)$$

where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, a user wants the highest speed (low C_{ISS}) device for a main MOSFET, but such a device usually has higher on resistance. Therefore, the user must select a device that meets the total power dissipation (about 0.8 W to 1.0 W for an 8-lead SOIC) when combining the switching and conduction losses.

For example, an IRF7821 device can be selected as the main MOSFET (one in total; that is, n_{MF} = 1), with approximately C_{ISS} = 1010 pF (maximum) and $R_{DS(MF)}$ = 18 mΩ (maximum at T_J = 120°C), and an IR7832 device can be selected as the synchronous MOSFET (two in total; that is, n_{SF} = 2), with $R_{DS(SF)}$ = 6.7 mΩ (maximum at T_J = 120°C). Solving for the power dissipation per MOSFET at I_O = 15 A and I_R = 5.0 A yields 178 mW for each synchronous MOSFET and 446 mW for each main MOSFET. A third synchronous MOSFET is an option to further increase the conversion efficiency and reduce thermal stress.

Finally, consider the power dissipation in the driver. This is best described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{SW}}{2\times n}\times\left(n_{MF}\times Q_{GMF} + n_{SF}\times Q_{GSF}\right) + I_{CC}\right]\times VCC \quad (18)$$

where Q_{GMF} is the total gate charge for each main MOSFET, and Q_{GSF} is the total gate charge for each synchronous MOSFET.

The previous equation also shows the standby dissipation (I_{CC} times the VCC) of the driver.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used to set the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of stability and transient response. Use the following expression to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad (19)$$

$$R_R = \frac{0.2 \times 560\ \text{nH}}{3 \times 5 \times 3.4\ \text{m}\Omega \times 5\ \text{pF}} = 439\ \text{k}\Omega$$

where:
A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low-side MOSFET on resistance.
C_R is the internal ramp capacitor value.

Another consideration in the selection of R_R is the size of the internal ramp voltage (see Equation 20). For stability and noise immunity, keep the ramp size larger than 0.5 V. Taking this into consideration, the value of R_R in this example is selected as 340 kΩ.

The internal ramp voltage magnitude can be calculated as follows:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (20)$$

$$V_R = \frac{0.2 \times (1 - 0.062) \times 1.174\ \text{V}}{340\ \text{k}\Omega \times 5\ \text{pF} \times 390\ \text{kHz}} = 0.33\ \text{V}$$

The size of the internal ramp can be increased or decreased. If it is increased, stability and transient response improves but thermal balance degrades. Conversely, if the ramp size is decreased, thermal balance improves but stability and transient response degrade. In the denominator of Equation 19, the factor of 3 sets the minimum ramp size that produces an optimal balance of good stability and transient response.

COMP PIN RAMP

In addition to the internal ramp, there is a ramp signal on the COMP pin due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - D)}{f_{SW} \times C_X \times R_O}\right)} \quad (21)$$

where C_X is the total bulk capacitance, and R_O is the droop resistance of the regulator.

For this example, the overall ramp signal is 0.23 V.

CURRENT LIMIT SETPOINT

To select the current limit setpoint, the resistor value for R_{CLIM} must be determined. The current limit threshold for the ADP3209 is set with R_{CLIM}. R_{CLIM} can be found using the following equation:

$$R_{CLIM} = \frac{R_{CS} \times 10 \times R_{SENSE} \times I_{CLIM}}{R_{PH} \times 10\ \mu\text{A}} \quad (22)$$

where:
R_{PH} is the resistor connecting the current sense resistor or inductor switch node to the current sense amplifier.
R_{CS} is the current sense amplifier feedback resistor.
R_{SENSE} is the sense current resistor or the inductor DCR.
I_{CLIM} is the current limit setpoint.

If R_{CLIM} is greater than 500 kΩ, the current limit may be lower than expected and require an adjustment of R_{CLIM}. In this example, I_{CLIM} is the average current limit for the output of the supply. For this example, choosing 20 A for I_{CLIM}, results in an R_{CLIM} of 104 kΩ.

POWER MONITOR

The PMON duty cycle is proportional to the load current. R_{PMONFS} sets the maximum duty cycle at the maximum current.

$$R_{PMONFS} = \frac{\left(I_{LOAD} \times R_O \times 9\right) + 1\ \text{V}}{10\ \mu\text{A}} \quad (23)$$

where I_{LOAD} is the load current in amps when PMON is 100% duty cycle, and R_O is the droop resistance in ohms.

When PMON is connected with a pull-up resistor to the output voltage, as shown in Figure 33, the average PMON voltage is given by

$$PMON = \frac{V_{GFX} \times I_{LOAD} \times R_O \times 9}{\left(R_{MONFS} \times 10\ \mu\text{A}\right) - 1\ \text{V}} \quad (24)$$

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3209 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and that is equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion with the load current at any load current slew rate, ensuring the optimal position and allowing the minimization of the output decoupling.

With the multimode feedback structure of the ADP3209, it is necessary to set the feedback compensation so that the converter's output impedance works in parallel with the output decoupling. In addition, it is necessary to compensate for the several poles and zeros created by the output inductor and decoupling capacitors (output filter).

A Type III compensator on the voltage feedback is adequate for proper compensation of the output filter. Figure 36 shows the Type III amplifier used in the ADP3209. Figure 37 shows the locations of the two poles and two zeros created by this amplifier.

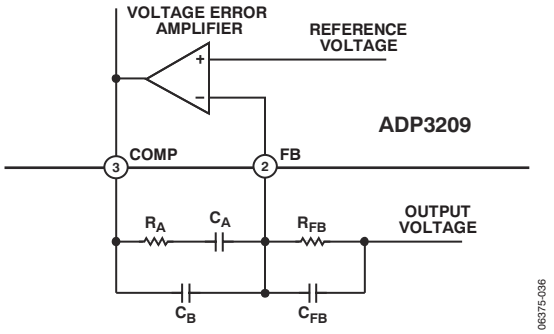


Figure 36. Voltage Error Amplifier

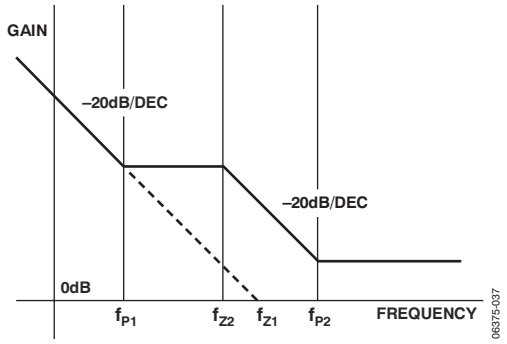


Figure 37. Poles and Zeros of Voltage Error Amplifier

The following equations give the locations of the poles and zeros shown in Figure 37:

$$f_{Z1} = \frac{1}{2\pi \times C_A \times R_A} \quad (25)$$

$$f_{Z2} = \frac{1}{2\pi \times C_{FB} \times R_{FB}} \quad (26)$$

$$f_{P1} = \frac{1}{2\pi (C_A + C_B) \times R_{FB}} \quad (27)$$

$$f_{P2} = \frac{C_A + C_B}{2\pi \times R_A \times C_B \times C_A} \quad (28)$$

The expressions that follow compute the time constants for the poles and zeros in the system and are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning Procedure for ADP3209 section):

$$R_E = R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - (n \times D)) \times V_{RT}}{C_X \times R_O \times V_{VID}} \quad (29)$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \quad (30)$$

$$T_B = (R_X + R' - R_O) \times C_X \quad (31)$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}} \right)}{V_{VID} \times R_E} \quad (32)$$

$$T_D = \frac{C_X \times C_Z \times R_O^2}{C_X \times (R_O - R') + C_Z \times R_O} \quad (33)$$

where:

R' is the PCB resistance from the bulk capacitors to the ceramics and is approximately 0.4 mΩ (assuming an 8-layer motherboard).

R_{DS} is the total low-side MOSFET for on resistance.

A_D is 5.

V_{RT} is 1.25 V.

L_X is the ESL of the bulk capacitors (450 pH for the two Panasonic SP capacitors).

The compensation values can be calculated as follows:

$$C_A = \frac{R_O \times T_A}{R_E \times R_B} \quad (34)$$

$$R_A = \frac{T_C}{C_A} \quad (35)$$

$$C_B = \frac{T_B}{R_B} \quad (36)$$

$$C_{FB} = \frac{T_D}{R_A} \quad (37)$$

The standard values for these components are subject to the tuning procedure described in the Tuning Procedure for ADP3209 section.

C_{IN} SELECTION AND INPUT CURRENT di/dt REDUCTION

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to V_{OUT}/V_{IN}. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum rms current. The maximum rms capacitor current occurs at the lowest input voltage and is given by

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{D} - 1} \quad (38)$$

$$I_{CRMS} = 0.15 \times 15\,\text{A} \times \sqrt{\frac{1}{0.15} - 1} = 5.36\,\text{A}$$

where I_O is the output current.

In a typical notebook system, the battery rail decoupling is achieved by using MLC capacitors or a mixture of MLC capacitors and bulk capacitors. In this example, the input capacitor bank is formed by four pieces of 10 µF, 25 V MLC capacitors, with a ripple current rating of about 1.5 A each.

SOFT TRANSIENT SETTING

As described in the Theory of Operation section, during the soft transient, the slew rate of the V_{CCGFX} reference voltage change is controlled by the ST pin capacitance. The ST pin capacitance is set to satisfy the slew rate for a fast exit as follows:

$$C_{ST} = \frac{7.5\,\mu\text{A}}{SLEWRATE} \quad (39)$$

where:
7.5 µA is the source/sink current of the ST pin.
SLEWRATE is the voltage slew rate after a change in VID voltage and is defined as 10 mV/µA in the IMVP-6+ specification.
C_{ST} is 750 pF, and the closest standard capacitance is 680 pF.

TUNING PROCEDURE FOR ADP3209

Set Up and Test the Circuit

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Connect a dc load to the circuit.
3. Turn on the ADP3209 and verify that it operates properly.
4. Check for jitter with no load and full load conditions.

Set the DC Load Line

1. Measure the output voltage with no load (V_{NL}) and verify that this voltage is within the specified tolerance range.
2. Measure the output voltage with a full load when the device is cold (V_{FLCOLD}). Allow the board to run for ~10 minutes with a full load and then measure the output when the device is hot (V_{FLHOT}). If the difference between the two measured voltages is more than a few millivolts, adjust R_{CS2} using Equation 40.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad (40)$$

3. Repeat Step 2 until no adjustment of R_{CS2} is needed.
4. Compare the output voltage with no load to that with a full load using 5 A steps. Compute the load line slope for each change and then find the average to determine the overall load line slope (R_{OMEAS}).
5. If the difference between R_{OMEAS} and R_O is more than 0.05 mΩ, use the following equation to adjust the R_{PH} values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad (41)$$

6. Repeat Steps 4 and 5 until no adjustment of R_{PH} is needed. Once this is achieved, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the rest of the procedure.
7. Measure the output ripple with no load and with a full load with scope, making sure both are within the specifications.

Set the AC Load Line

1. Remove the dc load from the circuit and connect a dynamic load.
2. Connect the scope to the output voltage and set it to dc coupling mode with a time scale of 100 µs/div.
3. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
4. Measure the output waveform (note that use of a dc offset on the scope may be necessary to see the waveform). Try to use a vertical scale of 100 mV/div or finer.
5. The resulting waveform will be similar to that shown in Figure 38. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 38. Do not measure the undershoot or overshoot that occurs immediately after the step.

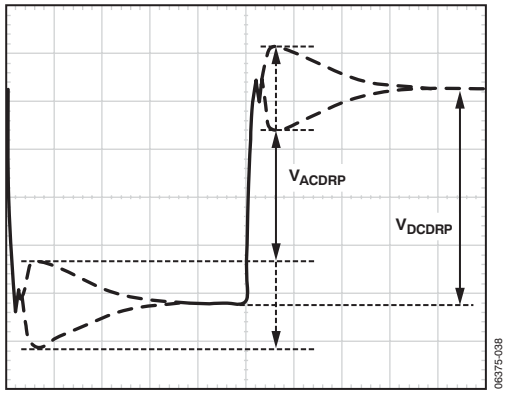


Figure 38. AC Load Line Waveform

6. If the difference between V_{ACDRP} and V_{DCDRP} is more than a couple of millivolts, use Equation 42 to adjust C_{CS}. It may

be necessary to try several parallel values to obtain an adequate one because there are limited standard capacitor values available (it is a good idea to have locations for two capacitors in the layout for this reason).

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad (42)$$

7. Repeat Steps 5 and 6 until no adjustment of C_{CS} is needed. Once this is achieved, do not change C_{CS} for the rest of the procedure.
8. Set the dynamic load step to its maximum step size (but do not use a step size that is larger than needed) and verify that the output waveform is square, meaning V_{ACDRP} and V_{DCDRP} are equal.
9. Ensure that the load step slew rate and the power-up slew rate are set to ~150 A/µs to 250 A/µs (for example, a load step of 50 A should take 200 ns to 300 ns) with no overshoot. Some dynamic loads have an excessive overshoot at power-up if a minimum current is incorrectly set (this is an issue if a VTT tool is in use).

Set the Initial Transient

1. With the dynamic load set at its maximum step size, expand the scope time scale to 2 µs/div to 5 µs/div. This results in a waveform that may have two overshoots and one minor undershoot before achieving the final desired value after V_{DROOP} (see Figure 39).

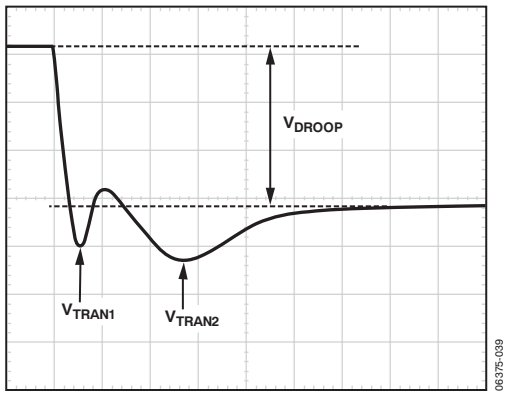


Figure 39. Transient Setting Waveform, Load Step

2. If both overshoots are larger than desired, try the following adjustments in the order shown.
   a. Increase the resistance of the ramp resistor (R_{RAMP}) by 25%.
   b. For V_{TRAN1}, increase C_B or increase the switching frequency.
   c. For V_{TRAN2}, increase R_A by 25% and decrease C_A by 25%.

   If these adjustments do not change the response, it is because the system is limited by the output decoupling. Check the output response and the switching nodes each time a change is made to ensure that the output decoupling is stable.
3. For load release (see Figure 40), if $V_{TRANREL}$ is larger than the value specified by IMVP-6+, a greater percentage of output capacitance is needed. Either increase the capacitance directly or decrease the inductor values. (If inductors are changed, however, it will be necessary to redesign the circuit using the information from the spreadsheet and to repeat all tuning guide procedures).

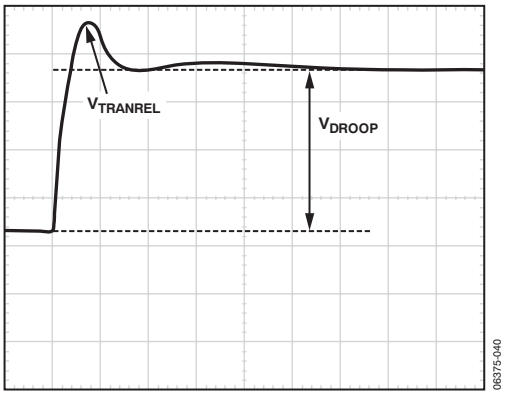


Figure 40. Transient Setting Waveform, Load Release

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a resistance of ~0.53 mΩ at room temperature.
2. When high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the output voltage sense lines of the ADP3209) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of increasing signal ground noise.
4. An analog ground plane should be used around and under the ADP3209 for referencing the components associated with the controller. This plane should be tied to the nearest ground of the output decoupling capacitor, but should not be tied to any other power circuitry to prevent power currents from flowing into the plane.

5. The components around the ADP3209 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are those to the FB and CSFB pins. Refer to Figure 35 for more details on the layout for the CSFB node.
6. The output capacitors should be connected as close as possible to the load (or connector) that receives the power (for example, a microprocessor core). If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
7. Avoid crossing signal lines over the switching power path loop, as described in the Power Circuitry section.

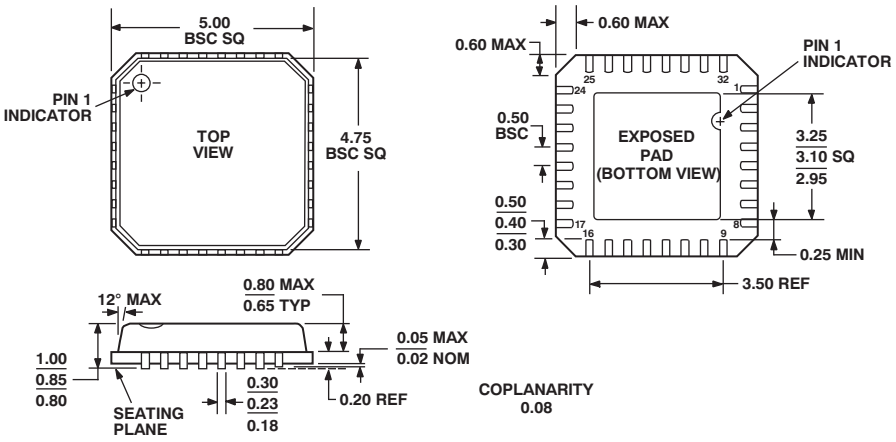
Power Circuitry

1. The switching power path on the PCB should be routed to encompass the shortest possible length to minimize radiated switching noise energy (that is, EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power-converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. The use of short, wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.
2. When a power-dissipating component (for example, a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer heat to the surrounding air. To achieve optimal thermal dissipation, mirror the pad configurations used to heat sink the MOSFETs on the opposite side of the PCB. In addition, improvements in thermal performance can be obtained using the largest possible pad area.
3. The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.
4. For best EMI containment, a solid power ground plane should be used as one of the inner layers and extended under all power components.

Signal Circuitry

1. The output voltage is sensed and regulated between the FB and FBRTN pins, and the traces of these pins should be connected to the signal ground of the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be as small as possible. Therefore, the FB and FBRTN traces should be routed adjacent to each other, atop the power ground plane, and back to the controller.
2. The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be Kelvin connected to the center point of the copper bar, which is the V_{CCGFX} common node for the inductor.
3. On the back of the ADP3209 package, there is a metal pad that can be used to heat sink the device. Therefore, running vias under the ADP3209 is not recommended because the metal pad may cause shorting between vias.

OUTLINE DIMENSION



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 41. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADP3209JCPZ-RL[1]	0°C to 100°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2	5,000

[1] Z = RoHS Compliant Part.

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