THE DATASHEET OF

LM4510SD/NOPB

LM4510 Synchronous Step-Up DC/DC Converter with True Shutdown Isolation

1 Features

- 18 V@ 80 mA from 3.2 V Input
- 5 V @ 280 mA from 3.2 V Input
- No External Schottky Diode Required
- 85% Peak Efficiency
- Soft Start
- True Shutdown Isolation
- Stable with Small Ceramic or Tantalum Output Capacitors
- Output Short-Circuit Protection
- Feedback Fault Protection
- Input Undervoltage Lock Out
- Thermal Shutdown
- 0.002-µA Shutdown Current
- Wide Input Voltage Range: 2.7 V to 5.5 V
- 1-MHz Fixed Frequency Operation
- Low-profile 10-pin WSON Package (3 mm x 3 mm x 0.8 mm)

2 Applications

- Organic LED Panel Power Supply
- Charging Holster
- White LED Backlight
- USB Power Supply
- Class D Audio Amplifier
- Camera Flash LED Driver

3 Description

The LM4510 is a current mode step-up DC/DC converter with a 1.2-A internal NMOS switch designed to deliver up to 120 mA at 16 V from a Li-Ion battery.

The device's synchronous switching operation (no external Schottky diode) at heavy-load, and non-synchronous switching operation at light-load, maximizes power efficiency.

True shutdown function by synchronous FET and related circuitry ensures input and output isolation.

A programmable soft-start circuit allows the user to limit the amount of inrush current during start-up. The output voltage can be adjusted by external resistors.

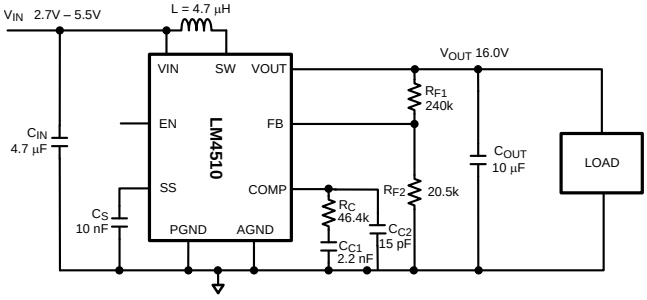
The LM4510 features advanced short-circuit protection to maximize safety during output to ground short condition. During shutdown the feedback resistors and the load are disconnected from the input to prevent leakage current paths to ground.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM4510	WSON (10)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



Efficiency at V_{OUT} = 16 V

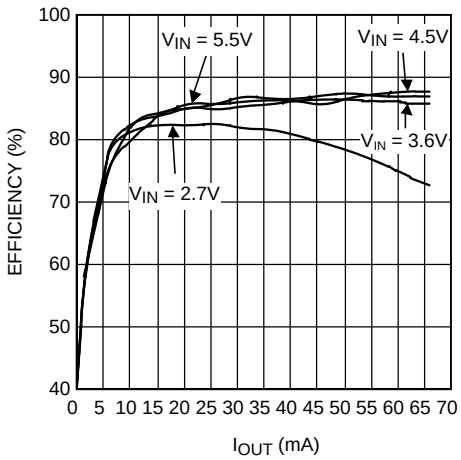


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D **Page**

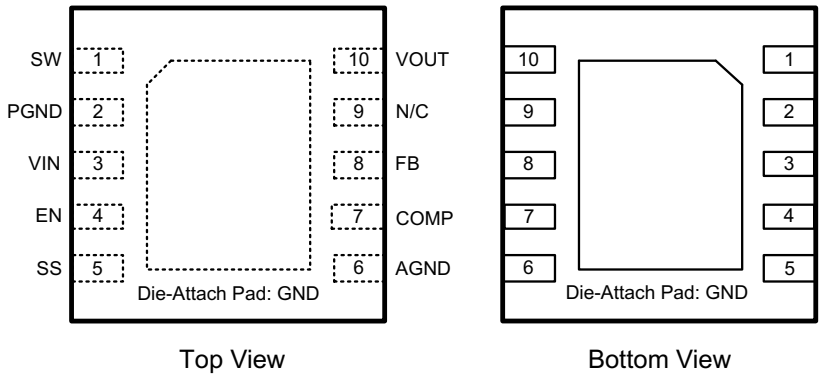
- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section ... 1

Changes from Revision B (May 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configuration and Functions

WSON Package (DSC)
10 Pins



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SW	A	Switch pin. Drain connections of both internal NMOS and PMOS devices.
2	PGND	G	Power ground
3	VIN	P	Analog and Power supply input. Input range: 2.7 V to 5.5 V.
4	EN	I	Enable logic input. HIGH= Enabled, LOW=Shutdown.
5	SS	A	Soft-start pin
6	AGND	G	Analog ground
7	COMP	A	Compensation network connection.
8	FB	A	Output voltage feedback connection.
9	N/C		No internal connection.
10	VOUT	A	Internal PMOS source connection for synchronous rectification.
DAP	DAP		Die Attach Pad thermal connection

6 Specifications

6.1 Absolute Maximum Ratings[1][2][3]

	MIN	MAX	UNIT
VIN	−0.3	6.5	V
VOUT	−0.3	21	V
SW[4]	–0.3	V_{OUT}+0.3	V
EN, SS, COMP FB	−0.3	6.5	V
PGND to AGND	−0.2	0.2	V
Continuous power dissipation[5]		Internally Limited	
Junction temperature (T_{J-MAX})	150	150	°C
Lead temperature (soldering, 10 sec)[6]		260	°C

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions for which the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics*.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) This condition applies if $V_{IN} < V_{OUT}$. If $V_{IN} > V_{OUT}$, a voltage greater than V_{IN} + 0.3 V should not be applied to the VOUT or SW pins. The absolute maximum specification applies to DC voltage. An extended negative voltage limit of –1 V applies for a pulse of up to 1 µs, and –2 V for a pulse of up to 40 ns. An extended positive voltage limit of 22 V applies for a pulse of up to 20 ns.
(5) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 150°C (Typ.) and disengages at T_J= 140°C (Typ.).
(6) For detailed soldering information and specifications, please refer to Application Note 1187: *Leadless Leadframe Package (LLP)* (SNOI401).

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]		2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]		1000	V
		Machine model		200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage (V_{IN})	2.7	5.5	V
Junction temperature (T_J)[1]	−40	125	°C
Output voltage (V_{OUT})		18	V

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$

6.4 Thermal Information

THERMAL METRIC[1]		LM4510 DSC 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	22	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	22.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise stated the following conditions apply: VIN = 3.6 V, EN = 3.6 V, T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
V_{FB}	FB Pin Voltage	2.7 V ≤ V_{IN} ≤ 5.5 V		1.265		V
		2.7 V ≤ V_{IN} ≤ 5.5 V, −40°C ≤ T_J ≤ 125°C	1.24		1.29	
I_{FB}	FB Pin Bias Current[3]	−40°C ≤ T_J ≤ 125°C		0.050	1.5	µA
$R_{DS(on)}$	NMOS Switch $R_{DS(on)}$	I_{SW} = 0.3 A		0.45	1.1	Ω
	PMOS Switch $R_{DS(on)}$	I_{SW} = 0.3 A, V_{OUT} = 10 V		0.9	1.1	
I_{CL}	NMOS Switch Current Limit		1	1.2	1.8	A
I_Q	Device Switching	EN = 3.6 V, FB = COMP		1.7		mA
		EN = 3.6 V, FB = COMP, −40°C ≤ T_J ≤ 125°C			2.5	
	Non-switching Current	EN = 3.6 V, FB > 1.29 V		0.8		
		EN = 3.6 V, FB > 1.29 V, −40°C ≤ T_J ≤ 125°C			2	
	Shutdown Current	EN = 0 V		0.002	0.050	µA
I_L	SW Leakage Current[3]	SW = 20 V		0.01	0.150	µA
I_{VOUT}	VOUT Bias Current[3]	V_{OUT} = 20 V		90		µA
		V_{OUT} = 20 V, −40°C ≤ T_J ≤ 125°C	50		150	
I_{VL}	PMOS Switch Leakage Current	SW = 0 V, V_{OUT} = 20 V		0.001	0.100	µA
f_{SW}	Switching Frequency			1		MHz
		−40°C ≤ T_J ≤ 125°C	0.85		1.2	
D_{MAX}	Maximum Duty Cycle	FB = 0 V		94%		
		FB = 0 V, −40°C ≤ T_J ≤ 125°C	88%			
D_{MIN}	Minimum Duty Cycle			15%	20%	
Gm	Error Amplifier Transconductance			130		µmho
		−40°C ≤ T_J ≤ 125°C	70		200	
EN Threshold	Device Enable	HIGH		0.81		V
		HIGH, −40°C ≤ T_J ≤ 125°C	1.2			
	Device Shutdown	LOW		0.78		
		LOW, −40°C ≤ T_J ≤ 125°C			0.4	

(1) All room temperature limits are production tested, specified through statistical analysis or by design. All limits at −40°C ≤ T_J ≤ 125°C are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) Current flows into the pin.

Electrical Characteristics (continued)

Unless otherwise stated the following conditions apply: VIN = 3.6 V, EN = 3.6 V, T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
I_{EN}	EN Pin Bias Current	0 < EN < 3.6 V		3.2		µA
		0 < EN < 3.6 V, −40°C ≤ T_J ≤ 125°C			8	
FB Fault Protection	Feedback Fault Protection	ON Threshold		19.7		V
		ON Threshold, −40°C ≤ T_J ≤ 125°C	18		20.7	
		OFF Threshold		18.7		
		OFF Threshold, −40°C ≤ T_J ≤ 125°C	17		20	
UVLO	Input Undervoltage Lockout	ON Threshold		2.5		V
		ON Threshold, −40°C ≤ T_J ≤ 125°C			2.65	
		OFF Threshold		2.35		
		OFF Threshold, −40°C ≤ T_J ≤ 125°C	2.1			
I_{SS}	Soft-Start Pin Current(4)			11.3		µA
		−40°C ≤ T_J ≤ 125°C	9		15	

(4) Current flows out of the pin.

6.6 Typical Characteristics

LM4510SD, Circuit of Figure 18, (L = 4.7 µH, COILCRAFT, DO3316-472ML; C_{IN} = 4 .7 µF, TDK, C2012X5R0J475K; C_{OUT} = 10 µF, AVX, 12103D106KAT2A; C_S = 10 nF, TDK, C1608C0G1E103J; C_{C1} = 2.2 nF, Taiyo Yuden, TMK107SD222JA-T; R_C = 46.4 kΩ, Yageo, 9t06031A4642FBHFT), V_{IN} = 3.6 V, V_{OUT} = 16 V, T_A = 25°C, unless otherwise noted.

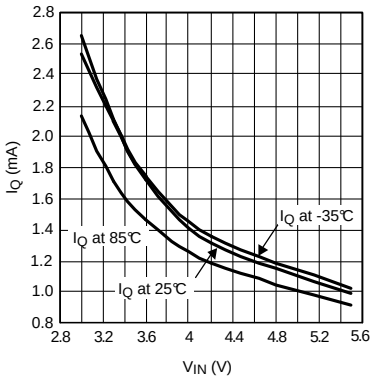


Figure 1. Switching Quiescent Current vs V_{IN}

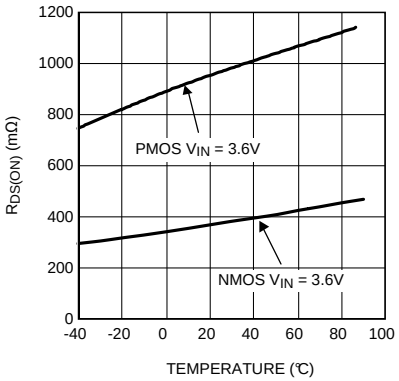


Figure 2. $R_{DS(on)}$ vs Temperature at V_{IN}= 3.6 V

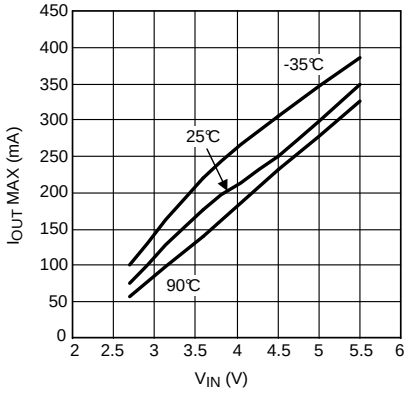


Figure 3. Load Capability vs V_{IN} (V_{OUT} = 16 V)

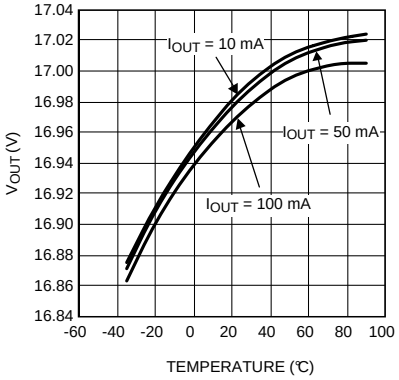


Figure 4. Output Voltage vs Temperature (V_{OUT} = 17 V)

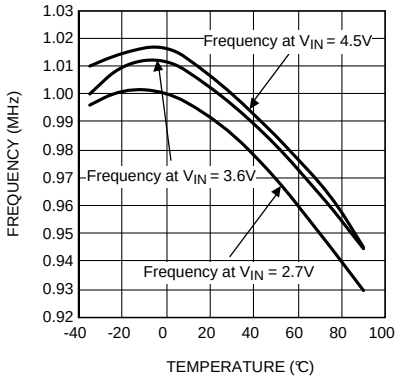


Figure 5. Switching Frequency vs Temperature

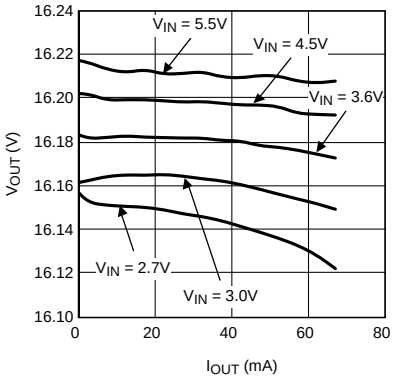


Figure 6. Load Regulation (V_{OUT} = 16 V)

Typical Characteristics (continued)

LM4510SD, Circuit of Figure 18, (L = 4.7 µH, COILCRAFT, DO3316-472ML; C_{IN} = 4 .7 µF, TDK, C2012X5R0J475K; C_{OUT} = 10 µF, AVX, 12103D106KAT2A; C_S = 10 nF, TDK, C1608C0G1E103J; C_{C1} = 2.2 nF, Taiyo Yuden, TMK107SD222JA-T; R_C = 46.4 kΩ, Yageo, 9t06031A4642FBHFT), V_{IN} = 3.6 V, V_{OUT} = 16 V, T_A = 25°C, unless otherwise noted.

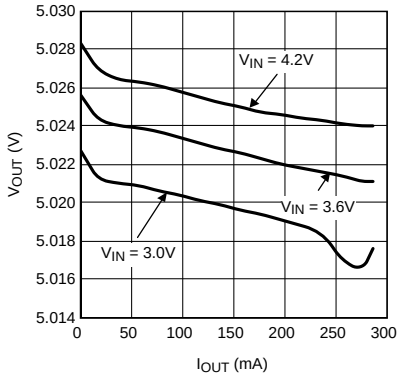


Figure 7. Load Regulation (V_{OUT} = 5 V)

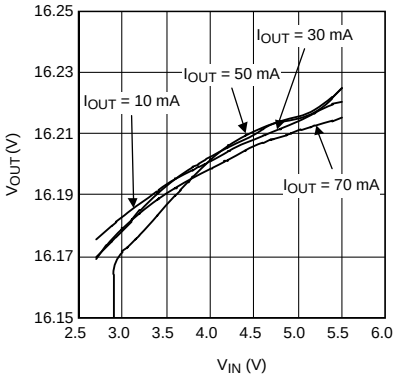


Figure 8. Line Regulation (V_{OUT} = 16 V)

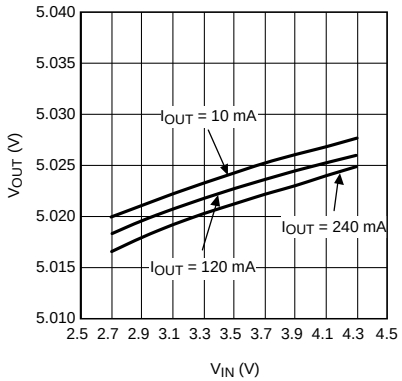


Figure 9. Line Regulation (V_{OUT} = 5 V)

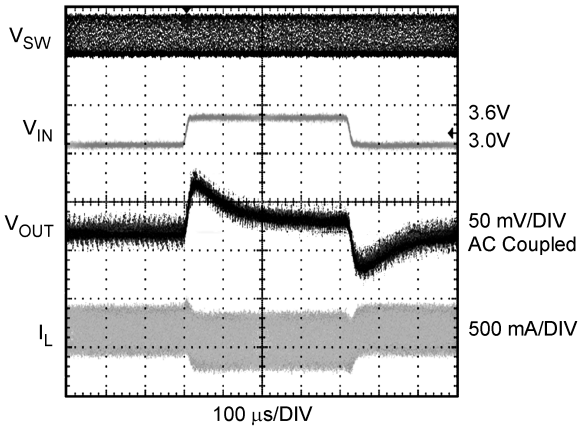


Figure 10. Line Transient Response (V_{OUT} = 16 V)

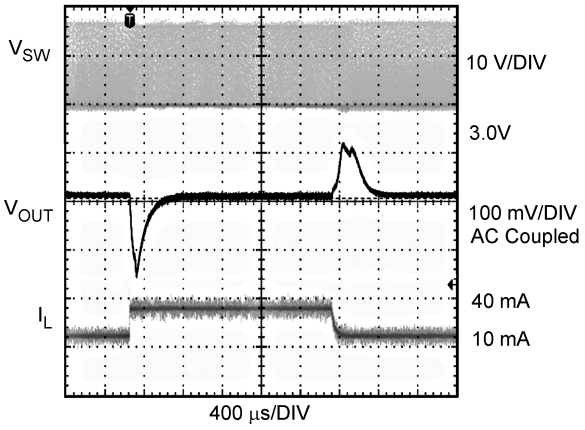


Figure 11. Load Transient Response (V_{OUT} = 16 V)

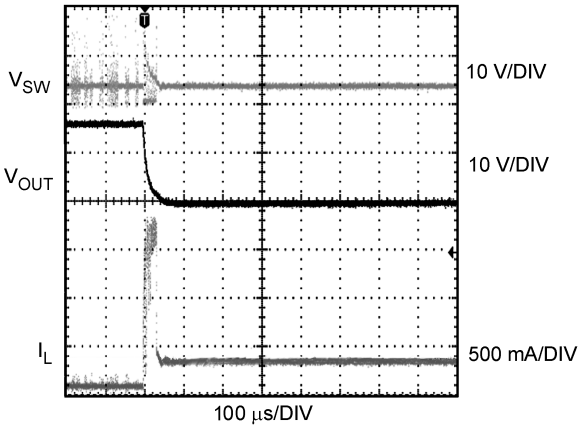


Figure 12. Short Circuit Response (V_{OUT} = 16 V)

Typical Characteristics (continued)

LM4510SD, Circuit of Figure 18, (L = 4.7 µH, COILCRAFT, DO3316-472ML; C_{IN} = 4 .7 µF, TDK, C2012X5R0J475K; C_{OUT} = 10 µF, AVX, 12103D106KAT2A; C_S = 10 nF, TDK, C1608C0G1E103J; C_{C1} = 2.2 nF, Taiyo Yuden, TMK107SD222JA-T; R_C = 46.4 kΩ, Yageo, 9t06031A4642FBHFT), V_{IN} = 3.6 V, V_{OUT} = 16 V, T_A = 25°C, unless otherwise noted.

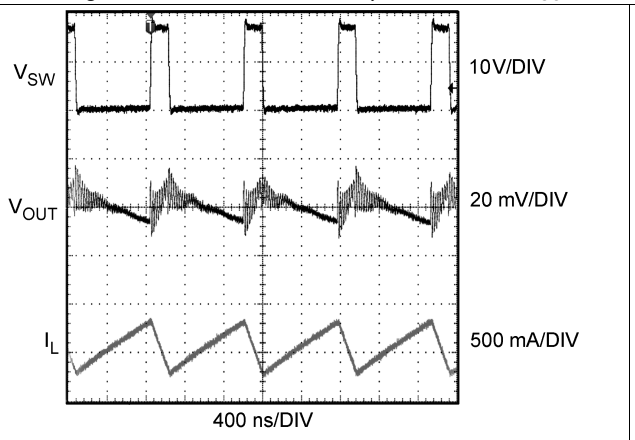


Figure 13. Output Voltage Ripple (V_{OUT} = 16 V, I_{OUT} = 90 mA)

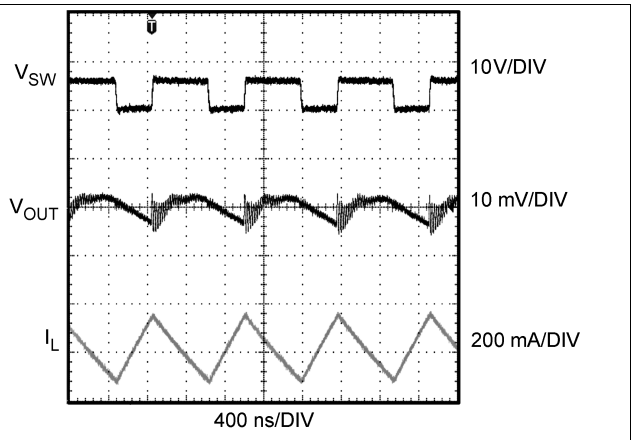


Figure 14. Output Voltage Ripple (V_{OUT} = 5 V, I_{OUT} = 100 mA)

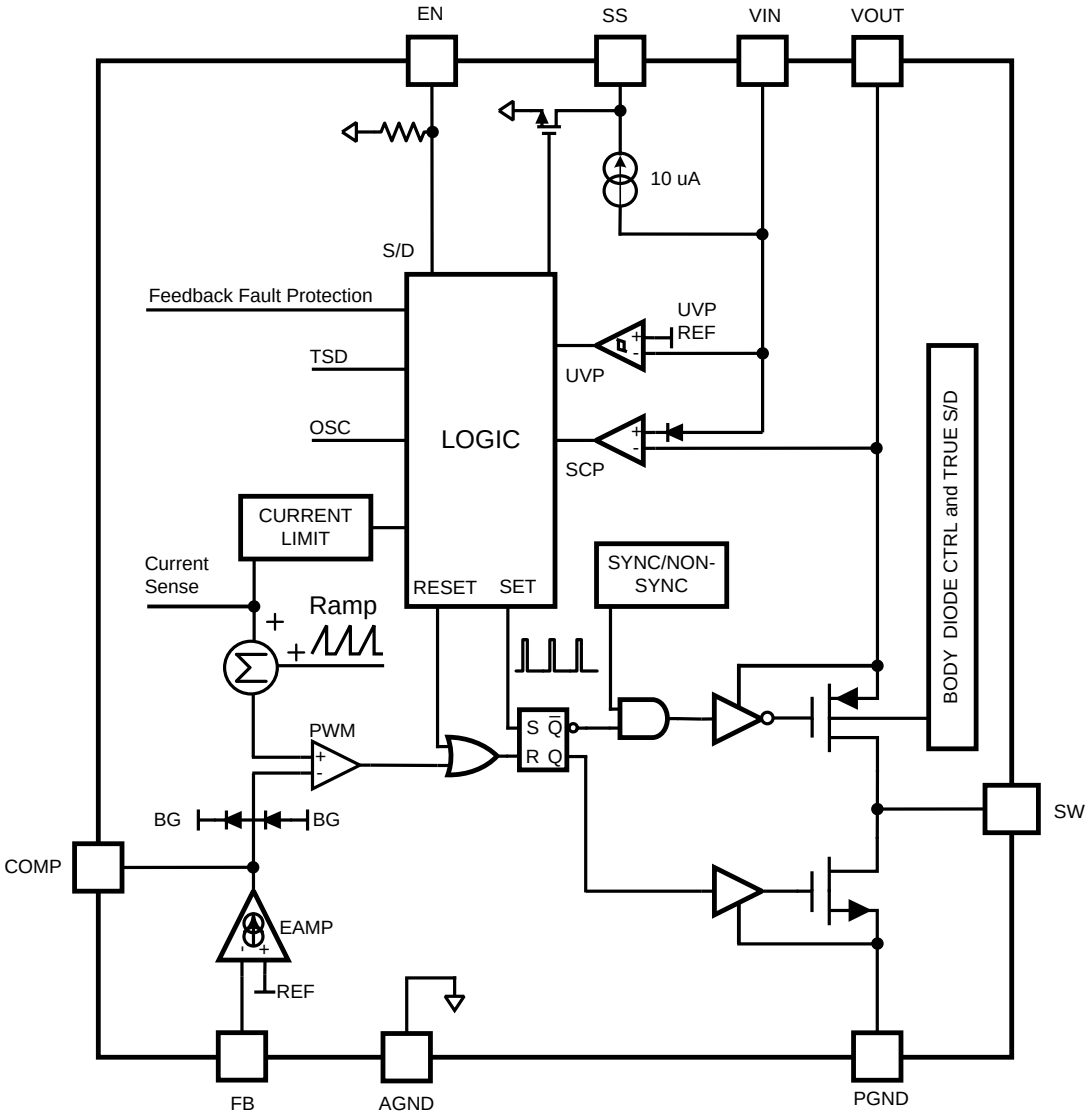
7 Detailed Description

7.1 Overview

LM4510 is a peak current-mode, fixed-frequency PWM boost regulator that employs both Synchronous and Non-Synchronous Switching.

The DC/DC regulator regulates the feedback output voltage providing excellent line and load transient response. The operation of the LM4510 can best be understood by referring to the Block Diagram.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Short Circuit Protection

When V_{OUT} goes down to V_{IN}–0.7V (typ.), the device stops switching due to the short-circuit protection circuitry and the short-circuit output current is limited to I_{INIT_CHARGE}.

Feature Description (continued)

7.3.2 Feedback Fault Protection

The LM4510 features unique Feedback Fault Protection to maximize safety when the feedback resistor is not properly connected to a circuit or the feedback node is shorted directly to ground.

Feedback fault triggers V_{OUT} monitoring. During monitoring, if V_{OUT} reaches a protection level, the device shuts down. When the feedback network is reconnected and V_{OUT} is lower than the OFF threshold level of Feedback Fault Protection, V_{OUT} monitoring stops. V_{OUT} is then regulated by the control loop.

7.3.3 Input Undervoltage Lock-Out

The LM4510 has dedicated circuitry to protect the IC and the external components when the battery voltage is lower than the preset threshold. This undervoltage lock-out with hysteresis prevents malfunctions during start-up or abnormal power off.

7.3.4 Thermal Shutdown

If the die temperature exceeds 150°C (typ.), the thermal protection circuitry shuts down the device. The switches remain off until the die temperature is reduced to approximately 140°C (typ.).

7.4 Device Functional Modes

7.4.1 Non-Synchronous Operation

The device operates in Non-synchronous Mode at light load (I_{OUT} < 10 mA) or when output voltage is lower than 10 V (typ.). At light load, LM4510 automatically changes its switching operation from 'Synchronous' to 'Non-Synchronous' depending on V_{IN} and L. Non-Synchronous operation at light load maximizes power efficiency by reducing PMOS driving loss.

7.4.2 Operation in Synchronous Continuous Conduction Mode (Cycle 1, Cycle 2)

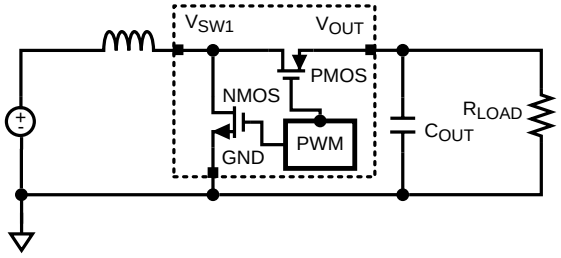


Figure 15. Schematic of Synchronous Boost Converter

Synchronous boost converter is shown in Figure 15. At the start of each cycle, the oscillator sets the driver logic and turns on the NMOS power device and turns off the PMOS power device.

7.4.2.1 Cycle 1 Description

Refer to Figure 16. NMOS switch turn-on → Inductor current increases and flows to GND.

PMOS switch turn-off → Isolate VOUT from SW → Output capacitor supplies load current.

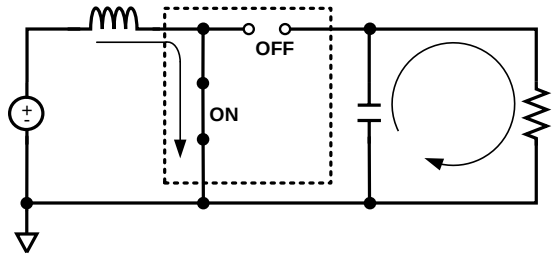


Figure 16. Equivalent Circuit During Cycle 1

Device Functional Modes (continued)

During operation, EAMP output voltage (V_{COMP}) increases for larger loads and decreases for smaller loads. When the sum of the ramp compensation and the sensed NMOS current reaches a level determined by the EAMP output voltage, the PWM COMP resets the logic, turning off the NMOS power device and turning on the PMOS power device.

7.4.2.2 Cycle 2 Description

Refer to Figure 17. NMOS Switch turn-off → PMOS Switch turn-on→ Inductor current decreases and flows through PMOS → Inductor current recharges output capacitor and supplies load current.

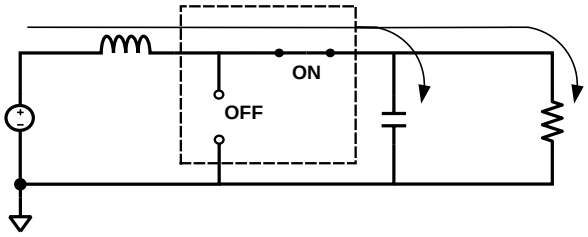


Figure 17. Equivalent Circuit During Cycle 2

After the switching period the oscillator then sets the driver logic again repeating the process.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM4510 shuts down when the EN pin is low. In this mode the feedback resistors and the load are disconnected from the input in order to avoid leakage current flow and to allow the output voltage to drop to 0 V.

The LM4510 turns on when EN is high. There is an internal pull-down resistor on the EN pin so the device is in a normally off state.

8.2 Typical Applications

8.2.1 2.7 V to 5.5 V Input with a 16 V Output

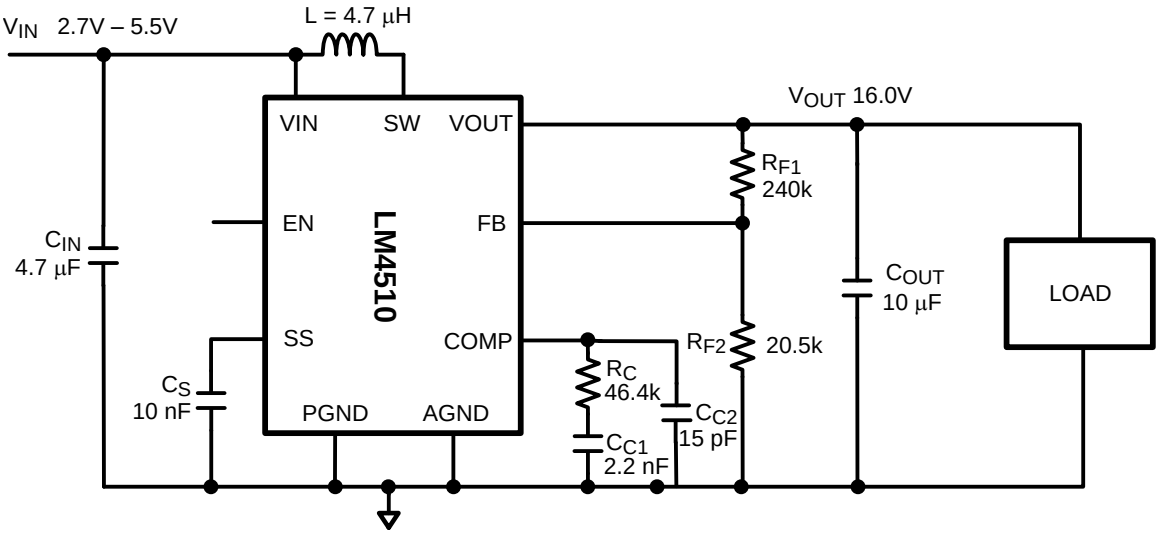


Figure 18. Typical Application Circuit for Normal DC/DC

8.2.1.1 Design Requirements

The LM4510 is designed to operate up to 75 mA at 2.7 V input and 350 mA at 5.5 V input to output 16 V. In any case, it is recommended to avoid starting up the device at minimum input voltage and maximum load. Special attention must be taken to avoid operating near thermal shutdown condition. A simple calculation can be used to determine the power dissipation at the operating condition. $P_{D\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - T_{A\text{-}MAX})/R_{\theta JA}(T_{J\text{-}MAX\text{-}OP} = 125°C)$.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Adjusting Output Voltage

The output voltage is set using the feedback pin and a resistor voltage divider (R_{F1}, R_{F2}) connected to the output as shown in Figure 18.

The ratio of the feedback resistors sets the output voltage.

R_{F2} Selection First of all choose a value for R_{F2} generally between 10 kΩ and 25 kΩ.

R_{F1} Selection Calculate R_{F1} using Equation 1:

Typical Applications (continued)

$$R_{F1} = \left(\frac{V_O}{V_{FB}} - 1\right) \times R_{F2} [\Omega] \quad (1)$$

Table 1 gives suggested component values for several typical output voltages.

Table 1. Suggested Component Values for Different Output Voltages

OUTPUT VOLTAGE (V)	R_{F2} (kΩ)	R_{F1} (kΩ)	R_C (kΩ)	C_{C1} (nF)
16	20.5	240	46.4	2.2
12	20.5	174	46.4	2.2
5	20.5	60.4	46.4	2.2
3.3	20.5	33	46.4	2.2

8.2.1.2.2 Maximum Output Current

When the output voltage is set at different level, it is important to know the maximum load capability. By first order estimation, $I_{OUT(MAX)}$ can be estimated by Equation 2:

$$I_{OUT\_Max} = \frac{1.32 \times V_{IN} - 2.79}{V_{OUT}} [A] \quad (2)$$

8.2.1.2.3 Inductor Selection

The larger value inductor makes lower peak inductor current and reduces stress on internal power NMOS.

On the other hand, the smaller value inductor has smaller outline, lower DCR and a higher current capacity. Generally a 4.7-µH to 15-µH inductor is recommended.

8.2.1.2.4 I_{L_AVE} Check

The average inductor current is given by Equation 3:

$$I_{L\_AVE} = \frac{I_{OUT}}{\eta \times D'} [A], D' = \frac{V_{IN}}{V_{OUT}} \quad (3)$$

Where I_{OUT} is output current, η is the converter efficiency of the total driven load and D' is the off duty cycle of the switching regulator.

Inductor DC current rating (40°C temperature rise) should be more than the average inductor current at worst case.

ΔI Define

The inductor ripple current is given by Equation 4:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} [A], D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (4)$$

Where D is the on-duty cycle of the switching regulator. A common choice is to set ΔI_L to about 30% of I_{L_AVE}.

$I_{L\_PK} \leq I_{CL}$ Check & I_{MIN} Define

The peak inductor current is given by Equation 5:

$$I_{L\_pk} = I_{L\_AVE} + \frac{\Delta I_L}{2} [A]$$

$$I_{L\_pk} = \frac{I_{OUT}}{\eta \times D'} + \frac{V_{IN} \times D}{2L \times f_{SW}} [A] \quad (5)$$

To prevent loss of regulation, ensure that the NMOS power switch current limit is greater than the worst-case peak inductor current in the target application.

Also make sure that the inductor saturation current is greater than the peak inductor current under the worst-case load transient, high ambient temperature and start-up conditions. Refer to Table 2 for suggested inductors.

Table 2. Suggested Inductors and Their Suppliers

MODEL	VENDOR	DIMENSIONS LxWxH (mm)	D.C.R (max)
DO3314-472ML	COILCRAFT	3.3mm x 3.3mm x 1.4mm	320 mΩ
DO3316P-472ML	COILCRAFT	12.95mm x 9.4mm x 5.4mm	18 mΩ

8.2.1.2.5 Input Capacitor Selection

Due to the presence of an inductor, the input current waveform is continuous and triangular. So the input capacitor is less critical than output capacitor in boost applications. Typically, a 4.7-µF to 10-µF ceramic input capacitor is recommended on the VIN pin of the IC.

I_{CIN_RMS} Check

The RMS current in the input capacitor is given by Equation 6:

$$I_{CIN\_RMS} = \frac{\Delta I_L}{\sqrt{12}} [A] \quad (6)$$

The input capacitor should be capable of handling the RMS current.

8.2.1.2.6 Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the switch is closed and the inductor is charging. As a result, it sees very large ripple currents.

A ceramic capacitor of value 4.7 µF to 10 µF is recommended at the output. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used.

I_{COUT_RMS} Check

The RMS current in the output capacitor is given by Equation 7:

$$I_{COUT\_RMS} = \sqrt{(1 - D)\left[I_{OUT}^2 \frac{D}{(1 - D)^2} + \frac{\Delta I_L^2}{12}\right]} [A] \quad (7)$$

The output capacitor should be capable of handling the RMS current.

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. The output capacitor also affects the soft-start time (See *Soft-Start Function and Soft-Start Capacitor Selection*). Table 3 shows suggested input and output capacitors.

Table 3. Suggested C_{IN} and C_{OUT} Capacitors and Their Suppliers

MODEL	TYPE	VENDOR	VOLTAGE RATING	CASE SIZE INCH (mm)
4.7 µF for C_{IN}				
C2012X5R0J475	Ceramic, X5R	TDK	6.3 V	0805 (2012)
GRM21BR60J475	Ceramic, X5R	muRata	6.3 V	0805 (2012)
JMK212BJ475	Ceramic, X5R	Taiyo-Yuden	6.3 V	0805 (2012)
C2012X5R0J475K	Ceramic, X5R	TDK	6.3 V	0603 (1608)
10 µF for C_{OUT}				
TMK316BJ106KL	Ceramic, X5R	Taiyo-Yuden	25 V	1206 (3216)
12103D106KAT2A	Ceramic, X5R	AVX	25 V	1210 (3225)

8.2.1.2.7 Soft-Start Function and Soft-Start Capacitor Selection

The LM4510 has a soft-start pin that can be used to limit the input inrush current. Connect a capacitor from SS pin to GND to set the soft-start period. Figure 19 describes the soft start process.

- Initial charging period: When the device is turned on, the control circuitry linearly regulating initial charge current charges V_{OUT} by limiting the inrush current.
- Soft-start period: After V_{OUT} reaches V_{IN} –0.7 V (typ.), the device starts switching and the C_S is charged at a constant current of 11 µA, ramping up to V_{IN}. This period ends when V_{SS} reaches V_{FB}. C_S should be large enough to ensure soft-start period ends after C_O is fully charged.

During the initial charging period, the required load current must be smaller than the initial charge current to ensure V_{OUT} reaches V_{IN} –0.7 V (typ.).

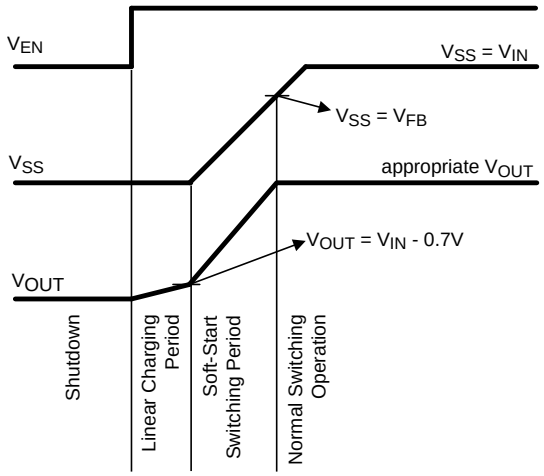


Figure 19. Soft-Start Timing Diagram

C_S Selection

The soft-start time without load can be estimated as:

$$t_{SS} = \frac{C_{OUT} \times (V_{IN} - 0.7)}{I_{INIT\_CHARGE}} + \frac{C_S \times V_{FB}}{I_{SS\_CHARGE}} \text{ [sec]} \quad (8)$$

Where the I_{INIT_CHARGE} is Initial Charging Current depending on V_{IN} and I_{SS_CHARGE} (11 µA (typ.). Also, when selecting the fuse current rating, make sure the value is higher than the initial charging current.

8.2.1.2.8 Compensation Component Selection

The LM4510 provides a compensation pin COMP to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_{C1} be used for the compensation network, as shown in the typical application circuit. In addition, C_{C2} is used for compensating high frequency zeros.

The series combination of R_C and C_{C1} introduces a pole-zero pair according to Equation 9:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_{C1}} \text{ [Hz]}$$

$$f_{ZC} = \frac{1}{2\pi R_C C_{C1}} \text{ [Hz]} \tag{9}$$

In addition, C_{C2} introduces a pole according to Equation 10:

$$f_{PC2} = \frac{1}{2\pi(R_C // R_O)C_{C2}} \text{ [Hz]} \tag{10}$$

Where R_O is the output impedance of the error amplifier, approximately 1 MΩ, and amplifier voltage gain is typically 200 V/V depending on temperature and V_{IN}.

Refer to Table 4 for suggested soft start capacitor and compensation components.

Table 4. Suggested C_S and Compensation Components

MODEL	TYPE	VENDOR	VOLTAGE RATING	CASE SIZE INCH (mm)
(C_S) C1608C0G1E103J	Ceramic, X5R	TDK	6.3 V	603 (1608)
(C_1)TMK107SD222JA-T	Ceramic, X5R	Taiyo Yuden	25 V	603 (1608)
(R_C) 9t06031A4642FBHFT	Resistor	Yageo Corporation	1/10 W	603 (1608)

8.2.1.3 Application Curves

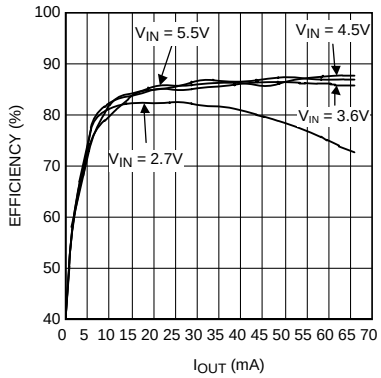


Figure 20. Efficiency vs Output Current (V_{OUT} = 16 V)

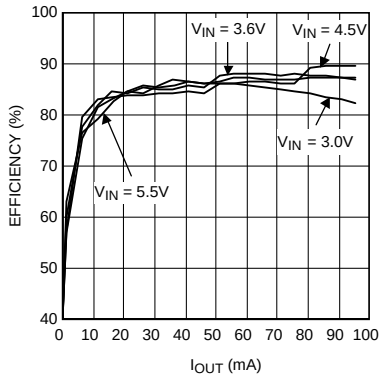


Figure 21. Efficiency vs Output Current (V_{OUT} = 12 V)

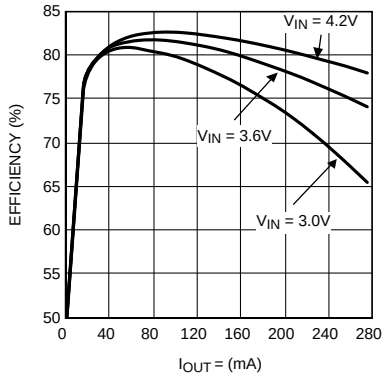


Figure 22. Efficiency vs Output Current (V_{OUT} = 5 V, L= DO3314-472ML)

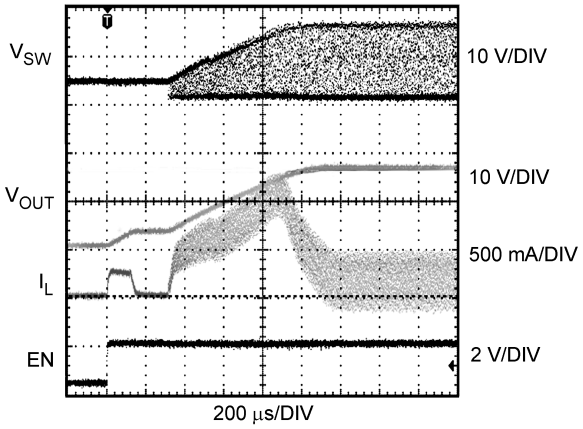


Figure 23. Start Up (V_{OUT} = 16 V, R_{LOAD} = 530 Ω)

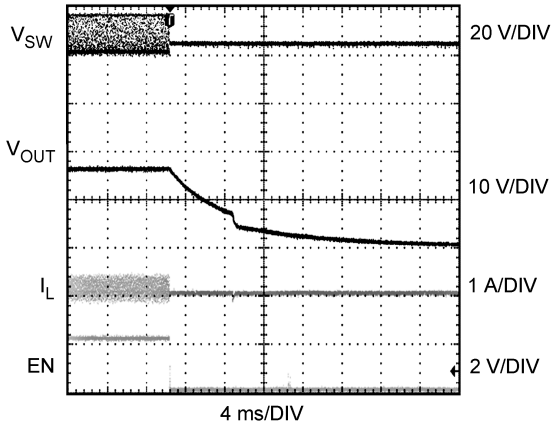


Figure 24. Shut Down (V_{OUT} = 16 V, R_{LOAD} = 940 Ω)

8.2.2 Flash and Torch Application

LM4510 can be configured to drive white LEDs for the flash and torch functions. The flash/torch can be set up with the circuit shown in Figure 25 by using the resistor R_T to determine the current in Torch Mode and R_F to determine the current in Flash Mode. The amount of current can be estimated using Equation 11:

$$I_{Torch} = \frac{V_{FB}}{R_T} [A]$$

$$I_{Flash} = \frac{V_{FB}}{R_T // R_F} [A] \quad (11)$$

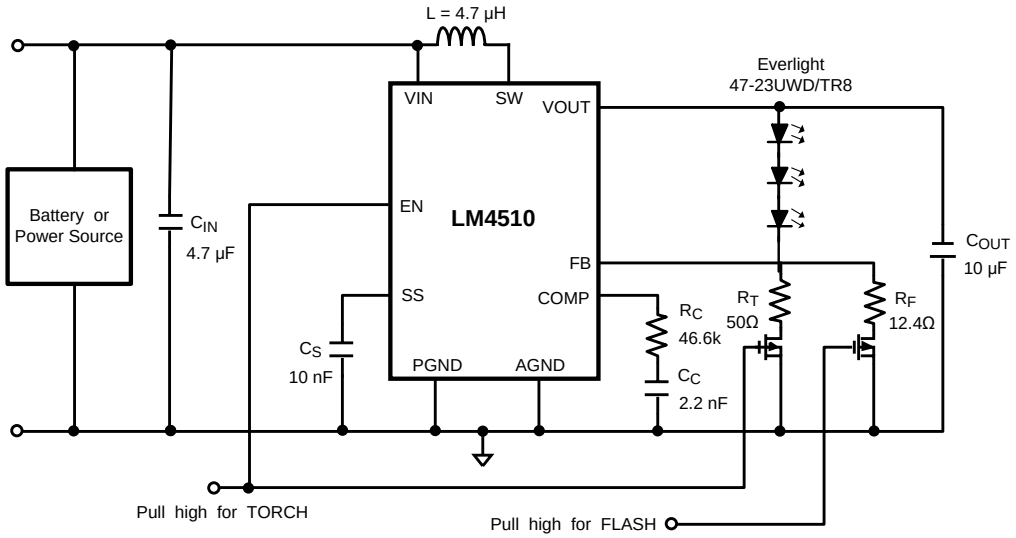


Figure 25. Typical Application Circuit for Flash/Torch

8.2.2.1 Design Requirements

See *Design Requirements*.

8.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure*.

8.2.2.3 Application Curve

See *Application Curves*.

9 Power Supply Recommendations

The power supply for the applications using the LM4510 device should be big enough considering output power and efficiency at given input voltage condition. Minimum current requirement condition is (V_{OUT} * I_{OUT})/(V_{IN} * efficiency) and approximately 20 - 30% higher than this value is recommended

10 Layout

10.1 Layout Guidelines

High frequency switching regulators require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LM4510 device. Refer to Figure 26 as an example. Some additional guidelines to be observed:

1. C_{IN} must be placed close to the device and connected directly from VIN to PGND pins. This reduces copper trace resistance, which affects the input voltage ripple of the device. For additional input voltage filtering, typically a 0.1 uF bypass capacitor can be placed between VIN and AGND. This bypass capacitor should be placed near the device closer than C_{IN}.
2. C_{OUT} must also be placed close to the device and connected directly from VOUT to PGND pins. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly affects output voltage ripple and makes noise during output voltage sensing.
3. All voltage-sensing resistors (R_{F1}, R_{F2}) should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the voltage-sensing resistor should be connected directly to the AGND pin.
4. Trace connections made to the inductor should be minimized to reduce power dissipation, EMI radiation and increase overall efficiency. Also poor trace connection increases the ripple of SW.
5. C_S, C_{C1}, C_{C2}, R_C must be placed close to the device and connected to AGND.
6. The AGND pin should connect directly to the ground. Not connecting the AGND pin directly, as close to the chip as possible, may affect the performance of the LM4510 and limit its current driving capability. AGND and PGND should be separate planes and should be connected at a single point.
7. For better thermal performance, DAP should be connected to ground, but cannot be used as the primary ground connection. The PC board land may be modified to a "dog bone" shape to reduce SON thermal impedance. For detail information, refer to Application Note AN-1187.

10.2 Layout Example

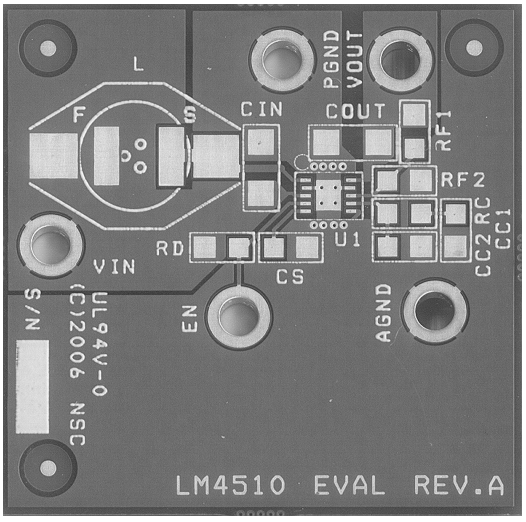


Figure 26. Evaluation Board Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4510SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	L4510	Samples
LM4510SDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	L4510	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

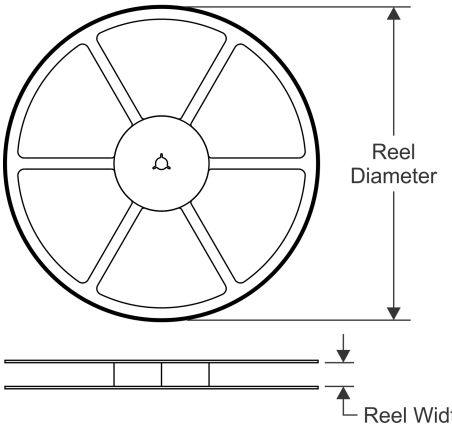
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

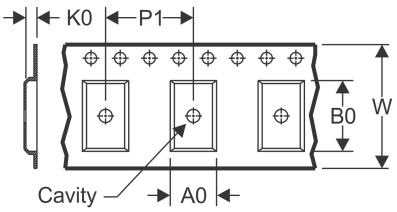
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

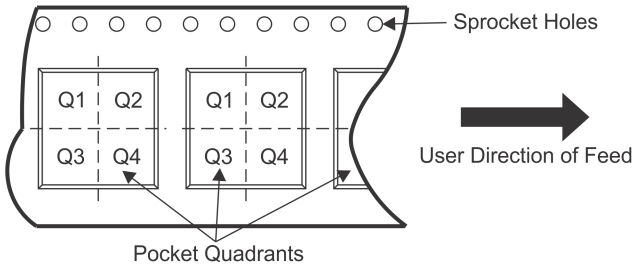


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

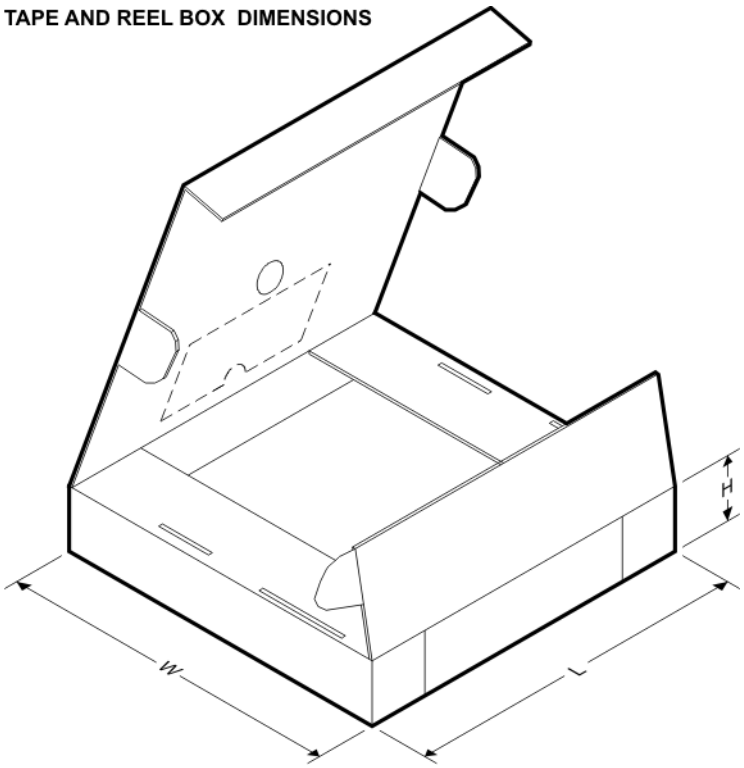
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4510SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM4510SDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

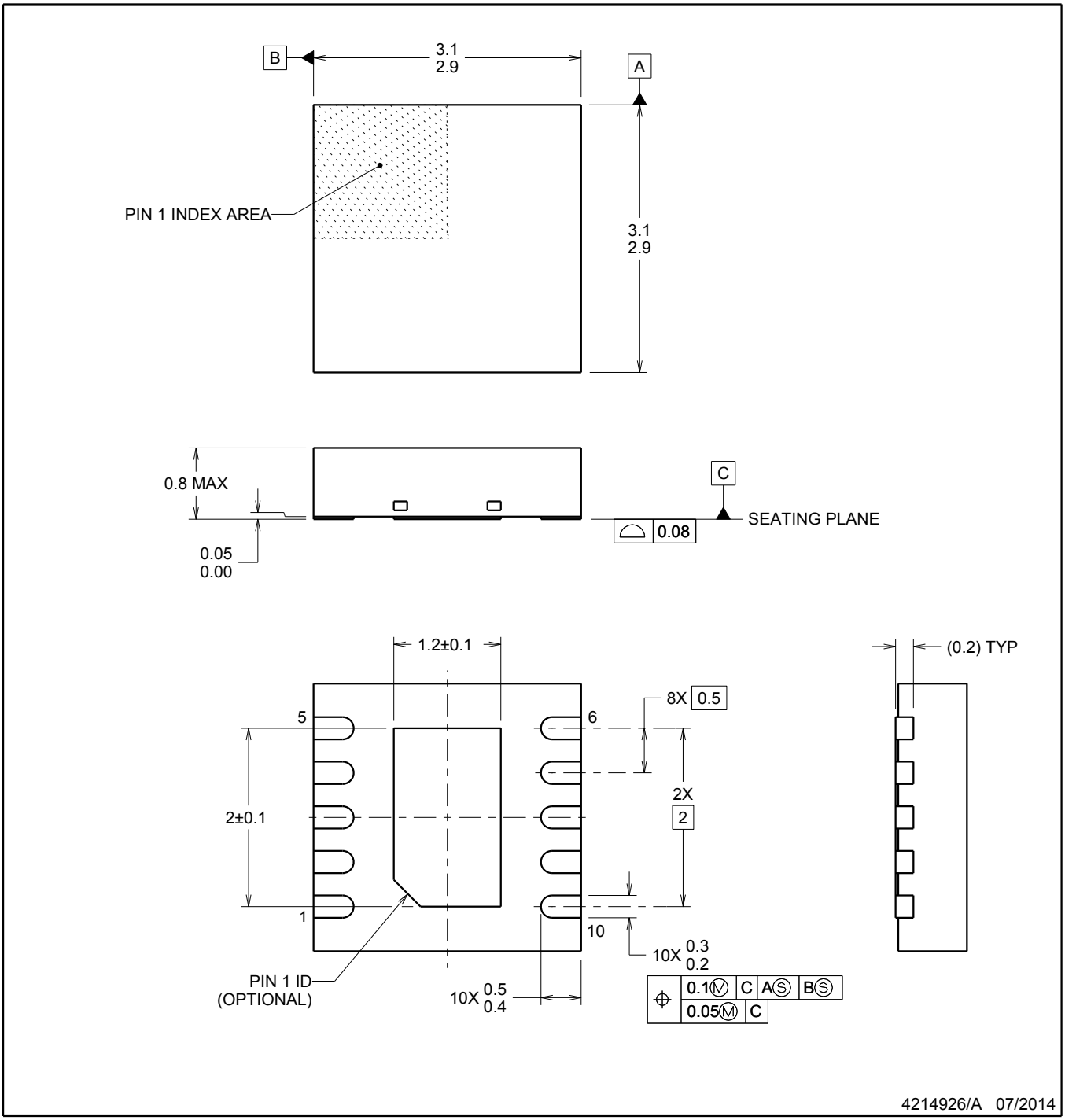
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4510SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM4510SDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DSC0010B

WSON - 0.8 mm max height

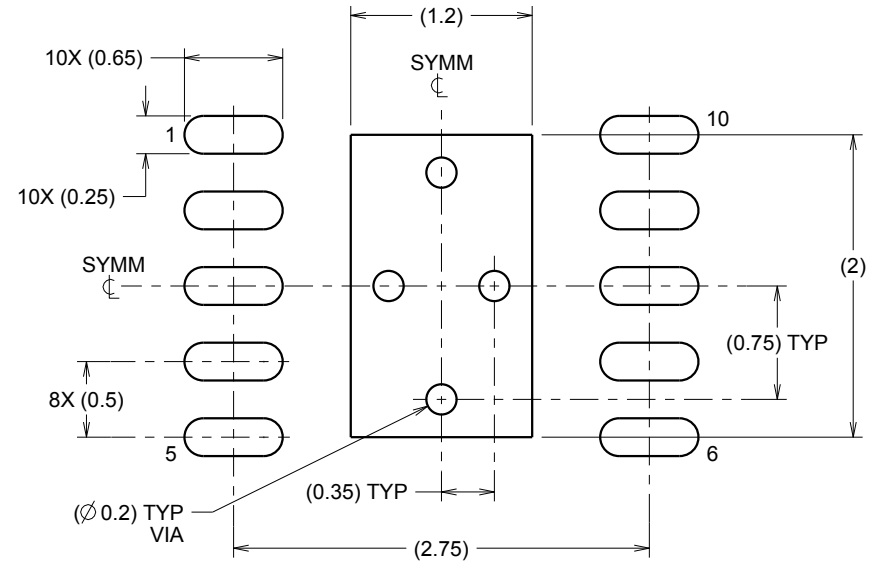
PLASTIC SMALL OUTLINE - NO LEAD



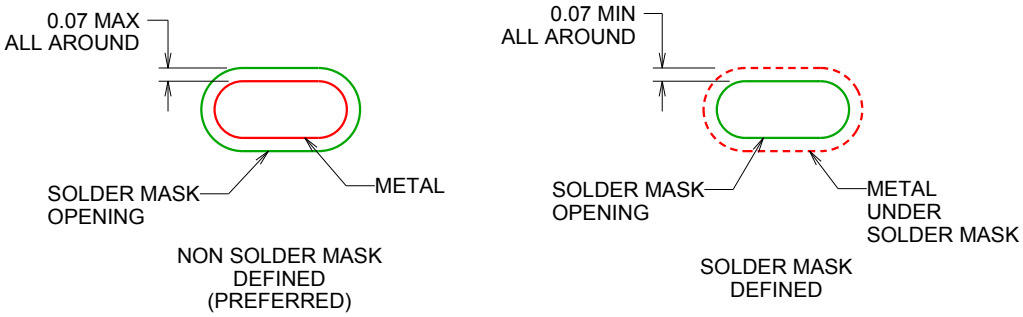
4214926/A 07/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4214926/A 07/2014

NOTES: (continued)

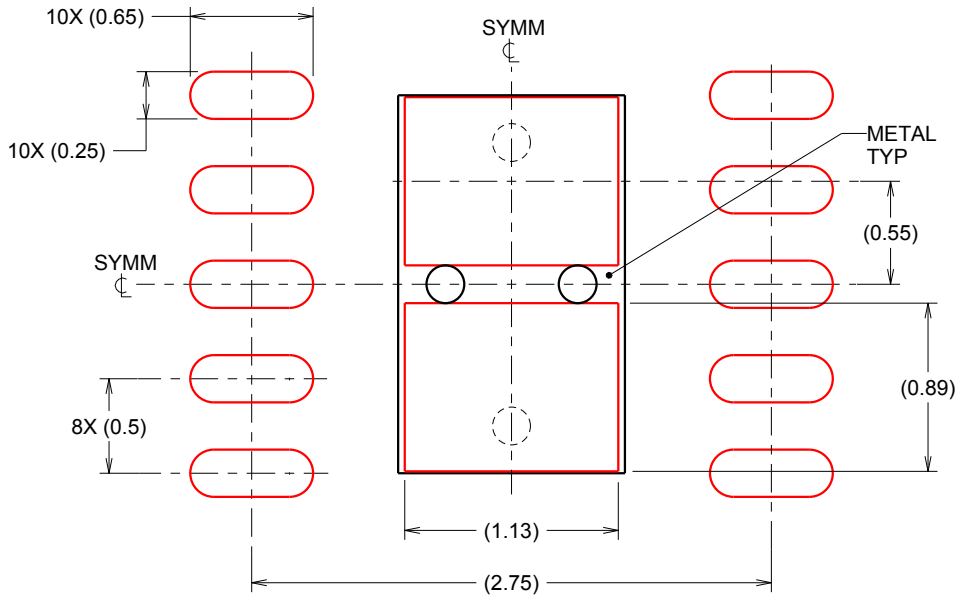
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSC0010B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4214926/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LM4510SD/NOPB on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management