THE DATASHEET OF

UCC28950PW

www.win-source.net 0086-755-83957316

UCC28950 Green Phase-Shifted Full-Bridge Controller With Synchronous Rectification

1 Features

- Enhanced Wide Range Resonant Zero Voltage Switching (ZVS) Capability
- Direct Synchronous Rectifier (SR) Control
- Light-Load Efficiency Management Including
  - Burst Mode Operation
  - Discontinuous Conduction Mode (DCM), Dynamic SR On and Off Control with Programmable Threshold
  - Programmable Adaptive Delay
- Average or Peak Current Mode Control With Programmable Slope Compensation and Voltage Mode Control
- Naturally Handles Pre-Biased Start Up With DCM Mode
- Closed Loop Soft Start and Enable Function
- Programmable Switching Frequency up to 1 MHz with Bi-Directional Synchronization
- (±3%) Cycle-by-Cycle Current Limit Protection With Hiccup Mode Support
- 150-µA Start-Up Current
- V_{DD} Undervoltage Lockout
- Wide Temperature Range –40°C to +125°C

2 Applications

- Phase-Shifted Full-Bridge Converters
- Datacom, Telecom, and Wireless Base-Station Power
- Server, Power Supplies
- Industrial Power Systems
- High-Density Power Architectures
- Solar Inverters, and Electric Vehicles

3 Description

The UCC28950 enhanced phase-shifted controller builds upon Texas Instrument's industry standard UCx895 phase-shifted controller family with enhancements that offer best in class efficiency in today's high performance power systems. The UCC28950 implements advanced control of the full-bridge along with active control of the synchronous rectifier output stage.

The primary-side signals allow programmable delays to ensure ZVS operation over wide-load current and input voltage range, while the load current naturally tunes the secondary-side synchronous rectifiers switching delays, maximizing overall system efficiency.

The UCC28950 also offers multiple light-load management features including burst mode and dynamic SR on/off control when transitioning in and out of Discontinuous Current Mode (DCM) operation, ensuring ZVS operation is extended down to much lighter loads.

In addition, the UCC28950 includes support for current or voltage mode control. Programmable switching frequency up to 1 MHz and a wide set of protection features including cycle-by-cycle current limit, UVLO and thermal shutdown. A 90-degree phase-shifted interleaved synchronized operation can be easily arranged between two converters.

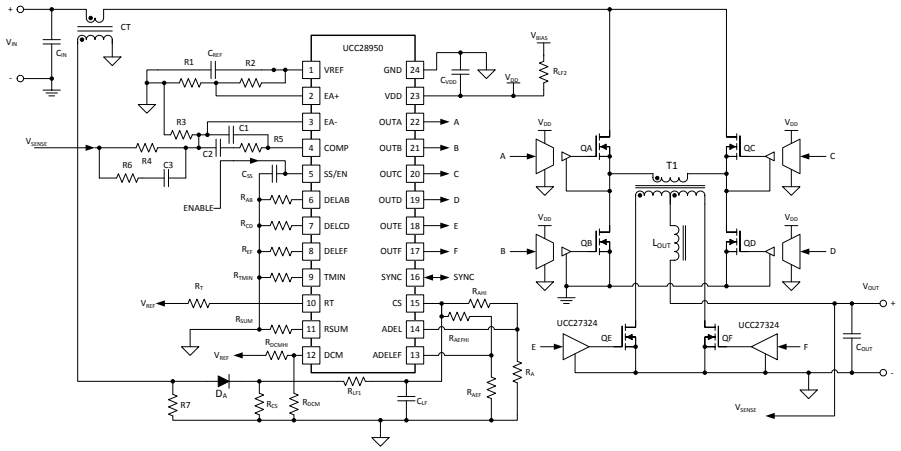
The UCC28950 is available in TSSOP-24 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28950	TSSOP (24)	7.80 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

UCC28950 Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2015) to Revision D — **Page**

- Changed Pin Functions table to be alphabetized. ... 4
- Added text to UCC28950 Startup Timing Diagram note, "Narrower pulse widths (less than 50% duty cycle) may be observed in the first OUTD pulse of a burst. The user must design the bootstrap capacitor charging circuit of the gate driver device so that the first OUTC pulse is transmitted to the MOSFET gate in all cases. Transformer based gate driver circuits are not affected. This behavior is described in more detail in the application note, Gate Driver Design Considerations". ... 9

Changes from Revision B (October 2011) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Moved Standard Temperature Range from ESD table to Absolute Maximum Ratings table ... 5
- Changed Figure 6 Startup Current value from mA to µA. ... 11
- Changed Figure 11 Nominal Switching Frequency value from Hz to kHz. ... 12
- Changed Figure 12 Maximum Switching Frequency value from Hz to kHz. ... 12
- Updated Adaptive Delay section. ... 19
- Changed values in Equation 3 ... 19
- Changed values in Equation 4 ... 19
- Changed line in Figure 34 to stop at R_{TMIN}= 10 kΩ and TMIN = 800 ns. ... 23
- Changed content in *Slope Compensation (R_{SUM})* section. ... 25
- Added T_{MIN} setting to Figure 39. ... 27
- Updated Synchronization (SYNC) section. ... 31
- Changed *Detailed Design Procedure* in the *Typical Application* section. ... 39
- Deleted V_g vs. Q_g for QE and QF FETs graph from Select FETs QE and QF section. ... 48
- Added Daughter Board Schematic. ... 62

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- Added Power Stage Schematic. 63

Changes from Revision A (July 2010) to Revision B **Page**

- Added Naturally Handles Pre-Biased Start Up with DCM Mode bullet 1
- Added Datacom, Telecom, and Wireless Base-Station Power 1
- Changed Server, Telecom Power Supplies bullet to Server, Power Supplies 1

Changes from Original (March 2010) to Revision A **Page**

- Changed UCC28950 Typical Application Diagram 1
- Changed Converter switching frequency from 1400 kHz to 1000 kHz 5
- Changed Functional Block Diagram 16
- Added Figure 30 20
- Changed Equation 21
- Added Typical Application Diagram 21
- Added always deliver even number of Power cycles to Power transformer. 23
- Deleted deliver either one or two power delivery cycle pulses. If controller delivers a power delivery cycle for OUTB and OUTC, then it stops. If it starts delivering to OUTA and OUTD, then it continues with another power delivery cycle to OUTB and OUTC, and then it stops. 23

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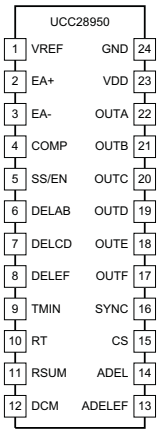
5 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
14	ADEL	I	Dead-time programming for the primary switches over CS voltage range, T_{ABSET} and T_{CDSET}.
13	ADELEF	I	Delay-time programming between primary side and secondary side switches, T_{AFSET} and T_{BESET}.
4	COMP	I/O	Error amplifier output and input to the PWM comparator.
15	CS	I	Current sense for cycle-by-cycle over-current protection and adaptive delay functions.
12	DCM	I	DCM threshold setting.
6	DELAB	I	Dead-time delay programming between OUTA and OUTB.
7	DELCD	I	Dead-time delay programming between OUTC and OUTD.
8	DELEF	I	Delay-time programming between OUTA to OUTF, and OUTB to OUTE.
2	EA+	I	Error amplifier non-inverting input.
3	EA–	I	Error amplifier inverting input.
24	GND	—	Ground. All signals are referenced to this node.
22	OUTA	O	0.2-A sink/source primary switching output.
21	OUTB	O	0.2-A sink/source primary switching output.
20	OUTC	O	0.2-A sink/source primary switching output.
19	OUTD	O	0.2-A sink/source primary switching output.
18	OUTE	O	0.2-A sink/source synchronous switching output.
11	RSUM	I	Slope compensation programming. Voltage mode or peak current mode setting.
10	RT	I	Oscillator frequency set. Master or slave mode setting.
5	SS/EN	I	Soft-start programming, device enable and hiccup mode protection circuit.
16	SYNC	I/O	Synchronization out from Master controller to input of slave controller.
17	OUTF	O	0.2-A sink/source synchronous switching output.
9	TMIN	I	Minimum duty cycle programming in burst mode.
23	VDD	I	Bias supply input.
1	VREF	O	5-V, ±1.5%, 20-mA reference voltage output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
Input supply voltage, V_{DD} (3)	–0.4	20	V
OUTA, OUTB, OUTC, OUTD, OUTE, OUTF	–0.4	VDD + 0.4	V
Input voltage on DELAB, DELCD, DELEF, SS/EN, DCM, TMIN, RT, SYNC, RSUM, EA+, EA-, COMP, CS, ADEL, ADELEF	–0.4	VREF + 0.4	V
Output voltage on VREF	–0.4	5.6	V
Continuous total power dissipation	See Dissipation Ratings		
Operating virtual junction temperature, T_J	–40	+150	°C
Operating ambient temperature, T_A	–40	+125	°C
Lead temperature (soldering, 10 sec.)		+300	°C
Storage temperature, T_{stg}	–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(3) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage range, V_{DD}	8	12	17	V
Operating junction temperature range	–40		125	°C
Converter switching frequency setting range, $F_{SW(nom)}$	50		1000	kHz
Programmable delay range between OUTA, OUTB and OUTC, OUTD set by resistors DELAB and DELCD and parameter K_A (1)	30		1000	ns
Programmable delay range between OUTA, OUTF and OUTB, OUTE set by resistor DELEF, and parameter K_{EF} (1)	30		1400	ns
Programmable DCM range as percentage of voltage at CS (1)	5%		30%	
Programmable T_{MIN} range	100		800	ns

(1) Verified during characterization only.

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6.4 Thermal Information

THERMAL METRIC[1]		UCC28950 PW (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{DD} = 12 V, $T_A = T_J$ = –40°C to +125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, R_{SUM} = 124 kΩ, R_{TMIN} = 88.7 kΩ, R_T = 59 kΩ connected between RT pin and 5-V voltage supply to set F_{SW} = 100 kHz (F_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from Figure 48.

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
UNDERVOLTAGE LOCKOUT (UVLO)						
UVLO_RTH	Start threshold		6.75	7.3	7.9	V
UVLO_FTH	Minimum operating voltage after start		6.15	6.7	7.2	V
UVLO_HYST	Hysteresis		0.53	0.6	0.75	V
SUPPLY CURRENTS						
$I_{DD(off)}$	Startup current	V_{DD} is 5.2 V		150	270	µA
I_{DD}	Operating supply current			5	10	mA
VREF OUTPUT VOLTAGE						
V_{REF}	VREF total output range	0 ≤ IR ≤ 20 mA; V_{DD} = from 8 V to 17 V	4.925	5	5.075	V
ISCC	Short circuit current	VREF = 0 V	–53		–23	mA
SWITCHING FREQUENCY (½ OF INTERNAL OSCILLATOR FREQUENCY F_{OSC})						
$F_{SW(nom)}$	Total range		92	100	108	kHz
D_{MAX}	Maximum duty cycle			95%	97%	
SYNCHRONIZATION						
PH_{SYNC}	Total range	R_T = 59 kΩ between RT and GND; Input pulses 200 kHz, D = 0.5 at SYNC	85	90	95	°PH
F_{SYNC}	Total range	R_T = 59 kΩ between RT and 5 V; –40 °C ≤ T_J ≤ +125°C	180	200	220	kHz
T_{PW}	Pulse width		2.2	2.5	2.8	µs

(1) Typical values for T_A = 25°C

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Electrical Characteristics (continued)

V_{DD} = 12 V, $T_A = T_J$ = –40°C to +125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, R_{SUM} = 124 kΩ, R_{TMIN} = 88.7 kΩ, R_T = 59 kΩ connected between RT pin and 5-V voltage supply to set F_{SW} = 100 kHz (F_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from Figure 48.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
ERROR AMPLIFIER						
V_{ICM}	Common mode input voltage range	V_{ICM} range ensures parameters, the functionality ensured for 3.6 V < V_{ICM} < VREF + 0.4 V, and –0.4 V < V_{ICM} < 0.5 V	0.5		3.6	V
V_{IO}	Offset voltage		– 7		7	mV
I_{BIAS}	Input bias current		–1		1	µA
EA_{HIGH}	High-level output voltage	(EA+) – (EA–) = 500 mV, I_{EAOUT} = –0.5 mA	3.9	4.25		V
EA_{LOW}	Low-level output voltage	(EA+) – (EA–) = –500 mV, I_{EAOUT} = 0.5 mA		0.25	0.35	V
I_{SOURCE}	Error amplifier source current		–8	–3.75	–0.5	mA
I_{SINK}	Error amplifier sink current		2.7	4.6	5.75	mA
I_{VOL}	Open-loop dc gain			100		dB
GBW	Unity gain bandwidth(2)			3		MHz
CYCLE-BY-CYCLE CURRENT LIMIT						
V_{CS_LIM}	CS pin cycle-by-cycle threshold		1.94	2	2.06	V
INTERNAL HICCUP MODE SETTINGS						
I_{DS}	Discharge current to set cycle-by-cycle current limit duration	CS = 2.5 V, VSS = 4 V	15	20	25	µA
V_{HCC}	Hiccup OFF Time threshold		3.2	3.6	4.2	V
I_{HCC}	Discharge current to set Hiccup Mode OFF Time		1.90	2.55	3.2	µA
SOFT START/ENABLE						
I_{SS}	Charge current	V_{SS} = 0 V	20	25	30	µA
V_{SS_STD}	Shutdown/restart/reset threshold		0.25	0.50	0.70	V
V_{SS_PU}	Pull up threshold		3.3	3.7	4.3	V
V_{SS_CL}	Clamp voltage		4.20	4.65	4.95	V
LIGHT-LOAD EFFICIENCY CIRCUIT						
V_{DCM}	DCM threshold, T = 25°C	V_{DCM} = 0.4 V, Sweep CS confirm there are OUTE and OUTF pulses	0.37	0.39	0.41	V
	DCM threshold, T = 0°C to +85°C (3)	V_{DCM} = 0.4 V, Sweep CS, confirm there are OUTE and OUTF pulses	0.364	0.390	0.416	V
	DCM threshold, T= –40°C to +125°C (3)	V_{DCM} = 0.4 V, Sweep CS, confirm there are OUTE and OUTF pulses	0.35	0.39	0.43	V
I_{DCM_SRC}	DCM Sourcing Current	CS < DCM threshold	14	20	26	µA
OUTPUTS OUTA, OUTB, OUTC, OUTD, OUTE, OUTF						
$I_{SINK/SRC}$	Sink/Source peak current(3)			0.2		A
R_{SRC}	Output source resistance	I_{OUT} = 20 mA	10	20	35	Ω
R_{SINK}	Output sink resistance	I_{OUT} = 20 mA	5	10	30	Ω
THERMAL SHUTDOWN						
	Rising threshold(3)			160		°C
	Falling threshold(3)			140		°C
	Hysteresis			20		°C

(2) Verified during characterization only.
(3) Verified during characterization only.

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6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
CYCLE-BY-CYCLE CURRENT LIMIT					
T_{CS}	Propagation delay from CS to OUTC and OUTD outputs Input pulse between CS and GND from zero to 2.5 V		100		ns
PROGRAMMABLE DELAY TIME SET ACCURACY AND RANGE(1)(2)(3)(4)(5)					
T_{ABSET1}	Short delay time set accuracy between OUTA and OUTB CS = ADEL = ADELEF = 1.8 V	32	45	56	ns
T_{ABSET2}	Long delay time set accuracy between OUTA and OUTB CS = ADEL = ADELEF = 0.2 V	216	270	325	ns
T_{CDSET1}	Short delay time set accuracy between OUTC and OUTD CS = ADEL = ADELEF = 1.8 V	32	45	56	ns
T_{CDSET2}	Long delay time set accuracy between OUTC and OUTD CS = ADEL = ADELEF = 0.2 V	216	270	325	ns
T_{AFSET1}	Short delay time set accuracy between falling OUTA, OUTF CS = ADEL = ADELEF = 0.2 V	22	35	48	ns
T_{AFSET2}	Long delay time set accuracy between falling OUTA, OUTF CS = ADEL = ADELEF = 1.8 V	190	240	290	ns
T_{BESET1}	Short delay time set accuracy between falling OUTB, OUTE CS = ADEL = ADELEF = 0.2 V	22	35	48	ns
T_{BESET2}	Long delay time set accuracy between falling OUTB, OUTE CS = ADEL = ADELEF = 1.8 V	190	240	290	ns
ΔT_{ADBC}	Pulse matching between OUTA rise, OUTD fall and OUTB rise, OUTC fall CS = ADEL = ADELEF = 1.8 V, COMP = 2 V	–50	0	50	ns
ΔT_{ABBA}	Half cycle matching between OUTA rise, OUTB rise and OUTB rise, OUTA rise CS = ADEL = ADELEF = 1.8 V, COMP = 2 V	–50	0	50	ns
ΔT_{EEFF}	Pulse matching between OUTE fall, OUTE rise and OUTF fall, OUTF rise CS = ADEL = ADELEF = 0.2 V, COMP = 2 V	–60	0	60	ns
ΔT_{EFFE}	Pulse matching between OUTE fall, OUTF rise and OUTF fall, OUTE rise CS = ADEL = ADELEF = 0.2 V, COMP = 2 V	–60	0	60	ns
LIGHT-LOAD EFFICIENCY CIRCUIT					
T_{MIN}	Total range, R_{TMIN} = 88.7 kΩ	425	525	625	ns
OUTPUTS OUTA, OUTB, OUTC, OUTD, OUTE, OUTF					
T_R	Rise time, C_{LOAD} = 100 pF		9	25	ns
T_F	Fall time, C_{LOAD} = 100 pF		7	25	ns

(1) See Figure 28 for timing diagram and T_{ABSET1}, T_{ABSET2}, T_{CDSET1}, T_{CDSET2} definitions.
(2) See Figure 31 for timing diagram and T_{AFSET1}, T_{AFSET2}, T_{BESET1}, T_{BESET2} definitions.
(3) Pair of outputs OUTC, OUTE and OUTD, OUTF always going high simultaneously.
(4) Outputs A or B are never allowed to go high if both outputs OUTE and OUTF are high.
(5) All delay settings are measured relative to 50% of pulse amplitude.

6.7 Dissipation Ratings

over operating free-air temperature range (unless otherwise noted)

PACKAGE	DERATING FACTOR	POWER RATING		
	ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
PW	10.7 mW/°C	1.07 W	0.59 W	0.429 W

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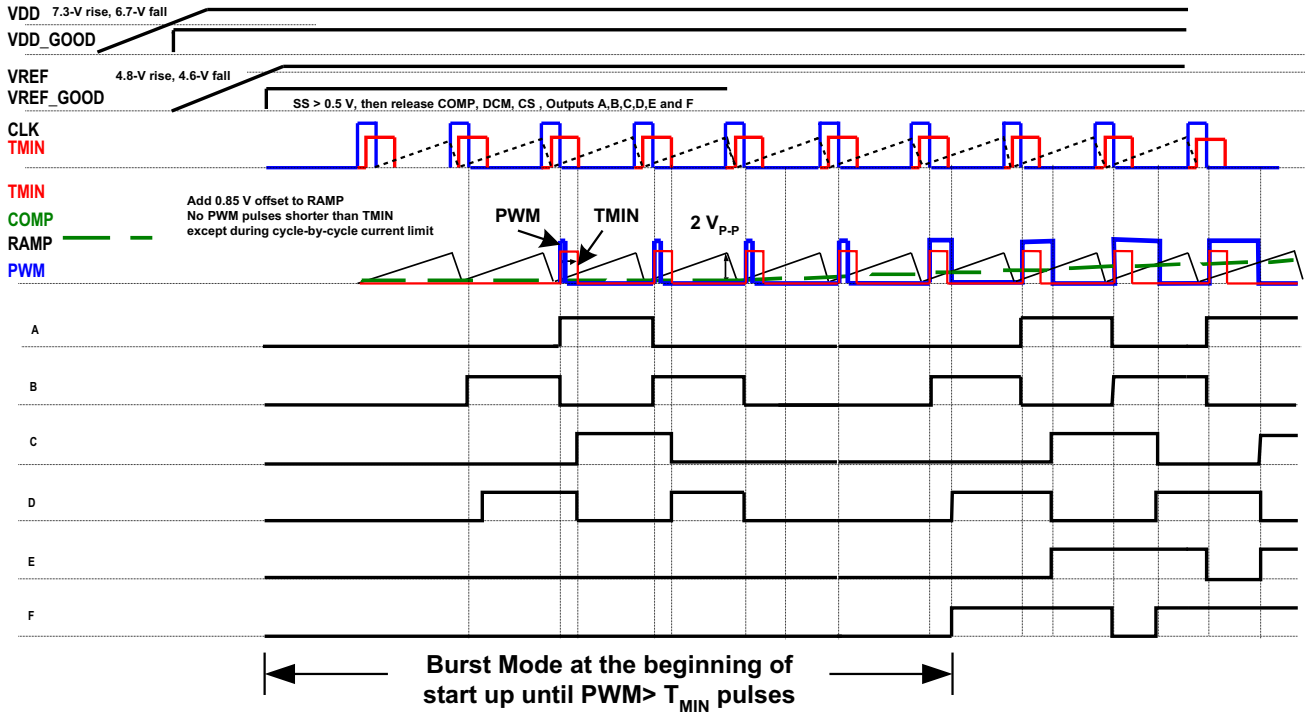

No output delay shown, COMP-to-RAMP offset not included.

There is no pulse on OUTE during burst mode at startup. Two falling edge PWM pulses are required before enabling the synchronous rectifier outputs. Narrower pulse widths (less than 50% duty cycle) may be observed in the first OUTD pulse of a burst. The user must design the bootstrap capacitor charging circuit of the gate driver device so that the first OUTC pulse is transmitted to the MOSFET gate in all cases. Transformer based gate driver circuits are not affected. This behavior is described in more detail in the application note, Gate Driver Design Considerations.

Figure 1. UCC28950 Startup Timing Diagram

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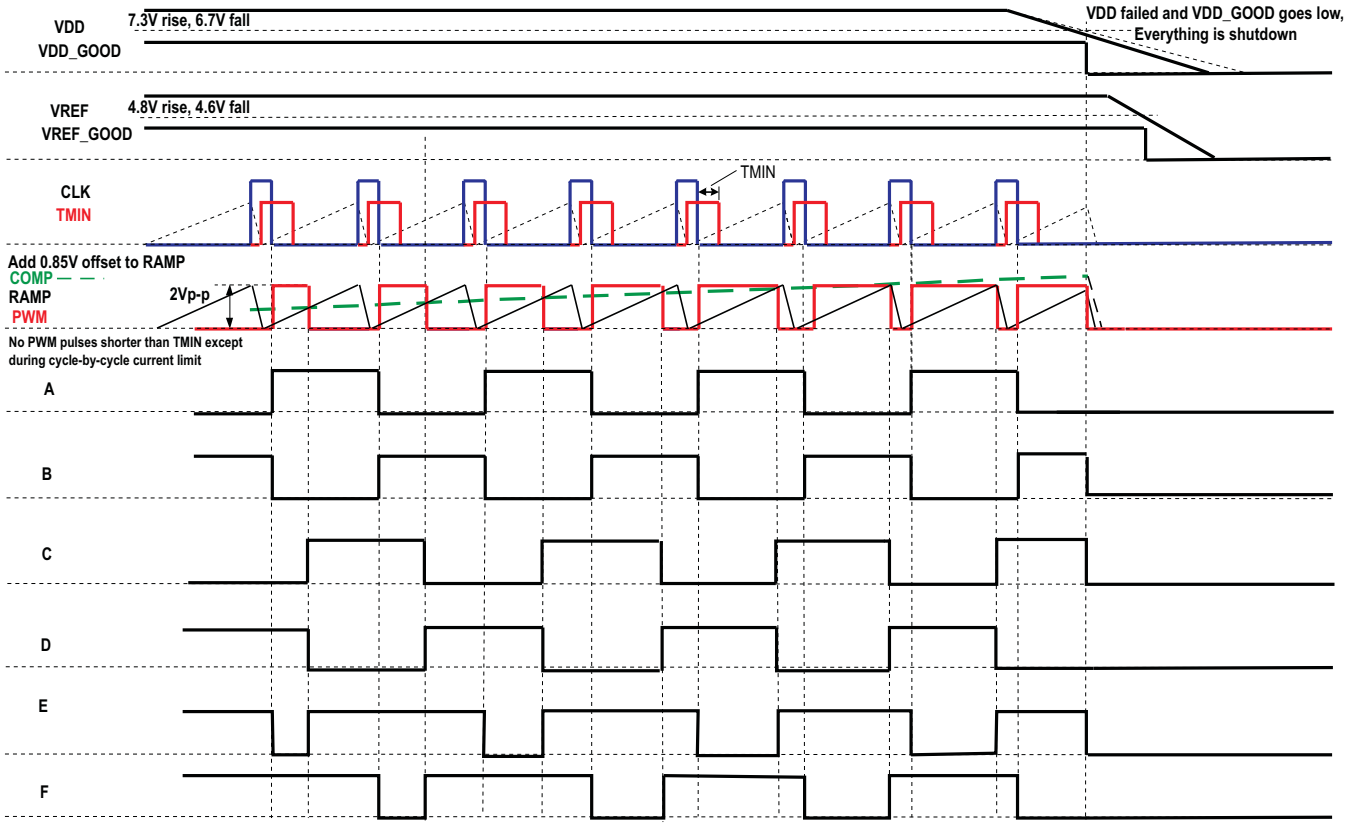

No output delay shown, COMP-to-RAMP offset not included.

Figure 2. UCC28950 Steady State/Shutdown Timing Diagram

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6.8 Typical Characteristics

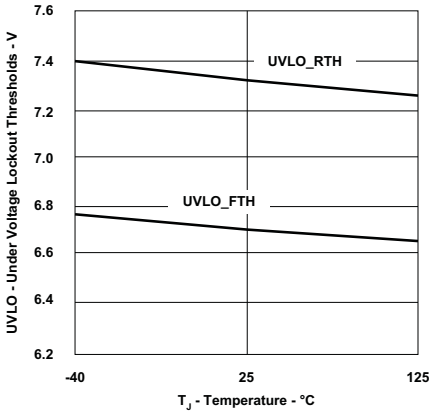

Figure 3. UVLO Thresholds vs Temperature

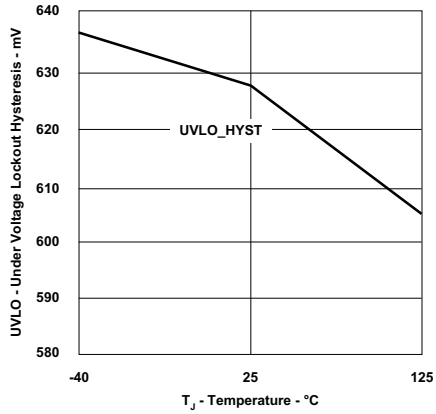

Figure 4. UVLO Hysteresis vs Temperature

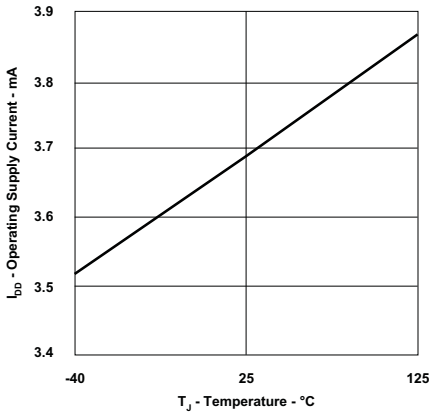

Figure 5. Supply Current vs Temperature

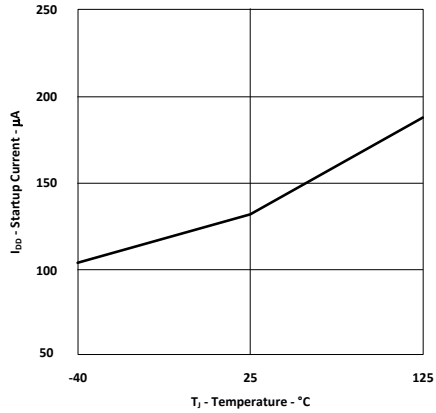

Figure 6. Startup Current vs Temperature

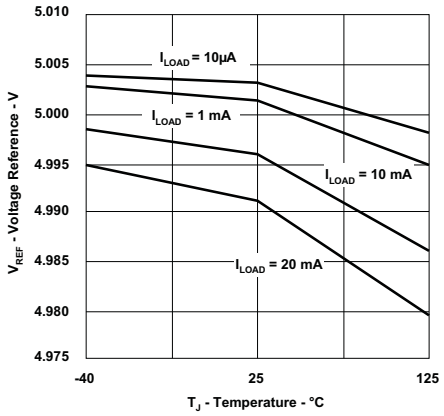

Figure 7. Voltage Reference (VDD = 12 V) vs Temperature

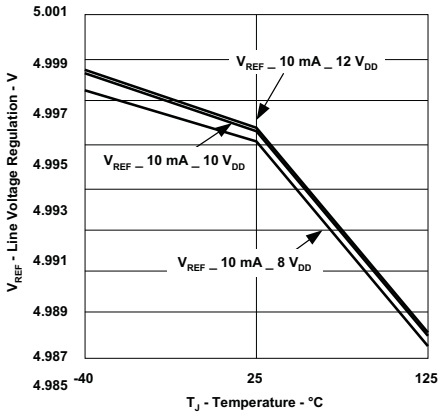

Figure 8. Line Voltage Regulation (I_{LOAD} = 10 mA) vs Temperature

Typical Characteristics (continued)

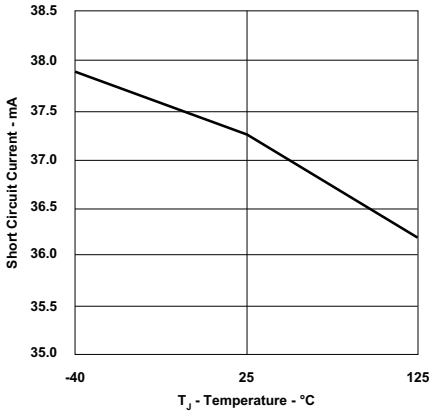

Figure 9. Short Circuit Current vs Temperature

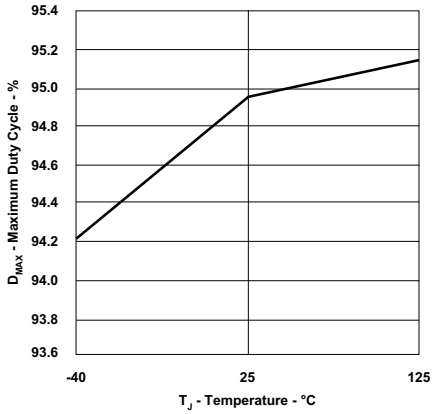

Figure 10. Maximum Duty Cycle vs Temperature

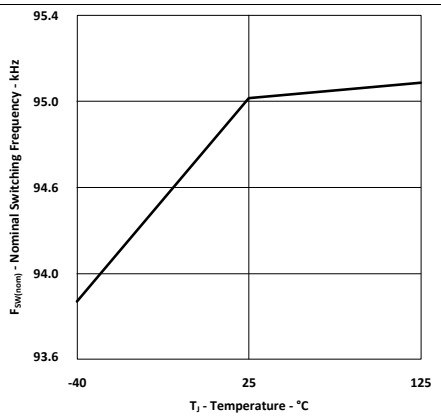

Figure 11. Nominal Switching Frequency vs Temperature

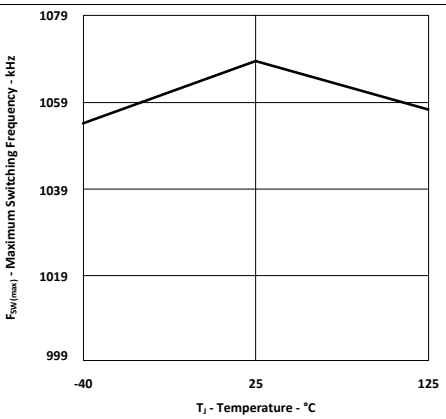

Figure 12. Maximum Switching Frequency vs Temperature

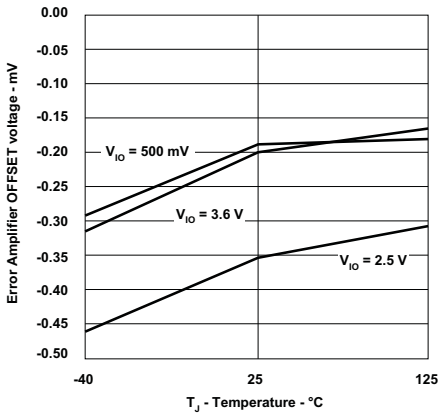

Figure 13. Error Amplifier Offset Voltage vs Temperature

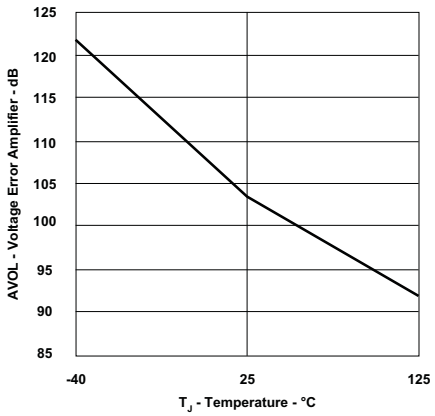

Figure 14. Voltage Error Amplifier (Open Loop Gain) vs Temperature

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Typical Characteristics (continued)

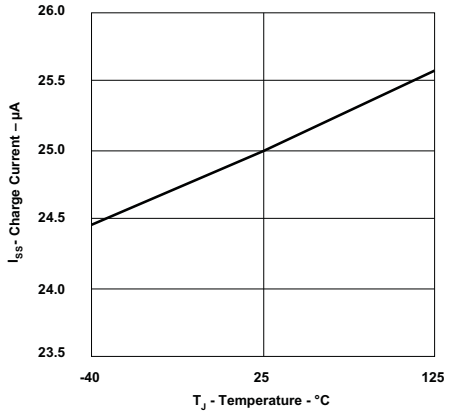

Figure 15. I_{SS} Charge Current vs Temperature

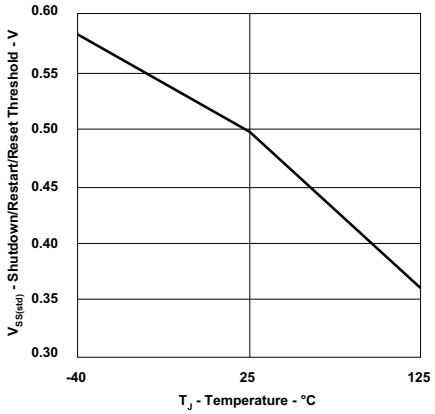

Figure 16. Shutdown/Restart/Reset Threshold vs Temperature

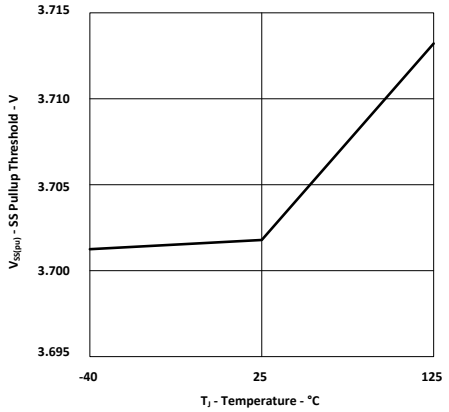

Figure 17. SS Pull-Up Threshold vs Temperature

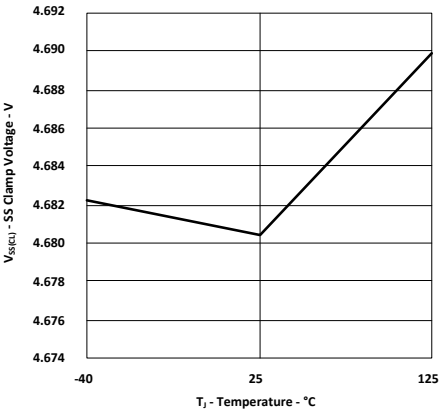

Figure 18. SS Clamp Voltage vs Temperature

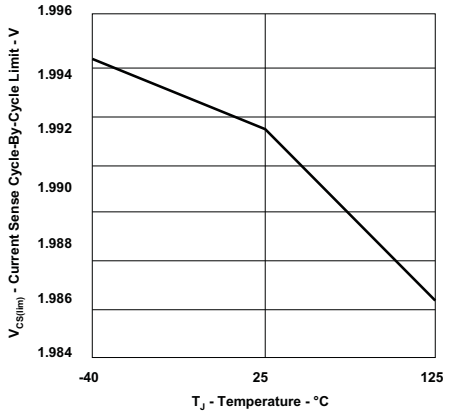

Figure 19. Current Sense Cycle-by-Cycle Limit vs Temperature

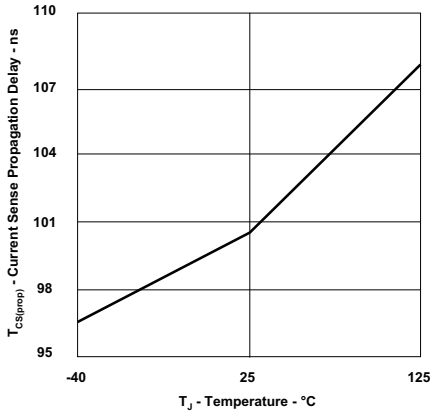

Figure 20. Current Sense Propagation Delay vs Temperature

Typical Characteristics (continued)

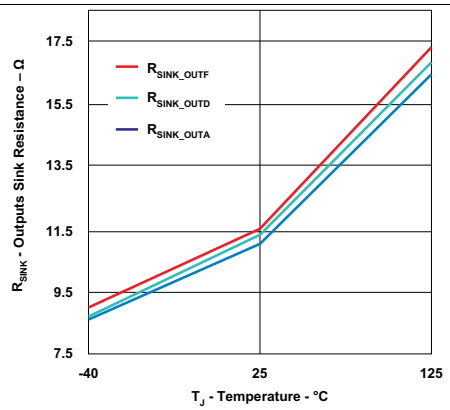

Figure 21. Outputs Sink Resistance vs Temperature

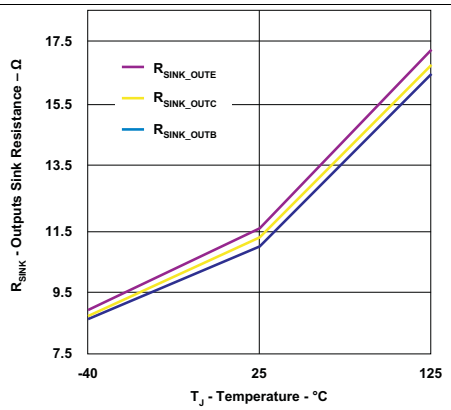

Figure 22. Outputs Sink Resistance vs Temperature

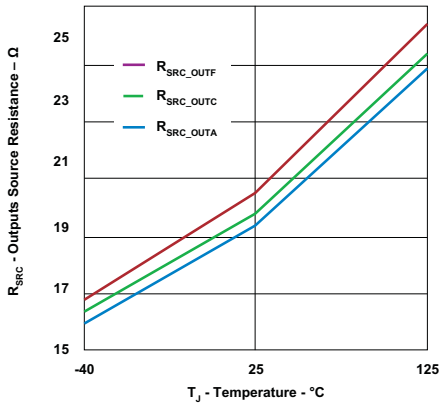

Figure 23. Outputs Source Resistance vs Temperature

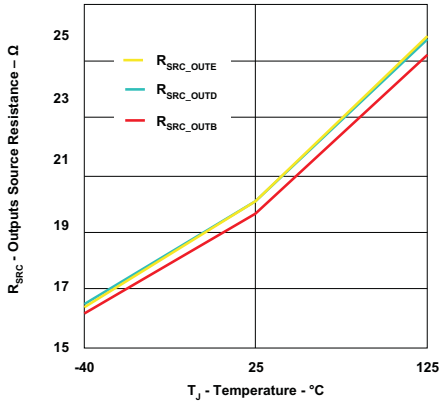

Figure 24. Outputs Source Resistance vs Temperature

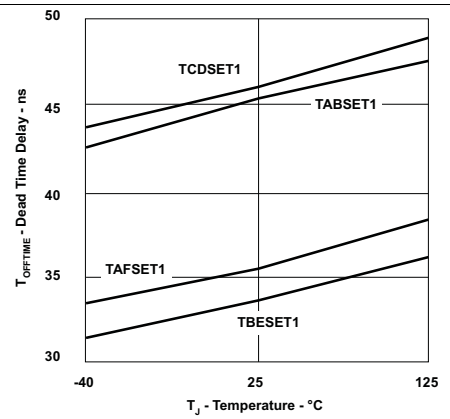

Figure 25. Dead Time Delay vs Temperature

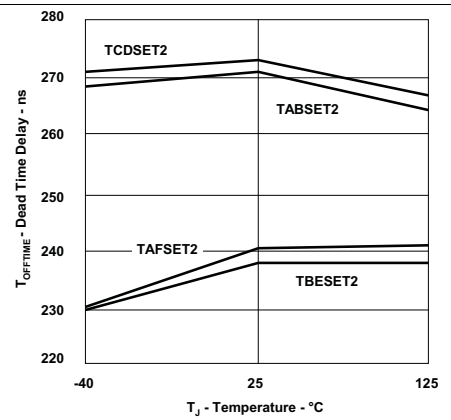

Figure 26. Dead Time Delay vs Temperature

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Typical Characteristics (continued)

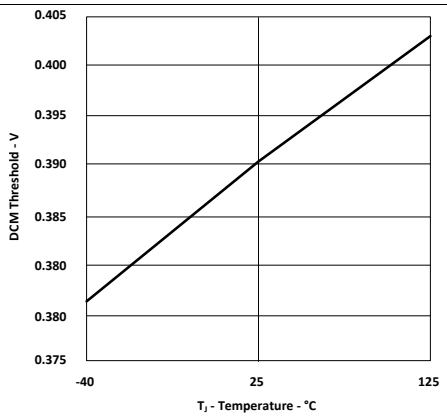

Figure 27. DCM Threshold vs Temperature

7 Detailed Description

7.1 Overview

The UCC28950 device combines all the functions necessary to control a phase-shifted full bridge power stage in a 24-pin TSSOP package. The device includes two Synchronous-Rectifier (SR), gate-drive outputs as well as the outputs needed to drive all four switches in the full-bridge circuit. The dead times between the upper and lower switches in the full bridge may be set using the DELAB and DELCD inputs. Further, this dead time may be dynamically adjusted according to the load level using the ADEL pin. This allows the user to optimize the dead time for their particular power circuit and to achieve ZVS over the entire operating range. In a similar manner, the dead times between the full bridge switches and the secondary SRs may be optimized using the DELEF input. This dead time may also be dynamically adjusted according to the load, using the ADELEF input to the controller. A DCM (Discontinuous Conduction Mode) option disables the SRs at a user settable light load in order to improve power circuit efficiency. The device enters a light-load-burst mode if the feedback loop demands a conduction time less than a user settable level (TMIN).

At higher-power levels, two or more UCC28950 devices may be easily synchronized in a Master/Slave configuration. A SS/EN input may be used to set the length of the soft start process and to turn the controller on and off. The controller may be configured for Voltage mode or Current mode control. Cycle-by-cycle current limiting is provided in Voltage mode and Peak Current mode. The switching frequency may be set over a wide range making this device suited to both IGBT and MOSFET based designs.

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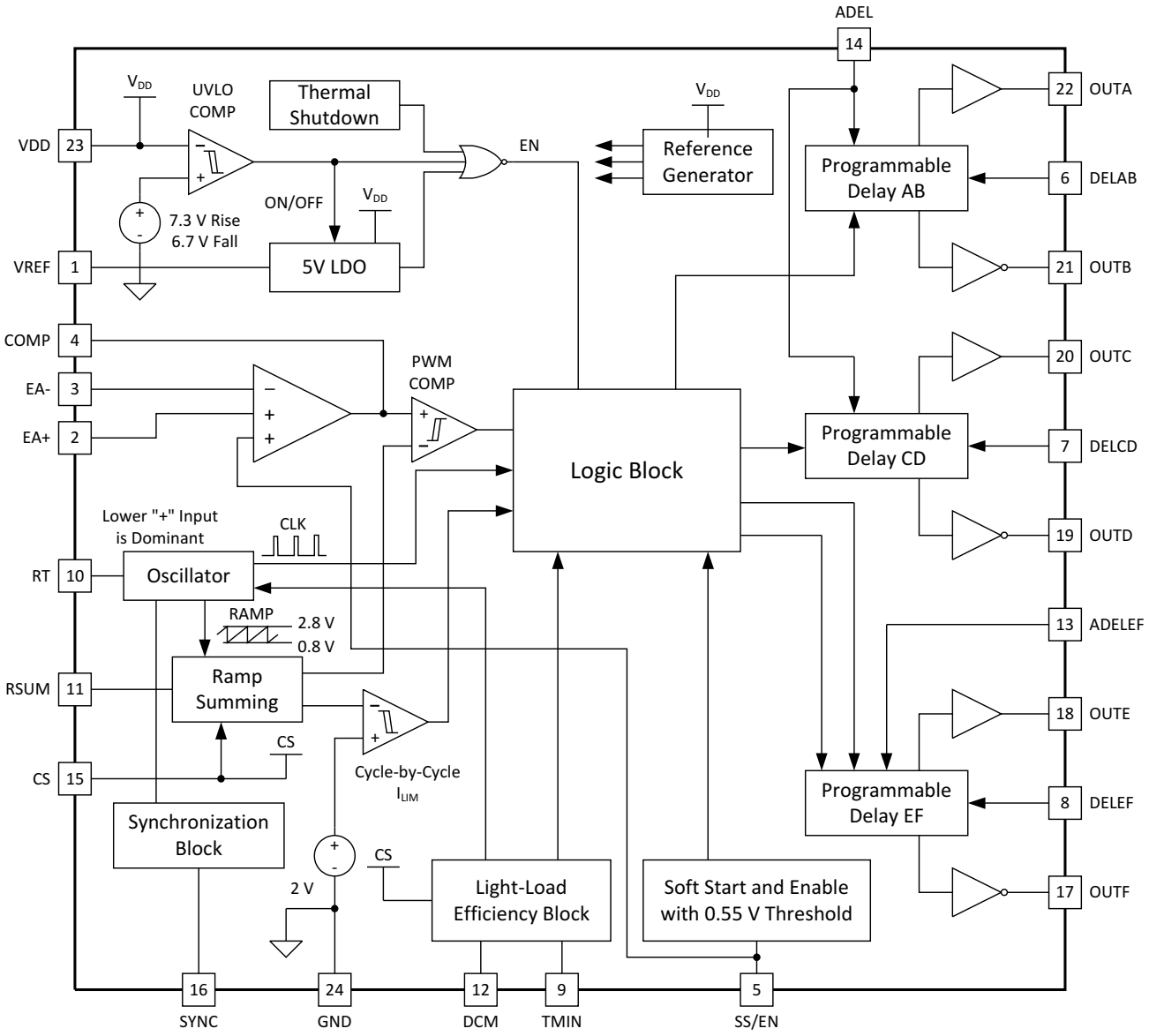
7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Start-Up Protection Logic

Before the UCC28950 controller will start up, the following conditions must be met:

- VDD voltage exceeds rising UVLO threshold 7.3-V typical.
- The 5-V reference voltage is available.
- Junction temperature is below the thermal shutdown threshold of 140°C.
- The voltage on the soft-start capacitor is not below 0.55-V typical.

If all those conditions are met, an internal enable signal EN is generated that initiates the soft start process. The duty cycle during the soft start is defined by the voltage at the SS pin, and cannot be lower than the duty cycle set by TMIN, or by cycle-by-cycle current limit circuit depending on load conditions.

7.3.2 Voltage Reference (VREF)

The accurate (±1.5%) 5-V reference voltage regulator with a short circuit protection circuit supplies internal circuitry and provides up to 20-mA external output current. Place a low ESR and ESL, preferably ceramic decoupling capacitor C_{REF} in 1-µF to 2.2-µF range from this pin to GND as close to the related pins as possible for best performance. The only condition where the reference regulator is shut down internally is during under voltage lockout.

7.3.3 Error Amplifier (EA+, EA–, COMP)

The error amplifier has two uncommitted inputs, EA+ and EA-, with a 3-MHz unity gain bandwidth, which allows flexibility in closing the feedback loop. The EA+ is a non-inverting input, the EA– is an inverting input and the COMP is the output of the error amplifier. The input voltage common mode range, where the parameters of the error amplifier are guaranteed, is from 0.5 V to 3.6 V. The output of the error amplifier is connected internally to the non-inverting input of the PWM comparator. The range of the error amplifier output of 0.25 V to 4.25 V far exceeds the PWM comparator input ramp-signal range, which is from 0.8 V to 2.8 V. The soft-start signal serves as an additional non-inverting input of the error amplifier. The lower of the two non-inverting inputs of the error amplifier is the dominant input and sets the duty cycle where the output signal of the error amplifier is compared with the internal ramp at the inputs of the PWM comparator.

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Feature Description (continued)

7.3.4 Soft Start and Enable (SS/EN)

The soft-start pin SS/EN is a multi-function pin used for the following operations:

- Closed loop soft start with the gradual duty cycle increase from the minimum set by TMIN up to the steady state duty cycle required by the regulated output voltage.
- Setting hiccup mode conditions during cycle-by-cycle overcurrent limit.
- On/off control for the converter.

During soft start, one of the voltages at the SS/EN or EA+ pins, whichever is lower (SS/EN – 0.55 V) or EA+ voltage (see Block Diagram), sets the reference voltage for a closed feedback loop. Both SS/EN and EA+ signals are non-inverting inputs of the error amplifier with the COMP pin being its output. Thus the soft start always goes under the closed feedback loop and the voltage at COMP pin sets the duty cycle. The duty cycle defined by the COMP pin voltage can not be shorter than TMIN pulse width set by the user. However, if the shortest duty cycle is set by the cycle-by-cycle current limit circuit, then it becomes dominant over the duty cycle defined by the COMP pin voltage or by the TMIN block.

The soft-start duration is defined by an external capacitor C_{SS}, connected between the SS/EN pin and ground, and the internal charge current that has a typical value of 25 µA. Pulling the soft-start pin externally below 0.55 V shuts down the controller. The release of the soft-start pin enables the controller to start, and if there is no current limit condition, the duty cycle applied to the output inductor gradually increases until it reaches the steady state duty cycle defined by the regulated output voltage of the converter. This happens when the voltage at the SS/EN pin reaches and then exceeds by 0.55 V, the voltage at the EA+ pin. Thus for the given soft-start time T_{SS}, the C_{SS} value can be defined by Equation 1 or Equation 2:

$$C_{SS(master)} = \frac{T_{SS} \times 25\,\mu A}{(0.55 + EA+)} \quad (1)$$

$$C_{SS(slave)} = \frac{T_{SS}}{825k \times Ln\left(\frac{20.6}{20.6 - 0.55 - EA+}\right)} \quad (2)$$

For example, in Equation 1, if the soft-start time T_{SS} is selected to be 10 ms, and the EA+ pin is 2.5 V, then the soft-start capacitor C_{SS} is equal to 82 nF.

NOTE

If the converter is configured in Slave Mode, place an 825-kΩ resistor from SS pin to ground.

7.3.5 Light-Load Power Saving Features

The UCC28950 offers four different light-load management techniques for improving the efficiency of a power converter over a wide load current range.

1. Adaptive Delay,
   (a) ADEL, which sets and optimizes the dead-time control for the primary switches over a wide load current range.
   (b) ADELEF, which sets and optimizes the delay-time control between the primary side switches and the secondary side switches.
2. TMIN, sets the minimum pulse width as long as the part is not in current limit mode.
3. Dynamic synchronous rectifier on/off control in DCM Mode, For increased efficiency at light loads. The DCM Mode starts when the voltage at CS pin is lower than the threshold set by the user. In DCM Mode, the synchronous output drive signals OUTE and OUTF are brought down low.
4. Burst Mode, for maximum efficiency at very light loads or no load. Burst Mode has an even number of PWM TMIN pulses followed by off time. Transition to the Burst Mode is defined by the TMIN duration set by the user.

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Feature Description (continued)

7.3.6 Adaptive Delay, (Delay between OUTA and OUTB, OUTC and OUTD (*DELAB, DELCD, ADEL*))

The resistor R_{AB} from the DELAB pin, DELAB to GND, along with the resistor divider R_{AHI} from CS pin to ADEL pin and R_A from ADEL pin to GND sets the delay T_{ABSET} between one of outputs OUTA or OUTB going low and the other output going high Figure 28. The total resistance of this resistor divider should be in the range between 10 kΩ and 20 kΩ

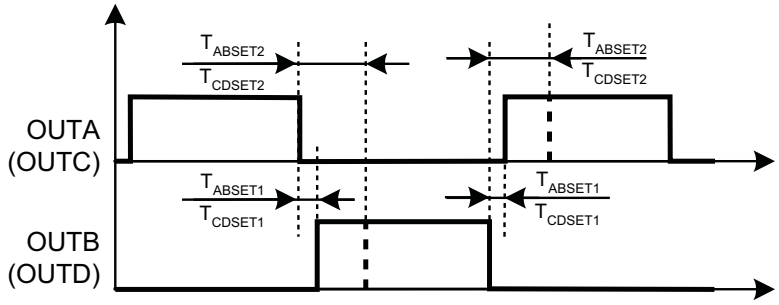

Figure 28. Delay Definitions Between OUTA and OUTB, OUTC and OUTD

This delay gradually increases as a function of the CS signal from T_{ABSET1}, which is measured at V_{CS} = 1.8 V, to T_{ABSET2}, which is measured at the V_{CS} = 0.2 V. This approach ensures there will be no shoot-through current during the high-side and low-side MOSFET switching and optimizes the delay for acheiving ZVS condition over a wide load current range. The ratio between the longest and shortest delays is set by the resistor divider R_{AHI} and R_A. The max ratio is achieved by tying the CS and ADEL pins together. If ADEL is connected to GND, then the delay is fixed, defined only by the resistor R_{AB} from DELAB to GND. The delay T_{CDSET1} and T_{CDSET2} settings and their behaviour for outputs OUTC and OUTD are very similar to the one described for OUTA and OUTB. The difference is that resistor R_{CD} connected between DELCD pin and GND sets the delay T_{CDSET}. The ratio between the longest and shortest delays is set by the resistor divider R_{AHI} and R_A.

The delay time T_{ABSET} is defined by the following Equation 3.

$$T_{ABSET} = \left(\frac{5 \times R_{AB}}{0.26\,V + CS \times K_A \times 1.3} \right) ns \tag{3}$$

The same equation is used to define the delay time T_{CDSET} in another leg except R_{AB} is replaced by R_{CD}.

$$T_{CDSET} = \left(\frac{5 \times R_{CD}}{0.26\,V + CS \times K_A \times 1.3} \right) ns \tag{4}$$

In these equations R_{AB} and R_{CD} are in kΩ and CS, the voltage at pin CS, is in volts and K_A is a numerical coefficient in the range from 0 to 1. The delay time T_{ABSET} and T_{CDSET} are in ns, and is measured at the IC pins. These equations are empirical and they are approximated from measured data. Thus, there is no unit agreement in the equations. As an example, assume R_{AB} = 15 kΩ, CS = 1 V and K_A = 0.5. Then the T_{ABSET} will be approximately 90 ns. In both Equation 3 and Equation 4, K_A is the same and is defined as:

$$K_A = \frac{R_A}{R_A + R_{AHI}} \tag{5}$$

K_A sets how the delay varies with the CS pin voltage as shown in Figure 29 and Figure 30.

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Feature Description (continued)

It is recommended to start by setting K_A = 0 and set T_{ABSET} and T_{CDSET} relatively large using equations or plots in this data sheet to avoid hard switching or even shoot through current. The delay between outputs A, B and C, D set by resistors R_{AB} and R_{CS} accordingly. Program the optimal delays at light load first. Then by changing K_A set the optimal delay for the outputs A, B at maximum current. K_A for outputs C, D is the same as for A,D. Usually outputs C, D always have ZVS if sufficient delay is provided.

NOTE

The allowed resistor range on DELAB and DELCD, R_{AB} and R_{CD} is 13 kΩ to 90 kΩ.

R_A and R_{AHI} define the portion of voltage at pin CS applied to the pin ADEL (See Figure 48). K_A defines how significantly the delay time depends on CS voltage. K_A varies from 0, where ADEL pin is shorted to ground (R_A = 0) and the delay does not depend on CS voltage, to 1, where ADEL is tied to CS (R_{AHI} = 0). Setting K_A, R_{AB} and R_{CD} provides the ability to maintain optimal ZVS conditions of primary switches over load current because the voltage at CS pin includes the load current reflected to the primary side through the current sensing circuit. The plots in Figure 29 and Figure 30 show the delay time settings as a function of CS voltage and K_A for two different conditions: R_{AB} = R_{CD} = 13 kΩ (Figure 29) and R_{AB} = R_{CD} = 90 kΩ (Figure 30).

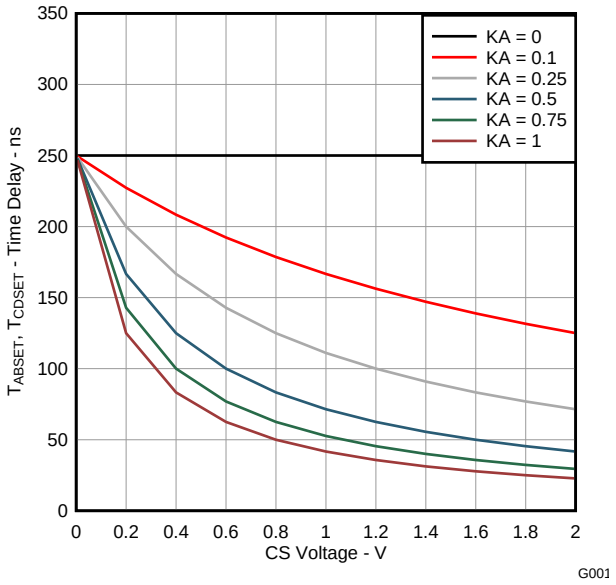

Figure 29. Delay Time Set T_{ABSET} and T_{CDSET} (Over CS voltage variation and selected K_A for R_{AB} and R_{CD} equal 13 kΩ)

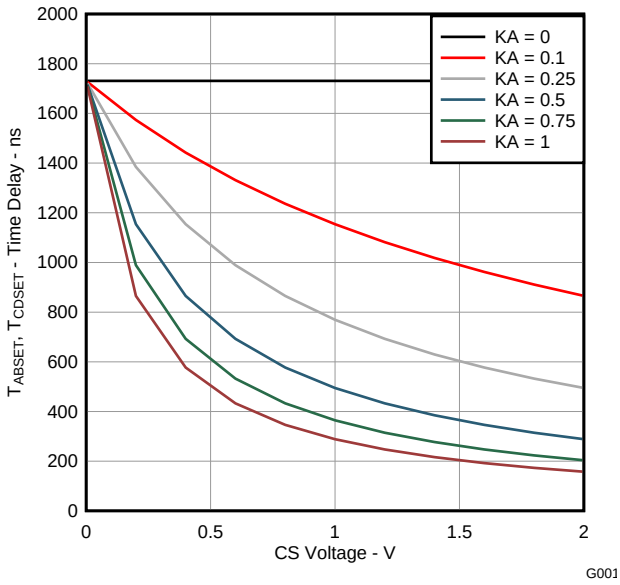

Figure 30. Delay time set T_{ABSET} and T_{CDSET} (Over CS voltage variation and selected K_A for R_{AB} and R_{CD} equal 90 kΩ)

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Feature Description (continued)

7.3.7 Adaptive Delay (Delay between OUTA and OUTF, OUTB and OUTE (*DELEF, ADELEF*))

The resistor R_{EF} from the DELEF pin to GND along with the resistor divider R_{AEFHI} from CS pin to ADELEF pin and R_{AEF} from ADELEF pin to GND sets equal delays T_{AFSET} and T_{BESET} between outputs OUTA or OUTB going low and related output OUTF or OUTE going low Figure 31. The total resistance of this resistor divider should be in the range between 10kΩ and 20kΩ.

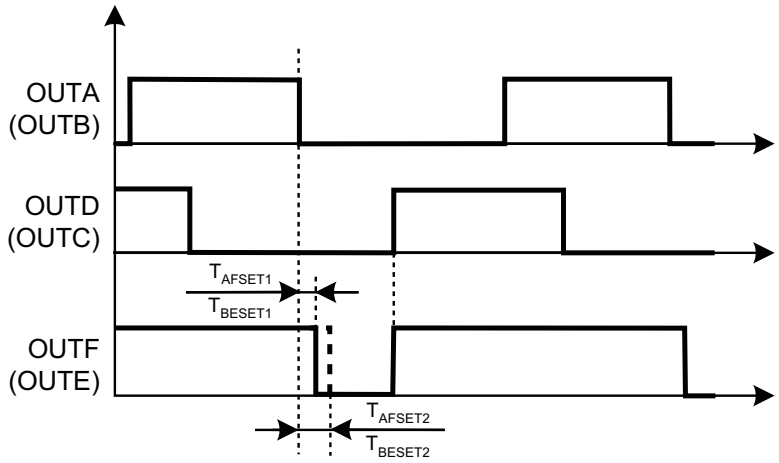

Figure 31. Delay Definitions Between OUTA and OUTF, OUTB and OUTE

These delays gradually increase as function of the CS signal from T_{AFSET1}, which is measured at V_{CS} = 0.2 V, to T_{AFSET2}, which is measured at V_{CS} = 1.8 V. This is opposite to the DELAB and DELCD behavior and this delay is longest (T_{AFSET2}) when the signal at CS pin is maximized and shortest (T_{AFSET1}) when the CS signal is minimized. This approach will reduce the synchronous rectifier MOSFET body diode conduction time over a wide load current range thus improving efficiency . The ratio between the longest and shortest delays is set by the resistor divider R_{AEFHI} and R_{AEF}. If CS and ADELEF are tied, the ratio is maximized. If ADELEF is connected to GND, then the delay is fixed, defined only by resistor R_{EF} from DELEF to GND.

The delay time T_{AFSET} is defined by the following Equation 6. *Equation 6* also defines the delay time T_{BESET}.

$$T_{AFSET} = \left(\left(\frac{5 \times R_{EF}}{2.65\,V - CS \times K_{EF} \times 1.32} \right) ns + 4\,ns \right) \tag{6}$$

In this equation R_{EF} is in kΩ, the CS, which is the voltage at pin CS, is in volts and K_{EF} is a numerical gain factor of CS voltage from 0 to 1. The delay time T_{AFSET} is in ns, and is measured at the IC pins. This equation is an empirical approximation of measured data, thus, there is no unit agreement in it. As an example, assume R_{EF} = 15 kΩ, CS = 1 V and K_{EF} = 0.5. Then the T_{AFSET} is going to be 41.7 ns. K_{EF} is defined as:

$$K_{EF} = \frac{R_{AEF}}{R_{AEF} + R_{AEF(hi)}} \tag{7}$$

R_{AEF} and R_{AEFHI} define the portion of voltage at pin CS applied to the pin ADELEF (See Figure 48). K_{EF} defines how significantly the delay time depends on CS voltage. K_{EF} varies from 0, where ADELEF pin is shorted to ground (R_{AEF} = 0) and the delay does not depend on CS voltage, to 1, where ADELEF is tied to CS (R_{AEFHI} = 0).

NOTE

The allowed resistor range on DELEF, R_{EF} is 13 kΩ to 90 kΩ.

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Feature Description (continued)

The plots in Figure 32 and Figure 33 show delay time settings as function of CS voltage and K_{EF} for two different conditions: R_{EF} = 13kΩ (Figure 32) and R_{EF} = 90kΩ (Figure 33)

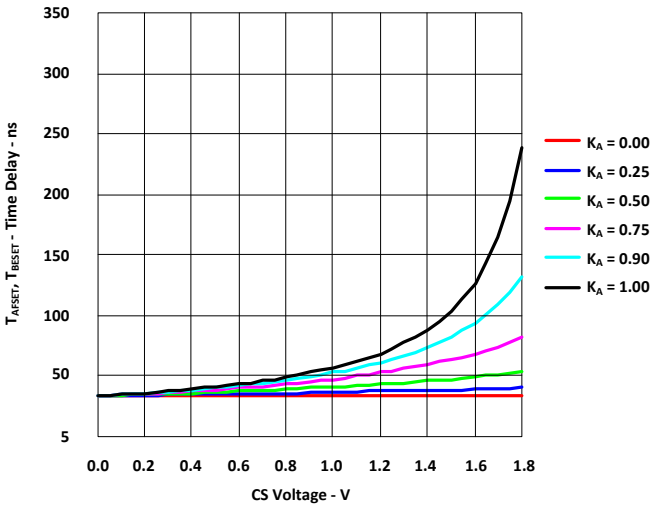

Figure 32. Delay Time T_{AFSET} and T_{BESET} (Over CS Voltage and Selected K_{EF} for R_{EF} equal 13 kΩ)

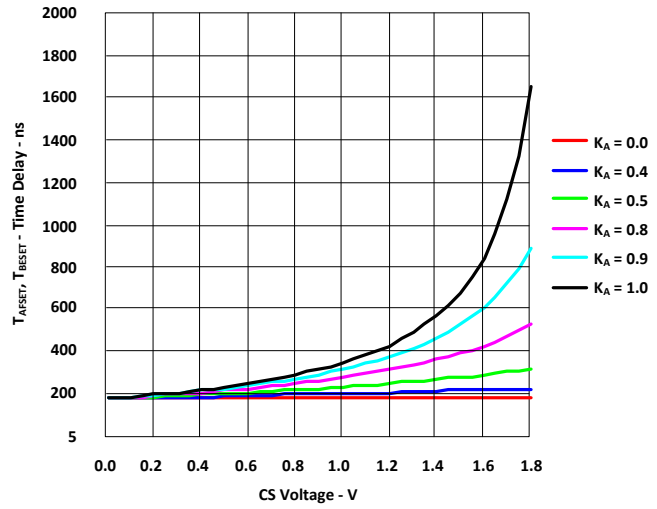

Figure 33. Delay Time T_{AFSET} and T_{BESET} (Over CS Voltage and Selected K_{EF} for R_{EF} equal 90 kΩ)

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Feature Description (continued)

7.3.8 Minimum Pulse (TMIN)

The resistor R_{TMIN} from the TMIN pin to GND sets a fixed minimum pulse width. This pulse is applied to the transformer and enables ZVS at light load. If the output PWM pulse demanded by the feedback loop is shorter than TMIN, then the controller proceeds to burst mode operation where an even number of TMIN pulses are followed by the off time dictated by the feedback loop. The proper selection of the TMIN duration is dictated by the time it takes to raise sufficient magnetizing current in the power transformer to maintain ZVS. The TMIN pulse is measured from the rising edge of OUTA to the falling edge of OUTD – or from the rising edge of OUTB to the falling edge of OUTC. The minimum pulse TMIN is then defined by Equation 8.

$$TMIN = \left(5.92 \times R_{TMIN}\right) ns \tag{8}$$

Where TMIN is in ns and R_{TMIN} is in kΩ The pulse width measured at the transformer will be modified (usually increased) by various propagation and response time delays in the power circuit. Because of the propagation and response time delays in the power circuit, selecting the correct TMIN setting will be an iterative process.

NOTE

The minimum allowed resistor on TMIN, R_{TMIN} is 10 kΩ.

The related plot is shown in Figure 34.

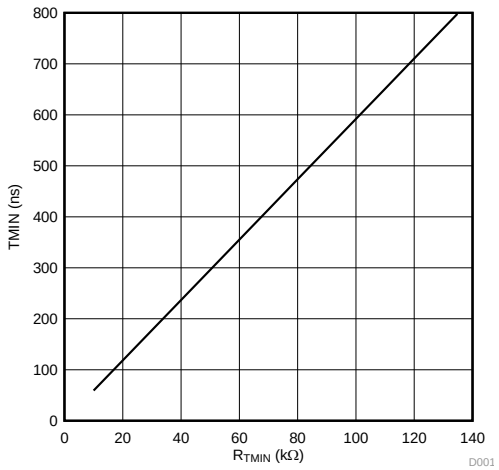

Figure 34. Minimum Time TMIN Over Setting Resistor R_{TMIN}

The value of minimum duty cycle DMIN is determined by Equation 9.

$$DMIN = \left(TMIN \times F_{SW(osc)} \times 10^{-4}\right)\% \tag{9}$$

Here, $F_{SW(osc)}$ is oscillator frequency in kHz, TMIN is the minimum pulse in ns and DMIN is in percent.

7.3.9 Burst Mode

If the converter is commanding a duty cycle lower than TMIN, then the controller will go into Burst Mode. The controller will always deliver an even number of Power cycles to the Power transformer. The controller always stops its bursts with an OUTB and an OUTC power delivery cycle. If the controller is still demanding a duty cycle less than TMIN, then the controller goes into shut down mode. Then it waits until the converter is demanding a duty cycle equal or higher than TMIN before the controller puts out TMIN or a PWM duty cycle as dictated by COMP voltage pin.

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Feature Description (continued)

7.3.10 Switching Frequency Setting

Connecting an external resistor R_T between the RT pin and VREF pins sets the fixed frequency operation and configures the controller as a master providing synchronization output pulses at SYNC pin with 0.5 duty cycle and frequency equal to the internal oscillator. To set the converter in slave mode, connect the external resistor R_T between the RT pin to GND and place an 825-kΩ resistor from the SS pin to GND in parallel with the SS_EN capacitor. This configures the controller as a slave. The slave controller operates with 90° phase shift relative to the master converter if their SYNC pins are tied together. The switching frequency of the converter is equal to the frequency of output pulses. The following Equation 10 defines the nominal switching frequency of the converter configured as a master (resistor R_T between the RT pin and VREF). On the UCC28950 there is an internal clock oscillator frequency which is twice as that of the controller's output frequency.

$$F_{SW(nom)} = \left(\frac{2.5 \times 10^3}{\left(\frac{R_T}{V_{REF} - 2.5\,V} + 1 \times \frac{k\Omega}{V} \right)} \right) kHz \tag{10}$$

In this equation R_T is in kΩ, VREF is in volts and $F_{SW(nom)}$ is in kHz. This is also an empirical approximation and thus, there is no unit agreement. Assume for example, VREF = 5 V, R_T = 65 kΩ. Then the switching frequency $F_{SW(nom)}$ is going to be 92.6 kHz.

Equation 11 defines the nominal switching frequency of converter if the converter configured as a slave and the resistor R_T is connected between the RT pin and GND.

$$F_{SW(nom)} = \left(\frac{2.5 \times 10^3}{\left(\frac{R_T}{2.5\,V} + 1 \times \frac{k\Omega}{V} \right)} \right) kHz \tag{11}$$

In this equation the R_T is in kΩ, and $F_{SW(nom)}$ is in kHz. Notice that for VREF = 5 V, Equation 10 and Equation 11 yield the same results.

The plot in Figure 35 shows how $F_{SW(nom)}$ depends on the resistor R_T value when the VREF = 5 V. As it is seen from Equation 10 and Equation 11, the switching frequency $F_{SW(nom)}$ is set to the same value for either master or slave configuration provided the same resistor value R_T is used.

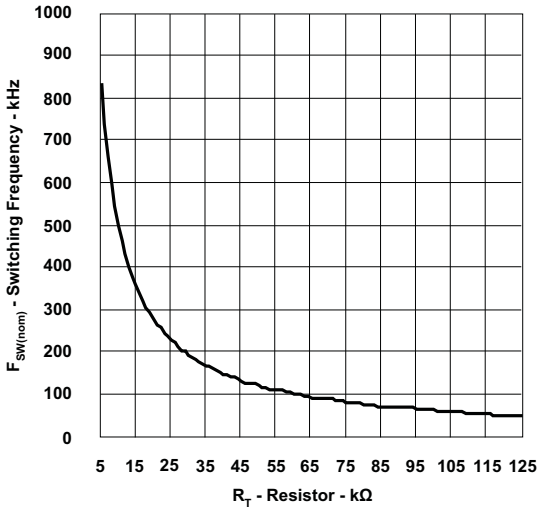

Figure 35. Converter Switching Frequency $F_{SW(nom)}$ Over resistor R_T Value

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Feature Description (continued)

7.3.11 Slope Compensation (R_{SUM})

Slope compensation is needed to prevent a sub-harmonic oscillation in a controller operating in peak current mode (PCM) control or during cycle-by-cycle current limit at duty cycles above 50% (some publications suggest it may happen at D < 50%). Slope compensation in the UCC28950 adds an additional ramp signal to the CS signal and is applied:

- To the PWM comparator in the case of peak current mode control.
- To the input of the cycle-by-cycle comparator.

At low duty cycles and light loads the slope compensation ramp reduces the noise sensitivity of Peak Current Mode control.

Placing a resistor from the R_{SUM} pin to ground allows the controller to operate in PCM control. Connecting a resistor from R_{SUM} to VREF switches the controller to voltage mode control (VMC) with the internal PWM ramp. In VMC the resistor at R_{SUM} provides CS signal slope compensation for operation in cycle-by-cycle current limit. That is, in VMC, the slope compensation is applied only to the cycle-by-cycle comparator while in PCM the slope compensation is applied to both the PWM and cycle-by-cycle current limit comparators. The operation logic of the slope compensation circuit is shown in Figure 36.

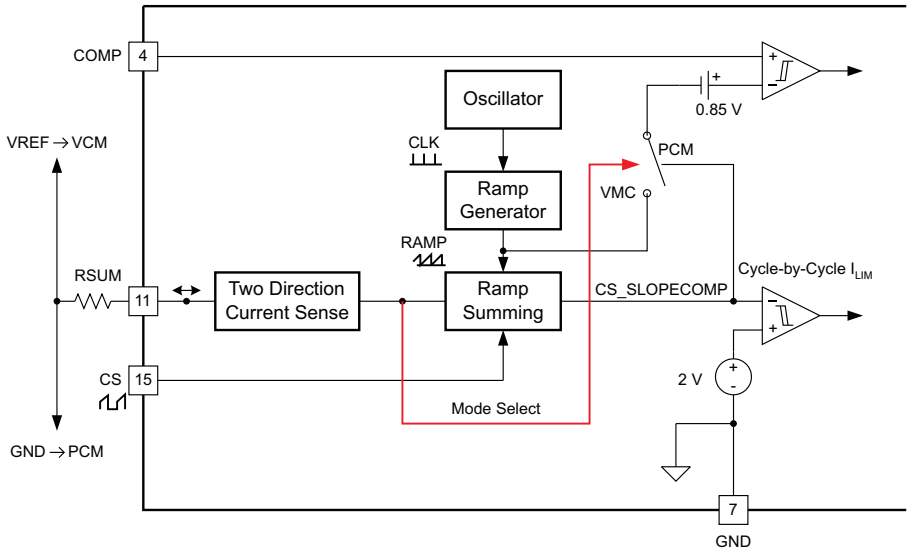

Figure 36. The Operation Logic of Slope Compensation Circuit

Too much slope compensation reduces the benefits of PCM control. In the case of cycle-by-cycle current limit, the average current limit becomes lower and this might reduce the start-up capability into large output capacitances.

The optimum compensation ramp varies, depending on duty cycle, L_{OUT} and L_{MAG}. A good starting point in selecting the amount of slope compensation is to set the slope compensation ramp to be half the inductor current ramp downslope (inductor current ramp during the off time). The inductor current ramp downslope – as seen at the CS pin input, and neglecting the effects of any filtering at the CS pin, will be:

$$m_0 = \frac{V_{OUT}}{L_{OUT}} \frac{R_S}{a1 \times CT_{RAT}} \quad (12)$$

Where, V_{OUT} is the converter's output voltage of the converter, L_{OUT} is the output inductor value, a1 is the transformer turns ratio (Np/Ns), CT_{RAT} is the current transformer ratio (Ip/Is, typically 100:1). Selection of L_{OUT}, a1 and CT_{RAT} are described elsewhere in this document. The total slope compensation is 0.5 m_0. Part of this ramp will be due to magnetizing current in the transformer, the rest is added by an appropriately chosen resistor from RSUM to ground.

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Feature Description (continued)

The slope of the additional ramp, me, added to the CS signal by placing a resistor from RSUM to ground is defined by Equation 13.

$$me = \left(\frac{2.5}{0.5 \times R_{SUM}} \right) \frac{V}{\mu s} \tag{13}$$

If the resistor from the RSUM pin is connected to the VREF pin, then the controller operates in voltage mode control, still having the slope compensation ramp added to the CS signal used for cycle-by-cycle current limit. In this case the slope is defined by Equation 14.

$$me = \left(\frac{(V_{REF} - 2.5\,V)}{0.5 \times R_{SUM}} \right) \frac{V}{\mu s} \tag{14}$$

In Equation 13 and Equation 14, VREF is in volts, R_{SUM} is in kΩ and me is in V/µs. These are empirically derived equations without units agreement. As an example, substituting VREF = 5V and R_{SUM} = 40 kΩ, yields the result 0.125 V/µs. The related plot of me as a function of R_{SUM} is shown in Figure 37, Because VREF = 5V, the plots generated from Equation 13 and Equation 14 coincide.

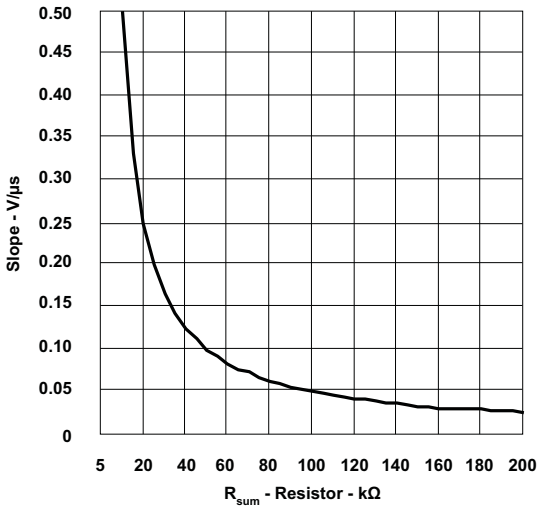

Figure 37. Slope of the Added Ramp Over Resistor R_{SUM}

NOTE

The recommended resistor range for R_{SUM} is 10 kΩ to 1 MΩ.

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Feature Description (continued)

7.3.12 Dynamic SR ON/OFF Control (DCM Mode)

The voltage at the DCM pin provided by the resistor divider R_{DCMHI} between VREF pin and DCM, and R_{DCM} from DCM pin to GND, sets the percentage of 2-V current limit threshold for the Current Sense pin, (CS). If the CS pin voltage falls below the DCM pin threshold voltage, then the controller initiates the light load power saving mode, and shuts down the synchronous rectifiers, OUTE and OUTF. If the CS pin voltage is higher than the DCM pin threshold voltage, then the controller runs in CCM mode. Connecting the DCM pin to VREF makes the controller run in DCM mode and shuts both Outputs OUTE and OUTF. Shorting the DCM pin to GND disables the DCM feature and the controller runs in CCM mode under all conditions.

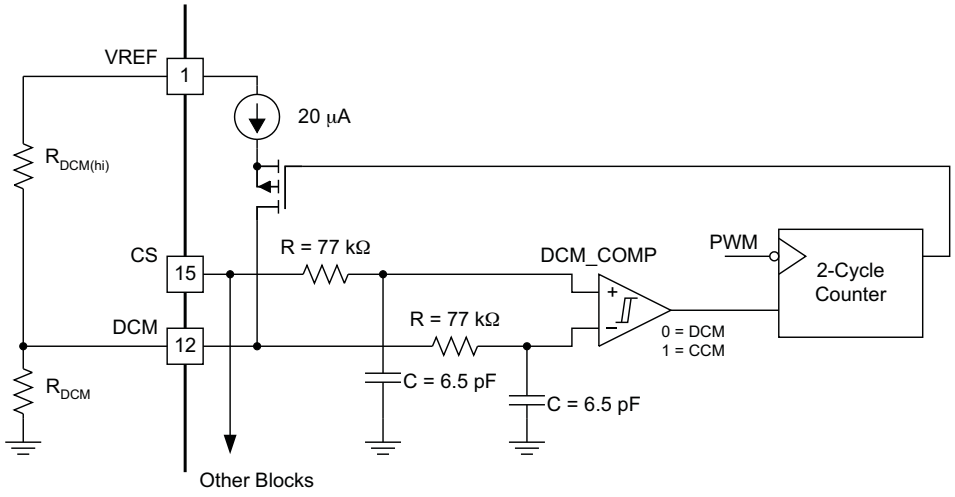

Figure 38. DCM Functional Block

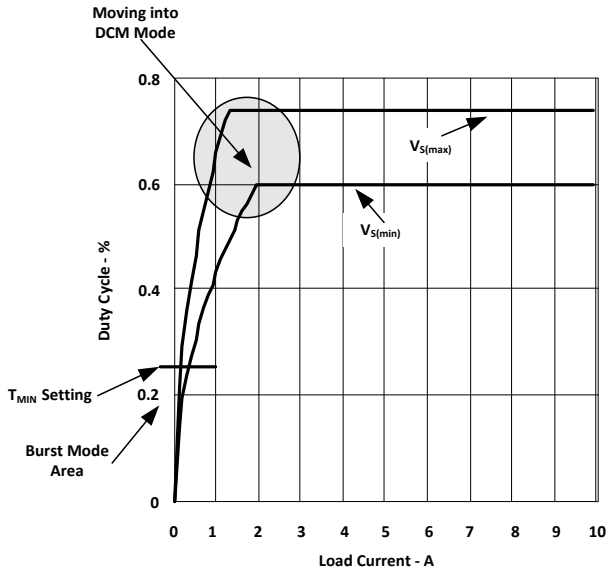

Figure 39. Duty Cycle Change Over Load Current Change

Feature Description (continued)

A nominal 20-µA switched current source is used to create hysteresis. The current source is active only when the system is in DCM Mode. Otherwise, it is inactive and does not affect the node voltage. Therefore, when in the DCM region, the DCM threshold is the voltage divider plus ΔV explained in Equation 15. When in the CCM region, the threshold is the voltage set by the resistor divider. When the CS pin reaches the threshold set on the DCM pin, the system waits to see two consecutive falling edge PWM cycles before switching from CCM to DCM and vice-versa. The magnitude of the hysteresis is a function of the external resistor divider impedance. The hysteresis can be calculated using the following Equation 15:

$$\Delta V = 2 \times 10^{-5} \frac{R_{DCMHI} \times R_{DCM}}{R_{DCMHI} + R_{DCM}} \quad (15)$$

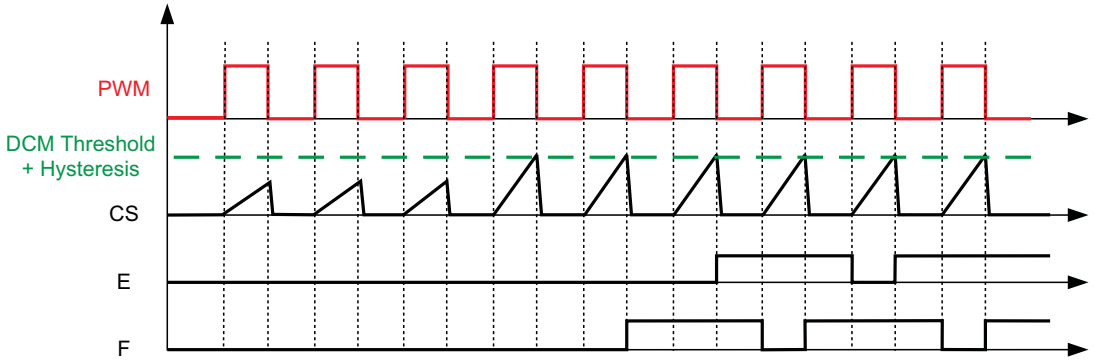

Figure 40. Moving from DCM to CCM Mode

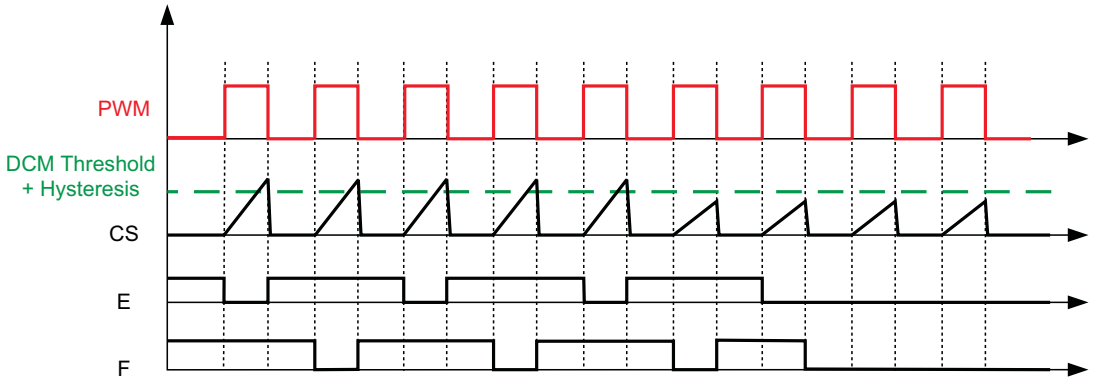

Figure 41. Moving from CCM to DCM Mode

DCM must be used in order to prevent reverse current in the output inductor which could cause the synchronous FETS to fail.

The controller must switch to DCM mode at a level where the output inductor current is positive. If the output inductor current is negative when the controller switches to DCM mode then the synchronous FETs will see a large V_{DS} spike and may fail.

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Feature Description (continued)

7.3.13 Current Sensing (CS)

The signal from the current sense pin is used for cycle-by-cycle current limit, peak-current mode control, light-load efficiency management and setting the delay time for outputs OUTA, OUTB, OUTC, OUTD and delay time for outputs OUTE, OUTF. Connect the current sense resistor R_{CS} between CS and GND. Depending on layout, to prevent a potential electrical noise interference, it is recommended to put a small R-C filter between the R_{CS} resistor and the CS pin.

7.3.14 Cycle-by-Cycle Current Limit Current Protection and Hiccup Mode

The cycle-by-cycle current limit provides peak current limiting on the primary side of the converter when the load current exceeds its predetermined threshold. For peak current mode control, a certain leading edge blanking time is needed to prevent the controller from false tripping due to switching noise. An internal 30-ns filter at the CS input is provided. The total propagation delay TCS from CS pin to outputs is 100 ns. An external RC filter is still needed if the power stage requires more blanking time. The 2.0-V ±3% cycle-by-cycle current limit threshold is optimized for efficient current transformer based sensing. The duration when a converter operates at cycle-by-cycle current limit depends on the value of soft-start capacitor and how severe the overcurrent condition is. This is achieved by the internal discharge current I_{DS} Equation 16 and Equation 17 at SS pin.

$$I_{DS(master)} = \left(-25 \times \left(1 - D\right) + 5\right)\mu A \tag{16}$$

$$I_{DS(slave)} = \left(-25 \times \left(1 - D\right)\right)\mu A \tag{17}$$

The soft-start capacitor value also determines the so called hiccup mode off-time duration. The behavior of the converter during different modes of operation, along with related soft start capacitor charge/discharge currents are shown in Figure 42.

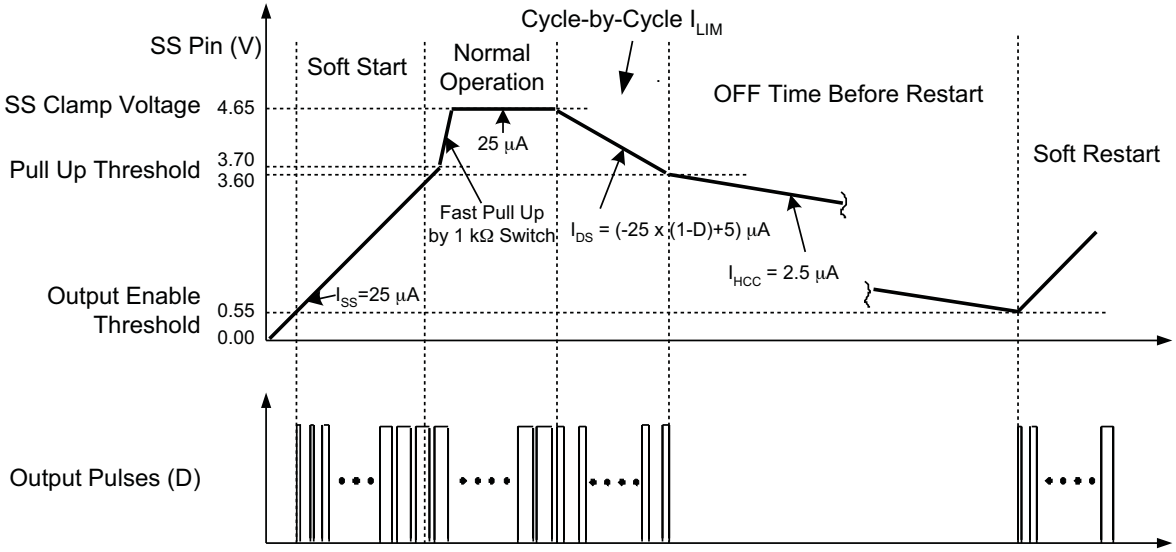

Figure 42. Timing Diagram of Soft-Start Voltage V_{SS}

Feature Description (continued)

The largest discharge current of 20 µA is when the duty cycle is close to zero. This current sets the shortest operation time during the cycle-by-cycle current limit which is defined as:

$$T_{CL(on_master)} = \frac{C_{SS} \times (4.65\,V - 3.7\,V)}{20\,\mu A} \quad (18)$$

$$T_{CL(on_slave)} = \frac{C_{SS} \times (4.65\,V - 3.7\,V)}{25\,\mu A} \quad (19)$$

Thus, if the soft-start capacitor C_{SS} = 100 nF is selected, then the $T_{CL(on)}$ time will be 5 ms.

To calculate the hiccup off time $T_{CL(off)}$ before the restart, the following Equation 20 or Equation 21 needs to be used:

$$T_{CL(off_master)} = \frac{C_{SS} \times (3.6\,V - 0.55\,V)}{2.5\,\mu A} \quad (20)$$

$$T_{CL(off_slave)} = \frac{C_{SS} \times (3.6\,V - 0.55\,V)}{4.9\,\mu A} \quad (21)$$

With the same soft start capacitor value 100 nF, the off time before the restart is going to be 122 ms. Notice, that if the overcurrent condition happens before the soft start capacitor voltage reaches the 3.7-V threshold during start up, the controller limits the current but the soft start capacitor continues to be charged. As soon as the 3.7-V threshold is reached, the soft-start voltage is quickly pulled up to the 4.65-V threshold by an internal 1-kΩ $R_{DS(on)}$ switch and the cycle-by-cycle current limit duration timing starts by discharging the soft start capacitor. Depending on specific design requirements, the user can override this default behavior by applying external charge or discharge currents to the soft start capacitor. The whole cycle-by-cycle current limit and hiccup operation is shown in Figure 42. In this example the cycle-by-cycle current limit lasts about 5 ms followed by 122 ms of off time.

Similarly to the overcurrent condition, the hiccup mode with the restart can be overridden by the user if a pullup resistor is connected between the SS and VREF pins. If the pullup current provided by the resistor exceeds 2.5 µA, then the controller remains in the latch off mode. In this case, an external soft-start capacitor value should be calculated with the additional pull-up current taken into account. The latch off mode can be reset externally if the soft-start capacitor is forcibly discharged below 0.55 V or the V_{DD} voltage is lowered below the UVLO threshold.

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Feature Description (continued)

7.3.15 Synchronization (SYNC)

The UCC28950 allows flexible configuration of converters operating in synchronized mode by connecting all SYNC pins together and by configuration of the controllers as master and/or slaves. The controller configured as master (resistor between RT and VREF) provides synchronization pulses at the SYNC pin with the frequency equal to 2X the converter frequency $F_{SW(nom)}$ and 0.5 duty cycle. The controller configured as a slave (resistor between RT and GND and 825-kΩ resistor between SS_EN pin to GND) does not generate the synchronization pulses. The Slave controller synchronizes its own clock to the falling edge of the synchronization signal thus operating 90° phase shifted versus the master converter's frequency $F_{SW(nom)}$.

The output inductor in a full bridge converter sees a switching frequency which is twice that seen by the transformer. In the case of the UCC28950 this means that the output inductor operates at 2 x $F_{SW(nom)}$. This means that the 90° phase shift between master and slave controllers gives a 180° phase shift between the currents in the output inductors and hence maximum ripple cancellation. For more information about synchronizing more than two UCC28950 devices, see *Synchronizing Three or More UCC28950 Phase-Shifted, Full-Bridge Controllers*, SLUA609.

If the synchronization feature is not used then the SYNC pin may be left floating, but connecting the SYNC pin to GND via a 10-kΩ resistor will reduce noise pickup and switching frequency jitter.

- If any converter is configured as a slave, the SYNC frequency must be greater than or equal to 1.8 times the converter frequency.
- Slave converter does not start until at least one synchronization pulse has been received.
- If any or all converters are configured as slaves, then each converter operates at its own frequency without synchronization after receiving at least one synchronization pulse. Thus, If there is an interruption of synchronization pulses at the slave converter, then the controller uses its own internal clock pulses to maintain operation based on the R_T value that is connected to GND in the slave converter.
- In master mode, SYNC pulses start after SS pin passes its enable threshold which is 0.55 V.
- Slave starts generating SS/EN voltage even though synchronization pulses have not been received.
- It is recommended that the SS on the master controller starts before the SS on the slave controller; therefore SS/EN pin on master converter must reach its enable threshold voltage before SS/EN on the slave converter starts for proper operation. On the same note, it's recommended that T_{MIN} resistors on both master and slave are set at the same value.

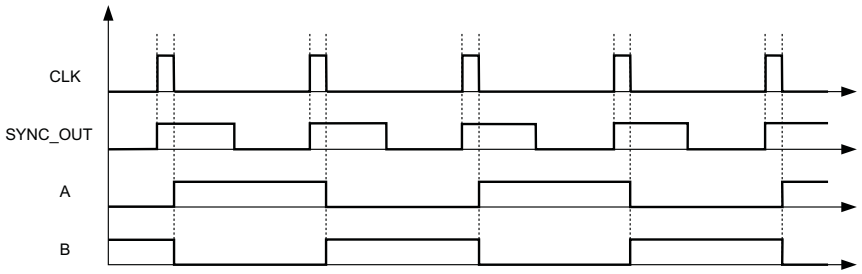

Figure 43. SYNC_OUT (Master Mode) Timing Diagram

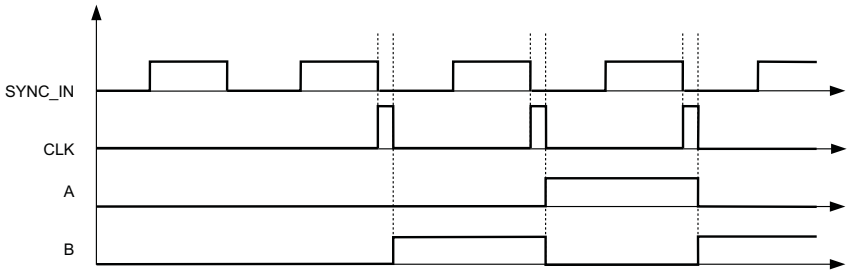

Figure 44. SYNC_IN (Slave Mode) Timing Diagram

Feature Description (continued)

7.3.16 Outputs (OUTA, OUTB, OUTC, OUTD, OUTE, OUTF)

- All MOSFET control outputs have 0.2-A drive capability.
- The control outputs are configured as P-MOS and N-MOS totem poles with typical $R_{DS(on)}$ 20 Ω and 10 Ω accordingly.
- The control outputs are capable of charging 100-pF capacitor within 12 ns and discharge within 8 ns.
- The amplitude of output control pulses is equal to V_{DD}.
- Control outputs are designed to be used with external gate MOSFET/IGBT drivers.
- The design is optimized to prevent the latch up of outputs and verified by extensive tests.

The UCC28950 device has outputs OUTA, OUTB driving the active leg, initiating the duty cycle leg of power MOSFETs in a phase-shifted full bridge power stage, and outputs OUTC, OUTD driving the passive leg, completing the duty cycle leg, as it is shown in the typical timing diagram in Figure 46. Outputs OUTE and OUTF are optimized to drive the synchronous rectifier MOSFETs (Figure 48). These outputs have 200-mA peak-current capabilities and are designed to drive relatively small capacitive loads like inputs of external MOSFET or IGBT drivers. Recommended load capacitance should not exceed 100 pF. The amplitude of the output signal is equal to the V_{DD} voltage.

7.3.17 Supply Voltage (VDD)

Connect this pin to a bias supply in the range from 8 V to 17 V. Place high quality, low ESR and ESL, at least 1-µF ceramic bypass capacitor C_{VDD} from this pin to GND. It is recommended to use a 10-Ω resistor in series from the bias supply to the VDD pin to form an RC filter with the C_{VDD} capacitor.

7.3.18 Ground (GND)

All signals are referenced to this node. It is recommended to have a separate quiet analog plane connected in one place to the power plane. The analog plane connects the components related to the pins VREF, EA+, EA-, COMP, SS/EN, DELAB, DELCD, DELEF, TMIN, RT, RSUM. The power plane connects the components related to the pins DCM, ADELEF, ADEL, CS, SYNC, OUTF, OUTE, OUTD, OUTC, OUTB, OUTA, and VDD. An example of layout and ground planes connection is shown in Figure 45.

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Feature Description (continued)

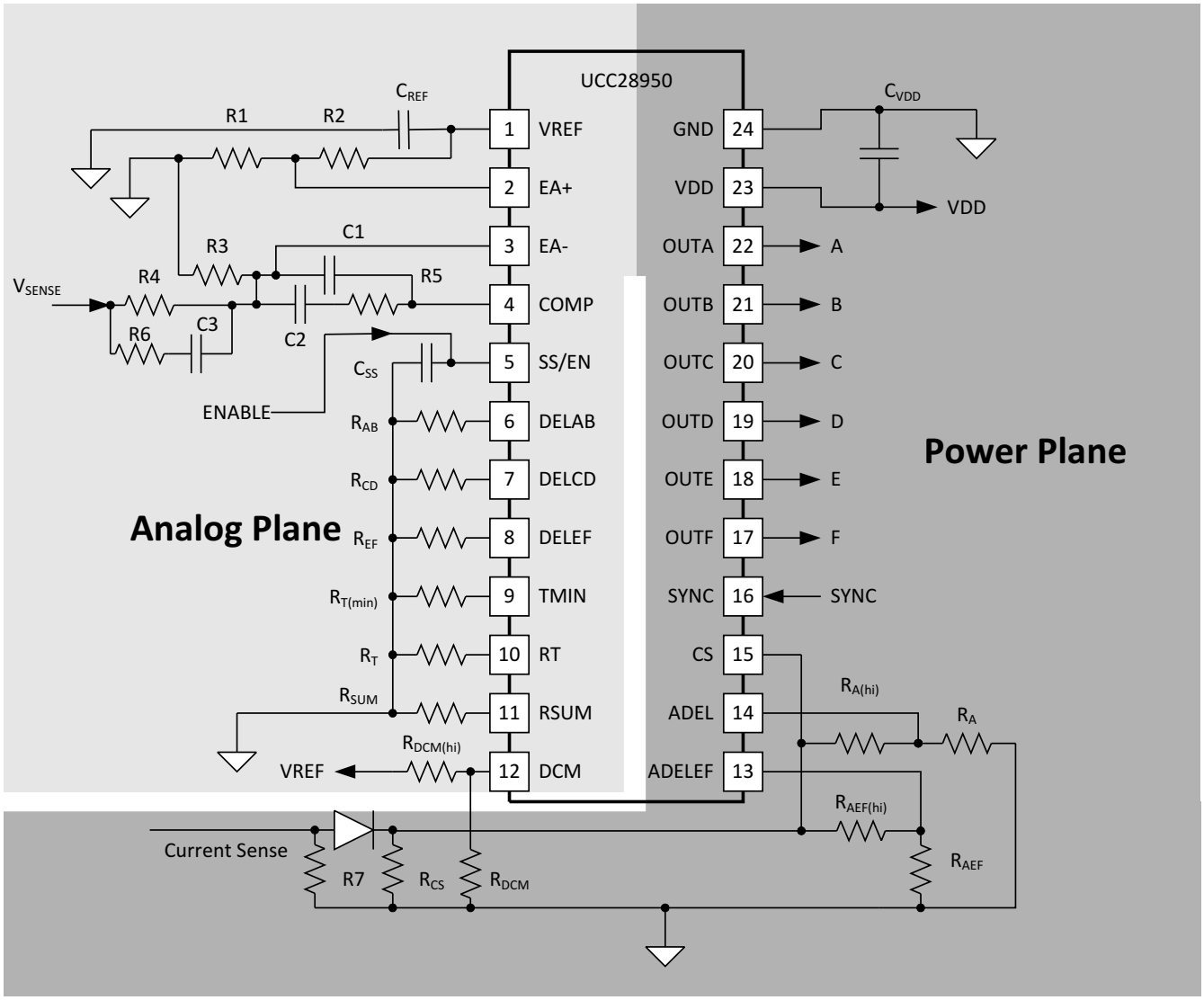

Figure 45. Layout Recommendation for Analog and Power Planes

7.4 Device Functional Modes

The UCC28950 has a number of operational modes. These modes are described in detail in *Feature Description*.

- Current mode(1). The UCC28950 device will operate in current mode control if the RSUM pin is connected to GND through a resistor (R_{SUM}) . The resistor sets the amount of slope compensation.
- Voltage mode(1). The UCC28950 device will operate in voltage mode control if the RSUM pin is connected to VREF through a resistor (R_{SUM}). The resistor value is chosen to give the correct amount of slope compensation for operation in current limit mode (cycle-by-cycle current limit).
- DCM mode. The UCC28950 device enters DCM mode if the signal at the CS pin falls below the level set by the resistor at the DCM pin. The SR drives (OUTE and OUTF) are turned off and secondary rectification is through the body diodes of the SRs.
- Burst mode. The UCC28950 device enters burst mode if the pulse width demanded by the feedback signal falls below the width set by the resistor at the TMIN pin.
- Master mode. This is the default operation mode of the UCC28950 device and is the mode used if there is only one UCC28950 device in the system. Connect the timing resistor (R_T) from the RT pin to VREF. In a system with more than one UCC28950, one will be configured as the master and the others as slaves(1).
- Slave mode. The slave controller will operate with a 90° phase shift relative to the Master (providing their SYNC pins are tied together). Connect the timing resistor (R_T) from the RT pin to GND and connect an 825 kΩ resistor from the SS/EN pin to GND(1).
- Synchronized mode. If a UC28950 is configured as a slave then its SYNC pin is used as an input. The slave will synchronize its internal oscillator at 90° to the signal at its SYNC pin. App note slua609 discusses how multiple Slave controllers may be synchronized to a single master oscillator.
- Hiccup mode. This mode provides overload protection to the power circuit. The UCC28950 device stops switching after a certain time in current limit. It starts again (soft start) after a delay time. The user can control the time spent in current limit before switching is stopped and the delay time before the soft start happens.
- Current-limit mode. The UCC28950 device will provide cycle-by-cycle current limiting if the signal at the CS pin reaches 2V.
- Latch-off mode. Connect a resistor between the SS pin and VREF. The UCC28950 will then latch off if the controller enters Current Limit mode. (1)

(1) Current mode control and voltage mode control are mutually exclusive as are master and slave modes.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The high efficiency of a phase-shifted full-bridge DC/DC converter using the UCC28950 is achieved by using synchronous rectification, a control algorithm providing ZVS condition over the entire load current range, accurate adaptive timing of the control signals between primary and secondary FETs and special operating modes at light load. A simplified electrical diagram of this converter is shown in Figure 48. The controller device is located on the secondary side of converter, although it could be located on primary side as well. The location on secondary side allows easy power system level communication and better handling of some transient conditions that require fast direct control of the synchronous rectifier MOSFETs. The power stage includes primary side MOSFETs, QA, QB, QC, QD and secondary side synchronous rectifier MOSFETs, QE and QF. For example, for the 12-V output converters in server power supplies use of the center-tapped rectifier scheme with L-C output filter is a popular choice.

To maintain high efficiency at different output power conditions, the converter operates in synchronous rectification mode at mid and high output power levels, transitioning to diode rectifier mode at light load and then into burst mode as the output power becomes even lower. All these transitions are based on current sensing on the primary side using a current sense transformer in this specific case.

The major waveforms of the phase-shifted converter during normal operation are shown in Figure 46. The upper six waveforms in Figure 46 show the output drive signals of the controller. In normal mode, the outputs OUTE and OUTF overlap during the part of the switching cycle when both rectifier MOSFETs are conducting and the windings of the power transformer are shorted. Current, I_{PR}, is the current flowing through the primary winding of the power transformer. The bottom four waveforms show the drain-source voltages of rectifier MOSFETs, V_{DS_QE} and V_{DS_QF}, the voltage at the output inductor, V L_{OUT}, and the current through the output inductor, I L_{OUT}. Proper timing between the primary switches and synchronous rectifier MOSFETs is critical to achieve highest efficiency and reliable operation in this mode. The controller device adjusts the turn OFF timing of the rectifier MOSFETs as a function of load current to ensure minimum conduction time and reverse recovery losses of their internal body diodes.

ZVS is an important feature of relatively high input voltage converters in reducing switching losses associated with the internal parasitic capacitances of power switches and transformers. The controller ensures ZVS conditions over the entire load current range by adjusting the delay time between the primary MOSFETs switching in the same leg in accordance to the load variation. The controller also limits the minimum ON-time pulse applied to the power transformer at light load, allowing the storage of sufficient energy in the inductive components of the power stage for the ZVS transition.

As the load current reduces from full load down to the no-load condition, the controller selects the most efficient power saving mode by moving from the normal operation mode to the discontinuous-current diode-rectification mode and, eventually, at very light-load and at no-load condition, to the burst mode. These modes and related output signals, OUTE, OUTF, driving the rectifier MOSFETs, are shown in Figure 47.

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Application Information (continued)

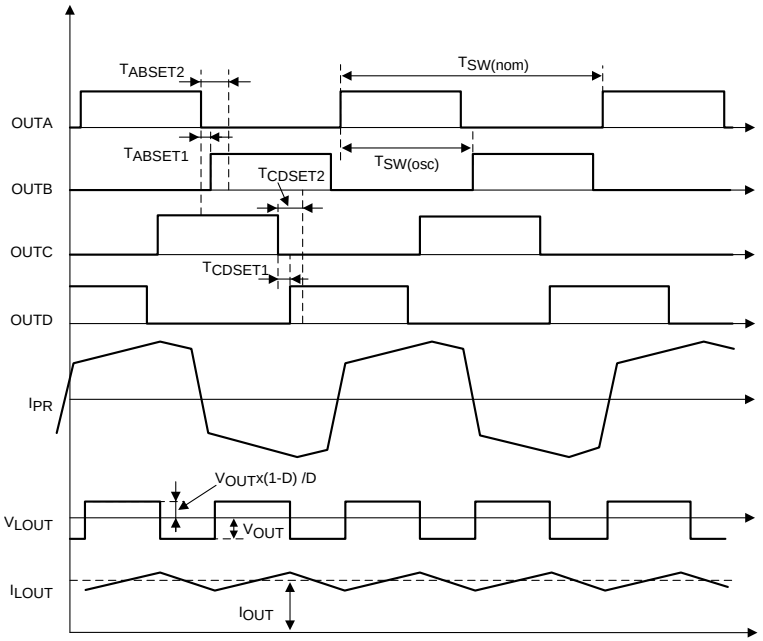

Figure 46. Major Waveforms of Phase-Shifted Converter

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Application Information (continued)

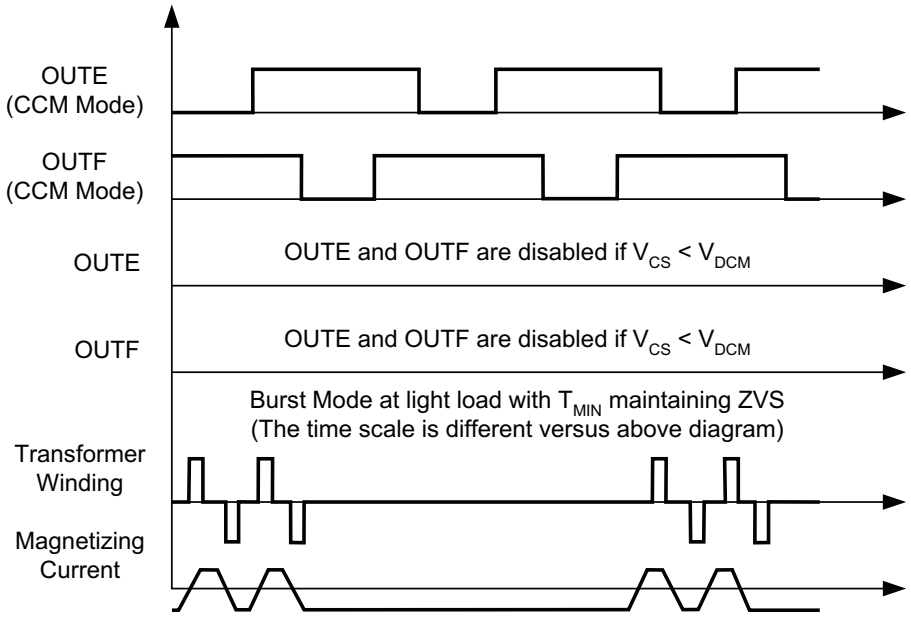

Figure 47. Major Waveforms During Transitions Between Different Operating Modes

It is necessary to prevent the reverse current flow through the synchronous rectifier MOSFETs and output inductor at light load, during parallel operation and at some transient conditions. Such reverse current results in circulating of some extra energy between the input voltage source and the load and, therefore, causes increased losses and reduced efficiency. Another negative effect of such reverse current is the loss of ZVS condition. The suggested control algorithm prevents reverse current flow, still maintaining most of the benefits of synchronous rectification by switching off the drive signals of rectifier MOSFETs in a predetermined way. At some pre-determined load current threshold, the controller disables outputs OUTE and OUTF by bringing them down to zero.

Synchronous rectification using MOSFETs requires some electrical energy to drive the MOSFETs. There is a condition below some light-load threshold when the MOSFET drive related losses exceed the saving provided by the synchronous rectification. At such light load, it is best to disable the drive circuit and use the internal body diodes of rectifier MOSFETs, or external diodes in parallel with the MOSFETs, for more efficient rectification. In most practical cases, the drive circuit needs to be disabled close to DCM mode. This mode of operation is called discontinuous-current diode-rectification mode.

At very light-load and no-load condition, the duty cycle, demanded by the closed-feedback-loop control circuit for output voltage regulation, can be very low. This could lead to the loss of ZVS condition and increased switching losses. To avoid the loss of ZVS, the control circuit limits the minimum ON-time pulse applied to the power transformer using resistor from TMIN pin to GND. Therefore, the only way to maintain regulation at very light load and at no-load condition is to skip some pulses. The controller skips pulses in a controllable manner to avoid saturation of the power transformer. Such operation is called burst mode. In Burst Mode there are always an even number of pulses applied to the power transformer before the skipping off time. Thus, the flux in the core of the power transformer always starts from the same point during the start of every burst of pulses.

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8.2 Typical Application

A typical application for the UCC28950 device is a controller for a phase-shifted full-bridge converter that converts a 390-V_{DC} input to a regulated 12-V output using synchronous rectifiers to achieve high efficiency.

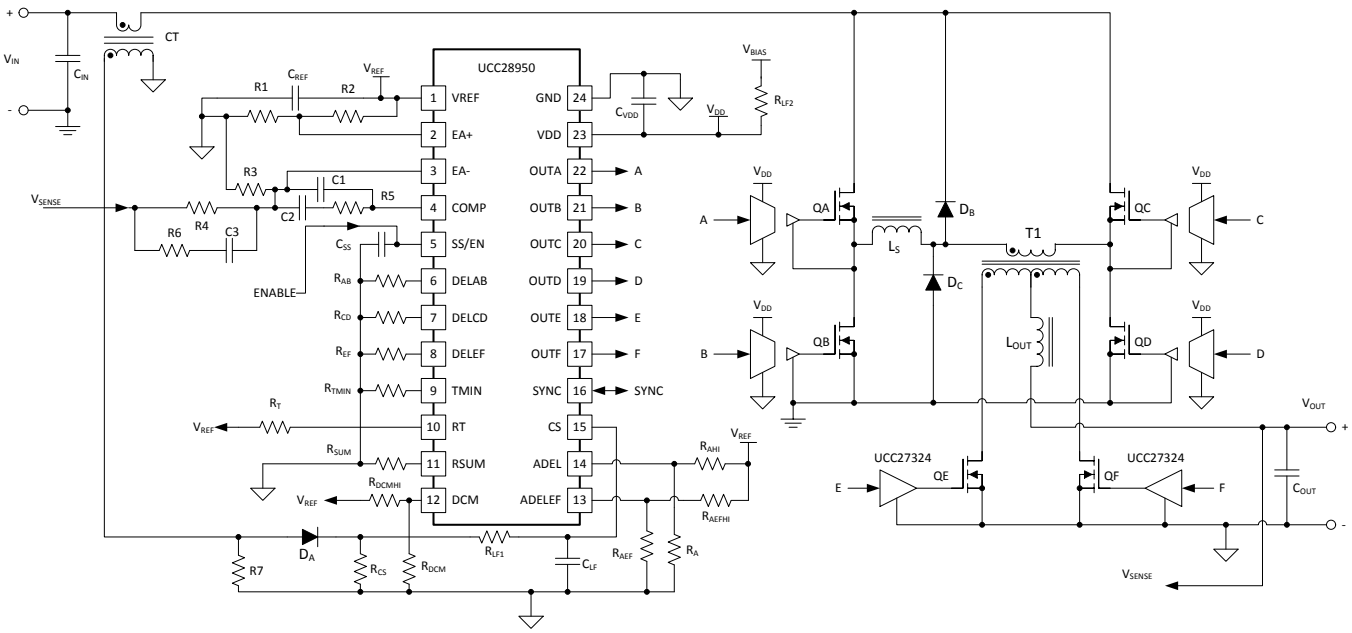

Figure 48. UCC28950 Typical Application

8.2.1 Design Requirements

Table 1 lists the requirements for this application.

Table 1. UCC28950 Typical Application Design Requirements

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	INPUT CHARACTERISTICS					
V_{IN}	DC input voltage range		370	390	410	V
$I_{IN(max)}$	Maximum input current	V_{IN}= 370 V_{DC} to 410 V_{DC}			2	A
	OUTPUT CHARACTERISTICS					
V_{OUT}	Output voltage	V_{IN}= 370 V_{DC} to 410 V_{DC}	11.4	12	12.6	V
I_{OUT}	Output current	V_{IN}= 370 V_{DC} to 410 V_{DC}			50	A
	Output voltage transient	90% load step		600		mV
P_{OUT}	Continuous output power	V_{IN}= 370 V_{DC} to 410 V_{DC}			600	W
	Load regulation	V_{IN} = 370 V_{DC} to 410 V_{DC}, I_{OUT}= 5 A to 50 A			140	mV
	Line regulation	V_{IN} = 370 V_{DC} to 410 V_{DC}, I_{OUT}= 5 A to 50 A			140	mV
	Output ripple voltage	V_{IN} = 370 V_{DC} to 410 V_{DC}, I_{OUT}= 5 A to 50 A			200	mV
	SYSTEM					
F_{SW}	Switching Frequency			100		kHz
	Full-load efficiency	V_{IN}= 370 V_{DC} to 410 V_{DC}, P_{OUT}= 500 W	93%	94%		

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8.2.2 Detailed Design Procedure

In high-power server applications to meet high-efficiency and green standards some power-supply designers have found it easier to use a phase-shifted, full-bridge converter. This is because the phase-shifted, full-bridge converter can obtain zero-voltage switching on the primary side of the converter, reducing switching losses, and EMI and increasing overall efficiency.

This is a review of the design of a 600-W, phase-shifted, full-bridge converter for one of these power systems using TI's UCC28950 device, which is based on typical values. In a production design, the values may need to be modified for worst-case conditions. TI has provided a *MathCAD Design Tool* and an *Excel Design Tool* to support the system designer. Both tools can be accessed in the Tools and Software tab of the UCC28950 product folder on TI.com, or can be downloaded through the following links: MathCAD Design Tool, Excel Design Tool.

NOTE

F_{SW} refers to the switching frequency applied to the power transformer. The output inductor experiences a switching frequency which is 2 x F_{SW} .

8.2.2.1 Power Loss Budget

To meet the efficiency goal a power loss budget needs to be set.

$$P_{BUDGET} = P_{OUT} \times \left(\frac{1-\eta}{\eta} \right) \approx 45.2\,W \tag{22}$$

8.2.2.2 Preliminary Transformer Calculations (T1)

Transformer turns ratio (a1):

$$a1 = \frac{N_P}{N_S} \tag{23}$$

Estimated FET voltage drop (V_{RDSON}):

$$V_{RDSON} = 0.3\,V \tag{24}$$

Select transformer turns based on 70% duty cycle (D_{MAX}) at minimum specified input voltage. This will give some room for dropout if a PFC front end is used.

$$a1 = \frac{N_P}{N_S} \tag{25}$$

$$a1 = \frac{(V_{INMIN} - 2 \times V_{RDSON}) \times D_{MAX}}{V_{OUT} + V_{RDSON}} \approx 21 \tag{26}$$

Turns ratio rounded to the nearest whole turn.

$$a1 = 21 \tag{27}$$

Calculated typical duty cycle (D_{TYP}) based on average input voltage.

$$D_{TYP} = \frac{(V_{OUT} + V_{RDSON}) \times a1}{(V_{IN} - 2 \times V_{RDSON})} \approx 0.66 \tag{28}$$

Output inductor peak-to-peak ripple current is set to 20% of the output current.

$$\Delta I_{LOUT} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = 10\,A \tag{29}$$

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Care must be taken in selecting the correct amount of magnetizing inductance (L_{MAG}). The following equations calculate the minimum magnetizing inductance of the primary of the transformer (T1) to ensure the converter operates in current-mode control. As L_{MAG} reduces, the increasing magnetizing current becomes an increasing proportion of the signal at the CS pin. If the magnetizing current increases enough it can swamp out the current sense signal across R_{CS} and the converter will operate increasingly as if it were in voltage mode control rather than current mode.

$$L_{MAG} \geq \frac{V_{IN} \times (1 - D_{TYP})}{\frac{\Delta I_{LOUT} \times 0.5}{a1} \times 2 \times F_{SW}} \approx 2.78\,mH \tag{30}$$

Figure 49 shows T1 primary current ($I_{PRIMARY}$) and synchronous rectifiers QE (I_{QE}) and QF (I_{QF}) currents with respect to the synchronous rectifier gate drive currents. Note that I_{QE} and I_{QF} are the same as the secondary winding currents of T1. Variable D is the duty cycle of the converter.

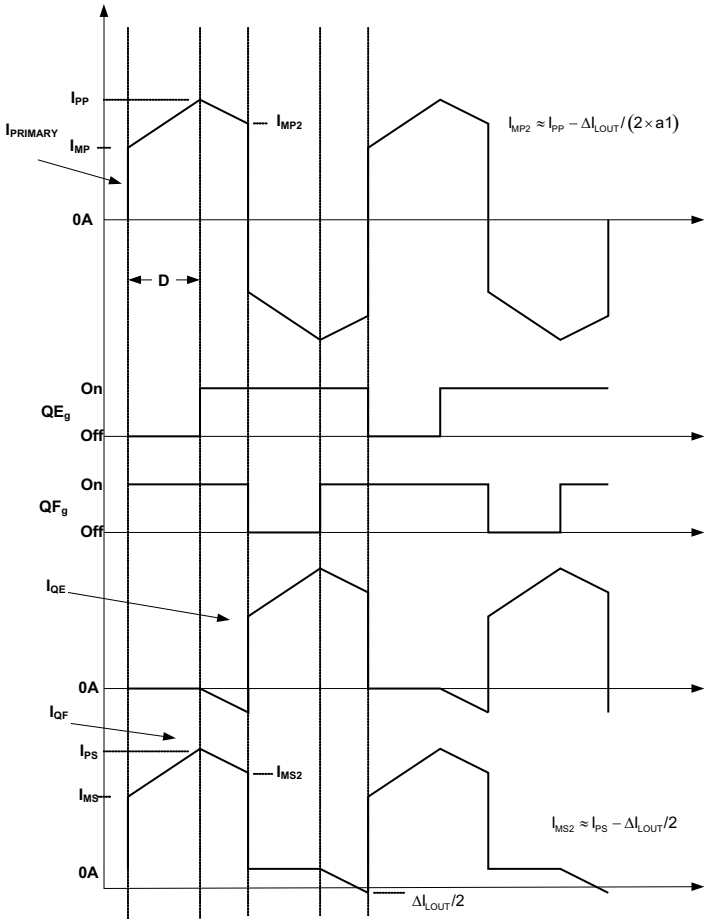

Figure 49. T1 Primary and QE and QF FET Currents

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Calculate T1 secondary RMS current (I_{SRMS}):

$$I_{PS} = \frac{P_{OUT}}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2} \approx 55\,A \quad (31)$$

$$I_{MS} = \frac{P_{OUT}}{V_{OUT}} - \frac{\Delta I_{LOUT}}{2} \approx 45\,A \quad (32)$$

$$I_{MS2} = I_{PS} - \frac{\Delta I_{LOUT}}{2} \approx 50\,A \quad (33)$$

Secondary RMS current (I_{SRMS1}) when energy is being delivered to the secondary:

$$I_{SRMS1} = \sqrt{\left(\frac{D_{MAX}}{2}\right)\left[I_{PS} \times I_{MS} + \frac{\left(I_{PS} - I_{MS}\right)^2}{3}\right]} \approx 29.6\,A \quad (34)$$

Secondary RMS current (I_{SRMS2}) when current is circulating through the transformer when QE and QF are both on.

$$I_{SRMS2} = \sqrt{\left(\frac{1 - D_{MAX}}{2}\right)\left[I_{PS} \times I_{MS2} + \frac{\left(I_{PS} - I_{MS2}\right)^2}{3}\right]} \approx 20.3\,A \quad (35)$$

Secondary RMS current (I_{SRMS3}) caused by the negative current in the opposing winding during freewheeling period, please refer to Figure 49.

$$I_{SRMS3} = \frac{\Delta I_{LOUT}}{2}\sqrt{\left(\frac{1 - D_{MAX}}{2 \times 3}\right)} \approx 1.1A \quad (36)$$

Total secondary RMS current (I_{SRMS}):

$$I_{SRMS} = \sqrt{I_{SRMS1}^{\ 2} + I_{SRMS2}^{\ 2} + I_{SRMS3}^{\ 2}} \approx 36.0\,A \quad (37)$$

Calculate T1 Primary RMS Current (I_{PRMS}):

$$\Delta I_{LMAG} = \frac{V_{INMIN} \times D_{MAX}}{L_{MAG} \times 2 \times F_{SW}} \approx 0.47\,A \quad (38)$$

$$I_{PP} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2}\right)\frac{1}{a1} + \Delta I_{LMAG} \approx 3.3\,A \quad (39)$$

$$I_{MP} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} - \frac{\Delta I_{LOUT}}{2}\right)\frac{1}{a1} + \Delta I_{LMAG} \approx 2.8A \quad (40)$$

$$I_{PRMS1} = \sqrt{\left(D_{MAX}\right)\left[I_{PP} \times I_{MP} + \frac{\left(I_{PP} - I_{MP}\right)^2}{3}\right]} \approx 2.5\,A \quad (41)$$

$$I_{MP2} = I_{PP} - \left(\frac{\Delta I_{LOUT}}{2}\right)\frac{1}{a1} \approx 3.0\,A \quad (42)$$

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T1 Primary RMS (I_{PRMS1}) current when energy is being delivered to the secondary.

$$I_{PRMS1} = \sqrt{(D_{MAX})\left[I_{PP} \times I_{MP} + \frac{(I_{PP} - I_{MP})^2}{3}\right]} \approx 2.5\,A \tag{43}$$

T1 Primary RMS (I_{PRMS2}) current when the converter is free wheeling.

$$I_{PRMS2} = \sqrt{(1 - D_{MAX})\left[I_{PP} \times I_{MP2} + \frac{(I_{PP} - I_{MP2})^2}{3}\right]} \approx 1.7\,A \tag{44}$$

Total T1 primary RMS current (I_{PRMS}):

$$I_{PRMS} = \sqrt{I_{PRMS1}^{\ 2} + I_{PRMS2}^{\ 2}} \approx 3.1A \tag{45}$$

For this design a Vitec™ transformer was selected part number 75PR8107 that had the following specifications.

$$a1 = 21 \tag{46}$$

$$L_{MAG} = 2.8\,mH \tag{47}$$

Measure leakage inductance on the Primary:

$$L_{LK} = 4\,\mu H \tag{48}$$

Transformer Primary DC resistance:

$$DCR_P = 0.215\,\Omega \tag{49}$$

Transformer Secondary DC resistance:

$$DCR_S = 0.58\,\Omega \tag{50}$$

Estimated transformer core losses (P_{T1}) are twice the copper loss.

NOTE

This is just an estimate and the total losses may vary based on magnetic design.

$$P_{T1} \approx 2 \times \left(I_{PRMS}^{\ 2} \times DCR_P + 2 \times I_{SRMS}^{\ 2} \times DCR_S\right) \approx 7.0\,W \tag{51}$$

Calculate remaining power budget:

$$P_{BUDGET} = P_{BUDGET} - P_{T1} \approx 38.1W \tag{52}$$

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8.2.2.3 QA, QB, QC, QD FET Selection

In this design to meet efficiency and voltage requirements 20 A, 650 V, CoolMOS FETs from Infineon are chosen for QA..QD.

FET drain to source on resistance:

$$R_{ds(on)QA} = 0.220\,\Omega \tag{53}$$

FET Specified C_{OSS}:

$$C_{OSS_QA_SPEC} = 780\,pF \tag{54}$$

Voltage across drain-to-source (V_{dsQA}) where C_{OSS} was measured, data sheet parameter:

$$V_{dsQA} = 25\,V \tag{55}$$

Calculate average C_{oss} [2]:

$$C_{OSS_QA_AVG} = C_{OSS_QA_SPEC}\sqrt{\frac{V_{dsQA}}{V_{INMAX}}} \approx 193\,pF \tag{56}$$

QA FET gate charge:

$$QA_g = 15\,nC \tag{57}$$

Voltage applied to FET gate to activate FET:

$$V_g = 12\,V \tag{58}$$

Calculate QA losses (P_{QA}) based on $R_{ds(on)QA}$ and gate charge (QA_g):

$$P_{QA} = I_{PRMS}{}^2 \times R_{DS(on)QA} + 2 \times QA_g \times V_g \times f_{SW} \approx 2.1W \tag{59}$$

Recalculate power budget:

$$P_{BUDGET} = P_{BUDGET} - 4 \times P_{QA} \approx 29.7\,W \tag{60}$$

8.2.2.4 Selecting L_S

Calculating the value of the shim inductor (L_S) is based on the amount of energy required to achieve zero voltage switching. This inductor needs to able to deplete the energy from the parasitic capacitance at the switch node. The following equation selects L_S to achieve ZVS at 100% load down to 50% load based on the primary FET's average total C_{OSS} at the switch node.

NOTE

The actual parasitic capacitance at the switched node may differ from the estimate and L_S may have to be adjusted accordingly.

$$L_S \geq \left(2 \times C_{OSS_QA_AVG}\right) \frac{V_{INMAX}^{\ 2}}{\left(\frac{I_{PP}}{2} - \frac{\Delta I_{LOUT}}{2 \times a1}\right)^2} - L_{LK} \approx 26\,\mu H \tag{61}$$

For this design a 26-µH Vitec inductor was chosen for L_S, part number 60PR964. The shim inductor had the following specifications.

$$L_S = 26\,\mu H \tag{62}$$

L_S DC Resistance:

$$DCR_{LS} = 27\,m\Omega \tag{63}$$

Estimate L_S power loss (P_{LS}) and readjust remaining power budget:

$$P_{LS} = 2 \times I_{PRMS}^{\ 2} \times DCR_{LS} \approx 0.5\,W \tag{64}$$

$$P_{BUDGET} = P_{BUDGET} - P_{LS} \approx 29.2\,W \tag{65}$$

8.2.2.5 Selecting Diodes D_B and D_C

There is a potential for high voltage ringing on the secondary rectifiers, caused by the difference in current between the transformer and the shim inductor when the transformer comes out of freewheeling. Diodes D_B and D_C provide a path for this current and prevent any ringing by clamping the transformer primary to the primary side power rails. Normally these diodes do not dissipate much power but they should be sized to carry the full primary current. The worse case power dissipated in these diodes is:

$$P = 0.5 \times L_S \times I^2_{PRMS} \times F_{SW} \tag{66}$$

The diodes should be ultra-fast types and rated for the input voltage of the converter – V_{IN} (410 VDC in this case).

A MURS360 part is suitable at this power level.

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8.2.2.6 Output Inductor Selection (L_{OUT})

Inductor L_{OUT} is designed for 20% inductor ripple current (ΔI_{LOUT}):

$$\Delta I_{LOUT} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = \frac{600\,W \times 0.2}{12\,V} \approx 10\,A \quad (67)$$

$$L_{OUT} = \frac{V_{OUT} \times (1 - D_{TYP})}{\Delta I_{LOUT} \times 2 \times f_{SW}} \approx 2\,\mu H \quad (68)$$

Calculate output inductor RMS current (I_{LOUT_RMS}):

$$I_{LOUT_RMS} = \sqrt{\left(\frac{P_{OUT}}{V_{OUT}}\right)^2 + \left(\frac{\Delta I_{LOUT}}{\sqrt{3}}\right)^2} = 50.3\,A \quad (69)$$

A 2-µH inductor from Vitec Electronics Corporation, part number 75PR8108, is suitable for this design. The inductor has the following specifications.

$$L_{OUT} = 2\,\mu H \quad (70)$$

Output inductor DC resistance:

$$DCR_{LOUT} = 750\,\mu\Omega \quad (71)$$

Estimate output inductor losses (P_{LOUT}) and recalculate power budget. Note P_{LOUT} is an estimate of inductor losses that is twice the copper loss. Note this may vary based on magnetic manufactures. It is advisable to double check the magnetic loss with the magnetic manufacture.

$$P_{LOUT} = 2 \times I_{LOUT_RMS}^2 \times DCR_{LOUT} \approx 3.8\,W \quad (72)$$

$$P_{BUDGET} = P_{BUDGET} - P_{LOUT} \approx 25.4\,W \quad (73)$$

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8.2.2.7 Output Capacitance (C_{OUT})

The output capacitor is selected based on holdup and transient (V_{TRAN}) load requirements.

Time it takes L_{OUT} to change 90% of its full load current:

$$t_{HU} = \frac{\frac{L_{OUT} \times P_{OUT} \times 0.9}{V_{OUT}}}{V_{OUT}} = 7.5\,\mu s \tag{74}$$

During load transients most of the current will immediately go through the capacitors equivalent series resistance (ESR_{COUT}). The following equations are used to select ESR_{COUT} and C_{OUT} based on a 90% load step in current. The ESR is selected for 90% of the allowable transient voltage (V_{TRAN}), while the output capacitance (C_{OUT}) is selected for 10% of V_{TRAN}.

$$ESR_{COUT} \le \frac{V_{TRAN} \times 0.9}{\frac{P_{OUT} \times 0.9}{V_{OUT}}} = 12\,m\Omega \tag{75}$$

$$C_{OUT} \ge \frac{\frac{P_{OUT} \times 0.9 \times t_{HU}}{V_{OUT}}}{V_{TRAN} \times 0.1} \approx 5.6\,mF \tag{76}$$

Before selecting the output capacitor, the output capacitor RMS current (I_{COUT_RMS}) must be calculated.

$$I_{COUT_RMS} = \frac{\Delta I_{LOUT}}{\sqrt{3}} \approx 5.8\,A \tag{77}$$

To meet the design requirements five 1500-µF, aluminum electrolytic capacitors are chosen for the design from United Chemi-Con™, part number EKY-160ELL152MJ30S. These capacitors have an ESR of 31 mΩ.

Number of output capacitors:

$$n = 5 \tag{78}$$

Total output capacitance:

$$C_{OUT} = 1500\,\mu F \times n \approx 7500\,\mu F \tag{79}$$

Effective output capacitance ESR:

$$ESR_{COUT} = \frac{31\,m\Omega}{n} = 6.2\,m\Omega \tag{80}$$

Calculate output capacitor loss (P_{COUT}):

$$P_{COUT} = I_{COUT_RMS}{}^2 \times ESR_{COUT} \approx 0.21\,W \tag{81}$$

Recalculate remaining Power Budget:

$$P_{BUDGET} = P_{BUDGET} - P_{COUT} \approx 25.2\,W \tag{82}$$

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8.2.2.8 Select FETs QE and QF

Selecting FETs for a design is an iterative process. To meet the power requirements of this design, we select 75-V, 120-A FETs, from Fairchild, part number FDP032N08. These FETs have the following characteristics.

$$QE_g = 152\,nC \tag{83}$$

$$R_{ds(on)QE} = 3.2\,m\Omega \tag{84}$$

Calculate average FET C_{OSS} ($C_{OSS_QE_AVG}$) based on the data sheet parameters for C_{OSS} (C_{OSS_SPEC}), and drain to source voltage where C_{OSS_SPEC} was measured (V_{ds_spec}), and the maximum drain to source voltage in the design (V_{dsQE}) that will be applied to the FET in the application.

Voltage across FET QE and QF when they are off:

$$V_{dsQE} = \frac{V_{INMAX}}{a1} \approx 19.5\,V \tag{85}$$

Voltage where FET C_{OSS} is specified and tested in the FET data sheet:

$$V_{ds_spec} = 25\,V \tag{86}$$

Specified output capacitance from FET data sheet:

$$C_{OSS_SPEC} = 1810\,pF \tag{87}$$

Average QE and QF C_{OSS} [2]:

$$C_{OSS_QE_AVG} = C_{OSS_SPEC}\sqrt{\frac{V_{dsQE}}{V_{ds_spec}}} \approx 1.6\,nF \tag{88}$$

QE and QF RMS current:

$$I_{QE_RMS} = I_{SRMS} = 36.0\,A \tag{89}$$

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To estimate FET switching loss the V_g vs. Q_g curve from the FET data sheet needs to be studied. First the gate charge at the beginning of the miller plateau needs to be determined (QE_{MILLER_MIN}) and the gate charge at the end of the miller plateau (QE_{MILLER_MAX}) for the given V_{DS}.

Maximum gate charge at the end of the miller plateau:

$$QE_{MILLER_MAX} \approx 100\,nC \tag{90}$$

Minimum gate charge at the beginning of the miller plateau:

$$QE_{MILLER_MIN} \approx 52\,nC \tag{91}$$

NOTE

The FETs in this design are driven with a UCC27324 Gate Driver IC, setup to drive 4-A (I_P) of gate drive current.

$$I_P \approx 4\,A \tag{92}$$

Estimated FET V_{ds} rise and fall time:

$$t_r \approx t_f = \frac{100nC - 52nC}{\frac{I_P}{2}} = \frac{48nC}{\frac{4A}{2}} \approx 24\,ns \tag{93}$$

Estimate QE and QF FET Losses (P_{QE}):

$$P_{QE} = I_{QE_RMS}{}^2 \times R_{ds(on)QE} + \frac{P_{OUT}}{V_{OUT}} \times V_{dsQE}\left(t_r + t_f\right) f_{SW} + 2 \times C_{OSS_QE_AVG} \times V_{dsQE}{}^2 f_{SW} + 2 \times Q_{gQE} \times V_{gQE} f_{SW} \tag{94}$$

$$P_{QE} \approx 9.3\,W \tag{95}$$

Recalculate the power budget.

$$P_{BUDGET} = P_{BUDGET} - 2 \times P_{QE} \approx 6.5\,W \tag{96}$$

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8.2.2.9 Input Capacitance (C_{IN})

The input voltage in this design is 390 V_{DC}, which is generally fed by the output of a PFC boost pre-regulator. The input capacitance is generally selected based on holdup and ripple requirements.

NOTE

The delay time needed to achieve ZVS can act as a duty cycle clamp (D_{CLAMP}).

Calculate tank frequency:

$$f_R = \frac{1}{2\pi\sqrt{L_S \times (2 \times C_{OSS_QA_AVG})}} \tag{97}$$

Estimated delay time:

$$t_{DELAY} = \frac{2}{f_R \times 4} \approx 314\,ns \tag{98}$$

Effective duty cycle clamp (D_{CLAMP}):

$$D_{CLAMP} = \left(\frac{1}{2 \times f_{SW}} - t_{DELAY} \right) \times 2 \times f_{SW} = 94\% \tag{99}$$

V_{DROP} is the minimum input voltage where the converter can still maintain output regulation. The converter's input voltage would only drop down this low during a brownout or line-drop condition if this converter was following a PFC pre-regulator.

$$V_{DROP} = \left(\frac{2 \times D_{CLAMP} \times V_{RDSON} + a1 \times (V_{OUT} + V_{RDSON})}{D_{CLAMP}} \right) = 276.2\,V \tag{100}$$

C_{IN} was calculated based on one line cycle of holdup:

$$C_{IN} \geq \frac{2 \times P_{OUT} \times \frac{1}{60\,Hz}}{\left(V_{IN}^{\ 2} - V_{DROP}^{\ 2}\right)} \approx 364\,\mu F \tag{101}$$

Calculate high frequency input capacitor RMS current (I_{CINRMS}).

$$I_{CINRMS} = \sqrt{I_{PRMS1}^{\ 2} - \left(\frac{P_{OUT}}{V_{INMIN} \times a1} \right)^2} = 1.8\,A \tag{102}$$

To meet the input capacitance and RMS current requirements for this design a 330-µF capacitor was chosen from Panasonic part number EETHC2W331EA.

$$C_{IN} = 330\,\mu F \tag{103}$$

This capacitor has a high frequency (ESR_{CIN}) of 150 mΩ, measured with an impedance analyzer at 200 kHz.

$$ESR_{CIN} = 0.150\,\Omega \tag{104}$$

Estimate C_{IN} power dissipation (P_{CIN}):

$$P_{CIN} = I_{CINRMS}^{\ 2} \times ESR_{CIN} = 0.5\,W \tag{105}$$

Recalculate remaining power budget:

$$P_{BUDGET} = P_{BUDGET} - P_{CIN} \approx 6.0\,W \tag{106}$$

There is roughly 6.0 W left in the power budget left for the current sensing network, and biasing the control device and all resistors supporting the control device.

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8.2.2.10 Current Sense Network (CT, R_{CS}, R7, D_A)

The CT chosen for this design has a turns ratio (CT_{RAT}) of 100:1

$$CT_{RAT} = \frac{I_P}{I_S} = 100 \tag{107}$$

Calculate nominal peak current (I_{P1}) at V_{INMIN}:

Peak primary current:

$$I_{P1} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2} \right) \frac{1}{a1} + \frac{V_{INMIN} \times D_{MAX}}{L_{MAG} \times 2 \times F_{SW}} \approx 3.3\,A \tag{108}$$

The CS pin voltage where peak current limit will trip.

$$V_P = 2\,V \tag{109}$$

Calculate current sense resistor (R_{CS}) and leave 300mV for slope compensation. Include a 1.1 factor for margin:

$$R_{CS} = \frac{V_P - 0.3\,V}{\frac{I_{P1}}{CT_{RAT}} \times 1.1} \approx 47\,\Omega \tag{110}$$

Select a standard resistor for R_{CS}:

$$R_{CS} = 47\,\Omega \tag{111}$$

Estimate power loss for R_{CS}:

$$P_{RCS} = \left(\frac{I_{PRMS1}}{CT_{RAT}} \right)^2 \times R_{CS} \approx 0.03\,W \tag{112}$$

Calculate maximum reverse voltage (V_{DA}) on D_A:

$$V_{DA} = V_P \frac{D_{CLAMP}}{1 - D_{CLAMP}} \approx 29.8\,V \tag{113}$$

Estimate D_A power loss (P_{DA}):

$$P_{DA} = \frac{P_{OUT} \times 0.6\,V}{V_{INMIN} \times \eta \times CT_{RAT}} \approx 0.01W \tag{114}$$

Calculate reset resistor R7:

Resistor R7 is used to reset the current sense transformer CT.

$$R7 = 100 \times R_{CS} = 4.7\,k\Omega \tag{115}$$

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Resistor R_{LF1} and capacitor C_{LF} form a low pass filter for the current sense signal (Pin 15). For this design we chose the following values. This filter has a low frequency pole (f_{LFP}) at 482 kHz. This should work for most applications but may be adjusted to suit individual layouts and EMI present in the design.

$$R_{LF1} = 1k\Omega \tag{116}$$

$$C_{LF} = 330pF \tag{117}$$

$$f_{LFP} = \frac{1}{2\pi f \times R_{LF1} \times C_{LF}} = 482kHz \tag{118}$$

The UCC28950 VREF output (Pin 1) needs a high frequency bypass capacitor to filter out high frequency noise. This pin needs at least 1 µF of high frequency bypass capacitance (C_{REF}).

$$C_{REF} = 1\mu F \tag{119}$$

The voltage amplifier reference voltage (Pin 2, EA +) can be set with a voltage divider (R1, R2), for this design example, the error amplifier reference voltage (V1) will be set to 2.5 V. Select a standard resistor value for R1 and then calculate resistor value R2.

UCC28950 reference voltage:

$$V_{REF} = 5V \tag{120}$$

Set voltage amplifier reference voltage:

$$V1 = 2.5V \tag{121}$$

$$R1 = 2.37k\Omega \tag{122}$$

$$R2 = \frac{R1 \times (V_{REF} - V1)}{V1} = 2.37k\Omega \tag{123}$$

Voltage divider formed by resistor R3 and R4 are chosen to set the DC output voltage (V_{OUT}) at Pin 3 (EA-).

Select a standard resistor for R3:

$$R3 = 2.37k\Omega \tag{124}$$

Calculate R4:

$$R4 = \frac{R3 \times (V_{OUT} - V1)}{V1} \approx 9k\Omega \tag{125}$$

Then choose a standard resistor for R4:

$$R4 = \frac{R3 \times (V_{OUT} - V1)}{V1} \approx 9.09k\Omega \tag{126}$$

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8.2.2.10.1 Voltage Loop Compensation Recommendation

For best results in the voltage loop, TI recommends using a Type 2 or Type 3 compensation network (Figure 50). A Type 2 compensation network does not require passive components C_{Z2} and R_{Z2}. Type 1 compensation is not versatile enough for a phase shifted full bridge. When evaluating the COMP for best results, TI recommends placing a 1-kΩ resistor between the socpe probe and the COMP pin of the UCC28950.

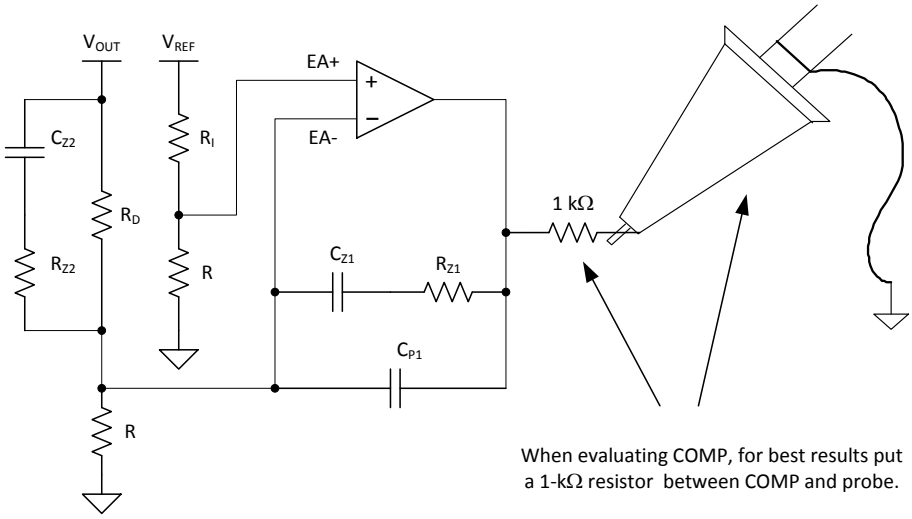

Figure 50. Type 3 Compensation Evaluation

Compensating the feedback loop can be accomplished by properly selecting the feedback components (R5, C1 and C2). These components are placed as close as possible to pin 3 and 4 of the UCC28950. A Type 2 compensation network is designed in this example.

Calculate load impedance at 10% load (R_{LOAD}):

$$R_{LOAD} = \frac{V_{OUT}^{2}}{P_{OUT} \times 0.1} = 2.4\,\Omega \tag{127}$$

Approximation of control to output transfer function ($G_{CO}(f)$) as a function of frequency:

$$G_{CO}(f) \approx \frac{\Delta V_{OUT}}{\Delta V_C} = a1 \times CT_{RAT} \times \frac{R_{LOAD}}{R_{CS}} \times \left(\frac{1 + 2\pi j \times f \times ESR_{COUT} \times C_{OUT}}{1 + 2\pi j \times f \times R_{LOAD} \times C_{OUT}} \right) \times \frac{1}{1 + \frac{S(f)}{2\pi \times f_{PP}} + \left(\frac{S(f)}{2\pi \times f_{PP}} \right)^2} \tag{128}$$

Double pole frequency of $G_{CO}(f)$:

$$f_{PP} \approx \frac{F_{SW}}{2} = 50\,kHz \tag{129}$$

Angular velocity:

$$S(f) = 2\pi \times j \times f \tag{130}$$

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Compensate the voltage loop with type 2 feedback network. The following transfer function is the compensation gain as a function of frequency ($G_C(f)$).

$$G_C(f) = \frac{\Delta V_C}{\Delta V_{OUT}} = \frac{2\pi j \times f \times R5 \times C2 + 1}{2\pi j \times f \times (C2 + C1) R4 \left(\frac{2\pi j \times f \times C2 \times C1 \times R5}{C2 + C1} + 1 \right)} \quad (131)$$

Calculate voltage loop feedback resistor (R5) based on crossing the voltage loop (f_C) over at a 10^{th} of the double pole frequency (f_{PP}).

$$f_C = \frac{f_{PP}}{10} = 5\,kHz \quad (132)$$

$$R5 = \frac{R4}{G_{CO}\left(\frac{f_{PP}}{10}\right)} \approx 27.9\,k\Omega \quad (133)$$

Select a standard resistor for R5.

$$R5 \approx 27.4\,k\Omega \quad (134)$$

Calculate the feedback capacitor (C2) to give added phase at crossover.

$$C2 = \frac{1}{2 \times \pi \times R5 \times \frac{f_C}{5}} \approx 5.8\,nF \quad (135)$$

Select a standard capacitance value for the design.

$$C2 = 5.6\,nF \quad (136)$$

Put a pole at two times f_C.

$$C1 = \frac{1}{2 \times \pi \times R5 \times f_C \times 2} \approx 580\,pF \quad (137)$$

Select a standard capacitance value for the design.

$$C1 = 560\,pF \quad (138)$$

Loop gain as a function of frequency ($T_V(f)$) in dB.

$$T_V dB(f) = 20 \log\left(\left|G_C(f) \times G_{CO}(f)\right|\right) \quad (139)$$

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Plot theoretical loop gain and phase to graphically check for loop stability (Figure 51). The theoretical loop gain crosses over at roughly 3.7 kHz with a phase margin of greater than 90 degrees.

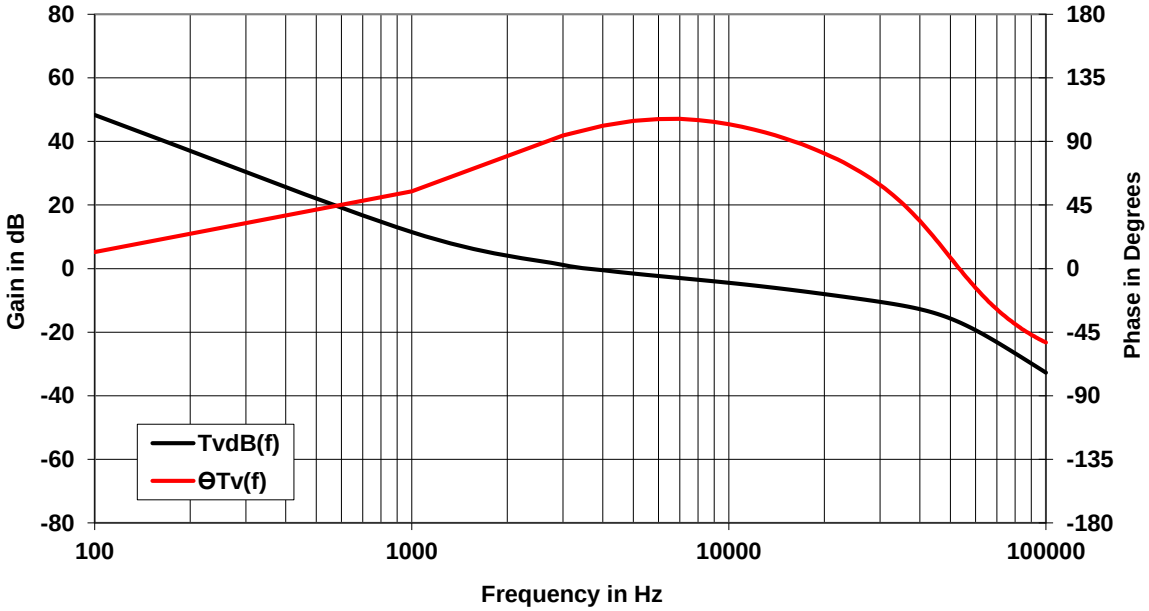

Figure 51. Loop Gain and Phase vs Frequency

NOTE

TI recommends checking your loop stability of your final design with transient testing and/or a network analyzer and adjust the compensation ($G_C(f)$) feedback as necessary.

$$L_{MAG} \geq \frac{V_{IN} \times (1 - D_{TYP})}{\frac{\Delta I_{LOUT} \times 0.5}{a1} \times 2 \times F_{SW}} \approx 2.78\,mH \quad (140)$$

where

- Loop Gain ($T_V dB(f)$), Loop Phase ($\Phi T_V(f)$)

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To limit over shoot during power up the UCC28950 has a soft-start function (SS, Pin 5) which in this application was set for a soft start time of 15 ms (t_{SS}).

$$t_{ss} = 15\,ms \tag{141}$$

$$C_{SS} = \frac{t_{SS} \times 25\,\mu A}{V1 + 0.55} \approx 123\,nF \tag{142}$$

Select a standard capacitor for the design.

$$C_{SS} = 150\,nF \tag{143}$$

This application note presents a fixed delay approach to achieving ZVS from 100% load down to 50% load. Adaptive delays can be generated by connecting the ADEL and ADELEF pins to the CS pin as shown in Figure 52.

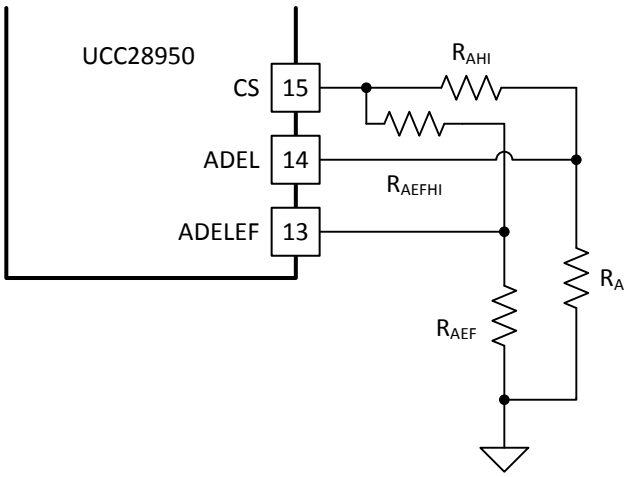

Figure 52. UCC28950 Adaptive Delays

When the converter is operating below 50% load the converter will be operating in valley switching. In order to achieve zero voltage switching on switch node of QB_d, the turn-on (t_{ABSET}) delays of FETs QA and QB need to be initially set based on the interaction of L_S and the theoretical switch node capacitance. The following equations are used to set t_{ABSET} initially.

Equate shim inductance to two times C_{OSS} capacitance:

$$2\pi \times f_R L_S = \frac{1}{2\pi \times f_R \times (2 \times C_{OSS_QA_AVG})} \quad (144)$$

Calculate tank frequency:

$$f_R = \frac{1}{2\pi \sqrt{L_S \times (2 \times C_{OSS_QA_AVG})}} \quad (145)$$

Set initial t_{ABSET} delay time and adjust as necessary.

NOTE

The 2.25 factor of the t_{ABSET} equation was derived from empirical test data and may vary based on individual design differences.

$$t_{ABSET} = \frac{2.25}{f_R \times 4} \approx 346\,ns \quad (146)$$

The resistor divider formed by R_A and R_{AHI} programs the t_{ABSET}, t_{CDSET} delay range of the UCC28950. Select a standard resistor value for R_{AHI}.

NOTE

t_{ABSET} can be programmed between 30 ns to 1000 ns.

$$R_{AHI} = 8.25\,k\Omega \quad (147)$$

The voltage at the ADEL input of the UCC28950 (V_{ADEL}) needs to be set with R_A based on the following conditions.

If t_{ABSET} > 155 ns set V_{ADEL} = 0.2 V, t_{ABSET} can be programmed between 155 ns and 1000 ns:

If $t_{ABSET} \leq$ 155 ns set V_{ADEL} = 1.8 V, t_{ABSET} can be programmed between 29 ns and 155 ns:

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Based on V_{ADEL} selection, calculate R_A:

$$R_A = \frac{R_{AHI} \times V_{ADEL}}{5V - V_{ADEL}} \approx 344\,\Omega \tag{148}$$

Select the closest standard resistor value for R_A:

$$R_A = 348\,\Omega \tag{149}$$

Recalculate V_{ADEL} based on resistor divider selection:

$$V_{ADEL} = \frac{5\,V \times R_A}{R_{AHI} + R_A} = 0.202\,V \tag{150}$$

Resistor R_{AB} programs t_{ABSET}:

$$R_{AB} = \frac{T_{ABSET}}{5} \times \left(0.26 + CS \times K_A \times 1.3\right) \approx 30.6k\Omega \tag{151}$$

Select a standard resistor value for the design:

$$R_{AB} = 30.1k\Omega \tag{152}$$

NOTE

Once you have a prototype up and running it is recommended you fine tune t_{ABSET} at light load to the peak and valley of the resonance between L_S and the switch node capacitance. In this design the delay was set at 10% load. Please refer to Figure 53.

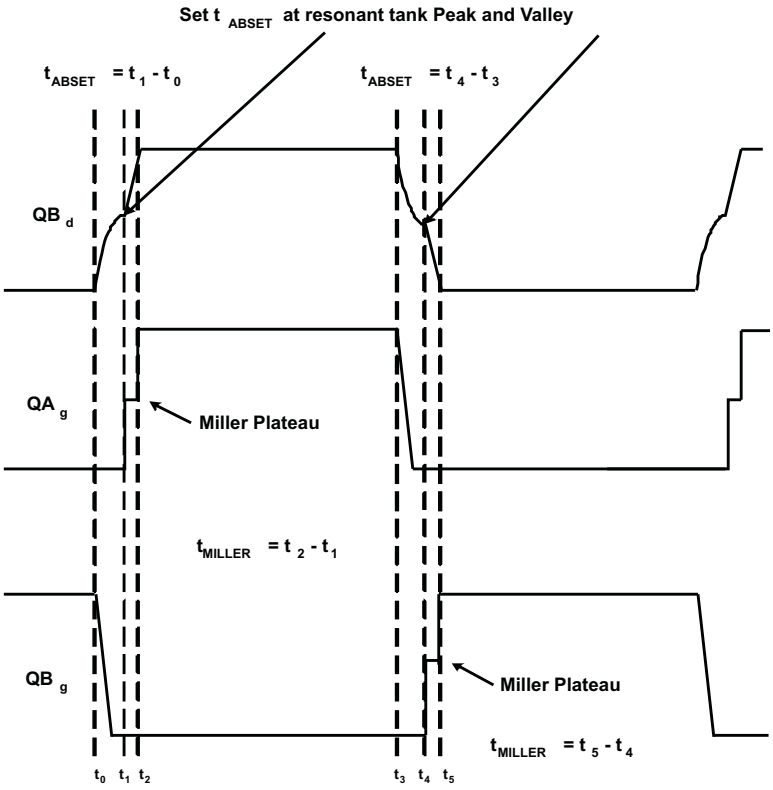

Figure 53. t_{ABSET} to Achieve Valley Switching at Light Loads

The QC and QD turnon delays (t_{CDSET}) should be initially set for the same delay as the QA and QB turn on delays (Pin 6). The following equations program the QC and QD turn-on delays (t_{CDSET}) by properly selecting resistor R_{DELCD} (Pin 7).

$$t_{ABSET} = t_{CDSET} \tag{153}$$

Resistor R_{CD} programs t_{CDSET}:

$$R_{CD} = \frac{T_{CDSET}}{5} \times \left(0.26 + CS \times K_A \times 1.3\right) \approx 30.6k\Omega \tag{154}$$

Select a standard resistor for the design:

$$R_{CD} = 30.1k\Omega \tag{155}$$

NOTE

Once you have a prototype up and running it is recommended to fine tune t_{CDSET} at light load. In this design the CD node was set to valley switch at roughly 10% load. Please refer to Figure 54. Obtaining ZVS at lighter loads with switch node QD_d is easier due to the reflected output current present in the primary of the transformer at FET QD and QC turnoff/on. This is because there was more peak current available to energize L_S before this transition, compared to the QA and QB turnoff/on.

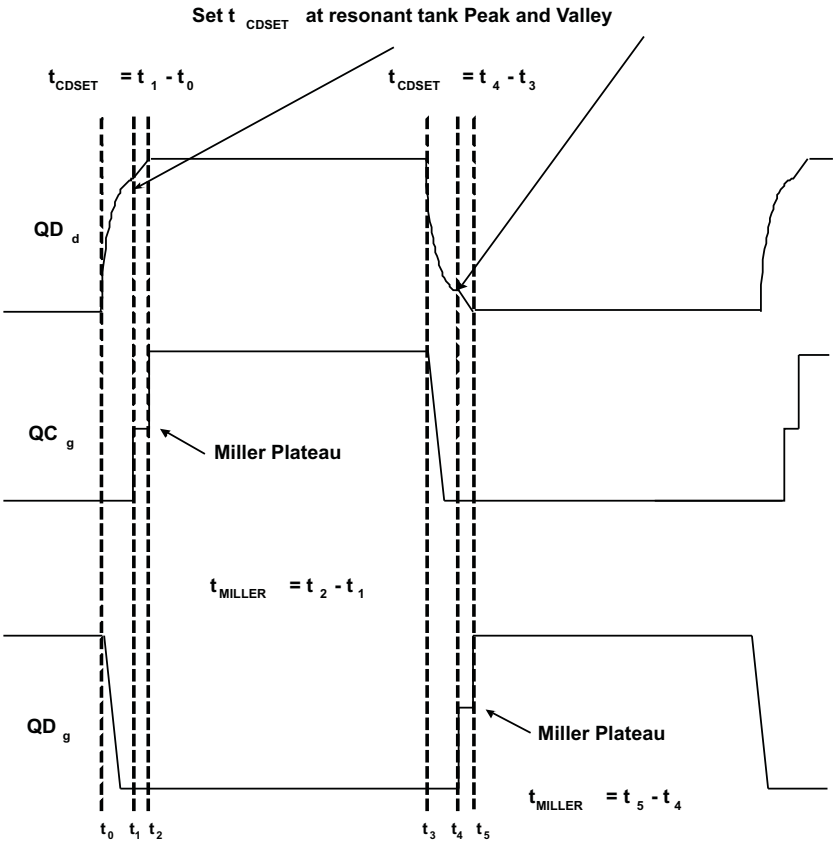

Figure 54. t_{CDSET} to Achieve Valley Switching at Light Loads

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There is a programmable delay for the turnoff of FET QF after FET QA turnoff (t_{AFSET}) and the turnoff of FET QE after FET QB turnoff (t_{BESET}). A good place to set these delays is 50% of t_{ABSET}. This will ensure that the appropriate synchronous rectifier turns off before the AB ZVS transition. If this delay is too large it will cause OUTE and OUTF not to overlap correctly and it will create excess body diode conduction on FETs QE and QF.

$$t_{AFSET} = t_{BESET} = t_{ABSET} \times 0.5 \tag{156}$$

The resistor divider formed by R_{AEF} and R_{AEFHI} programs the t_{AFSET} and t_{BESET} delay range of the UCC28950. Select a standard resistor value for R_{AEFHI}.

NOTE

t_{EFSET} and t_{BESET} can be programmed between 32 ns to 1100 ns.

$$R_{AEFHI} = 8.25\,k\Omega \tag{157}$$

The voltage at the ADELEF pin of the UCC28950 (V_{ADELEF}) needs to be set with R_{AEF} based on the following conditions.

If t_{AFSET} < 170 ns set V_{ADEL} = 0.2 V, t_{ABSET} can be programmed between 32 ns and 170 ns:

If t_{ABSET} > or = 170 ns set V_{ADEL} = 1.7 V, t_{ABSET} can be programmed between 170 ns and 1100 ns:

Based on V_{ADELEF} selection, calculate R_{AEF}:

$$R_{AEF} = \frac{R_{AEFHI} \times V_{ADELEF}}{5\,V - V_{ADELEF}} \approx 4.25\,k\Omega \tag{158}$$

Select the closest standard resistor value for R_{AEF}:

$$R_{AEF} = 4.22\,k\Omega \tag{159}$$

Recalculate V_{ADELEF} based on resistor divider selection:

$$V_{ADELEF} = \frac{5\,V \times R_{AEF}}{R_{AEFHI} + R_{AEF}} = 1.692\,V \tag{160}$$

The following equation was used to program t_{AFSET} and t_{BESET} by properly selecting resistor R_{EF}.

$$R_{EF} = \frac{\left(t_{AFSET} \times 0.5 - 4\,ns\right)}{ns} \times \frac{\left(2.65\,V - V_{ADELEF} \times 1.32\right) \times 10^3}{5} \times \frac{1}{1A} \approx 14.1\,k\Omega \tag{161}$$

A standard resistor was chosen for the design.

$$R_{EF} = 14\,k\Omega \tag{162}$$

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Resistor R_{TMIN} programs the minimum on time (t_{MIN}) that the UCC28950 (Pin 9) can demand before entering burst mode. If the UCC28950 controller tries to demand a duty cycle on time of less than t_{MIN} the power supply will go into burst mode operation. For this design we set the minimum on time to 75 ns.

$$t_{MIN} = 75\,ns \tag{163}$$

The minimum on time is set by selecting R_{TMIN} with the following equation.

$$R_{TMIN} = \frac{t_{MIN}}{5.92} \approx 12.7\,k\Omega \tag{164}$$

A standard resistor value is then chosen for the design.

$$R_{TMIN} = 13\,k\Omega \tag{165}$$

A resistor from the RT pin to ground sets the converter switching frequency.

$$R_T = \left(\frac{2.5 \times 10^6 \frac{\Omega Hz}{V}}{\frac{F_{SW}}{2}} - \frac{\Omega}{V} \right) \times \left(V_{REF} - 2.5\,V \right) \times 2.5 \times 10^3 \approx 60\,k\Omega \tag{166}$$

Select a standard resistor for the design.

$$R_T = 61.9\,k\Omega \tag{167}$$

The UCC28950 provides slope compensation. The amount of slope compensation is set by the resistor R_{SUM}. As suggested earlier, we set the slope compensation ramp to be half the inductor current ramp downslope (inductor current ramp during the off time), reflected through the main transformer and current sensing networks as explained earlier in *Slope Compensation (R_{SUM})*.

The required slope compensation ramp is

$$me = 0.5 \times \frac{V_{OUT} \times R_{CS}}{L_{OUT} \times a1 \times CT_{RAT}} = 0.5 \times \frac{12 \times 47}{2 \times 10^{-6} \times 21 \times 100} = 67 \frac{mV}{\mu s} \tag{168}$$

The magnetizing current of the power transformer provides part of the compensating ramp and is calculated from Equation 169.

$$m_{MAG} = \frac{V_{INMAX} \times R_{CS}}{L_{MAG} \times CT_{RAT}} = \frac{400 \times 47}{2.76x10^{-3} \times 100} \approx 7 \frac{mV}{\mu s} \tag{169}$$

The required compensating ramp is

$$m_{SUM} = me - m_{MAG} = (67 - 7) \frac{mV}{\mu s} = 60 \frac{mV}{\mu s} \tag{170}$$

The value for the resistor, R_{SUM}, may be found from the graph in Figure 37 or calculated from rearranged versions of Equation 12 or Equation 13 depending on whether the controller is operating in Current or Voltage Control Mode. In this case we are using Current Mode Control and Equation 12 is rearranged and evaluated as follows

$$R_{SUM} = \frac{2.5}{0.5 \times m_{SUM}} = \frac{2.5}{0.5 \times 60x10^{-3}} \approx 82k\Omega \tag{171}$$

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Check that the 300mV we allowed for the slope compensation ramp when choosing R_{CS} in Equation 110 is sufficient.

$$\Delta V_{SLOPE-COMP} = \frac{m_{SUM} \times D_{MAX}}{2 \times F_{SW}} = \frac{60\frac{mV}{\mu s} \times 0.7}{2 \times 100kHz} = 210mV \tag{172}$$

To increase efficiency at lighter loads the UCC28950 is programmed (Pin 12, DCM) under light load conditions to disable the synchronous FETs on the secondary side of the converter (Q_E and Q_F). This threshold is programmed with resistor divider formed by R_{DCMHI} and R_{DCM}. This DCM threshold needs to be set at a level before the inductor current goes discontinuous. The following equation sets the level at which the synchronous rectifiers are disabled at roughly 15% load current.

$$V_{RCS} = \frac{\left(\frac{P_{OUT} \times 0.15}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2}\right) \times R_{CS}}{a1 \times CT_{RAT}} = 0.29\,V \tag{173}$$

Select a standard resistor value for R_{DCM}.

$$R_{DCM} = 1k\Omega \tag{174}$$

Calculate resistor value R_{DCMHI}.

$$R_{DCMHI} = \frac{R_{DCM}\left(V_{REF} - V_{RCS}\right)}{V_{RCS}} \approx 16.3k\Omega \tag{175}$$

Select a standard resistor value for this design

$$R_{DCMHI} = 16.9k\Omega \tag{176}$$

NOTE

It is recommended to use an RCD clamp to protect the output synchronous FETs from overvoltage due to switch node ringing.

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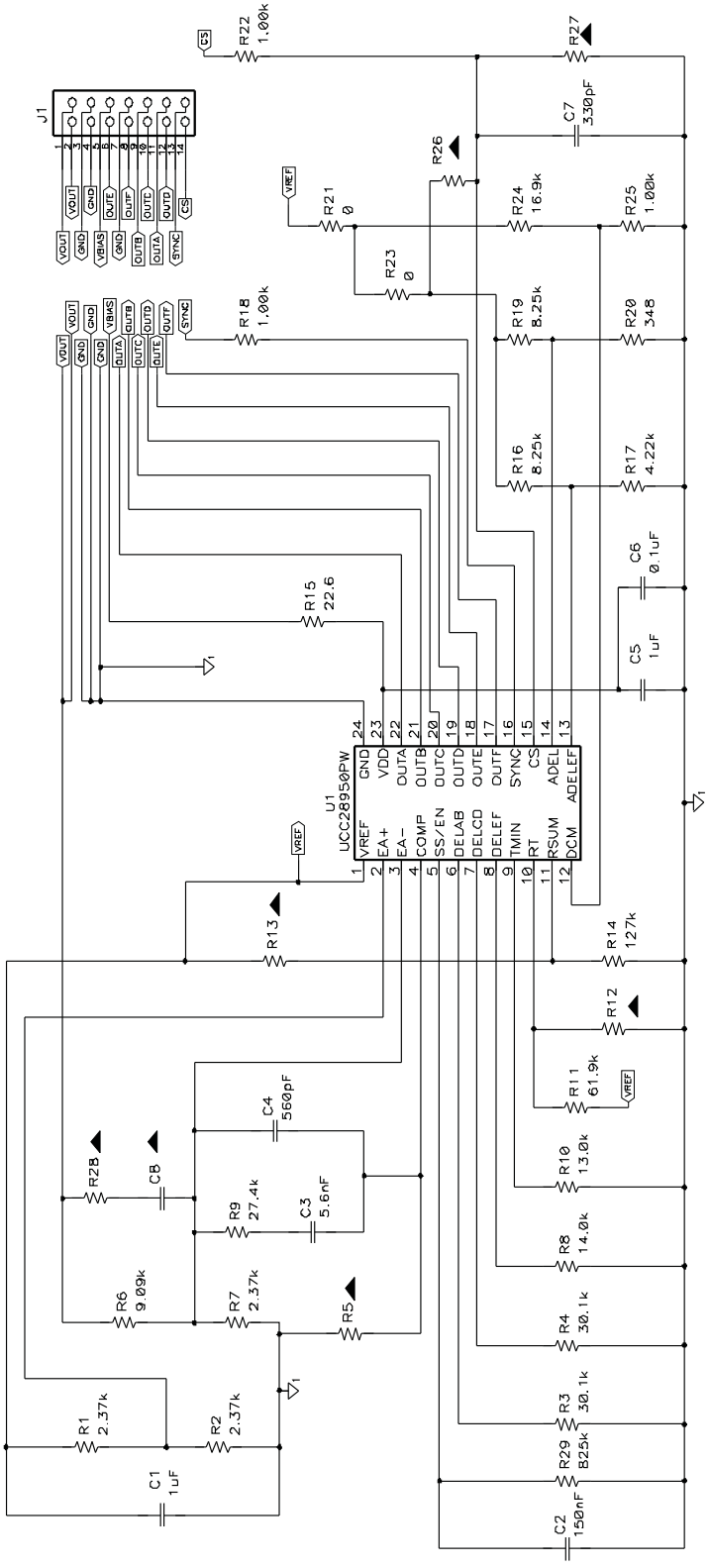

Figure 55. Daughter Board Schematic

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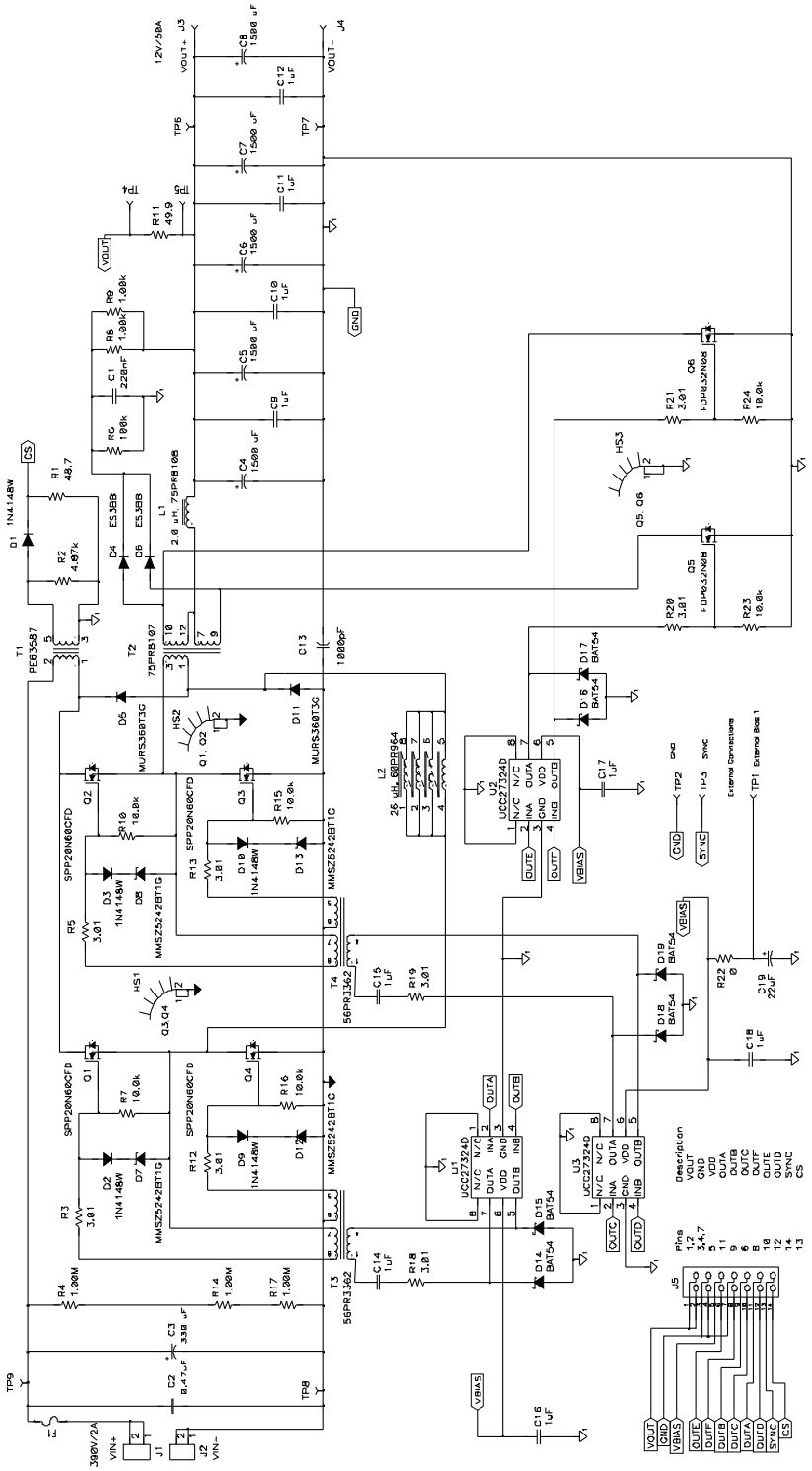
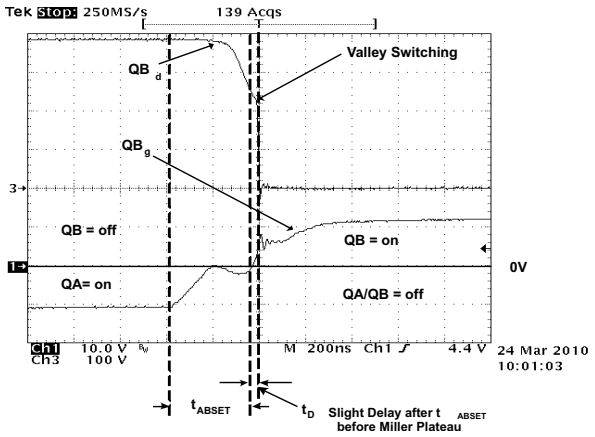


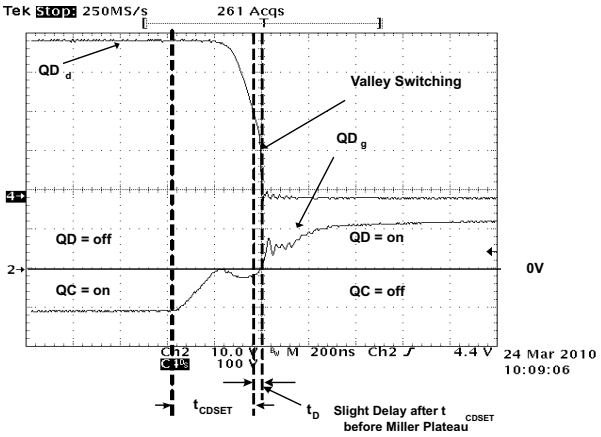
Figure 56. Power Stage Schematic

8.2.3 Application Curves



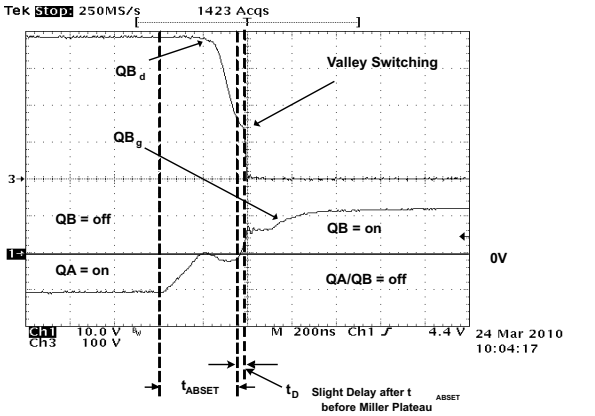
V_{IN} = 390 V
I_{OUT} = 5 A

Figure 57. Full Bridge Gate Drives and Primary Switch Nodes (QB_d and QD_d)



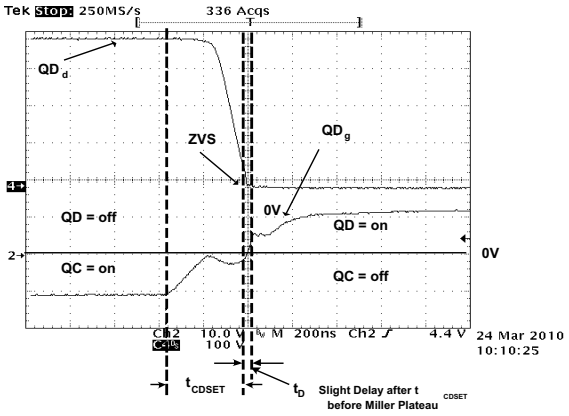
V_{IN} = 390 V
I_{OUT} = 5 A

Figure 58. Full Bridge Gate Drives and Primary Switch Nodes (QD_g QD_d)



V_{IN} = 390 V
I_{OUT} = 10 A

Figure 59. Full-Bridge Gate Drives and Switch Nodes (QB_g QB_d)



V_{IN} = 390 V
I_{OUT} = 10 A

Figure 60. Full-Bridge Gate Drives and Switch Nodes (QD_g QD_d)

NOTE

Switch node QB_d is valley switching and node QD_d has achieved ZVS. Please refer to Figure 59 and Figure 60. It is not uncommon for switch node QD_d to obtain ZVS before QB_d. This is because during the QD_d switch node voltage transition, the reflected output current provides immediate energy for the LC tank at the switch node. Where at the QB_d switch node transition the primary has been shorted out by the high side or low side FETs in the H bridge. This transition is dependent on the energy stored in L_S and L_{LK} to provide energy for the LC tank at switch node QB_d making it take longer to achieve ZVS.

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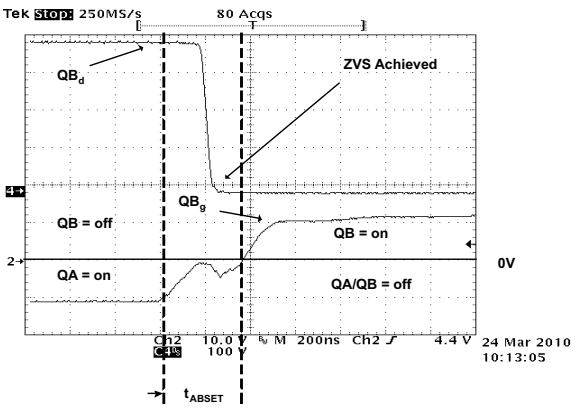

Figure 61. Full-Bridge Gate Drives and Switch Nodes (QB_g QB_d)

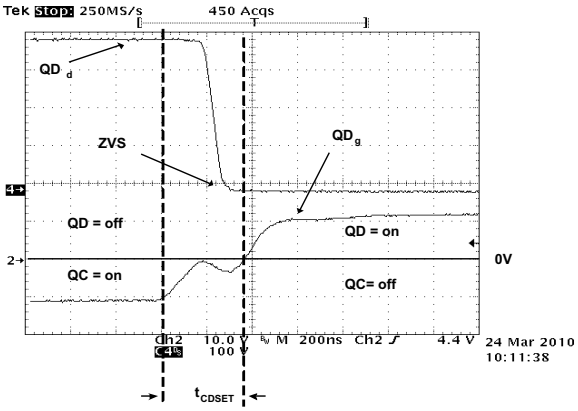

Figure 62. Full-Bridge Gate Drives and Switch Nodes (QD_g QD_d)

NOTE

When the converter is running at 25 A, both switch nodes are operating into zero voltage switching (ZVS). It is also worth mentioning that there is no evidence of the gate miller plateau during gate driver switching. This is because the voltage across the drains and sources of FETs QA through QD have already transitioned before.

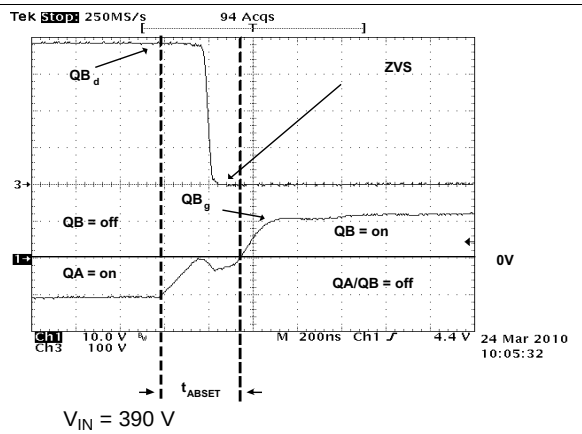

Figure 63. Full-Bridge Gate Drives and Switch Nodes (QB_g QB_d)

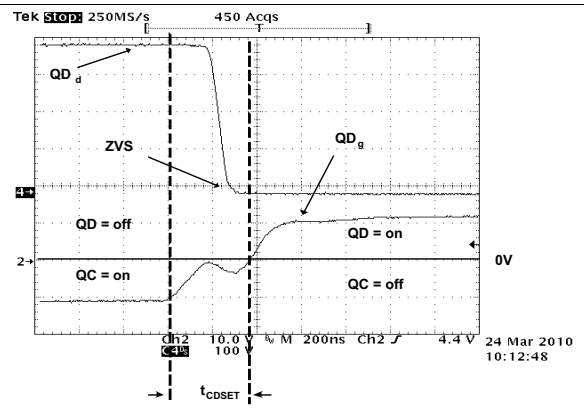

Figure 64. Full-Bridge Gate Drives and Switch Nodes (QD_g QD_d)

NOTE

ZVS maintained from 50% to 100% output power.

9 Power Supply Recommendations

The UCC28950 device should be operated from a V_{DD} rail within the limits given in the *Recommended Operating Conditions* section of this datasheet. To avoid the possibility that the device might stop switching, V_{DD} must not be allowed to fall into the UVLO_FTH range. In order to minimize power dissipation in the device, V_{DD} should not be unnecessarily high. Keeping V_{DD} at 12 V is a good compromise between these competing constraints. The gate drive outputs from the UCC28950 device deliver large-current pulses into their loads. This indicates the need for a low-ESR decoupling capacitor to be connected as directly as possible between the V_{DD} and GND terminals.

TI recommends ceramic capacitors with stable dielectric characteristics over temperature, such as X7R. Avoid capacitors which have a large drop in capacitance with applied DC voltage bias. For example, use a part that has a low-voltage co-efficient of capacitance. The recommended decoupling capacitance is 1 μF, X7R, with at least a 25-V rating with a 0.1-μF NPO capacitor in parallel.

10 Layout

10.1 Layout Guidelines

In order to increase the reliability and robustness of the design, TI recommends the following layout guidelines.

- VREF pin. Decouple this pin to GND with a good quality ceramic capacitor. A 1-uF, X7R, 25V capacitor is recommended. Keep VREF PCB tracks as far away as possible from sources of switching noise.
- EA+ pin. This is the non-inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- EA– pin. This is the inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- COMP pin. The error amplifier compensation network is normally connected to this pin. Keep tracks from this pin as short as possible.
- SS/EN pin. Keep tracks from this pin as short as possible. If the Enable signal is coming from a remote source then avoid running it close to any source of high dv/dt (MOSFET Drain connections for example) and add a simple RC filter at the SS/EN pin.
- DELAB, DELCD, DELEF, TMIN, RT, R_{SUM}, DCM, ADELEF and ADEL pins. The components connected to these pins are used to set important operating parameters. Keep these components close to the IC and provide short, low impedance return connections to the GND pin.
- CS pin. This connection is arguably the most important single connection in the entire PSU system. Avoid running the CS signal traces near to sources of high dv/dt. Provide a simple RC filter as close to the pin as possible to help filter out leading edge noise spikes which will occur at the beginning of each switching cycle.
- SYNC pin. This pin is essentially a digital I/O port. If it is unused, then it may be left open circuit or tied to ground via a 1-kΩ resistor. If Synchronisation is used, then route the incoming Synchronisation signal as far away from noise sensitive input pins as possible.
- OUTA, OUTB, OUTC, OUTD, OUTE and OUTF pins. These are the gate drive output pins and will have a high dv/dt rate associated with their rising and falling edges. Keep the tracks from these pins as far away from noise sensitive input pins as possible. Ensure that the return currents from these outputs do not cause voltage changes in the analog ground connections to noise sensitive input pins. Follow the layout recommendation for Analog and Power ground Planes in Figure 45.
- VDD pin. This pin must be decoupled to GND using ceramic capacitors as detailed in the 'Power Supply Recommendations' section. Keep this capacitor as close to the VDD and GND pins as possible.
- GND pin. This pin provides the ground reference to the controller. Use a Ground Plane to minimize the impedance of the ground connection and to reduce noise pickup.

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10.2 Layout Example

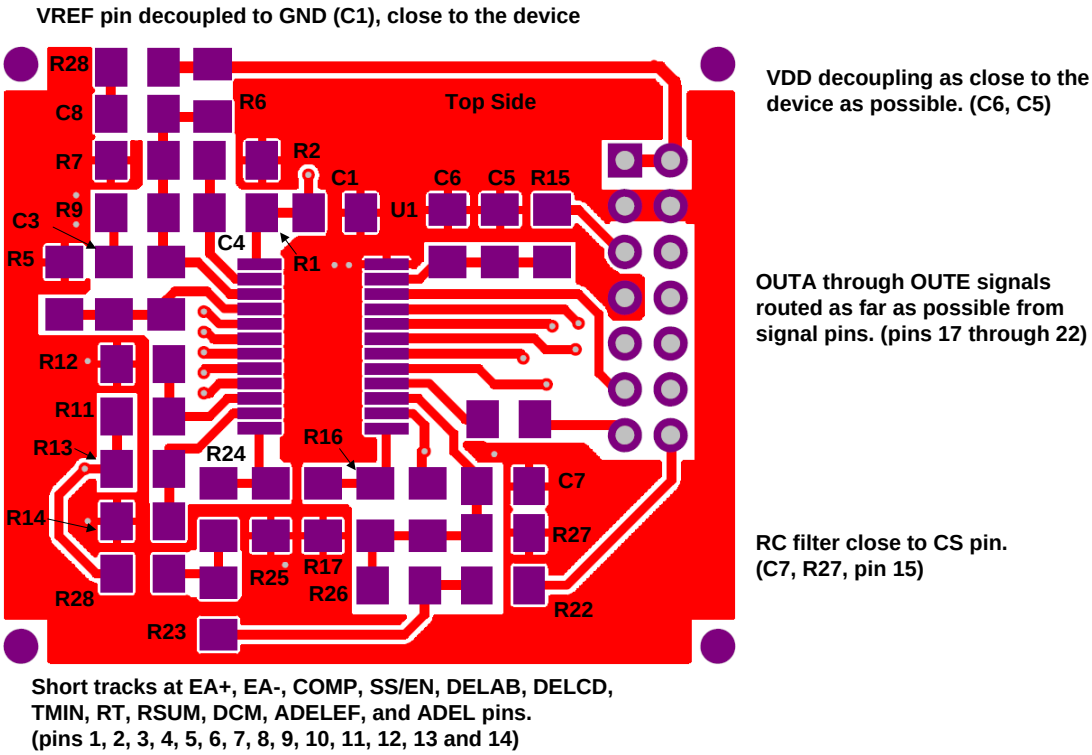

Figure 65. UCC28950 Layout Example (Top Side)

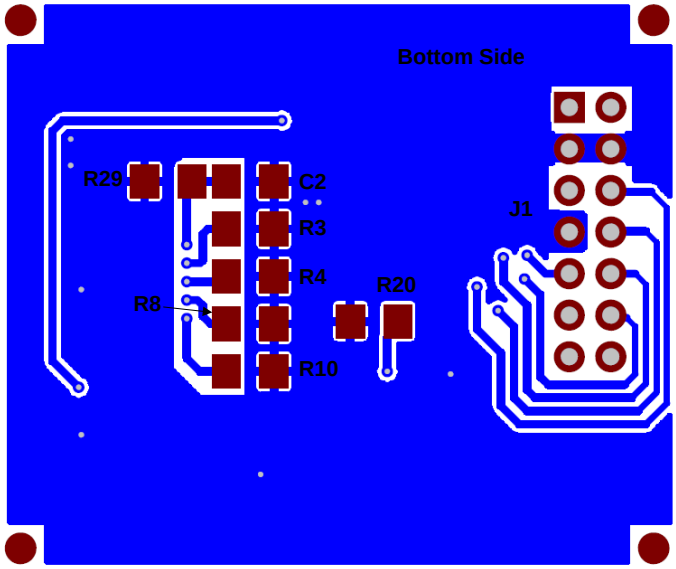

Figure 66. UCC28950 Layout Example (Bottom Side)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For the MathCAD Design Tool, see SLUC210.

For the Excel Design Tool, see SLUC222.

11.2 Documentation Support

11.2.1 Related Documentation

Synchronizing Three or More UCC28950 Phase-Shifted, Full-Bridge Controllers, SLUA609.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28950PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28950	Samples
UCC28950PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28950	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC28950 :

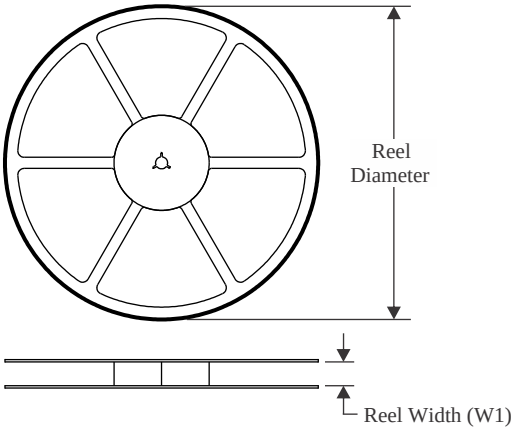
- Automotive: UCC28950-Q1

NOTE: Qualified Version Definitions:

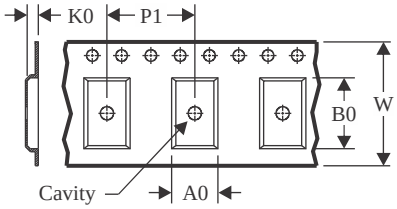
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

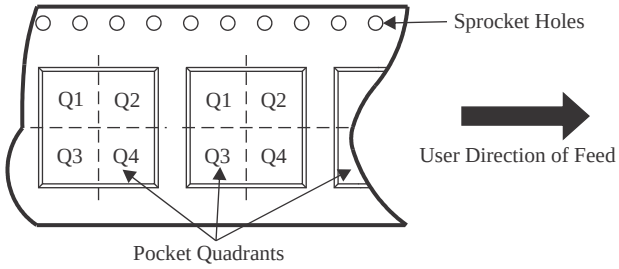


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

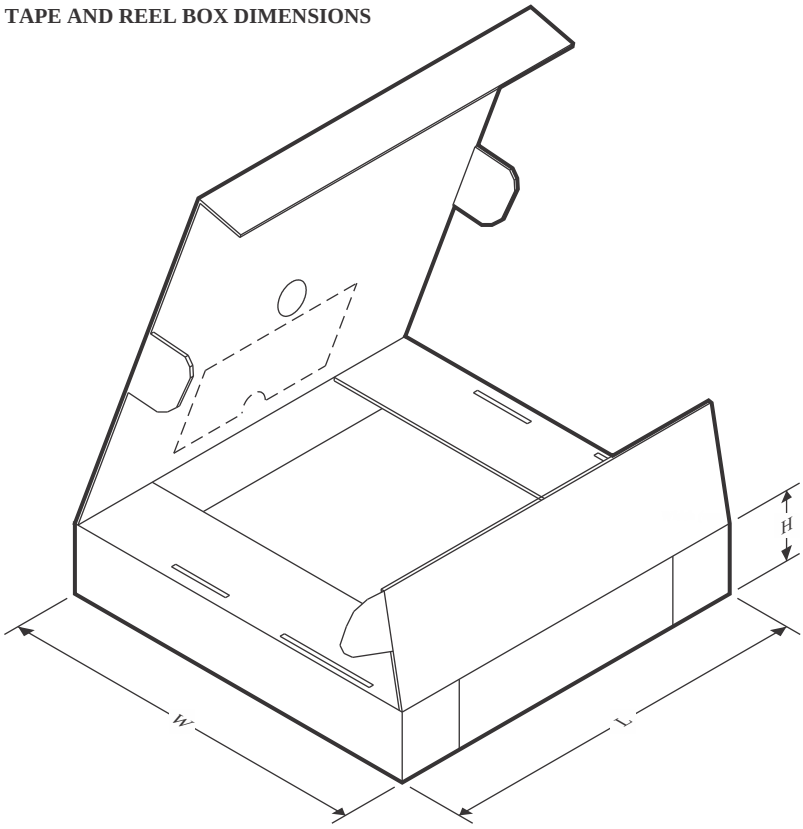
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28950PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

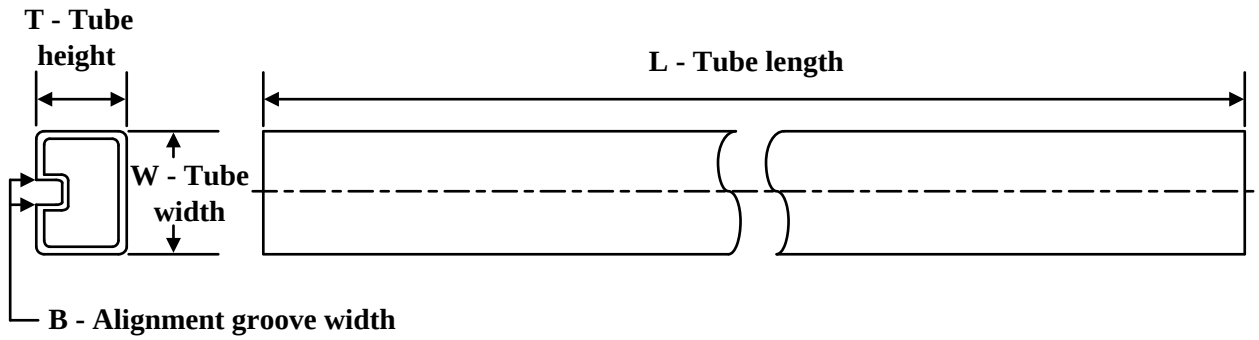
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28950PWR	TSSOP	PW	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

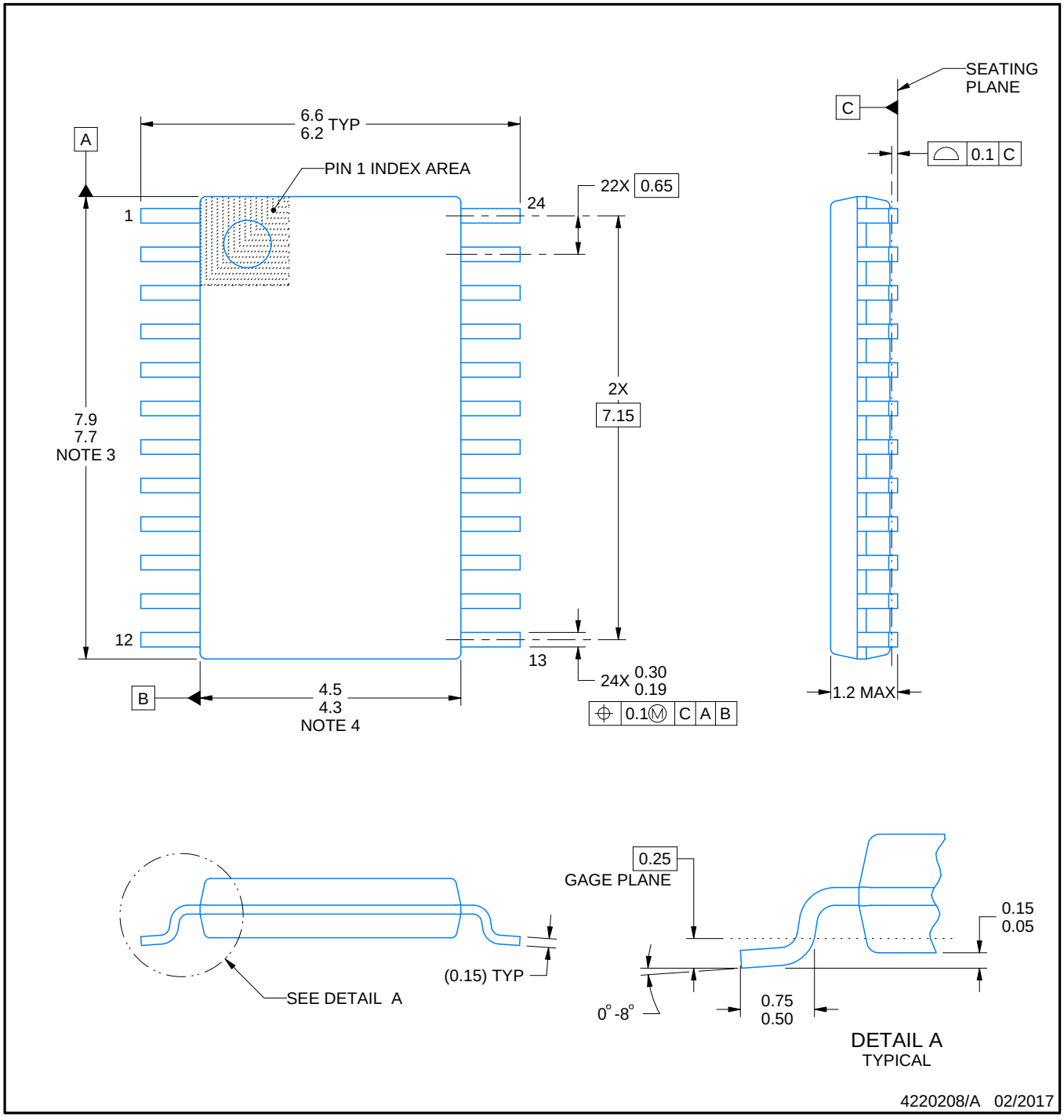
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28950PW	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

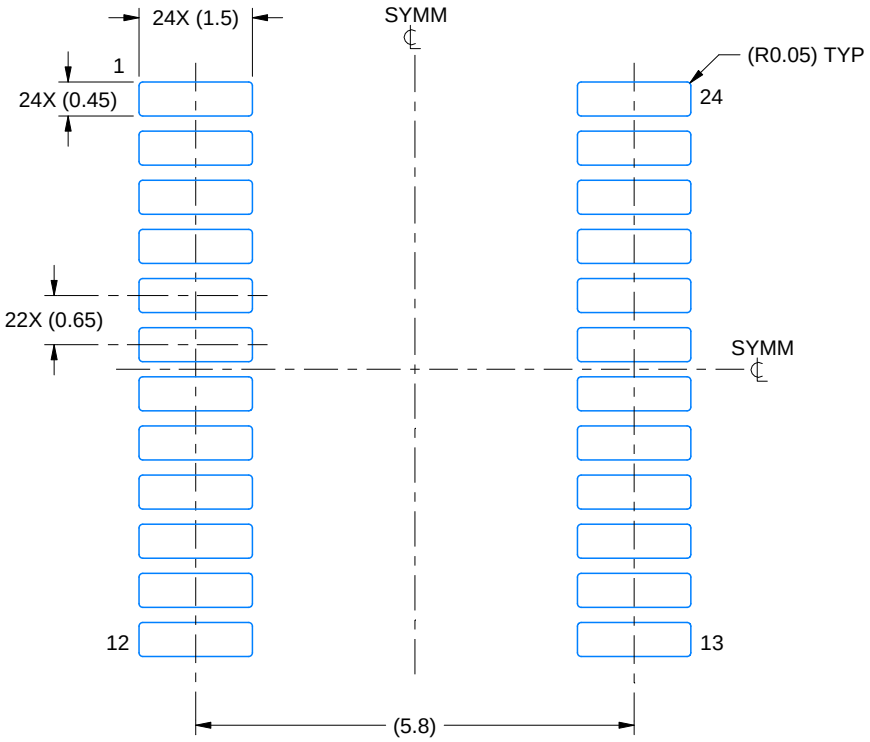
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

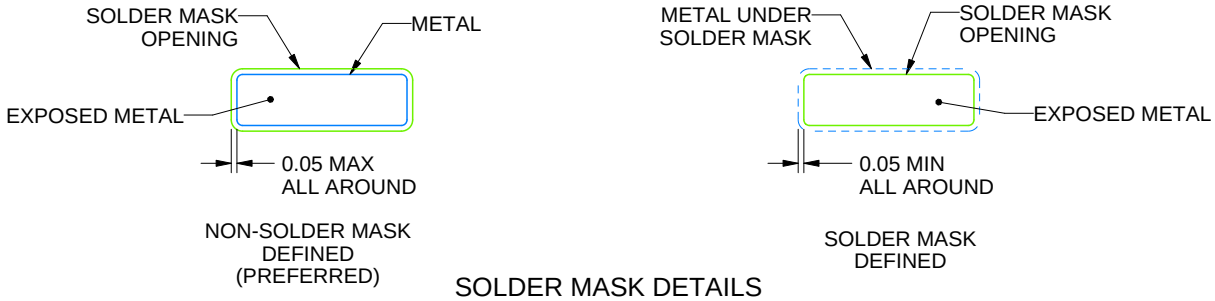


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

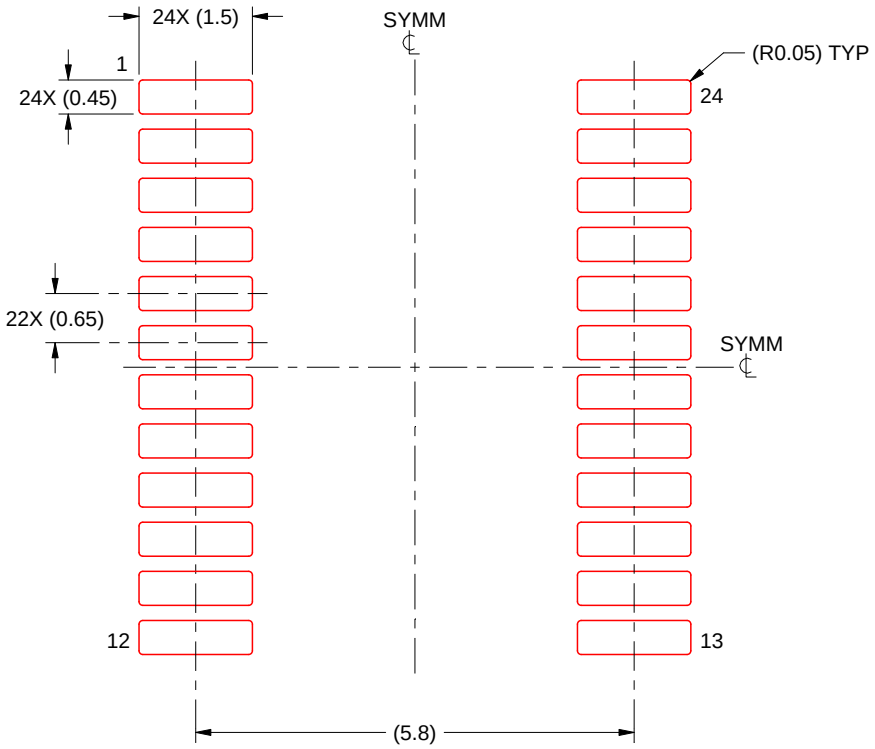


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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