THE DATASHEET OF

ADS58C48IPFPR

Quad Channel IF Receiver with SNRBoost 3G

Check for Samples: ADS58C48

FEATURES

- **Maximum Sample Rate: 200 MSPS**
- **High Dynamic Performance**
  - **SFDR 82 dBc at 140 MHz**
  - **72.3 dBFS SNR in 60 MHz BW Using *SNRBoost* 3G technology**
- ***SNRBoost* 3G Highlights**
  - **Supports Wide Bandwidth up to 60 MHz**
  - **Programmable Bandwidths – 60 MHz, 40 MHz, 30 MHz, 20 MHz**
  - **Flat Noise Floor within the Band**
  - **Independent *SNRBoost* 3G Coefficients for Every Channel**
- **Output Interface**
  - **Double Data Rate (DDR) LVDS with Programmable Swing and Strength**
    - **Standard Swing: 350 mV**
    - **Low Swing: 200 mV**
    - **Default Strength: 100-Ω Termination**
    - **2x Strength: 50-Ω Termination**
  - **1.8V Parallel CMOS Interface Also Supported**
- **Ultra-Low Power with Single 1.8-V Supply**
  - **0.9-W Total Power**
  - **1.32-W Total Power (200 MSPS) with *SNRBoost* 3G on all 4 Channels**
  - **1.12-W Total Power (200 MSPS) with *SNRBoost* 3G on 2 Channels**
- **Programmable Gain up to 6dB for SNR/SFDR Trade-Off**
- **DC Offset Correction**
- **Supports Low Input Clock Amplitude**
- **80-TQFP Package**

DESCRIPTION

The ADS58C48 is a quad channel 11-bit A/D converter with sampling rate up to 200 MSPS. It uses innovative design techniques to achieve high dynamic performance, while consuming extremely low power at 1.8V supply. This makes it well-suited for multi-carrier, wide band-width communications applications.

The ADS58C48 uses third-generation *SNRBoost* 3G technology to overcome SNR limitation due to quantization noise (for bandwidths < Nyquist, Fs/2). Enhancements in the *SNRBoost* 3G technology allow support for SNR improvements over wide bandwidths (up to 60 MHz). In addition, separate *SNRBoost* 3G coefficients can be programmed for each channel.

The device has digital gain function that can be used to improve SFDR performance at lower full-scale input ranges. It includes a dc offset correction loop that can be used to cancel the ADC offset.

The digital outputs of all channels are output as DDR LVDS (Double Data Rate) together with an LVDS clock output. The low data rate of this interface (400 Mbps at 200 MSPS sample rate) makes it possible to use low-cost FPGA-based receivers. The strength of the LVDS output buffers can be increased to support 50-Ω differential termination. This allows the output clock signal to be connected to two separate receiver chips with an effective 50-Ω termination (such as the two clock ports of the GC5330).

The same digital output pins can also be configured as a parallel 1.8-V CMOS interface.

It includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. The device is specified over the industrial temperature range (–40°C to 85°C).

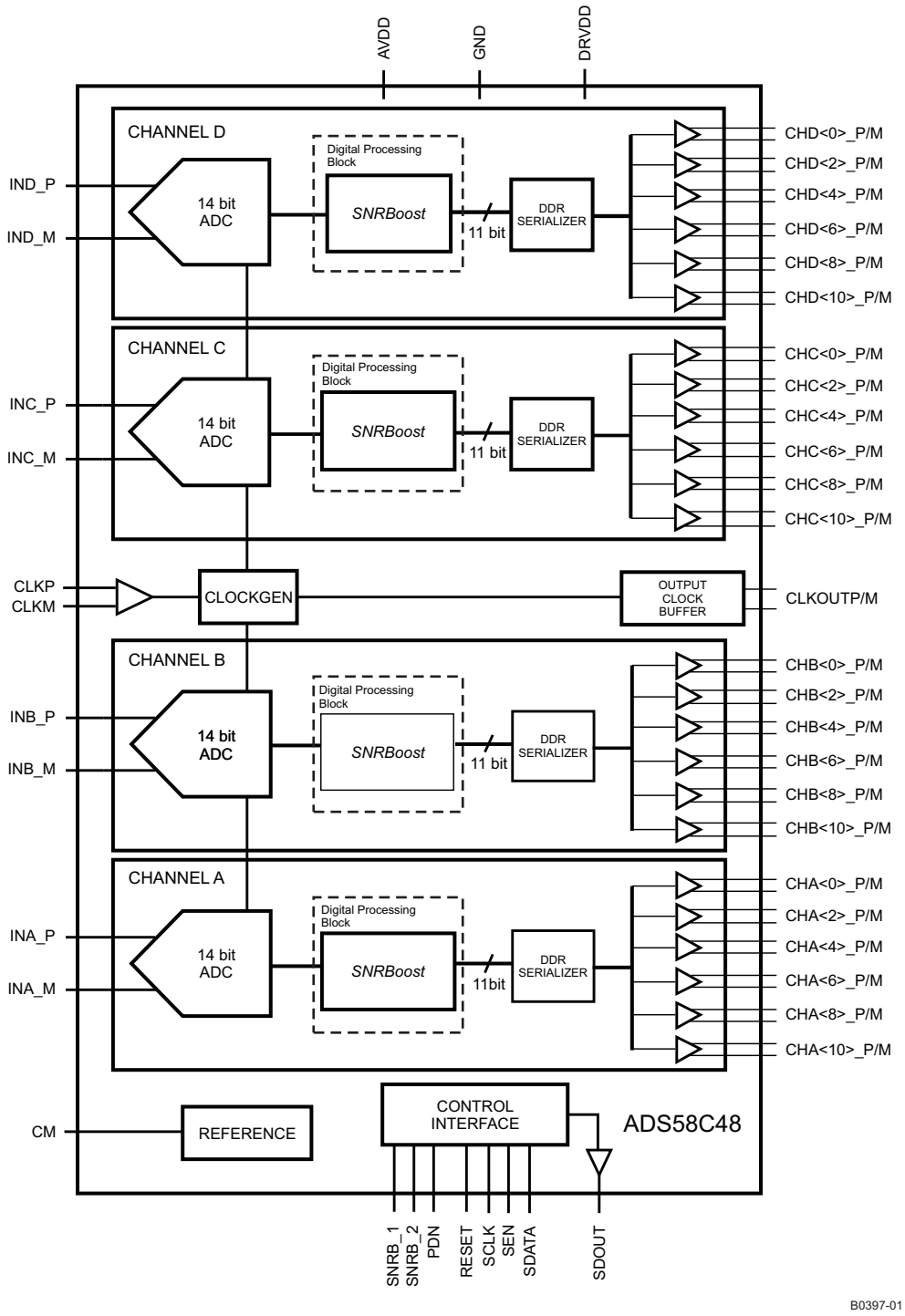


Figure 1. ADS58C48 Block Diagram (LVDS interface)

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN (2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS58C48	TQFP-80	PFP	–40°C to 85°C	GREEN (RoHS and no Sb/Br)	Cu NiPdAu	ADS58C48I	ADS58C48IPFP	Tray
							ADS58C48IPFPR	Tape & reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com
(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines Green to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage range, AVDD		–0.3 V to 2.1 V	V
Supply voltage range, DRVDD		–0.3 V to 2.1 V	V
Voltage between AGND and DRGND		–0.3 V to 0.3 V	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		–2.4 V to +2.4 V	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		–2.4 V to +2.4 V	V
Voltage applied to input pins	INP, INM	–0.3 V to minimum (1.9, AVDD + 0.3 V)	V
	CLKP, CLKM(2)	-0.3 V to AVDD + 0.3 V	
	RESET, SCLK, SDATA, SEN, SNRB_1, SNRB_2, PDN	–0.3 V to 3.9 V	
Operating free-air temperature range, T_A		–40 to 85	°C
Operating junction temperature range, T_J		125	°C
Storage temperature range, T_{stg}		–65 to 150	°C
ESD, human body model		2	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is < |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYPICAL VALUE	UNIT
$R_{\theta JA}$ (2)	Soldered thermal pad, no airflow	24	°C/W
	Soldered thermal pad, 200 LFM	16	°C/W
$R_{\theta JC}$ (3)	Bottom of package (thermal pad)	0.3	°C/W

(1) With a JEDEC standard high K board and 5x5 via array. See the Exposed Pad section in the Application Information.
(2) $R_{\theta JA}$ is the thermal resistance from the junction to ambient
(3) $R_{\theta JC}$ is the thermal resistance from the junction to the thermal pad.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLIES					
Analog supply voltage, AVDD		1.7	1.8	1.9	V
Digital supply voltage, DRVDD		1.7	1.8	1.9	V
ANALOG INPUTS					
Differential input voltage range			2		V_{PP}
Input common-mode voltage			V_{CM} ±0.05		V
Maximum analog input frequency with 2-V_{pp} input amplitude (1)			400		MHz
Maximum analog input frequency with 1-V_{pp} input amplitude (1)			600		MHz
CLOCK INPUT					
Input clock sample rate		1		200	MSPS
Input clock amplitude differential (V_{CLKP} - V_{CLKM})	Sine wave, ac-coupled	0.2	1.5		V_{pp}
	LVPECL, ac-coupled		1.6		V_{pp}
	LVDS, ac-coupled		0.7		V_{pp}
	LVCMOS, single-ended, ac-coupled		3.3		V
Input clock duty cycle			50%		
DIGITAL OUTPUTS					
Maximum external load capacitance from each output pin to DRGND C_{LOAD}	Default strength		5		pF
	Maximum strength		10		pF
Differential load resistance between the LVDS output pairs (LVDS mode), R_{LOAD}			100		Ω
HIGH PERFORMANCE MODES (2) (3)					
High perf mode	Set this register bit to get best performance across sample clock and input signal frequencies	Register address = 0x03, data = 0x03			
High freq mode	Set these register bits for high input signal frequencies (> 200 MHz)	Register address = 0x4A, data = 0x01			
		Register address = 0x58, data = 0x01			
		Register address = 0x66, data = 0x01			
		Register address = 0x74, data = 0x01			
Operating free-air temperature, T_A		–40		85	°C

(1) See the THEORY OF OPERATION section in the Application Information
(2) It is recommended to use these modes to get best performance.
(3) See the SERIAL INTERFACE section for details on register programming.

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, 50% clock duty cycle, –1 dBFS differential analog input, LVDS and CMOS interfaces unless otherwise noted.
MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, DRVDD = 1.8 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution					11	bits
ANALOG INPUTS						
	Differential input voltage range			2		Vpp
	Differential input resistance (at 200 MHz, see Figure 52)			0.75		kΩ
	Differential input capacitance (at 200 MHz, see Figure 53)			3.7		pF
	Analog input bandwidth			550		MHz
	Analog input common mode current (per input pin of each channel)			0.8		µA/MSPS
	VCM common mode voltage output			0.95		V
	VCM output current capability			4		mA
POWER SUPPLY						
IAVDD	Analog supply current			290	330	mA
IDRVDD	Output buffer supply current LVDS interface	350-mV LVDS swing with 100-Ω external termination after reset.		207	230	mA
	Analog power			522		mW
	Digital power LVDS interface			373		mW
	Global power down				30	mW

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, 50% clock duty cycle, –1 dBFS differential analog input, LVDS and CMOS interfaces unless otherwise noted.
MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, DRVDD = 1.8 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
DNL	Differential non-linearity	Fin = 170 MHz	–0.9		1.2	LSB
INL	Integral non-linearity	Fin = 170 MHz	–2.0	±1.0	2.0	LSB
	Offset error	Specified across devices and across channels within a device	–25		25	mV
There are two sources of gain error – internal reference inaccuracy and channel gain error						
	Gain error due to internal reference inaccuracy alone	Specified across devices and across channels within a device	–2.5		2.5	%FS
	Gain error of channel alone (1)	Specified across devices and across channels within a device		–0.1%	–1.0%	
	Channel gain error temperature coefficient			0.001		Δ%/°C

(1) This is specified by design and characterization; it is not tested in production.

Table 1. SNR Enhancement with *SNRBoost* [3G] Enabled[(1)]

BANDWIDTH, MHz	SNR WITHIN SPECIFIED BANDWIDTH (dBFS)					
	IN DEFAULT MODE (*SNRBoost* [3G] Disabled)			WITH *SNRBoost* [3G] ENABLED[(2)(3)]		
	MIN	TYP	MAX	MIN	TYP	MAX
60		68		69.7	72.3	
40		69.8		71.8	74.5	
30		71		72.8	75.4	
20		72.8		74.4	76.8	

(1) SNRBoost [3G] bath-tub centered at (3/4)xFs, -2 dBFS input applied at Fin = 140 MHz, sampling frequency = 200 MSPS
(2) Using suitable filters. See note on SNRBoost [3G] in the SNR ENHANCEMENT USING SNRBOOST section.
(3) Specified by characterization.

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, 50% clock duty cycle, –1 dBFS differential analog input, *SNRBoost* disabled, LVDS and CMOS interfaces unless otherwise noted.
MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, DRVDD = 1.8 V

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SNR Signal to noise ratio, **LVDS**	Fin= 20 MHz			66.7		dBFS
	Fin = 100 MHz			66.5		
	Fin = 170 MHz		65	66.1		
SINAD Signal to noise and distortion ratio	Fin = 20 MHz			66.6		dBFS
	Fin = 100 MHz			66.4		
	Fin = 170 MHz		64	65.9		
SFDR Spurious free dynamic range	Fin = 20 MHz			84		dBc
	Fin = 100 MHz			84		
	Fin = 170 MHz		70.5	80		
THD Total harmonic distortion	Fin = 20 MHz			81.5		dBc
	Fin = 100 MHz			82.5		
	Fin = 170 MHz		70	78		
HD2 Second harmonic distortion	Fin = 20 MHz			88		dBc
	Fin = 100 MHz			86		
	Fin = 170 MHz		70.5	82		
HD3 Third harmonic distortion	Fin = 20 MHz			84		dBc
	Fin = 100 MHz			84		
	Fin = 170 MHz		70.5	80		
Worst Spur Other than second, third harmonics	Fin = 20 MHz			90		dBc
	Fin = 100 MHz			89		
	Fin = 170 MHz		76.5	88		
IMD 2-tone inter-modulation distortion	F1 = 185 MHz, F2 = 190 MHZ, each tone at –7 dBFS			83		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input			1		clock cycles
Crosstalk	With a full-scale 170MHz aggressor signal applied and no input on the victim channel	Far channel		98		dB
		Near channel		83		
PSRR AC power supply rejection ratio	For 50-mV_{pp} signal on AVDD supply			25		dB

DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 1.8 V, DRVDD = 1.8 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS – RESET, SCLK, SDATA, SEN, SNRB_1, SNRB_2 and PDN						
High-level input voltage		RESET, SCLK, SDATA and SEN support 1.8 V and 3.3 V CMOS logic levels.	1.3			V
Low-level input voltage					0.4	V
High-level input current	SDATA, SCLK(1)	V_{HIGH} = 1.8 V		10		µA
	SEN(2)	V_{HIGH} = 1.8 V		0		µA
Low-level input current	SDATA, SCLK	V_{LOW} = 0 V		0		µA
	SEN	V_{LOW} = 0 V		–10		µA
DIGITAL OUTPUTS – CMOS INTERFACE (CHx_Dn, SDOUT)						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS – LVDS INTERFACE (CHx<>P/M, CLKOUTP/M)						
V_{ODH}, High-level output voltage(3)		Standard swing LVDS	275	350	425	mV
V_{ODL}, Low-level output voltage(3)		Standard swing LVDS	–425	–350	–275	mV
V_{ODH}, High-level output voltage(3)		Low swing LVDS(4)		200		mV
V_{ODL}, Low-level output voltage(3)		Low swing LVDS(4)		–200		mV
V_{OCM}, Output common-mode voltage			0.9	1.05	1.25	V

(1) SDATA, SCLK have internal 170-kΩ pull-down resistor.
(2) SEN has internal 170-kΩ pull-up resistor to AVDD.
(3) With external 100-Ω termination.
(4) See the LVDS Output Data and Clock Buffers section in the Application Information.

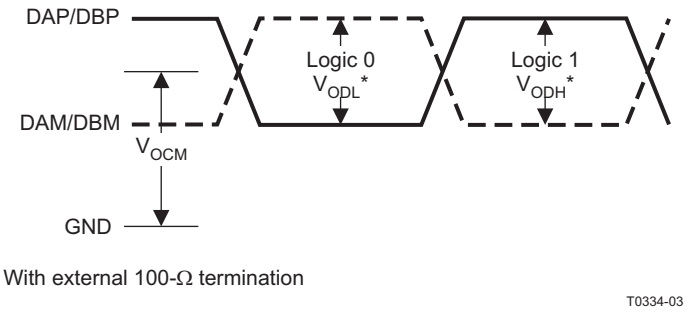


Figure 2. LVDS Output Voltage Levels

TIMING CHARACTERISTICS – LVDS AND CMOS MODES (1)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock, C_{LOAD} = 5 pF (2), R_{LOAD} = 100 Ω(3), unless otherwise noted.
MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, DRVDD = 1.7 V to 1.9 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay		0.5	0.8	1.1	ns
	Aperture delay matching	Between the 4 channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at same temperature and DRVDD supply		±150		ps
t_j	Aperture jitter			140		fs rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		5	25	µs
		Time to valid data after coming out of GLOBAL power down mode		100	500	µs
		Time to valid data after stopping and restarting the input clock		50		µs
	ADC latency (4)	Default latency after reset, DIGITAL MODE1=0, DIGITAL MODE2=0		10		Clock cycles
		SNRBoost only enabled, DIGITAL MODE1=0, DIGITAL MODE2=1		11		Clock cycles
		SNRBoost, Gain and Offset corr enabled, DIGITAL MODE1=1, DIGITAL MODE2=0 or 1		18		Clock cycles
DDR LVDS MODE (5)						
t_{su}	Data setup time(6)	Data valid(6) to zero-crossing of CLKOUTP	0.5	1.1		ns
t_h	Data hold time(6)	Zero-crossing of CLKOUTP to data becoming invalid(6)	0.35	0.70		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*	4.5	6	7.5	ns
	Variation of t_{PDI}	Between two devices at same temperature and DRVDD supply		±0.8		ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*	45%	50%	55%	
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100 mV to +100 mV Fall time measured from +100 mV to –100 mV *1MSPS ≤ Sampling frequency ≤ 200 MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to +100 mV Fall time measured from +100 mV to –100 mV *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		0.18		ns
PARALLEL CMOS MODE						
t_{START}	Input clock to data delay	Input clock falling edge cross-over to start of data valid(7)			–0.40	ns
t_{DV}	Data valid time	Time interval of data valid(7)	3.2	3.8		ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *1 MSPS ≤ Sampling frequency ≤ 150 MSPS*		45%		
t_{RISE} , t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ Sampling frequency ≤ 200 MSPS*		0.6		ns

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to LOGIC HIGH of +100.0 mV and LOGIC LOW of –100.0 mV.
(7) Data valid refers to LOGIC HIGH of 1.26 V and LOGIC LOW of 0.54 V

TIMING CHARACTERISTICS – LVDS AND CMOS MODES [1] (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock, C_{LOAD} = 5 pF [2], R_{LOAD} = 100 Ω [3], unless otherwise noted.
MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, DRVDD = 1.7 V to 1.9 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CLKRISE}$, Output clock rise time $t_{CLKFALL}$ Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ Sampling frequency ≤ 150 MSPS*		0.6		ns

Table 2. LVDS Timings Across Sampling Frequencies

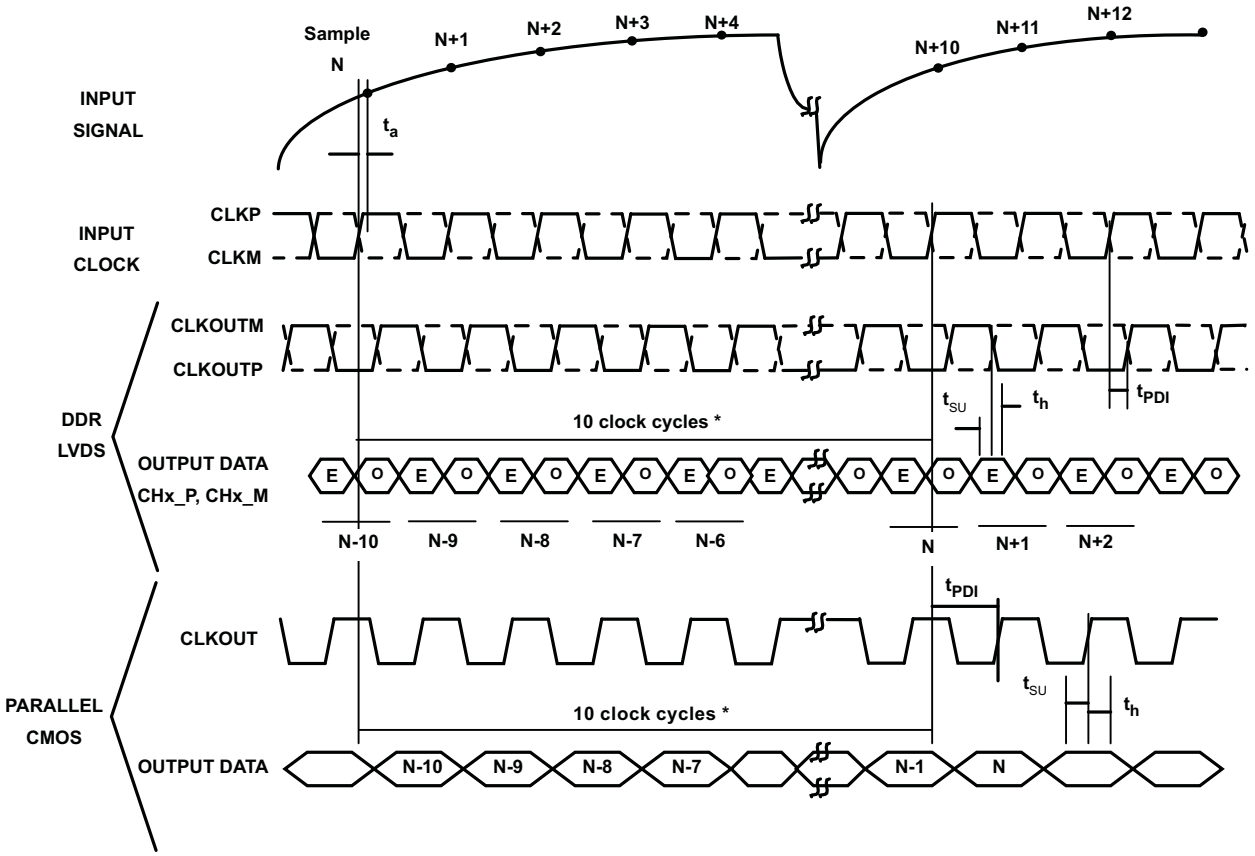
SAMPLING FREQUENCY, MSPS	SETUP TIME, ns			HOLD TIME, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
185	0.7	1.30		0.35	0.70	
170	0.9	1.55		0.35	0.70	
150	1.2	1.9		0.35	0.70	
125	1.9	2.6		0.35	0.70	

Table 3. CMOS Timings Across Sampling Frequencies

SAMPLING FREQUENCY MSPS	TIMINGS SPECIFIED WITH RESPECT TO INPUT CLOCK								
	t_{START}, ns			DATA VALID TIME, ns					
	MIN	TYP	MAX	MIN	TYP	MAX			
185			–1.4	3.6	4.2				
170			–2.8	4.2	4.7				
150			–4.6	4.8	5.4				
125			1.0	6.2	6.8				

SAMPLING FREQUENCY MSPS	TIMINGS SPECIFIED WITH RESPECT TO CLKOUT								
	SETUP TIME, ns			HOLD TIME, ns			t_{PDI}, CLOCK PROPAGATION DELAY, ns [1]		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
150	2.0	2.8		2.0	2.8				
125	2.6	3.5		2.6	3.5				
80	4.8	5.8		4.8	5.8				
80 to 150							5	6.5	8

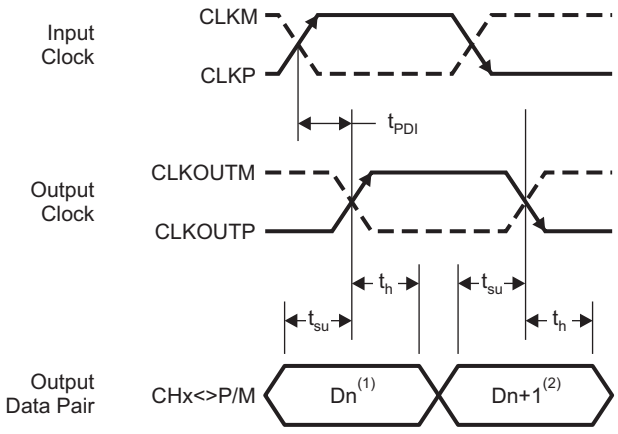
(1) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.



1) ADC latency after reset, At higher sampling frequencies, t_{PDI} > 1 clock cycle which then makes the overall latency = ADC latency + 1.

2) E – Even bits D0, D2, D4…, O – Odd bits D1, D3, D5...

Figure 3. Latency Diagram



1. Dn - Bits D0,D2,D4...
2. Dn +1 - Bits D1,D3,D5...

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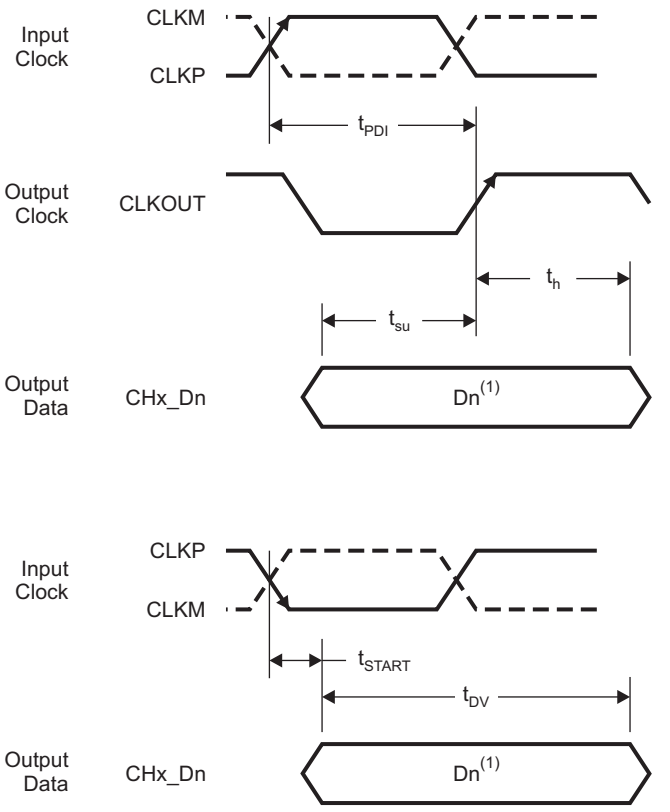
Figure 4. LVDS Mode Timing



1. Dn - Bits D0,D1,D2... of channel A,B,C, and D

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Figure 5. CMOS Mode Timing

DEVICE CONFIGURATION

ADS58C48 has several modes that can be configured using a serial programming interface, as described below. In addition, the device has three dedicated parallel pins for controlling common functions such as power down and *SNRBoost* ^{3G} control.

The functions controlled by each parallel pin are described below.

Table 4. PDN (Digital Control Pin)

VOLTAGE APPLIED ON PDN	STATE OF REGISTER BIT <CONFIGURE PDN PIN>	DESCRIPTION
0	X	Normal operation
HIGH	0	All channel ADCs are put in STANDBY mode (with internal references powered down). This is an intermediate power down mode, with quick wake-up time.
HIGH	1	Device is put in global power down (all channel ADCs, references and output buffers) drawing minimum power, with slow wake-up time.

Table 5. SNRB_1 (Digital Control Pin)

VOLTAGE APPLIED ON SNRB_1	DESCRIPTION
LOW	*SNRBoost* ^{3G} mode OFF for channels C and D
HIGH	*SNRBoost* ^{3G} mode ON for channels C and D

Table 6. SNRB_2 (Digital Control Pin)

VOLTAGE APPLIED ON SNRB_2	DESCRIPTION
LOW	*SNRBoost* ^{3G} mode OFF for channels A and B
HIGH	*SNRBoost* ^{3G} mode ON for channels A and B

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

When SEN is low,

- Serial shift of bits into the device is enabled.
- Serial data (on SDATA pin) is latched at every falling edge of SCLK.
- The serial data is loaded into the register at every 16th SCLK falling edge.

In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits are the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers MUST be initialized to their default values. This can be done in one of two ways –

1. through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10ns) as shown in Figure 6

   OR

2. By applying software reset. Using the serial interface, set the **<RESET>** bit (D1 in register 0x00) to HIGH. This initializes internal registers to their default values and then self-resets the **<RESET>** bit to ***low***. In this case the RESET pin is kept ***low***.

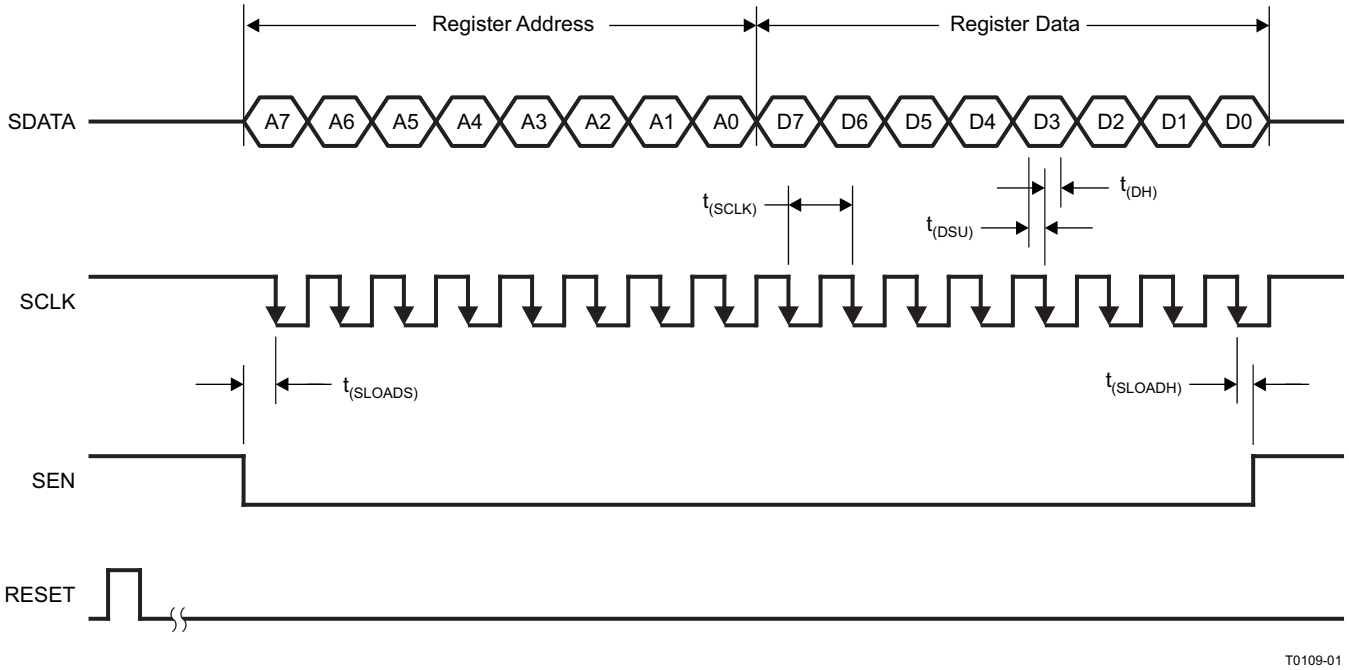


Figure 6. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, DRVDD = 1.8 V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1/ t_{SCLK})	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DS}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

Serial Register Readout

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

a. First, set register bit **<READOUT>** = 1 to put the device in serial readout mode. This disables any further writes into the registers, EXCEPT the register at address 0. Note that the **<READOUT>** bit is also located in register 0. The device can exit readout mode by writing **<READOUT>** to 0.
b. Also, only the contents of register at address 0 cannot be read in the register readout mode
c. Initiate a serial interface cycle specifying the address of the register (A7 – A0) whose content has to be read.
d. The device outputs the contents (D15 – D0) of the selected register on the SDOUT pin
e. The external controller can latch the contents at the falling edge of SCLK.
f. To enable register writes, reset register bit **<READOUT>** = 0.

The serial register readout works with CMOS and LVDS interfaces.

When **<READOUT>** is disabled, SDOUT pin is in high-impedance state.

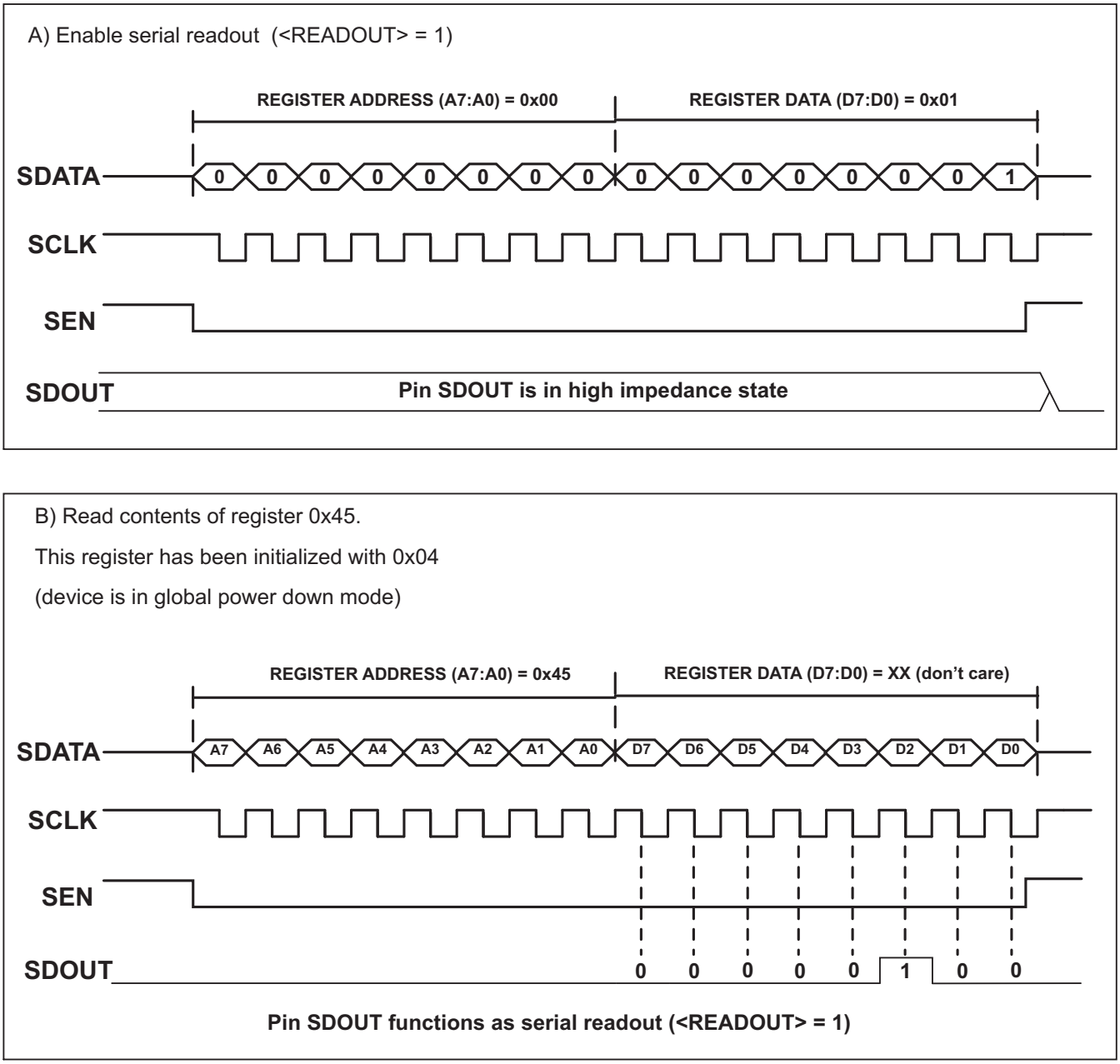
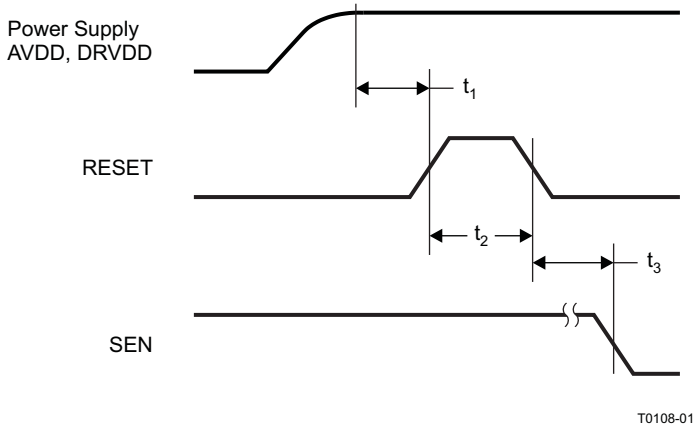


Figure 7. Serial Readout

RESET TIMING

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset.

Figure 8. Reset Timing Diagram

SERIAL REGISTER MAP

Table 7. Summary of Functions Supported by Serial Interface(1) (2)

REGISTER ADDRESS	REGISTER DATA							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	<RESET>	<READOUT>
01	<LVDS SWING>						0	0
25	<GAIN CH B>				0	<TEST PATTERNS – CH B>		
26	0	<*CH B* SNRBoost FILTER #>						
28	0	<SNRBoost *CH B* ON>	0	0	0	0	0	0
29	0	0	0	<DATA FORMAT CH A CH B>		0	0	0
2B	<GAIN CH A>				0	<TEST PATTERNS – CH A>		
2D	0	<*CH A* SNRBoost FILTER #>						
2E	0	<SNRBoost *CH A* ON>	0	0	0	0	0	0
31	<GAIN CH C>				0	<TEST PATTERNS – CH C>		
32	0	<*CH C* SNRBoost FILTER #>						
34	0	<SNRBoost *CH C* ON>	0	0	0	0	0	0
35	0	0	0	<DATA FORMAT CH C CH D>		0	0	0
37	<GAIN CH D>				0	<TEST PATTERNS – CH D>		
39	0	<*CH D* SNRBoost FILTER #>						
3A	0	<SNRBoost *CH D* ON>	0	0	0	0	0	0
3D	0	0	<EN OFFSET CORR>	0	0	0	0	0
3F	0	0	<CUSTOM PATTERN HIGH D10:D5>					
40	<CUSTOM PATTERN D4:D0>					0	0	0
41	<LVDS CMOS>		<CMOS CLKOUT STRENGTH>		0	0	<PDN OBUF LVDS>	
42	<CLKOUT FALL POSN>		<CLKOUT RISE POSN>		<DIGITAL MODE 1>	<PDN OBUF CMOS>		0
44	0	0	0	0	0	0	0	<DIGITAL MODE 2>
45	<STBY>	<LVDS CLKOUT STRENGTH>	<LVDS DATA STRENGTH>	0	0	<PDN GLOBAL>	0	<CONFIG PDN Pin>
BF	<OFFSET PEDESTAL – *CH B*>			0	0	0	0	0
C1	<OFFSET PEDESTAL – *CH A*>			0	0	0	0	0
C3	<OFFSET PEDESTAL – *CH C*>			0	0	0	0	0
C5	<OFFSET PEDESTAL – *CH D*>			0	0	0	0	0
CF	<FREEZE OFFSET CORR>	0	<OFFSET CORR TIME CONSTANT>				0	0
EA	<OVERRIDE SNRB pins>	0	0	0	0	0	0	0
F1	0	0	0	0	0	0	<EN LVDS SWING>	
03	0	0	0	0	0	0	<HIGH PERF MODE>	

(1) All registers default to zeros after reset.
(2) Multiple functions in a register can be programmed in a single write operation.

Table 7. Summary of Functions Supported by Serial Interface (1) (2) (continued)

REGISTER ADDRESS	REGISTER DATA							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
4A	0	0	0	0	0	0	0	<HIGH FREQ MODE CH B>
58	0	0	0	0	0	0	0	<HIGH FREQ MODE CH A>
66	0	0	0	0	0	0	0	<HIGH FREQ MODE CH C>
74	0	0	0	0	0	0	0	<HIGH FREQ MODE CH D>

DESCRIPTION OF SERIAL REGISTERS

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
00	00	0	0	0	0	0	0	**<RESET>**	**<READOUT>**

D1 **<RESET>**

1 Software reset applied – resets all internal registers to their default values and self-clears to 0.

D0 **<READOUT>**

0 Serial readout of registers is disabled. Pin SDOUT is put in high-impedance state.

1 Serial readout is enabled. Pin SDOUT functions as serial data readout with CMOS logic levels, running off DRVDD supply.
See Serial Register Readout section.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
01	00	**<LVDS SWING>**						0	0

D7-D2 **<LVDS SWING>** LVDS swing programmability

000000 Default LVDS swing; ±350mV with external 100-Ω termination

011011 LVDS swing increases to ±410mV

110010 LVDS swing increases to ±465mV

010100 LVDS swing increases to ±570mV

111110 LVDS swing decreases to ±200mV

001111 LVDS swing decreases to ±125mV

Other combinations Do not use

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
25	00	**<GAIN CH B>**				0	**<TEST PATTERNS – CH B>**		

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
26	00	0	**<CHB SNRBoost FILTER #>**						

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
28	00	0	**<SNRBoost CH B ON>**	0	0	0	0	0	0

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
29	00	0	0	0	<DATA FORMAT CH A CH B>		0	0	0

D4-D3	<DATA FORMAT CH A CH B>
00	Both channels in 2s complement
01	Both channels in 2s complement
10	Both channels in 2s complement
11	Both channels in offset binary

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
2B	00	<GAIN CH A>				0	<TEST PATTERNS – CH A>		

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
2D	00	0	<CHA SNRBoost FILTER #>						

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
2E	00	0	<SNRBoost CH A ON>	0	0	0	0	0	0

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
31	00	<GAIN CH C>				0	<TEST PATTERNS – CH C>		

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
32	00	0	<CHC SNRBoost FILTER #>						

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
34	00	0	<SNRBoost CH C ON>	0	0	0	0	0	0

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
35	00	0	0	0	<DATA FORMAT CH C CH D>		0	0	0

D4-D3 **<DATA FORMAT CH C CH D>**

00 Both channels in 2s complement

01 Both channels in 2s complement

10 Both channels in 2s complement

11 Both channels in offset binary

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
37	00	<GAIN CH D>				0	<TEST PATTERNS – CH D>		

D7-D4 **<GAIN>** Gain programmability in 0.5 dB steps for channels A,B,C,D

0000 0 dB gain, default after reset

0001 0.5 dB gain

0010 1.0 dB gain

0011 1.5 dB gain

0100 2.0 dB gain

0101 2.5 dB gain

0110 3.0 dB gain

0111 3.5 dB gain

1000 4.0 dB gain

1001 4.5 dB gain

1010 5.0 dB gain

1011 5.5 dB gain

1100 6 dB gain

D2-D0 **<TEST PATTERNS – CH X>** Test Patterns to verify data capture for channels A, B, C, D
ONLY when register bit DIGITAL MODE1 is set

000 Normal operation

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern
Output data <D10:D0> is an alternating sequence of 10101010101 and 01010101010.

100 Outputs digital pattern
Output data increments by one LSB (11-bit) every 8th clock cycle from code 0 to code 2047

101 Outputs custom pattern
(use registers 0x3F, 0x40 for setting the custom pattern)

110 Unused

111 Unused

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
39	00	0	<CHD SNRBoost FILTER #>						

D6-D0 **<CH X SNRBoost FILTER #>** Select any one of 55 SNRBoost filters for channel X,
Refer to Digital Functions Control Bits

Refer to section SNR ENHANCEMENT USING SNRBOOST

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
3A	00	0	<SNRBoost CH D ON>	0	0	0	0	0	0

D6 **<SNRBoost CH X ON>**

0 SNRBoost for channel A,B,C,D is OFF

1 SNRBoost for channel A,B,C,D is ON

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
3D	00	0	0	<EN OFFSET CORR>	0	0	0	0	0

D5 **<EN OFFSET CORR>** *ONLY when register bit DIGITAL MODE1 is set*

0 Offset correction disabled

1 Offset correction enabled

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
3F	00	0	0	<CUSTOM PATTERN D10:D5>					
40	00	<CUSTOM PATTERN D10:D5>					0	0	0

D5-D0 **<CUSTOM PATTERN D10:D5>**

6 Upper bits of custom pattern available at output instead of ADC data

D7-D3 **<CUSTOM PATTERN D4:D0>**

5 Lower bits of custom pattern available at output instead of ADC data

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
41	00	<LVDS CMOS>		<CMOS CLKOUT STRENGTH>		0	0	<PDN OBUF LVDS>	

D7-D6 <LVDS CMOS>

00 LVDS interface

01 CMOS interface

10 CMOS interface

11 CMOS interface

D5-D4 <CMOS CLKOUT STRENGTH>

00 Maximum strength (recommended and used for specified timings)

01 Medium strength

10 Low strength

11 Very low strength

D1-D0 <PDN OBUF LVDS>

00 LVDS data buffers enabled for all channels

01 LVDS data buffers powered down and output 3-stated for channel A and channel D

10 LVDS data buffers powered down and output 3-stated for channel B and channel C

11 LVDS data buffers powered down and output 3-stated for all channels including the LVDS output clock buffer

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
42	00	<CLKOUT FALL POSN>		<CLKOUT RISE POSN>		<DIGITAL MODE 1>	<PDN OBUF CMOS>		0

D7-D6 <CLKOUT FALL POSN>

00 Default position (timings are specified in this condition)

01 Setup increases by 450 ps, hold decreases by 450 ps

10 Setup decreases by 300 ps, Hold increases by 300 ps
In this setting, the bit order is swapped compared to default case.
For example, default order is [CLKOUTP fall-D1, CLKOUTP rise –D2]. In this setting, the order becomes [CLKOUTP fall-D2, CLKOUTP rise –D1]

11 Setup increases by 1.0 ns, Hold decreases by 1.0 ns

D5-D4 <CLKOUT RISE POSN>

00 Default position (timings are specified in this condition)

01 Setup increases by 550 ps, hold decreases by 550 ps

10 Setup increases by 600 ps, Hold decreases by 600 ps
In this setting, the bit order is swapped compared to default case.
For example, default order is [CLKOUTP fall-D1, CLKOUTP rise –D2] In this setting, the order becomes [CLKOUTP fall-D2, CLKOUTP rise –D1]

11 Setup increases by 1.1 ns, Hold decreases by 1.1 ns

D3 **<DIGITAL MODE 1>**

Refer to section SNR ENHANCEMENT USING SNRBOOST

D2-D1 **<PDN OBUF CMOS>(1)**

00 CMOS data buffers enabled for all channels

01 CMOS data buffers powered down and output 3-stated for channel A and channel D

10 CMOS data buffers powered down and output 3-stated for channel B and channel C

11 CMOS data buffers powered down and output 3-stated for all channels

1. With CMOS interface, to power down the output clock CLKOUT, set the bits <PDN OBUF LVDS> = 11

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
44	00	0	0	0	0	0	0		**<DIGITAL MODE 2>**
EA	00	**<OVERRIDE SNRB pins>**	0	0	0	0	0	0	0
F1	00	0	0	0	0	0	0	**<EN LVDS SWING>**	

Refer to section SNR ENHANCEMENT USING SNRBOOST

D1-D0 **<EN LVDS SWING>**Enable LVDS swing control using the <LVDS SWING> bits

00 LVDS swing control using LVDS SWING register bits is disabled

01, 10 Do not use

11 LVDS swing control using LVDS SWING register bits is enabled

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
45	00	**<STBY>**	**<LVDS CLKOUT STRENGTH>**	**<LVDS DATA STRENGTH>**	0	0	**<PDN GLOBAL>**	0	**<CONFIG PDN Pin>**

D0 **<CONFIGURE PDN Pin>**

0 PDN pin functions as STBY control pin.

1 PDN pin functions as Global Power down control pin.

D2 **<PDN GLOBAL>**

0 Normal operation

1 Total power down – All channel ADCs, internal references and output buffers are powered down. Wake-up time from this mode is slow, typically, 100 µsec.

D5 **<LVDS DATA STRENGTH>**

0 All LVDS data buffers have default strength to be used with 100-Ω external termination

1 All LVDS data buffers have ***double*** strength to be used with 50-Ω external termination

D6 **<LVDS CLKOUT STRENGTH>**

0 LVDS output clock buffer has default strength to be used with 100-Ω external termination

1 LVDS output clock buffer has ***double*** strength to be used with 50-Ω external termination

D7 <STBY>

0 Normal operation

1 All 4 channels are put in standby. Wake-up time from this mode is fast, typically 10 µsec

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
BF	00	<OFFSET PEDESTAL – CH B>			0	0	0	0	0
C1	00	<OFFSET PEDESTAL – CH A>			0	0	0	0	0
C3	00	<OFFSET PEDESTAL – CH C>			0	0	0	0	0
C5	00	<OFFSET PEDESTAL – CH D>			0	0	0	0	0

D7-D5 <OFFSET PEDESTAL – CH X> When the offset correction is enabled, the final converged value after the offset is corrected will be the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits. Refer to the OFFSET CORRECTION section in Application Information. Channels can be independently programmed for different offset pedestal by choosing relevant register address.

011 PEDESTAL = 3 LSB

010 PEDESTAL = 2 LSB

001 PEDESTAL = 1 LSB

000 PEDESTAL = 0 LSB

111 PEDESTAL = –1 LSB

110 PEDESTAL = –2 LSB

101 PEDESTAL = –3 LSB

100 PEDESTAL = –4 LSB

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
CF	00	<FREEZE OFFSET CORR>	0	<OFFSET CORR TIME CONSTANT>				0	0

D7 <FREEZE OFFSET CORR> This bit sets the freeze offset correction.

0 Estimation of offset correction is not frozen (bit <EN OFFSET CORR> must be set)

1 Estimation of offset correction is frozen (bit <EN OFFSET CORR> must be set). When frozen, the last estimated value is used for offset correction every clock cycle. Refer to the OFFSET CORRECTION section.

D5-D2 <OFFSET CORR TIME CONSTANT> Offset correction loop time constant in number of clock cycles. Refer to the OFFSET CORRECTION section.

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
03	00	0	0	0	0	0	0	<HIGH PERF MODE>	

D1-D0 <HIGH PERF MODE>

00 Default performance after reset

01 Do not use

10 Do not use

11 To get best performance across sample clock and input signal frequencies, set the <HIGH PERF MODE> bits

ADDRS A7-A0 IN HEX	DEFAULT VALUE AFTER RESET	D7	D6	D5	D4	D3	D2	D1	D0
4A	00	0	0	0	0	0	0	0	<HIGH FREQ MODE CH B>
58	00	0	0	0	0	0	0	0	<HIGH FREQ MODE CH A>
66	00	0	0	0	0	0	0	0	<HIGH FREQ MODE CH C>
74	00	0	0	0	0	0	0	0	<HIGH FREQ MODE CH D>

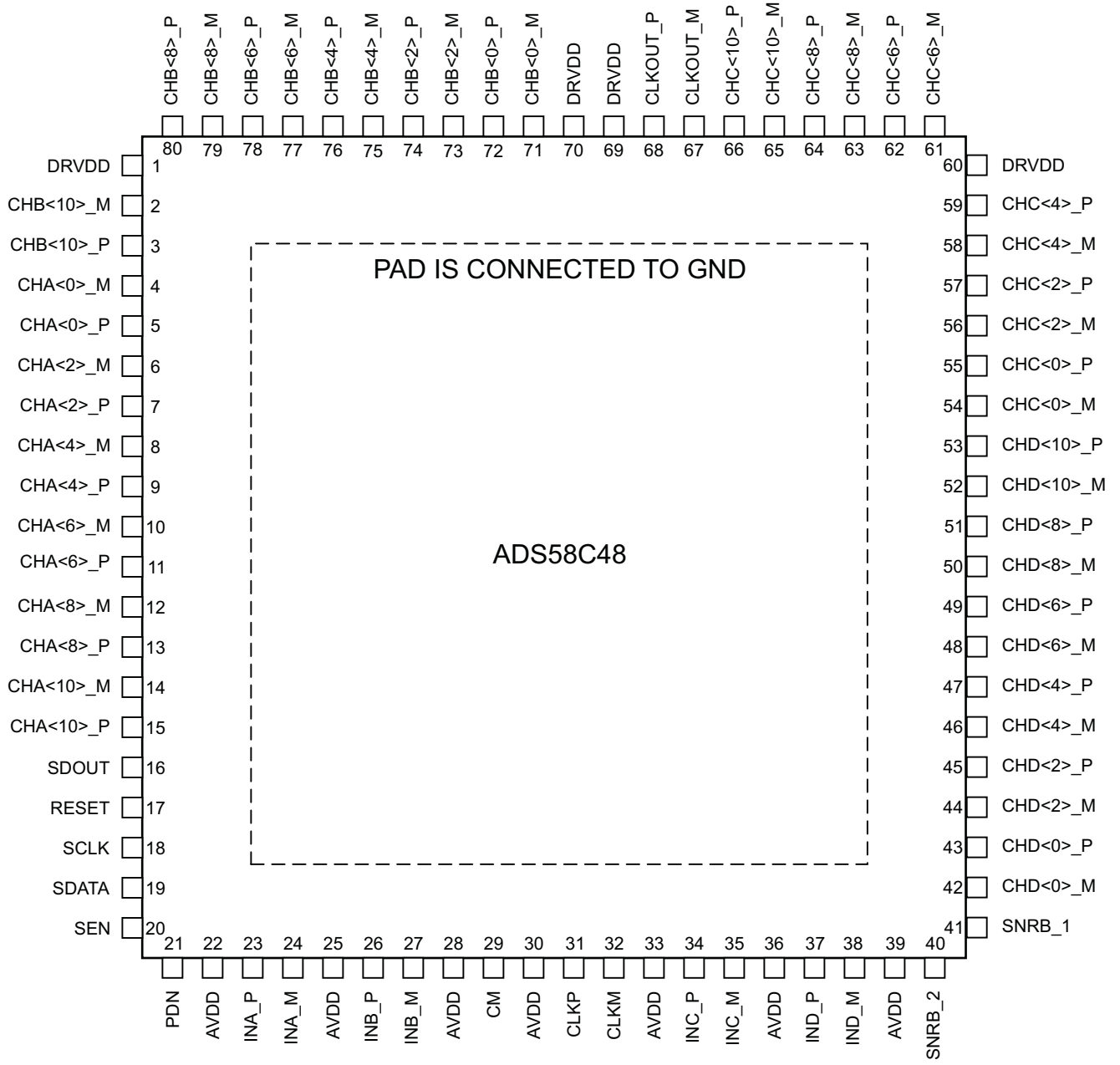
D0 <HIGH FREQ MODE CHx> This bit is recommended for high input signal frequencies greater than 200 MHz.

0 Default performance after reset

1 For high frequency input signals, set the HIGH FREQ MODE bits for each channel

DEVICE INFORMATION

PIN CONFIGURATION (LVDS MODE)



P0027-05

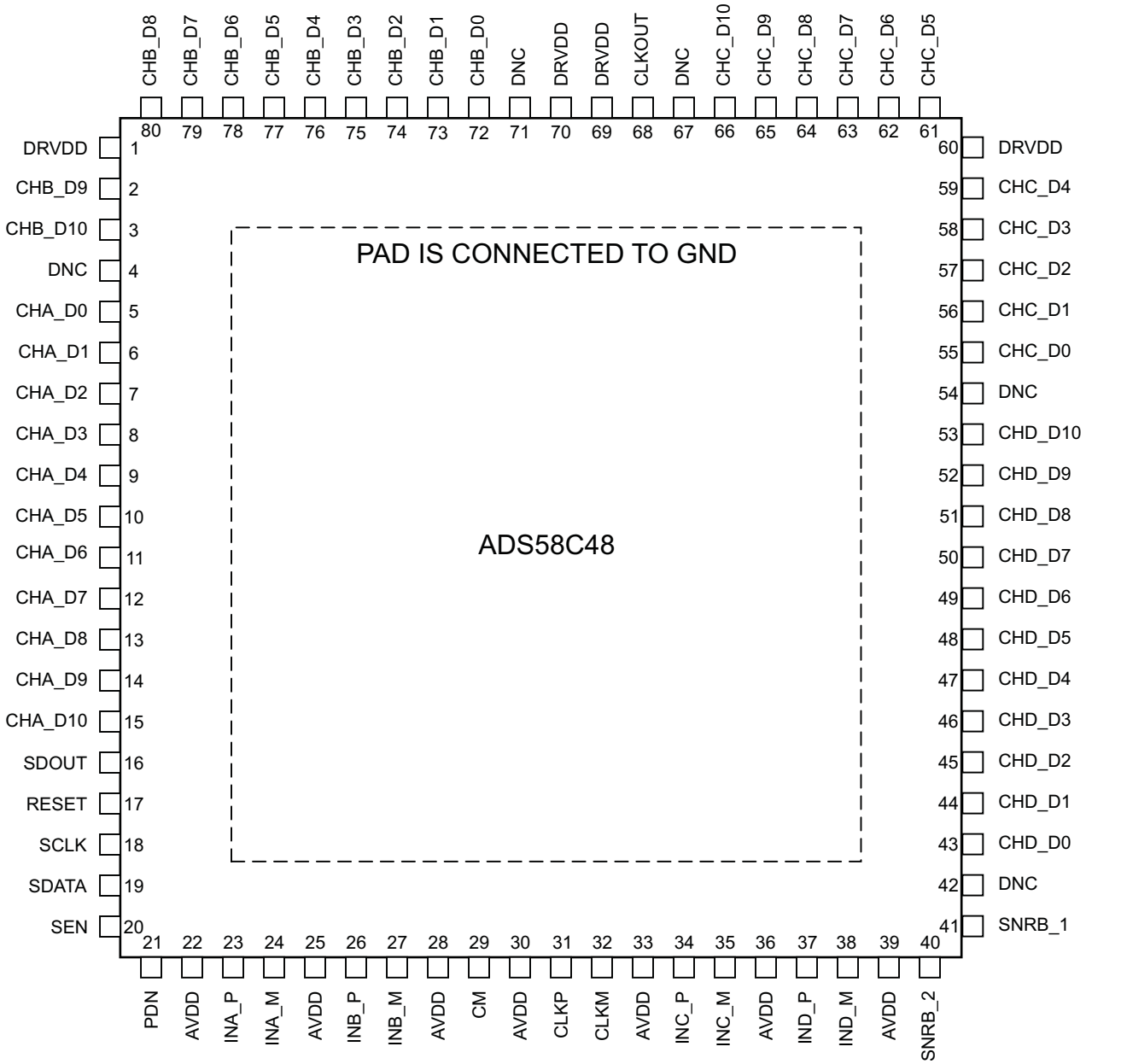
PIN ASSIGNMENTS (LVDS INTERFACE)

PIN NAME	DESCRIPTION	PIN		NUMBER OF PINS
		TYPE	NUMBER	
AVDD	1.8 V, analog power supply	I	22, 25, 28, 30, 33, 36, 39	7
CLKP, CLKM	Differential clock input	I	31, 32	2

PIN NAME	DESCRIPTION	PIN		NUMBER OF PINS
		TYPE	NUMBER	
INA_P, INA_M	Differential analog input, Channel A	I	23, 24	2
INB_P, INB_M	Differential analog input, Channel B	I	26, 27	2
INC_P, INC_M	Differential analog input, Channel C	I	34, 35	2
IND_P, IND_M	Differential analog input, Channel D	I	37, 38	2
CM	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.	O	29	1
RESET	Serial interface RESET input. The user ***must*** initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to SERIAL INTERFACE section. The pin has an internal 100kΩ pull-down resistor.	I	17	1
SCLK	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.	I	18	1
SDATA	Serial interface data input. The pin has an internal 100-kΩ pull-down resistor.	I	19	1
SEN	Serial interface enable input. The pin has an internal 100-kΩ pull-up resistor to DRVDD	I	20	1
SDOUT	This pin functions as serial interface register readout, when the **<READOUT>** bit is enabled. When **<READOUT>** = 0, this pin is put in high impedance state.It is a CMOS output pin running off DRVDD supply.	O	16	1
PDN	Power down control pin. The pin has an internal 150-kΩ pull-down resistor to DRGND.	I	21	1
SNRB_1, SNRB_2	*SNRBoost* ^{3G} control pins. Each pin has an internal 150-kΩ pull-down resistor to DRGND.	I	41, 40	2
DRVDD	1.8 V, digital supply	I	1, 60, 69, 70	
CLKOUTP, CLKOUTM	Differential output clock	O	68, 67	2
CHA<0>_P, CHA<0>_M	Differential output data pair, '0' and D0 multiplexed – Channel A	O	5,4 Refer to Figure 9	2
CHA<2>_P, CHA<2>_M	Differential output data D1 and D2 multiplexed, true – Channel A	O	7,6	2
CHA<4>_P, CHA<4>_M	Differential output data D3 and D4 multiplexed, true – Channel A	O	9,8	2
CHA<6>_P, CHA<6>_M	Differential output data D5 and D6 multiplexed, true – Channel A	O	11,10	2
CHA<8>_P, CHA<8>_M	Differential output data D7 and D8 multiplexed, true – Channel A	O	13,12	2
CHA<10>_P, CHA<10>_M	Differential output data D9 and D10 multiplexed, true – Channel A	O	15,14	2
CHB<0>_P, CHB<0>_M	Differential output data pair, '0' and D0 multiplexed – Channel B	O	72,71	2
CHB<2>_P, CHB<2>_M	Differential output data D1 and D2 multiplexed, true – Channel B	O	74,73	2
CHB<4>_P, CHB<4>_M	Differential output data D3 and D4 multiplexed, true – Channel B	O	76,75	2
CHB<6>_P, CHB<6>_M	Differential output data D5 and D6 multiplexed, true – Channel B	O	78,77	2
CHB<8>_P, CHB<8>_M	Differential output data D7 and D8 multiplexed, true – Channel B	O	80,79	2
CHB<10>_P, CHB<10>_M	Differential output data D9 and D10 multiplexed, true – Channel B	O	3,2	2
CHC<0>_P, CHC<0>_M	Differential output data pair, '0' and D0 multiplexed – Channel C	O	55,54	2

PIN NAME	DESCRIPTION	PIN		NUMBER OF PINS
		TYPE	NUMBER	
CHC<2>_P, CHC<2>_M	Differential output data D1 and D2 multiplexed, true – Channel C	O	57,56	2
CHC<4>_P, CHC<4>_M	Differential output data D3 and D4 multiplexed, true – Channel C	O	59,58	2
CHC<6>_P, CHC<6>_M	Differential output data D5 and D6 multiplexed, true – Channel C	O	62,61	2
CHC<8>_P, CHC<8>_M	Differential output data D7 and D8 multiplexed, true – Channel C	O	64,63	2
CHC<10>_P, CHC<10>_M	Differential output data D9 and D10 multiplexed, true – Channel C	O	66,65	2
CHD<0>_P, CHD<0>_M	Differential output data pair, '0' and D0 multiplexed – Channel D	O	43,42	2
CHD<2>_P, CHD<2>_M	Differential output data D1 and D2 multiplexed, true – Channel D	O	45,44	2
CHD<4>_P, CHD<4>_M	Differential output data D3 and D4 multiplexed, true – Channel D	O	47,46	2
CHD<6>_P, CHD<6>_M	Differential output data D5 and D6 multiplexed, true – Channel D	O	49,48	2
CHD<8>_P, CHD<8>_M	Differential output data D7 and D8 multiplexed, true – Channel D	O	51,50	2
CHD<10>_P, CHD<10>_M	Differential output data D9 and D10 multiplexed, true – Channel D	O	53,52	2
PAD	MUST be connected to ground.			

PIN CONFIGURATION (CMOS INTERFACE)



P0027-06

PIN ASSIGNMENTS (CMOS MODE)

PIN NAME	DESCRIPTION	PIN		NUMBER OF PINS
		TYPE	NUMBER	
AVDD	1.8 V, analog power supply	I	22, 25, 28, 30, 33, 36, 39	7
CLKP, CLKM	Differential clock input	I	31, 32	2
INA_P, INA_M	Differential analog input, Channel A	I	23, 24	2
INB_P, INB_M	Differential analog input, Channel B	I	26, 27	2

PIN NAME	DESCRIPTION	PIN		NUMBER OF PINS
		TYPE	NUMBER	
INC_P, INC_M	Differential analog input, Channel C	I	34, 35	2
IND_P, IND_M	Differential analog input, Channel D	I	37, 38	2
CM	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.	O	29	1
RESET	Serial interface RESET input. The user ***must*** initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to SERIAL INTERFACE section. The pin has an internal 100kΩ pull-down resistor.	I	17	1
SCLK	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.	I	18	1
SDATA	Serial interface data input. The pin has an internal 100-kΩ pull-down resistor.	I	19	1
SEN	Serial interface enable input. The pin has an internal 100-kΩ pull-up resistor to DRVDD	I	20	1
SDOUT	This pin functions as serial interface register readout, when the **<READOUT>** bit is enabled. When **<READOUT>** = 0, this pin is put in high impedance state.It is a CMOS output pin running off DRVDD supply.	O	16	1
PDN	Power down control pin. The pin has an internal 150-kΩ pull-down resistor to DRGND.	I	21	1
SNRB_1, SNRB_2	*SNRBoost* ^{3G} control pins. Each pin has an internal 150-kΩ pull-down resistor to DRGND.	I	41, 40	2
CLKOUT	CMOS output clock	O	68	
CHA_D0 to CHA_D10	Channel A ADC output data bits, CMOS levels	O	Refer to Figure 10	11
CHB_D0 to CHB_D10	Channel B ADC output data bits, CMOS levels	O		11
CHC_D0 to CHC_D10	Channel C ADC output data bits, CMOS levels	O		11
CHD_D0 to CHD_D10	Channel D ADC output data bits, CMOS levels	O		11
DRVDD	1.8 V, digital supply	I	1,60, 69, 70	
DNC	Do not connect		4, 42, 54, 67, 71	5
PAD	MUST be connected to ground.			

TYPICAL CHARACTERISTICS

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

FFT FOR 20-MHz INPUT SIGNAL

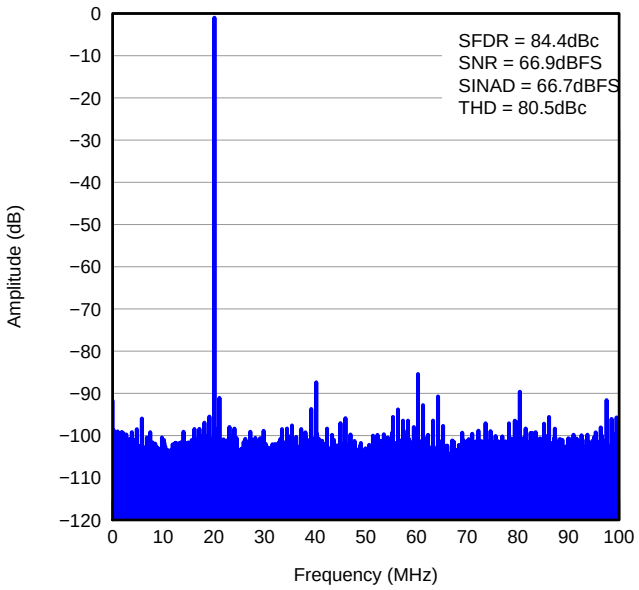


Figure 9.

FFT FOR 170-MHz INPUT SIGNAL

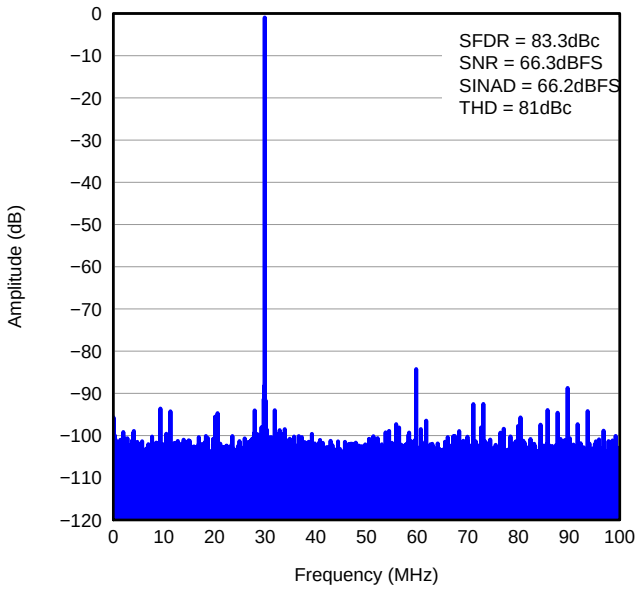


Figure 10.

FFT FOR 270-MHz INPUT SIGNAL

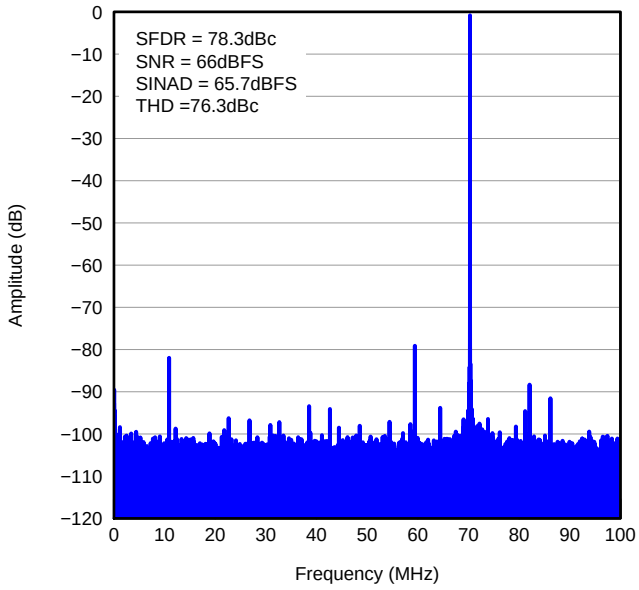


Figure 11.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

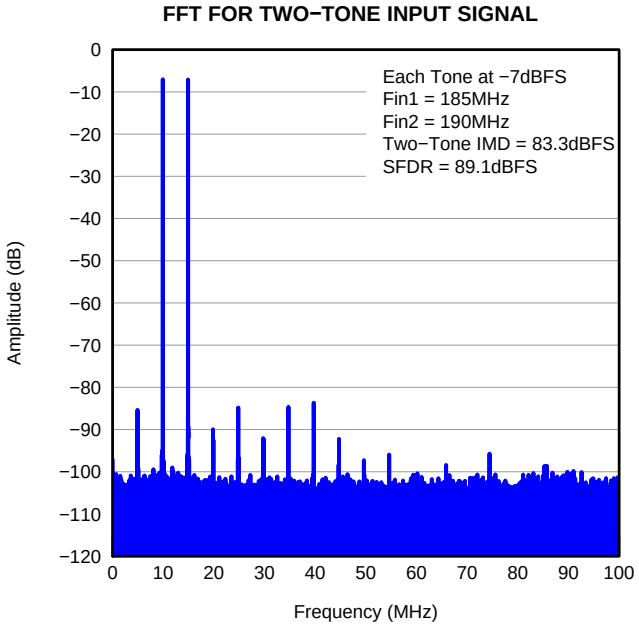


Figure 12.

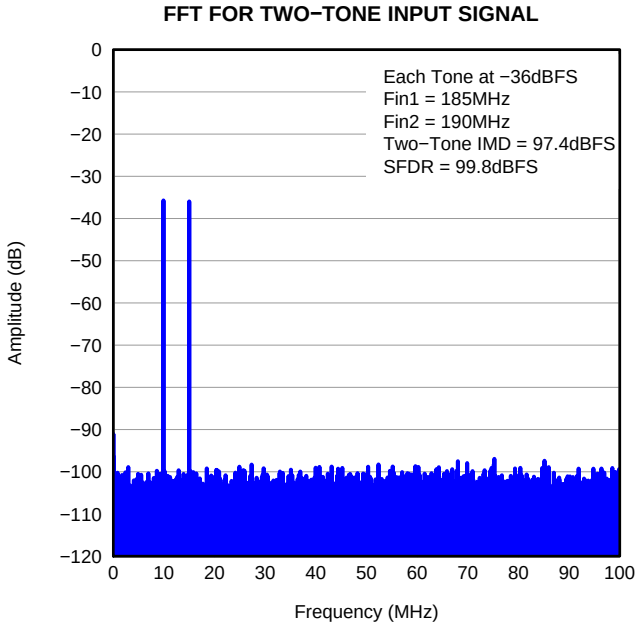


Figure 13.

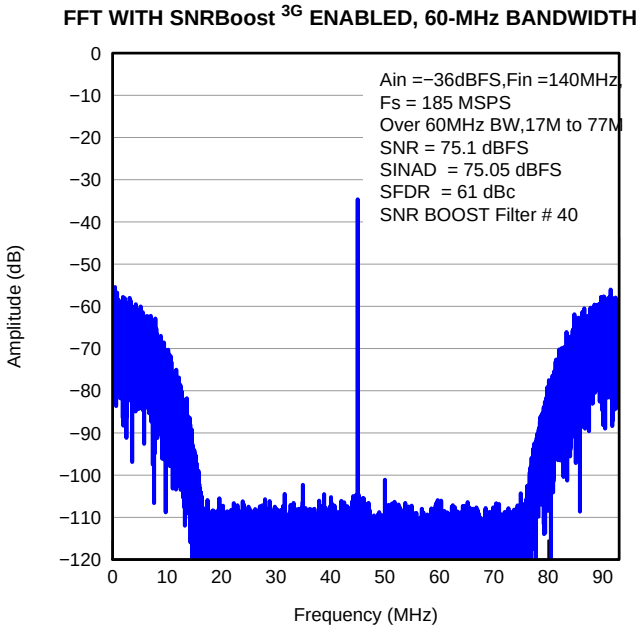


Figure 14.

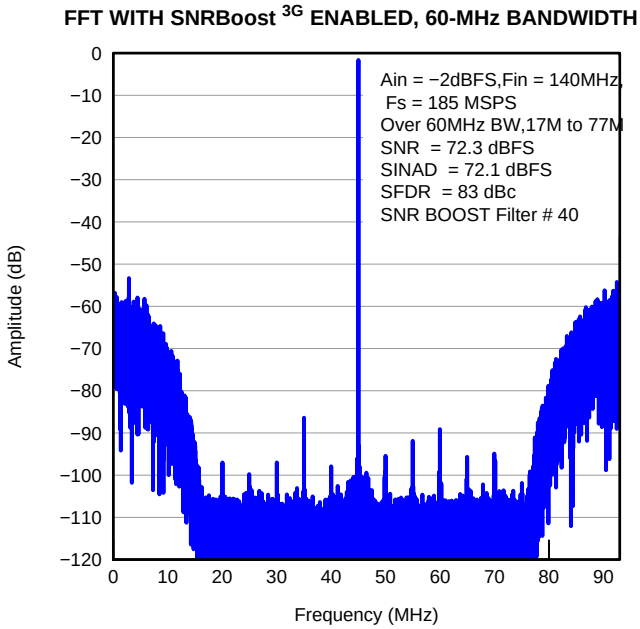


Figure 15.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

FFT WITH SNRBoost 3G ENABLED, 40-MHz BANDWIDTH

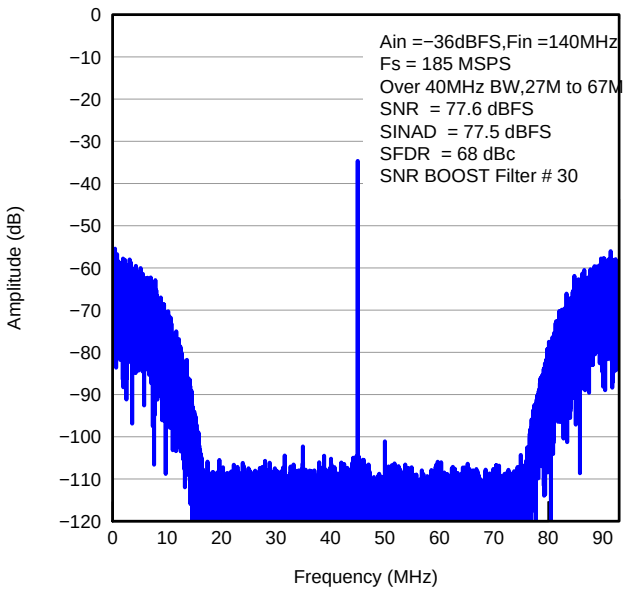


Figure 16.

FFT WITH SNRBoost 3G ENABLED, 40-MHz BANDWIDTH

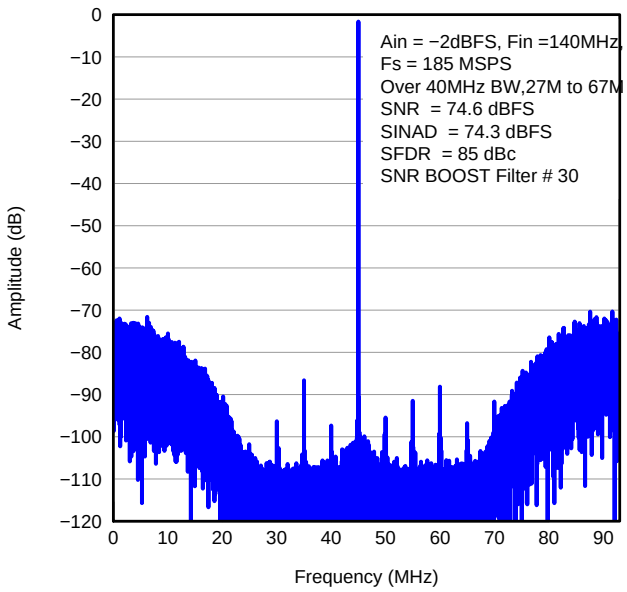


Figure 17.

FFT WITH SNRBoost 3G ENABLED, 30-MHz BANDWIDTH

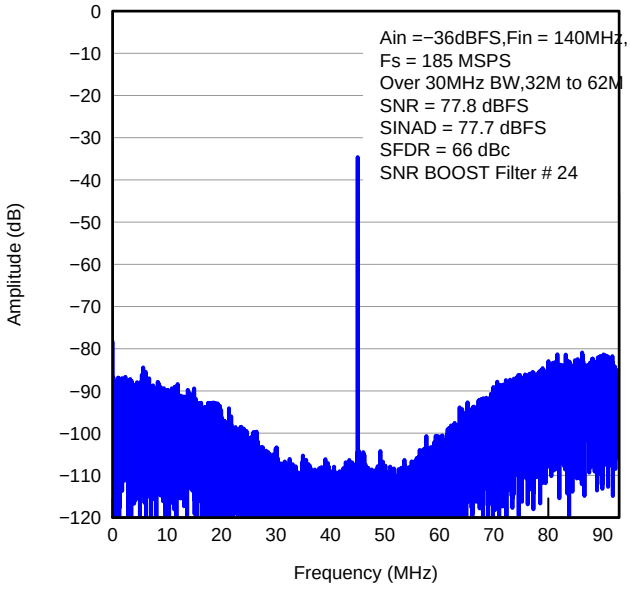


Figure 18.

FFT WITH SNRBoost 3G ENABLED, 30-MHz BANDWIDTH

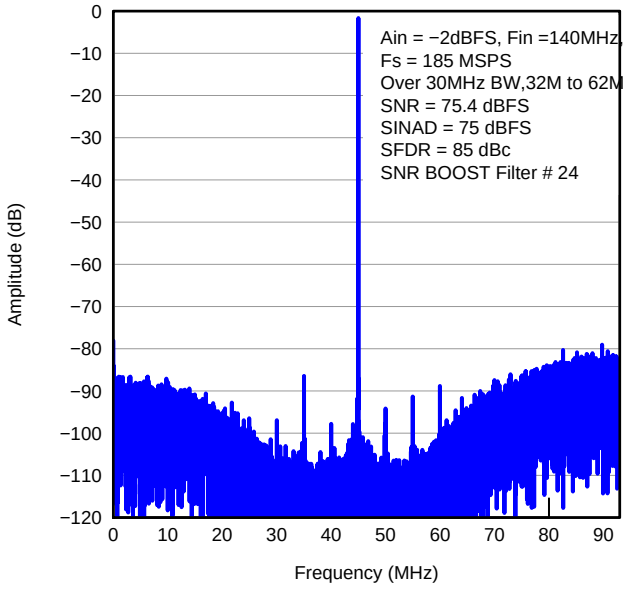


Figure 19.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

FFT WITH SNRBoost 3G ENABLED, 20-MHz BANDWIDTH

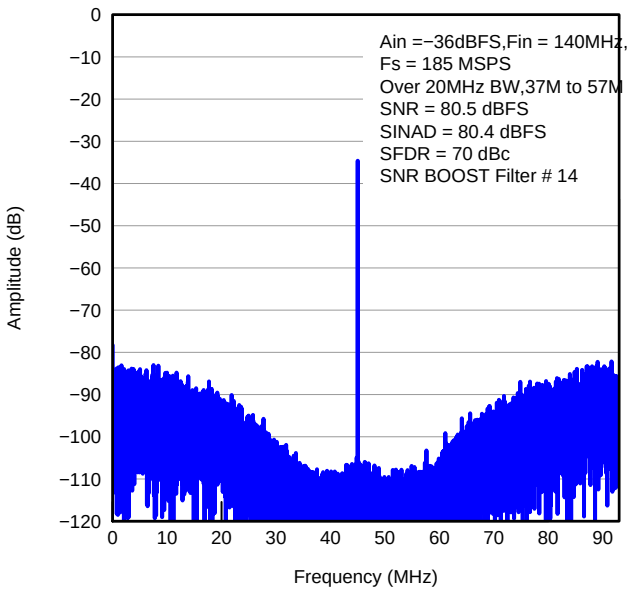


Figure 20.

FFT WITH SNRBoost 3G ENABLED, 20-MHz BANDWIDTH

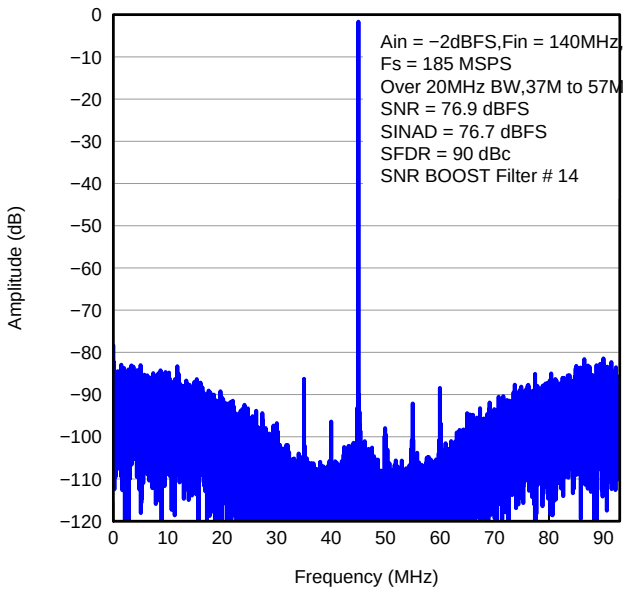


Figure 21.

TIME DOMAIN WAVEFORM OF UNWRAP SIGNAL, SNRBoost 3G DISABLED

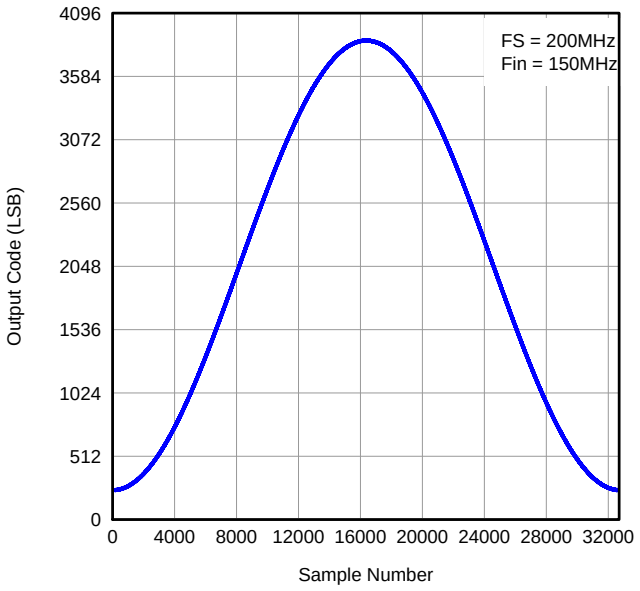


Figure 22.

TIME DOMAIN WAVEFORM OF UNWRAP SIGNAL, SNRBoost 3G ENABLED

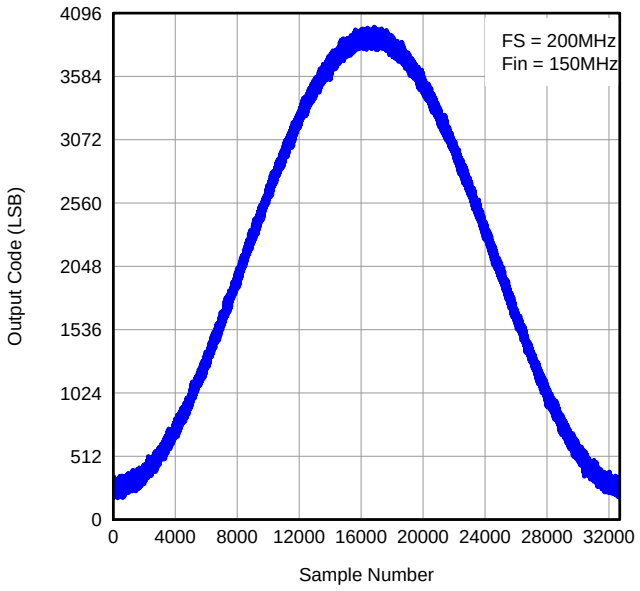


Figure 23.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

SFDR vs INPUT FREQUENCY

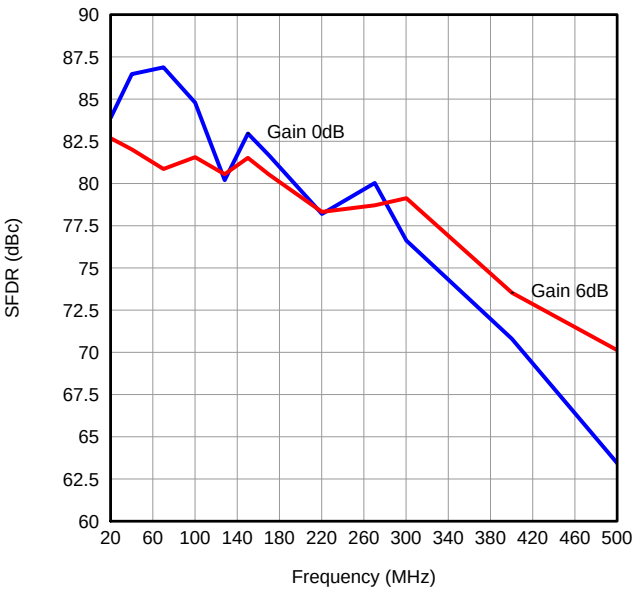


Figure 24.

SNR vs INPUT FREQUENCY

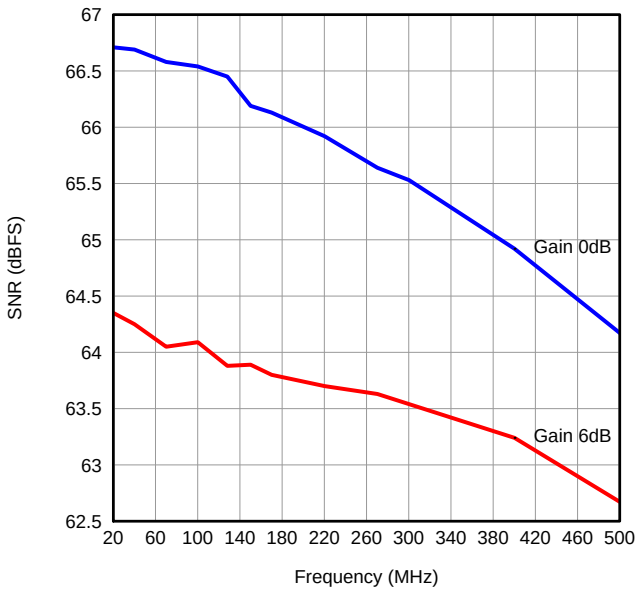


Figure 25.

SFDR vs DIGITAL GAIN

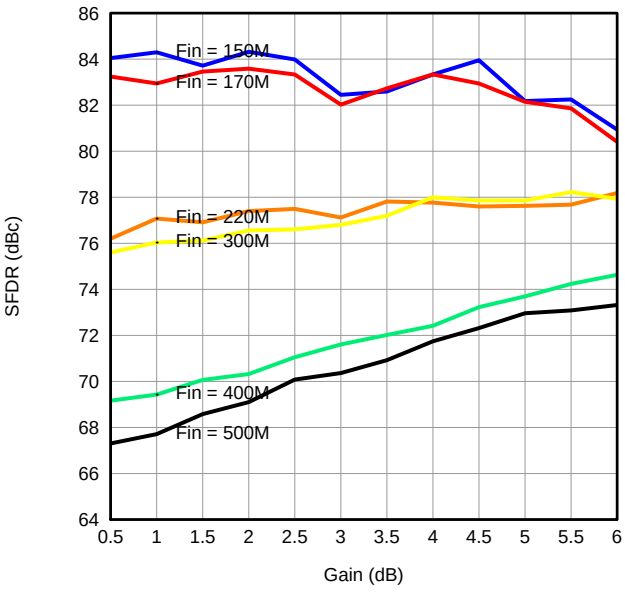


Figure 26.

SINAD vs DIGITAL GAIN

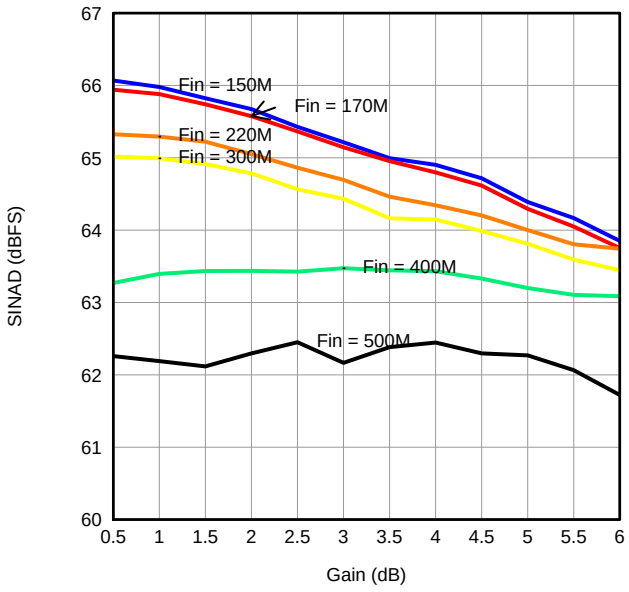


Figure 27.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

PERFORMANCE ACROSS INPUT AMPLITUDE WITH SNRBoost 3G DISABLED

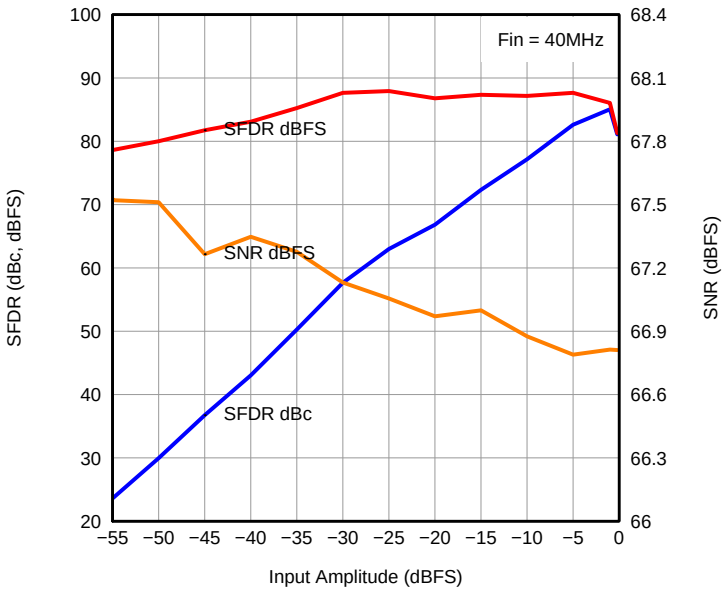


Figure 28.

PERFORMANCE ACROSS INPUT AMPLITUDE WITH SNRBoost 3G ENABLED, 60-MHz BANDWIDTH

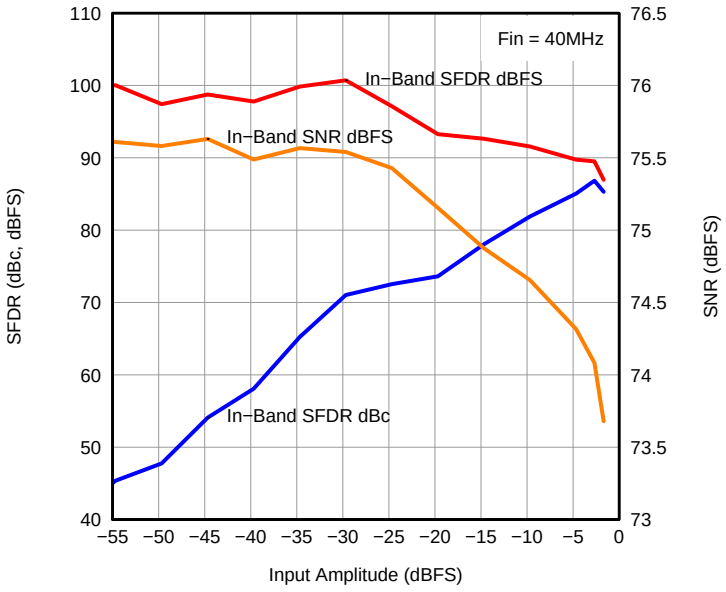


Figure 29.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

PERFORMANCE ACROSS INPUT AMPLITUDE WITH SNRBoost 3G DISABLED

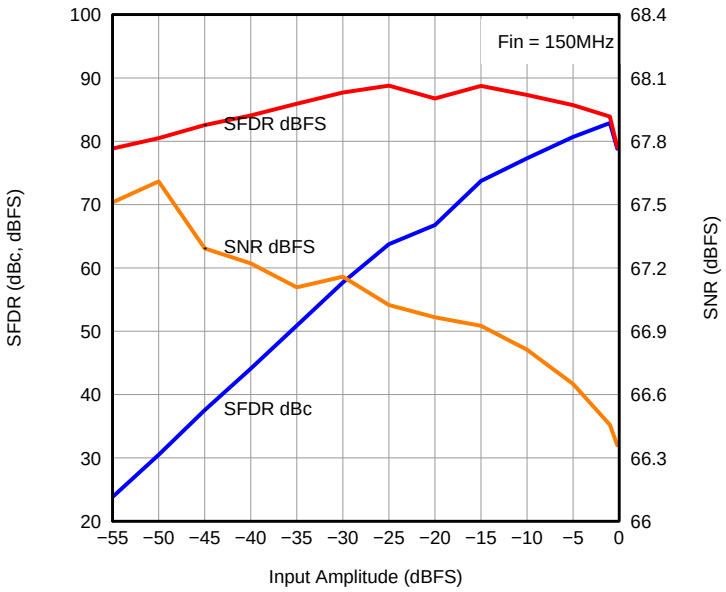


Figure 30.

PERFORMANCE ACROSS INPUT AMPLITUDE WITH SNRBoost 3G ENABLED, 60-MHz BANDWIDTH

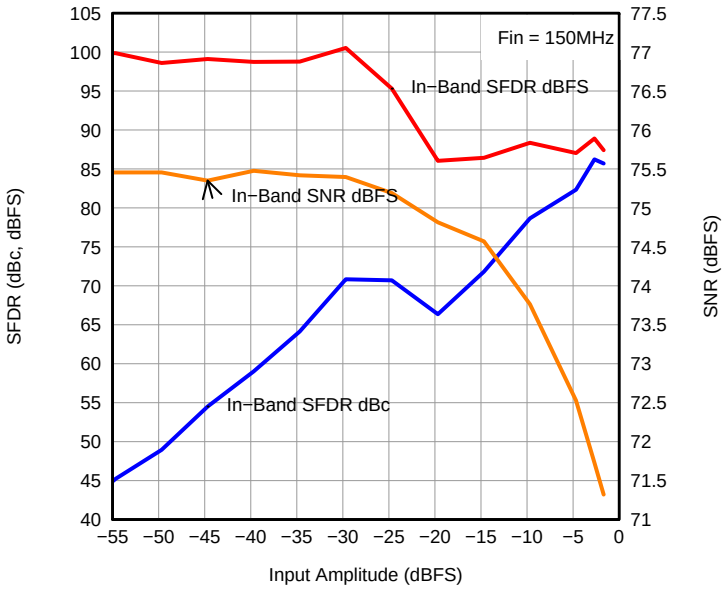


Figure 31.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

PERFORMANCE vs INPUT COMMON−MODE VOLTAGE

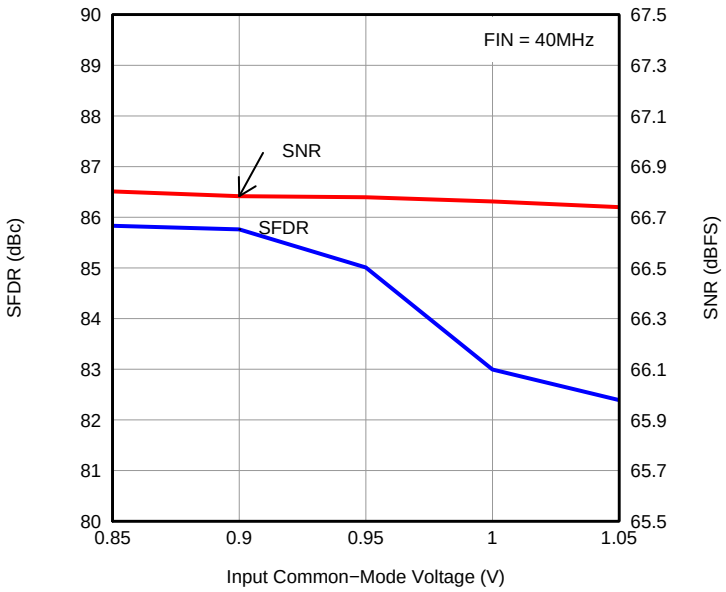


Figure 32.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

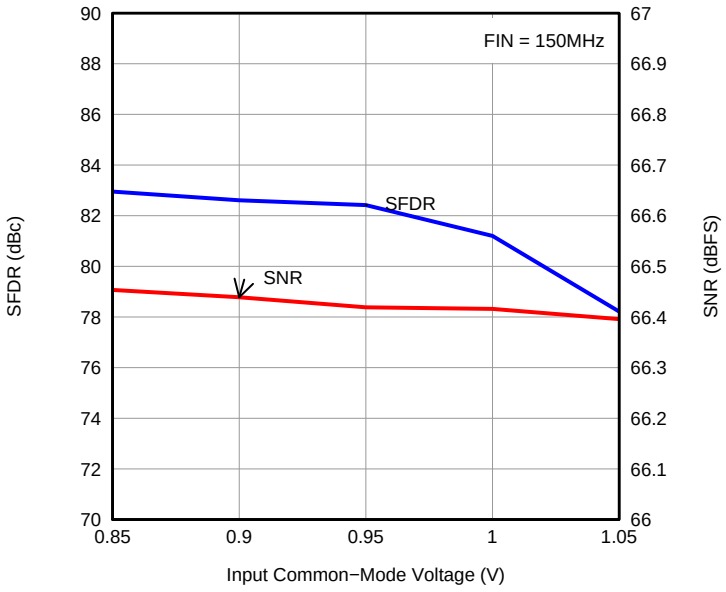


Figure 33.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

SFDR ACROSS TEMPERATURE vs AVDD SUPPLY

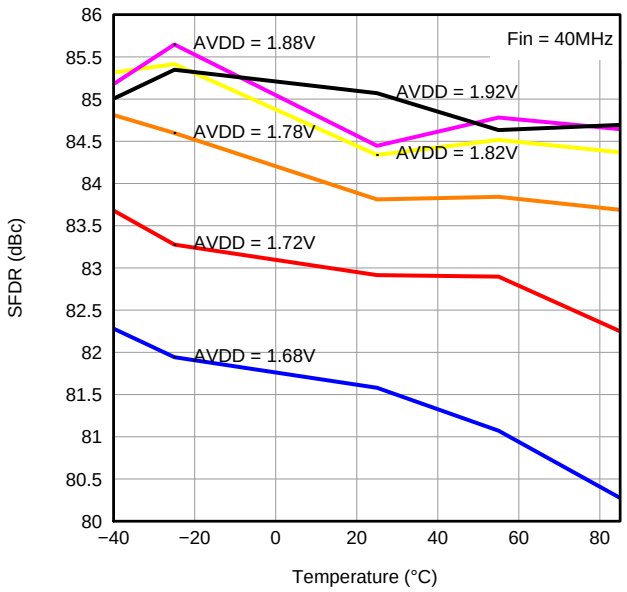


Figure 34.

SNR ACROSS TEMPERATURE vs AVDD SUPPLY

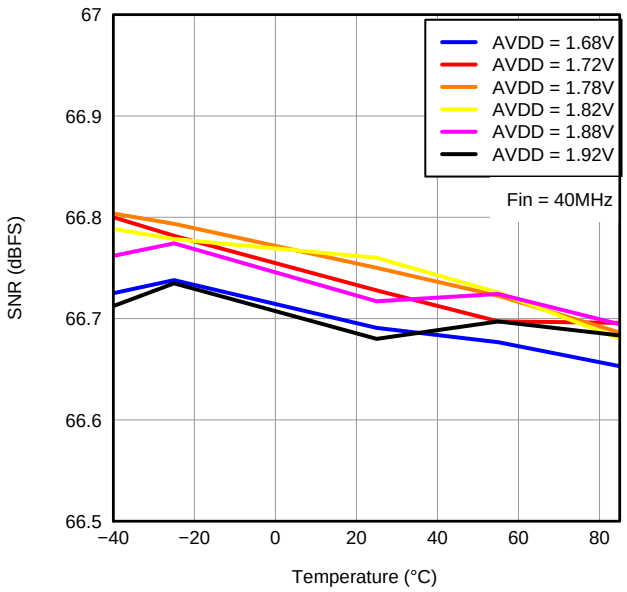


Figure 35.

PERFORMANCE ACROSS DRVDD SUPPLY VOLTAGE

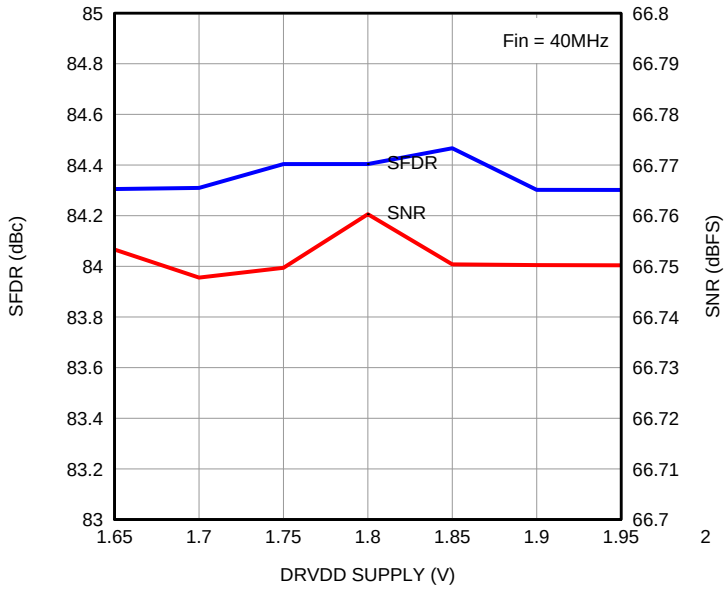


Figure 36.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

PERFORMANCE ACROSS DRVDD SUPPLY VOLTAGE (CMOS)

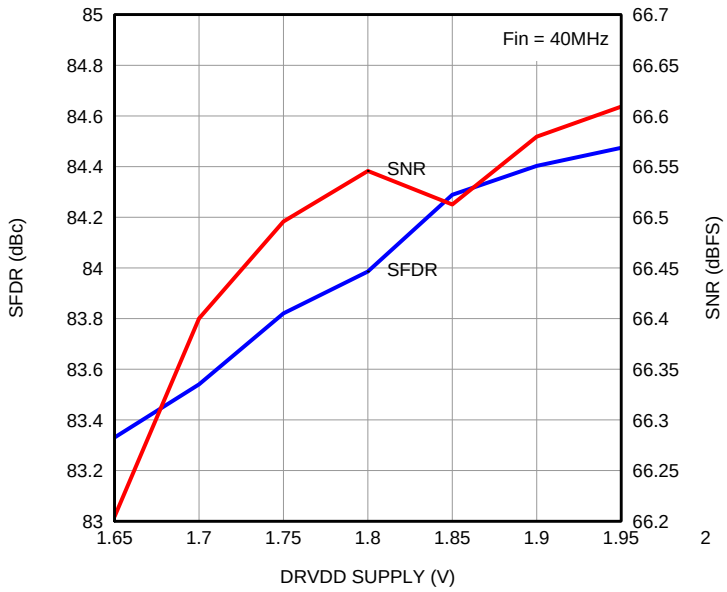


Figure 37.

SFDR vs INPUT CLOCK AMPLITUDE

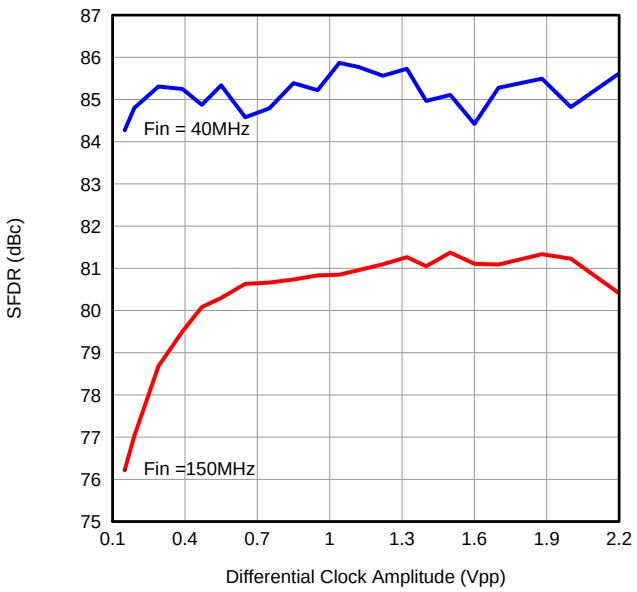


Figure 38.

SNR vs INPUT CLOCK AMPLITUDE

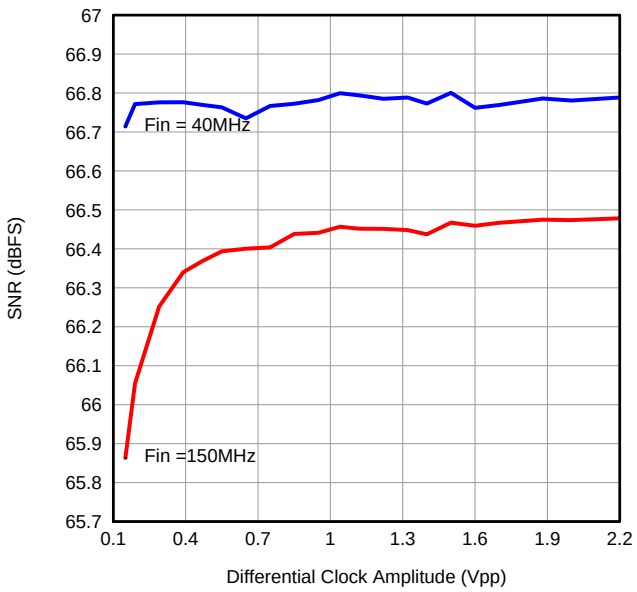


Figure 39.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

PERFORMANCE ACROSS INPUT CLOCK DUTY CYCLE

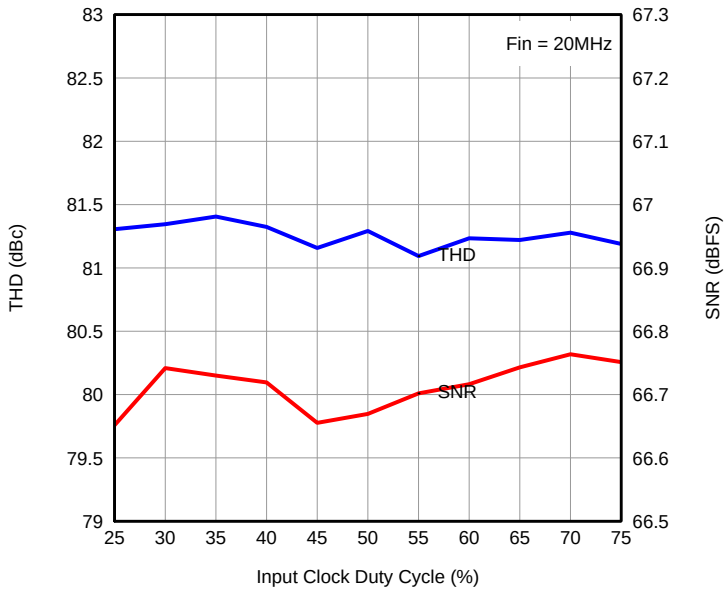


Figure 40.

ANALOG POWER vs SAMPLING FREQUENCY

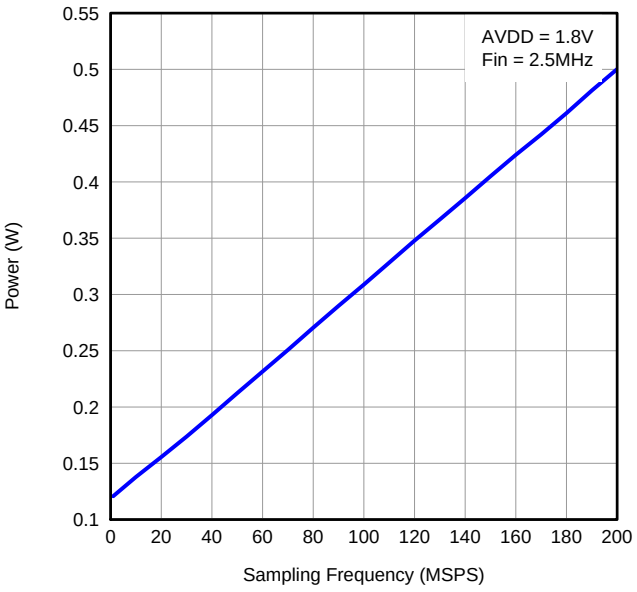


Figure 41.

DIGITAL POWER vs SAMPLING FREQUENCY

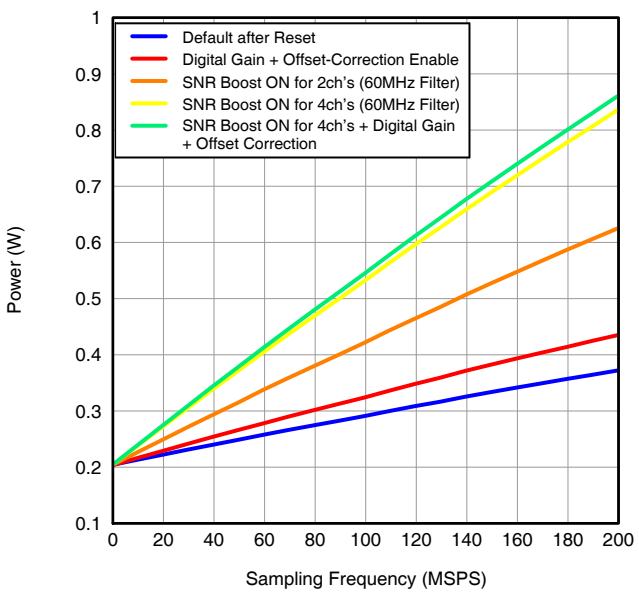


Figure 42.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

CMRR vs FREQUENCY

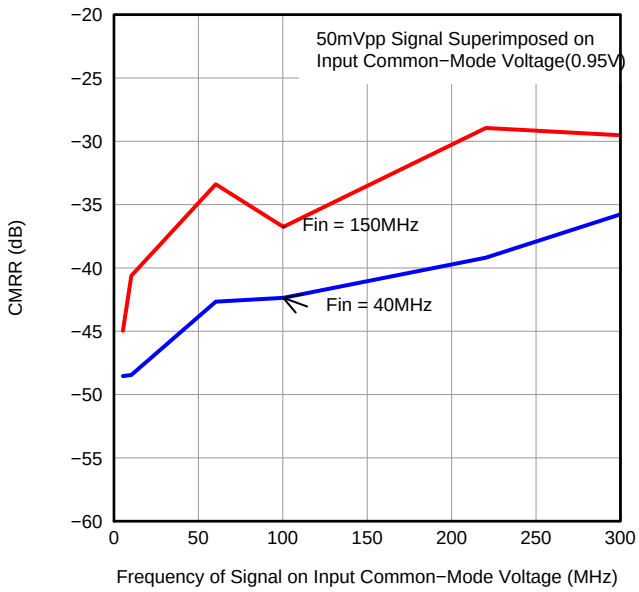


Figure 43.

CMRR SPECTRUM

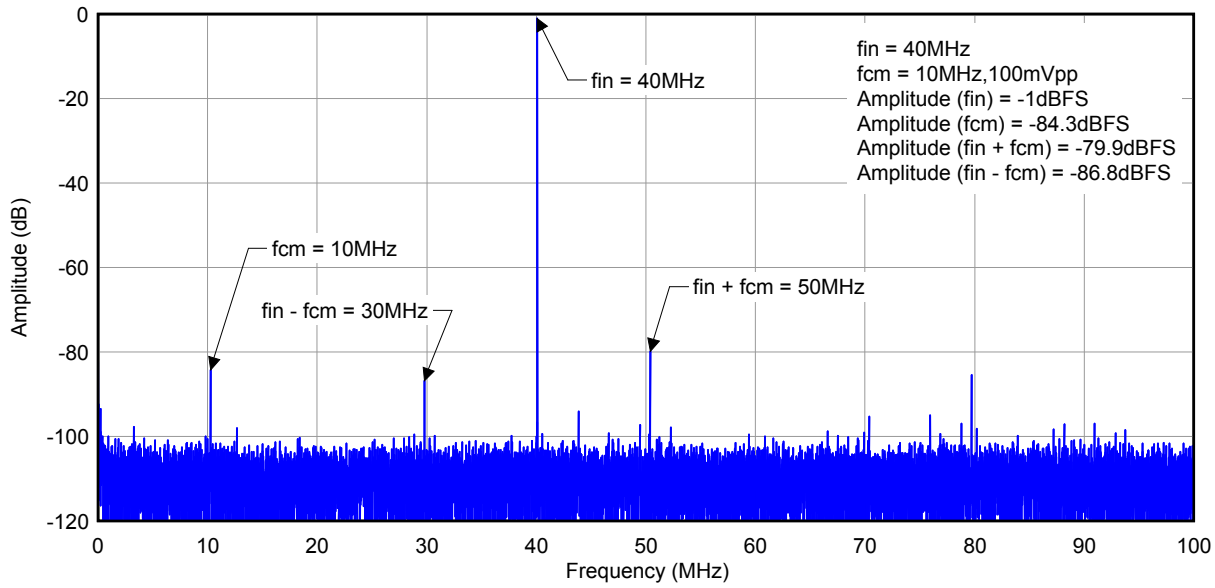


Figure 44.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

PSRR vs FREQUENCY

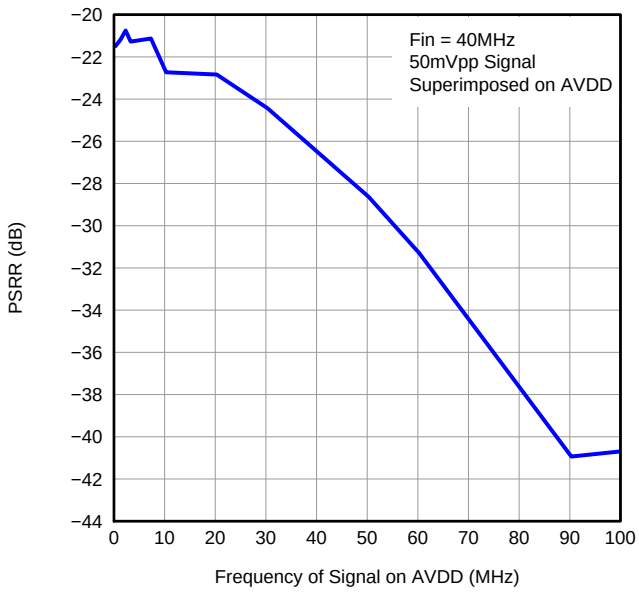


Figure 45.

PSRR SPECTRUM

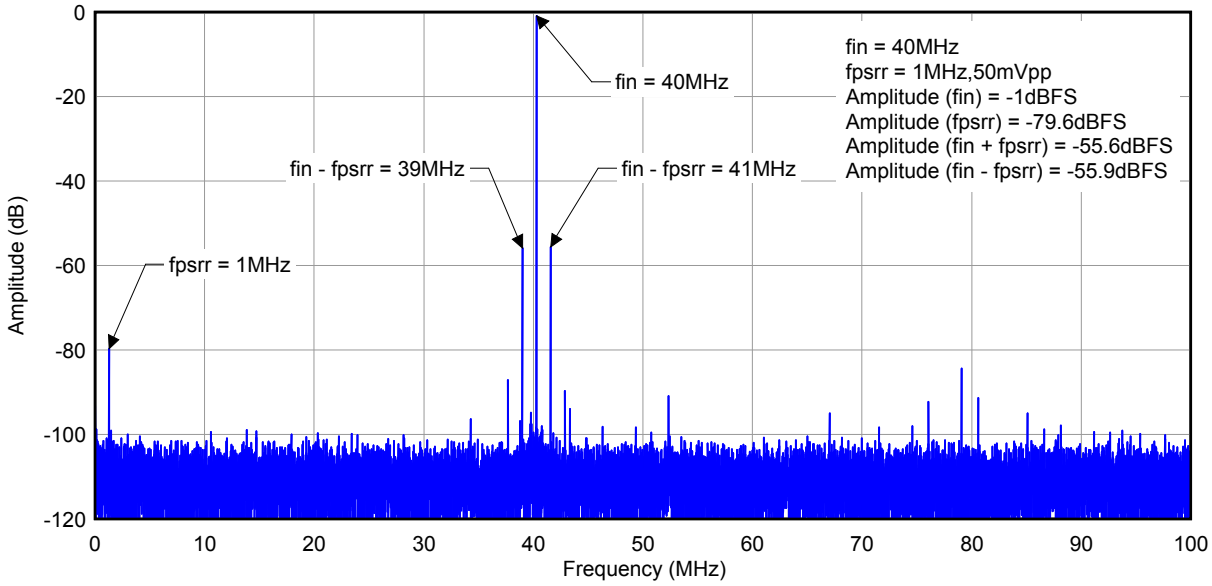


Figure 46.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

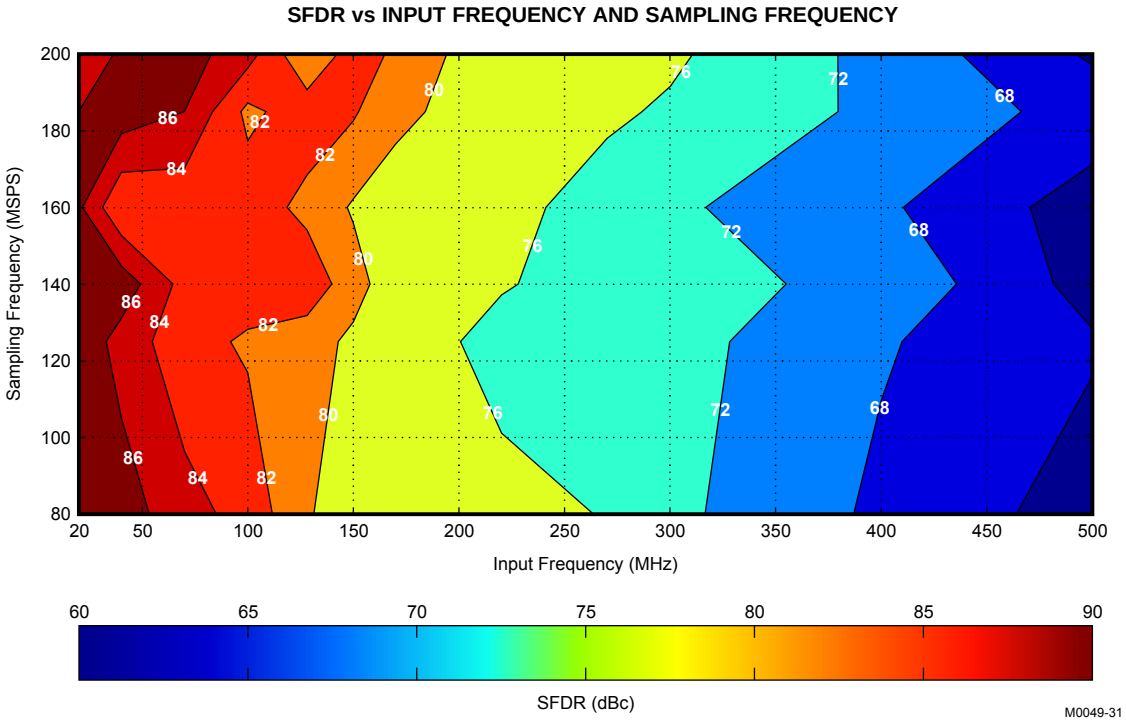


Figure 47. SFDR CONTOUR, 0-dB GAIN

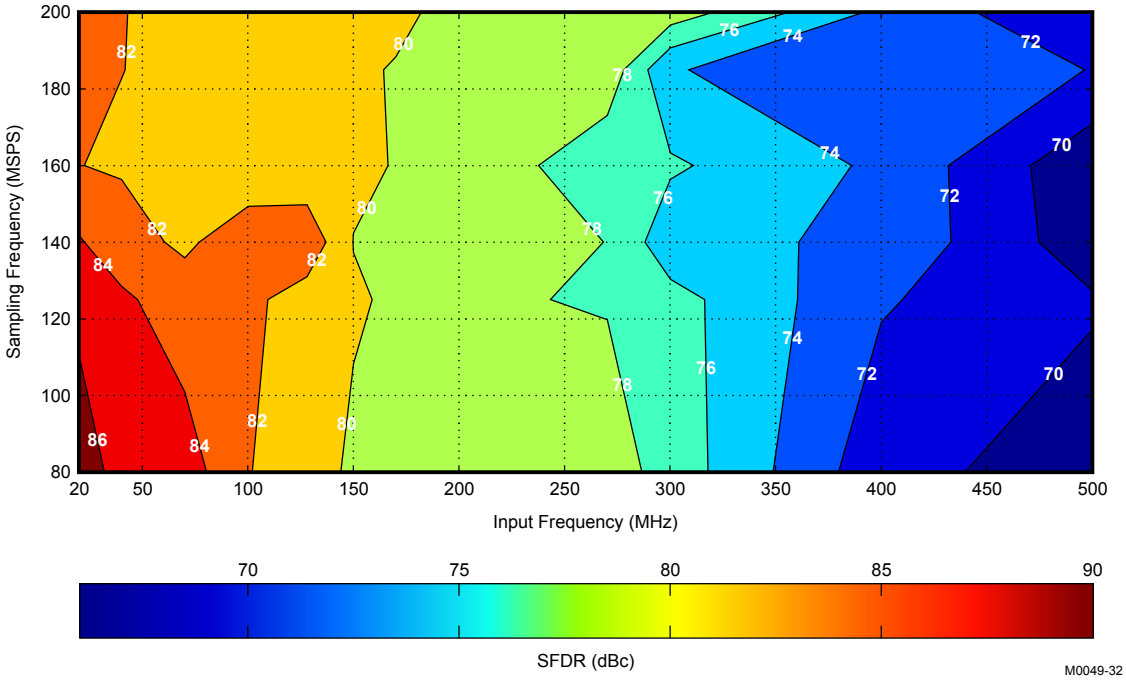


Figure 48. SFDR CONTOUR, 6-dB GAIN

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High Perf Mode disabled, 0 dB gain, DDR LVDS output interface, 32k point FFT (unless otherwise noted)

SNR vs INPUT FREQUENCY AND SAMPLING FREQUENCY

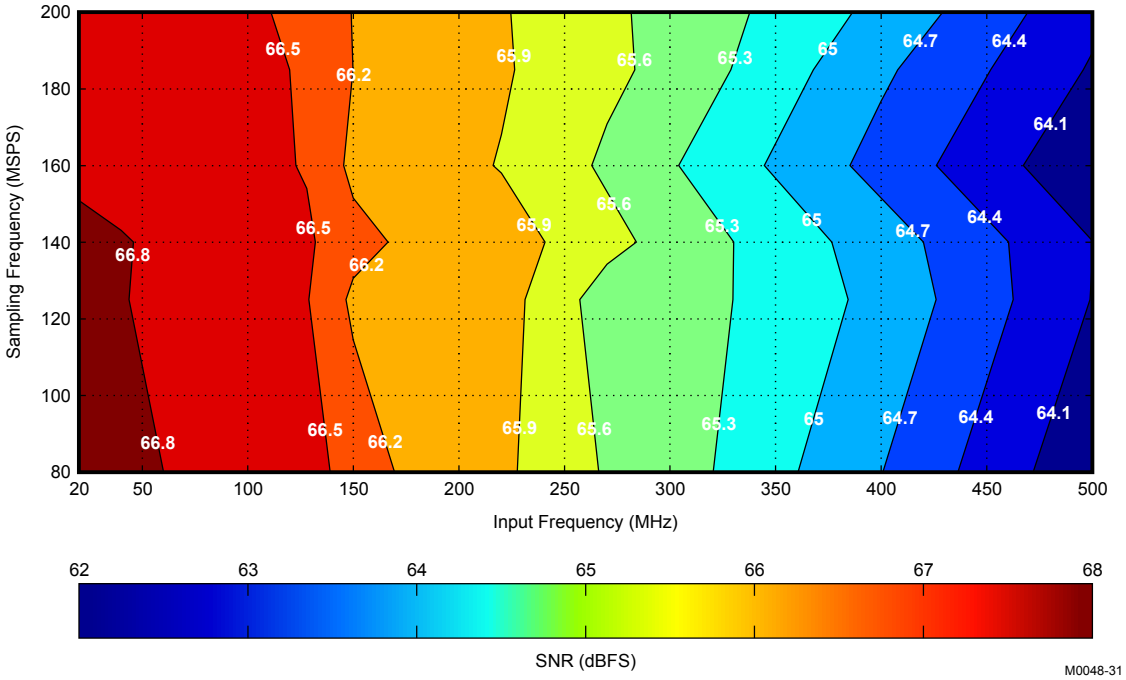


Figure 49. SNR CONTOUR, 0-dB GAIN

SNR vs INPUT FREQUENCY AND SAMPLING FREQUENCY

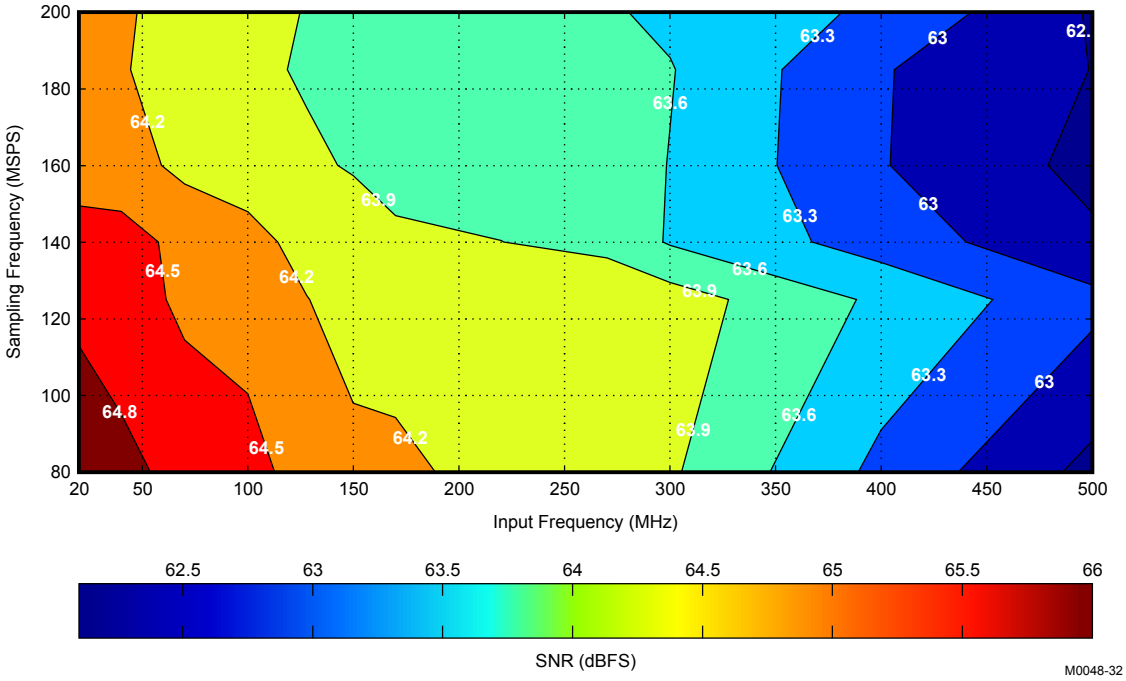


Figure 50. SNR CONTOUR, 6-dB GAIN

APPLICATION INFORMATION

THEORY OF OPERATION

ADS58C48 is a quad channel 11-bit A/D converter with sampling rates up to 200 MSPS.

At every rising edge of the input clock, the analog input signal of each channel is sampled simultaneously. The sampled signal in each channel is converted by a pipeline of low resolution stages. In each stage, the sampled and held signal is converted by a high speed, low resolution flash sub-ADC. The difference (residue) between the stage input and its quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and processed digitally to create the final code, after a data latency of 10 clock cycles.

The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary 2s complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture. This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 0.95 V, available on VCM pin. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-Vpp differential input swing.

The input sampling circuit has a high 3-dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage).

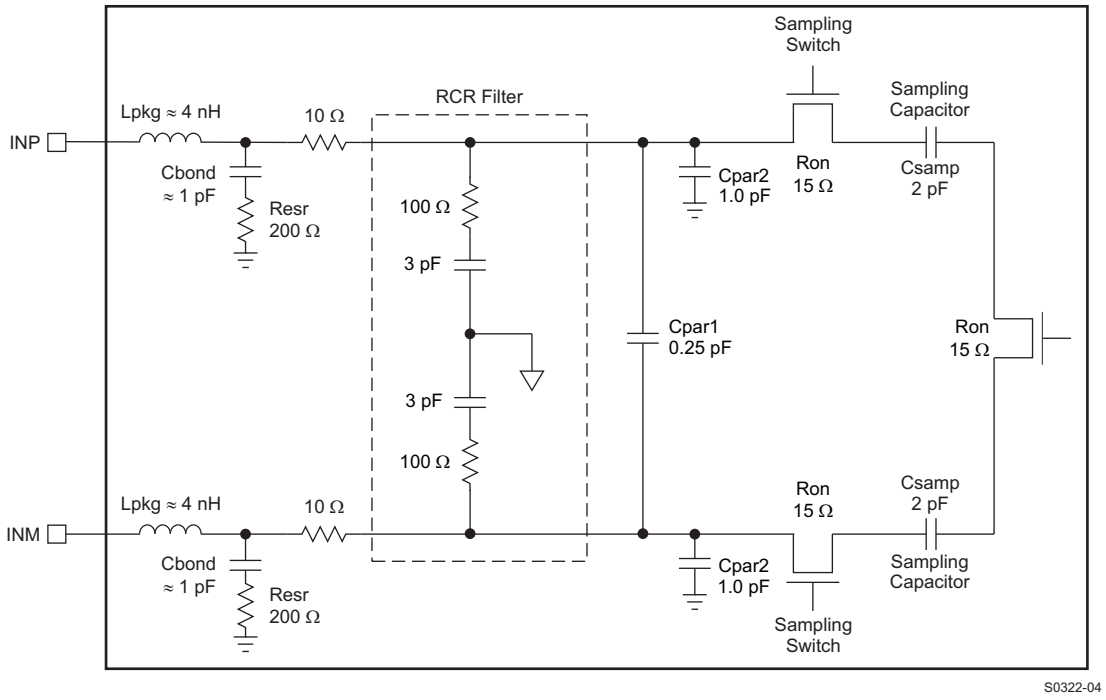


Figure 51. Analog Input Circuit

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitic.

SFDR performance can be limited due to several reasons - the effect of sampling glitches (described below), non-linearity of the sampling circuit and non-linearity of the quantizer that follows the sampling circuit.

Depending on the input frequency, sample rate AND input amplitude, one of these plays a dominant part in limiting performance.

At very high input frequencies (> about 300 MHz), SFDR is determined largely by the device's sampling circuit non-linearity. At low input amplitudes, the quantizer non-linearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, this could limit performance, mainly at low input frequencies (up to about 200 MHz). It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cut-off frequency of the R-C filter involves a trade-off.

A lower cut-off frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cut-off frequency (smaller C), bandwidth support is maximized. But now, the sampling glitches need to be supplied by the external drive circuit. This has limitations due to the presence of the package bond-wire inductance.

In ADS58C48, the R-C component values have been optimized while supporting high input bandwidth (up to 550 MHz). However, in applications with input frequencies up to 200 - 300 MHz, the filtering of the glitches can be improved further using an external R-C-R filter (as shown in Figure 54 and Figure 55).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 52 and Figure 53 show the impedance (Zin = Rin || Cin) looking into the ADC input pins.

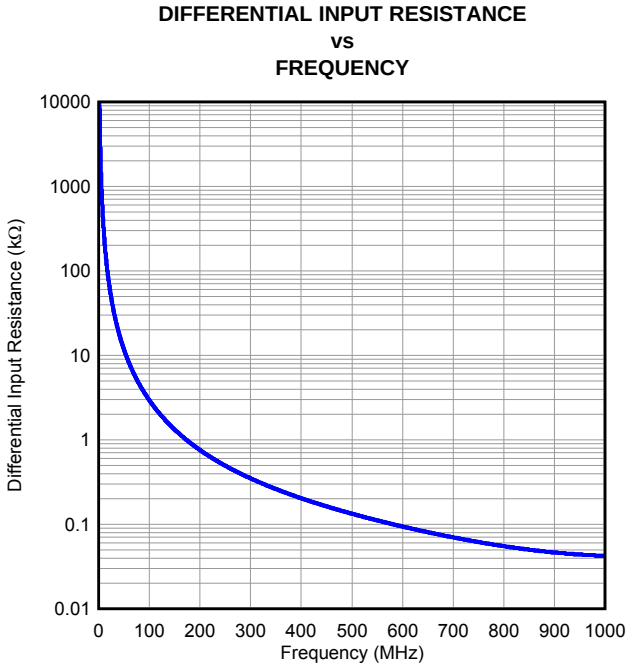


Figure 52. ADC Analog Input Resistance (Rin) Across Frequency

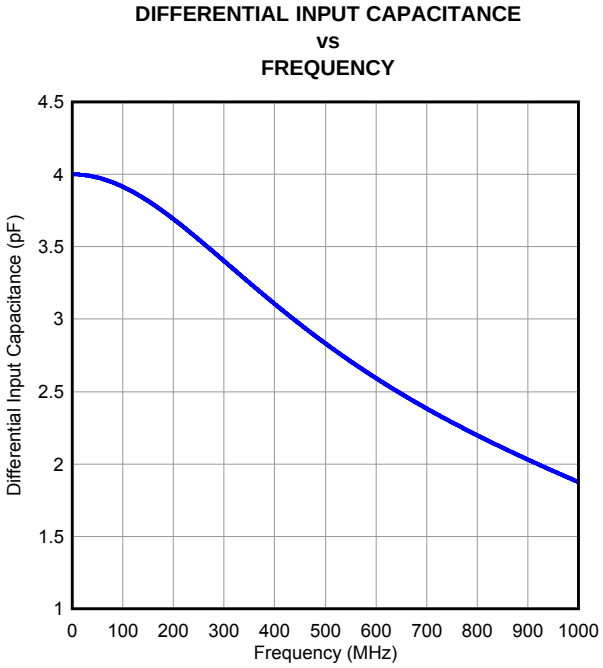


Figure 53. ADC Analog Input Capacitance (Cin) Across Frequency

Driving Circuit

Two example driving circuit configurations are shown in Figure 54 and Figure 55, one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies.

Note that both the drive circuits have been terminated by 50 Ω near the ADC side. The termination is accomplished by a 25-Ω resistor from each input to the 1.5-V common-mode (VCM) from the device. This allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair may be required between the two transformers as shown in the figures. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side have to be chosen to get an effective 50 Ω (in the case of 50-Ω source impedance).

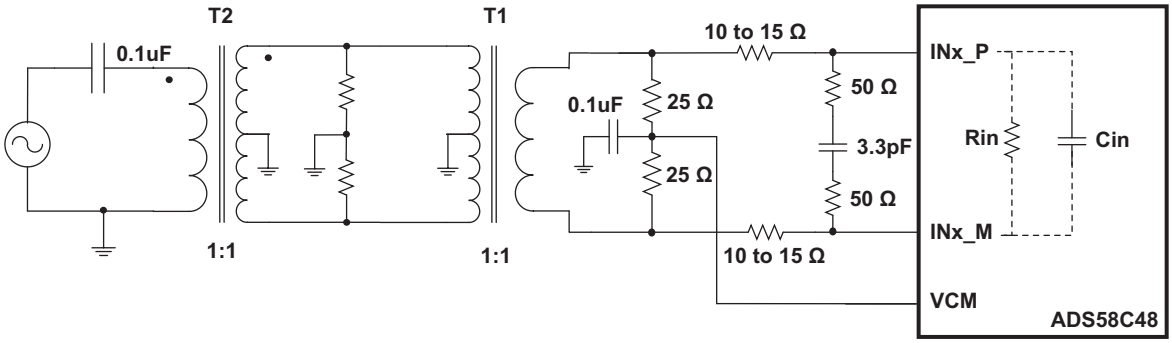


Figure 54. Drive Circuit with Low Bandwidth (For low input frequencies)

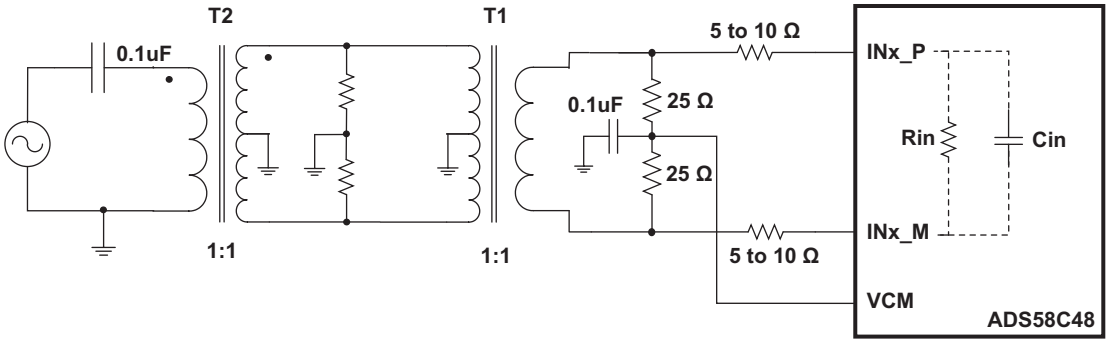


Figure 55. Drive Circuit with High Bandwidth (For high input frequencies)

All these examples show 1:1 transformers being used with a 50-Ω source. As explained in the *Drive Circuit Requirements*, this helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance will be 200 Ω. The higher impedance can lead to degradation in performance, compared to the case with 1:1 transformers.

For applications where only a band of frequencies are used, the drive circuit can be tuned to present a low impedance for the sampling glitches. Figure 56 shows an example with 1:4 transformer, tuned for a band around 150 MHz.

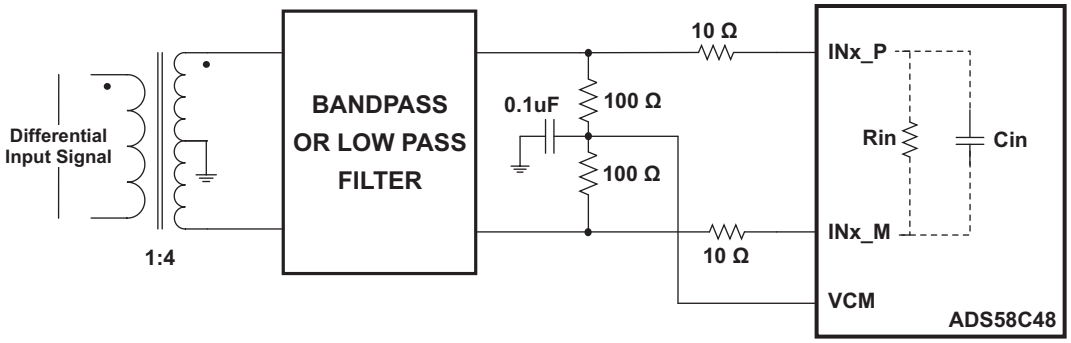


Figure 56. Drive Circuit with 1:4 Transformer

INPUT COMMON-MODE

To ensure a low-noise, common-mode reference, the VCM pin is filtered with a 0.1-μF low-inductance capacitor connected to ground. The VCM pin is designed to directly bias the ADC inputs (refer to Figure 54 to Figure 56). Each ADC input pin sinks a common-mode current of approximately 0.8 μA per MSPS of clock frequency.

When a differential amplifier is used to drive the ADC (with dc-coupling), ensure that the output common-mode of the amplifier is within the acceptable input common-mode range of the ADC inputs (Vcm ± 50mV).

CLOCK INPUT

The clock inputs of ADS58C48 can be driven differentially (sine, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources

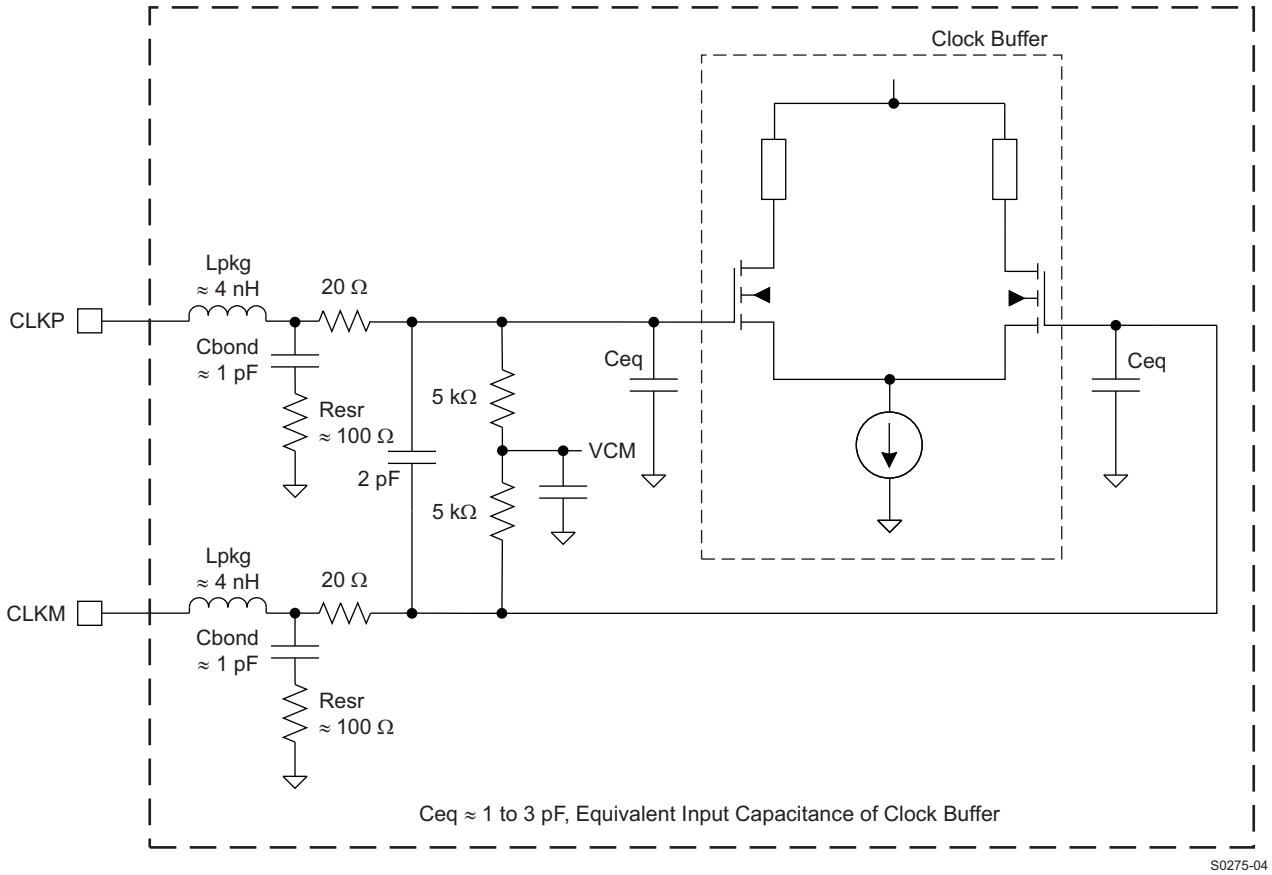


Figure 57. Internal Clock Buffer

Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-μF capacitor, as shown in Figure 59. For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

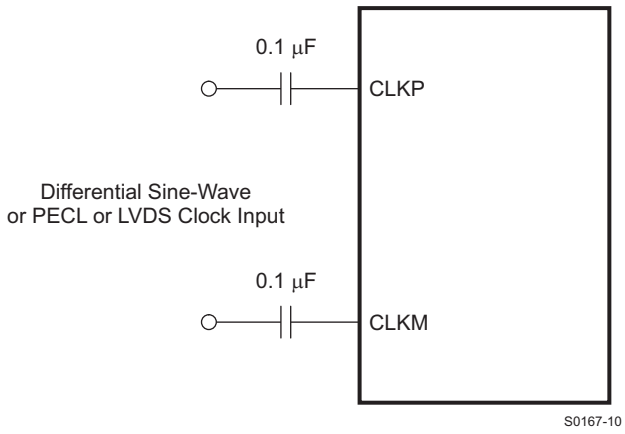


Figure 58. Differential Clock Driving Circuit

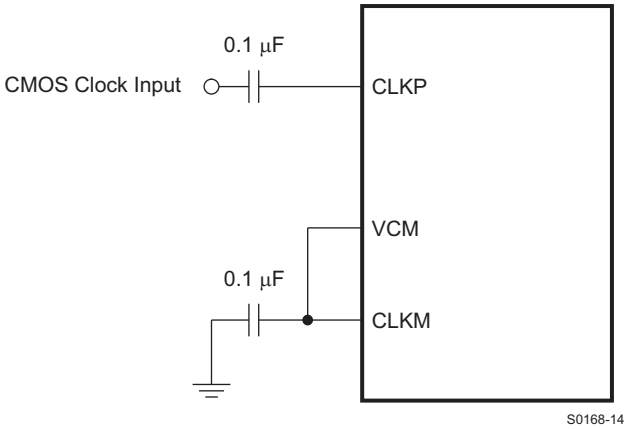


Figure 59. Single-Ended Clock Driving Circuit

DIGITAL FUNCTIONS

The device has several useful digital functions such as test patterns, gain, offset correction and SNRBoost. These can be controlled using two control bits **<DIGITAL MODE 1>** and **<DIGITAL MODE 2>** as per Table 8.

Table 8. Digital Functions Control Bits

DIGITAL FUNCTION	<DIGITAL MODE 1>	<DIGITAL MODE 2>	DESCRIPTION
All digital functions disabled	0	0	–
Only SNRBoost ^{3G} *enabled*	0	1	Set register bit <SNRBoost CH x ON> OR use the SNRB pins (1)
Test patterns, gain and offset correction *disabled*			–
SNRBoost ^{3G} enabled	1	X	To turn ON SNRBoost ^{3G}, set register bit <SNRBoost CH x ON> OR use the SNRB pins (1)
Test patterns enabled			Use register bits <TEST PATTERNS CH x> to select required pattern
Gain enabled			Device is in 0 dB gain mode, use bits <GAIN> to choose other gain settings (2)
Offset correction enabled			Use <EN OFFSET CORR> to turn ON the offset correction. Use <OFFSET CORR TIME CONSTANT> to choose the time constant (3)

(1) Refer to section SNR ENHANCEMENT USING SNRBOOST
(2) Refer to section GAIN FOR SFDR/SNR TRADE-OFF
(3) Refer to section OFFSET CORRECTION

SNR ENHANCEMENT USING SNRBoost 3G

SNRBoost 3G technology makes it possible to overcome SNR limitations due to quantization noise. Using SNRBoost 3G, enhanced SNR can be obtained for any bandwidth (less than Nyquist or Fs/2). The SNR improvement is achieved without affecting the default harmonic performance.

ADS58C48 uses 3rd generation SNRBoost technology (SNRBoost 3G) to achieve SNR enhancement over very wide bandwidths (up to 60MHz). When SNRBoost 3G is enabled, the noise floor in the spectrum acquires a typical bath-tub shape. The special feature of SNRBoost 3G is the nearly flat noise floor within the entire band of the bath-tub.

The position of the center of the bath-tub and its bandwidth are programmable. The available bandwidths are 60 MHz, 40 MHz, 30 MHz and 20 MHz. Several center frequency options are available for each bandwidth.

ADS58C48 includes 55 pre-programmed combinations of center frequency and bandwidth. Any one of these combinations can be selected by programming the register bits **<Ch SNRBoost Filter #>**. Each channel can be programmed with independent center frequency and bandwidths.

One of the characteristics of SNRBoost 3G is that the bandwidth scales with the sampling frequency. 60-MHz and 40-MHz bandwidths are achieved at sampling rate of 184 MHz; at higher sample rates, even higher bandwidths are possible .

The lower bandwidths 30 MHz and 20 MHz are achieved at sample rate of 200 MHz; at lower sample rates, the achieved bandwidth will be lower. Table 10 shows all combinations of center frequency for each bandwidth, specified as fraction of the sample rate.

By positioning the bath-tub within the desired signal band, SNR improvement can be achieved. Note that as the bandwidth is increased, the amount of SNR improvement reduces.

After reset, the SNRBoost function is disabled.

Table 9. SNRBoost 3G Control Using SNRB Pins

VOLTAGE APPLIED ON SNRB PINS	SNRB_1	SNRB_2
LOW	*SNRBoost 3G* mode OFF for channels C and D	*SNRBoost 3G* mode OFF for channels A and B
HIGH	*SNRBoost 3G* mode ON for channels C and D	*SNRBoost 3G* mode ON for channels A and B

To use SNRBoost 3G with SNRB pins follow the exact sequence below:

Select and enable the SNRBoost 3G Filter

1. First, disable bits <DIGITAL MODE 1> and <DIGITAL MODE 2> (= 0)
2. Next, select the appropriate SNRBoost 3G filter using register bits <Ch SNRBoost Filter #>.
3. Finally, set bit <DIGITAL MODE 2> (= 1)

Turn On/OFF SNRBoost 3G

1. Use the SNRB1 and SNRB2 pins to dynamically turn on/off the SNRBoost 3G for each pair of channels.

To use SNRBoost 3G without using SNRB pins follow the exact sequence below :

Select and enable the SNRBoost 3G Filter

1. First, disable bits <DIGITAL MODE 1> and <DIGITAL MODE 2> (= 0)
2. Next, select the appropriate SNRBoost filter using register bits <Ch SNRBoost Filter #>.
3. Finally, set bit <DIGITAL MODE 2> (= 1)
4. Set the SNRB pin over-ride bit <OVERRIDE SNRB pins>

Turn On/OFF SNRBoost 3G

1. Turn ON and OFF the SNRBoost 3G for each channel using the register bits <SNRBoost CH A ON>, <SNRBoost CH B ON>, <SNRBoost CH C ON> and <SNRBoost CH D ON>

NOTE

To use a different SNRBoost [3G] filter, it is required to follow all the above steps in the exact order specified. Not following the order can result in incorrect operation of SNRBoost [3G] filter.

To just turn on and off the filter without changing the filter #, simply follow the steps under Turn On/OFF SNRBoost [3G].

Table 10. Complete List of SNRBoost [3G] Modes (Fs = Sampling frequency in MSPS)

SNRBoost FILTER #	BANDWIDTH OF THE BATH-TUB, MHz	CENTER FREQUENCY OF THE BATH-TUB, MHz
0	25 x (Fs/200)	15 x (Fs/200)
1	20 x (Fs/200)	30 x (Fs/200)
2	20 x (Fs/200)	35 x (Fs/200)
3	20 x (Fs/200)	42 x (Fs/200)
4	20 x (Fs/200)	50 x (Fs/200)
5	20 x (Fs/200)	58 x (Fs/200)
6	20 x (Fs/200)	65 x (Fs/200)
7	20 x (Fs/200)	75 x (Fs/200)
8	20 x (Fs/200)	85 x (Fs/200)
9	25 x (Fs/200)	87.5 x (Fs/200)
10	25 x (Fs/200)	15 x (Fs/200)
11	20 x (Fs/200)	25 x (Fs/200)
12	20 x (Fs/200)	35 x (Fs/200)
13	20 x (Fs/200)	42 x (Fs/200)
14	20 x (Fs/200)	50 x (Fs/200)
15	20 x (Fs/200)	58 x (Fs/200)
16	20 x (Fs/200)	65 x (Fs/200)
17	20 x (Fs/200)	75 x (Fs/200)
18	25 x (Fs/200)	82.5 x (Fs/200)
19	25 x (Fs/200)	87.5 x (Fs/200)
20	25 x (Fs/200)	15 x (Fs/200)
21	30 x (Fs/200)	30 x (Fs/200)
22	30 x (Fs/200)	35 x (Fs/200)
23	30 x (Fs/200)	45 x (Fs/200)
24	30 x (Fs/200)	55 x (Fs/200)
25	30 x (Fs/200)	65 x (Fs/200)
26	30 x (Fs/200)	70 x (Fs/200)
27	30 x (Fs/200)	80 x (Fs/200)
28	30 x (Fs/200)	85 x (Fs/200)
29	25 x (Fs/200)	87.5 x (Fs/200)
30	40 x (Fs/184)	46 x (Fs/184)
31	40 x (Fs/184)	72 x (Fs/184)
32	40 x (Fs/184)	20 x (Fs/184)
33	40 x (Fs/184)	40 x (Fs/184)
34	40 x (Fs/184)	39.5 x (Fs/184)

Table 10. Complete List of SNRBoost [3G] Modes (Fs = Sampling frequency in MSPS) (continued)

SNRBoost FILTER #	BANDWIDTH OF THE BATH-TUB, MHz	CENTER FREQUENCY OF THE BATH-TUB, MHz
35	40 x (Fs/184)	33.5 x (Fs/184)
36	40 x (Fs/184)	27 x (Fs/184)
37	40 x (Fs/184)	53 x (Fs/184)
38	40 x (Fs/184)	59 x (Fs/184)
39	40 x (Fs/184)	65.5 x (Fs/184)
40	60 x (Fs/184)	46 x (Fs/184)
41	60 x (Fs/184)	46 x (Fs/184)
42	60 x (Fs/184)	30 x (Fs/184)
43	60 x (Fs/184)	30 x (Fs/184)
44	60 x (Fs/184)	62 x (Fs/184)
45	60 x (Fs/184)	62 x (Fs/184)
46	60 x (Fs/184)	40.5 x (Fs/184)
47	60 x (Fs/184)	40.5 x (Fs/184)
48	60 x (Fs/184)	37 x (Fs/184)
49	60 x (Fs/184)	37 x (Fs/184)
50	60 x (Fs/184)	53 x (Fs/184)
51	60 x (Fs/184)	50 x (Fs/184)
52	60 x (Fs/184)	54 x (Fs/184)
53	58 x (Fs/184)	58 x (Fs/184)
54	60 x (Fs/184)	62 x (Fs/184)

GAIN FOR SFDR/SNR TRADE-OFF

ADS58C48 includes gain settings that can be used to get improved SFDR performance. The gain is programmable from 0 dB to 6 dB (in 0.5 dB steps) using the <GAIN> register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 11.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades about 0.5 -1dB. The SNR degradation is less at high input frequencies. As a result, the fine gain is very useful at high input frequencies as the SFDR improvement is significant with marginal degradation in SNR. So, the fine gain can be used to trade-off between SFDR and SNR.

After a reset, the gain function is disabled. To use fine gain:

- First, program the bits <DIGITAL MODE 1> and <DIGITAL MODE 2> as per the table above to enable the gain function.
- This enables gain and puts device in 0 dB gain mode.
- For other gain settings, program the <GAIN> register bits.

Table 11. Full-Scale Range Across Gains

GAIN, dB	TYPE	FULL-SCALE, V_{PP}
0	Default after reset	2
1	Programmable gain	1.78
2		1.59
3		1.42
4		1.26
5		1.12
6		1.00

OFFSET CORRECTION

ADS58C48 has an internal offset correction algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled using the serial register bit <EN OFFSET CORR>. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using register bits <OFFSET CORR TIME CONSTANT> as described in Table 12.

After the offset is estimated, the correction can be frozen by setting <FREEZE OFFSET CORR > = 1. Once frozen, the last estimated value is used for offset correction every clock cycle. Note that offset correction is disabled by default after reset.

After a reset, the offset correction is disabled. To use offset correction:

- First, program the bits <DIGITAL MODE 1> and <DIGITAL MODE 2> as per the table above to enable the correction.
- Then set <EN OFFSET CORR> to 1 and program the required time constant.

Table 12. Time Constant of Offset Correction Algorithm

OFFSET CORR	TIME CONSTANT (Number of clock cycles)	TIME CONSTANT, TC_{CLK} x 1/fs(sec)(1)
0000	1M	5.2 ms
0001	2M	10.5 ms
0010	4M	21 ms
0011	8M	42 ms
0100	16M	84 ms
0101	32M	167.8 ms
0110	64M	335.5 ms
0111	128M	671 ms
1000	256M	1.34 s
1001	512M	2.7 s
1010	1G	5.4 s
1011	2G	10.7 s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, Fs = 200 MSPS

DIGITAL OUTPUT INFORMATION

ADS58C48 provides 11-bit digital data for each channel and a common output clock synchronized with the data.

Output Interface

Two output interface options are available – Double Data Rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit <LVDS CMOS>.

DDR LVDS Outputs

In this mode, the data bits and clock are output using Low Voltage Differential Signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair.

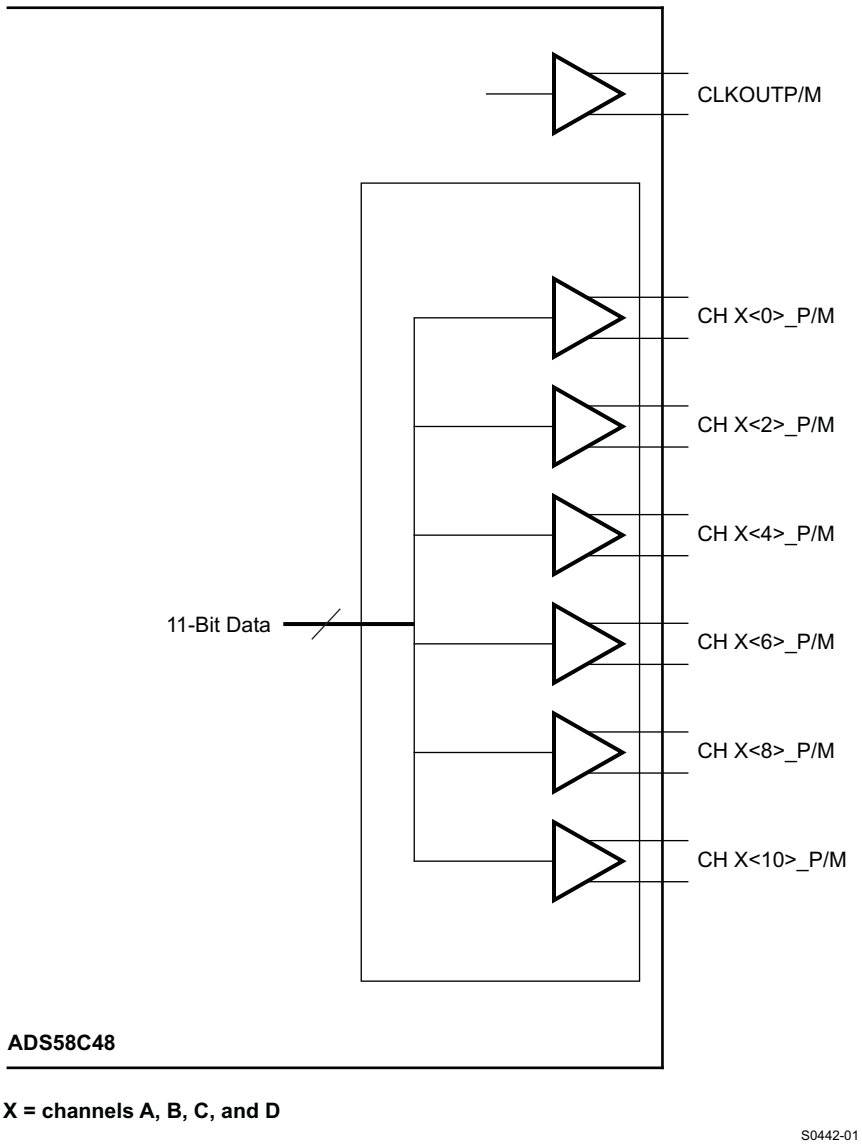


Figure 60. DDR LVDS Interface

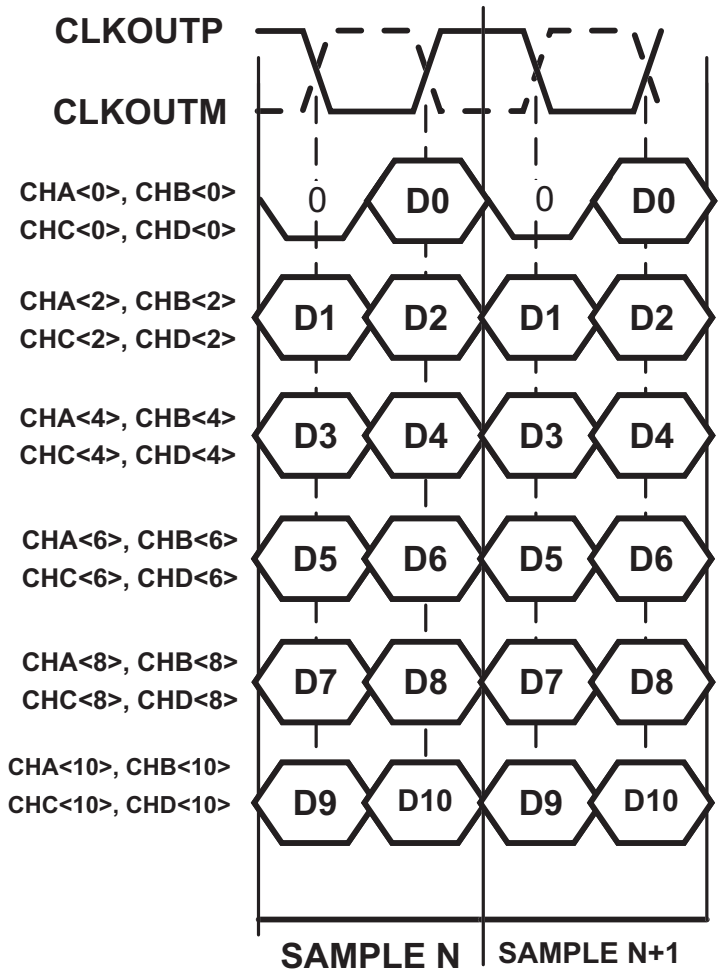


Figure 61. DDR LVDS Interface Timing Diagram

LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 62. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100-Ω termination.

The Vdiff voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The Vdiff voltage is programmable using the register bits <LVDS SWING> from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination. This can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled using register bits <LVDS DATA STRENGTH> and <LVDS CLKOUT STRENGTH> for data and output clock buffers respectively.

The buffer output impedance behaves like a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

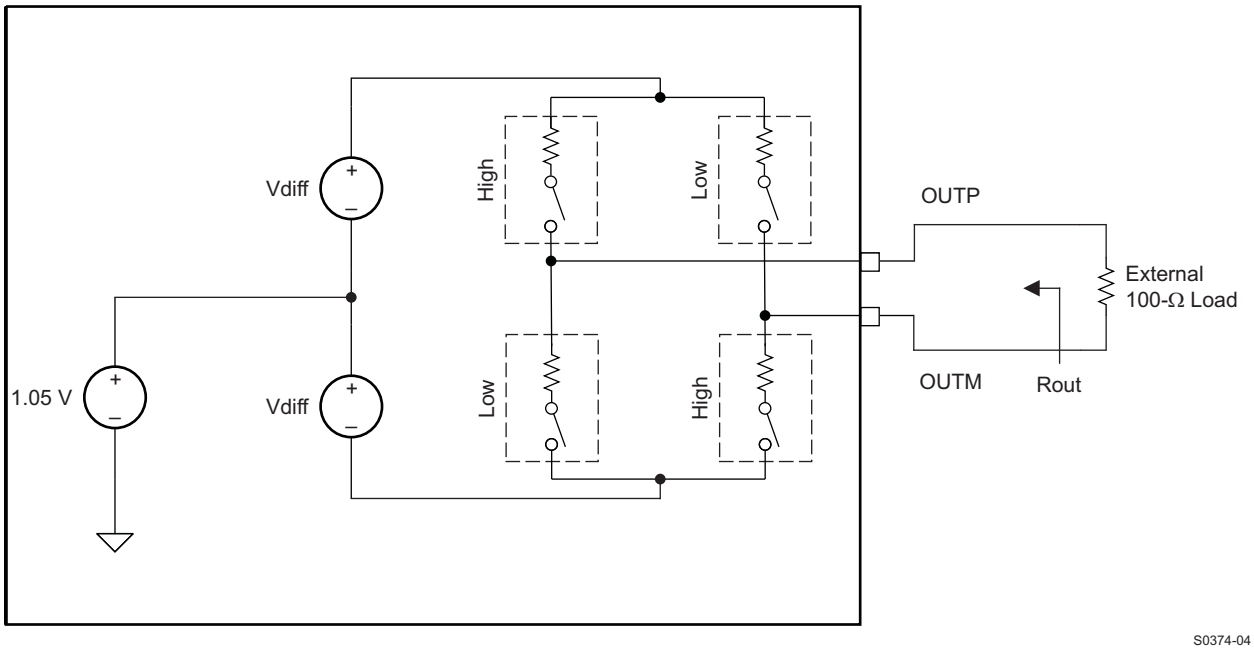


Figure 62. LVDS Buffer Equivalent Circuit

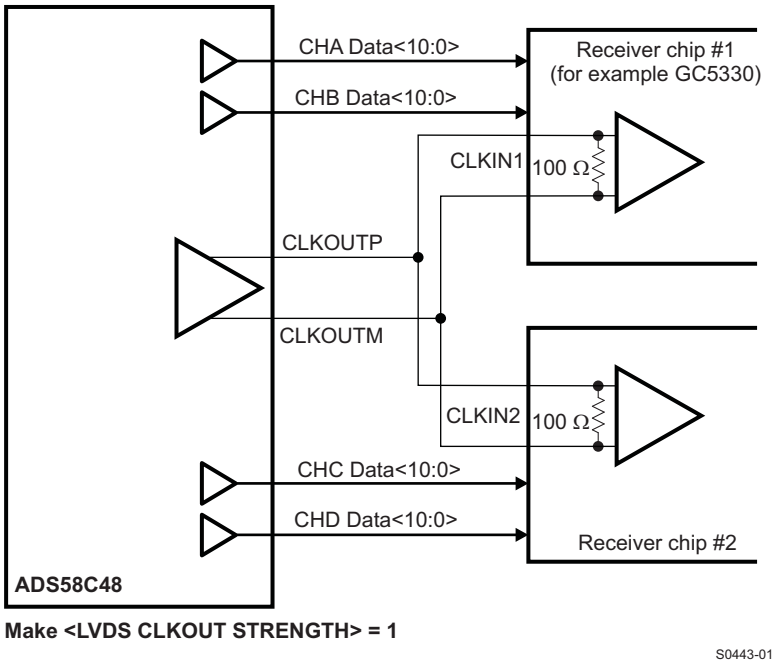


Figure 63. LVDS Strength Doubling - Example Application

Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pin as CMOS voltage level, every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures wide data stable window provided the data outputs have minimal load capacitance. It is recommended to use short traces (1 to 2 inches) terminated with not more than 5-pF load capacitance.

For sampling frequencies greater than 150 MSPS, it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified for the higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture the data.

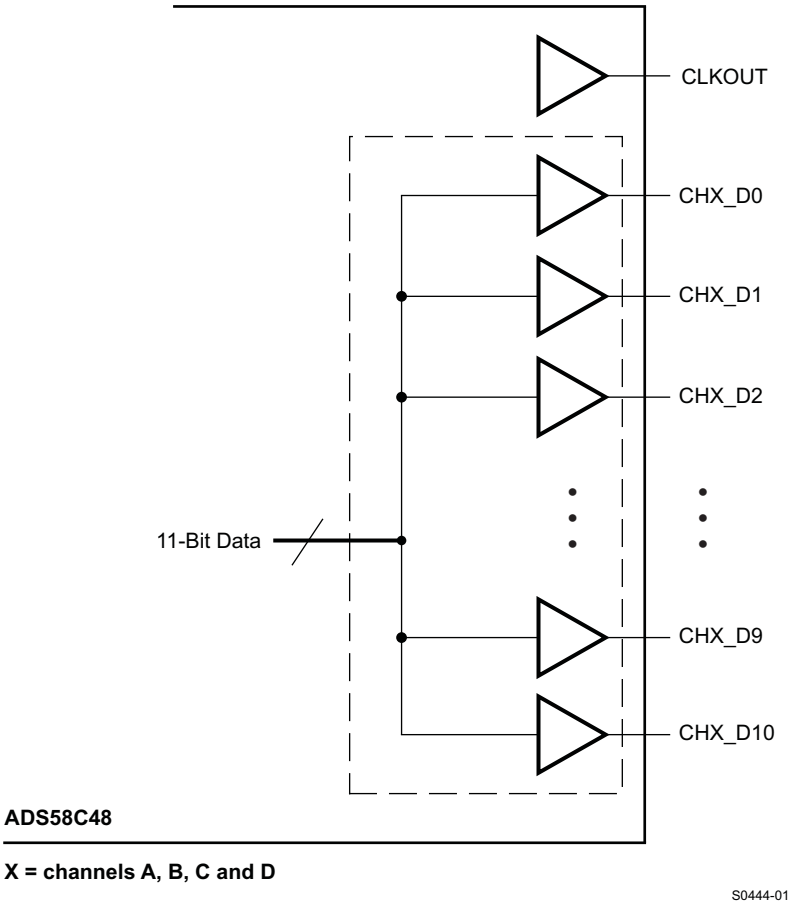


Figure 64. CMOS Interface

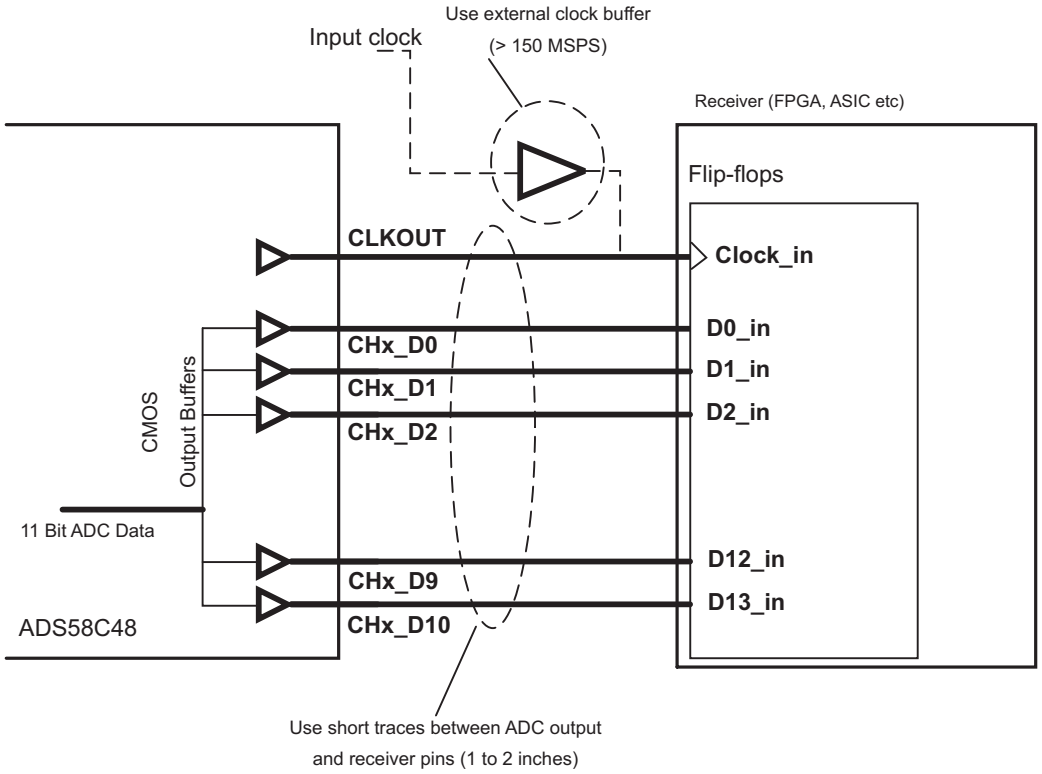


Figure 65. Data Capture with CMOS Interface

CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current due to CMOS output switching = C_L x DRVDD x (N x F_{AVG}),
where C_L = load capacitance, N x F_{AVG} = average number of output bits switching.

Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the serial interface register bit <DATA FORMAT CHx>.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0x7FF in offset binary output format, and 0x3FF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x400 in 2s complement output format.

BOARD DESIGN CONSIDERATIONS

For EVM board information, refer to the ADS58C48 EVM User's Guide (SLAU313).

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User's Guide (SLAU313) for details on layout and grounding.

Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to analog and digital ground internally. So, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$\text{SINAD} = 10\text{Log}^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{3}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10\text{Log}^{10}\frac{P_S}{P_N} \tag{4}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) – DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10}\frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \tag{5}$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10}\frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \tag{6}$$

Crosstalk (only for multi-channel ADCs) – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS58C48IPFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS58C48I	Samples
ADS58C48IPFPR	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS58C48I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

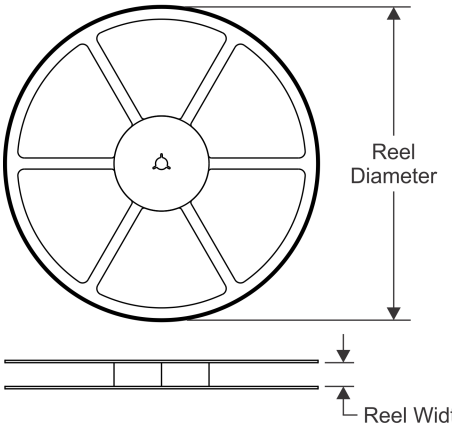
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

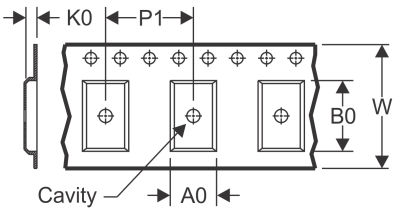
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

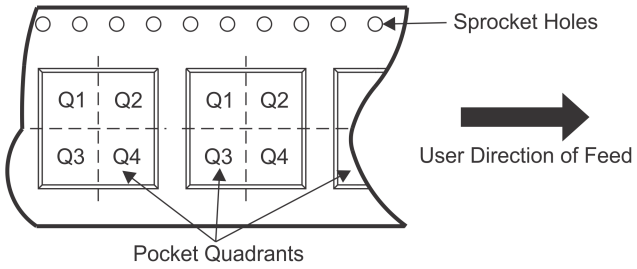


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

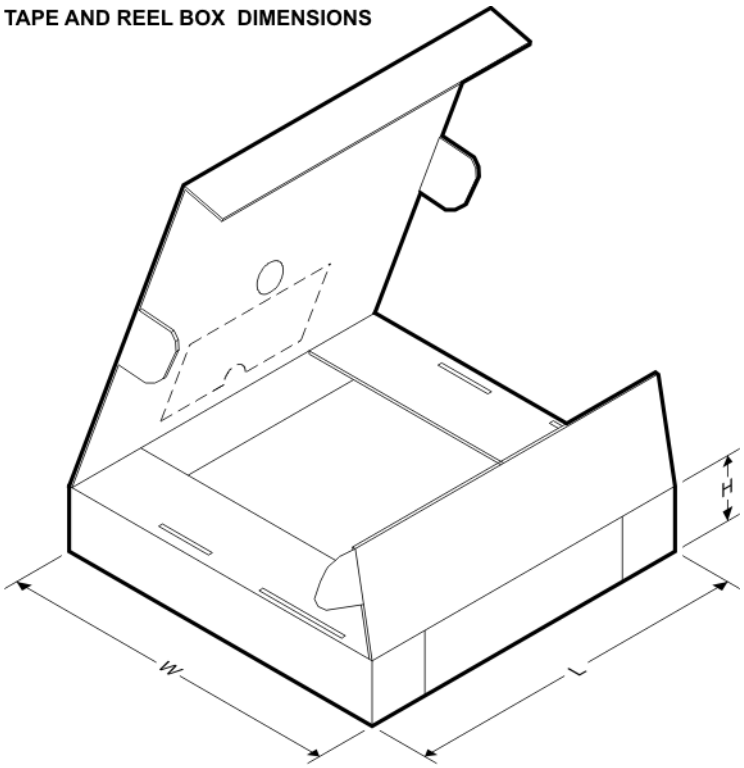
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS58C48IPFPR	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

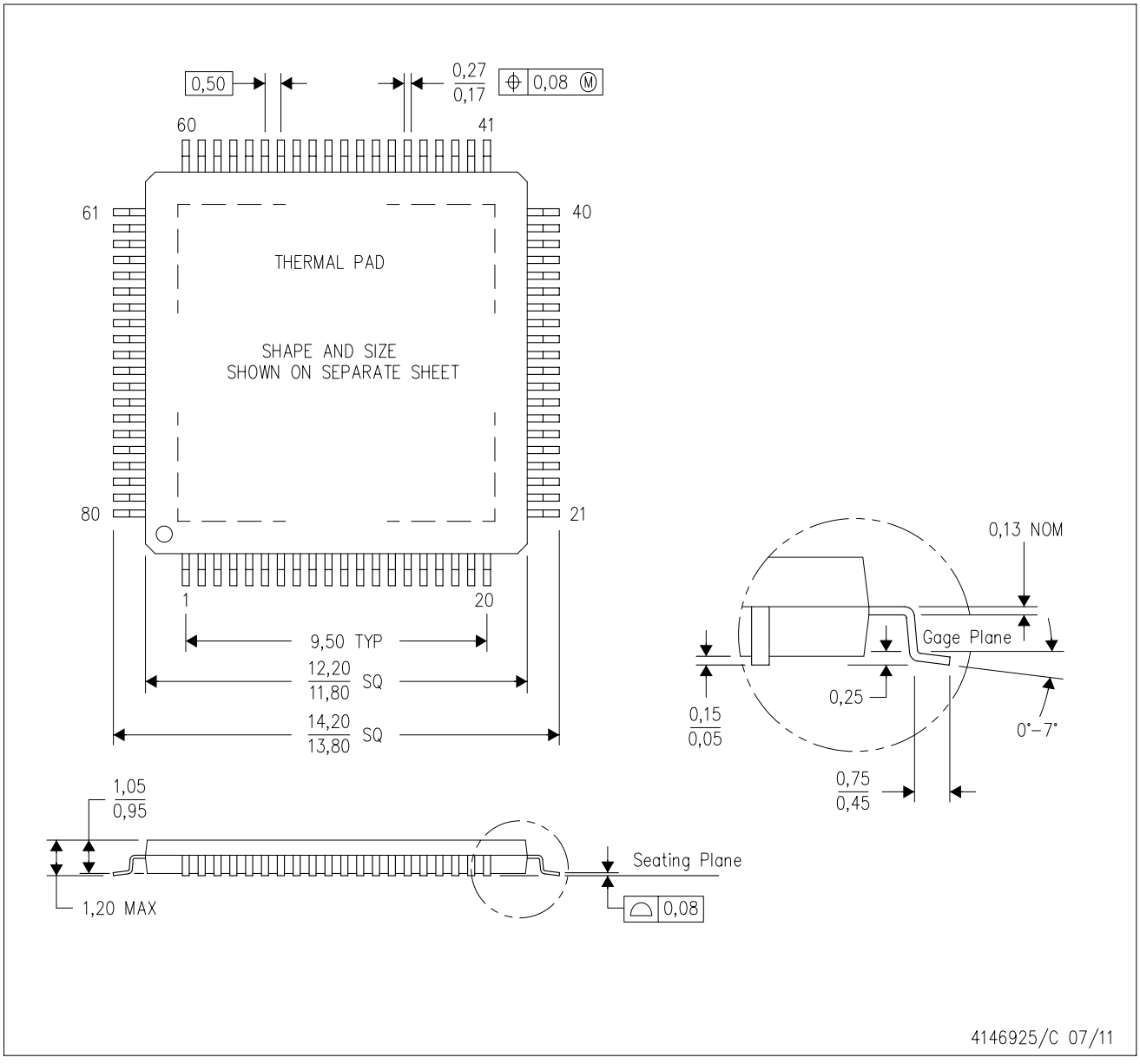
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS58C48IPFPR	HTQFP	PFP	80	1000	350.0	350.0	43.0

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

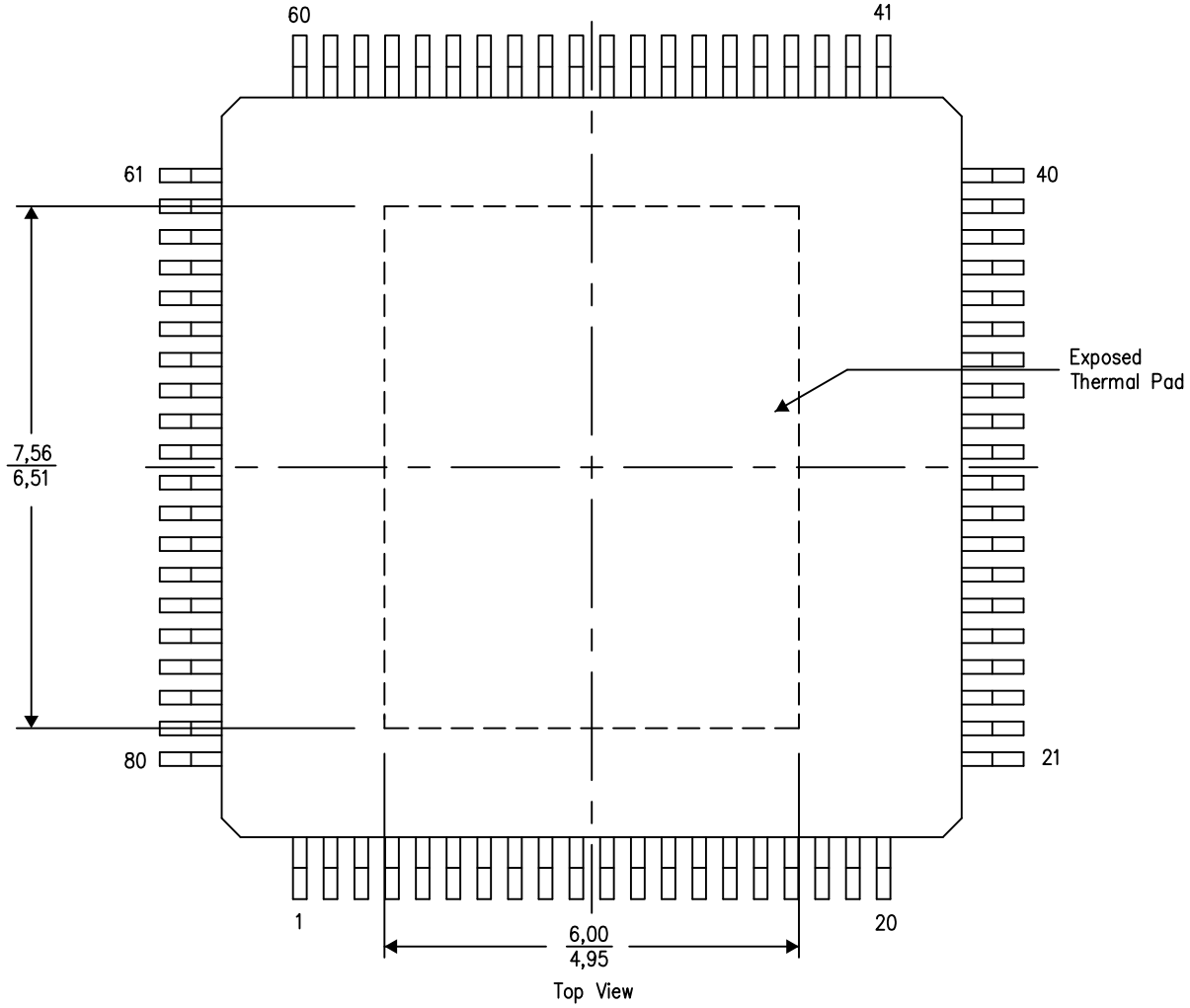
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206327–14/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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