



# THE DATASHEET OF UC3843B



### Description

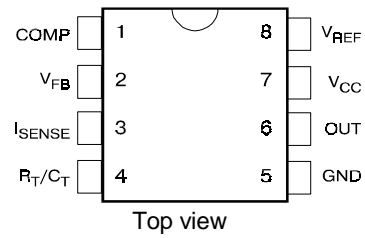
The 3842/43/44/45 are fixed frequency current mode PWM controller. They are specially designed for OFF-Line and DC to DC converter applications with a minimal external components. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Protection circuitry includes built undervoltage lockout and current limiting. The 3842 and 3844 have UVLO thresholds of 16 V (on) and 10 V (off). The corresponding thresholds for the 3843/45 are 8.4V (on) and 7.6V (off). The 3842) and 3843 can operate within 100% duty cycle. The 3844 and 3845 can operate within 50% duty cycle.

The 384X has Start-Up Current 0.17mA (typ).

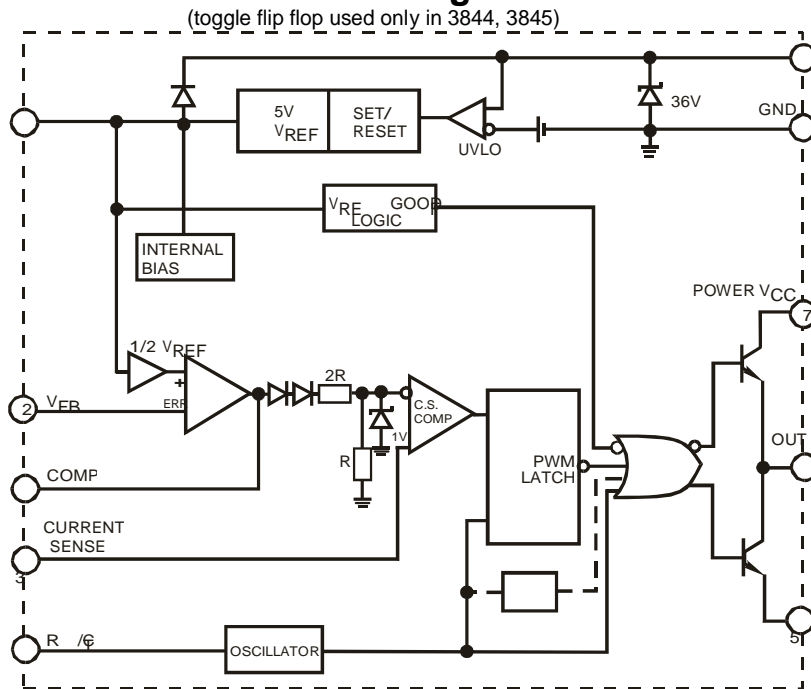
### Features

- Low Start-Up and Operating Current
- High Current Totem Pole Output
- Undervoltage Lockout With Hysteresis
- Operating Frequency Up To 300KHz (384X)  
500KHz (384X)

### Pin Connection



### Block diagram



### Absolute Maximum Ratings

Symbol	Parameter	Maximum	Units
V <sub>CC</sub>	Supply Voltage (low impedance source)	30	V
I <sub>o</sub>	Output Current	±1	A
V <sub>i</sub>	Input Voltage (Analog Inputs pins 2,3)	-0.3 to 5.5	V
I <sub>SINK (E.A)</sub>	Error Amp Output Sink Current	10	mA
P <sub>o</sub>	Power Dissipation (T <sub>A</sub> =25°C)	1	W
T <sub>stg</sub>	Storage Temperature Range	-65 to 150	°C
T <sub>L</sub>	Lead Temperature (soldering 5 sec.)	260	°C

**Electrical characteristics**

 (\* $V_{CC}=15V$ ,  $R_T=10k\Omega$ ,  $C_T=3.3nF$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Units	
<b>Reference Section</b>							
Reference Output Voltage	$V_{REF}$	$T_J = 25^{\circ}C$ , $I_{REF} = 1\text{ mA}$	4.9	5.0	5.1	V	
Line Regulation	$\Delta V_{REF}$	$12V \leq V_{CC} \leq 25\text{ V}$		6.0	20	mV	
Load Regulation	$\Delta V_{REF}$	$1\text{ mA} \leq I_{REF} \leq 20\text{mA}$		6.0	25		
Short Circuit Output Current	$I_{SC}$	$T_A = 25^{\circ}C$		-100	-180	mA	
<b>Oscillator Section</b>							
Oscillation Frequency	f	$T_J = 25^{\circ}C$	384X	47	50	57	KHz
			384X	47	52	57	
Frequency Change with Voltage	$\Delta f/\Delta V_{CC}$	$12V \leq V_{CC} \leq 25\text{ V}$		0.05	1.0	%	
Oscillator Amplitude	$V_{(OSC)}$	(peak to peak)		1.6		V	
<b>Error Amplifier Section</b>							
Input Bias Current	$I_{BIAS}$	$V_{FB}=3V$		-0.1	-2	$\mu A$	
Input Voltage	$V_{(I.E.A)}$	$V_{pin1} = 2.5V$	2.42	2.5	2.58	V	
Open Loop Voltage Gain	$A_{VOL}$	$2V \leq V_o \leq 4V$	65	90		dB	
Power Supply Rejection Ratio	PSRR	$12V \leq V_{CC} \leq 25\text{ V}$	60	70			
Output Sink Current	$I_{SINK}$	$V_{pin2} = 2.7V$ , $V_{pin1} = 1.1V$	2	7		mA	
Output Source Current	$I_{SOURCE}$	$V_{pin2} = 2.3V$ , $V_{pin1} = 5V$	-0.5	-1.0		mA	
High Output Voltage	$V_{OH}$	$V_{pin2} = 2.3V$ , $R_L = 15K\Omega$ to GND	5.0	6.0		V	
Low Output Voltage	$V_{OL}$	$V_{pin2} = 2.7V$ , $R_L = 15K\Omega$ to PIN 8		0.8	1.1		
<b>Current Sense Section</b>							
Gain	$G_V$	(Note 1 & 2)	2.85	3.0	3.15	V/V	
Maximum Input Signal	$V_{(MAX)}$	$V_{pin1} = 5V$ (Note1)	0.9	1.0	1.1	V	
Supply Voltage Rejection	SVR	$12V \leq V_{CC} \leq 25\text{ V}$ (Note 1)		70		dB	
Input Bias Current	$I_{BIAS}$	$V_{pin3} = 3V$		-3.0	-10	$\mu A$	
<b>Output Section</b>							
Low Output Voltage	$V_{OL}$	$I_{SINK} = 20\text{ mA}$		0.08	0.4	V	
		$I_{SINK} = 200\text{ mA}$		1.4	2.2		
High Output Voltage	$V_{OH}$	$I_{SINK} = 20\text{ mA}$	13	13.5		V	
		$I_{SINK} = 200\text{ mA}$	12	13.0			
Rise Time	$t_r$	$T_J = 25^{\circ}C$ , $C_L = 1nF$ (Note 3)		45	150	nS	
Fall Time	$t_f$	$T_J = 25^{\circ}C$ , $C_L = 1nF$ (Note 3)		35	150		
<b>Undervoltage Lockout Section</b>							
Start Theshold	$V_{TH(ST)}$	3842/44	14.5	16.0	17.5	V	
		3843/45	7.8	8.4	9.0		
Min. Operating Voltage (After Turn On)	$V_{OPR(min)}$	3842/44	8.5	10	11.5	V	
		3843/45	7.0	7.6	8.2		
<b>PWM Section</b>							
Max. Duty Cycle	$D_{(MAX)}$	3842/43	95	97	100	%	
		3844/45	47	48	50		
Min. Duty Cycle	$D_{(MAX)}$				0		
<b>Total Standby Current</b>							
Start-Up Current	$I_{ST}$	384X		0.17	0.3	mA	
Operating Supply Current	$I_{CC (OPR)}$	$V_{pin3} = V_{pin2} = 0V$		13	17		
Zener Voltage	$V_Z$	$I_{CC}=25\text{ mA}$	30	38		V	

 \* - Adjust  $V_{CC}$  above the start threshold before setting it to 15V.

 Note 1: Parameter measured at trip point of latch with  $V_{pin2}=0$ .

 Note 2: Gain defined as  $A=\Delta V_{pin1}/\Delta V_{pin3}$ ;  $0 \leq V_{pin3} \leq 0.8V$ .

Note 3: These parameters, although guaranteed, are not 100% tested in production.

### Pin functions

N	Function	Description
1	COMP	This pin is the Error Amplifier output and is made for loop compensation.
2	V <sub>FB</sub>	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I <sub>SENSE</sub>	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R <sub>T</sub> /C <sub>T</sub>	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R <sub>T</sub> to V <sub>ref</sub> and capacitor C <sub>T</sub> to ground.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sink by this pin.
7	V <sub>CC</sub>	This pin is the positive supply of the integrated circuit.
8	V <sub>ref</sub>	This is the reference output. It provides charging current for capacitor C <sub>T</sub> through resistor R <sub>T</sub> .

### Application information

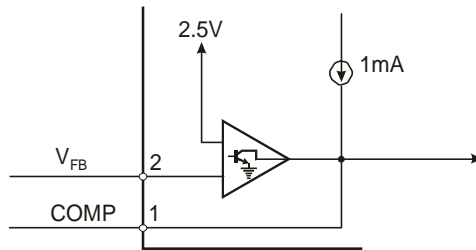


Figure 1. Error Amp Configuration

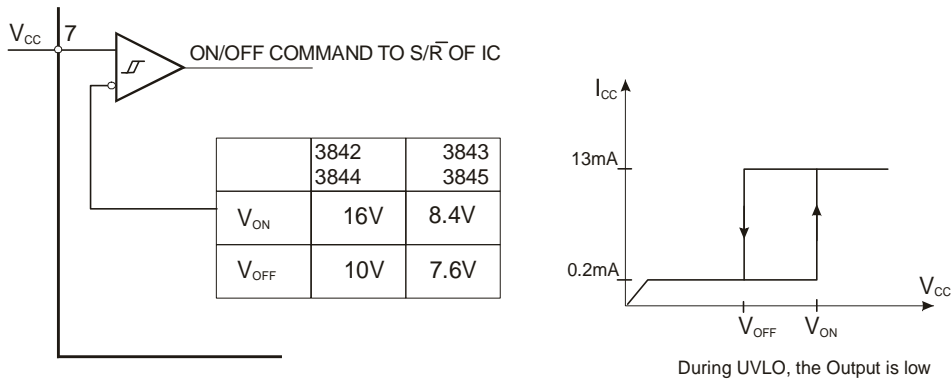


Figure 2. Undervoltage Lockout

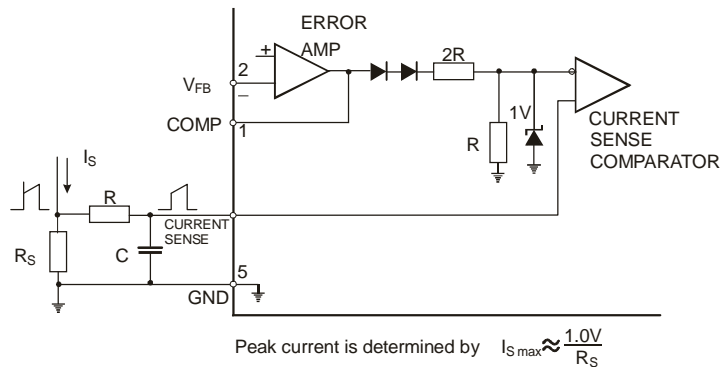


Figure 3. Current Sense Circuit

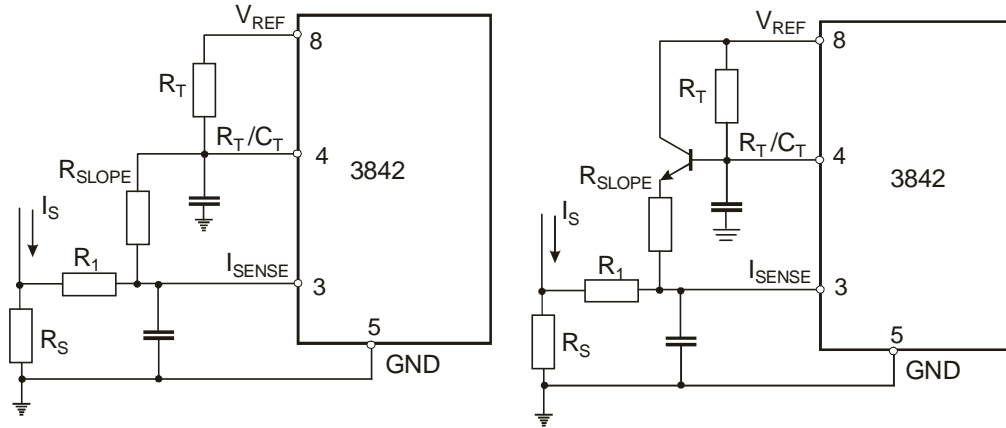
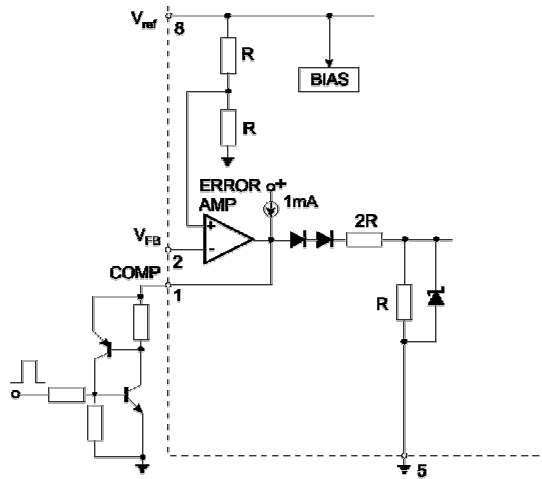
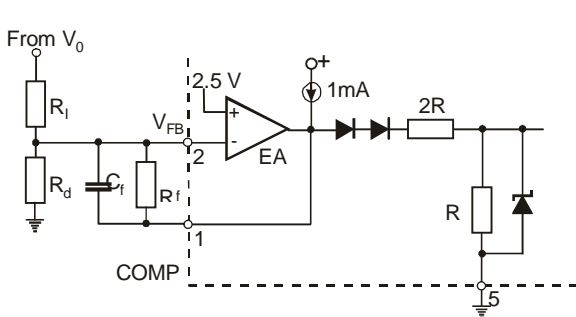


Figure 4. Slope Compensation Techniques

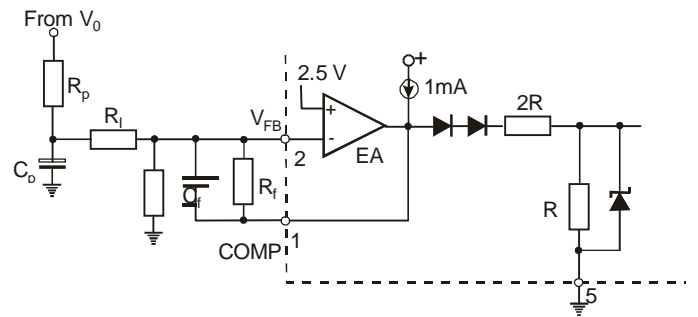


SCR must be selected for a holding current of less than 0.5mA.  
The simple two transistor circuit can be used in place of the SCR as shown.

Figure 5. Latched Shutdown



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 6. Error Amplifier Compensation

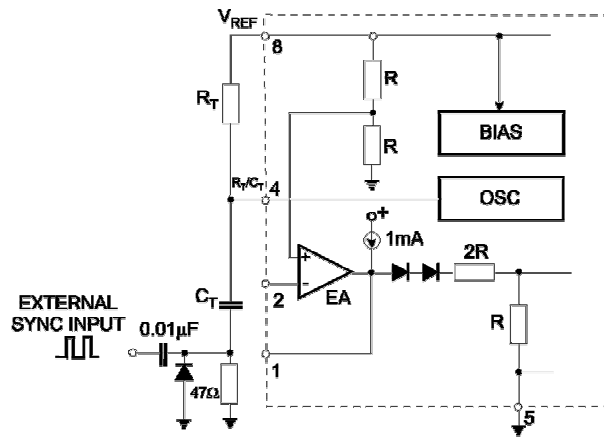


Figure 7. External Clock Synchronization

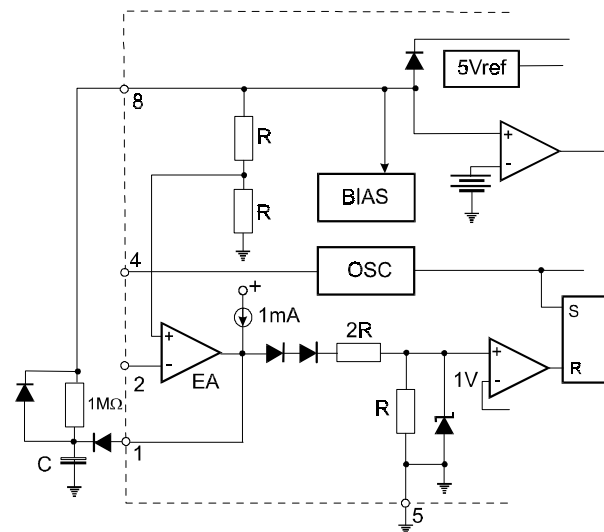


Figure 8. Soft-Start Circuit

Typical Performance Characteristics

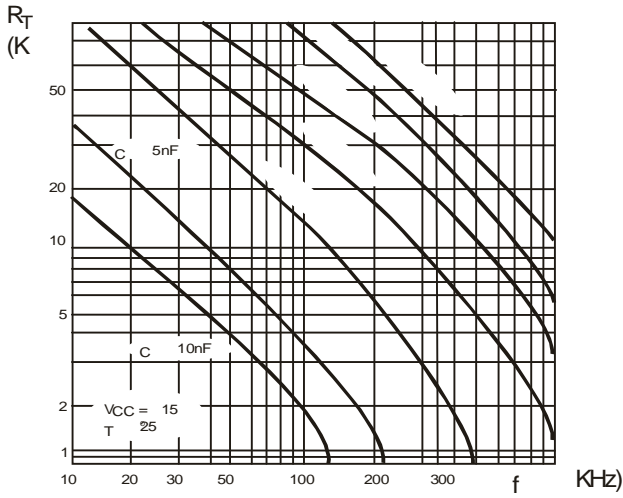


Figure 1. Timing Resistor vs. Oscillator Frequency.

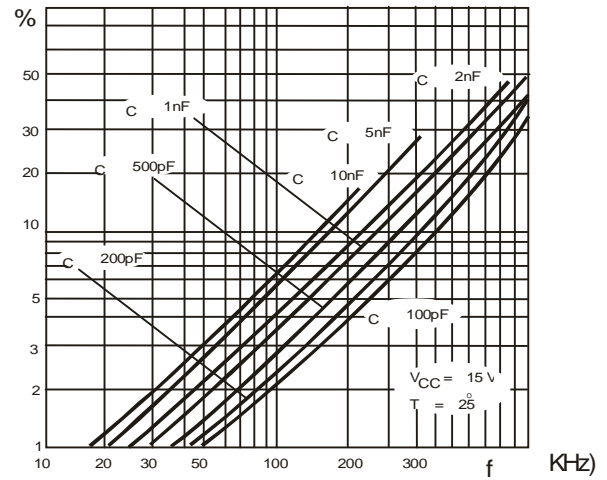


Figure 2. Output Dead-Time vs. Oscillator Frequency.

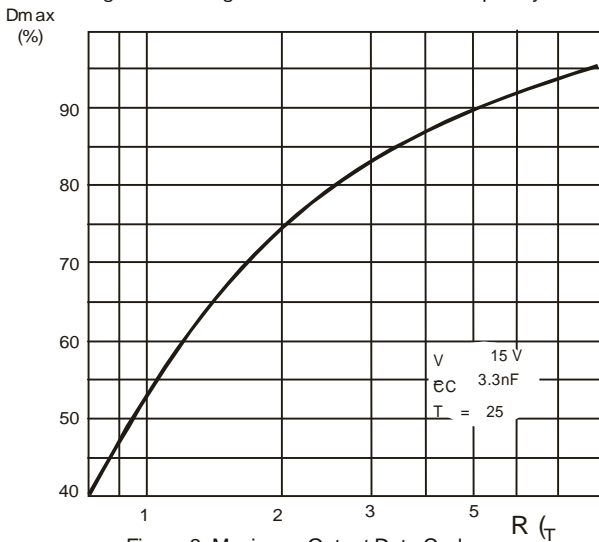


Figure 3. Maximum Output Duty Cycle vs. Timing Resistor (3842/43).

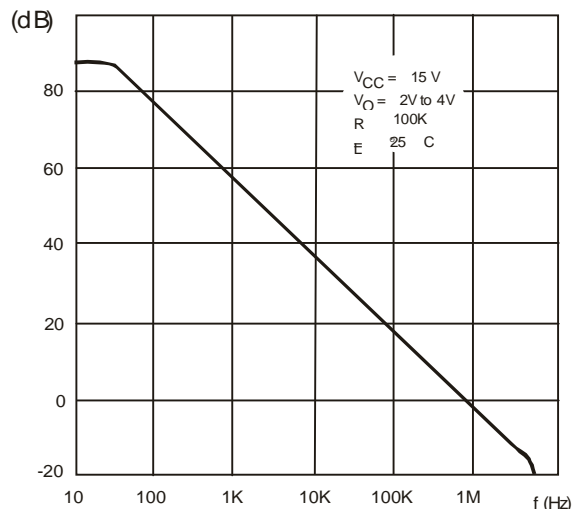


Figure 4. Error Amp Open-Loop Gain vs. Frequency.

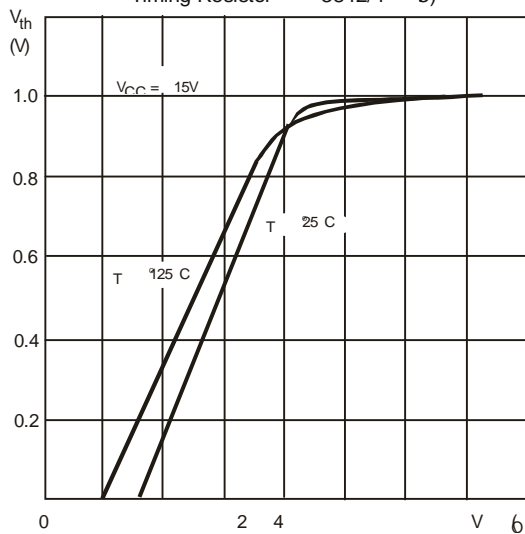


Figure 5. Current Sense Input Threshold vs. Error Amp Output Voltage.

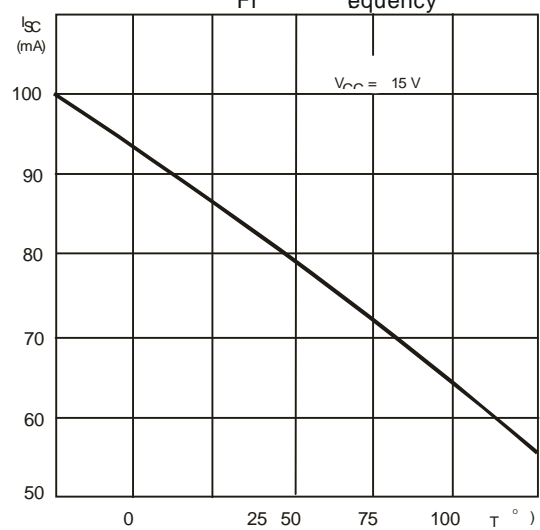


Figure 6. Reference Short Circuit Current vs. Temperature.

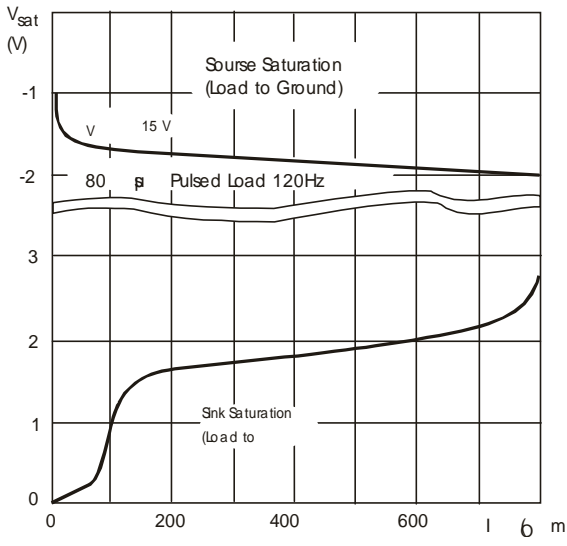


Figure 7 Output Saturation Voltage vs. Load

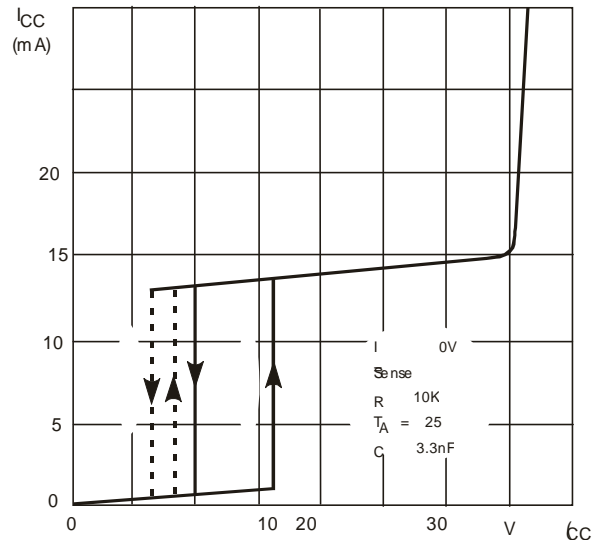


Figure 8 Supply Current vs. Supply

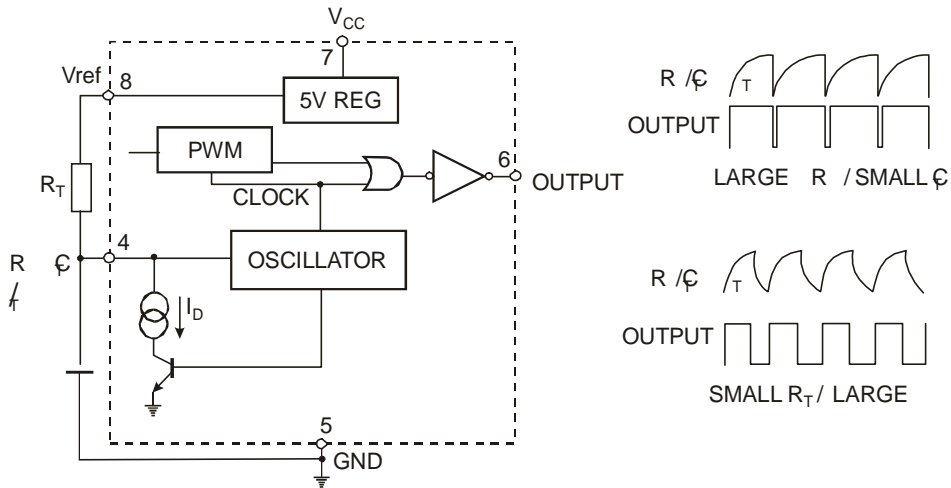




Figure 9. Oscillator and Output Waveforms

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