THE DATASHEET OF

ADP1876ACPZ-R7

600 kHz Dual Output Synchronous Buck PWM Controller with Linear Regulator

Data Sheet **ADP1876**

FEATURES

- Wide input range: 2.75 V to 20 V
- Power stage input voltage: 1 V to 20 V
- Output voltage range: 0.6 V up to 90% V_{IN}
- Linear dropout (LDO) regulator with a fixed output 1.5 V at 150 mA
- Output current more than 25 A per channel
- 180° phase shift between channels for reduced input capacitance
- ±0.85% reference voltage accuracy from −40°C to +85°C
- Integrated boost diodes
- Independent channel precision enable
- Overcurrent limit protection
- Externally programmable soft start, slope compensation, and current sense gain
- Thermal overload protection
- Input undervoltage lockout (UVLO)
- Power good with internal pull-up resistor
- Available in 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- Consumer applications
- Telecommunications base station and networking
- Industrial and instrumentation

TYPICAL OPERATION CIRCUIT

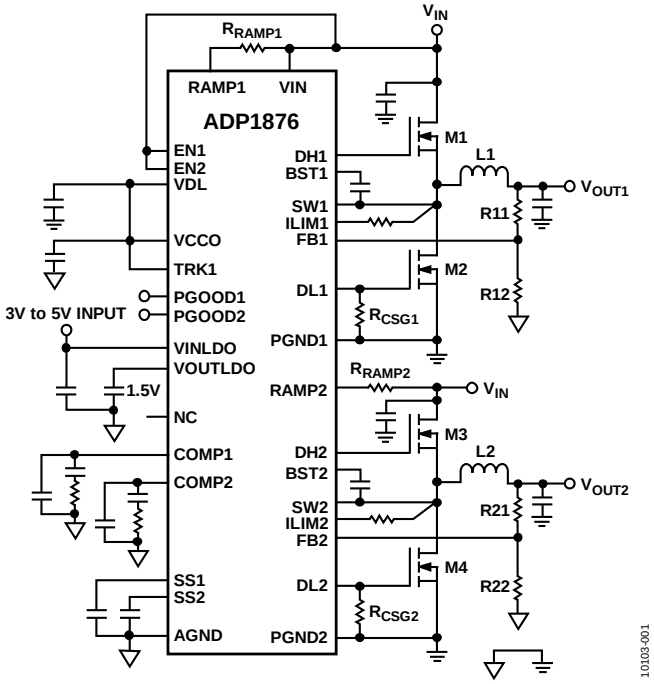

Figure 1.

GENERAL DESCRIPTION

The ADP1876 is a dual output dc-to-dc synchronous buck controller operating at 600 kHz fixed frequency with integrated drivers that drive N-channel power MOSFETs. An additional fixed voltage output, 150 mA linear regulator is available for powering low power loads. The device operates in current mode for improved transient response and uses valley current sensing for enhanced noise immunity. The two PWM outputs are phase shifted 180° for reducing the input current ripple and the required input capacitance.

The ADP1876 provides high speed, high peak current drive capability with dead time optimization to enable energy efficient power conversion.

Rev. B

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REVISION HISTORY

3/2017—Rev. A to Rev. B

Changed CP-32-11 to CP-32-12 ... Throughout
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11/2011—Rev. 0 to Rev. A

Added Evaluation Board to Ordering Guide ... 24

9/2011—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

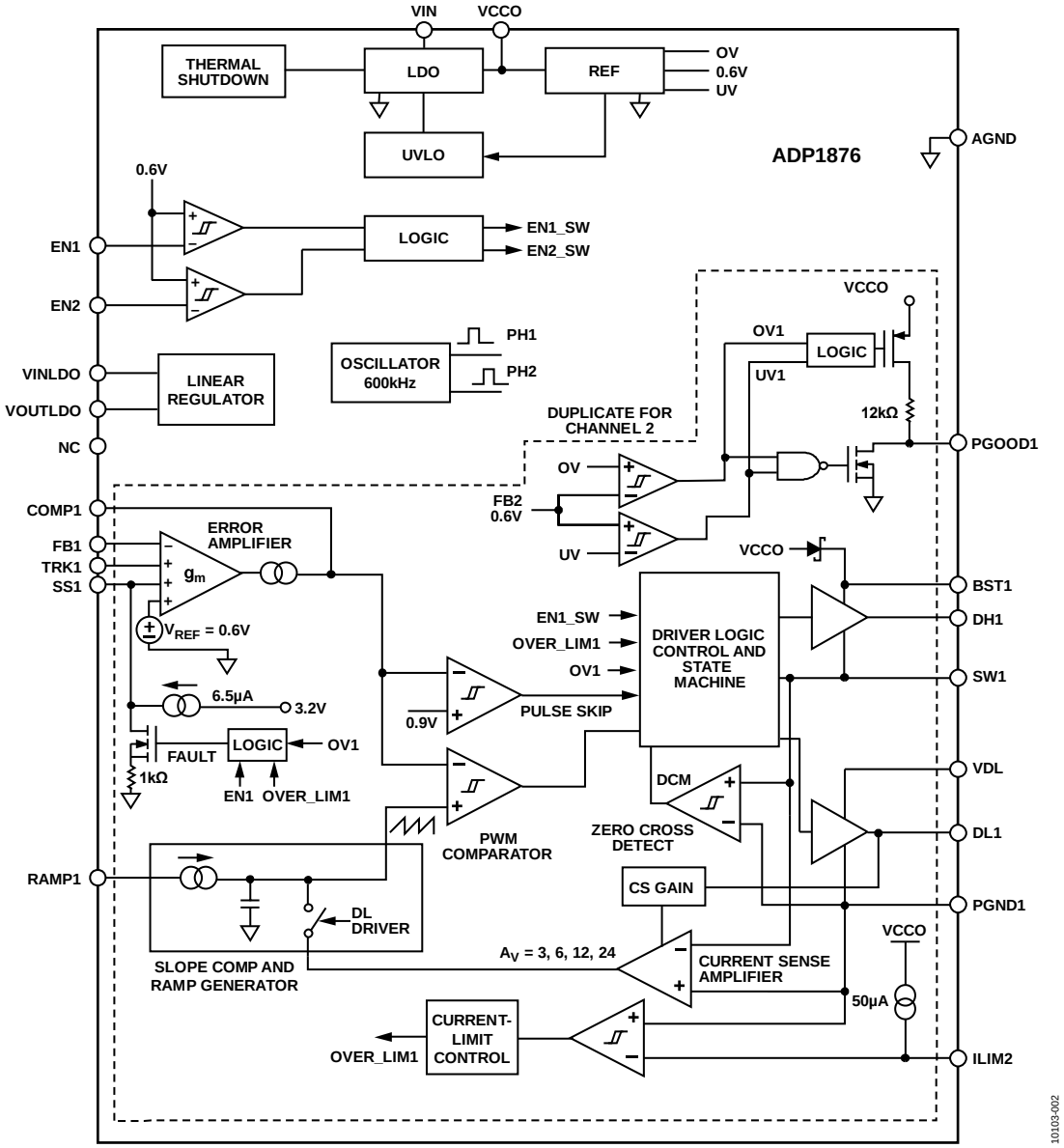


Figure 2. Functional Block Diagram

SPECIFICATIONS

All limits at temperature extremes are guaranteed via correlation using standard statistical quality control. V_{IN} = 12 V. The specifications are valid for T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_A = 25°C.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Input Voltage	V_{IN}		2.75		20	V
Undervoltage Lockout Threshold	IN_{UVLO}	V_{IN} rising	2.45	2.6	2.75	V
		V_{IN} falling	2.4	2.5	2.6	
Undervoltage Lockout Hysteresis				0.1		V
Quiescent Current	I_{IN}	EN1 = EN2 = V_{IN} = 12 V, V_{FB} = V_{CCO} (no switching)		4.5	5.9	mA
Shutdown Current	I_{IN_SD}	EN1 = EN2 = GND, V_{IN} = 5.5 V or 20 V		100	200	µA
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB}		−100	+1	+100	nA
Transconductance	g_m	Sink or source 1 µA	385	550	715	µS
TRK1 Input Bias Current	I_{TRK}	0 V < V_{TRK1} < 1.5 V	−100	+1	+100	nA
CURRENT SENSE AMPLIFIER GAIN	A_{CS}	Gain resistor connected to DLx, R_{CSG} = 47 kΩ ± 5%	2.4	3	3.6	V/V
		Gain resistor connected to DLx, R_{CSG} = 22 kΩ ± 5%	5.2	6	6.9	V/V
		Default setting, R_{CSG} = open	10.5	12	13.5	V/V
		Gain resistor connected to DLx, R_{CSG} = 100 kΩ ± 5%	20.5	24	26.5	V/V
OUTPUT CHARACTERICTISTICS						
Feedback Accuracy Voltage	V_{FB}	T_J = −40°C to +85°C, V_{FB} = 0.6 V	−0.85%	+0.6	+0.85%	V
		T_J = −40°C to +125°C, V_{FB} = 0.6 V	−1.5%	+0.6	+1.5%	V
Line Regulation of PWM	$\Delta V_{FB}/\Delta V_{IN}$			±0.015		%/V
Load Regulation of PWM	$\Delta V_{FB}/\Delta V_{COMP}$	V_{COMP} range 0.9 V to 2.2 V		±0.3		%
Oscillator Frequency	f_{OSC}		475	600	690	kHz
LINEAR REGULATOR VCCO						
VCCO Output Voltage		T_A = 25°C, I_{VCCO} = 100 mA	4.8	5.0	5.18	V
		T_J = −40°C to +125°C	4.7	5.0	5.3	V
VCCO Load Regulation		I_{VCCO} = 0 mA to 100 mA,		35		mV
VCCO Line Regulation		V_{IN} = 5.5 V to 20 V, I_{VCCO} = 20 mA		10		mV
VCCO Short-Circuit Current[1]		VCCO < 0.5 V		370	400	mA
VIN to VCCO Dropout Voltage[2]	$V_{DROPOUT}$	I_{VCCO} = 100 mA, V_{IN} ≤ 5 V		0.33		V
LOGIC INPUTS						
EN1, EN2 Threshold		EN1/EN2 rising	0.57	0.63	0.68	V
EN1, EN2 Hysteresis				0.03		V
EN1, EN2 Input Leakage Current	I_{EN}	V_{IN} = 2.75 V to 20 V		1	200	nA
GATE DRIVERS (DHx, DLx PINS)						
DHx Rise Time		C_{DH} = 3 nF, V_{BST} − V_{SW} = 5 V		16		ns
DHx Fall Time		C_{DH} = 3 nF, V_{BST} − V_{SW} = 5 V		14		ns
DLx Rise Time		C_{DL} = 3 nF		16		ns
DLx Fall Time		C_{DL} = 3 nF		14		ns
DHx to DLx Dead Time		External 3 nF capacitor is connected to DHx and DLx		25		ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DHx or DLx Driver R_{ON}, Sourcing Current[1]	R_{ON_SOURCE}	Sourcing 2 A with a 100 ns pulse		2		Ω
		Sourcing 1 A with a 100 ns pulse, V_{IN} = 3 V		2.3		Ω
DHx or DLx Driver R_{ON}, Tempco	TC_{RON}	V_{IN} = 3 V or 12 V		0.3		%/°C
DHx or DLx Driver R_{ON}, Sinking Current[1]	R_{ON_SINK}	Sinking 2 A with a 100 ns pulse		1.5		Ω
		Sinking 1 A with a 100 ns pulse, V_{IN} = 3 V		2		Ω
DHx Maximum Duty Cycle		f_{OSC} = 600 kHz		76		%
Minimum DHx On Time					130	ns
Minimum DHx Off Time					340	ns
Minimum DLx On Time					290	ns
COMP VOLTAGE RANGE	V_{COMP}		0.85		2.3	V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{TMSD}			155		°C
Thermal Shutdown Hysteresis				20		°C
OVERVOLTAGE AND POWER-GOOD THRESHOLDS (FBx PINS)						
FBx Overvoltage Threshold	V_{OV}	V_{FB} rising	0.67	0.7	0.73	V
FBx Overvoltage Hysteresis				40		mV
FBx Undervoltage Threshold	V_{UV}	V_{FB} rising	0.51	0.54	0.57	V
FBx Undervoltage Hysteresis				30		mV
FB1 TO TRK1 OFFSET VOLTAGE		TRK1 = 0.3 V to 0.55 V, offset = $V_{FB} - V_{TRK}$	−120		+50	mV
SOFT START (SSx Pins)						
SSx Output Current	I_{SS}	During start-up	4.6	6.5	8.4	µA
SSx Pull-Down Resistor		During a fault condition		1		kΩ
POWER GOOD (PGOODx Pins)						
PGOODx Pull-up Resistor	R_{PGOOD}	Internal pull-up resistor to VCCO		12.5		kΩ
PGOODx Delay				12		µs
Overvoltage or Undervoltage Minimum Duration		This is the minimum duration required to trip the PGOODx signal		12		µs
ILIM1, ILIM2 Threshold Voltage[1]		Relative to PGNDx	−5	0	+5	mV
ILIM1, ILIM2 Output Current		ILIMx = PGNDx	40	50	60	µA
Current Sense Blanking Period		After DLx goes high, current limit is not sensed during this period		100		ns
INTEGRATED RECTIFIER (BOOST DIODE) RESISTANCE		At 20 mA forward current		16		Ω
INDEPENDENT LOW DROPOUT LINEAR REGULATOR						
VINLDO Voltage Range	V_{INLDO}	Input range	2.7		5.5	V
VOUTLDO Voltage	V_{OUTLDO}	V_{INLDO} = 2.7 V to 5.5 V, I_{OUTLDO} = 1 mA to 150 mA	1.47	1.5	1.53	V
VOUTLDO Maximum Load	V_{OUTLDO}	V_{INLDO} = 2.7 V to 5.5 V			150	mA
Quiescent Current	I_{INLDO}	V_{INLDO} = 2.7 V to 5.5 V, no load at output		30	60	µA
Line Regulation	ΔV_{OUTLDO}	I_{OUTLDO} = 150 mA, V_{INLDO} = 2.7 V to 5.5 V			0.3	%
Load Regulation	ΔV_{OUTLDO}	V_{INLDO} = 2.7 V to 5.5 V, I_{OUTLDO} = 1 mA to 150 mA			0.4	%
Power Supply Rejection Ratio	PSRR	1 kHz, V_{INDLO} = 2.7 V to 5.5 V, 10 mA load		70		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RMS Output Noise	N	10 Hz to 100 kHz, VINLDO = 5 V		40		μV rms
Short-Circuit Current		V_{OUTLDO} = GND		400		mA
Undervoltage Lockout Threshold	V_{INLDO_UVLO}	V_{INLDO} rising	2.35	2.5	2.65	V
Undervoltage Lockout Hysteresis		V_{INLDO}		0.18		V

[1] Guaranteed by design. Not production tested.
[2] Connect V_{IN} to VCCO when V_{IN} < 5.5 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN1/EN2, RAMP1/RAMP2	21 V
FB1/FB2, COMP1/COMP2, SS1/SS2, TRK1, VINLDO, VOUTLDO, VCCO, VDL, PGOOD1/PGOOD2	−0.3 V to +6 V
ILIM1/ILIM2	−0.3 V to +21 V
BST1/BST2 to SW1/SW2	−0.3 V to +6 V
BST1/BST2, DH1/DH2, SW1/SW2 to PGND1/PGND2	−0.3 V to +28 V
DL1/DL2 to PGND1/PGND2	−0.3 V to VCCO + 0.3 V
BST1/BST2 to PGND1/PGND2, SW1/SW2 to PGND1/PGND2 (20 ns Transients)	32 V
SW1, SW2 to PGND1, PGND2 (20 ns Transients)	25 V
DL1/DL2, SW1/SW2, ILIM1/ILIM2 to PGND1/PGND2 (20 ns Negative Transients)	−8 V
PGND1/PGND2 to AGND	−0.3 V to +0.3 V
PGND1/PGND2 to AGND (20 ns Transients)	−8 V to +4 V
θ_{JA}, Multilayer PCB (Natural Convection)[1, 2]	32.6°C/W
Operating Junction Temperature Range[3]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Soldering Lead Temperature	260°C

[1] Measured with exposed pad attached to the printed circuit board (PCB).
[2] Junction-to-ambient thermal resistance (θ_{JA}) of the package was calculated or simulated on a multilayer PCB.
[3] The junction temperature, T_J, of the device is dependent on the ambient temperature, T_A, the power dissipation of the device, P_D, and the junction to ambient thermal resistance of the package, θ_{JA}. Maximum junction temperature is calculated from the ambient temperature and power dissipation using the formula, $T_J = T_A + P_D \times \theta_{JA}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

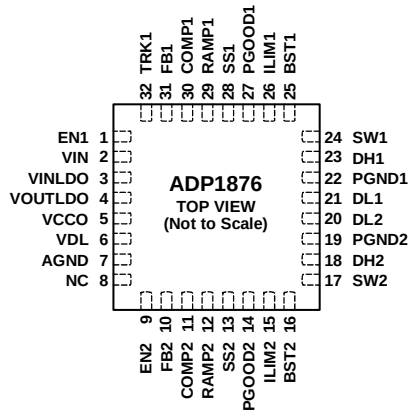


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN1	Enable Input for Channel 1. Drive EN1 high to turn on the Channel 1 controller, and drive it low to turn it off. Tie EN1 to VIN for automatic startup. For a precision UVLO, put an appropriately sized resistor divider from VIN to AGND and tie the midpoint to this pin.
2	VIN	Connect to Main Power Supply. Bypass with a 1 µF or larger ceramic capacitor connected as close to this pin as possible and PGNDx.
3	VINLDO	Input for Independent Linear Dropout (LDO) Regulator.
4	VOUTLDO	Output for Independent LDO Regulator.
5	VCCO	Output of the Internal LDO. The internal circuitry and gate drivers are powered from VCCO. Bypass VCCO to AGND with a 1 µF or larger ceramic capacitor. The VCCO output is always active, even during fault conditions, and it cannot be turned off even when EN1 or EN2 is low. For operation at VIN below 5 V, VIN can be jumped to VCCO. Do not use the VCCO to power any other auxiliary system load.
6	VDL	Power Supply for the Low-Side Driver. Bypass VDL to PGNDx with a 1 µF ceramic capacitor. Connect VCCO to VDL.
7	AGND	Analog Ground.
8	NC	No connect. Do not connect to this pin.
9	EN2	Enable Input for Channel 2. Drive EN2 high to turn on the Channel 2 controller, and drive it low to turn off. Tie EN2 to VIN for automatic startup. For a precision UVLO, put an appropriately sized resistor divider from VIN to AGND and tie the midpoint to this pin.
10	FB2	Output Voltage Feedback for Channel 2.
11	COMP2	Compensation Node for Channel 2. Output of the Channel 2 error amplifier. Connect a series resistor/capacitor network from COMP2 to AGND to compensate the regulation control loop.
12	RAMP2	Programmable Current Setting for Slope Compensation of Channel 2. Connect a resistor from RAMP2 to VIN. The voltage at RAMP2 is 0.2 V during operation. This pin is high impedance when the channel is disabled.
13	SS2	Soft Start Input for Channel 2. Connect a capacitor from SS2 to AGND to set the soft start period. This node is internally pulled up to 3.2 V through a 6.5 µA current source.
14	PGOOD2	Open-Drain Power-Good Indicator Logic Output at PGOOD2. An internal 12 kΩ resistor is connected between PGOOD2 and VCCO. PGOOD2 is pulled to ground when the Channel 2 output is outside the regulation window. An external pull-up resistor is not required.
15	ILIM2	Current-Limit Sense Comparator Inverting Input for Channel 2. Connect a resistor between ILIM2 and SW2 to set the current-limit offset. For accurate current-limit sensing, connect ILIM2 to a current sense resistor at the source of the low-side MOSFET.
16	BST2	Boot Strapped Upper Rail of High-Side Internal Driver for Channel 2. Connect a 0.1 µF to 0.22 µF multilayer ceramic capacitor (MLCC) between BST2 and SW2. There is an internal boost rectifier connected between VDL and BST2.
17	SW2	Switch Node for Channel 2. Connect to the source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET of Channel 2.
18	DH2	High-Side Switch Gate Driver Output for Channel 2.

Pin No.	Mnemonic	Description
19	PGND2	Power Ground for Channel 2. Ground for Internal Channel 2 driver. Differential current is sensed between SW2 and PGND2. Directly shorting PGND2 to PGND1 is not recommended.
20	DL2	Low-Side Synchronous Rectifier Gate Driver Output for Channel 2. To set the gain of the current sense amplifier, connect a resistor between DL2 and PGND2.
21	DL1	Low-Side Synchronous Rectifier Gate Driver Output for Channel 1. To set the gain of the current sense amplifier, connect a resistor between DL1 and PGND1.
22	PGND1	Power Ground for Channel 1. Ground for internal Channel 1 driver. Differential current is sensed between SW1 and PGND1. Directly shorting PGND2 to PGND1 is not recommended.
23	DH1	High-Side Switch Gate Driver Output for Channel 1.
24	SW1	Power Switch Node for Channel 1. Connect SW1 to the source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET of Channel 1.
25	BST1	Boot Strapped Upper Rail of High-Side Internal Driver for Channel 1. Connect a 0.1µF to 0.22 µF multilayer ceramic capacitor (MLCC) between BST1 and SW1. There is an internal boost diode or rectifier connected between VDL and BST1.
26	ILIM1	Current-Limit Sense Comparator Inverting Input for Channel 1. Connect a resistor between ILIM1 and SW1 to set the current-limit offset. For accurate current-limit sensing, connect ILIM1 to a current sense resistor at the source of the low-side MOSFET.
27	PGOOD1	Open-Drain Power-good Indicator Logic Output. PGOOD1 includes an internal 12 kΩ resistor connected between PGOOD1 and VCCO. PGOOD1 is pulled to ground when the Channel 1 output is outside the regulation window. An external pull-up resistor is not required.
28	SS1	Soft Start Input for Channel 1. Connect a capacitor from SS1 to AGND to set the soft start period. This node is internally pulled up to 3.2 V through a 6.5 µA current source.
29	RAMP1	Programmable Current Setting for Channel 1 Slope Compensation. Connect a resistor from RAMP1 to VIN. The voltage at RAMP1 is 0.2 V during operation. This pin is high impedance when the channel is disabled.
30	COMP1	Compensation Node For Channel 1. Output of Channel 1 error amplifier. Connect a series resistor/capacitor network from COMP1 to AGND to compensate the regulation control loop.
31	FB1	Output Voltage Feedback for Channel 1.
32	TRK1	Tracking Input for Channel 1.

TYPICAL PERFORMANCE CHARACTERISTICS

Test conditions are at T_A = 25°C and V_{IN} = 12 V, unless otherwise specified.

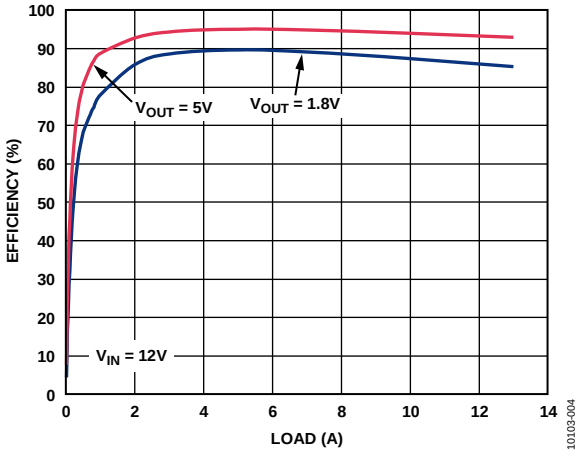


Figure 4. Efficiency Plot of Figure 33

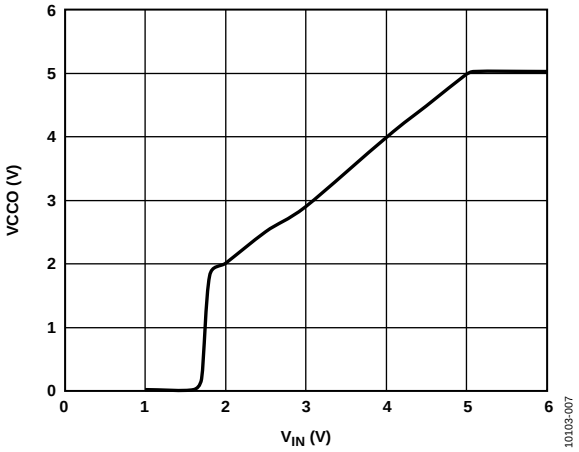


Figure 7. VCCO vs. V_{IN}

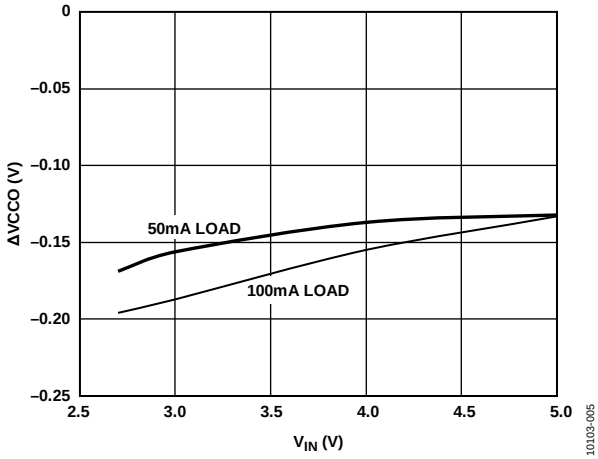


Figure 5. VCCO Dropout

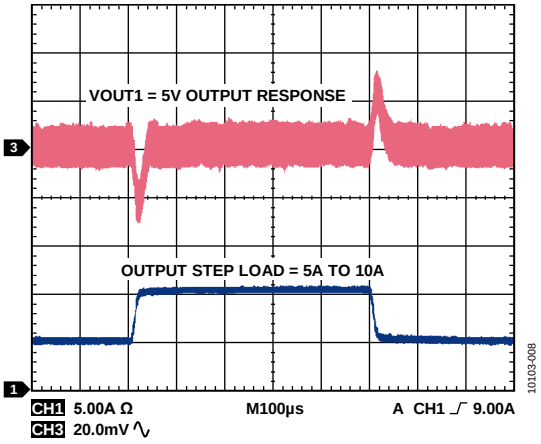


Figure 8. Step Load Transient of Figure 33

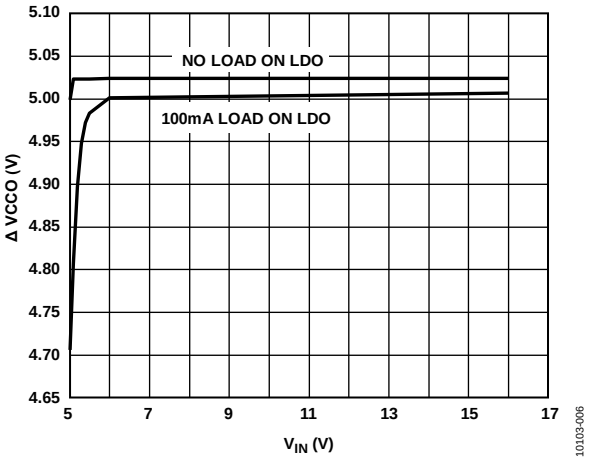


Figure 6. VCCO Line Regulation

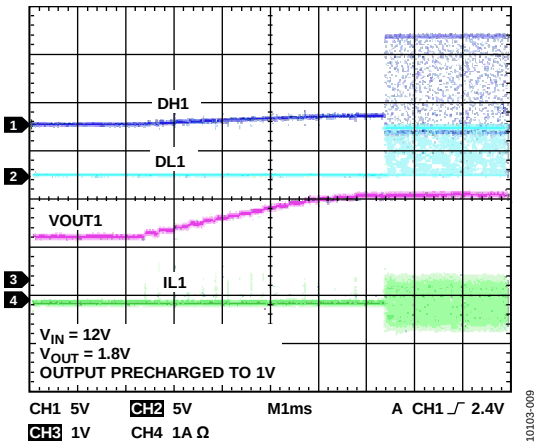


Figure 9. Soft Start Into Precharged Output

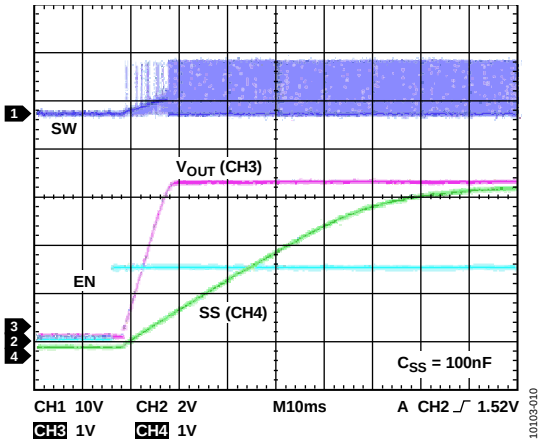


Figure 10. Enable Startup Function

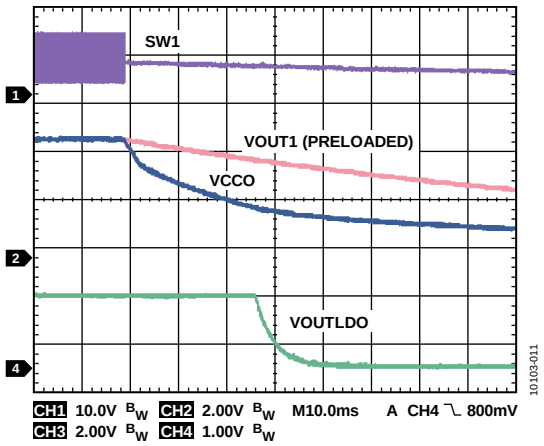


Figure 11. Thermal Shutdown Waveform

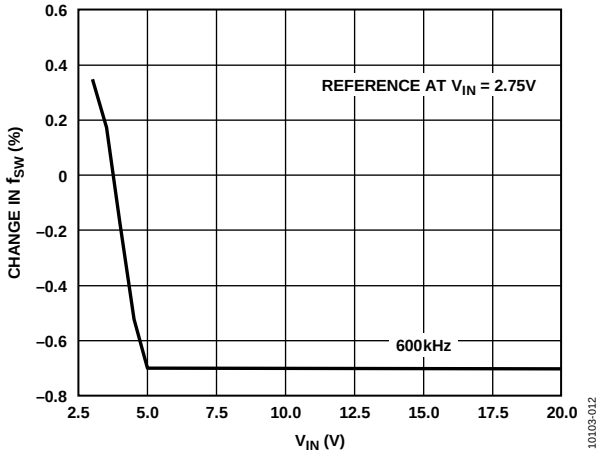


Figure 12. Change in f_{SW} vs. V_{IN}

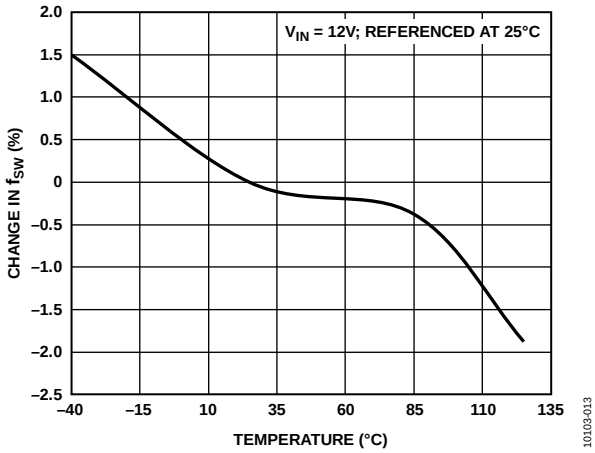


Figure 13. f_{SW} vs. Temperature

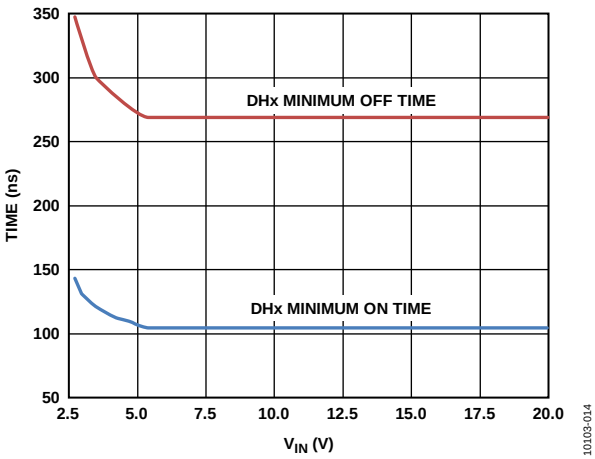


Figure 14. Typical DHx Minimum On Time and Off Time

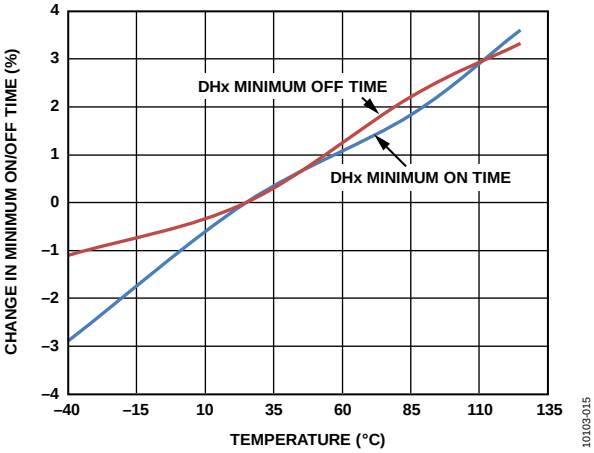


Figure 15. DHx Minimum On Time and Off Time Over Temperature

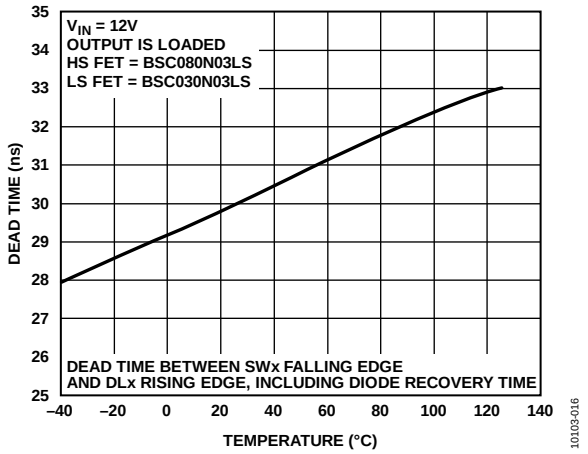


Figure 16. Dead Time vs. Temperature

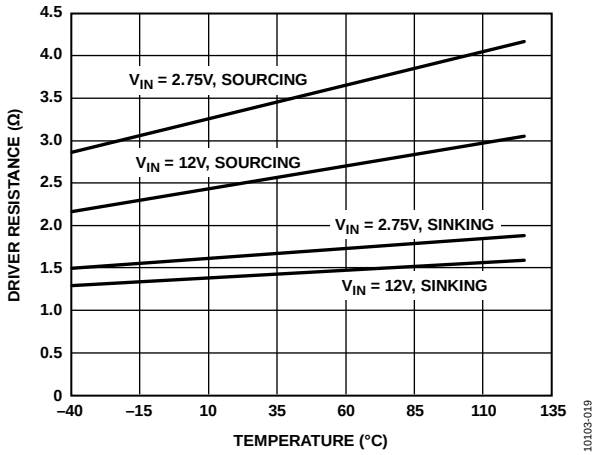


Figure 19. Driver Resistance vs. Temperature

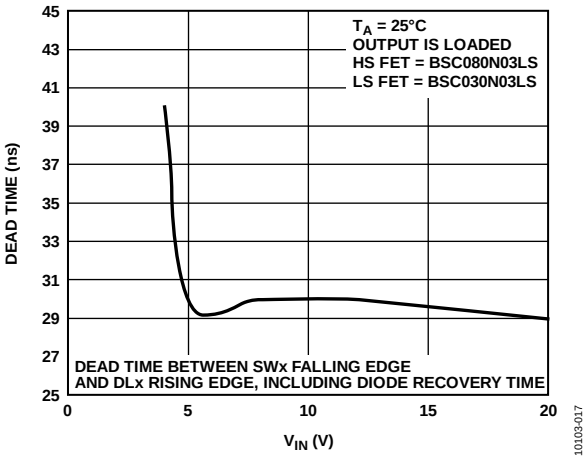


Figure 17. Dead Time vs. V_{IN}

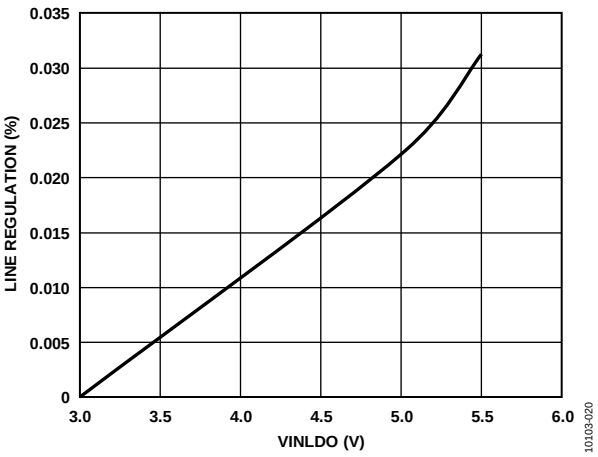


Figure 20. VOUTLDO Line Regulation

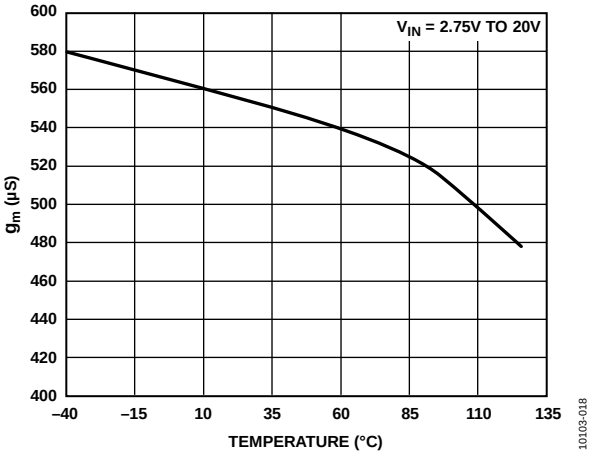


Figure 18. g_m of Error Amplifier vs. Temperature

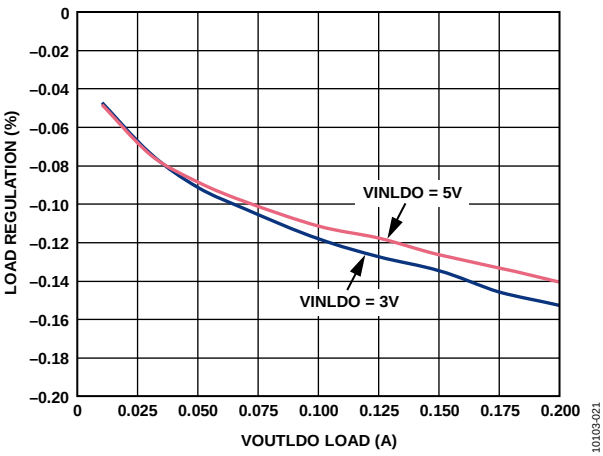


Figure 21. VOUTLDO Load Regulation

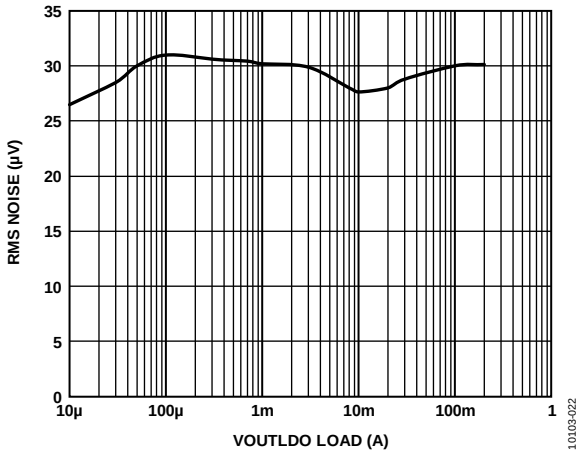


Figure 22. VOUTLDO Noise Spectral Density

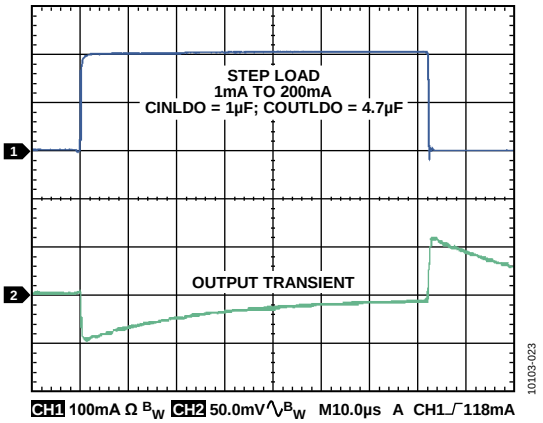


Figure 23. VOUTLDO Step Load Transient

THEORY OF OPERATION

The ADP1876 is a dual output dc-to-dc synchronous buck controller with integrated drivers that drive N-channel power MOSFETs. The device operates in current mode for improved transient response and uses valley current sensing for enhanced noise immunity. The two outputs are phase shifted 180°. This reduces the input current ripple and the required input capacitance.

The integrated boost diodes in the ADP1876 reduce the overall system cost and component count. The ADP1876 operates at a fixed frequency of 600 kHz and includes programmable soft start, current limit, and power good.

INDEPENDENT LOW DROPOUT LINEAR REGULATOR

In addition to the dual channel step-down controller, a stand-alone linear dropout (LDO) voltage regulator with a fixed output of 1.5 V is built into the ADP1876 and operates independently from the controllers. The output of the LDO delivers up to 150 mA to the load. See the Applications Information section for more information.

CONTROLLER ARCHITECTURE

The ADP1876 is based on a fixed frequency, current mode PWM control architecture. The inductor current is sensed by the voltage drop measured across the external low-side MOSFET R_{DSON} during the off period of the switching cycle (valley inductor current). The current sense signal is further processed by the current sense amplifier. The output of the current sense amplifier is held, and the emulated current ramp is multiplexed and fed into the PWM comparator (see Figure 24). The valley current information is captured at the end of the off period, and the emulated current ramp is applied at that point when the next on cycle begins. An error amplifier integrates the error between the feedback voltage and the generated error voltage from the COMP pin (see the "from error amp" in Figure 24).

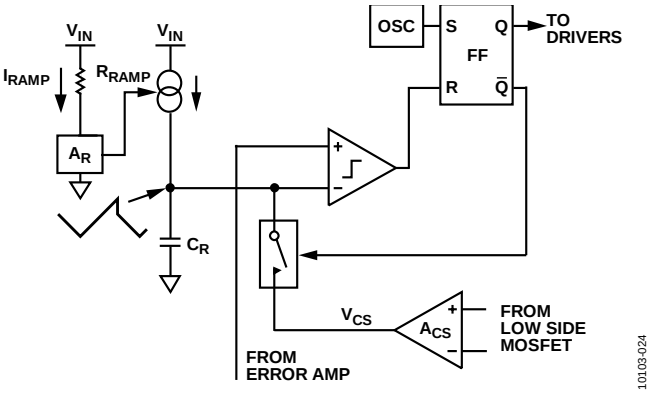


Figure 24. Simplified Control Architecture

As shown in Figure 24, the emulated current ramp is generated inside the IC but offers programmability through the RAMPx pin (see Figure 1 for the typical operation circuit). Selecting an appropriate value resistor from V_{IN} to the RAMPx pin programs a desired slope compensation value and, at the same time, provides a feedforward feature. The benefits realized by deploying this type of control scheme are as follows:

- The turn-on current spike does not corrupt the current ramp.
- The current signal is stable because the current signal is sampled at the end of the turn-off period, which gives time for the switch node ringing to settle.

The normal benefits of using current mode control scheme still apply, such as simplicity of loop compensation. Control logic enforces antishoot through operation to limit cross conduction of the internal drivers and external MOSFETs.

Synchronous Rectifier and Dead Time

The synchronous rectifier (low-side MOSFET) improves efficiency by replacing the Schottky diode that is normally used in an asynchronous buck regulator. In the ADP1876, the antishoot through circuit monitors the SW and DL nodes and adjusts the low-side and high-side drivers to ensure break-before-make switching to prevent cross conduction or shoot through between the high-side and low-side MOSFETs. This break-before-make switching is known as the dead time, which is not fixed and depends on how fast the MOSFETs are turned on and off. In a typical application circuit that uses medium sized MOSFETs with input capacitance of approximately 3 nF, the typical dead time is approximately 30 ns. When small and fast MOSFETs are used, the dead time can be as low as 13 ns.

INPUT UNDERVOLTAGE LOCKOUT

When the bias input voltage, V_{IN}, is less than the undervoltage lockout (UVLO) threshold, the switch drivers stay inactive. When V_{IN} exceeds the UVLO threshold, the switchers begin switching.

INTERNAL LINEAR REGULATOR (VCCO)

The internal linear regulator is low dropout, meaning it can regulate its output voltage, VCCO. VCCO powers the internal control circuitry and provides power for the gate drivers. It is guaranteed to have more than 200 mA of output current capability, which is sufficient to handle the gate drive requirements of typical logic threshold MOSFETs. VCCO is always active and cannot be shut down by the EN1/EN2 pins. Bypass VCCO to AGND with a 1 µF or greater capacitor.

Because the LDO supplies the gate drive current, the output of VCCO is subject to sharp transient currents as the drivers switch and the boost capacitors recharge during each switching cycle.

The LDO has been optimized to handle these transients without overload faults. Due to the gate drive loading, using the VCCO output for other external auxiliary system loads is not recommended.

The LDO includes a current limit well above the expected maximum gate drive load. This current limit also includes a short-circuit fold back to further limit the VCCO current in the event of a short-circuit fault.

The VDL pin provides power to the low-side driver. Connect VDL to VCCO. Bypass VDL to PGND with a 1 µF (minimum) ceramic capacitor, which must be placed close to the VDL pin.

For an input voltage of less than 5.5 V, it is recommended to bypass the LDO by connecting VIN to VCCO, as shown in Figure 25, thus eliminating the dropout voltage. However, for example, if the input range is 4 V to 7 V, the LDO cannot be bypassed by shorting VIN to VCCO because the 7 V input has exceeded the maximum voltage rating of the VCCO pin. In this case, use the LDO to drive the internal drivers noting that there is a dropout when V_{IN} is less than 5 V.

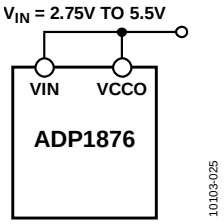


Figure 25. Configuration for V_{IN} < 5.5 V

OVERVOLTAGE PROTECTION

The ADP1876 operates at a 600 kHz fixed frequency PWM. When the output is shorted to a voltage higher than the regulation voltage, the duty cycle of the controller modulates to keep the output stable at the preset regulation voltage by sinking current through the low-side N-channel MOSFET during the off cycle.

POWER GOOD

The PGOODx pin is an open-drain NMOS with an internal 12 kΩ pull-up resistor connected between PGOODx and VCCO. PGOODx is internally pulled up to VCCO during normal operation and is active low when tripped. When the feedback voltage, V_{FB}, rises above the overvoltage threshold or drops below the undervoltage threshold, the PGOODx output is pulled to ground after a delay of 12 µs. The overvoltage or undervoltage condition must exist for more than 12 µs for PGOODx to become active. The PGOODx output also becomes active if a thermal overload condition is detected.

SHORT-CIRCUIT AND CURRENT-LIMIT PROTECTION

When the output is shorted or the output current exceeds the current limit set by the current-limit setting resistor (between ILIMx and SWx) for eight consecutive cycles, the ADP1876 shuts off both the high-side and low-side drivers and restarts the soft start sequence every 10 ms, which is known as hiccup mode. The SS node discharges to zero through an internal 1 kΩ resistor during an overcurrent or short-circuit event. Figure 26 shows that the ADP1876 (a 20 A application circuit) is entering current-limit hiccup mode when the output is shorted.

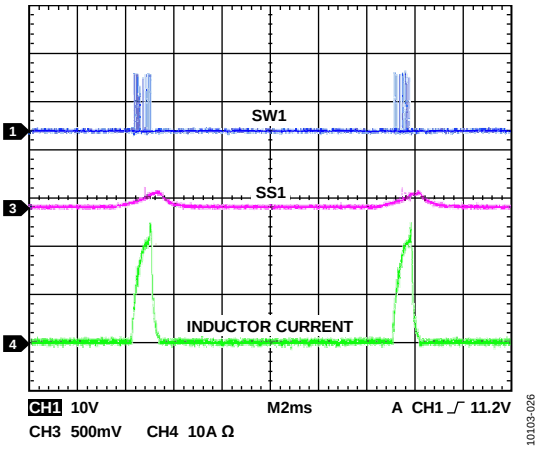


Figure 26. Current-Limit Hiccup Mode, 20 A Circuit

SHUTDOWN CONTROL

The EN1 and EN2 pins enable or disable Channel 1 and Channel 2, respectively, of the ADP1876. The precision enable threshold for EN1 or EN2 is typically 0.63 V. When the EN1 or EN2 voltage rises above 0.63 V, the ADP1876 is enabled and starts normal operation after the soft start period. When the voltage at ENx drops below 0.57 V, the switchers and the internal circuits in the ADP1876 are turned off. Note that EN1/EN2 cannot shut down the VOUTLDO or VCCO, which are always active.

For the purpose of start-up power sequencing, the startup of the ADP1876 can be programmed by connecting an appropriate resistor divider from the master power supply to the EN1 or EN2 pin, as shown in Figure 27. For instance, if the desired start-up voltage from the master power supply is 10 V, R1 and R2 can be set to 156 kΩ and 10 kΩ, respectively.

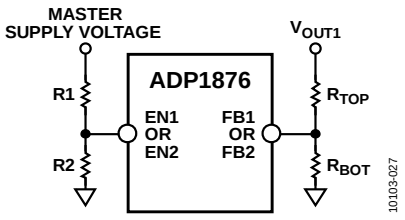


Figure 27. Optional Power-Up Sequencing Circuit

THERMAL OVERLOAD PROTECTION

The ADP1876 has an internal temperature sensor that senses the junction temperature of the chip. When the junction temperature of the ADP1876 reaches approximately 155°C, the ADP1876 enters thermal shutdown, where the converter, VCCO, and VOUTLDO are turned off and SSx discharges toward zero through an internal 1 kΩ resistor. When the junction temperature drops below 135°C, the ADP1876 resumes normal operation after the soft start sequence.

APPLICATIONS INFORMATION

INDEPENDENT LOW DROPOUT LINEAR REGULATOR

The input voltage range to VINLDO of the independent LDO regulator is 2.7 V to 5.5 V, and the output is fixed at 1.5 V with a 150 mA maximum load current. The internal short-circuit current limit is set to about 430 mA. Apply power to the VIN pin to keep the LDO operating within specification. The LDO is enabled when V_{INLDO} exceeds the input undervoltage lockout (UVLO) threshold. Safety features include short-circuit protection and thermal overload shutdown.

SETTING THE OUTPUT VOLTAGE OF THE CONTROLLER

The output voltage is set using a resistive voltage divider from the output to FBx. The voltage divider divides down the output voltage to the 0.6 V FBx regulation voltage to set the regulation output voltage. The output voltage can be set to as low as 0.6 V and as high as 90% of the power input voltage.

The maximum input bias current into FBx is 100 nA. For a 0.15% degradation in regulation voltage, and with 100 nA bias current, the low-side resistor, R_{BOT}, must be less than 9 kΩ, which results in 67 µA of divider current. For R_{BOT}, use a 1 kΩ to 20 kΩ resistor. A larger value resistor can be used but results in a reduction in output voltage accuracy due to the input bias current at the FBx pin, whereas lower values cause increased quiescent current consumption. Choose R_{TOP} to set the output voltage by using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right)$$

where:
R_{TOP} is the high-side voltage divider resistance.
R_{BOT} is the low-side voltage divider resistance.
V_{OUT} is the regulated output voltage.
V_{FB} is the feedback regulation threshold, 0.6 V.

The minimum output voltage is dependent on f_{SW} and minimum DHx on time. The maximum output voltage is dependent on f_{SW}, the minimum DHx off time, the IR drop across the high-side N-channel MOSFET, and the DCR of the inductor.

SOFT START

The soft start period is set by an external capacitor between SS1 or SS2 and AGND. The soft start function limits the input inrush current and prevents output overshoot.

When EN1/EN2 is enabled, a current source of 6.5 µA starts charging the capacitor, and the regulation voltage is reached when the voltage at SS1/SS2 reaches 0.6 V.

The soft start period is approximated by the following equation:

$$t_{SS} = \frac{0.6\text{ V}}{6.5\,\mu\text{A}} C_{SS}$$

The SSx pin reaches a final voltage of 3.2 V. If the output voltage is precharged prior to turn on, the ADP1876 prevents reverse inductor current, which discharges the output capacitor. When the voltage at SSx exceeds the regulation voltage (typically at 0.6 V), the reverse current is enabled to allow the output voltage regulation to be independent of load current.

When a controller is disabled, for instance, EN1/EN2 is pulled low or experiences an overcurrent limit condition, the soft start capacitor is discharged through an internal 1 kΩ pull-down resistor.

SETTING THE CURRENT LIMIT

The current-limit comparator measures the voltage across the low-side MOSFET to determine the load current.

The current limit is set by an external current-limit resistor, R_{ILIM}, between ILIMx and SWx. The current sense pin, ILIMx, sources nominally 50 µA to this external resistor. This creates an offset voltage of R_{ILIM} multiplied by 50 µA. When the drop across the low-side MOSFET R_{DSON} is equal to or greater than this offset voltage, the ADP1876 flags a current-limit event.

Because the ILIMx current and the MOSFET R_{DSON} vary over process and temperature, set the minimum current limit to ensure that the system can handle the maximum desired load current. To do this, use the peak current in the inductor, which is the desired output current-limit level, plus ½ of the ripple current, the maximum R_{DSON} of the MOSFET at its highest expected temperature, and the minimum ILIM current. Keep in mind that the temperature coefficient of the MOSFET R_{DSON} is typically 0.4%/°C.

$$R_{ILIM} = \frac{I_{LPK} \times R_{DSON\_MAX}}{40\,\mu\text{A}}$$

where:
I_{LPK} is the peak inductor current.

ACCURATE CURRENT-LIMIT SENSING

R_{DSON} of the MOSFET can vary by more than 50% over the temperature range. Accurate current-limit sensing is achieved by adding a current sense resistor from the source of the low-side MOSFET to PGNDx. Make sure that the power rating of the current sense resistor is adequate for the application. Apply the previous equation and calculate R_{ILIM} by replacing R_{DSON_MAX} with R_{SENSE}. See Figure 28 for the implementation of this accurate current-limit sensing scheme.

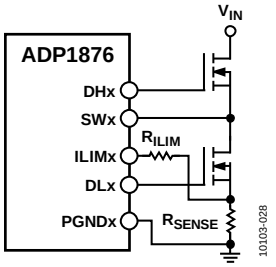


Figure 28. Accurate Current-Limit Sensing

SETTING THE SLOPE COMPENSATION

In a current mode control topology, slope compensation is needed to prevent subharmonic oscillations in the inductor current and to maintain a stable output. The external slope compensation is implemented by summing the amplified sense signal and a scaled voltage at the RAMPx pin. To implement the slope compensation, connect a resistor between RAMPx and the input voltage. The resistor, R_{RAMP}, is calculated by

$$R_{RAMP} = \frac{3.6 \times 10^{10} L}{A_{CS} \times R_{DSON\_MAX}}$$

where:
3.6×10^{10} is an internal parameter.
L is the inductance of the inductor.
R_{DSON_MAX} is the the low-side MOSFET maximum on resistance.
A_{CS} is the gain, either 3 V/V, 6 V/V, 12 V/V, or 24 V/V, of the current sense amplifier (see the Setting the Current Sense Gain section for more details).

Keep in mind that R_{DSON} is temperature dependent and can vary as much as 0.4%/°C. Choose R_{DSON} at the maximum operating temperature. The voltage at RAMPx is fixed at 0.2 V, and the current going into RAMPx should be between 6 µA and 200 µA. Ensure that the following condition is satisfied:

$$6\,\mu A \le \frac{V_{IN} - 0.2\,V}{R_{RAMP}} \le 200\,\mu A$$

For instance, with an input voltage of 12 V, R_{RAMP} should not exceed 1.9 MΩ. If the calculated R_{RAMP} produces less than 6 µA, select an R_{RAMP} value that produces between 6 µA and 20 µA. Figure 29 illustrates the connection of the slope compensation resistor, R_{RAMP}, and the current sense gain resistor, R_{CSG}.

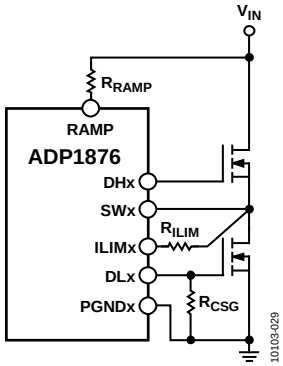


Figure 29. Slope Compensation and CS Gain Connection

SETTING THE CURRENT SENSE GAIN

The voltage drop across the external low-side MOSFET is sensed by a current sense amplifier by multiplying the peak inductor current and the R_{DSON} of the MOSFET. The result is amplified by a gain factor of either 3 V/V, 6 V/V, 12 V/V, or 24 V/V, which is programmable by an external resistor, R_{CSG}, connected to the DLx pin. This gain is sensed during power-up only and not during normal operation. The amplified voltage is summed with the slope compensation ramp voltage and fed into the PWM controller for a stable regulation voltage.

The voltage range of the internal node, V_{CS}, is between 0.4 V and 2.2 V. Select the current sense gain such that the internal minimum amplified voltage (V_{CSMIN}) is above 0.4 V and the maximum amplified voltage (V_{CSMAX}) is 2.1 V. Note that V_{CSMIN} or V_{CSMAX} is not the same as V_{COMP}, which has a range of 0.85 V to 2.3 V. Make sure that the maximum V_{COMP} ($V_{COMPMAX}$) does not exceed 2.2 V to account for temperature and device to device variations. The following are equations for V_{CSMIN}, V_{CSMAX}, and $V_{COMPMAX}$:

$$V_{CSMIN} = 0.75\,V - \frac{1}{2} I_{LPP} \times R_{DSON\_MIN} \times A_{CS}$$

$$V_{CSMAX} = 0.75\,V + (I_{LOADMAX} + \frac{1}{2} I_{LPP}) \times R_{DSON\_MAX} \times A_{CS}$$

$$V_{COMPMAX} = \frac{(V_{IN} - 0.2\,V) t_{ON}}{25\,pF \times R_{RAMP}} + V_{CSMAX}$$

where:
V_{CSMIN} is the minimum amplified voltage of the internal current sense amplifier at zero output current.
V_{CSMAX} is the maximum amplified voltage of the internal current sense amplifier at maximum output current.
R_{DSON_MIN} is the the low-side MOSFET minimum on resistance.
I_{LPP} is the peak-to-peak ripple current in the inductor.
$I_{LOADMAX}$ is the maximum output dc load current.
$V_{COMPMAX}$ is the maximum voltage at the COMP pin.
A_{CS} is the current sense gain of either 3 V/V, 6 V/V, 12 V/V, or 24 V/V set by the gain resistor between DLx and PGNDx.
25 pF is an internal parameter.
t_{ON} is on time for the high-side driver (DH).

INPUT CAPACITOR SELECTION

The input current to a buck converter is a pulse waveform. It is zero when the high-side switch is off and approximately equal to the load current when it is on. The input capacitor carries the input ripple current, allowing the input power source to supply only the direct current. The input capacitor needs a sufficient ripple current rating to handle the input ripple, as well as an equivalent series resistance (ESR) that is low enough to mitigate input voltage ripple. For the usual current ranges for these converters, it is good practice to use two parallel capacitors placed close to the drains of the high-side switch MOSFETs (one bulk capacitor of sufficiently high current rating and a 10 µF ceramic decoupling capacitor, typically).

Select an input bulk capacitor based on its ripple current rating. First, determine the duty cycle of the output.

$$D = \frac{V_{OUT}}{V_{IN}}$$

The input capacitor rms ripple current is given by

$$I_{RMS} = I_O \sqrt{D(1-D)}$$

where:
I_O is the output current.
D is the duty cycle.

The minimum input capacitance required for a particular load is

$$C_{IN,MIN} = \frac{I_O \times D(1-D)}{(V_{PP} - I_O \times D \times R_{ESR}) f_{SW}}$$

where:
V_{PP} is the desired input ripple voltage.
R_{ESR} is the equivalent series resistance of the capacitor.
If an MLCC capacitor is used, the ESR is near 0, then the equation is simplified to

$$C_{IN,MIN} = I_O \times \frac{D(1-D)}{V_{PP} \times f_{SW}}$$

The capacitance of MLCC is voltage dependent. The actual capacitance of the selected capacitor must be derated according to the manufacturer's specification. In addition, add more bulk capacitance, such as by using electrolytic or polymer capacitors, as necessary for large step load transients. Make sure the current ripple rating of the bulk capacitor exceeds the maximum input current ripple of a particular design.

INPUT FILTER

Normally a 0.1 µF (or greater value) bypass capacitor from the input pin (VIN) to AGND is sufficient for filtering any unwanted switching noise. However, depending on the printed circuit board (PCB) layout, some switching noise can enter the ADP1876 internal circuitry; therefore, it is recommended to have a low-pass filter at the VIN pin. Connecting a resistor, between 2 Ω and 5 Ω, in series with VIN and a 1 µF ceramic capacitor between VIN and AGND creates a low-pass filter that effectively filters out any unwanted glitches caused by the switching regulator. Note that the input current can be larger than 100 mA when driving large MOSFETs. A 100 mA current across a 5 Ω resistor creates a 0.5 V drop, which is the same voltage drop in VCCO. In this case, a lower resistor value is desirable.

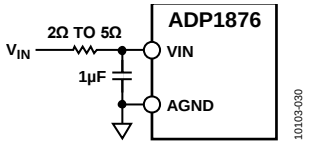


Figure 30. Input Filter Configuration

BOOST CAPACITOR SELECTION

To lower system component count and cost, the ADP1876 has an integrated rectifier (equivalent to the boost diode) between VCCO and BSTx. Choose a boost ceramic capacitor with a value between 0.1 µF and 0.22 µF; this capacitor provides the current for the high-side driver during switching.

INDUCTOR SELECTION

The output LC filter smoothes the switched voltage at SWx. For most applications, choose an inductor value such that the inductor ripple current is between 20% and 40% of the maximum dc output load current. Generally, a larger inductor current ripple generates more power loss in the inductor and larger voltage ripples at the output. Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design.

Choose the inductor value by using the following equation:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}}$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
ΔI_L is the inductor ripple current.

OUTPUT CAPACITOR SELECTION

Choose the output bulk capacitor to set the desired output voltage ripple. The impedance of the output capacitor at the switching frequency multiplied by the ripple current gives the output voltage ripple. The impedance comprises the capacitive impedance plus the nonideal parasitic characteristics, the equivalent series resistance (ESR), and the equivalent series inductance (ESL). The output voltage ripple can be approximated by

$$\Delta V_{OUT} \cong \Delta I_L \left(R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}} + 4 f_{SW} \times L_{ESL} \right)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
R_{ESR} is the equivalent series resistance of the output capacitor (or the parallel combination of ESR of all output capacitors).
L_{ESL} is the equivalent series inductance of the output capacitor (or the parallel combination of ESL of all capacitors).

Solving C_{OUT} in the previous equation yields

$$C_{OUT} \cong \frac{\Delta I_L}{8 f_{SW}} \times \frac{1}{\Delta V_{OUT} - \Delta I_L R_{ESR} - 4 \Delta I_L f_{SW} \times L_{ESL}}$$

Usually, the impedance is dominated by ESR, such as in electrolytic or polymer capacitors, at the switching frequency, as stated in the maximum ESR rating on the capacitor data sheet; therefore, output ripple reduces to

$$\Delta V_{OUT} \cong \Delta I_L \times R_{ESR}$$

Electrolytic capacitors also have significant ESL, on the order of 5 nH to 20 nH, depending on type, size, and geometry. PCB traces contribute some ESR and ESL, as well. However, using the maximum ESR rating from the capacitor data sheet often provides enough margin such that measuring the ESL is not usually required.

In the case of output capacitors where the impedance of the ESR and ESL are small at the switching frequency, for instance, where the output capacitor is a bank of parallel MLCC capacitors, the capacitive impedance dominates and the output capacitance equation reduces to

$$C_{OUT} \cong \frac{\Delta I_L}{8 \Delta V_{OUT} \times f_{SW}}$$

Ensure that the ripple current rating of the output capacitors is greater than the maximum inductor ripple current.

For example, during a load step transient on the output, when the load is suddenly increased, the output capacitor supplies the load until the control loop has a chance to ramp the inductor current. This initial output voltage deviation results in a voltage droop or undershoot. The output capacitance (assuming 0 Ω ESR) that is required to satisfy the voltage droop requirement can be approximated by

$$C_{OUT} \cong \frac{\Delta I_{STEP}}{\Delta V_{DROOP} \times f_{SW}}$$

where:
ΔI_{STEP} is the step load.
ΔV_{DROOP} is the voltage droop at the output.

When a load is suddenly removed from the output, the energy stored in the inductor rushes into the capacitor, causing the output to overshoot. The output capacitance required to satisfy the output overshoot requirement can be approximated by

$$C_{OUT} \cong \frac{\Delta I_{STEP}{}^2 L}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}{}^2}$$

where:
$\Delta V_{OVERSHOOT}$ is the overshoot voltage during the step load.

Select the largest output capacitance given by any of the previous three equations.

MOSFET SELECTION

The choice of MOSFET directly affects the dc-to-dc converter performance. A MOSFET with low on resistance reduces I^2R losses, and a low gate charge reduces transition losses. A MOSFET that has low thermal resistance ensures that the power dissipated in the MOSFET does not result in excessive MOSFET die temperature.

The high-side MOSFET carries the load current during on time and usually carries most of the transition losses of the converter. Typically, the lower the on resistance of the MOSFET, the higher the gate charge, and vice versa. Therefore, it is important to choose a high-side MOSFET that balances the two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C \cong (I_{LOAD})^2 \times R_{DSON} \left(\frac{V_{OUT}}{V_{IN}} \right)$$

where:
R_{DSON} is the MOSFET on resistance.

The gate charging loss is approximated by the equation

$$P_G \cong V_{PV} \times Q_G \times f_{SW}$$

where
V_{PV} is the gate driver supply voltage.
Q_G is the MOSFET total gate charge.

Note that the gate charging power loss is not dissipated in the MOSFET but rather in the ADP1876 internal drivers. This power loss must be considered when calculating the overall power efficiency.

The high-side MOSFET transition loss is approximated by the equation

$$P_T \cong \frac{V_{IN} \times I_{LOAD} \times (t_R + t_F) \times f_{SW}}{2}$$

where:
P_T is the high-side MOSFET switching loss power.
t_R is the rise time in charging the high-side MOSFET.
t_F is the fall time in discharging the high-side MOSFET.
t_R and t_F can be estimated by the following equations:

$$t_R \cong \frac{Q_{GSW}}{I_{DRIVER\_RISE}}$$

$$t_F \cong \frac{Q_{GSW}}{I_{DRIVER\_FALL}}$$

where:
Q_{GSW} is the gate charge of the MOSFET during switching and is given in the MOSFET data sheet.
I_{DRIVER_RISE} and I_{DRIVER_FALL} are the driver current output by the ADP1876 internal gate drivers.

If Q_{GSW} is not given in the data sheet, it can be approximated by

$$Q_{GSW} \cong Q_{GD} + \frac{Q_{GS}}{2}$$

where Q_{GD} and Q_{GS} are the gate-to-drain and gate-to-source charges given in the MOSFET data sheet.

I_{DRIVER_RISE} and I_{DRIVER_FALL} can be estimated by

$$I_{DRIVER\_RISE} \cong \frac{V_{DD} - V_{SP}}{R_{ON\_SOURCE} + R_{GATE}}$$

$$I_{DRIVER\_FALL} \cong \frac{V_{SP}}{R_{ON\_SINK} + R_{GATE}}$$

where:
V_{DD} is the input supply voltage to the driver and is between 2.75 V and 5 V, depending on the input voltage.
V_{SP} is the switching point where the MOSFET fully conducts; this voltage can be estimated by inspecting the gate charge graph given in the MOSFET data sheet.
R_{ON_SOURCE} is the on resistance of theADP1876 internal driver (listed in Table 1), when charging the MOSFET.
R_{ON_SINK} is the on resistance of the ADP1876 internal driver (listed in Table 1), when discharging the MOSFET.
R_{GATE} is the on gate resistance of MOSFET listed in the MOSFET data sheet. If an external gate resistor is added, add this external resistance to R_{GATE}.

The total power dissipation of the high-side MOSFET is the sum of conduction and transition losses:

$$P_{HS} \cong P_C + P_T$$

The synchronous rectifier, or low-side MOSFET, carries the inductor current when the high-side MOSFET is off. The low-side MOSFET transition loss is small and can be neglected in the calculation. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time. Therefore, to achieve high efficiency, it is critical to optimize the low-side MOSFET for low on resistance. In cases where the power loss exceeds the MOSFET rating or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET conduction power loss is

$$P_{CLS} \cong (I_{LOAD})^2 \times R_{DSON}\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

There is an additional power loss during the time known as dead time between the turn off of the high-side switch and the turn on of the low-side switch when the body diode of the low-side MOSFET conducts the output current.

The power loss in the body diode is given by

$$P_{BODYDIODE} = V_F \times t_D \times f_{SW} \times I_O$$

where:
V_F is the forward voltage drop of the body diode, typically 0.7 V.
t_D is the dead time in the ADP1876, typically 30 ns when driving some medium-size MOSFETs with input capacitance, C_{iss}, of approximately 3 nF. The dead time is not fixed. Its effective value varies with gate drive resistance and C_{iss} thereby increasing $P_{BODYDIODE}$ in high load current designs and low voltage designs. Therefore, the power loss in the low-side MOSFET becomes

$$P_{LS} = P_{CLS} + P_{BODYDIODE}$$

Note that MOSFET R_{DSON} increases as temperature increases with a typical temperature coefficient of 0.4%/°C. The MOSFET junction temperature rise over the ambient temperature is

$$T_J = T_A + \theta_{JA} \times P_D$$

where:
θ_{JA} is the thermal resistance of the MOSFET package.
T_A is the ambient temperature.
P_D is the total power dissipated in the MOSFET.

LOOP COMPENSATION

As with most current mode step-down controllers, a transconductance error amplifier is used to stabilize the external voltage loop. Compensating the ADP1876 is fairly easy; an RC compensator is needed between COMP and AGND. Figure 31 shows the configuration of the compensation components: R_{COMP}, C_{COMP}, and C_{C2}. Because C_{C2} is very small compared to C_{COMP}, to simplify calculation, C_{C2} is ignored for the stability compensation analysis.

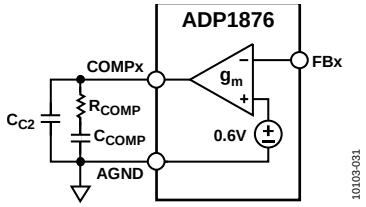


Figure 31. Compensation Components

The open-loop gain transfer function at angular frequency, s, is given by

$$H(s) = g_m \times G_{CS} \times \frac{V_{REF}}{V_{OUT}} \times Z_{COMP}(s) \times Z_{FILTER}(s) \quad (1)$$

where:
g_m is the transconductance of the error amplifer, 500 µS
G_{CS} is the tranconductance of the current sense amplifier.
Z_{COMP} is the impedance of the compensation network.
Z_{FILTER} is the impedance of the output filter.
V_{REF} = 0.6 V

G_{CS} with units of A/V is given by

$$G_{CS} = \frac{1}{A_{CS} \times R_{DSON\_MIN}} \quad (2)$$

where:
A_{CS} is the current sense gain of either 3 V/V, 6 V/V, 12 V/V, or 24 V/V set by the gain resistor between DLx and PGNDx.
R_{DSON_MIN} is the the low-side MOSFET minimum on resistance.

If a sense resistor, R_S, is added in series with the low-side FET, then G_{CS} becomes

$$G_{CS} = \frac{1}{A_{CS} \times (R_{DSON\_MIN} + R_S)}$$

Because the zero produced by the ESR of the output capacitor is not needed to stabilize the control loop, assuming ESR is small, the ESR is ignored for analysis. Then, Z_{FILTER} is given by

$$Z_{FILTER} = \frac{1}{sC_{OUT}} \quad (3)$$

Because C_{C2} is small relative to C_{COMP}, Z_{COMP} can be simplified to

$$Z_{COMP} = R_{COMP} + \frac{1}{sC_{COMP}} = \frac{1 + sR_{COMP} \times C_{COMP}}{sC_{COMP}} \quad (4)$$

At the crossover frequency, the open-loop transfer function is unity of 0 dB, H (f_{CROSS}) = 1. Combining Equation 1 and Equation 3, Z_{COMP} at the crossover frequency can be written as

$$Z_{COMP}(f_{CROSS}) = \left(\frac{2\pi \times f_{CROSS}}{g_m \times G_{CS}}\right)\left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (5)$$

The zero produced by R_{COMP} and C_{COMP} is

$$f_{ZERO} = \frac{1}{2\pi R_{COMP} \times C_{COMP}} \quad (6)$$

At the crossover frequency, Equation 4 can be shown as

$$Z_{COMP}(f_{CROSS}) = R_{COMP} \times \frac{\sqrt{f_{CROSS}^2 + f_{ZERO}2}}{f_{CROSS}} \quad (7)$$

Combining Equation 5 and Equation 7 and solving for R_{COMP} gives

$$R_{COMP} = \frac{f_{CROSS}}{f_{CROSS} + f_{ZERO}} \times \left(\frac{2\pi \times f_{CROSS}}{g_m \times G_{CS}}\right) \times \left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (8)$$

Choose the crossover and zero frequencies as follows:

$$f_{CROSS} = \frac{f_{SW}}{12} \quad (9)$$

$$f_{ZERO} = \frac{f_{CROSS}}{4} = \frac{f_{SW}}{48} \quad (10)$$

Substituting Equation 2, Equation 9, and Equation 10 into Equation 8 yields

$$R_{COMP} = 0.97 \times A_{CS} \times R_{DSON}\left(\frac{2\pi \times f_{CROSS}}{g_m}\right) \times \left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (11)$$

where:
g_m is the transconductance of the error amplifer, 500 µS.
A_{CS} is the current sense gain of 3 V/V, 6 V/V, 12 V/V, or 24 V/V.
R_{DSON} is the on resistance of the low-side MOSFET.
V_{REF} = 0.6 V.

And combining Equation 6 and Equation 10 yields

$$C_{COMP} = \frac{2}{\pi R_{COMP} \times f_{CROSS}} \quad (12)$$

Note that the previous simplified compensation equations for R_{COMP} and C_{COMP} yield reasonable results in f_{CROSS} and phase margin assuming that the compensation ramp current is ideal. Varying the ramp current, or deviating the ramp current from ideal, can affect f_{CROSS} and phase margin.

Lastly, set C_{C2} to

$$\frac{1}{20} \times C_{COMP} \le C_{C2} \le \frac{1}{10} \times C_{COMP} \quad (13)$$

SWITCHING NOISE AND OVERSHOOT REDUCTION

In any high speed step-down regulator, high frequency noise (generally in the range of 50 MHz to 100 MHz) and voltage overshoot are always present at the gate, the switch node (SW), and the drains of the external MOSFETs. The high frequency noise and overshoot are caused by the parasitic capacitance, C_{GD}, of the external MOSFET as well as the parasitic inductance of the gate trace and the packages of the MOSFETs. When the high current is switched, electromagnetic interference (EMI) is generated, which can affect the operation of the surrounding circuits. To reduce voltage ringing and noise, it is recommended to add an RC snubber between SWx and PGNDx for high current applications, as illustrated in Figure 32.

In most applications, R_{SNUB} is typically 2 Ω to 4 Ω, and C_{SNUB} is typically 1.2 nF to 3 nF.

R_{SNUB} can be estimated by

$$R_{SNUB} \cong 2\sqrt{\frac{L_{MOSFET}}{C_{OSS}}}$$

And C_{SNUB} can be estimated by

$$C_{SNUB} \cong C_{OSS}$$

where:
L_{MOSFET} is the total parasitic inductance of the high-side and low-side MOSFETs, typically 3 nH, and is package dependent.
C_{OSS} is the total output capacitance of the high-side and low-side MOSFETs given in the MOSFET data sheet.

The size of the RC snubber components need to be chosen correctly to handle the power dissipation. The power dissipated in R_{SNUB} is

$$R_{SNUB} = V_{IN}^2 \times C_{SNUB} \times f_{SW}$$

In most applications, a component size 0805 for R_{SNUB} is sufficient. However, the use of an RC snubber reduces the overall efficiency, generally by an amount in the range of 0.1% to 0.5%. The RC snubber does not reduce the voltage overshoot.

A resistor, shown as R_{RISE} in Figure 32 at the BST1 pin, helps to reduce overshoot and is generally between 2 Ω and 4 Ω. Adding a resistor in series, typically between 2 Ω and 4 Ω, with the gate driver also helps to reduce overshoot. If a gate resistor is added, R_{RISE} is not needed.

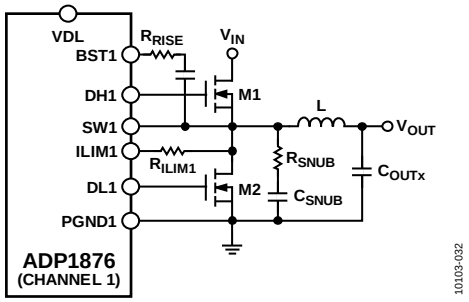
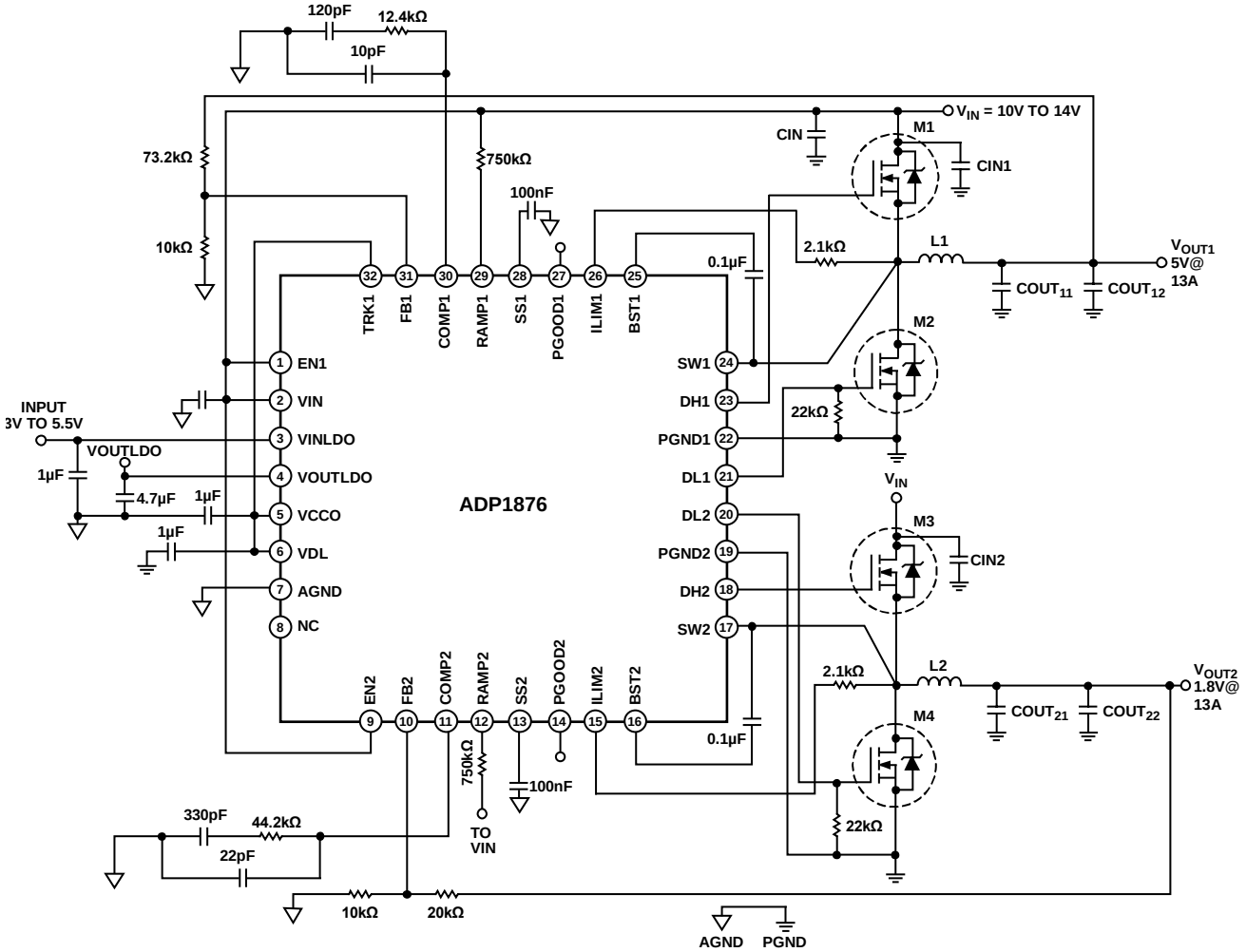


Figure 32. Application Circuit with a Snubber

PCB LAYOUT GUIDELINE

For additional information about PCB layout, see the AN-1119 Application Note, *Printed Circuit Board Layout Guidelines for Step-Down Regulators, Optimizing for Low Noise Design with Dual Channel Switching Controllers*.

TYPICAL APPLICATIONS CIRCUIT



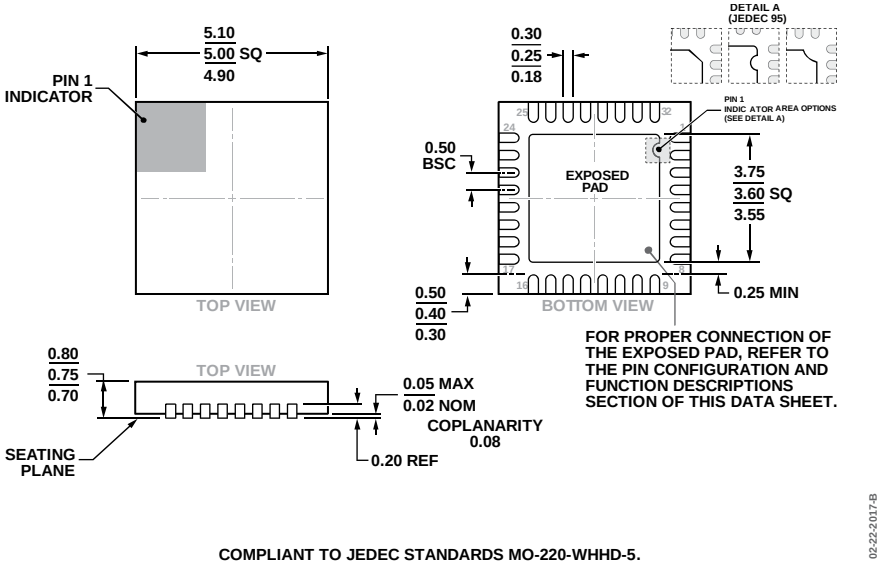
CIN = 150µF/20V, OS-CON, 20SEP150M, SANYO
L1, L2: 1.2µH, WURTH ELEKTRONIK, 744325120
M1, M3: BSC080N03LS
M2, M4: BSC030N03LS

CIN1, CIN2: 10µF/X7R/25V/1210 × 2, GRM32DR71E106KA12, MUR ATA
$COUT_{11}$, $COUT_{21}$: 330µF/6.3V/POSCAP × 2, 6TPF330M9L, SANYO
$COUT_{12}$, $COUT_{22}$: 22µF/X5R/0805/6.3V × 3, GRM21BR60J226ME39, MUR ATA

Figure 33. Typical Applications Circuit

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5.

Figure 34. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body, and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1876ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADP1876-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D10103-0-3/17(B)

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