



**THE DATASHEET OF
NTLTS3107PR2G**



NTLTS3107P

Power MOSFET

-20 V, -8.3 A, Single P-Channel, Micro8 Leadless Package

Features

- Low $R_{DS(on)}$ for Extended Battery Life
- Surface Mount Micro8 Leadless for Improved Thermal Performance
- Low Profile (<1.0 mm) Optimal for Portable Designs
- Low Turn-On Voltage
- This is a Pb-Free Device

Applications

- Optimized for Load Management Applications
- Charge Control in Battery Powered Systems
- Cell Phones, DSC, Notebooks, Portable Games, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	-20	V	
Gate-to-Source Voltage		V_{GS}	± 8.0	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-8.3	A
			$T_A = 85^\circ\text{C}$	-6.0	
	$t \leq 10\text{ s}$	$T_A = 25^\circ\text{C}$		-12	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.6	W
			$t \leq 10\text{ s}$	3.3	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-5.9	A
		$T_A = 85^\circ\text{C}$		-3.7	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	P_D	0.8	W
Pulsed Drain Current (Note 1)	$t_p = 10\ \mu\text{s}$	I_{DM}	-25	A	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	-1.6	A	
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)		T_L	260	$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	38	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	160	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 sq. in. pad size (Cu. area = 1.127 sq. in. [1 oz] including traces).
2. Surface-mounted on FR4 board using minimum recommended pad size (Cu. area = TBD sq. in.).

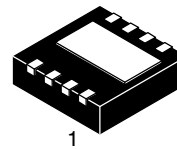
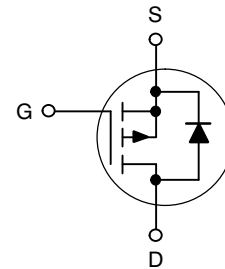


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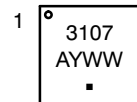
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-20 V	12.2 m Ω @ -4.5 V	-8.3 A
	15.6 m Ω @ -2.5 V	
	26.2 m Ω @ -1.8 V	

P-Channel MOSFET



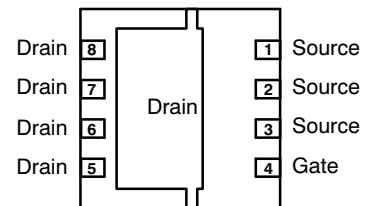
Micro8 Leadless
CASE 846C

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

PIN ASSIGNMENT



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLTS3107PR2G	Micro8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTLTS3107P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			11		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -16 V			-10	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8.0 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-0.45		-1.2	V	
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			3.4		mV/°C	
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -8.0 A		12.2	16	mΩ	
			V _{GS} = -2.5 V, I _D = -7.0 A		15.6		21
			V _{GS} = -1.8 V, I _D = -5.8 A		26.2		
Forward Transconductance	g _{FS}	V _{DS} = -5 V, I _D = -8.0 A		25		S	

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = -16 V		5900	6500	pF
Output Capacitance	C _{OSS}			625	675	
Reverse Transfer Capacitance	C _{RSS}			425	525	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -16 V, I _D = -8.0 A		55	70	nC
Threshold Gate Charge	Q _{G(TH)}			3.0		
Gate-to-Source Gate Charge	Q _{GS}			7.0		
Gate-to-Drain "Miller" Charge	Q _{GD}			11		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -8.0 A, R _G = 3.0 Ω		30		ns
Rise Time	t _r			20		
Turn-Off Delay Time	t _{d(off)}			250		
Fall Time	t _f			80		

DRAIN-SOURCE DIODE CHARACTERISTICS (Note 3)

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1.6 A	T _J = 25°C		-0.7	-1.2	V
			T _J = 125°C		0.5		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -1.6 A		75	100	ns	
Charge Time	t _a			28			
Discharge Time	t _b			47			
Reverse Recovery Charge	Q _{RR}			81.5		nC	

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

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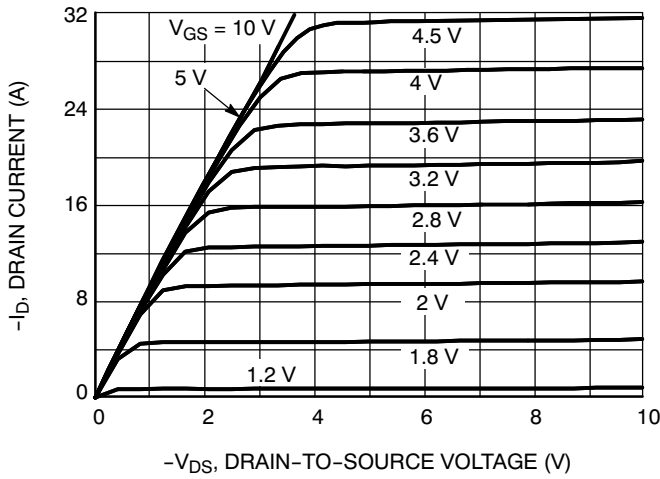


Figure 1. On-Region Characteristics

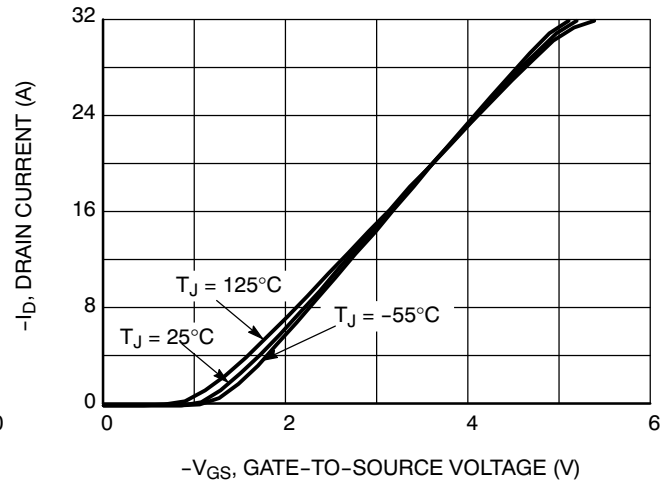


Figure 2. Transfer Characteristics

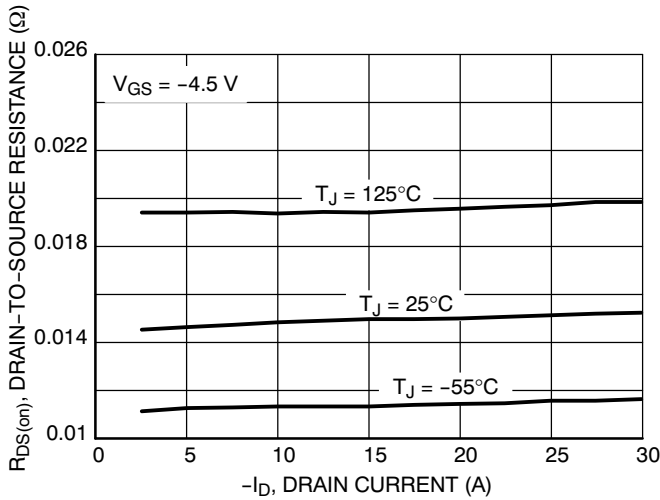


Figure 3. On-Resistance versus Drain Current and Temperature

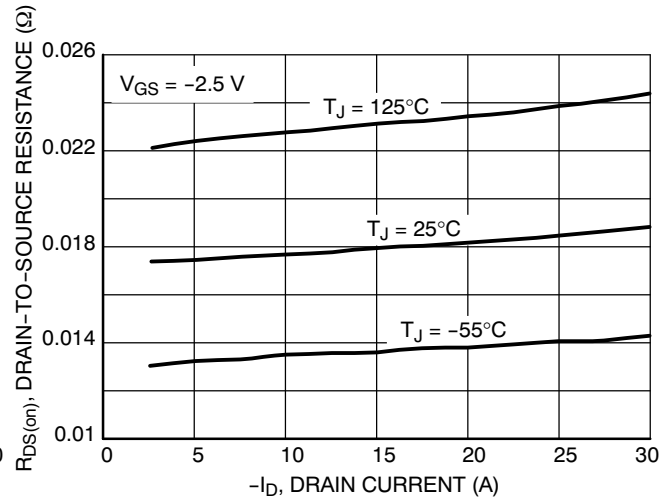


Figure 4. On-Resistance versus Drain Current and Temperature

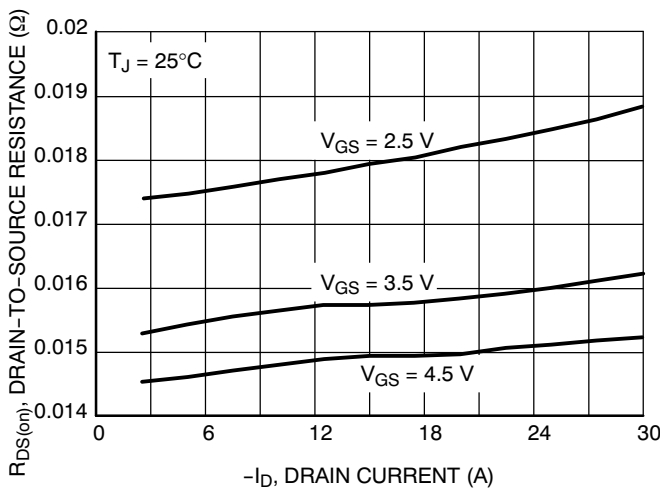


Figure 5. On-Resistance versus Drain Current and Gate Voltage

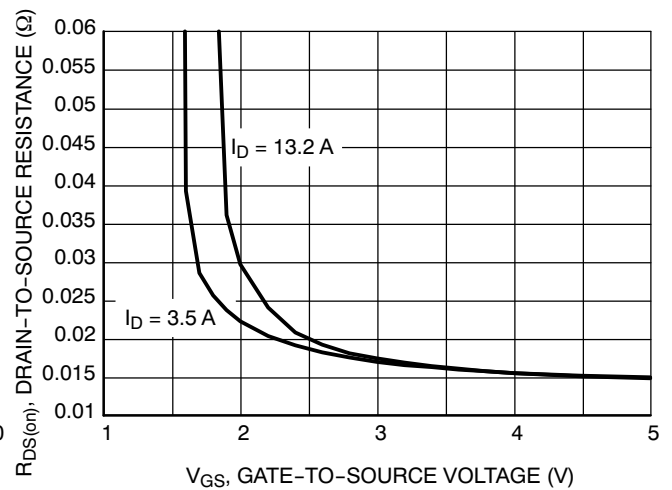


Figure 6. On-Resistance versus Gate Voltage

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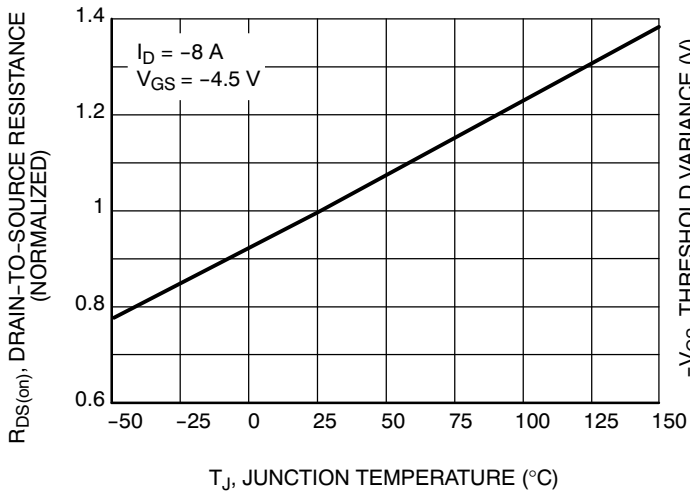


Figure 7. On-Resistance Variation with Temperature

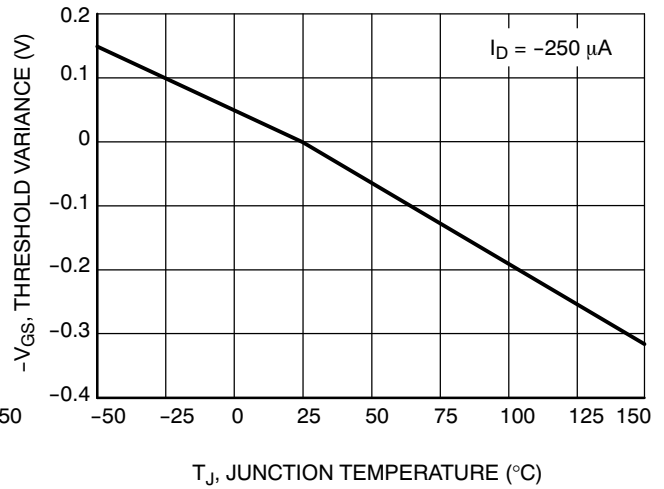


Figure 8. Threshold Voltage

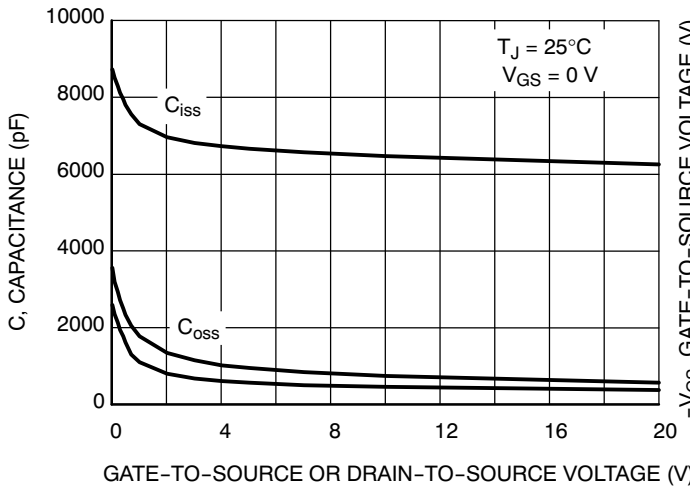


Figure 9. Capacitance Variation

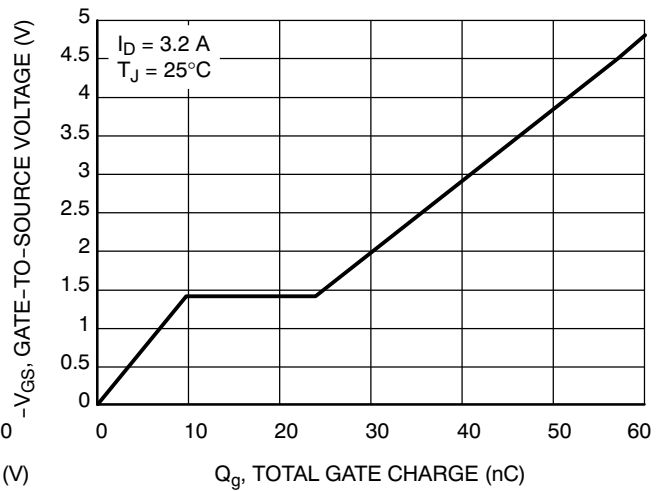


Figure 10. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

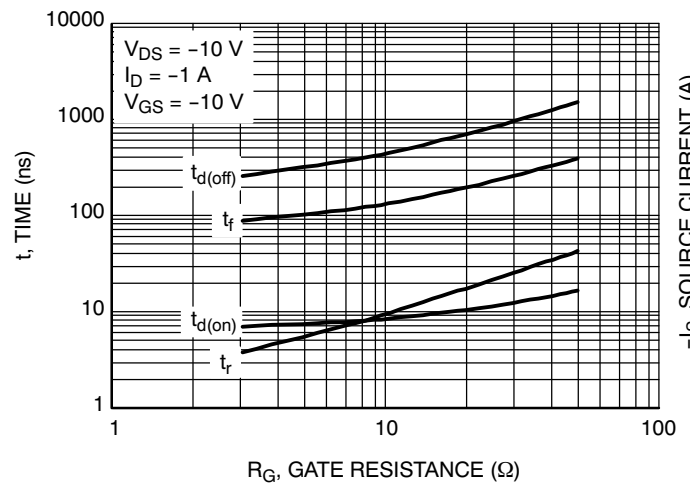


Figure 11. Resistive Switching Time Variation versus Gate Resistance

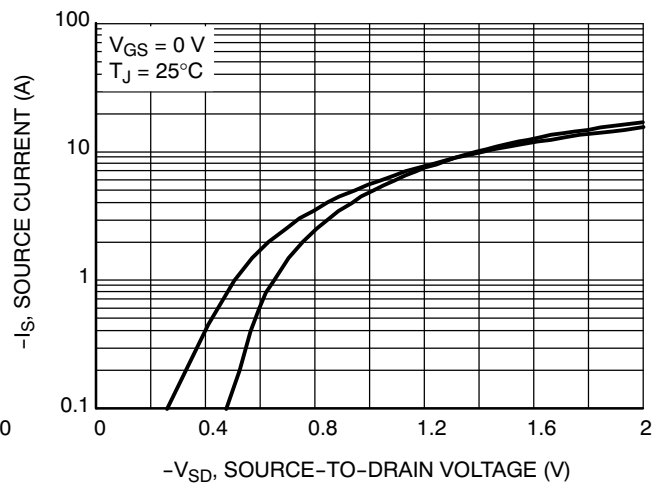
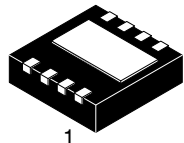


Figure 12. Diode Forward Voltage versus Current

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

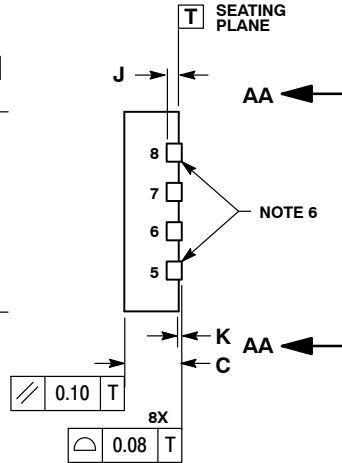
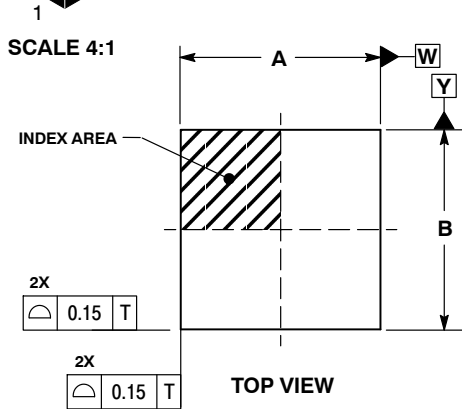
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DFN8 3x3, (MICRO8 LEADLESS)

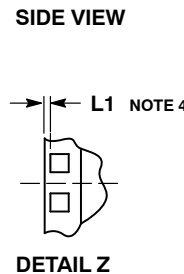
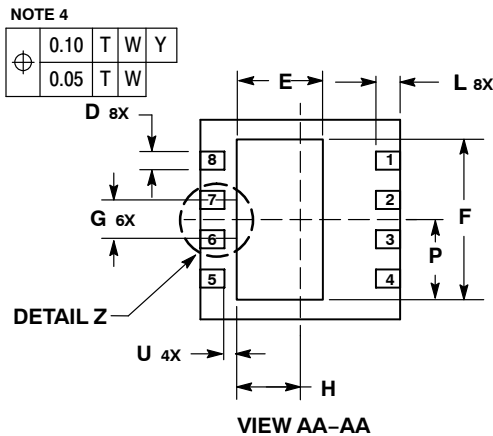
CASE 846C-01
ISSUE D

DATE 28 JUN 2010



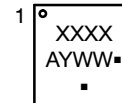
NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
4. DIMENSION D APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 MM AND 0.30 MM FROM TERMINAL TIP. DIMENSION L1 IS THE TERMINAL PULL BACK FROM PACKAGE EDGE, UP TO 0.1 MM IS ACCEPTABLE. L1 IS OPTIONAL.
5. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
6. OPTIONAL SIDE VIEW CAN SHOW LEADS 5 AND 8 REMOVED.



DIM	MILLIMETERS	
	MIN	MAX
A	3.30	BSC
B	3.30	BSC
C	0.85	0.95
D	0.25	0.35
E	1.30	1.50
F	2.55	2.75
G	0.65	BSC
H	0.95	1.15
J	0.25	BSC
K	0.00	0.05
L	0.35	0.45
L1	0.00	0.10
P	1.28	1.38
U	0.17	TYP

GENERIC MARKING DIAGRAM*

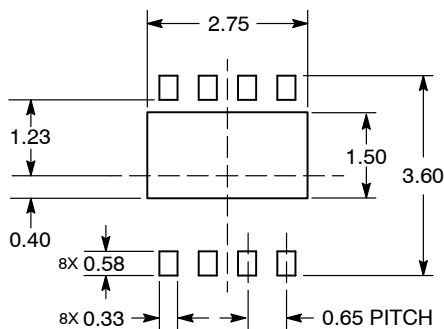


- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8 3X3, (MICRO8 LEADLESS)	PAGE 1 OF 1

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