THE DATASHEET OF

AFE4490RHAR

AFE4490 Integrated Analog Front-End for Pulse Oximeters

1 Features

- Fully-Integrated Analog Front-End for Pulse Oximeter Applications:
  - Flexible Pulse Sequencing and Timing Control
- Transmit:
  - Integrated LED Driver (H-Bridge, Push, or Pull)
  - 110-dB Dynamic Range Across Full Range (Enables Low Noise at Low LED Current)
  - LED Current:
    - Programmable Ranges of 50 mA, 75 mA, 100 mA, 150 mA, and 200 mA, Each with 8-Bit Current Resolution
  - Low Power:
    - 100 µA + Average LED Current
  - LED On-Time Programmability from (50 µs + Settle Time) to 4 ms
  - Independent LED2, LED1 Current Reference
- Receive Channel with High Dynamic Range:
  - Input-Referred Noise: 50 pA_{RMS} (at 5-µA PD Current)
  - 13.5 Noise-Free Bits (at 5-µA PD Current)
  - Analog Ambient Cancellation Scheme with Selectable 1-µA to 10-µA Ambient Current
  - Low Power: < 2.3 mW at 3.0-V Supply
  - Rx Sample Time: 50 µs to 4 ms
  - I-V Amplifier with Seven Separate LED2 and LED1 Programmable Feedback R and C Settings
  - Integrated Digital Ambient Estimation and Subtraction
- Integrated Fault Diagnostics:
  - Photodiode and LED Open and Short Detection
  - Cable On or Off Detection
- Supplies:
  - Rx = 2.0 V to 3.6 V
  - Tx = 3.0 V or 5.25 V
- Package: Compact VQFN-40 (6 mm × 6 mm)
- Specified Temperature Range: –40°C to 85°C

2 Applications

- Medical Pulse Oximeter Applications
- Industrial Photometry Applications

3 Description

The AFE4490 is a fully-integrated analog front-end (AFE) that is ideally suited for pulse-oximeter applications. The device consists of a low-noise receiver channel with a 22-bit analog-to-digital converter (ADC), an LED transmit section, and diagnostics for sensor and LED fault detection. The device is a very configurable timing controller. This flexibility enables the user to have complete control of the device timing characteristics. To ease clocking requirements and provide a low-jitter clock to the device, an oscillator is also integrated that functions from an external crystal. The device communicates to an external microcontroller or host processor using an SPI™ interface.

The device is a complete AFE solution packaged in a single, compact VQFN-40 package (6 mm × 6 mm) and is specified over the operating temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE4490	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

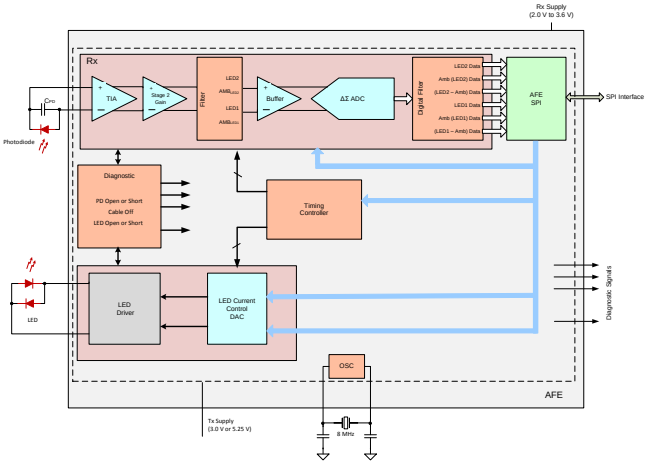


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (June 2014) to Revision H — **Page**

- Changed $V_{(ESD)}$ parameter specification values in Absolute Maximum Ratings table ... 8
- Updated *AFE Register Description* section to current standards: added legend and bit settings to each bit register ... 59

Changes from Revision F (October 2013) to Revision G — **Page**

- Added *Applications and Implementation*, *Power Supply Recommendations*, and *Layout* sections ... 1
- Changed sub-bullet of *Transmit* Features bullet ... 1
- Changed second sub-bullet of *Integrated Fault Diagnostics* Features bullet ... 1
- Changed VCM row in Pin Functions table: changed INM to INN in VCM description ... 7
- Changed Absolute Maximum Ratings table: changed first five rows and added TXP, TXN pins row ... 8
- Added Handling Ratings table ... 8
- Changed I-V Transimpedance Amplifier, $V_{O(shield)}$ parameter: changed test conditions and added minimum and maximum specifications ... 11
- Changed Example value for rows t, t_2, t_4, t_5, t_7, t_{11}, t_{13}, t_{15}, t_{17}, t_{19}, t_{22}, t_{24}, t_{26}, and t_{28} in Table 2 ... 36
- Added footnote 2 to Table 2 ... 36
- Added footnote 2 to Figure 63 ... 37
- Added footnote 2 to Figure 64 ... 38
- Changed INN pin name in Figure 76 ... 49
- Changed INM to INN throughout Table 3 ... 51
- Added STAGE2EN1 and STG2GAIN1[2:0] in TIAGAIN register ... 57
- Changed STAGE2EN to STAGE2EN2 and STG2GAIN[2:0] to STG2GAIN2[2:0] in TIA_AMB_GAIN register ... 57
- Added last two sentences to NUMAV[7:0] description in CONTROL1: Control Register 1 ... 72

Changes from Revision E (October 2013) to Revision F **Page**

- Changed LED_DRV_SUP parameter in Recommended Operating Conditions table ... 9
- Changed *TXM* to *TXN* in V_{LED} footnote of Recommended Operating Conditions table ... 9
- Changed V_{LED} footnote and added V_{HR} footnote to Recommended Operating Conditions table ... 9
- Changed Figure 77 (changed TXP and TXN pin names, deleted LED 1 and LED 2 pin names) ... 50
- Changed Table 6 (added V_{HR} columns to table) ... 76

Changes from Revision D (May 2013) to Revision E **Page**

- Changed 2.3 mA to 2.3 mW in 4th sub-bullet and changed 250 µs to 4 ms in 5th sub-bullet of *Receive Channel with High Dynamic Range* Features bullet ... 1
- Changed Rx, Tx supplies and deleted 5-V supply from front-page graphic ... 1
- Changed Tx Power Supply column in Family and Ordering Information table ... 6
- Changed *TX_REF* description in Pin Descriptions table ... 7
- Changed conditions of Electrical Characteristics table ... 10
- Changed Performance, *PRF* parameter minimum specification in Electrical Characteristics table ... 10
- Changed PRF = 1300 Hz to PRF = 1200 Hz in test conditions for the Performance, *Total integrated noise current* and N_{FB} parameters in Electrical Characteristics table ... 10
- Changed Ambient Cancellation Stage, *Gain* parameter in Electrical Characteristics table ... 11
- Added last two Low-Pass Filter parameters to Electrical Characteristics table ... 11
- Added Diagnostics, *Diagnostics current* parameter to Electrical Characteristics table ... 12
- Changed C_F to C and added TX_REF capacitor to Functional Block Diagram graphic ... 27
- Updated Figure 55 ... 28
- Changed second sentence in second paragraph of *Receiver Front-End* section ... 28
- Changed third paragraph of *Receiver Front-End* section ... 28
- Changed second paragraph of *Ambient Cancellation Scheme* section ... 30
- Added last paragraph and Table 1 to *Ambient Cancellation Scheme* section ... 31
- Updated Figure 58 ... 32
- Updated Figure 60 ... 34
- Added footnote 1 to Table 2 and changed Example column in Table 2 ... 36
- Changed corresponding register column description in rows t_{13}, t_{15}, t_{17}, and t_{19} and example column values for rows t_{22}, t_{24}, t_{26}, and t_{28} in Table 2 ... 36
- Updated Figure 63 ... 37
- Updated Figure 64 ... 38
- Deleted supply voltage range from RX_ANA_SUP and RX_DIG_SUP in Figure 65 ... 39
- Changed entire *Transmit Section* ... 39
- Deleted *_5V* from TX_CTRL_SUP and LED_DRV_SUP in Figure 68 ... 42
- Changed second paragraph of *ADC Operation and Averaging Module* section ... 43
- Updated Equation 5 and Figure 71 ... 44
- Updated Figure 72 ... 46
- Added first paragraph of *AFE Output Mode (ADC Bypass Mode)* section ... 47
- Updated Figure 75 ... 48
- Added last paragraph to the *Diagnostics Module* section ... 52
- Added first and last sentence to *Writing Data* section ... 52
- Changed second to last sentence in *Writing Data* section ... 52
- Added first and last sentence to *Reading Data* section ... 53
- Changed second to last sentence in *Reading Data* section ... 53

- Added *Multiple Data Reads and Writes* section 54
- Added last sentence to the *AFE SPI Interface Design Considerations* section 55
- Added Register Control column to Table 4 56
- Changed bits D16 and D10 in CONTROL2 row of Table 4 57
- Changed CONTROL0 paragraph description 59
- Added note to bit D2 description of CONTROL0 register 59
- Changed PRPCOUNT[15:0] (bits D[15:0]) description in PRPCOUNT register 72
- Changed note within CLKALMPIN[2:0] (bits D[11:9]) description of CONTROL1 register 72
- Changed second and third columns of Table 5 73
- Changed *001* and *011* bit settings for the STG2GAIN[2:0] bits (bits D[10:8]) in the TIA_AMB_GAIN register 75
- Changed description and name of bits D16 and D10 in CONTROL2 register 77

Changes from Revision C (April 2013) to Revision D **Page**

- Changed descriptions of RX_ANA_SUP, RX_DIG_SUP, and TX_CTRL_SUP pins in Pin Descriptions table 7
- Added *CMRR* parameter to Electrical Characteristics table 10
- Added External Clock, *External clock input voltage* and *External clock input current* parameters to Electrical Characteristics table 12
- Changed TIMING, $t_{\overline{RESET}}$ parameter unit in Electrical Characteristics table 12
- Added *Pin Leakage Current* section to Electrical Characteristics table 12
- Added Supply Current, *ADC bypass mode* parameter to Electrical Characteristics table 13
- Changed *Serial Interface Timing* section 15
- Added Figure 14 18
- Added Figure 20 19
- Added Figure 26 20
- Added Figure 32 21
- Added Figure 54 25
- Updated Functional Block Diagram graphic 27
- Changed name of register 15h 56
- Added note to descriptions of LED2-ALED2VAL and LED1-ALED1VAL registers 82

Changes from Revision B (February 2013) to Revision C **Page**

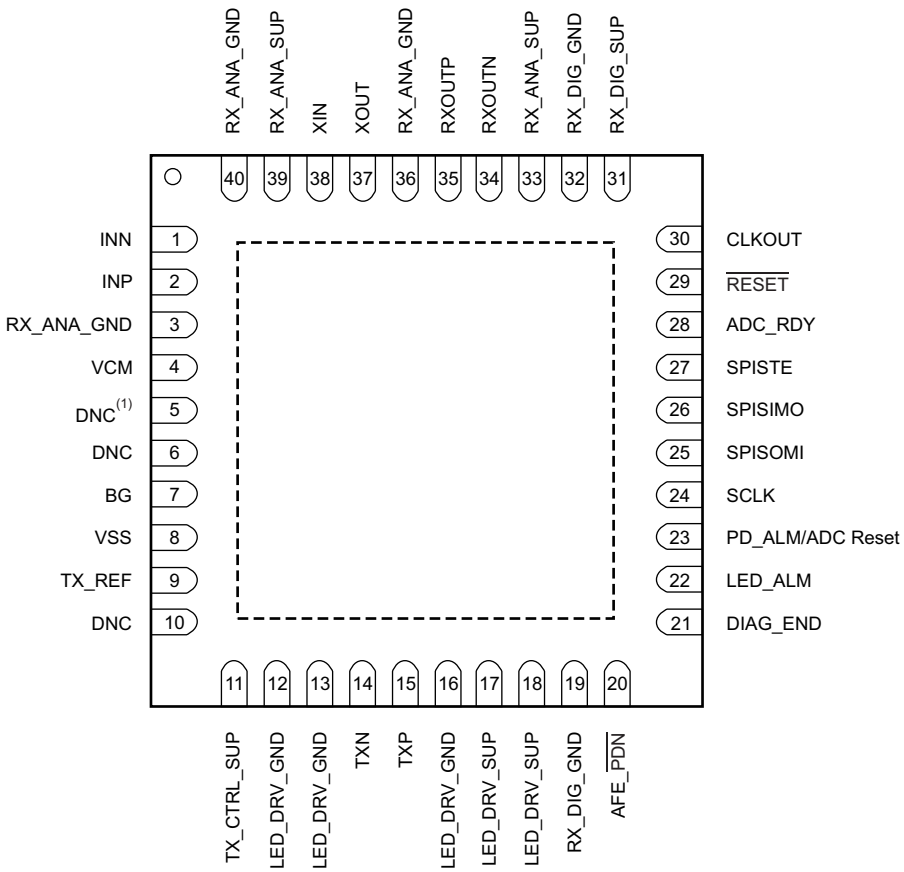
- Changed first two sub-bullets of *Receive Channel with High Dynamic Range* Features bullet 1
- Changed pin out figure 6
- Changed ESD ratings specification values in Absolute Maximum Ratings table 8
- Added Performance, *PSRR* parameter to Electrical Characteristics table 10
- Changed Performance, *Total integrated noise current* and N_{FB} parameters in Electrical Characteristics table 10
- Changed first row of Receiver Functional Block Level Specification, *Total integrated noise current* parameter in Electrical Characteristics table 10
- Changed Ambient Cancellation Stage, *Gain* parameter specifications in Electrical Characteristics table 11
- Changed Transmitter, *Transmitter noise dynamic range* parameter in Electrical Characteristics table 11
- Added External Clock, *External clock input frequency* parameter to Electrical Characteristics table 12
- Added Timing, *Wake-up time from Rx power-down* and *Wake-up time from Tx power-down* parameters to Electrical Characteristics table 12
- Changed Supply Current section of Electrical Characteristics table 13
- Changed typical specification in first row and unit in second row of Power Dissipation, $P_{D(q)}$ parameter in Electrical Characteristics table 14

5 Device Comparison Table

PRODUCT	PACKAGE-LEAD	LED DRIVE CONFIGURATION	LED DRIVE CURRENT (mA, max)	Tx POWER SUPPLY (V)	OPERATING TEMPERATURE RANGE
AFE4490	VQFN-40	Bridge, push-pull	50, 75, 100, 150, and 200	3 to 5.25	–40°C to 85°C
AFE4400	VQFN-40	Bridge, push-pull	50	3 to 5.25	0°C to 70°C
AFE4403	WCSP-36	Bridge, push-pull	100	3 to 5.25	–20°C to 70°C

6 Pin Configuration and Functions

RHA Package
VQFN-40
(Top View)



(1) DNC = Do not connect.

Pin Functions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
ADC_RDY	28	Digital	Output signal that indicates ADC conversion completion. Can be connected to the interrupt input pin of an external microcontroller.
AFE_$\overline{\text{PDN}}$	20	Digital	AFE-only power-down input; active low. Can be connected to the port pin of an external microcontroller.
BG	7	Reference	Decoupling capacitor for internal band-gap voltage to ground (2.2-µF decoupling capacitor to ground, expected voltage = 1.0 V).
CLKOUT	30	Digital	Buffered 4-MHz output clock output. Can be connected to the clock input pin of an external microcontroller.
DIAG_END	21	Digital	Output signal that indicates completion of diagnostics. Can be connected to the port pin of an external microcontroller.
DNC(1)	5, 6, 10	—	Do not connect these pins. Leave as open-circuit.
INN	1	Analog	Receiver input pin. Connect to photodiode anode.
INP	2	Analog	Receiver input pin. Connect to photodiode cathode.
LED_DRV_GND	12, 13, 16	Supply	LED driver ground pin, H-bridge. Connect to common board ground.
LED_DRV_SUP	17, 18	Supply	LED driver supply pin, H-bridge. Connect to an external power supply capable of supplying the large LED current, which is drawn by this supply pin.
LED_ALM	22	Digital	Output signal that indicates an LED cable fault. Can be connected to the port pin of an external microcontroller.
PD_ALM/ADC Reset	23	Digital	Output signal that indicates a PD sensor or cable fault. Can be connected to the port pin of an external microcontroller. In ADC bypass mode, the PD_ALM pin can be used to bring out the ADC reset signal.
$\overline{\text{RESET}}$	29	Digital	AFE-only reset input, active low. Can be connected to the port pin of an external microcontroller.
RX_ANA_GND	3, 36, 40	Supply	Rx analog ground pin. Connect to common board ground.
RX_ANA_SUP	33, 39	Supply	Rx analog supply pin; 0.1-µF decoupling capacitor to ground
RX_DIG_GND	19, 32	Supply	Rx digital ground pin. Connect to common board ground.
RX_DIG_SUP	31	Supply	Rx digital supply pin; 0.1-µF decoupling capacitor to ground
RXOUTN	34	Analog	External ADC negative input when in ADC bypass mode
RXOUTP	35	Analog	External ADC positive input when in ADC bypass mode
SCLK	24	SPI	SPI clock pin
SPISIMO	26	SPI	SPI serial in master out
SPISOMI	25	SPI	SPI serial out master in
SPISTE	27	SPI	SPI serial interface enable
TX_CTRL_SUP	11	Supply	Transmit control supply pin (0.1-µF decoupling capacitor to ground)
TX_REF	9	Reference	Transmitter reference voltage, 0.75 V default after reset. Connect a 2.2-µF decoupling capacitor to ground.
TXN	14	Analog	LED driver out B, H-bridge output. Connect to LED.
TXP	15	Analog	LED driver out B, H-bridge output. Connect to LED.
VCM	4	Reference	Input common-mode voltage output. Connect a series resistor (1 kΩ) and a decoupling capacitor (10 nF) to ground. The voltage across the capacitor can be used to shield (guard) the INP, INN traces. Expected voltage = 0.9 V.
VSS	8	Supply	Substrate ground. Connect to common board ground.
XOUT	37	Digital	Crystal oscillator pins. Connect an external 8-MHz crystal between these pins with the correct load capacitor (as specified by vendor) to ground.
XIN	38	Digital	Crystal oscillator pins. Connect an external 8-MHz crystal between these pins with the correct load capacitor (as specified by vendor) to ground.

(1) Leave pins as open circuit. Do not connect.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
RX_ANA_SUP, RX_DIG_SUP to RX_ANA_GND, RX_DIG_GND		–0.3	4	V
TX_CTRL_SUP, LED_DRV_SUP to LED_DRV_GND		–0.3	6	V
RX_ANA_GND, RX_DIG_GND to LED_DRV_GND		–0.3	0.3	V
Analog inputs		RX_ANA_GND – 0.3	RX_ANA_SUP + 0.3	V
Digital inputs		RX_DIG_GND – 0.3	RX_DIG_SUP + 0.3	V
TXP, TXN pins		–0.3	Minimum [6, (LED_DRV_SUP + 0.3)]	V
Input current to any pin except supply pins(2)			±7	mA
Input current	Momentary		±50	mA
	Continuous		±7	mA
Operating temperature range		–40	85	°C
Maximum junction temperature, T_J			125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing beyond the supply rails must be current-limited to 10 mA or less.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–60	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–1000	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–250	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
SUPPLIES				
RX_ANA_SUP	AFE analog supply	2.0	3.6	V
RX_DIG_SUP	AFE digital supply	2.0	3.6	V
TX_CTRL_SUP	Transmit controller supply	3.0	5.25	V
LED_DRV_SUP	Transmit LED driver supply, H-bridge or common anode configuration	[3.0 or (V_{HR} + V_{LED} + V_{CABLE})(1)(2)(3), whichever is greater]	5.25	V
	Difference between LED_DRV_SUP and TX_CTRL_SUP	–0.3	0.3	V
TEMPERATURE				
	Specified temperature range	–40	85	°C

(1) V_{HR} refers to the required voltage headroom necessary to drive the LEDs. See Table 6 for the appropriate V_{HR} value.
(2) V_{LED} refers to the maximum voltage drop across the external LED (at maximum LED current) connected between the TXP and TXN pins (in H-bridge mode) and from the TXP and TXN pins to LED_DRV_SUP (in the common anode configuration).
(3) V_{CABLE} refers to voltage drop across any cable, connector, or any other component in series with the LED.

7.4 Thermal Information

THERMAL METRIC(1)		AFE4490 RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31	
$R_{\theta JB}$	Junction-to-board thermal resistance	26	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	N/A	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Minimum and maximum specifications are at T_A = –40°C to 85°C. Typical specifications are at 25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PERFORMANCE (Full-Signal Chain)						
I_{IN_FS}	Full-scale input current	R_F = 10 kΩ		50		µA
		R_F = 25 kΩ		20		µA
		R_F = 50 kΩ		10		µA
		R_F = 100 kΩ		5		µA
		R_F = 250 kΩ		2		µA
		R_F = 500 kΩ		1		µA
		R_F = 1 MΩ		0.5		µA
PRF	Pulse repetition frequency		62.5		5000	SPS
DC_{PRF}	PRF duty cycle				25%	
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz and 60 Hz, LED1 and LED2 with R_{SERIES} = 500 kΩ, R_F = 500 kΩ		75		dB
		f_{CM} = 50 Hz and 60 Hz, LED1-AMB and LED2-AMB with R_{SERIES} = 500 kΩ, R_F = 500 kΩ		95		dB
PSRR	Power-supply rejection ratio	f_{PS} = 50 Hz, 60 Hz at PRF = 200 Hz		100		dB
		f_{CM} = 50 Hz, 60 Hz at PRF = 600 Hz		106		dB
$PSRR_{LED}$	PSRR, transmit LED driver	With respect to ripple on LED_DRV_SUP		75		dB
$PSRR_{Tx}$	PSRR, transmit control	With respect to ripple on TX_CTRL_SUP		60		dB
$PSRR_{Rx}$	PSRR, receiver	With respect to ripple on RX_ANA_SUP and RX_DIG_SUP		60		dB
	Total integrated noise current, input-referred (receiver with transmitter loop back, 0.1-Hz to 20-Hz bandwidth)	R_F = 100 kΩ with stage 2 gain disabled, PRF = 1200 Hz, duty cycle = 5%		36		pA_{RMS}
		R_F = 500 kΩ with ambient cancellation enabled and stage 2 gain = 4, PRF = 1200 Hz, duty cycle = 25%		13		pA_{RMS}
N_{FB}	Noise-free bits (receiver with transmitter loop back, 0.1-Hz to 20-Hz bandwidth)(1)	R_F = 100 kΩ, PRF = 1200 Hz, duty cycle = 5%		14.3		Bits
		R_F = 500 kΩ, PRF = 1200 Hz, duty cycle = 25%		13.5		Bits
RECEIVER FUNCTIONAL BLOCK LEVEL SPECIFICATION						
	Total integrated noise current, input-referred (receiver alone) over 0.1-Hz to 5-Hz bandwidth	R_F = 500 kΩ, ambient cancellation enabled, stage 2 gain = 4, PRF = 1300 Hz, LED duty cycle = 25%		1.4		pA_{RMS}
		R_F = 500 kΩ, ambient cancellation enabled, stage 2 gain = 4, PRF = 1300 Hz, LED duty cycle = 5%		5		pA_{RMS}

(1) Noise-free bits (N_{FB}) are defined as:

$$N_{FB} = \log 2 \left(\frac{I_{PD}}{6.6 \times I_{NOISE}} \right)$$

where: I_{PD} is the photodiode current, and I_{NOISE} is the input-referred RMS noise current.

Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –40°C to 85°C. Typical specifications are at 25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I-V TRANSIMPEDANCE AMPLIFIER						
G	Gain	R_F = 10 kΩ to R_F = 1 MΩ		See the *Receiver Channel* section for details		V/µA
	Gain accuracy			±7%		
	Feedback resistance	R_F		10k, 25k, 50k, 100k, 250k, 500k, and 1M		Ω
	Feedback resistor tolerance	R_F		±7%		
	Feedback capacitance	C_F		5, 10, 25, 50, 100, and 250		pF
	Feedback capacitor tolerance	C_F		±20%		
$V_{OD(fs)}$	Full-scale differential output voltage			1		V
	Common-mode voltage on input pins	Set internally		0.9		V
	External differential input capacitance	Includes equivalent capacitance of photodiode, cables, EMI filter, and so forth	10		1000	pF
$V_{O(shield)}$	Shield output voltage, V_{CM}	With a 1-kΩ series resistor and a 10-nF decoupling capacitor to ground, when loaded with a small current (for example, of a few µA or less)	0.8	0.9	1.0	V
AMBIENT CANCELLATION STAGE						
G	Gain			0, 3.5, 6, 9.5, and 12		dB
	Current DAC range		0		10	µA
	Current DAC step size			1		µA
LOW-PASS FILTER						
	Low-pass corner frequency	3-dB attenuation		0.5 and 1		kHz
	Pass-band attenuation, 2 Hz to 10 Hz	Duty cycle = 25%		0.004		dB
		Duty cycle = 10%		0.041		dB
	Filter settling time	After diagnostics mode with filter corner = 500 Hz		28		ms
		After diagnostics mode with filter corner = 1000 Hz		16		ms
	ADC bypass outputs output impedance	RXOUTP and RXOUTN		1		kΩ
ANALOG-TO-DIGITAL CONVERTER						
	Resolution				22	Bits
	Sample rate	See the *ADC Operation and Averaging Module* section		4 × PRF		SPS
	ADC full-scale voltage			±1.2		V
	ADC conversion time	See the *ADC Operation and Averaging Module* section	50		PRF / 4	µs
	ADC reset time		2			t_{CLK}
TRANSMITTER						
	Output current range			0, 50, 75, 100, 150, and 200 (see the *LEDCNTRL: LED Control Register* for details)		mA
	LED current DAC error			±5%		
	Output current resolution			8		Bits
	Transmitter noise dynamic range	0.1-Hz to 20-Hz bandwidth, at 25-mA output current		110		dB
		0.1-Hz to 20-Hz bandwidth, at 100-mA output current		110		dB
	Minimum sample time of LED1 and LED2 pulses			50		µs
	LED current DAC leakage current	LED_ON = 0		1		µA
		LED_ON = 1		50		µA
	LED current DAC linearity	Percent of full-scale current		0.5%		
	Output current settling time (with resistive load)	From zero current to 150 mA		7		µs
		From 150 mA to zero current		7		µs

Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –40°C to 85°C. Typical specifications are at 25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIAGNOSTICS						
	Duration of diagnostics state machine	EN_SLOW_DIAG = 0 Start of diagnostics after the DIAG_EN register bit is set. End of diagnostic indicated by DIAG_END going high.		8		ms
		EN_SLOW_DIAG = 1 Start of diagnostics after the DIAG_EN register bit is set. End of diagnostic indicated by DIAG_END going high.		16		ms
	Open fault resistance			> 100		kΩ
	Short fault resistance			< 10		kΩ
	Diagnostics current	During diagnostics mode		< 100		µA
INTERNAL OSCILLATOR						
f_{CLKOUT}	CLKOUT frequency	With an 8-MHz crystal connected to the XIN and XOUT pins		4		MHz
DC_{CLKOUT}	CLKOUT duty cycle			50%		
	Crystal oscillator start-up time	With an 8-MHz crystal connected to the XIN and XOUT pins		200		µs
EXTERNAL CLOCK						
	Maximum allowable external clock jitter				50	ps
	External clock input frequency	±10%		8		MHz
	External clock input voltage	Voltage input high (V_{IH})	0.75 × RX_DIG_SUP			V
		Voltage input low (V_{IL})	0.25 × RX_DIG_SUP			V
	External clock input current			1		µA
TIMING						
	Wake-up time from complete power-down			1000		ms
	Wake-up time from Rx power-down			100		µs
	Wake-up time from Tx power-down			1000		ms
$t_{\overline{RESET}}$	Active low $\overline{RESET}$ pulse duration			1		ms
$t_{DIAGEND}$	DIAG_END pulse duration at diagnostics completion			4		CLKOUT cycles
t_{ADCRDY}	ADC_RDY pulse duration			1		CLKOUT cycles
DIGITAL SIGNAL CHARACTERISTICS						
V_{IH}	Logic high input voltage	$\overline{AFE\_PDN}$, SPI CLK, SPI SIMO, SPI STE, $\overline{RESET}$	0.75 × RX_DIG_SUP			V
V_{IL}	Logic low input voltage	$\overline{AFE\_PDN}$, SPI CLK, SPI SIMO, SPI STE, $\overline{RESET}$			0.25 × RX_DIG_SUP	V
I_{IN}	Logic input current	Digital inputs at V_{IH} or V_{IL}		0.1		µA
V_{OH}	Logic high output voltage	DIAG_END, LED_ALM, PD_ALM, SPI SOMI, ADC_RDY, CLKOUT	RX_DIG_SUP – 0.1			V
V_{OL}	Logic low output voltage	DIAG_END, LED_ALM, PD_ALM, SPI SOMI, ADC_RDY, CLKOUT			0.1	V
PIN LEAKAGE CURRENT						
	Pin leakage current	To GND and supply		1		nA

Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –40°C to 85°C. Typical specifications are at 25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
	Receiver analog supply current	RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 disabled		0.6		mA
		RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 enabled		0.7		mA
	Receiver digital supply current	RX_DIG_SUP = 3.0 V		0.27		mA
	ADC bypass mode	RX_ANA_SUP + RX_DIG_SUP (Excluding external ADC current)		1.8		mA
LED_DRV_SUP	LED driver supply current	With zero LED current setting		55		µA
TX_CTRL_SUP	Transmitter control supply current			15		µA
	Complete power-down (using AFE_PDN pin)	Receiver current only (RX_ANA_SUP)		3		µA
		Receiver current only (RX_DIG_SUP)		3		µA
		Transmitter current only (LED_DRV_SUP)		1		µA
		Transmitter current only (TX_CTRL_SUP)		1		µA
	Power-down Rx alone	Receiver current only (RX_ANA_SUP)		220		µA
		Receiver current only (RX_DIG_SUP)		220		µA
	Power-down Tx alone	Transmitter current only (LED_DRV_SUP)		2		µA
		Transmitter current only (TX_CTRL_SUP)		2		µA

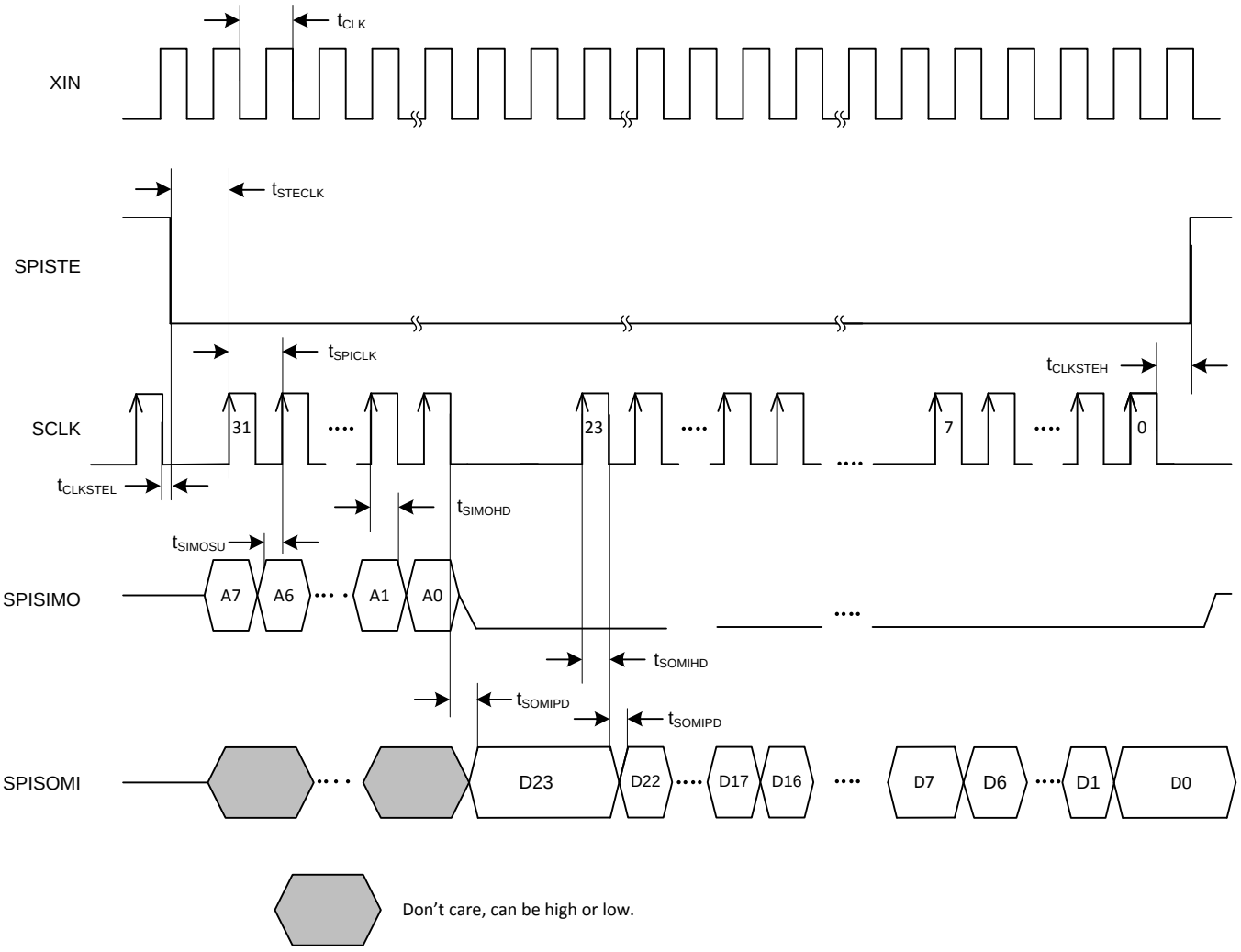
Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –40°C to 85°C. Typical specifications are at 25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER DISSIPATION							
$P_{D(q)}$	Quiescent power dissipation		Normal operation (excluding LEDs)		2.84		mW
			Power-down		0.1		mW
	Power-down with the AFE_PDN pin	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		1		µA
		TX_CTRL_SUP			1		µA
		RX_ANA_SUP			5		µA
		RX_DIG_SUP			0.1		µA
	Power-down with the PDNAFE register bit	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		1		µA
		TX_CTRL_SUP			1		µA
		RX_ANA_SUP			15		µA
		RX_DIG_SUP			20		µA
	Power-down Rx	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		50		µA
		TX_CTRL_SUP			15		µA
		RX_ANA_SUP			220		µA
		RX_DIG_SUP			220		µA
	Power-down Tx	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		2		µA
		TX_CTRL_SUP			2		µA
		RX_ANA_SUP			600		µA
		RX_DIG_SUP			230		µA
	After reset, with 8-MHz clock running	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		55		µA
		TX_CTRL_SUP			15		µA
		RX_ANA_SUP			600		µA
		RX_DIG_SUP			230		µA
	With stage 2 mode enabled and 8-MHz clock running	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		55		µA
		TX_CTRL_SUP			15		µA
		RX_ANA_SUP			700		µA
		RX_DIG_SUP			270		µA

7.6 Timing Requirements: Serial Interface

		MIN	TYP	MAX	UNIT
t_{CLK}	Clock frequency on XIN pin		8		MHz
t_{SCLK}	Serial shift clock period	62.5			ns
t_{STECLK}	STE low to SCLK rising edge, setup time	10			ns
$t_{CLKSTEH,L}$	SCLK transition to SPI STE high or low	10			ns
t_{SIMOSU}	SIMO data to SCLK rising edge, setup time	10			ns
t_{SIMOHD}	Valid SIMO data after SCLK rising edge, hold time	10			ns
t_{SOMIPD}	SCLK falling edge to valid SOMI, setup time	17			ns
t_{SOMIHD}	SCLK rising edge to invalid data, hold time	0.5			t_{SCLK}



(1) The SPI_READ register bit must be enabled before attempting a register read.

(2) Specify the register address whose contents must be read back on A[7:0].

(3) The AFE outputs the contents of the specified register on the SOMI pin.

Figure 1. Serial Interface Timing Diagram, Read Operation (1)(2)(3)

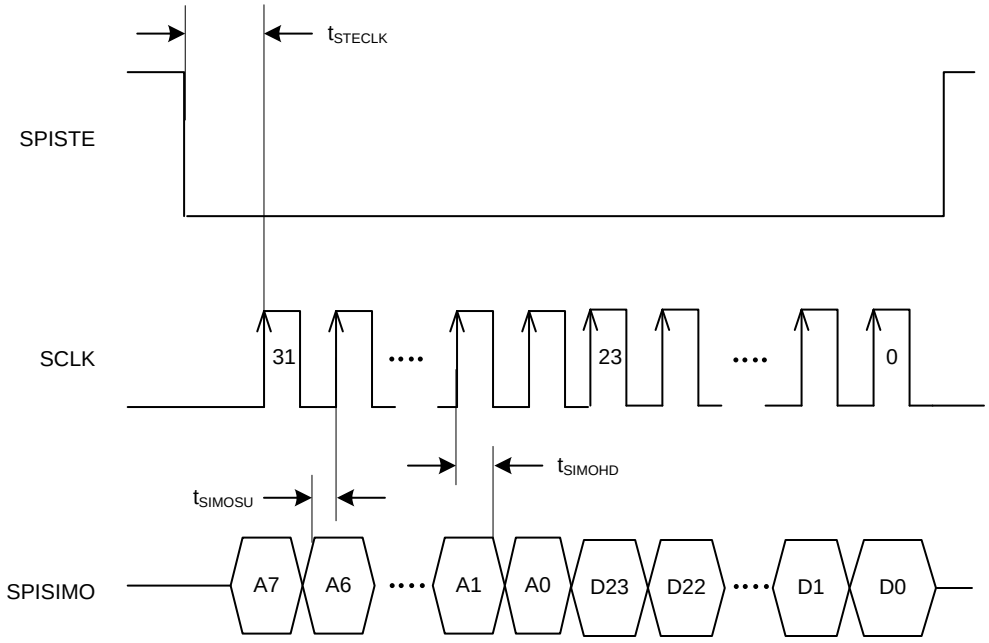


Figure 2. Serial Interface Timing Diagram, Write Operation

7.7 Supply Ramp and Power-Down Timing Requirements

		VALUE
t_1	Time between Rx and Tx supplies ramping up	Keep as small as possible (for example, ±10 ms)
t_2	Time between both supplies stabilizing and high-going edge of $\overline{\text{RESET}}$	> 100 ms
t_3	$\overline{\text{RESET}}$ pulse width	> 0.5 ms
t_4	Time between $\overline{\text{RESET}}$ and SPI commands	> 1 µs
t_5	Time between SPI commands and the ADC_$\overline{\text{RESET}}$ which corresponds to valid data	> 3 ms of cumulative sampling time in each phase(1)(2)(3)
t_6	Time between $\overline{\text{RESET}}$ pulse and high-accuracy data coming out of the signal chain	> 1 s(3)
t_7	Time from AFE_$\overline{\text{PDN}}$ high-going edge and $\overline{\text{RESET}}$ pulse(4)	> 100 ms
t_8	Time from AFE_$\overline{\text{PDN}}$ high-going edge (or PDN_AFE bit reset) to high-accuracy data coming out of the signal chain	> 1 s(3)

(1) This time is required for each of the four switched RC filters to fully settle to the new settings. The same time is applicable whenever there is a change to any of the signal chain controls (for example, LED current setting, TIA gain, and so forth)
(2) If the SPI commands involve a change in the value of TX_REF from its default, then there is additional wait time that is approximately 1 s (for a 2.2-µF decoupling capacitor on the TX_REF pin).
(3) Dependent on the value of the capacitors on the BG and TX_REF pins. The 1-s wait time is necessary when the capacitors are 2.2 µF and scale down proportionate to the capacitor value. A very low capacitor (for example, 0.1 µF) on these pins causes the transmitter dynamic range to reduce to approximately 100 dB.
(4) After an active power-down from AFE_$\overline{\text{PDN}}$, reset the device by using a low-going pulse on $\overline{\text{RESET}}$.

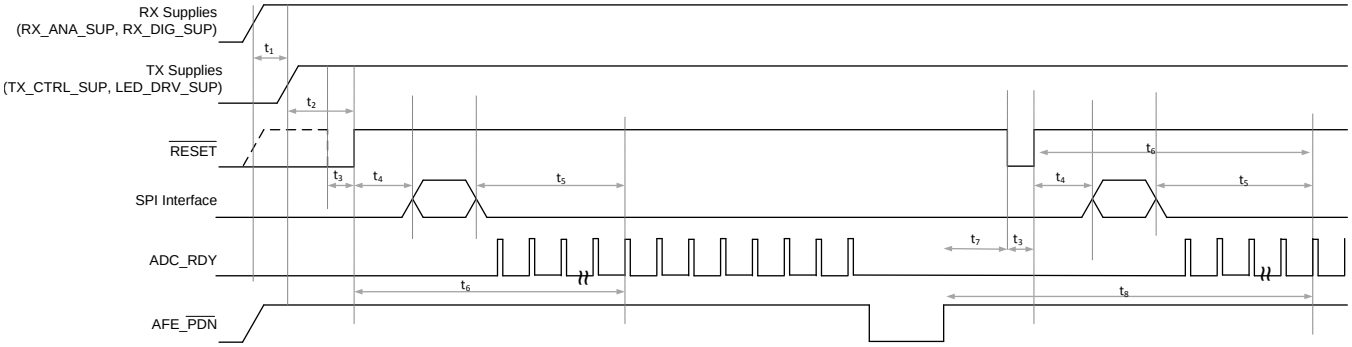


Figure 3. Supply Ramp and Hardware Power-Down Timing

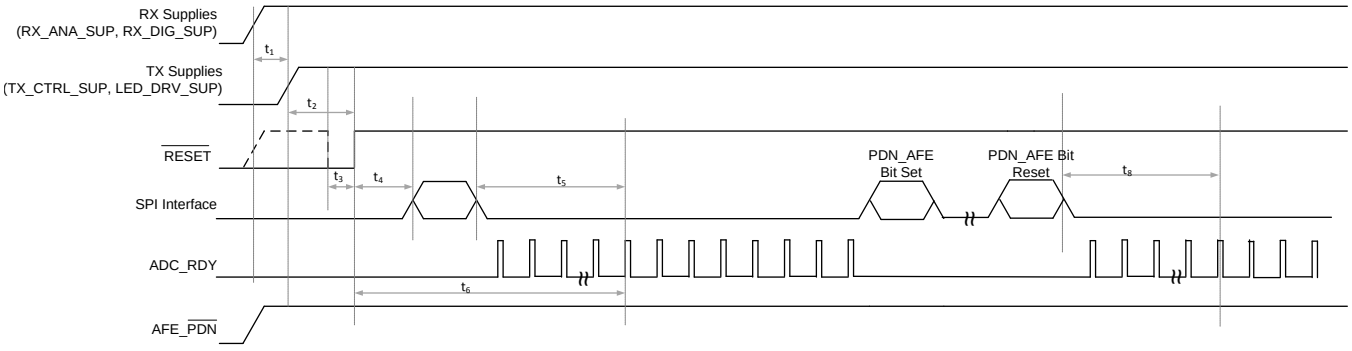


Figure 4. Supply Ramp and Software Power-Down Timing

7.8 Typical Characteristics

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

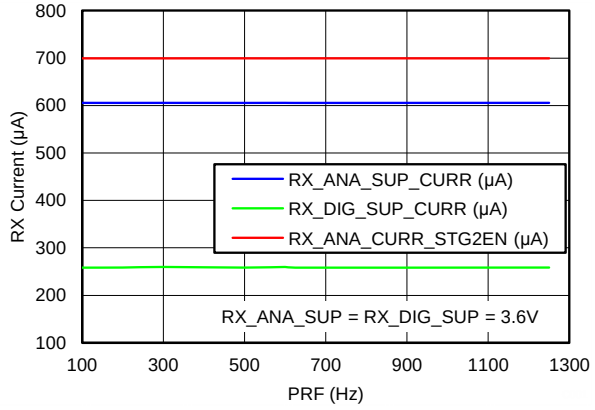


Figure 5. Total Rx Current vs PRF

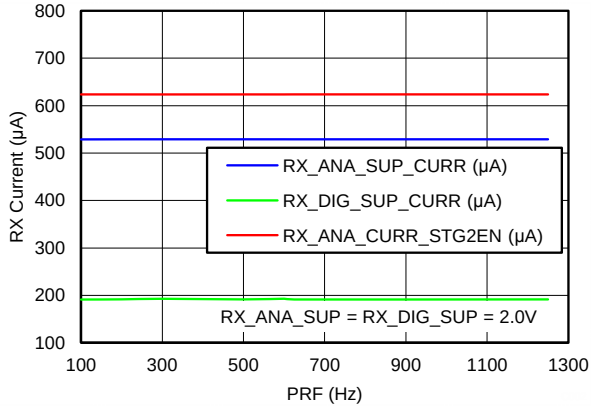


Figure 6. Total Rx Current vs PRF

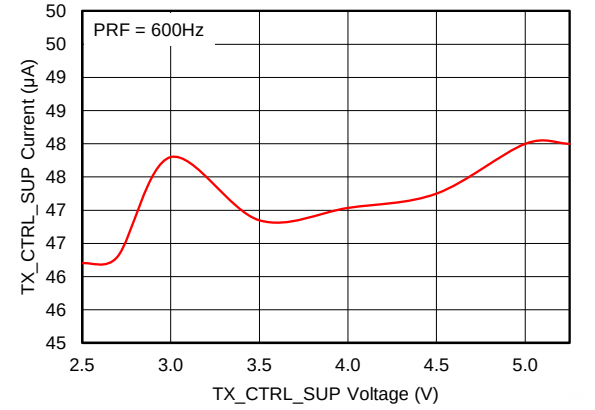


Figure 7. TX_CTRL_SUP Current vs TX_CTRL_SUP Voltage

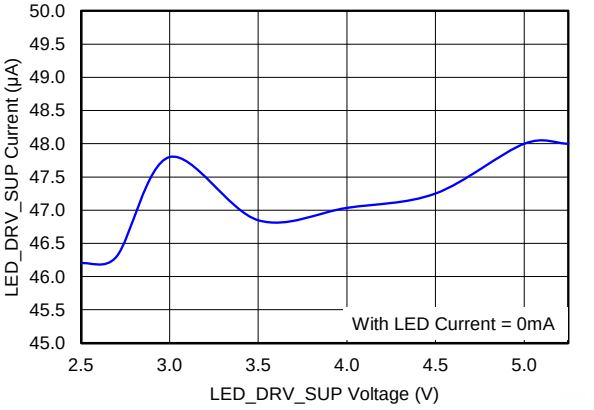


Figure 8. LED_DRV_SUP Current vs LED_DRV_SUP Voltage

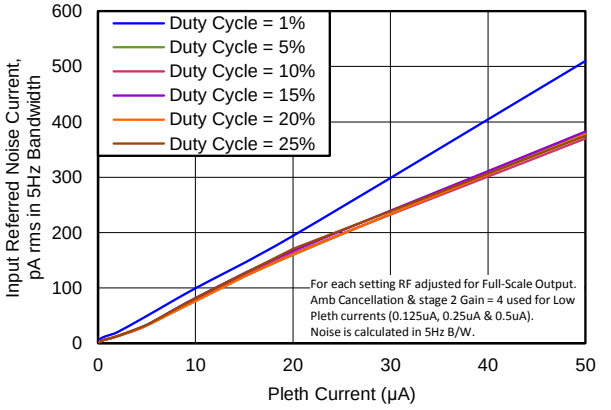


Figure 9. Input-Referred Noise Current vs PLETH Current (BW = 5 Hz, PRF = 100 Hz)

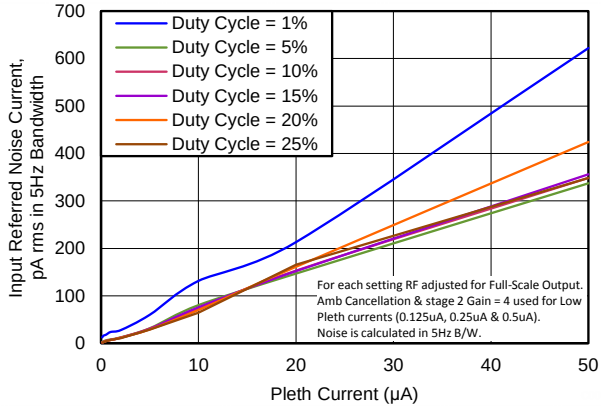


Figure 10. Input-Referred Noise Current vs PLETH Current (BW = 5 Hz, PRF = 300 Hz)

Typical Characteristics (continued)

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

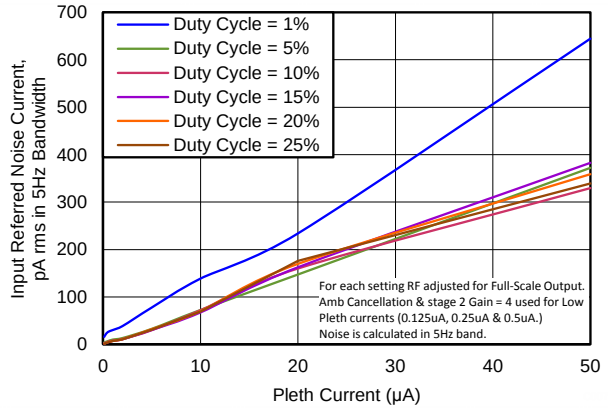


Figure 11. Input-Referred Noise Current vs PLETH Current (BW = 5 Hz, PRF = 600 Hz)

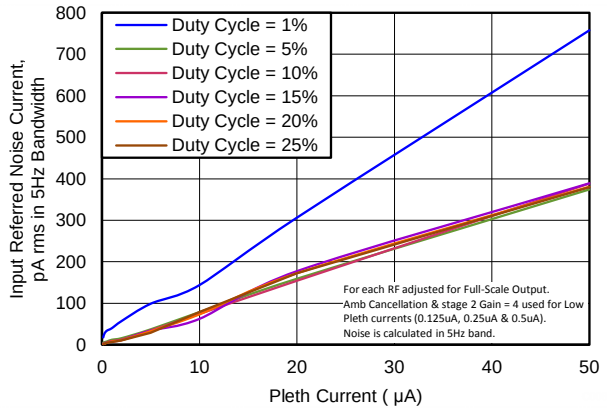


Figure 12. Input-Referred Noise Current vs PLETH Current (BW = 5 Hz, PRF = 1200 Hz)

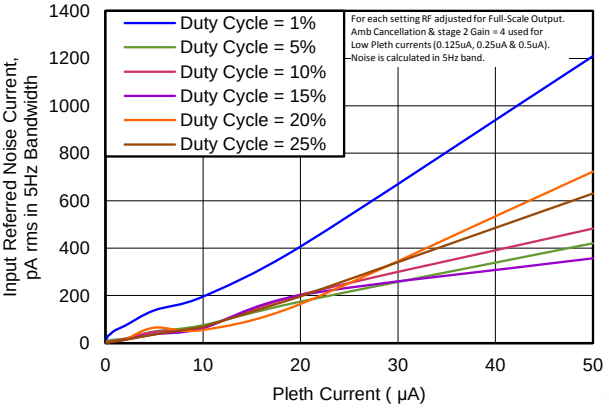


Figure 13. Input-Referred Noise Current vs PLETH Current (BW = 5 Hz, PRF = 2500 Hz)

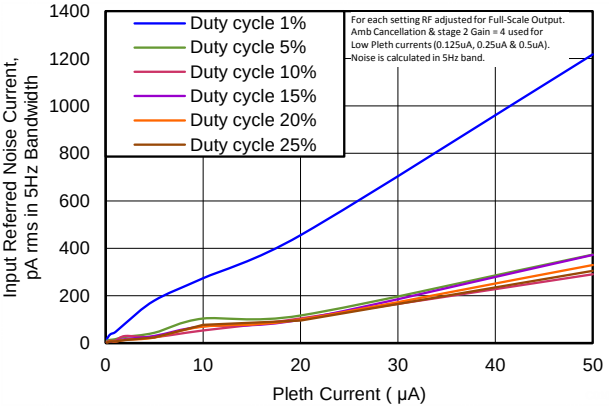


Figure 14. Input-Referred Noise Current vs PLETH Current (BW = 5 Hz, PRF = 5000 Hz)

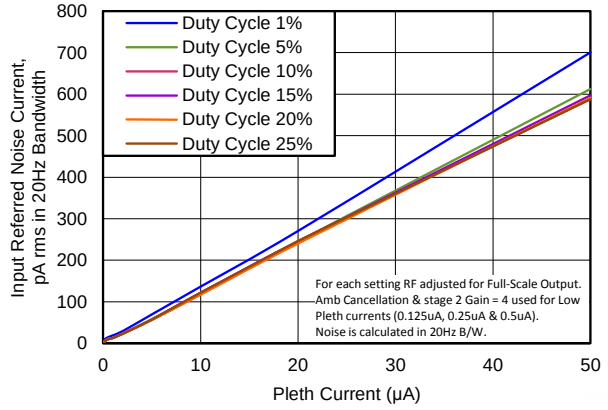


Figure 15. Input-Referred Noise Current vs PLETH Current (BW = 20 Hz, PRF = 100 Hz)

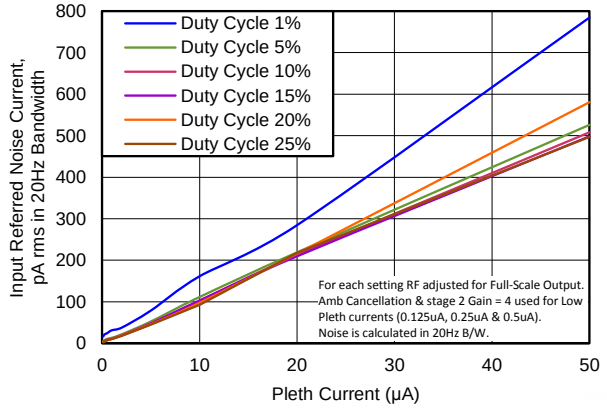


Figure 16. Input-Referred Noise Current vs PLETH Current (BW = 20 Hz, PRF = 300 Hz)

Typical Characteristics (continued)

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

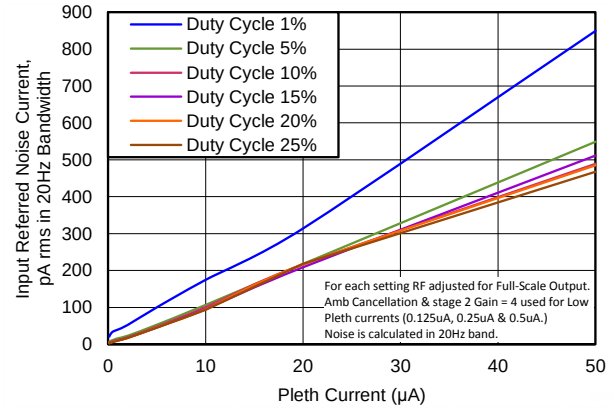


Figure 17. Input-Referred Noise Current vs PLETH Current (BW = 20 Hz, PRF = 600 Hz)

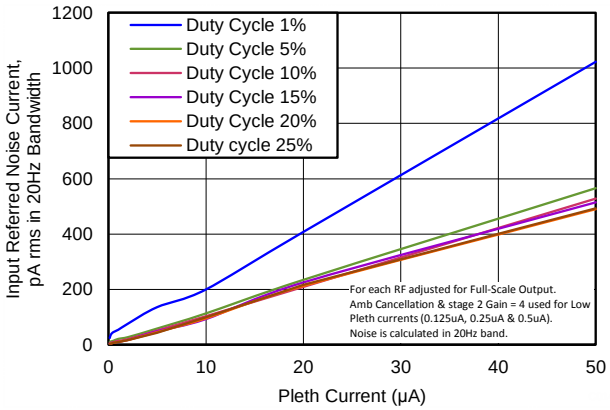


Figure 18. Input-Referred Noise Current vs PLETH Current (BW = 20 Hz, PRF = 1200 Hz)

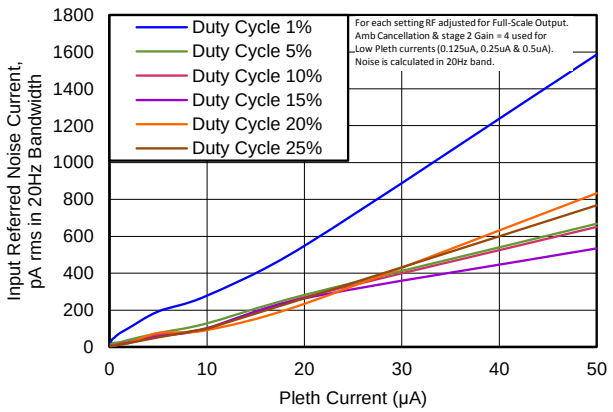


Figure 19. Input-Referred Noise Current vs PLETH Current (BW = 20 Hz, PRF = 2500 Hz)

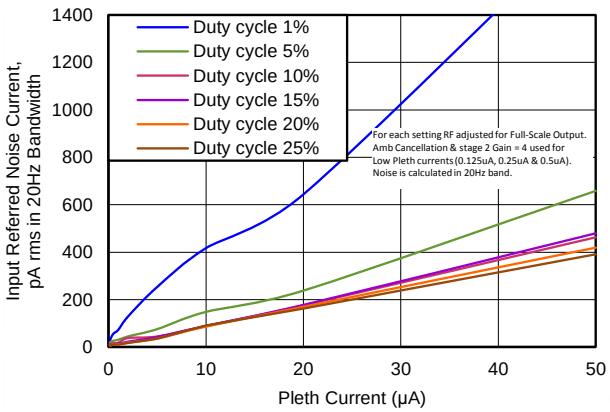


Figure 20. Input-Referred Noise Current vs PLETH Current (BW = 20 Hz, PRF = 5000 Hz)

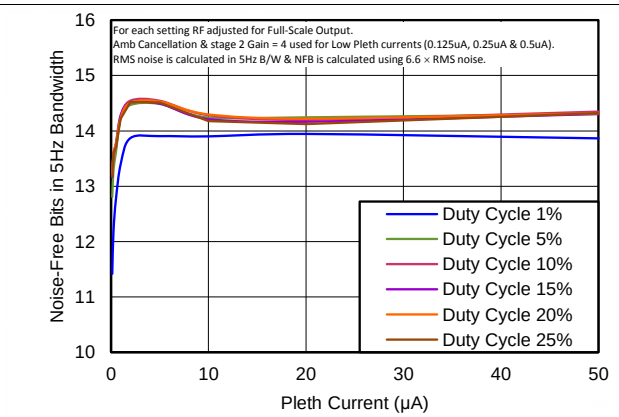


Figure 21. Noise-Free Bits vs PLETH Current (BW = 5 Hz, PRF = 100 Hz)

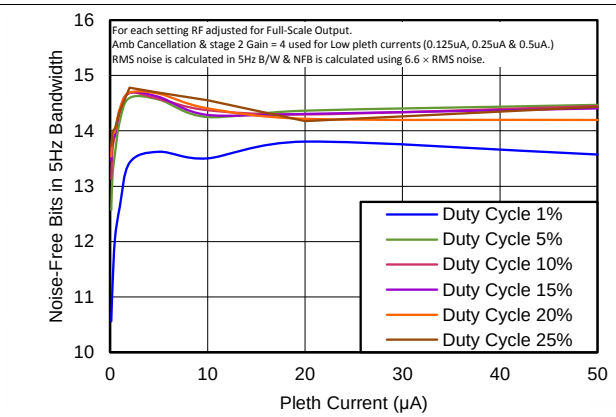


Figure 22. Noise-Free Bits vs PLETH Current (BW = 5 Hz, PRF = 300 Hz)

Typical Characteristics (continued)

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

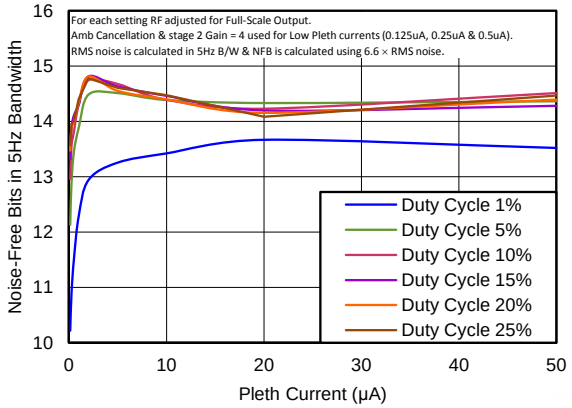


Figure 23. Noise-Free Bits vs PLETH Current (BW = 5 Hz, PRF = 600 Hz)

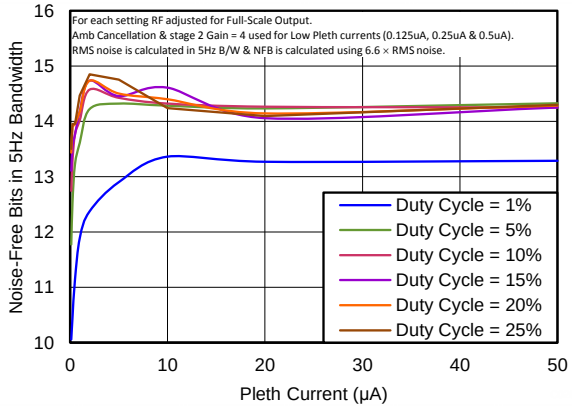


Figure 24. Noise-Free Bits vs PLETH Current (BW = 5 Hz, PRF = 1200 Hz)

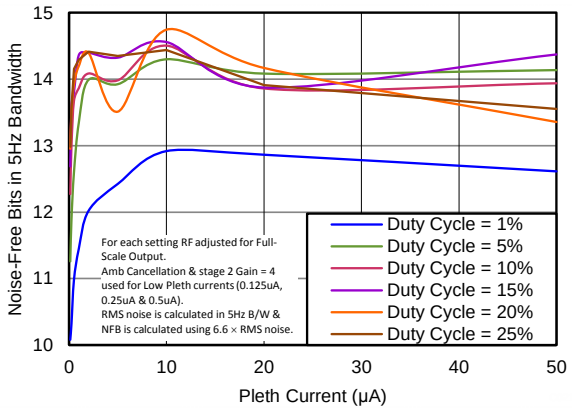


Figure 25. Noise-Free Bits vs PLETH Current (BW = 5 Hz, PRF = 2500 Hz)

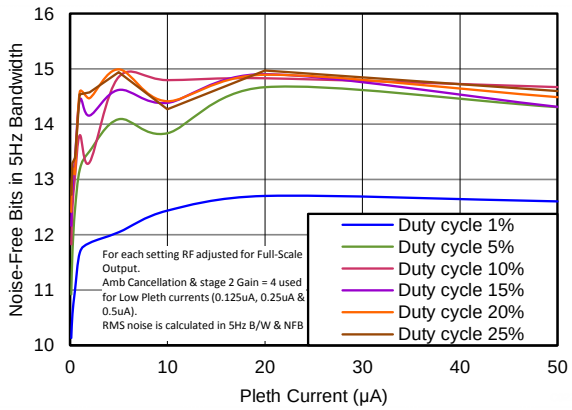


Figure 26. Noise-Free Bits vs PLETH Current (BW = 5 Hz, PRF = 5000 Hz)

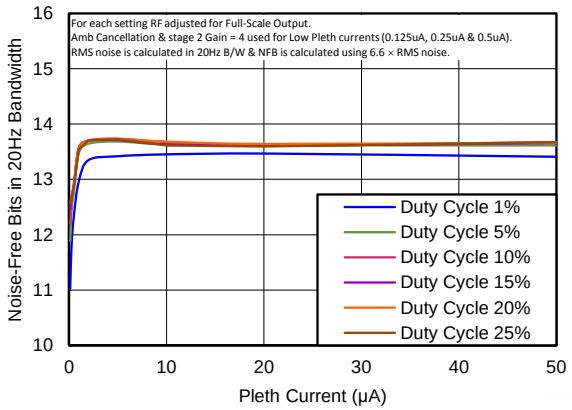


Figure 27. Noise-Free Bits vs PLETH Current (BW = 20 Hz, PRF = 100 Hz)

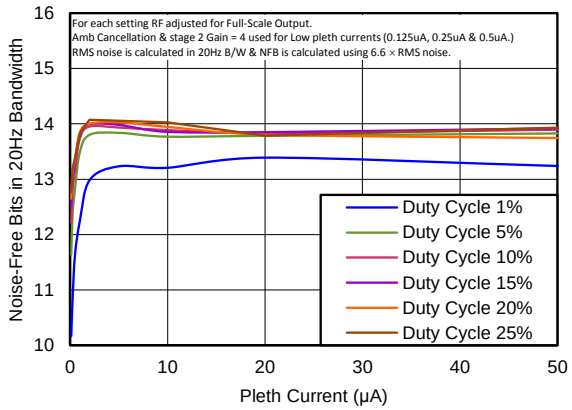


Figure 28. Noise-Free Bits vs PLETH Current (BW = 20 Hz, PRF = 300 Hz)

Typical Characteristics (continued)

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

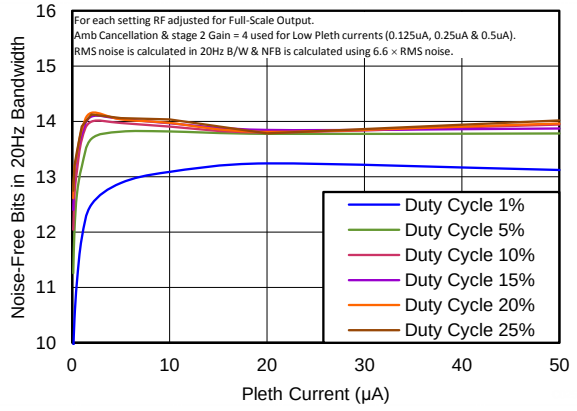


Figure 29. Noise-Free Bits vs PLETH Current (BW = 20 Hz, PRF = 600 Hz)

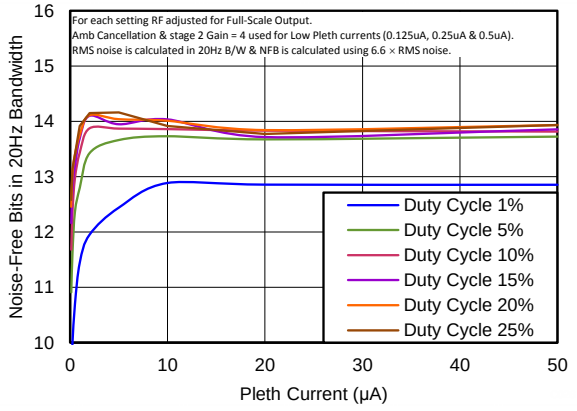


Figure 30. Noise-Free Bits vs PLETH Current (BW = 20 Hz, PRF = 1200 Hz)

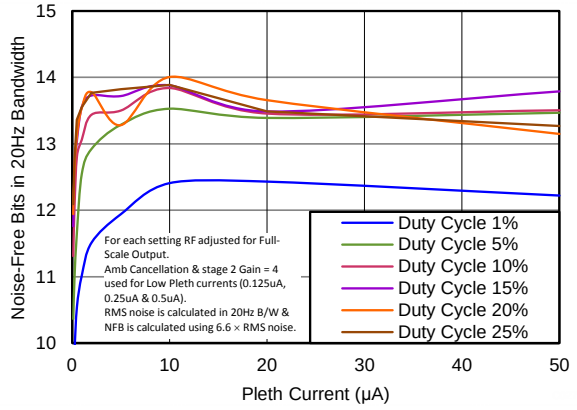


Figure 31. Noise-Free Bits vs PLETH Current (BW = 20 Hz, PRF = 2500 Hz)

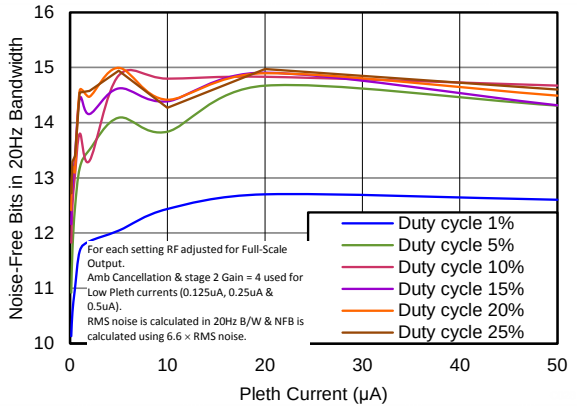


Figure 32. Noise-Free Bits vs PLETH Current (BW = 20 Hz, PRF = 5000 Hz)

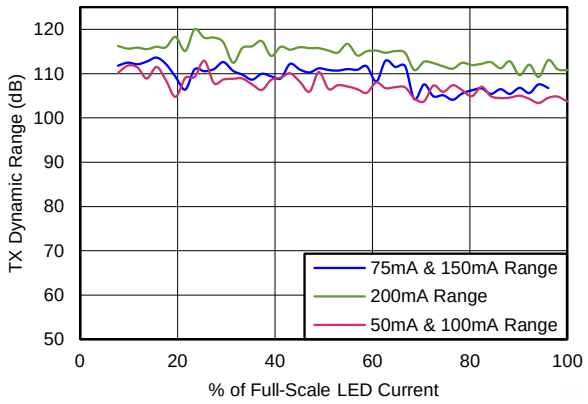


Figure 33. Transmitter Dynamic Range (5-Hz BW)

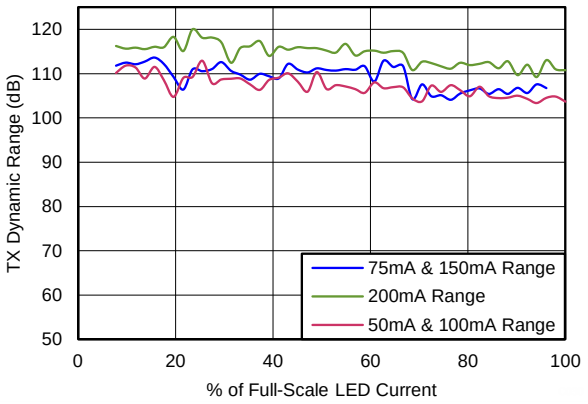


Figure 34. Transmitter Dynamic Range (20-Hz BW)

Typical Characteristics (continued)

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

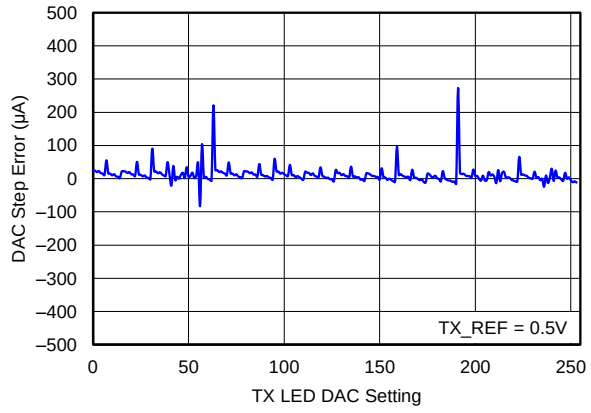


Figure 35. Transmitter DAC Current Step Error (200 mA, Max)

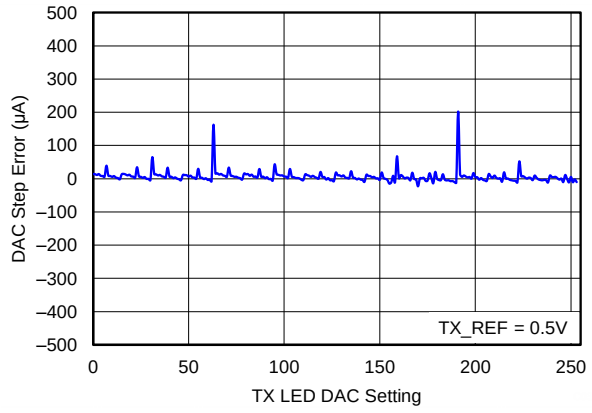


Figure 36. Transmitter DAC Current Step Error (150 mA, Max)

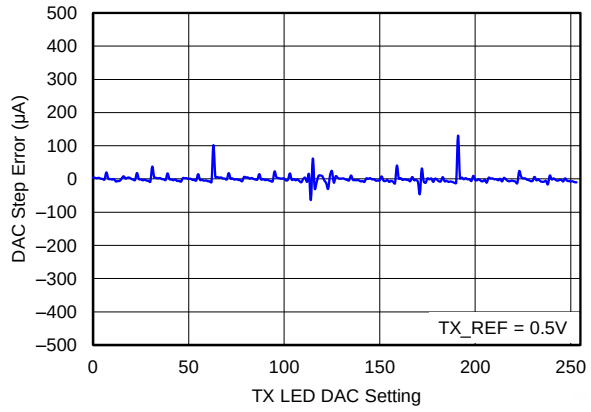


Figure 37. Transmitter DAC Current Step Error (100 mA, Max)

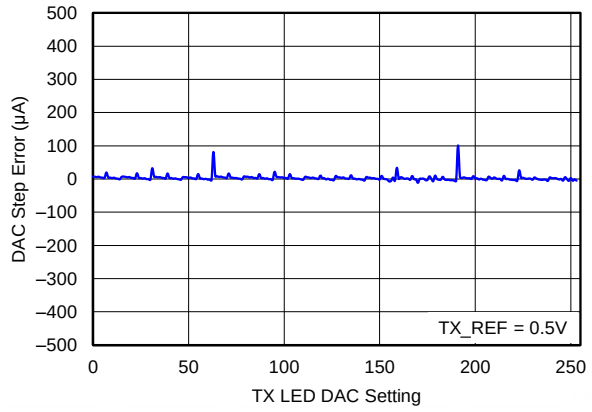


Figure 38. Transmitter DAC Current Step Error (75 mA, Max)

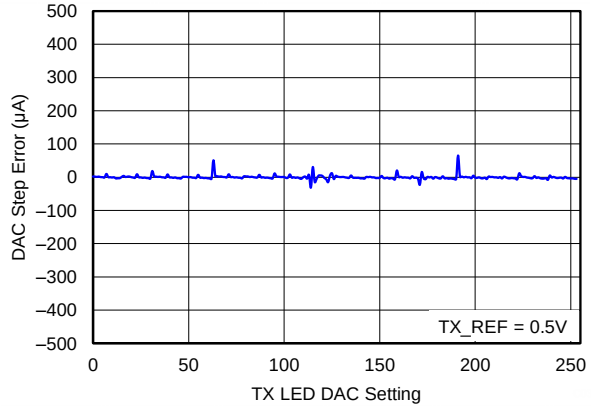


Figure 39. Transmitter DAC Current Step Error (50 mA, Max)

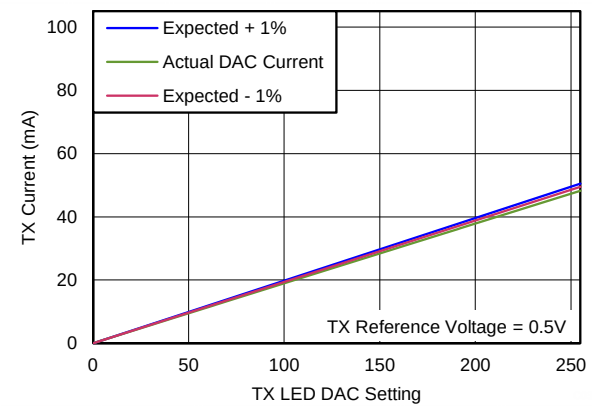


Figure 40. Transmitter Current Linearity (50-mA Range)

Typical Characteristics (continued)

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

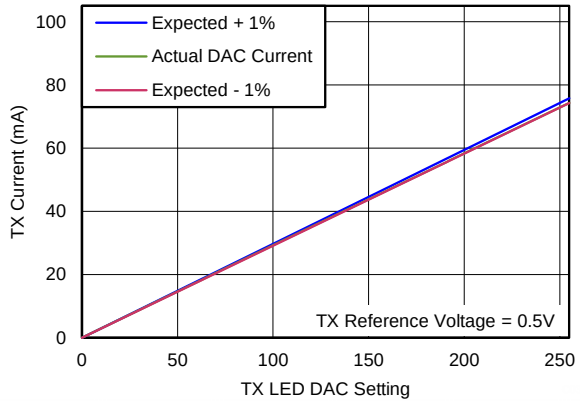


Figure 41. Transmitter Current Linearity (75-mA Range)

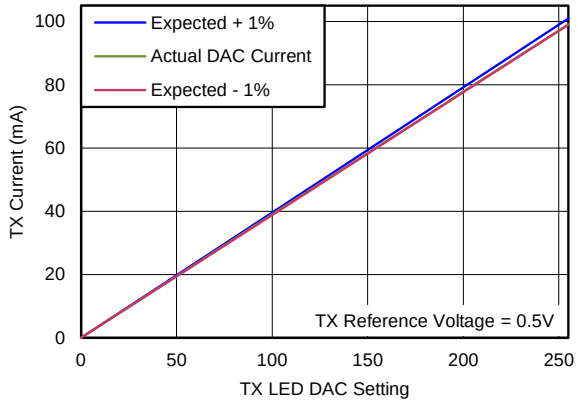


Figure 42. Transmitter Current Linearity (100-mA Range)

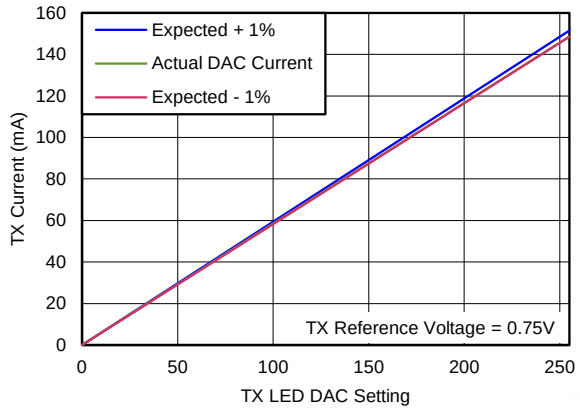


Figure 43. Transmitter Current Linearity (150-mA Range)

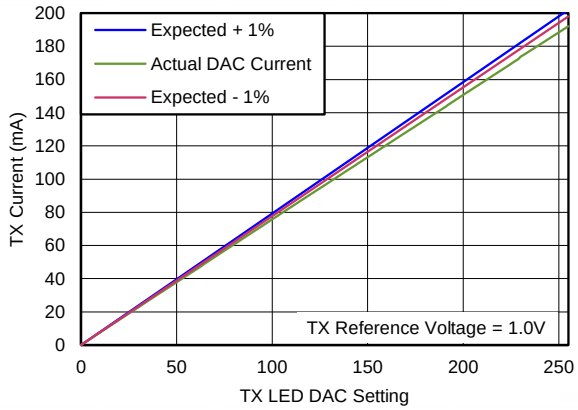


Figure 44. Transmitter Current Linearity (200-mA Range)

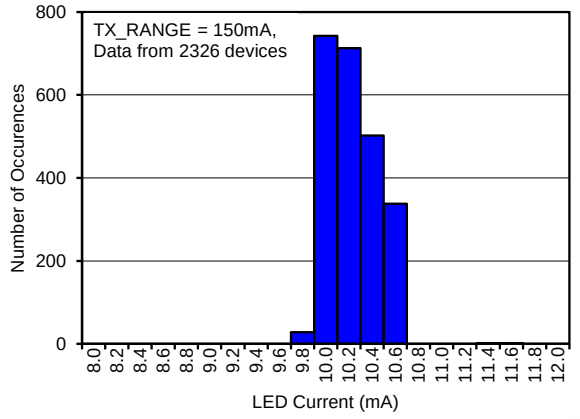


Figure 45. LED Current with Tx DAC Setting = 17 (10 mA)

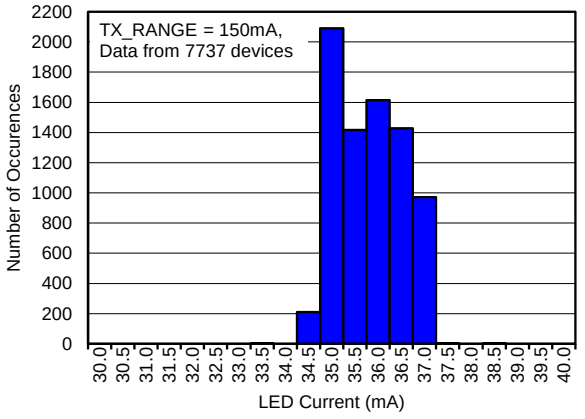


Figure 46. LED Current with Tx DAC Setting = 60 (35 mA)

Typical Characteristics (continued)

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

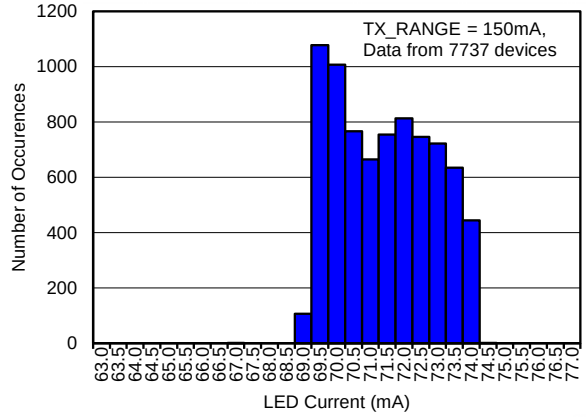


Figure 47. LED Current with Tx DAC Setting = 120 (70 mA)

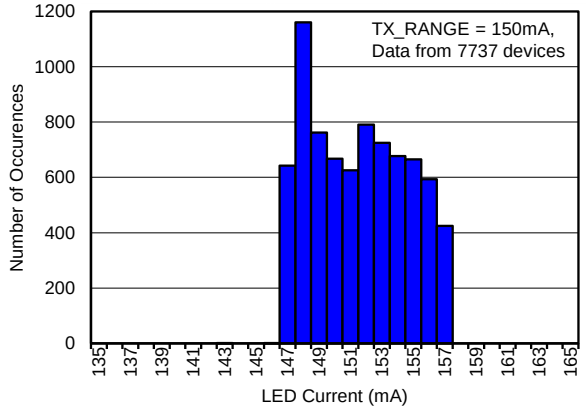


Figure 48. LED Current with Tx DAC Setting = 255 (150 mA)

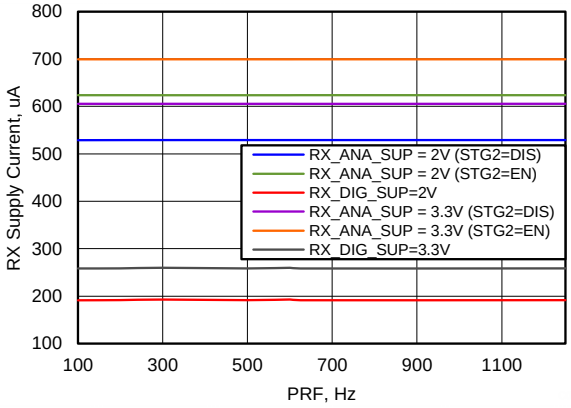


Figure 49. Receiver Supplies vs PRF

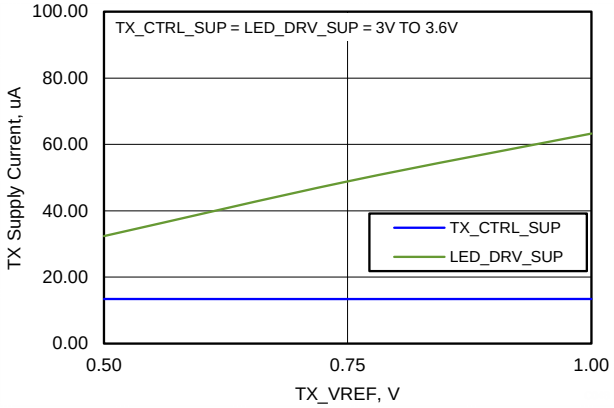


Figure 50. Transmitter Supplies vs TX_REF

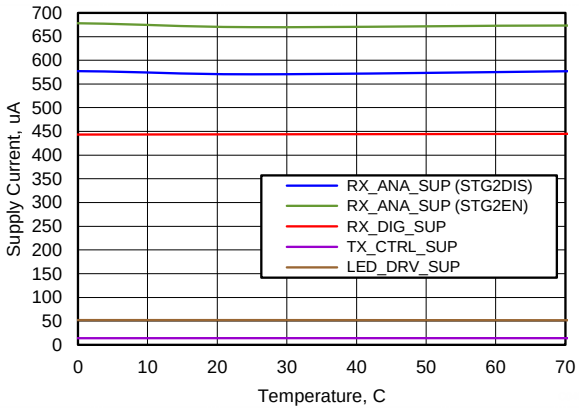


Figure 51. Power Supplies vs Temperature

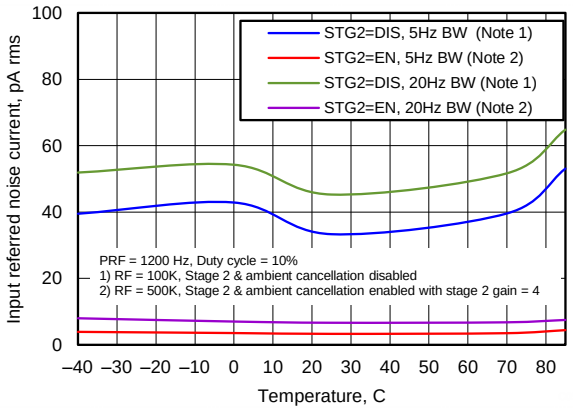


Figure 52. Input-Referred Noise vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 5 V, and f_{CLK} = 8 MHz, unless otherwise noted.

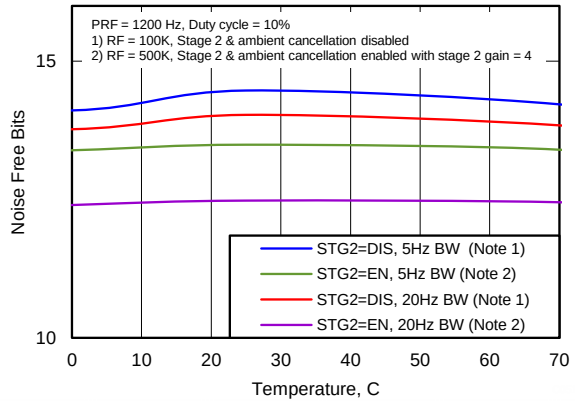


Figure 53. Noise-Free Bits vs Temperature

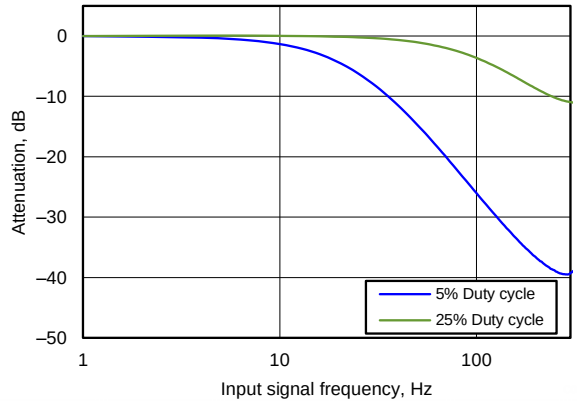


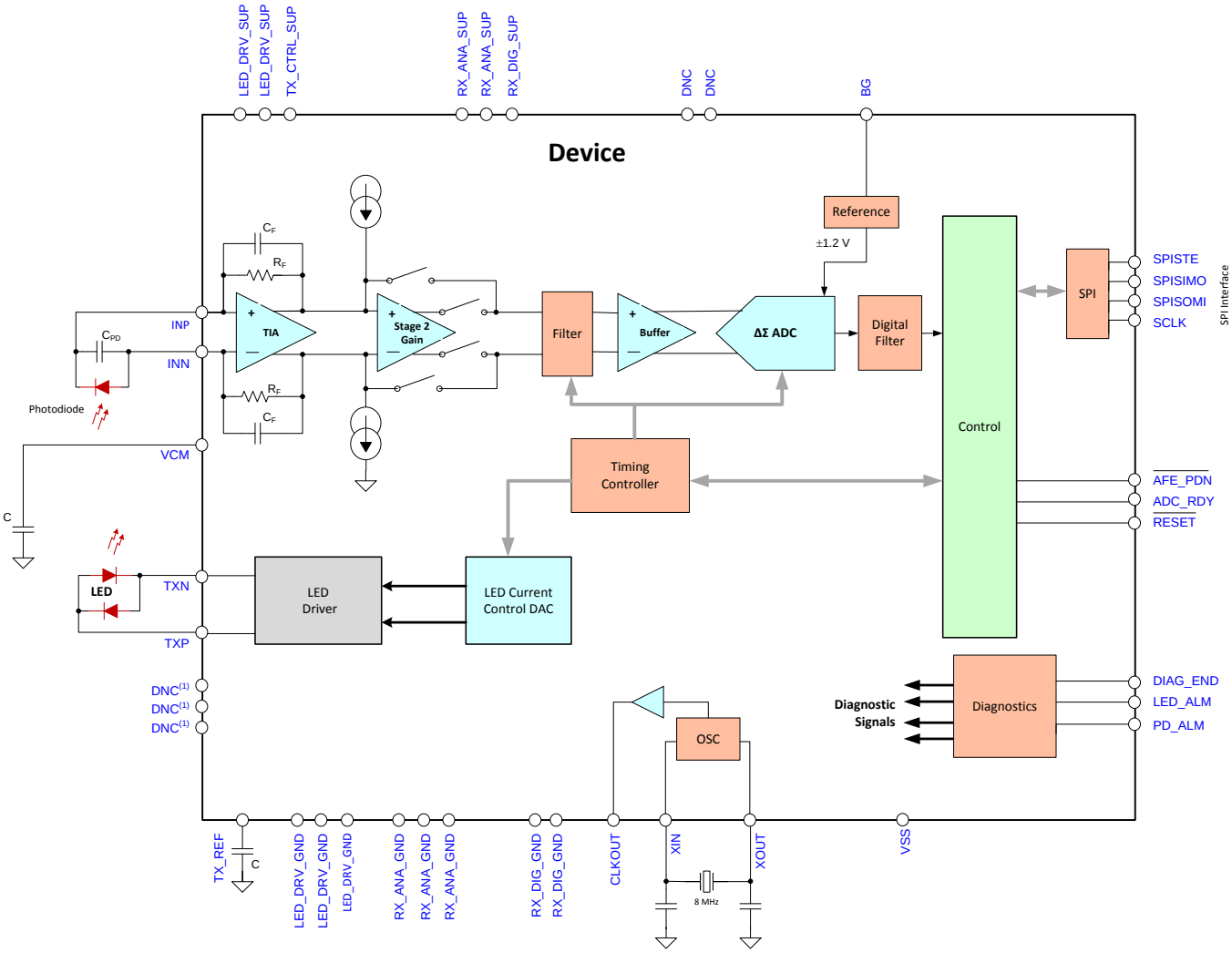
Figure 54. Filter Response vs Duty Cycle

8 Detailed Description

8.1 Overview

The AFE4490 is a complete analog front-end (AFE) solution targeted for pulse-oximeter applications. The device consists of a low-noise receiver channel, an LED transmit section, and diagnostics for sensor and LED fault detection. To ease clocking requirements and provide the low-jitter clock to the AFE, an oscillator is also integrated that functions from an external crystal. The device communicates to an external microcontroller or host processor using an SPI interface. The *Functional Block Diagram* section provides a detailed block diagram for the device. The blocks are described in more detail in the following sections.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Receiver Channel

This section describes the receiver channel functionality.

8.3.1.1 Receiver Front-End

The receiver consists of a differential current-to-voltage (I-V) transimpedance amplifier that converts the input photodiode current into an appropriate voltage, as shown in Figure 55. The feedback resistor of the amplifier (R_F) is programmable to support a wide range of photodiode currents. Available R_F values include: 1 MΩ, 500 kΩ, 250 kΩ, 100 kΩ, 50 kΩ, 25 kΩ, and 10 kΩ.

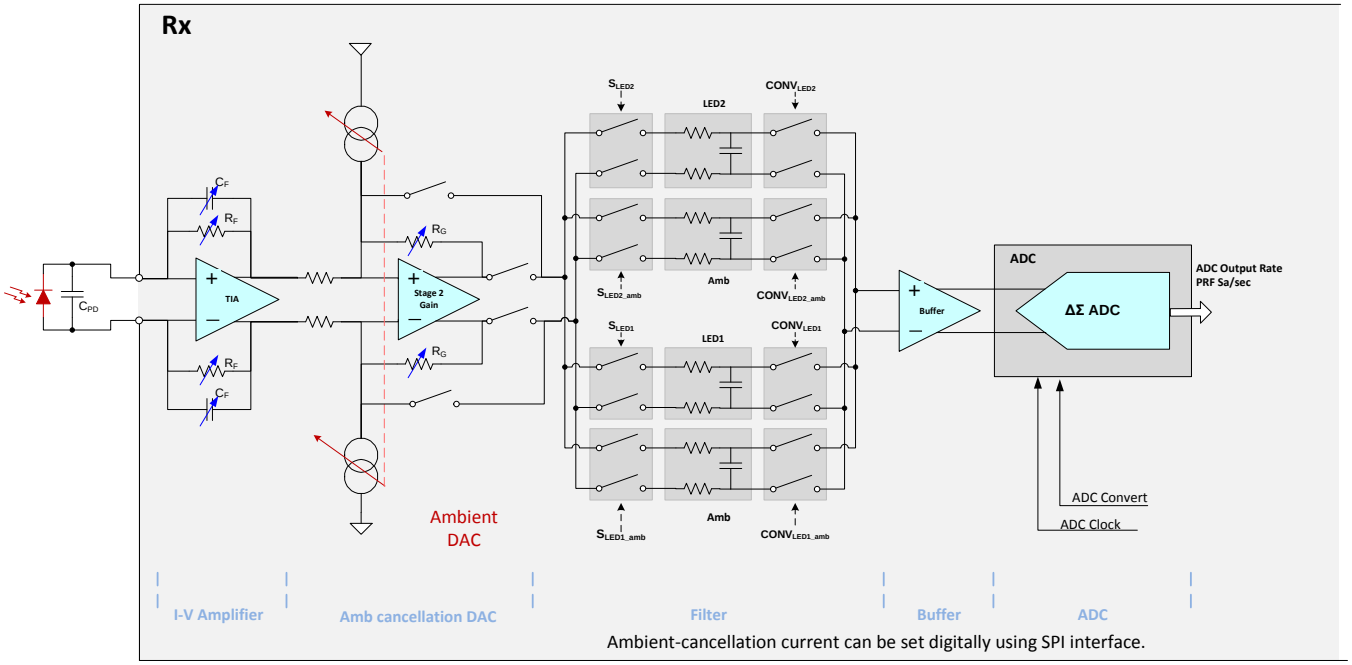


Figure 55. Receiver Front-End

The R_F amplifier and the feedback capacitor (C_F) form a low-pass filter for the input signal current. Always ensure that the low-pass filter RC time constant has sufficiently high bandwidth (as shown by Equation 1) because the input current consists of pulses. For this reason, the feedback capacitor is also programmable. Available C_F values include: 5 pF, 10 pF, 25 pF, 50 pF, 100 pF, and 250 pF. Any combination of these capacitors can also be used.

$$R_F \times C_F \leq \frac{\text{Rx Sample Time}}{10} \quad (1)$$

The output voltage of the I-V amplifier includes the pleth component (the desired signal) and a component resulting from the ambient light leakage. The I-V amplifier is followed by the second stage, which consists of a current digital-to-analog converter (DAC) that sources the cancellation current and an amplifier that gains up the pleth component alone. The amplifier has five programmable gain settings: 0 dB, 3.5 dB, 6 dB, 9.5 dB, and 12 dB. The gained-up pleth signal is then low-pass filtered (500-Hz bandwidth) and buffered before driving a 22-bit ADC. The current DAC has a cancellation current range of 10 µA with 10 steps (1 µA each). The DAC value can be digitally specified with the SPI interface. Using ambient compensation with the ambient DAC allows the dc-biased signal to be centered to near mid-point of the amplifier (±0.9 V). Using the gain of the second stage allows for more of the available ADC dynamic range to be used.

The output of the ambient cancellation amplifier is separated into LED2 and LED1 channels. When LED2 is on, the amplifier output is filtered and sampled on capacitor C_R. Similarly, the LED1 signal is sampled on the C_{LED1} capacitor when LED1 is ON. In between the LED2 and LED1 pulses, the idle amplifier output is sampled to estimate the ambient signal on capacitors C_{LED2_amb} and C_{LED1_amb}.

Feature Description (continued)

The sampling duration is termed the *Rx sample time* and is programmable for each signal, independently. Sampling can start after the I-V amplifier output is stable (to account for LED and cable settling times). The Rx sample time is used for all dynamic range calculations; the minimum time supported is 50 µs.

A single, 22-bit ADC converts the sampled LED2, LED1, and ambient signals sequentially. Each conversion takes a maximum of 25% of the pulse repetition period (PRP) and provides a single digital code at the ADC output. As discussed in the *Receiver Timing* section, the conversions are staggered so that the LED2 conversion starts after the end of the LED2 sample phase, and so on. This configuration also means that the Rx sample time for each signal is no greater than 25% of the pulse repetition period.

Note that four data streams are available at the ADC output (LED2, LED1, ambient LED2, and ambient LED1) at the same rate as the pulse repetition frequency. The ADC is followed by a digital ambient subtraction block that additionally outputs the (LED2 – ambient LED2) and (LED1 – ambient LED1) data values.

8.3.1.2 Ambient Cancellation Scheme

The receiver provides digital samples corresponding to ambient duration. The host processor (external to the AFE) can use these ambient values to estimate the amount of ambient light leakage. The processor must then set the value of the ambient cancellation DAC using the SPI, as shown in Figure 56.

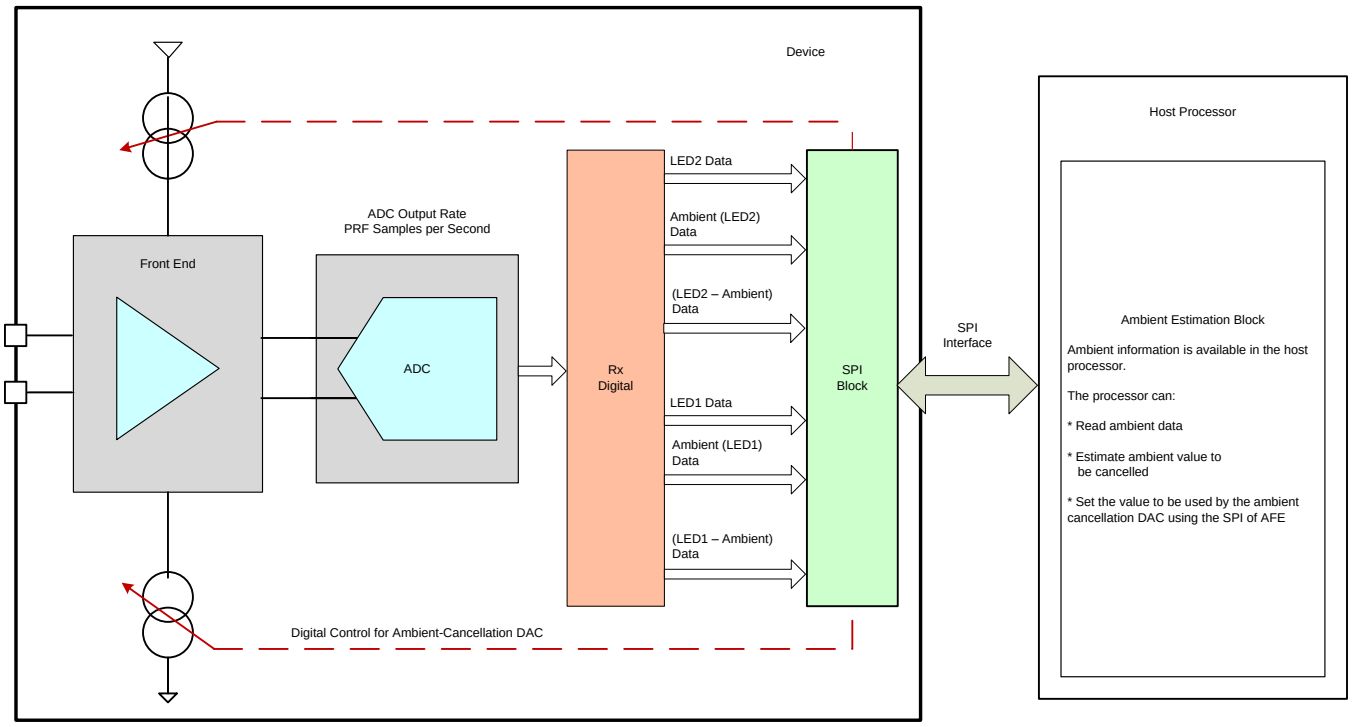


Figure 56. Ambient Cancellation Loop (Closed by the Host Processor)

Feature Description (continued)

Using the set value, the ambient cancellation stage subtracts the ambient component and gains up only the pleth component of the received signal, as shown in Figure 57. The amplifier gain is programmable to 0 dB, 3.5 dB, 6 dB, 9.5 dB, and 12 dB.

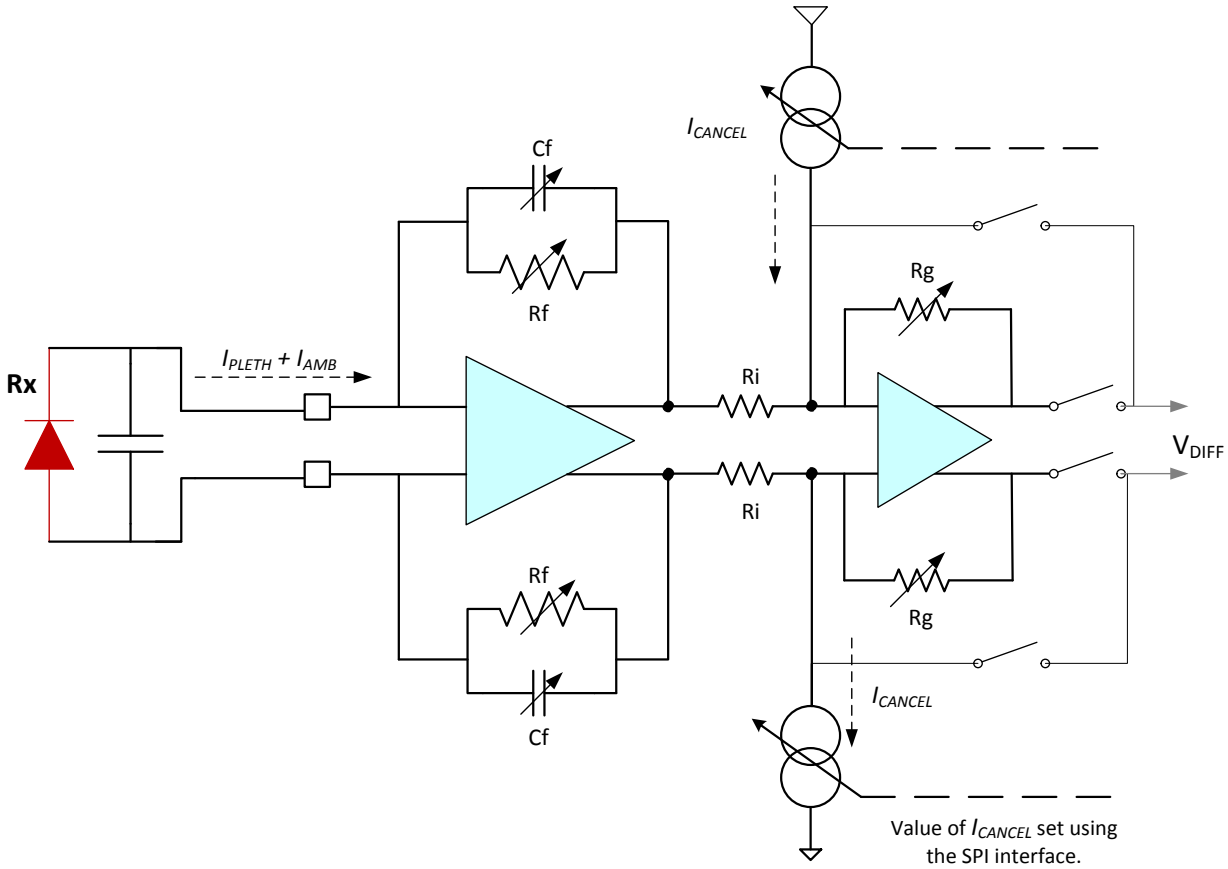


Figure 57. Front-End (I-V Amplifier and Cancellation Stage)

The differential output of the second stage is V_{DIFF}, as given by Equation 2:

$$V_{DIFF} = 2 \times \left(I_{PLETH} \times \frac{R_F}{R_I} + I_{AMB} \times \frac{R_F}{R_I} - I_{CANCEL} \right) \times R_G \quad (2)$$

where:

- R_I = 100 kΩ,
- I_{PLETH} = photodiode current pleth component,
- I_{AMB} = photodiode current ambient component, and
- I_{CANCEL} = the cancellation current DAC value (as estimated by the host processor).

Feature Description (continued)

R_G values with various gain settings are listed in Table 1.

Table 1. R_G Values

R_G (dB)	GAIN (kΩ)
0 (x1)	100
3.5 (x1.5)	150
6 (x2)	200
9.5 (x3)	300
12 (x4)	400

8.3.1.3 Receiver Control Signals

LED2 sample phase (S_{LED2}): When this signal is high, the amplifier output corresponds to the LED2 on-time. The amplifier output is filtered and sampled into capacitor C_{LED2}. To avoid settling effects resulting from the LED or cable, program S_{LED2} to start after the LED turns on. This settling delay is programmable.

Ambient sample phase (S_{LED2_amb}): When this signal is high, the amplifier output corresponds to the LED2 off-time and can be used to estimate the ambient signal (for the LED2 phase). The amplifier output is filtered and sampled into capacitor C_{LED2_amb}.

LED1 sample phase (S_{LED1}): When this signal is high, the amplifier output corresponds to the LED1 on-time. The amplifier output is filtered and sampled into capacitor C_{LED1}. To avoid settling effects resulting from the LED or cable, program S_{LED1} to start after the LED turns on. This settling delay is programmable.

Ambient sample phase (S_{LED1_amb}): When this signal is high, the amplifier output corresponds to the LED1 off-time and can be used to estimate the ambient signal (for the LED1 phase). The amplifier output is filtered and sampled into capacitor C_{LED1_amb}.

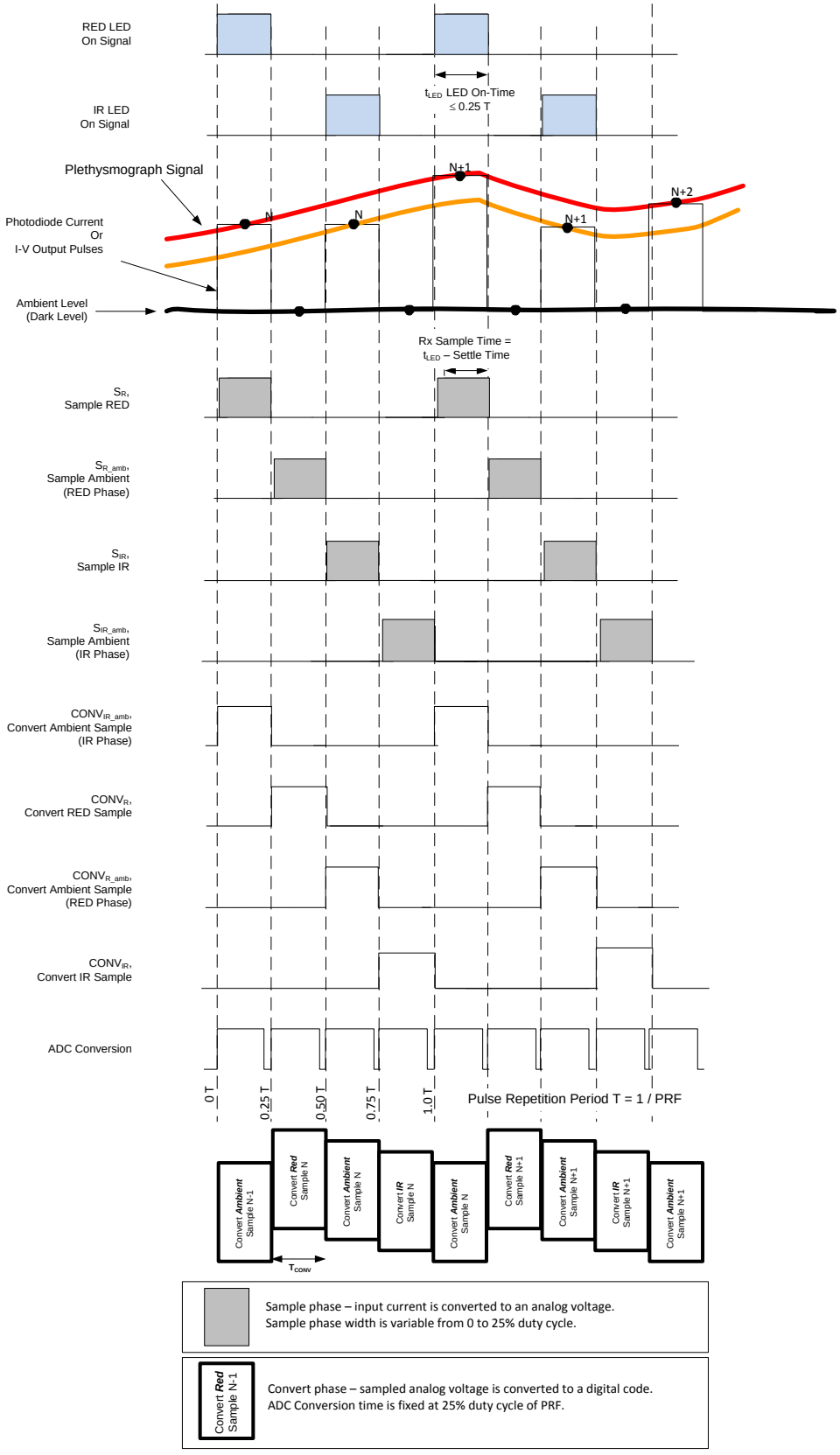
LED2 convert phase ($CONV_{LED2}$): When this signal is high, the voltage sampled on C_{LED2} is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the LED2 sample.

Ambient convert phases ($CONV_{LED2\_amb}$, $CONV_{LED1\_amb}$): When this signal is high, the voltage sampled on C_{LED2_amb} (or C_{LED1_amb}) is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the ambient sample.

LED1 convert phase ($CONV_{LED1}$): When this signal is high, the voltage sampled on C_{LED1} is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the LED1 sample.

8.3.1.4 Receiver Timing

See Figure 58 for a timing diagram detailing the control signals related to the LED on-time, Rx sample time, and the ADC conversion times for each channel.



NOTE: Relationship to the AFE4490EVM is: LED1 = IR and LED2 = RED.

Figure 58. Rx Timing Diagram

8.3.2 Clocking and Timing Signal Generation

The crystal oscillator generates a master clock signal using an external 8-MHz crystal. A divide-by-2 block converts the 8-MHz clock to 4 MHz, which is used by the AFE to operate the timer modules, ADC, and diagnostics. The 4-MHz clock is buffered and output from the AFE in order to clock an external microcontroller. The clocking functionality is shown in Figure 59.

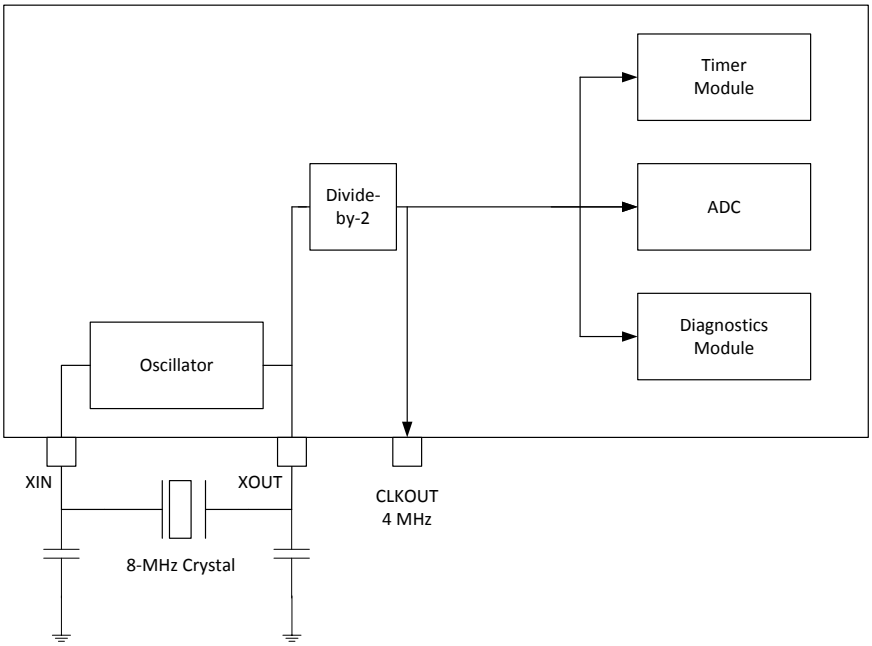
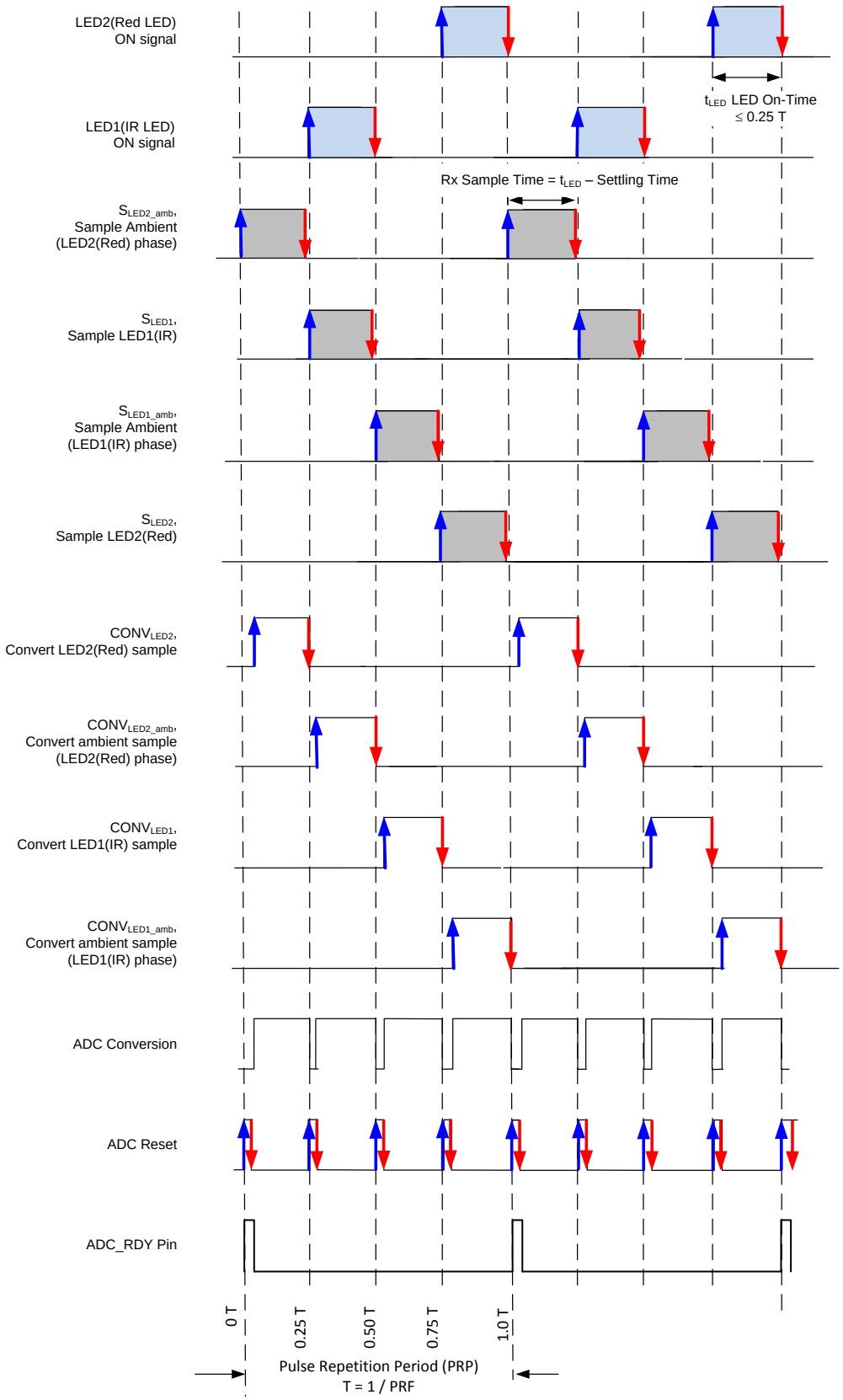


Figure 59. AFE Clocking

8.3.3 Timer Module

See Figure 60 for a timing diagram detailing the various timing edges that are programmable using the timer module. The rising and falling edge positions of 11 signals can be controlled. The module uses a single 16-bit counter (running off of the 4-MHz clock) to set the time-base.

All timing signals are set with reference to the pulse repetition period (PRP). Therefore, a dedicated compare register compares the 16-bit counter value with the reference value specified in the PRF register. Every time that the 16-bit counter value is equal to the reference value in the PRF register, the counter is reset to '0'.



NOTE: Programmable edges are shown in blue and red.

Figure 60. AFE Control Signals

For the 11 signals in Figure 58, the start and stop edge positions are programmable with respect to the PRF period. Each signal uses a separate timer compare module that compares the counter value with preprogrammed reference values for the start and stop edges. All reference values can be set using the SPI interface.

When the counter value equals the start reference value, the output signal is set. When the counter value equals the stop reference value, the output signal is reset. Figure 61 shows a diagram of the timer compare register. With a 4-MHz clock, the edge placement resolution is 0.25 µs. The ADC conversion signal requires four pulses in each PRF clock period. The 11th timer compare register uses four sets of start and stop registers to control the ADC conversion signal.

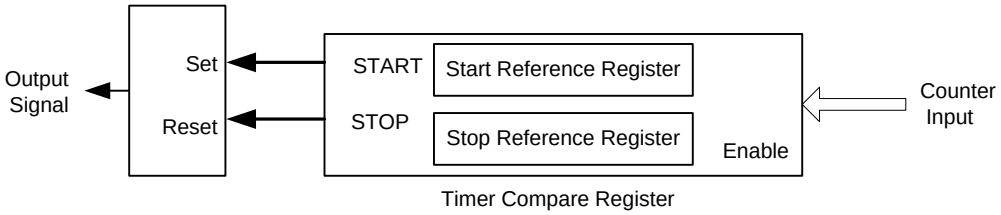


Figure 61. Compare Register

The ADC conversion signal requires four pulses in each PRF clock period. Timer compare register 11 uses four sets of start and stop registers to control the ADC conversion signal, as shown in Figure 62.

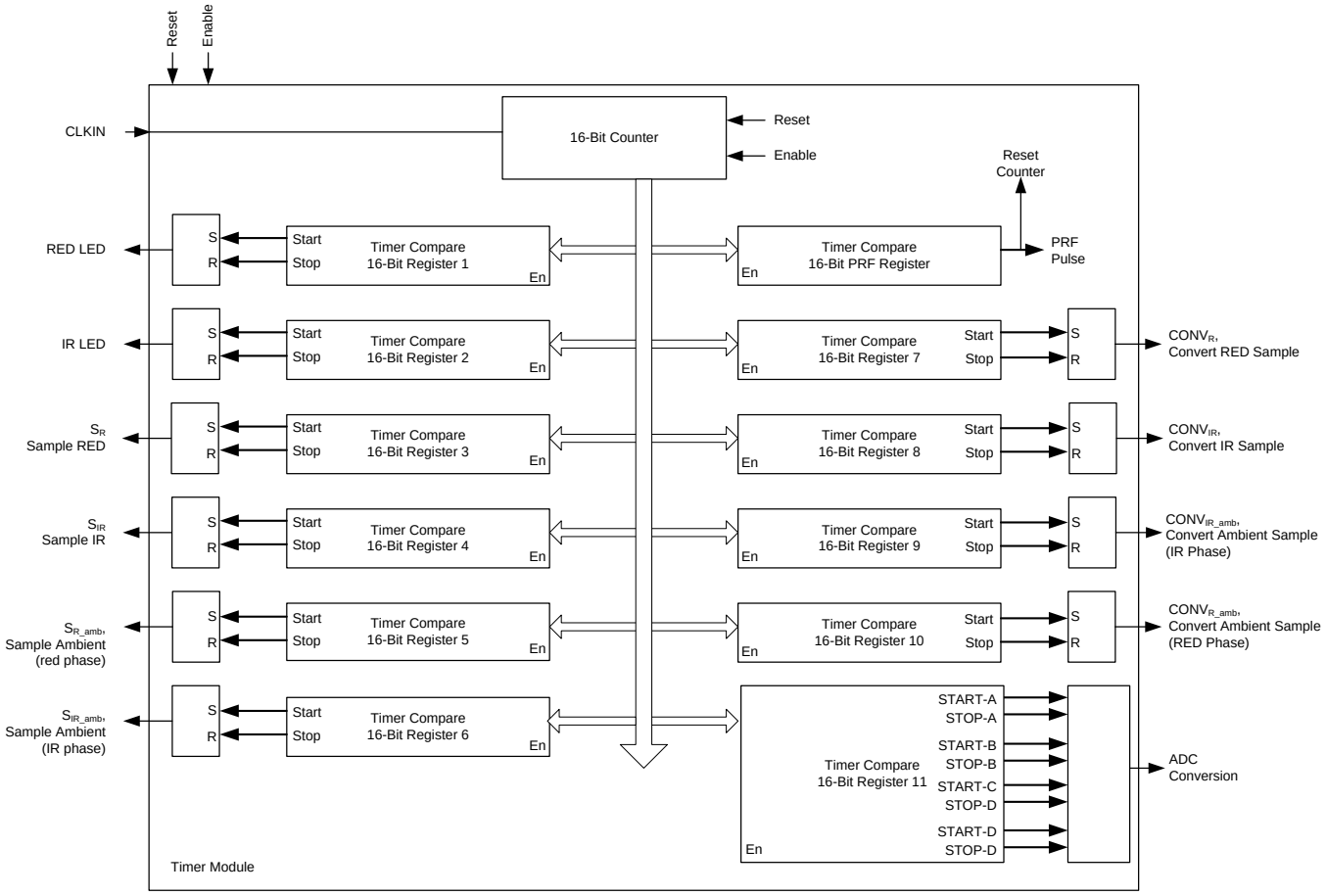


Figure 62. Timer Module

8.3.3.1 Using the Timer Module

The timer module registers can be used to program the start and end instants in units of 4-MHz clock cycles. These timing instants and the corresponding registers are listed in Table 2.

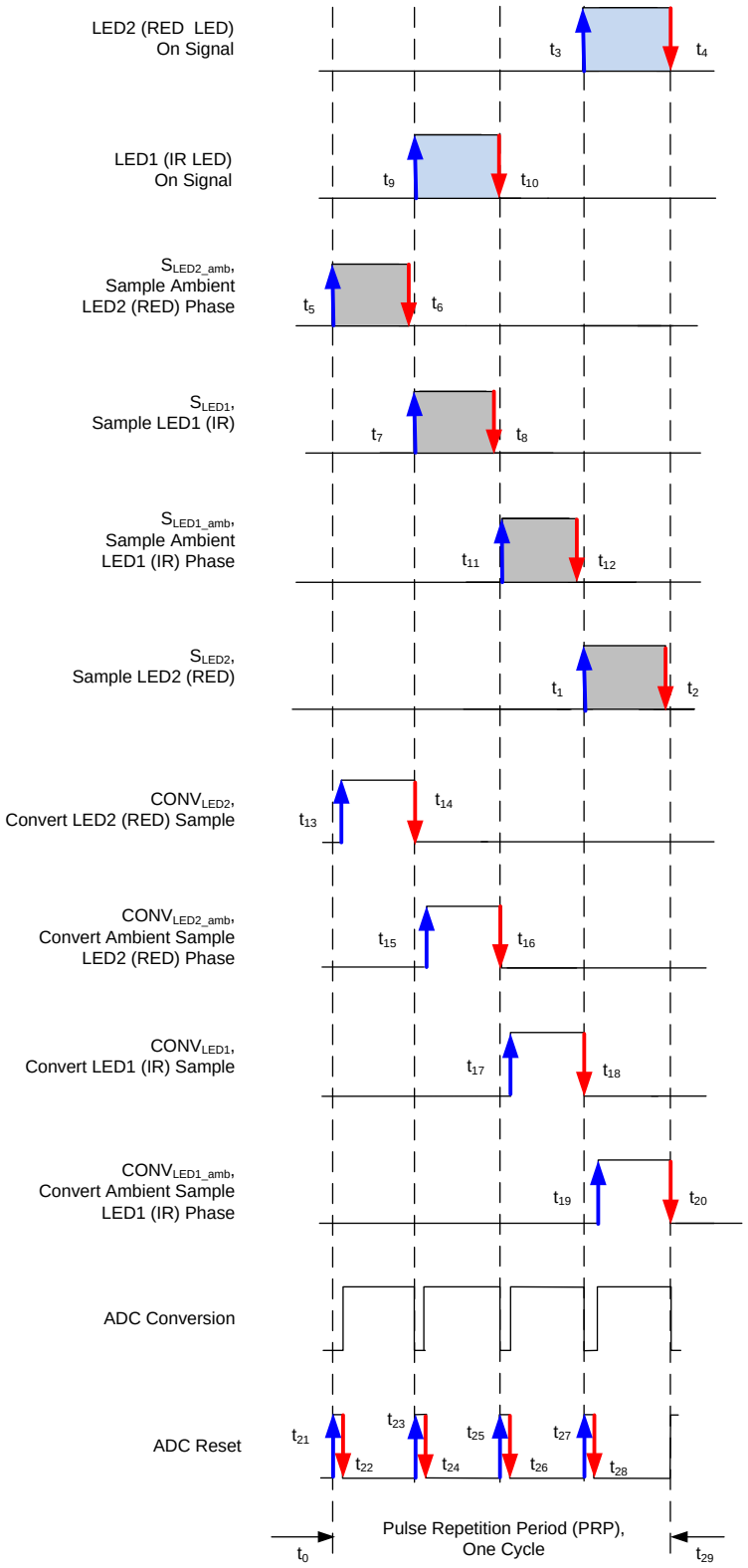
Note that the device does not restrict the values in these registers; thus, the start and end edges can be positioned anywhere within the pulse repetition period. Care must be taken by the user to program suitable values in these registers to avoid overlapping the signals and to make sure none of the edges exceed the value programmed in the PRP register. Writing the same value in the start and end registers results in a pulse duration of one clock cycle. The following steps describe the timer sequencing configuration:

1. With respect to the start of the PRP period (indicated by timing instant t_0 in Figure 63 and Figure 64), the sequence of conversions must be followed in order: convert LED2 → LED2 ambient → LED1 → LED1 ambient.
2. Also, starting from t_0, the sequence of sampling instants must be staggered with respect to the respective conversions as follows: sample LED2 ambient → LED1 → LED1 ambient → LED2.
3. Finally, align the edges for the two LED pulses with the respective sampling instants.

Table 2. Clock Edge Mapping to SPI Registers

TIME INSTANT (See Figure 63 and Figure 64)	DESCRIPTION	CORRESPONDING REGISTER ADDRESS AND REGISTER BITS	EXAMPLE(1) (Decimal)
t_0	Start of pulse repetition period	No register control	—
t_1	Start of sample LED2 pulse	Sample LED2 start count (bits 15-0 of register 01h)	6050
t_2	End of sample LED2 pulse	Sample LED2 end count (bits 15-0 of register 02h)	7998
t_3	Start of LED2 pulse	LED2 start count (bits 15-0 of register 03h)	6000
t_4	End of LED2 pulse	LED2 end count (bits 15-0 of register 04h)	7999
t_5	Start of sample LED2 ambient pulse	Sample ambient LED2 start count (bits 15-0 of register 05h)	50
t_6	End of sample LED2 ambient pulse	Sample ambient LED2 end count (bits 15-0 of register 06h)	1998
t_7	Start of sample LED1 pulse	Sample LED1 start count (bits 15-0 of register 07h)	2050
t_8	End of sample LED1 pulse	Sample LED1 end count (bits 15-0 of register 08h)	3998
t_9	Start of LED1 pulse	LED1 start count (bits 15-0 of register 09h)	2000
t_{10}	End of LED1 pulse	LED1 end count (bits 15-0 of register 0Ah)	3999
t_{11}	Start of sample LED1 ambient pulse	Sample ambient LED1 start count (bits 15-0 of register 0Bh)	4050
t_{12}	End of sample LED1 ambient pulse	Sample ambient LED1 end count (bits 15-0 of register 0Ch)	5998
t_{13}	Start of convert LED2 pulse	LED2 convert start count (bits 15-0 of register 0Dh) Must start one AFE clock cycle after the ADC reset pulse ends.	4
t_{14}	End of convert LED2 pulse	LED2 convert end count (bits 15-0 of register 0Eh)	1999
t_{15}	Start of convert LED2 ambient pulse	LED2 ambient convert start count (bits 15-0 of register 0Fh) Must start one AFE clock cycle after the ADC reset pulse ends.	2004
t_{16}	End of convert LED2 ambient pulse	LED2 ambient convert end count (bits 15-0 of register 10h)	3999
t_{17}	Start of convert LED1 pulse	LED1 convert start count (bits 15-0 of register 11h) Must start one AFE clock cycle after the ADC reset pulse ends.	4004
t_{18}	End of convert LED1 pulse	LED1 convert end count (bits 15-0 of register 12h)	5999
t_{19}	Start of convert LED1 ambient pulse	LED1 ambient convert start count (bits 15-0 of register 13h) Must start one AFE clock cycle after the ADC reset pulse ends.	6004
t_{20}	End of convert LED1 ambient pulse	LED1 ambient convert end count (bits 15-0 of register 14h)	7999
t_{21}	Start of first ADC conversion reset pulse	ADC reset 0 start count (bits 15-0 of register 15h)	0
t_{22}	End of first ADC conversion reset pulse(2)	ADC reset 0 end count (bits 15-0 of register 16h)	3
t_{23}	Start of second ADC conversion reset pulse	ADC reset 1 start count (bits 15-0 of register 17h)	2000
t_{24}	End of second ADC conversion reset pulse(2)	ADC reset 1 end count (bits 15-0 of register 18h)	2003
t_{25}	Start of third ADC conversion reset pulse	ADC reset 2 start count (bits 15-0 of register 19h)	4000
t_{26}	End of third ADC conversion reset pulse(2)	ADC reset 2 end count (bits 15-0 of register 1Ah)	4003
t_{27}	Start of fourth ADC conversion reset pulse	ADC reset 3 start count (bits 15-0 of register 1Bh)	6000
t_{28}	End of fourth ADC conversion reset pulse(2)	ADC reset 3 end count (bits 15-0 of register 1Ch)	6003
t_{29}	End of pulse repetition period	Pulse repetition period count (bits 15-0 of register 1Dh)	7999

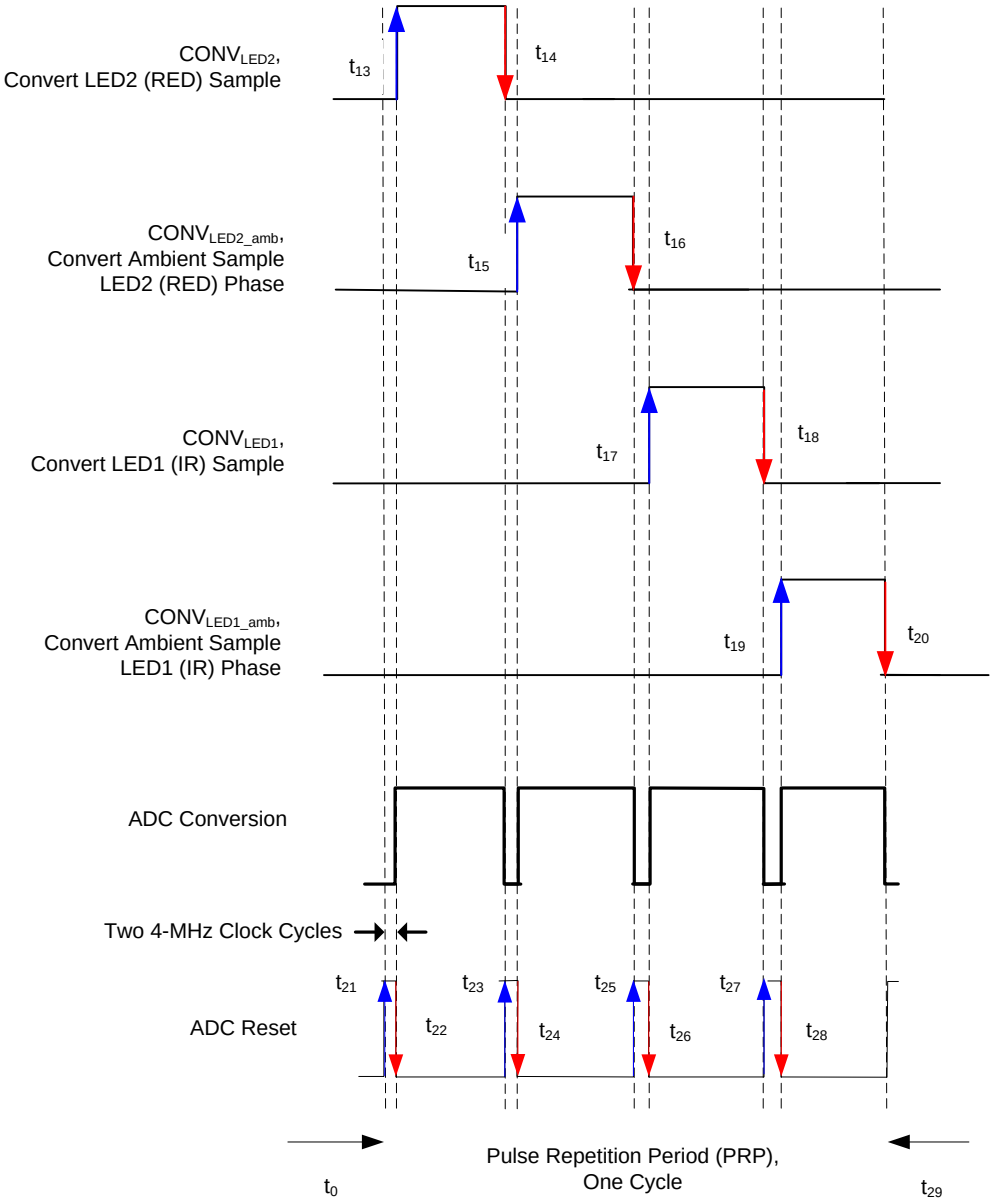
(1) Values are based off of a pulse repetition frequency (PRF) = 500 Hz and duty cycle = 25%.
(2) See Figure 64, note 2 for the affect of the ADC reset time crosstalk.



(1) RED = LED2, IR = LED1.

(2) A low ADC reset time can result in a small component of the LED signal leaking into the ambient phase. With an ADC reset of two clock cycles, a –60-dB leakage is expected. In many cases, this leakage does not affect system performance. However, if this crosstalk must be completely eliminated, a longer ADC reset time of approximately six clock cycles is recommended for t_{22}, t_{24}, t_{26}, and t_{28}.

Figure 63. Programmable Clock Edges(1)(2)



(1) RED = LED2, IR = LED1.

(2) A low ADC reset time can result in a small component of the LED signal leaking into the ambient phase. With an ADC reset of two clock cycles, a –60-dB leakage is expected. In many cases, this leakage does not affect system performance. However, if this crosstalk must be completely eliminated, a longer ADC reset time of approximately six clock cycles is recommended for t_{22}, t_{24}, t_{26}, and t_{28}.

Figure 64. Relationship Between the ADC Reset and ADC Conversion Signals(1)(2)

8.3.4 Receiver Subsystem Power Path

The block diagram in Figure 65 shows the device Rx subsystem power routing.

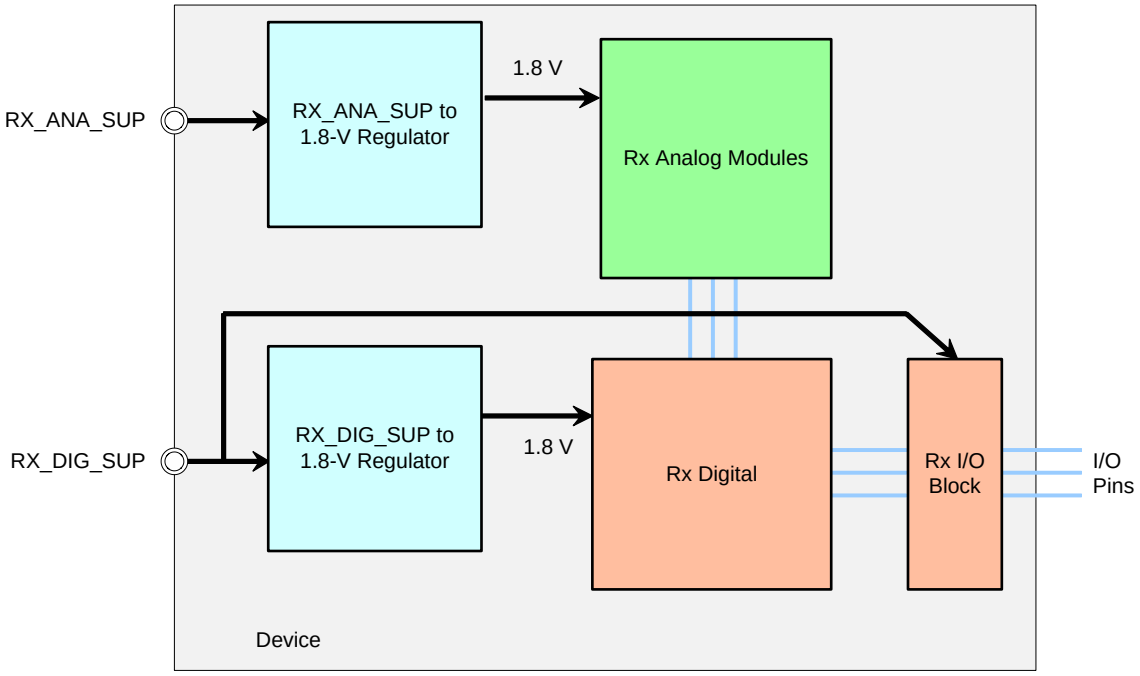


Figure 65. Receive Subsystem Power Routing

8.3.5 Transmit Section

The transmit section integrates the LED driver and the LED current control section with 8-bit resolution. This integration is designed to meet a dynamic range of better than 105 dB (based on a 1-sigma LED current noise).

The RED and IR LED reference currents can be independently set. The current source (I_{LED}) locally regulates and ensures that the actual LED current tracks the specified reference. The transmitter section uses a reference voltage for operation. This reference voltage is available on the REF_TX pin and must be decoupled to ground with a 2.2-µF capacitor. The TX_REF voltage is derived from the TX_CTRL_SUP. The maximum LED current setting depends on the transmitter reference voltage. By default, after reset, this voltage is 0.75 V and supports up to a 150-mA LED current. For higher LED currents up to 200 mA, the reference can be programmed to 1.0 V (using the LED_RANGE[1:0] register bits).

The minimum LED_DRV_SUP voltage required for operation depends on the:

- Voltage drop across the LED (V_{LED}),
- Voltage drop across the external cable, connector, and any other component in series with the LED (V_{CABLE}), and
- Transmitter reference voltage.

Using the default reference voltage of 0.75 V, the minimum LED_DRV_SUP voltage can be as low as 3.25 V, provided that Equation 3 is met. Refer to the *Recommended Operating Conditions* table.

$$3.25\ V - (V_{LED} + V_{CABLE}) > 1.4\ V \quad (3)$$

To lower the minimum LED_DRV_SUP voltage even further, the transmitter reference voltage can be programmed to 0.5 V. By doing so, the minimum LED_DRV_SUP voltage can be reduced to 3.0 V, provided that Equation 4 is met. Refer to the *Recommended Operating Conditions* table.

$$3.0\ V - (V_{LED} + V_{CABLE}) > 1.4\ V \quad (4)$$

Note that with the 0.5-V transmitter reference voltage, the maximum LED current supported is 100 mA.

Two LED driver schemes are supported:

- An H-bridge drive for a two-pin, back-to-back LED package, as shown in Figure 66.
- A push-pull drive for a three-pin, common-anode LED package; see Figure 67.

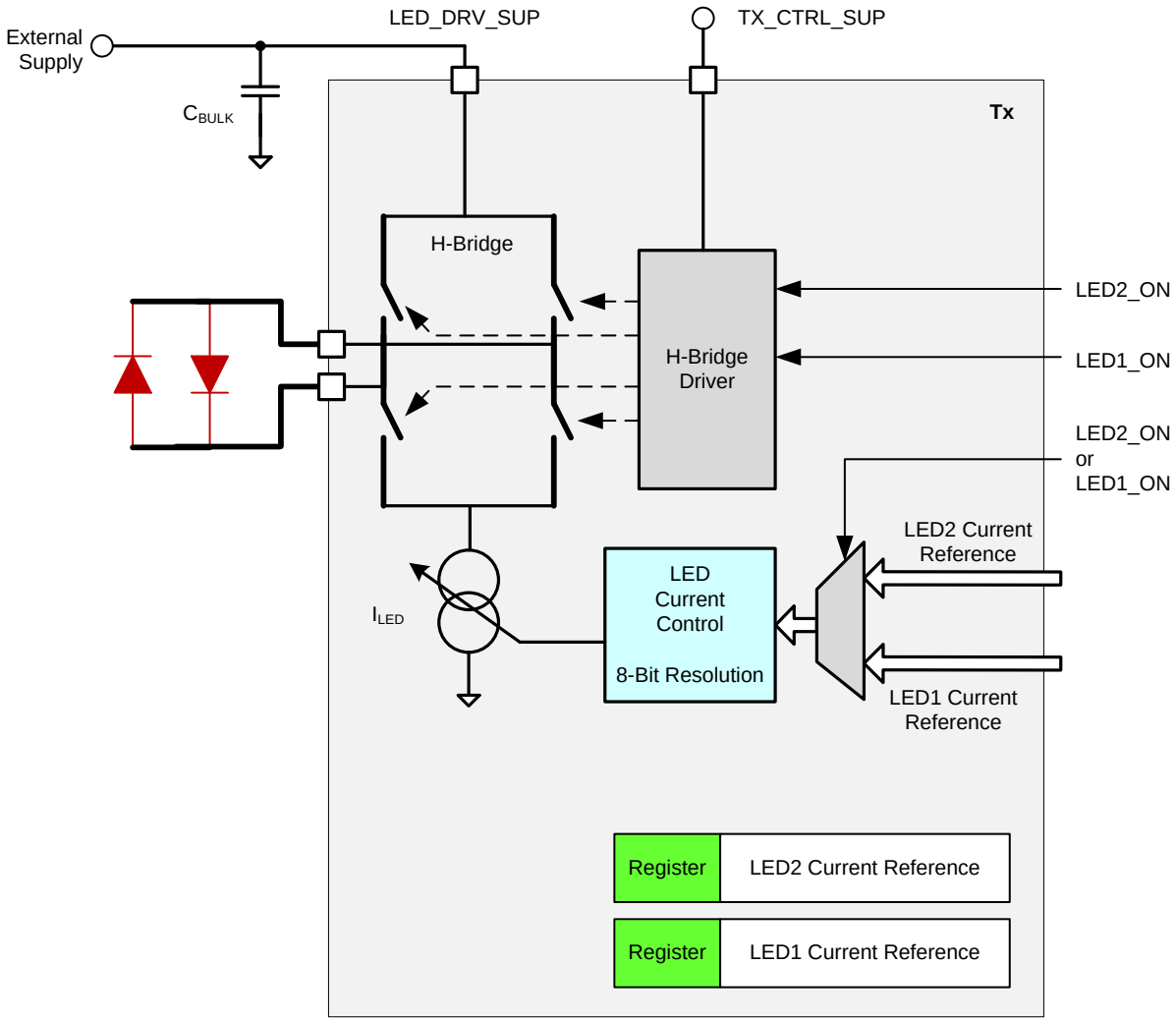


Figure 66. Transmit: H-Bridge Drive

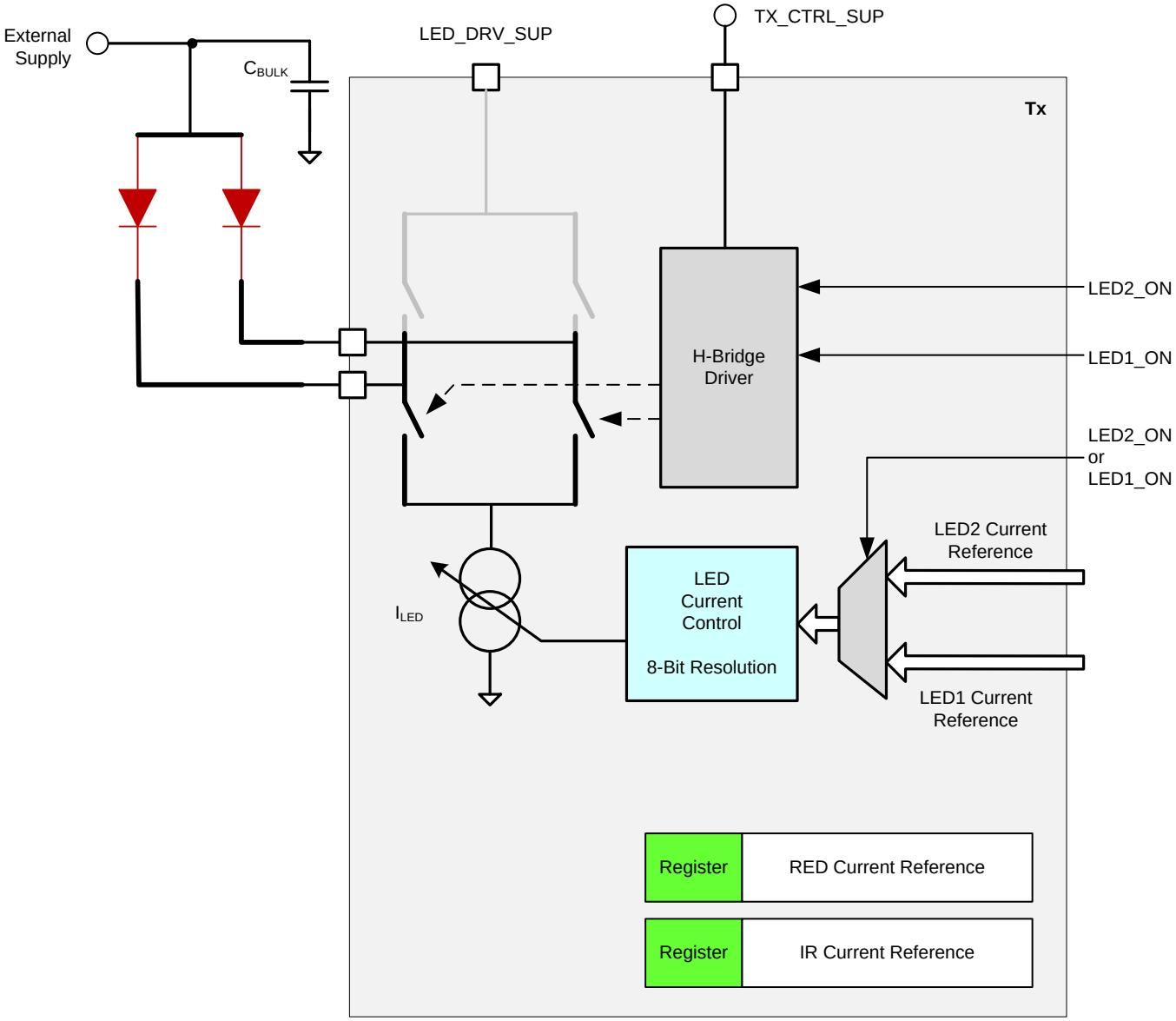


Figure 67. Transmit: Push-Pull LED Drive for Common Anode LED Configuration

8.3.5.1 Transmitter Power Path

The block diagram in Figure 68 shows the device Tx subsystem power routing.

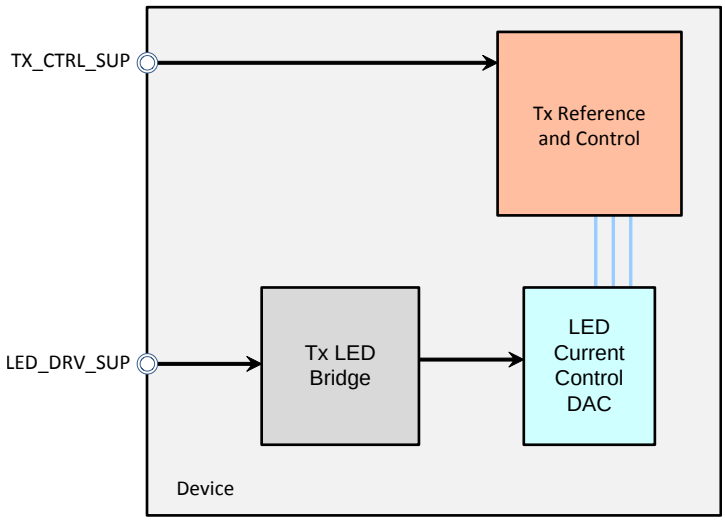


Figure 68. Transmit Subsystem Power Routing

8.3.5.2 LED Power Reduction During Periods of Inactivity

The diagram in Figure 69 shows how LED bias current passes 50 µA whenever LED_ON occurs. In order to minimize power consumption in periods of inactivity, the LED_ON control must be turned off. Furthermore, disable the TIMEREN bit in the CONTROL1 register by setting the value to '0'.

Note that depending on the LEDs used, the LED may sometimes appear dimly lit even when the LED current is set to 0 mA. This appearance is because of the switching leakage currents (as shown in Figure 69) inherent to the timer function. The dimmed appearance does not effect the ambient light level measurement because during the ambient cycle, LED_ON is turned off for the duration of the ambient measurement.

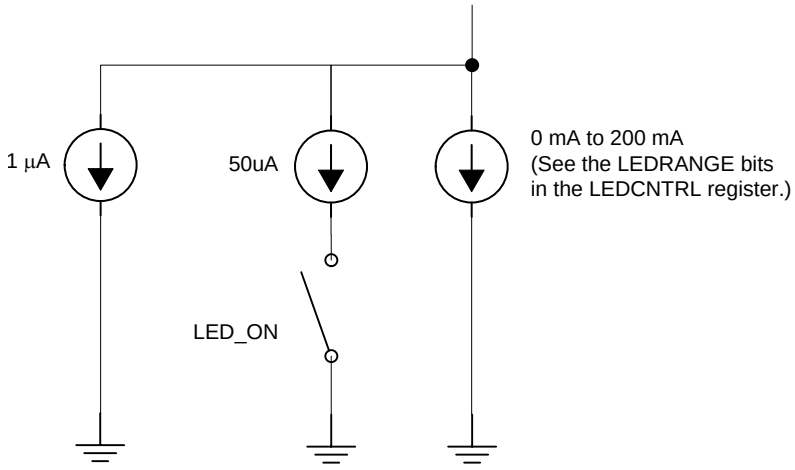


Figure 69. LED Bias Current

8.4 Device Functional Modes

8.4.1 ADC Operation and Averaging Module

After the falling edge of the ADC reset signal, the ADC conversion phase starts (refer to Figure 64). Each ADC conversion takes 50 µs.

There are two modes of operation: without averaging and with averaging. The averaging mode can average multiple ADC samples and reduce noise to improve dynamic range because the ADC conversion time is usually shorter than 25% of the pulse repetition period. Figure 70 shows a diagram of the averaging module. The ADC output format is in 22-bit twos complement. The two MSB bits of the 24-bit data can be ignored.

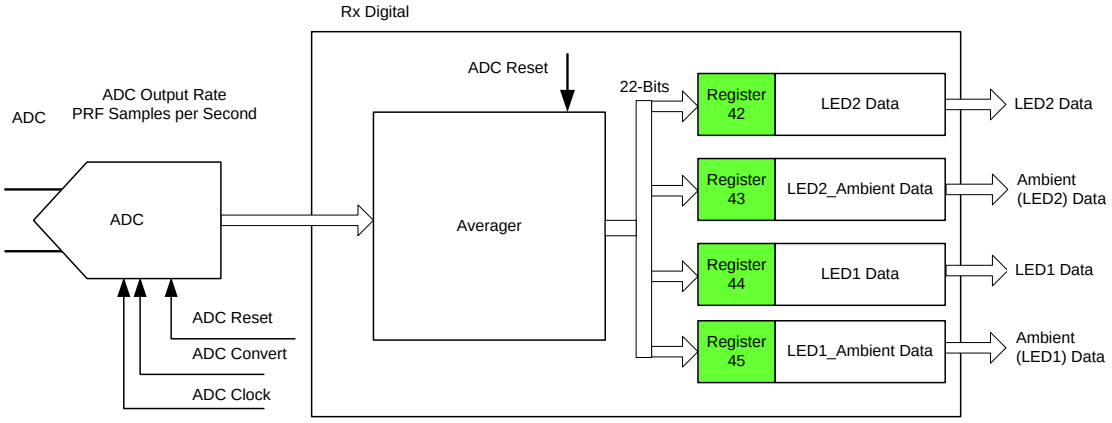


Figure 70. Averaging Module

8.4.1.1 Operation Without Averaging

In this mode, the ADC outputs a digital sample one time for every 50 µs. At the next rising edge of the ADC reset signal, the first 22-bit conversion value is written into the result registers sequentially as follows (see Figure 71):

- At the 25% reset signal, the first 22-bit ADC sample is written to register 2Ah.
- At the 50% reset signal, the first 22-bit ADC sample is written to register 2Bh.
- At the 75% reset signal, the first 22-bit ADC sample is written to register 2Ch.
- At the next 0% reset signal, the first 22-bit ADC sample is written to register 2Dh. The contents of registers 2Ah and 2Bh are written to register 2Eh and the contents of registers 2Ch and 2Dh are written to register 2Fh.

At the rising edge of the ADC_RDY signal, the contents of all six result registers can be read out.

8.4.1.2 Operation With Averaging

In this mode, all ADC digital samples are accumulated and averaged after every 50 µs. At the next rising edge of the ADC reset signal, the average value (22-bit) is written into the output registers sequentially as follows (see Figure 72):

- At the 25% reset signal, the averaged 22-bit word is written to register 2Ah.
- At the 50% reset signal, the averaged 22-bit word is written to register 2Bh.
- At the 75% reset signal, the averaged 22-bit word is written to register 2Ch.
- At the next 0% reset signal, the averaged 22-bit word is written to register 2Dh. The contents of registers 2Ah and 2Bh are written to register 2Eh and the contents of registers 2Ch and 2Dh are written to register 2Fh.

At the rising edge of the ADC_RDY signal, the contents of all six result registers can be read out.

Device Functional Modes (continued)

The number of samples to be used per conversion phase is specified in the CONTROL1 register (NUMAV[7:0]). The user must specify the correct value for the number of averages, as described in Equation 5:

$$\text{NUMAV[7:0]} + 1 = \left(\frac{0.25 \times \text{Pulse Repetition Period}}{50\ \mu\text{s}} \right) - 1 \quad (5)$$

When the number of averages is '0', the averaging is disabled and only one ADC sample is written to the result registers.

Note that he number of average conversions is limited by 25% of the PRF. For example, eight samples can be averaged with PRF = 625 Hz, and four samples can be averaged with PRF = 1250 Hz.

Device Functional Modes (continued)

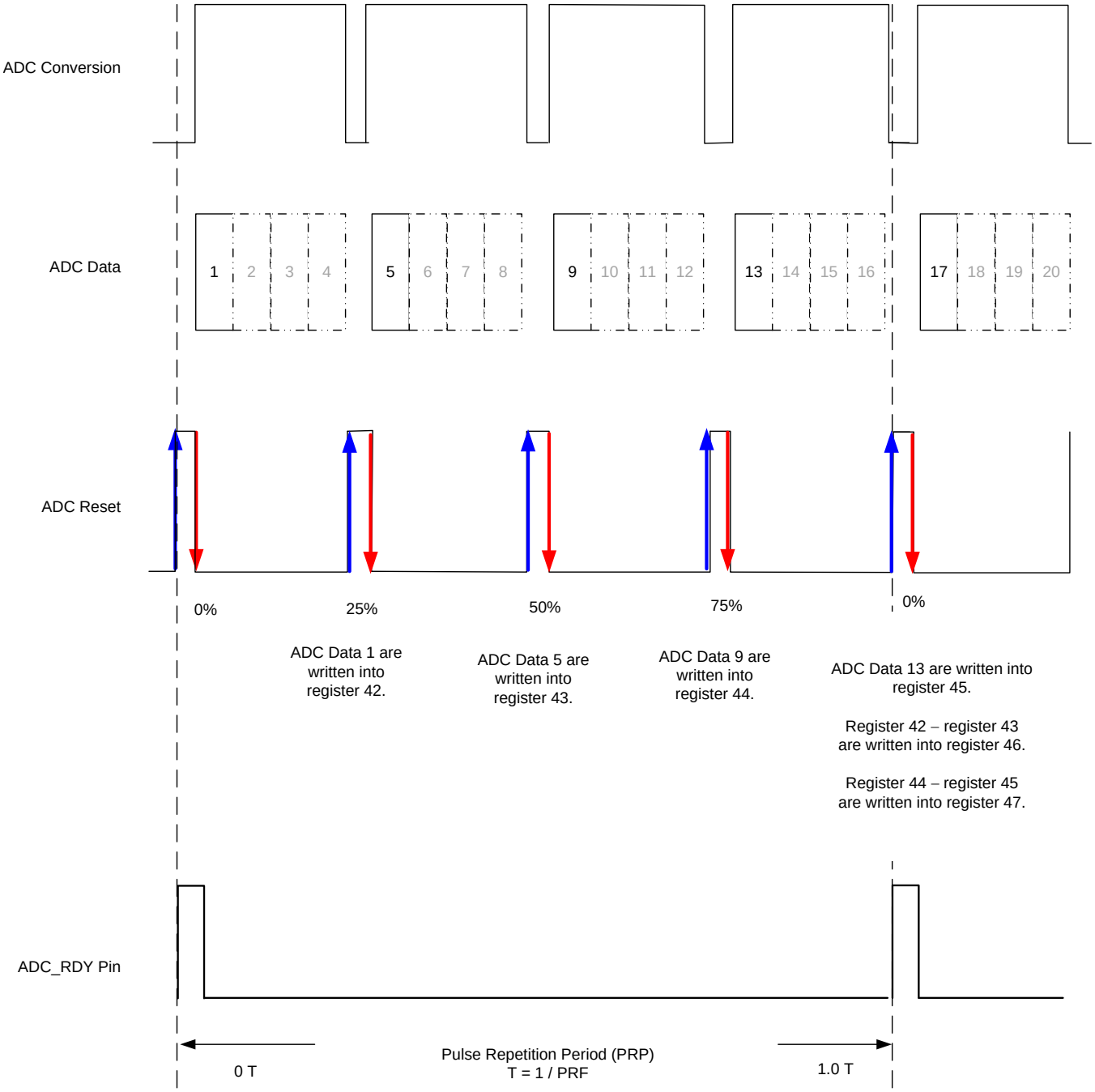
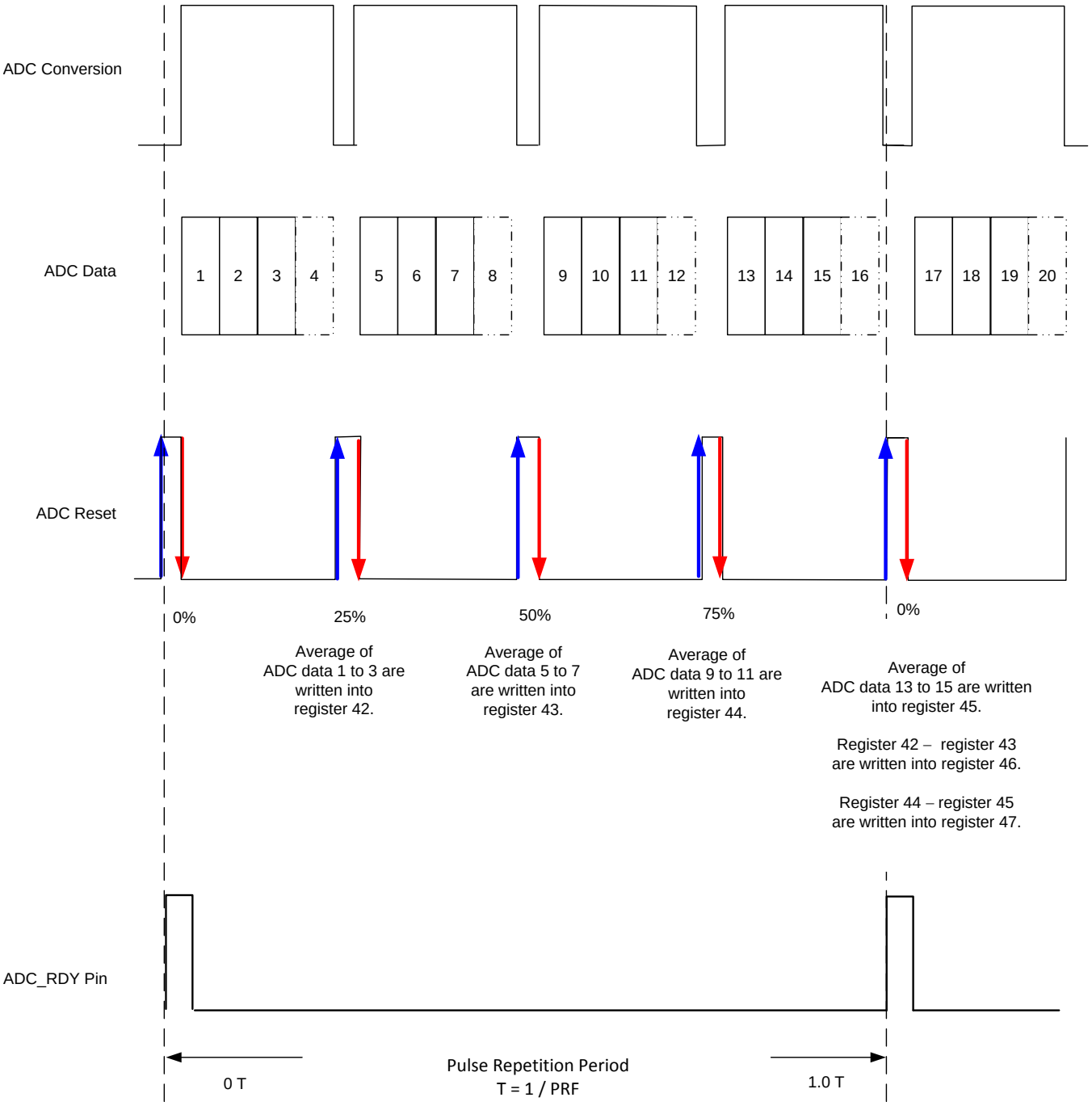


Figure 71. ADC Data without Averaging (when Number of Averages = 0)

Device Functional Modes (continued)



NOTE: Example is with three averages. The value of the NUMAVG[7:0] register bits = 2.

Figure 72. ADC Data with Averaging Enabled

Device Functional Modes (continued)

8.4.2 AFE Analog Output Mode (ADC Bypass Mode)

This mode is only intended for use in system debug. Note that this function is not recommended for production use because of the minimal device production testing performed on this function.

The ADC bypass mode brings out the analog output voltage of the receiver front-end on two pins (RXOUTP, RXOUTN), around a common-mode voltage of approximately 0.9 V. In this mode, the internal ADC of the AFE4490 is disabled. Figure 73 shows a block diagram of this mode.

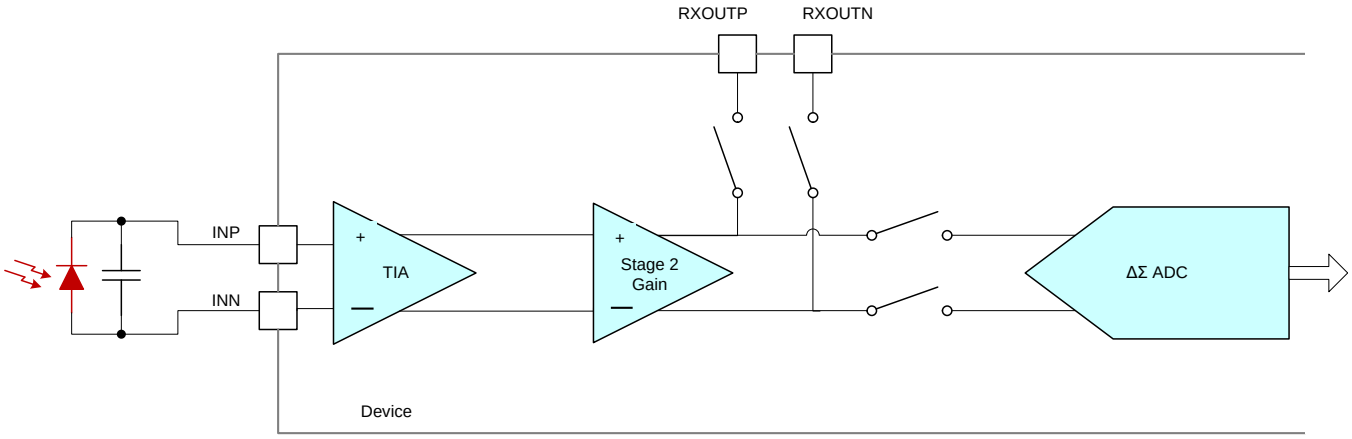


Figure 73. Device Set to ADC Bypass Mode

In ADC bypass mode, one of the internal clocks (ADC_Reset) can be brought out on the PD_ALM pin, as shown in Figure 74. This signal can be used to convert each of the four phases (within every pulse repetition period). Additionally, the ADC_RDY signal can be used to synchronize the external ADC with the AFE. See Figure 75 for the timing of this mode.

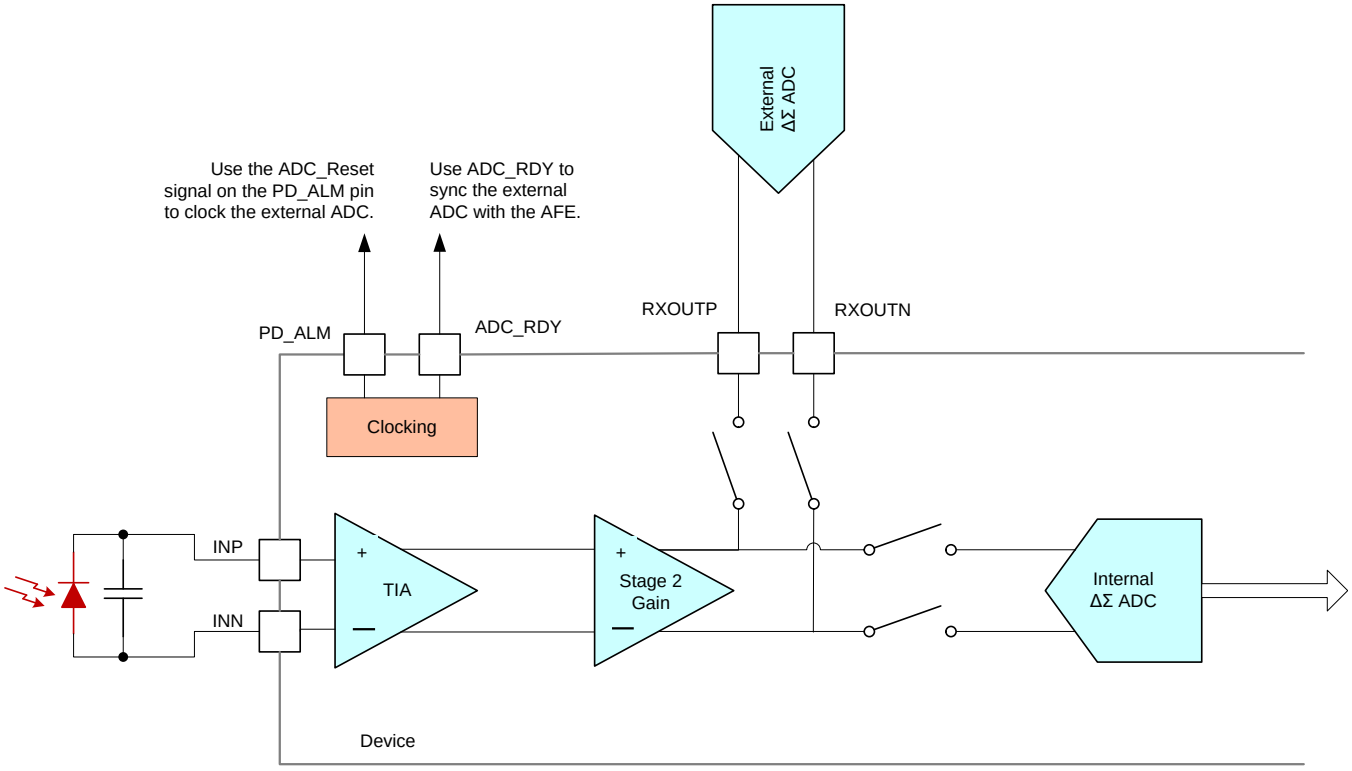
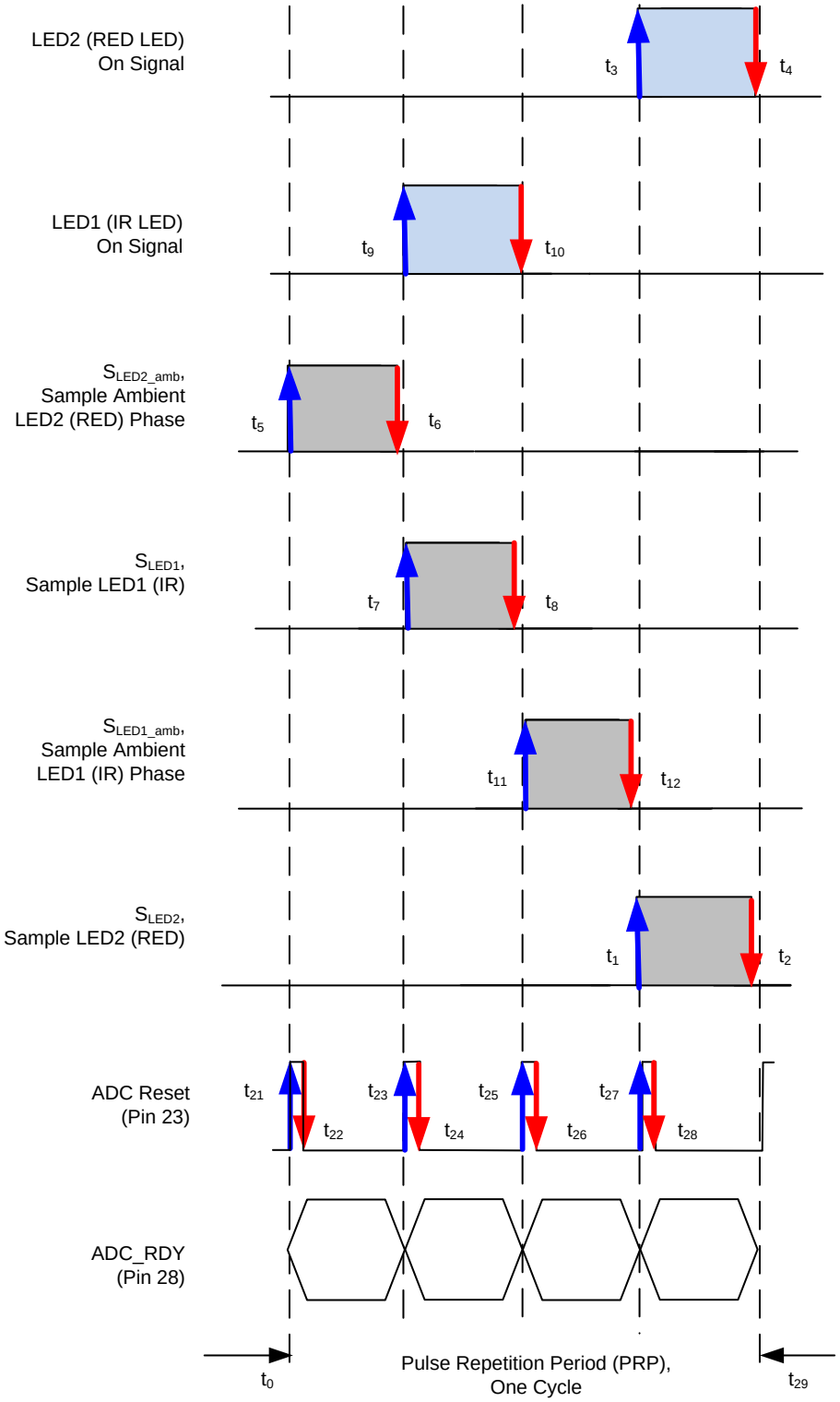


Figure 74. Device in ADC Bypass Mode with ADC_Reset to PD_ALM Pin

Device Functional Modes (continued)



NOTE: RED = LED2, IR = LED1.

Figure 75. Device Analog Output Mode (ADC Bypass) Timing Diagram

Device Functional Modes (continued)

In ADC bypass mode, the ADC reset signal can be used to start conversions with the external ADC. Use registers 15h through 1Ch to position the ADC reset signal edges appropriately. Also, use the CLKALMPIN[2:0] bits on the PD_ALM pin register bit to bring out the ADC reset signal to the PD_ALM pin. ADC_RDY can be used to indicate the start of the pulse repetition period to the external ADC.

8.4.3 Diagnostics

The device includes diagnostics to detect open or short conditions of the LED and photosensor, LED current profile feedback, and cable on or off detection.

8.4.3.1 Photodiode-Side Fault Detection

Figure 76 shows the diagnostic for the photodiode-side fault detection.

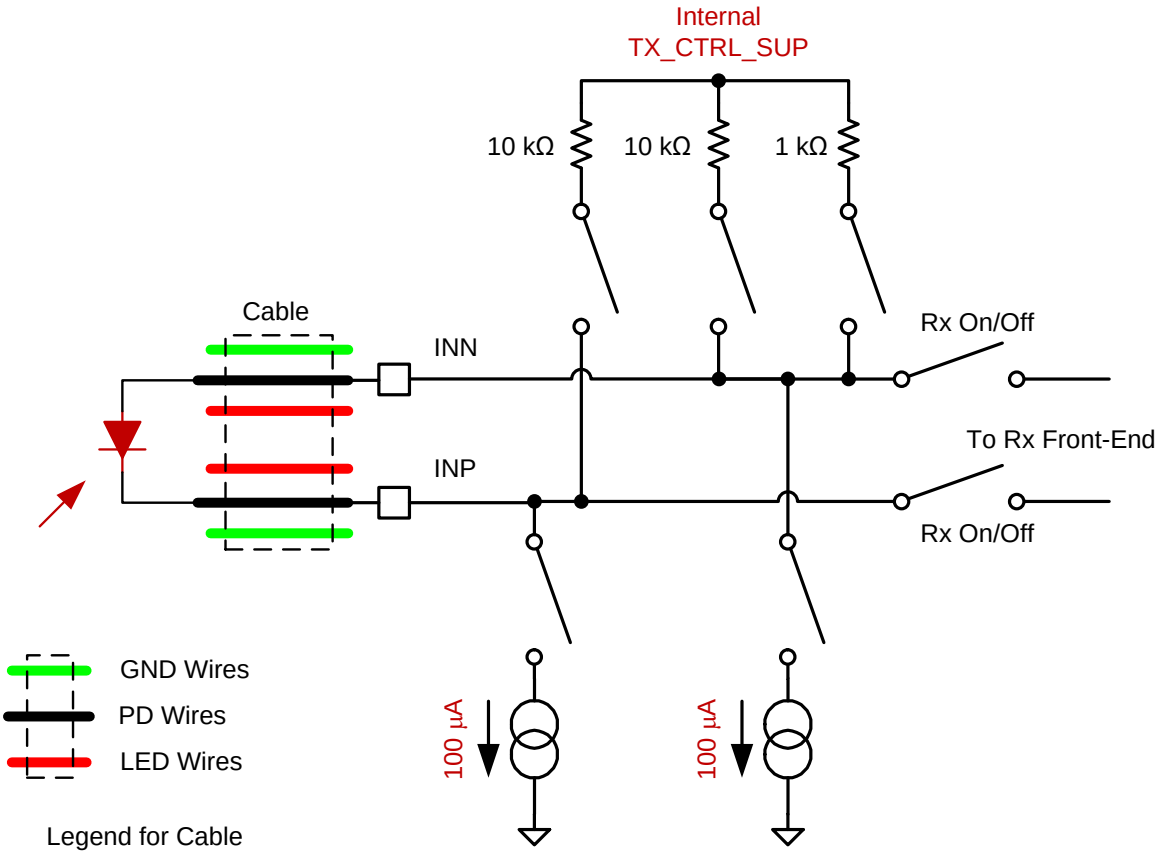


Figure 76. Photodiode Diagnostic

Device Functional Modes (continued)

8.4.3.2 Transmitter-Side Fault Detection

Figure 77 shows the diagnostic for the transmitter-side fault detection.

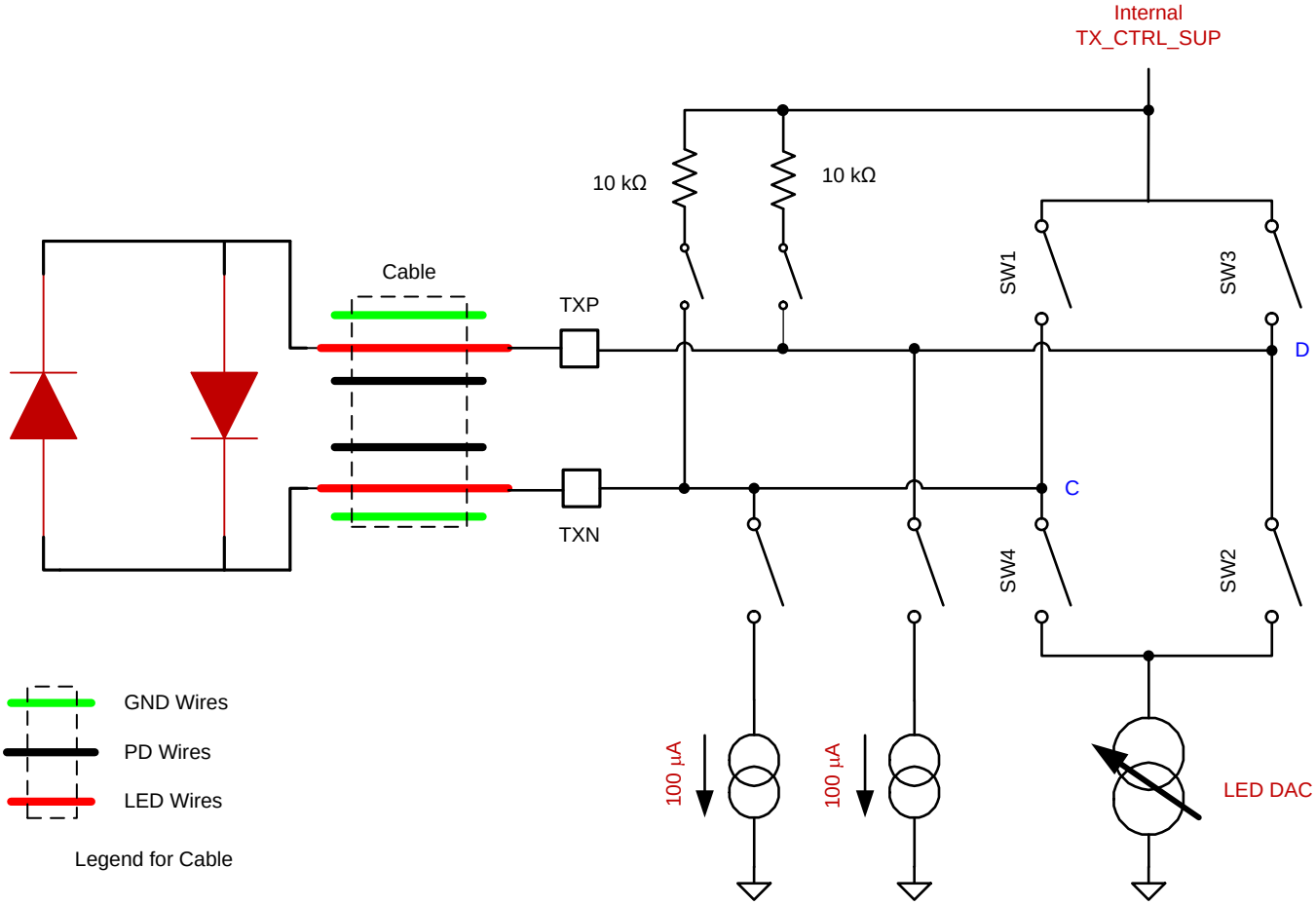


Figure 77. Transmitter Diagnostic

Device Functional Modes (continued)

8.4.3.3 Diagnostics Module

The diagnostics module, when enabled, checks for nine types of faults sequentially. The results of all faults are latched in 11 separate flags. At the end of the sequence, the state of the 11 flags are combined to generate two interrupt signals: PD_ALM for photodiode-related faults and LED_ALM for transmit-related faults. The status of all flags can also be read using the SPI interface. Table 3 details each fault and flag used. Note that the diagnostics module requires all AFE blocks to be enabled in order to function reliably.

Table 3. Fault and Flag Diagnostics(1)

MODULE	SEQ.	FAULT	FLAG1	FLAG2	FLAG3	FLAG4	FLAG5	FLAG6	FLAG7	FLAG8	FLAG9	FLAG10	FLAG11
—	—	No fault	0	0	0	0	0	0	0	0	0	0	0
PD	1	Rx INP cable shorted to LED cable	1										
	2	Rx INN cable shorted to LED cable		1									
	3	Rx INP cable shorted to GND cable			1								
	4	Rx INN cable shorted to GND cable				1							
	5	PD open or shorted					1	1					
LED	6	Tx OUTM line shorted to GND cable							1				
	7	Tx OUTP line shorted to GND cable								1			
	8	LED open or shorted									1	1	
	9	LED open or shorted											1

(1) Resistances below 10 kΩ are considered to be shorted.

Figure 78 shows the timing for the diagnostic function.

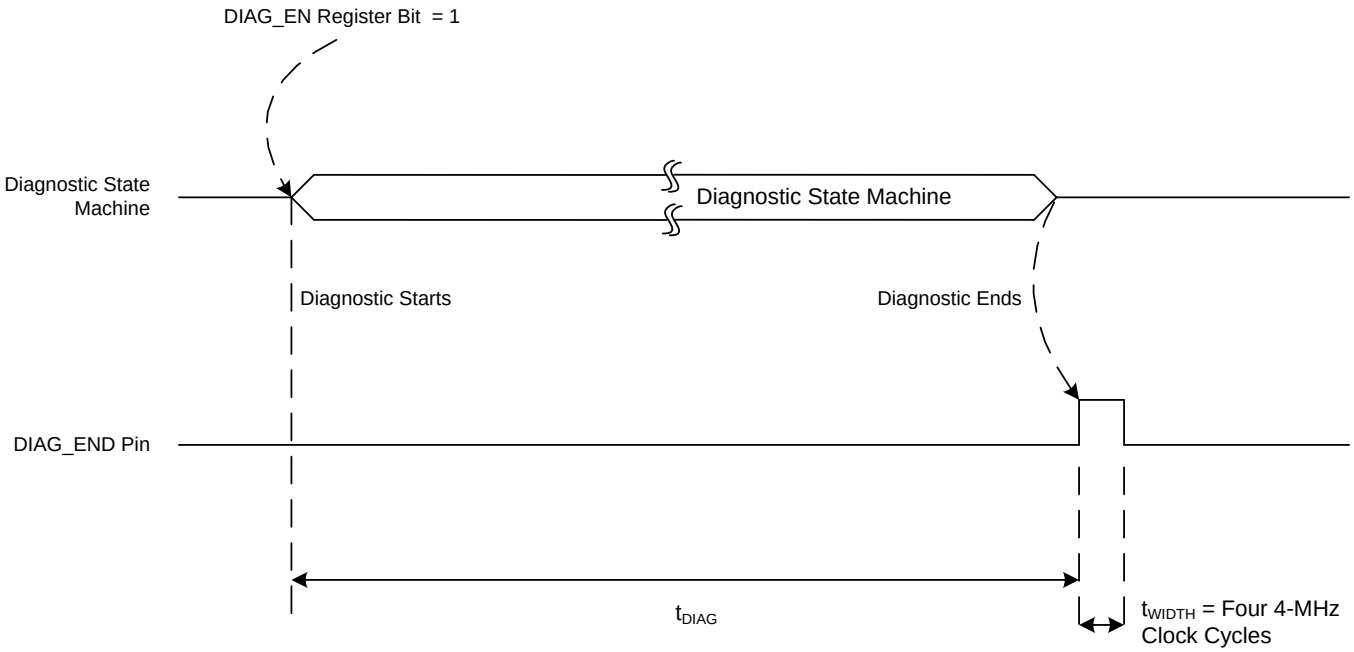


Figure 78. Diagnostic Timing Diagram

By default, the diagnostic function takes t_{DIAG} = 8 ms to complete after the DIAG_EN register bit is enabled. By setting the EN_SLOW_DIAG register bit (CONTROL2 register, bit D8) the diagnostic time can be increased to 16 ms.

After completion of the diagnostics function, time must be allowed for the device filter to settle. See the *Electrical Characteristics* for the filter settling time. The slow diagnostics feature is provided for use in systems where high-capacitance sensors (such as photodiodes, capacitors, cables, and so forth) are connected to the INP, INN, TXP, or TXN pins.

8.5 Programming

8.5.1 Serial Programming Interface

The SPI-compatible serial interface consists of four signals: SCLK (serial clock), SPISOMI (serial interface data output), SPISIMO (serial interface data input), and SPISTE (serial interface enable).

The serial clock (SCLK) is the serial peripheral interface (SPI) serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a Schmitt-triggered input and clocks data out on SPISOMI. Data are clocked in on the SPISIMO pin. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low.

The SPISOMI (SPI serial out master in) pin is used with SCLK to clock out device data. The SPISIMO (SPI serial in master out) pin is used with SCLK to clock in data to the device. The SPISTE (SPI serial interface enable) pin enables the serial interface to clock data on the SPISIMO pin in to the device.

8.5.2 Reading and Writing Data

The device has a set of internal registers that can be accessed by the serial programming interface formed by the SPISTE, SCLK, SPISIMO, and SPISOMI pins.

8.5.2.1 Writing Data

The SPI_READ register bit must be first set to '0' before writing to a register. When SPISTE is low,

- Serially shifting bits into the device is enabled.
- Serial data (on the SPISIMO pin) are latched at every SCLK rising edge.
- The serial data are loaded into the register at every 32nd SCLK rising edge.

In case the word length exceeds a multiple of 32 bits, the excess bits are ignored. Data can be loaded in multiples of 32-bit words within a single active SPISTE pulse. The first eight bits form the register address and the remaining 24 bits form the register data. Figure 79 shows an SPI timing diagram for a single write operation. For multiple read and write cycles, refer to the *Multiple Data Reads and Writes* section.

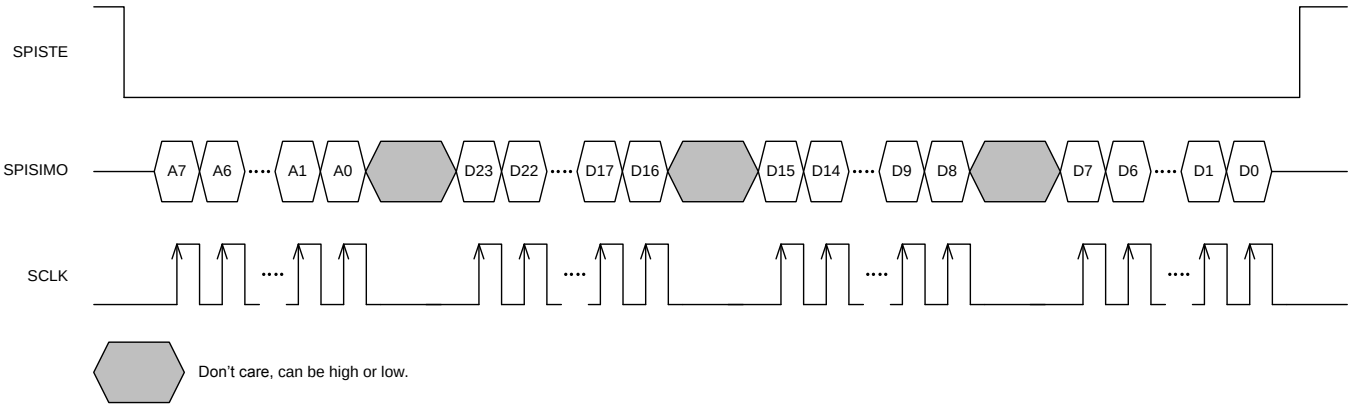
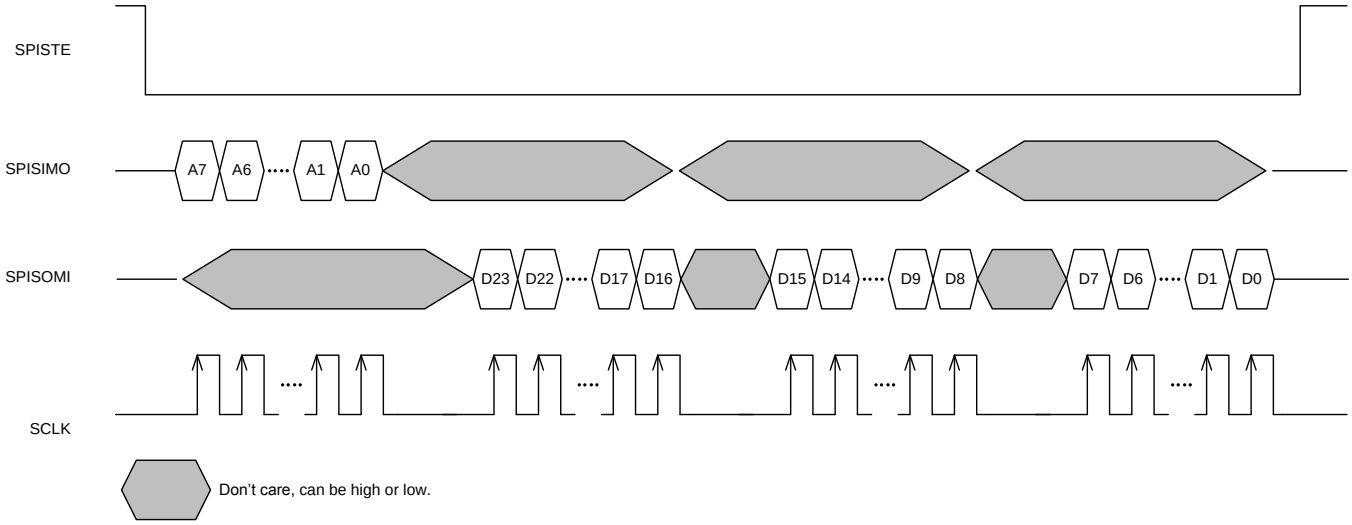


Figure 79. AFE SPI Write Timing Diagram

Programming (continued)

8.5.2.2 Reading Data

The SPI_READ register bit must be first set to '1' before reading from a register. The device includes a mode where the contents of the internal registers can be read back on the SPISOMI pin. This mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the AFE. To enable this mode, first set the SPI_READ register bit using the SPI write command, as described in the *Writing Data* section. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SPISOMI pin. Figure 80 shows an SPI timing diagram for a single read operation. For multiple read and write cycles, refer to the *Multiple Data Reads and Writes* section.



(1) The SPI_READ register bit must be enabled before attempting a serial readout from the AFE.

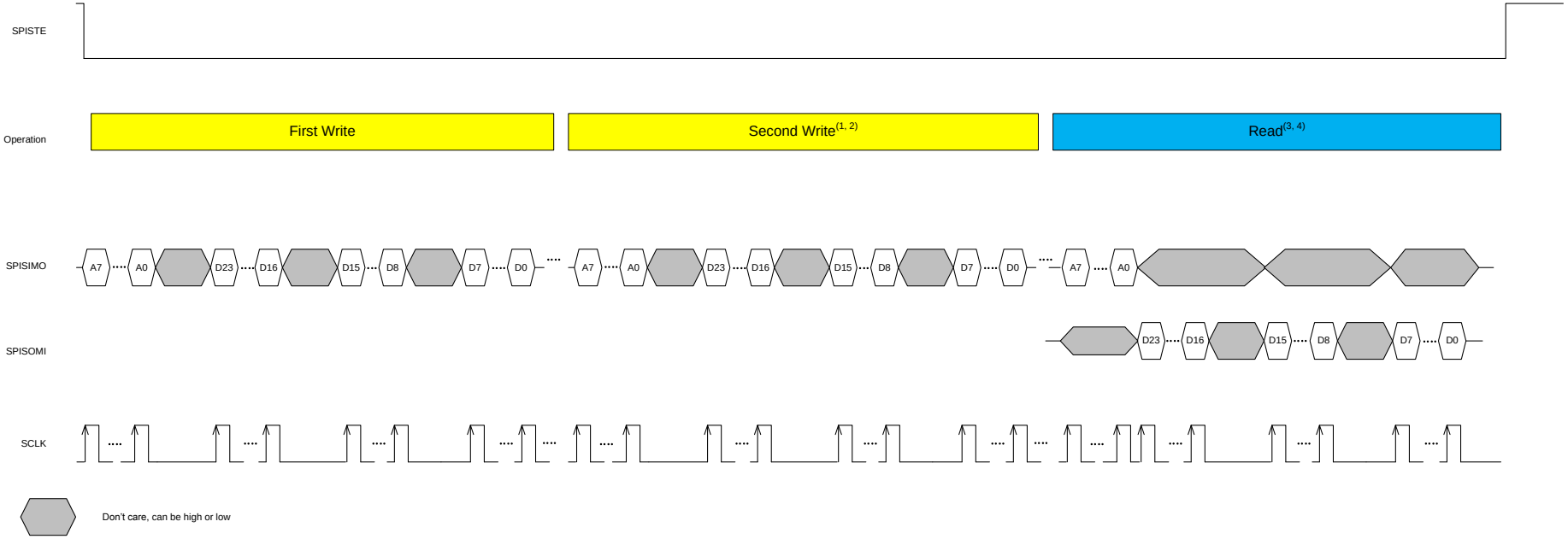
(2) Specify the register address of the content that must be readback on bits A[7:0].

(3) The AFE outputs the contents of the specified register on the SPISOMI pin.

Figure 80. AFE SPI Read Timing Diagram(1)(2)(3)

8.5.2.3 Multiple Data Reads and Writes

The device includes functionality where multiple read and write operations can be performed during a single SPISTE event. To enable this functionality, the first eight bits determine the register address to be written and the remaining 24 bits determine the register data. Perform two writes with the SPI read bit enabled during the second write operation in order to prepare for the read operation, as described in the *Writing Data* section. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SPISOMI pin. This functionality is described in the *Writing Data* and *Reading Data* sections. Figure 81 shows a timing diagram for the SPI multiple read and write operations.



(1) The SPI read register bit must be enabled before attempting a serial readout from the AFE.

(2) The second write operation must be configured for register 0 with data 000001h.

(3) Specify the register address whose contents must be read back on A[7:0].

(4) The AFE outputs the contents of the specified register on the SOMI pin.

Figure 81. Serial Multiple Read and Write Operations

8.5.2.4 Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be done in one of two ways:

- Through a hardware reset by applying a low-going pulse on the $\overline{\text{RESET}}$ pin, or
- By applying a software reset. Using the serial interface, set SW_RESET (bit D3 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets to '0'. In this case, the $\overline{\text{RESET}}$ pin is kept high (inactive).

8.5.2.5 AFE SPI Interface Design Considerations

Note that when the device is deselected, the SPISOMI, CLKOUT, ADC_RDY, PD_ALM, LED_ALM, and DIAG_END digital output pins do not enter a 3-state mode. This condition, therefore, must be taken into account when connecting multiple devices to the SPI port and for power-management considerations. In order to avoid loading the SPI bus when multiple devices are connected, the DIGOUT_TRISTATE register bit must be to '1' whenever the AFE SPI is inactive.

8.6 Register Maps

The AFE consists of a set of registers that can be used to configure it, such as receiver timings, I-V amplifier settings, transmit LED currents, and so forth. The registers and their contents are listed in Table 4. These registers can be accessed using the AFE SPI interface.

Table 4. AFE Register Map

NAME	REGISTER CONTROL(1)	ADDRESS		REGISTER DATA																					
		Hex	Dec	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL0	W	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW_RST	DIAG_EN	TIM_COUNT_RST	SPI_READ
LED2STC	R/W	01	1	0	0	0	0	0	0	0	0	LED2STC[15:0]															
LED2ENDC	R/W	02	2	0	0	0	0	0	0	0	0	LED2ENDC[15:0]															
LED2LEDSTC	R/W	03	3	0	0	0	0	0	0	0	0	LED2LEDSTC[15:0]															
LED2LEDENDC	R/W	04	4	0	0	0	0	0	0	0	0	LED2LEDENDC[15:0]															
ALED2STC	R/W	05	5	0	0	0	0	0	0	0	0	ALED2STC[15:0]															
ALED2ENDC	R/W	06	6	0	0	0	0	0	0	0	0	ALED2ENDC[15:0]															
LED1STC	R/W	07	7	0	0	0	0	0	0	0	0	LED1STC[15:0]															
LED1ENDC	R/W	08	8	0	0	0	0	0	0	0	0	LED1ENDC[15:0]															
LED1LEDSTC	R/W	09	9	0	0	0	0	0	0	0	0	LED1LEDSTC[15:0]															
LED1LEDENDC	R/W	0A	10	0	0	0	0	0	0	0	0	LED1LEDENDC[15:0]															
ALED1STC	R/W	0B	11	0	0	0	0	0	0	0	0	ALED1STC[15:0]															
ALED1ENDC	R/W	0C	12	0	0	0	0	0	0	0	0	ALED1ENDC[15:0]															
LED2CONVST	R/W	0D	13	0	0	0	0	0	0	0	0	LED2CONVST[15:0]															
LED2CONVEND	R/W	0E	14	0	0	0	0	0	0	0	0	LED2CONVEND[15:0]															
ALED2CONVST	R/W	0F	15	0	0	0	0	0	0	0	0	ALED2CONVST[15:0]															
ALED2CONVEND	R/W	10	16	0	0	0	0	0	0	0	0	ALED2CONVEND[15:0]															
LED1CONVST	R/W	11	17	0	0	0	0	0	0	0	0	LED1CONVST[15:0]															
LED1CONVEND	R/W	12	18	0	0	0	0	0	0	0	0	LED1CONVEND[15:0]															
ALED1CONVST	R/W	13	19	0	0	0	0	0	0	0	0	ALED1CONVST[15:0]															
ALED1CONVEND	R/W	14	20	0	0	0	0	0	0	0	0	ALED1CONVEND[15:0]															
ADCRSTSTCT0	R/W	15	21	0	0	0	0	0	0	0	0	ADCRSTCT0[15:0]															
ADCRSTENDCT0	R/W	16	22	0	0	0	0	0	0	0	0	ADCRENDCT0[15:0]															
ADCRSTSTCT1	R/W	17	23	0	0	0	0	0	0	0	0	ADCRSTCT1[15:0]															
ADCRSTENDCT1	R/W	18	24	0	0	0	0	0	0	0	0	ADCRENDCT1[15:0]															
ADCRSTSTCT2	R/W	19	25	0	0	0	0	0	0	0	0	ADCRSTCT2[15:0]															
ADCRSTENDCT2	R/W	1A	26	0	0	0	0	0	0	0	0	ADCRENDCT2[15:0]															
ADCRSTSTCT3	R/W	1B	27	0	0	0	0	0	0	0	0	ADCRSTCT3[15:0]															
ADCRSTENDCT3	R/W	1C	28	0	0	0	0	0	0	0	0	ADCRENDCT3[15:0]															

(1) R = read only, R/W = read or write, N/A = not available, and W = write only.

Register Maps (continued)

Table 4. AFE Register Map (continued)

NAME	REGISTER CONTROL[1]	ADDRESS		REGISTER DATA																						
		Hex	Dec	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PRPCOUNT	R/W	1D	29	0	0	0	0	0	0	0	0	PRPCT[15:0]															
CONTROL1	R/W	1E	30	0	0	0	0	0	0	0	0	0	0	0	0	CLKALMPIN[2:0]			TIMEREN	NUMAV[7:0]							
SPARE1	N/A	1F	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TIAGAIN	R/W	20	32	0	0	0	0	0	0	0	0	ENSEPGAN	STAGE2EN1	0	0	0	STG2GAIN1[2:0]			CF_LED1[4:0]					RF_LED1[2:0]		
TIA_AMB_GAIN	R/W	21	33	0	0	0	0	AMBDAC[3:0]				FLTRCNRSEL	STAGE2EN2	0	0	0	STG2GAIN2[2:0]			CF_LED2[4:0]					RF_LED2[2:0]		
LEDCNTRL	R/W	22	34	0	0	0	0	0	0	LED RANGE[1:0]		LED1[7:0]								LED2[7:0]							
CONTROL2	R/W	23	35	0	0	0	0	0	TX_REF1	TX_REF0	RST_CLK_ON_PD_ALM	EN_ADC_BYP	0	0	0	TXBRGMOD	DIGOUT_TRISTATE	XTALDIS	EN_SLOW_DIAG	0	0	0	0	0	PDNTX	PDNRX	PDNAFE
SPARE2	N/A	24	36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPARE3	N/A	25	37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPARE4	N/A	26	38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED1	N/A	27	39	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
RESERVED2	N/A	28	40	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ALARM	R/W	29	41	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ALMPINCLKEN	0	0	0	0	0	0	0

Register Maps (continued)

Table 4. AFE Register Map (continued)

NAME	REGISTER CONTROL(1)	ADDRESS		REGISTER DATA																						
		Hex	Dec	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2VAL	R	2A	42	LED2VAL[23:0]																							
ALED2VAL	R	2B	43	ALED2VAL[23:0]																							
LED1VAL	R	2C	44	LED1VAL[23:0]																							
ALED1VAL	R	2D	45	ALED1VAL[23:0]																							
LED2-ALED2VAL	R	2E	46	LED2-ALED2VAL[23:0]																							
LED1-ALED1VAL	R	2F	47	LED1-ALED1VAL[23:0]																							
DIAG	R	30	48	0	0	0	0	0	0	0	0	0	0	0	PD_ALM	LED_ALM	LED1OPEN	LED2OPEN	LEDSC	OUTPSHGN	OUTNSHGND	PDOC	PDSC	INNSCGND	INPSCGND	INNSCLED	INPSCLED

8.6.1 AFE Register Description

Figure 82. CONTROL0: Control Register 0 (Address = 00h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	SW_RST	DIAG_EN	TIM_ COUNT_ RST	SPI_ READ
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

This register is write-only. CONTROL0 is used for AFE software and count timer reset, diagnostics enable, and SPI read functions.

Bits D[23:4] **Must be '0'**

Bit D3 **SW_RST: Software reset**

0 = No action (default after reset)
1 = Software reset applied; resets all internal registers to the default values and self-clears to '0'

Bit D2 **DIAG_EN: Diagnostic enable**

0 = No Action (default after reset)
1 = Diagnostic mode is enabled and the diagnostics sequence starts when this bit is set. At the end of the sequence, all fault statuses are stored in the *DIAG: Diagnostics Flag Register*. Afterwards, the DIAG_EN register bit self-clears to '0'.
Note that the diagnostics enable bit is automatically reset after the diagnostics completes (slow =16 ms, fast = 8 ms). During diagnostics mode, the ADC data are invalid because of toggling diagnostics switches.

Bit D1 **TIM_CNT_RST: Timer counter reset**

0 = Disables timer counter reset, required for normal timer operation (default after reset)
1 = Timer counters are in reset state

Bit D0 **SPI READ: SPI read**

0 = SPI read is disabled (default after reset)
1 = SPI read is enabled

Figure 83. LED2STC: Sample LED2 Start Count Register (Address = 01h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2STC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2STC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for the LED2 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2STC[15:0]: Sample LED2 start count**

The contents of this register can be used to position the start of the sample LED2 signal with respect to the pulse repetition period (PRP), as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 84. LED2ENDC: Sample LED2 End Count Register (Address = 02h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2ENDC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2ENDC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for the LED2 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2ENDC[15:0]: Sample LED2 end count**

The contents of this register can be used to position the end of the sample LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 85. LED2LEDSTC: LED2 LED Start Count Register (Address = 03h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2LEDSTC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2LEDSTC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for when the LED2 signal turns on.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2LEDSTC[15:0]: LED2 start count**

The contents of this register can be used to position the start of the LED2 with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 86. LED2LEDENDC: LED2 LED End Count Register (Address = 04h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2LEDENDC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2LEDENDC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for when the LED2 signal turns off.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2LEDENDC[15:0]: LED2 end count**

The contents of this register can be used to position the end of the LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 87. ALED2STC: Sample Ambient LED2 Start Count Register (Address = 05h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2STC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2STC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for the ambient LED2 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED2STC[15:0]: Sample ambient LED2 start count**

The contents of this register can be used to position the start of the sample ambient LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 88. ALED2ENDC: Sample Ambient LED2 End Count Register (Address = 06h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2ENDC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2ENDC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for the ambient LED2 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED2ENDC[15:0]: Sample ambient LED2 end count**

The contents of this register can be used to position the end of the sample ambient LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 89. LED1STC: Sample LED1 Start Count Register (Address = 07h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1STC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1STC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for the LED1 signal sample.

Bits D[23:17] **Must be '0'**

Bits D[16:0] **LED1STC[15:0]: Sample LED1 start count**

The contents of this register can be used to position the start of the sample LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 90. LED1ENDC: Sample LED1 End Count (Address = 08h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1ENDC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1ENDC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for the LED1 signal sample.

Bits D[23:17] **Must be '0'**

Bits D[16:0] **LED1ENDC[15:0]: Sample LED1 end count**

The contents of this register can be used to position the end of the sample LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 91. LED1LEDSTC: LED1 LED Start Count Register (Address = 09h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1LEDSTC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1LEDSTC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for when the LED1 signal turns on.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED1LEDSTC[15:0]: LED1 start count**

The contents of this register can be used to position the start of the LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 92. LED1LEDENDC: LED1 LED End Count Register (Address = 0Ah, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1LEDENDC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1LEDENDC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for when the LED1 signal turns off.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED1LEDENDC[15:0]: LED1 end count**

The contents of this register can be used to position the end of the LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 93. ALED1STC: Sample Ambient LED1 Start Count Register (Address = 0Bh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1STC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1STC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for the ambient LED1 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED1STC[15:0]: Sample ambient LED1 start count**

The contents of this register can be used to position the start of the sample ambient LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 94. ALED1ENDC: Sample Ambient LED1 End Count Register (Address = 0Ch, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1ENDC[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1ENDC[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for the ambient LED1 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED1ENDC[15:0]: Sample ambient LED1 end count**

The contents of this register can be used to position the end of the sample ambient LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 95. LED2CONVST: LED2 Convert Start Count Register (Address = 0Dh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2CONVST[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2CONVST[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for the LED2 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2CONVST[15:0]: LED2 convert start count**

The contents of this register can be used to position the start of the LED2 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 96. LED2CONVEND: LED2 Convert End Count Register (Address = 0Eh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2CONVEND[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2CONVEND[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for the LED2 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2CONVEND[15:0]: LED2 convert end count**

The contents of this register can be used to position the end of the LED2 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 97. ALED2CONVST: LED2 Ambient Convert Start Count Register (Address = 0Fh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2CONVST[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2CONVST[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for the ambient LED2 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED2CONVST[15:0]: LED2 ambient convert start count**

The contents of this register can be used to position the start of the LED2 ambient conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 98. ALED2CONVEND: LED2 Ambient Convert End Count Register (Address = 10h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2CONVEND[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2CONVEND[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for the ambient LED2 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED2CONVEND[15:0]: LED2 ambient convert end count**

The contents of this register can be used to position the end of the LED2 ambient conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 99. LED1CONVST: LED1 Convert Start Count Register (Address = 11h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1CONVST[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1CONVST[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for the LED1 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED1CONVST[15:0]: LED1 convert start count**

The contents of this register can be used to position the start of the LED1 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 100. LED1CONVEND: LED1 Convert End Count Register (Address = 12h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1CONVEND[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1CONVEND[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for the LED1 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED1CONVEND[15:0]: LED1 convert end count**

The contents of this register can be used to position the end of the LED1 conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 101. ALED1CONVST: LED1 Ambient Convert Start Count Register (Address = 13h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1CONVST[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1CONVST[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start timing value for the ambient LED1 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED1CONVST[15:0]: LED1 ambient convert start count**

The contents of this register can be used to position the start of the LED1 ambient conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 102. ALED1CONVEND: LED1 Ambient Convert End Count Register (Address = 14h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1CONVEND[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1CONVEND[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end timing value for the ambient LED1 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED1CONVEND[15:0]: LED1 ambient convert end count**

The contents of this register can be used to position the end of the LED1 ambient conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 103. ADCRSTSTCT0: ADC Reset 0 Start Count Register (Address = 15h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT0[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT0[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start position of the ADC0 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTSTCT0[15:0]: ADC RESET 0 start count**

The contents of this register can be used to position the start of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

Figure 104. ADCRSTENDCT0: ADC Reset 0 End Count Register (Address = 16h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT0[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT0[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end position of the ADC0 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTENDCT0[15:0]: ADC RESET 0 end count**

The contents of this register can be used to position the end of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

Figure 105. ADCRSTSTCT1: ADC Reset 1 Start Count Register (Address = 17h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT1[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT1[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start position of the ADC1 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTSTCT1[15:0]: ADC RESET 1 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 106. ADCRSTENDCT1: ADC Reset 1 End Count Register (Address = 18h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT1[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT1[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end position of the ADC1 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTENDCT1[15:0]: ADC RESET 1 end count**

The contents of this register can be used to position the end of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 107. ADCRSTSTCT2: ADC Reset 2 Start Count Register (Address = 19h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT2[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT2[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start position of the ADC2 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTSTCT2[15:0]: ADC RESET 2 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 108. ADCRSTENDCT2: ADC Reset 2 End Count Register (Address = 1Ah, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT2[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT2[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end position of the ADC2 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTENDCT2[15:0]: ADC RESET 2 end count**

The contents of this register can be used to position the end of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 109. ADCRSTSTCT3: ADC Reset 3 Start Count Register (Address = 1Bh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT3[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT3[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the start position of the ADC3 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTSTCT3[15:0]: ADC RESET 3 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 110. ADCRSTENDCT3: ADC Reset 3 End Count Register (Address = 1Ch, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT3[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT3[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the end position of the ADC3 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTENDCT3[15:0]: ADC RESET 3 end count**

The contents of this register can be used to position the end of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

Figure 111. PRPCOUNT: Pulse Repetition Period Count Register (Address = 1Dh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	PRPCOUNT[15:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PRPCOUNT[15:0]											
R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the device pulse repetition period count.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **PRPCOUNT[15:0]: Pulse repetition period count**

The contents of this register can be used to set the pulse repetition period (in number of clock cycles of the 4-MHz clock). The PRPCOUNT value must be set in the range of 800 to 64000. Values below 800 do not allow sufficient sample time for the four samples; see the *Electrical Characteristics* table.

Figure 112. CONTROL1: Control Register 1 (Address = 1Eh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CLKALMPIN[2:0]			TIMEREN	NUMAV[7:0]							
R/W-0h			R/W-0h	R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

This register configures the clock alarm pin, timer, and number of averages.

Bits D[23:12] **Must be '0'**

Bits D[11:9] **CLKALMPIN[2:0]: Clocks on ALM pins**

Internal clocks can be brought to the PD_ALM and LED_ALM pins for monitoring.
Note that the ALMPINCLKEN register bit must be set before using this register bit. Table 5 defines the settings for the two alarm pins.

Bit D8 **TIMEREN: Timer enable**

0 = Timer module is disabled and all internal clocks are off (default after reset)
1 = Timer module is enabled

Bits D[7:0] **NUMAV[7:0]: Number of averages**

Specify an 8-bit value corresponding to the number of ADC samples to be averaged – 1.
For example, to average four ADC samples, set NUMAV[7:0] equal to 3.
The maximum number of averages is 16. Any NUMAV[7:0] setting greater than or equal to a decimal value of 15 results in the number of averages being set to 16.

Table 5. PD_ALM and LED_ALM Pin Settings

CLKALMPIN[2:0]	PD_ALM PIN SIGNAL	LED_ALM PIN SIGNAL
000	Sample LED2 pulse	Sample LED1 pulse
001	LED2 LED pulse	LED1 LED pulse
010	Sample LED2 ambient pulse	Sample LED1 ambient pulse
011	LED2 convert	LED1 convert
100	LED2 ambient convert	LED1 ambient convert
101	No output	No output
110	No output	No output
111	No output	No output

Figure 113. SPARE1: SPARE1 Register For Future Use (Address = 1Fh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

This register is a spare register and is reserved for future use.

Bits D[23:0] Must be '0'

Figure 114. TIAGAIN: Transimpedance Amplifier Gain Setting Register (Address = 20h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ENSEP GAIN	STAGE2 EN1	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	STG2GAIN1[2:0]			CF_LED1[4:0]					RF_LED1[2:0]		
R/W-0h	R/W-0h			R/W-0h					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the device transimpedance amplifier gain mode and feedback resistor and capacitor values.

Bits D[23:16] **Must be '0'**

Bit D15 **ENSEPGAIN: Enable separate gain mode**

0 = The R_F, C_F values and stage 2 gain settings are the same for both the LED2 and LED1 signals; the values are specified by the RF_LED2, CF_LED2, STAGE2EN2, and STG2GAIN2 bits in the TIA_AMB_GAIN register (default after reset)
1 = The R_F, C_F values and stage 2 gain settings can be independently set for the LED2 and LED1 signals. The values for LED1 are specified using the RF_LED1, CF_LED1, STAGE2EN1, and STG2GAIN1 bits in the TIAGAIN register, whereas the values for LED2 are specified using the corresponding bits in the TIA_AMB_GAIN register.

Bit D14 **STAGE2EN1: Enable Stage 2 for LED 1**

0 = Stage 2 is bypassed (default after reset)
1 = Stage 2 is enabled with the gain value specified by the STG2GAIN1[2:0] bits

Bits D[13:11] **Must be '0'**

Bits D[10:8] **STG2GAIN1[2:0]: Program Stage 2 gain for LED1**

000 = 0 dB, or linear gain of 1 (default after reset)
001 = 3.5 dB, or linear gain of 1.5
010 = 6 dB, or linear gain of 2
011 = 9.5 dB, or linear gain of 3
100 = 12 dB, or linear gain of 4
101 = Do not use
110 = Do not use
111 = Do not use

Bits D[7:3] **CF_LED1[4:0]: Program C_F for LED1**

00000 = 5 pF (default after reset)
00001 = 5 pF + 5 pF
00010 = 15 pF + 5 pF
00100 = 25 pF + 5 pF
01000 = 50 pF + 5 pF
10000 = 150 pF + 5 pF

Note that any combination of these C_F settings is also supported by setting multiple bits to '1'. For example, to obtain C_F = 100 pF, set D[7:3] = 01111.

Bits D[2:0] **RF_LED1[2:0]: Program R_F for LED1**

000 = 500 kΩ (default after reset)
001 = 250 kΩ
010 = 100 kΩ
011 = 50 kΩ
100 = 25 kΩ
101 = 10 kΩ
110 = 1 MΩ
111 = None

Figure 115. TIA_AMB_GAIN: Transimpedance Amplifier and Ambient Cancellation Stage Gain Register (Address = 21h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	AMBDAC[3:0]				FLTR CNRSEL	STAGE2 EN2	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	STG2GAIN2[2:0]			CF_LED2[4:0]					RF_LED2[2:0]		
R/W-0h	R/W-0h			R/W-0h					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

This register configures the ambient light cancellation amplifier gain, cancellation current, and filter corner frequency.

Bits D[23:20] **Must be '0'**

Bits D[19:16] **AMBDAC[3:0]: Ambient DAC value**

These bits set the value of the cancellation current.

0000 = 0 µA (default after reset)
0001 = 1 µA
0010 = 2 µA
0011 = 3 µA
0100 = 4 µA
0101 = 5 µA
0110 = 6 µA
0111 = 7 µA
1000 = 8 µA
1001 = 9 µA
1010 = 10 µA
1011 = Do not use
1100 = Do not use
1101 = Do not use
1110 = Do not use
1111 = Do not use

Bit D15 **FLTRCNRSEL: Filter corner selection**

0 = 500-Hz filter corner (default after reset)
1 = 1000-Hz filter corner

Bit D14 **STAGE2EN2: Stage 2 enable for LED 2**

0 = Stage 2 is bypassed (default after reset)
1 = Stage 2 is enabled with the gain value specified by the STG2GAIN2[2:0] bits

Bits D[13:11] **Must be '0'**

Bits D[10:8] **STG2GAIN2[2:0]: Stage 2 gain setting for LED 2**

000 = 0 dB, or linear gain of 1 (default after reset)
001 = 3.5 dB, or linear gain of 1.5
010 = 6 dB, or linear gain of 2
011 = 9.5 dB, or linear gain of 3
100 = 12 dB, or linear gain of 4
101 = Do not use
110 = Do not use
111 = Do not use

Bits D[7:3] **CF_LED2[4:0]: Program C_F for LED2**

00000 = 5 pF (default after reset)
00001 = 5 pF + 5 pF
00010 = 15 pF + 5 pF
00100 = 25 pF + 5 pF
01000 = 50 pF + 5 pF
10000 = 150 pF + 5 pF

Note that any combination of these C_F settings is also supported by setting multiple bits to '1'. For example, to obtain C_F = 100 pF, set D[7:3] = 01111.

Bits D[2:0] **RF_LED2[2:0]: Program R_F for LED2**

000 = 500 kΩ
001 = 250 kΩ
010 = 100 kΩ
011 = 50 kΩ
100 = 25 kΩ
101 = 10 kΩ
110 = 1 MΩ
111 = None

Figure 116. LEDCNTRL: LED Control Register (Address = 22h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	LED_RANGE[1:0]		LED1[7:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h			
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1[7:0]				LED2[7:0]							
R/W-0h				R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

This register sets the LED current range and the LED1 and LED2 drive current.

Bits D[23:18] **Must be '0'**

Bits D[17:16] **LED_RANGE[1:0]: LED range**

These bits program the full-scale LED current range for Tx. Table 6 details the settings.

Bits D[15:8] **LED1[7:0]: Program LED current for LED1 signal**

Use these register bits to specify the LED current setting for LED1 (default after reset is 00h).
The nominal value of the LED current is given by Equation 6,
where the full-scale LED current is either 0 mA, 50 mA, 75 mA, 100 mA, 150 mA, or 200 mA (as specified by the LED_RANGE[1:0] register bits).

Bits D[7:0] **LED2[7:0]: Program LED current for LED2 signal**

Use these register bits to specify the LED current setting for LED2 (default after reset is 00h).
The nominal value of LED current is given by Equation 7,
where the full-scale LED current is either 0 mA, 50 mA, 75 mA, 100 mA, 150 mA, or 200 mA (as specified by the LED_RANGE[1:0] register bits).

Table 6. Full-Scale LED Current across Tx Reference Voltage Settings(1)

LED_RANGE[1:0]	0.75 V (TX_REF[1:0] = 00)		0.5 V (TX_REF[1:0] = 01)		1.0 V (TX_REF[1:0] = 10)	
	I_{MAX}	V_{HR}	I_{MAX}	V_{HR}	I_{MAX}	V_{HR}
00 (default after reset)	150 mA	1.4 V	100 mA	1.1 V	200 mA	1.7 V
01	75 mA	1.3 V	50 mA	1.0 V	100 mA	1.6 V
10	150 mA	1.4 V	100 mA	1.1 V	200 mA	1.7 V
11	Tx is off	—	Tx is off	—	Tx is off	—

(1) For a 3-V to 3.6-V supply, use TX_REF = 0.5 V. For a 4.75-V to 5.25-V supply, use TX_REF = 0.75 V or 1.0 V.

$$\frac{\text{LED1[7:0]}}{256} \times \text{Full-Scale Current} \quad (6)$$

$$\frac{\text{LED2[7:0]}}{256} \times \text{Full-Scale Current} \quad (7)$$

Figure 117. CONTROL2: Control Register 2 (Address = 23h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	TX_REF1	TX_REF0	RST_CLK_ON_PD_ALM	EN_ADC_BYP	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TXBRGMOD	DIGOUT_TRISTATE	XTALDIS	EN_SLOW_DIAG	0	0	0	0	0	PDNTX	PDNRX	PDNAFE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

This register controls the LED transmitter, crystal, and the AFE, transmitter, and receiver power modes.

Bits D[23:19] **Must be '0'**

Bits D[18:17] **TX_REF[1:0]: Tx reference voltage**

These bits set the transmitter reference voltage. This Tx reference voltage is available on the device TX_REF pin.

00 = 0.75-V Tx reference voltage (default value after reset)
01 = 0.5-V Tx reference voltage
10 = 1.0-V Tx reference voltage
11 = 0.75-V Tx reference voltage

NOTE: For best results, use TX_REF = 0.5 V for 3-V operation. Use TX_REF = 0.75V and TX_REF = 1.0 V for 5-V operation.

Bit D16 **RST_CLK_ON_PD_ALM: Reset clock onto PD_ALM pin**

0 = Normal mode; no reset clock signal is connected to the PD_ALM pin
1 = Reset clock signal is connected to the PD_ALM pin

Bit D15 **EN_ADC_BYP: ADC bypass mode enable**

0 = Normal mode, the internal ADC is active (default after reset)
1 = ADC bypass mode, the analog signal is output to the ADC_BYPP and ADC_BYPN pins

Bits D[14:12] **Must be '0'**

Bit D11 **TXBRGMOD: Tx bridge mode**

0 = LED driver is configured as an H-bridge (default after reset)
1 = LED driver is configured as a push-pull

Bit D10 **DIGOUT_TRISTATE: Digital output 3-state mode**

This bit determines the state of the device digital output pins, including the clock output pin and SPI output pins. In order to avoid loading the SPI bus when multiple devices are connected, this bit must be set to '1' (3-state mode) whenever the device SPI is inactive.

0 = Normal operation (default)
1 = 3-state mode

Bit D9 **XTALDIS: Crystal disable mode**

0 = The crystal module is enabled; the 8-MHz crystal must be connected to the XIN and XOUT pins
1 = The crystal module is disabled; an external 8-MHz clock must be applied to the XIN pin

Bit D8 **EN_SLOW_DIAG: Fast diagnostics mode enable**

0 = Fast diagnostics mode, 8 ms (default value after reset)
1 = Slow diagnostics mode, 16 ms

Bits D[7:3] **Must be '0'**

Bit D2 **PDN_TX: Tx power-down**

0 = The Tx is powered up (default after reset)
1 = Only the Tx module is powered down

Bit D1 **PDN_RX: Rx power-down**

0 = The Rx is powered up (default after reset)
1 = Only the Rx module is powered down

Bit D0 **PDN_AFE: AFE power-down**

0 = The AFE is powered up (default after reset)
1 = The entire AFE is powered down (including the Tx, Rx, and diagnostics blocks)

Figure 118. SPARE2: SPARE2 Register For Future Use (Address = 24h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

This register is a spare register and is reserved for future use.

Bits D[23:0] **Must be '0'**

Figure 119. SPARE3: SPARE3 Register For Future Use (Address = 25h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

This register is a spare register and is reserved for future use.

Bits D[23:0] **Must be '0'**

Figure 120. SPARE4: SPARE4 Register For Future Use (Address = 26h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

This register is a spare register and is reserved for future use.

Bits D[23:0] **Must be '0'**

Figure 121. RESERVED1: RESERVED1 Register For Factory Use Only (Address = 27h, Reset Value = XXXXh)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
X(1)	X	X	X	X	X	X	X	X	X	X	X
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

(1) X = don't care.

This register is reserved for factory use. Readback values vary between devices.

Bits D[23:0] Must be '0'

Figure 122. RESERVED2: RESERVED2 Register For Factory Use Only (Address = 28h, Reset Value = XXXXh)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
X(1)	X	X	X	X	X	X	X	X	X	X	X
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

(1) X = don't care.

This register is reserved for factory use. Readback values vary between devices.

Bits D[23:0] Must be '0'

Figure 123. ALARM: Alarm Register (Address = 29h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	ALMPIN CLKEN	0	0	0	0	0	0	0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

This register controls the Alarm pin functionality.

Bits D[23:8] Must be '0'

Bit D7 ALMPINCLKEN: Alarm pin clock enable

0 = Disables the monitoring of internal clocks; the PD_ALM and LED_ALM pins function as diagnostic fault alarm output pins (default after reset)
1 = Enables the monitoring of internal clocks; these clocks can be brought out on PD_ALM and LED_ALM selectively (depending on the value of the CLKALMPIN[2:0] register bits).

Bits D[6:0] Must be '0'

Figure 124. LED2VAL: LED2 Digital Sample Value Register (Address = 2Ah, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED2VAL[23:0]											
R-0h											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2VAL[23:0]											
R-0h											

LEGEND: R = Read only; -n = value after reset

This register contains the digital value of the latest LED2 sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

Bits D[23:0] **LED2VAL[23:0]: LED2 digital value**

This register contains the digital value of the latest LED2 sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

Figure 125. ALED2VAL: Ambient LED2 Digital Sample Value Register (Address = 2Bh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
ALED2VAL[23:0]											
R-0h											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2VAL[23:0]											
R-0h											

LEGEND: R = Read only; -n = value after reset

This register contains the digital value of the latest LED2 ambient sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

Bits D[23:0] **ALED2VAL[23:0]: LED2 ambient digital value**

This register contains the digital value of the latest LED2 ambient sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

Figure 126. LED1VAL: LED1 Digital Sample Value Register (Address = 2Ch, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED1VAL[23:0]											
R-0h											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1VAL[23:0]											
R-0h											

LEGEND: R = Read only; -n = value after reset

This register contains the digital value of the latest LED1 sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

Bits D[23:0] **LED1VAL[23:0]: LED1 digital value**

This register contains the digital value of the latest LED1 sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

Figure 127. ALED1VAL: Ambient LED1 Digital Sample Value Register (Address = 2Dh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
ALED1VAL[23:0]											
R-0h											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1VAL[23:0]											
R-0h											

LEGEND: R = Read only; -n = value after reset

This register contains the digital value of the latest LED1 ambient sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

Bits D[23:0] **ALED1VAL[23:0]: LED1 ambient digital value**

This register contains the digital value of the latest LED1 ambient sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

Figure 128. LED2-ALED2VAL: LED2-Ambient LED2 Digital Sample Value Register (Address = 2Eh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED2-ALED2VAL[23:0]											
R-0h											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2-ALED2VAL[23:0]											
R-0h											

LEGEND: R = Read only; -n = value after reset

This register contains the digital value of the LED2 sample after the LED2 ambient is subtracted. The host processor must readout this register before the next sample is converted by the AFE.

Bits D[23:0] **LED2-ALED2VAL[23:0]: (LED2 – LED2 ambient) digital value**

This register contains the digital value of the LED2 sample after the LED2 ambient is subtracted. The host processor must readout this register before the next sample is converted by the AFE.
Note that this value is inverted when compared to waveforms shown in many publications.

Figure 129. LED1-ALED1VAL: LED1-Ambient LED1 Digital Sample Value Register (Address = 2Fh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED1-ALED1VAL[23:0]											
R-0h											
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1-ALED1VAL[23:0]											
R-0h											

LEGEND: R = Read only; -n = value after reset

This register contains the digital value of the LED1 sample after the LED1 ambient is subtracted. The host processor must readout this register before the next sample is converted by the AFE.

Bits D[23:0] **LED1-ALED1VAL[23:0]: (LED1 – LED1 ambient) digital value**

This register contains the digital value of the LED1 sample after the LED1 ambient is subtracted from it. The host processor must readout this register before the next sample is converted by the AFE.
Note that this value is inverted when compared to waveforms shown in many publications.

Figure 130. DIAG: Diagnostics Flag Register (Address = 30h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	PD_ALM
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED_ ALM	LED1 OPEN	LED2 OPEN	LEDSC	OUTPSH GND	OUTNSH GND	PDOC	PDSC	INNSC GND	INPSC GND	INNSC LED	INPSC LED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

This register is read only. This register contains the status of all diagnostic flags at the end of the diagnostics sequence. The end of the diagnostics sequence is indicated by the signal going high on DIAG_END pin.

Bits D[23:13] **Read only**

Bit D12 **PD_ALM: Power-down alarm status diagnostic flag**

This bit indicates the status of PD_ALM (and the PD_ALM pin).
0 = No fault (default after reset)
1 = Fault present

Bit D11 **LED_ALM: LED alarm status diagnostic flag**

This bit indicates the status of LED_ALM (and the LED_ALM pin).
0 = No fault (default after reset)
1 = Fault present

Bit D10 **LED1OPEN: LED1 open diagnostic flag**

This bit indicates that LED1 is open.
0 = No fault (default after reset)
1 = Fault present

Bit D9 **LED2OPEN: LED2 open diagnostic flag**

This bit indicates that LED2 is open.
0 = No fault (default after reset)
1 = Fault present

Bit D8 **LEDSC: LED short diagnostic flag**

This bit indicates an LED short.
0 = No fault (default after reset)
1 = Fault present

Bit D7 **OUTPSHGND: OUTP to GND diagnostic flag**

This bit indicates that OUTP is shorted to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit D6 **OUTNSHGND: OUTN to GND diagnostic flag**

This bit indicates that OUTN is shorted to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit D5 **PDOC: PD open diagnostic flag**

This bit indicates that PD is open.
0 = No fault (default after reset)
1 = Fault present

Bit D4 **PDSC: PD short diagnostic flag**

This bit indicates a PD short.
0 = No fault (default after reset)
1 = Fault present

Bit D3 **INNSCGND: INN to GND diagnostic flag**

This bit indicates a short from the INN pin to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit D2 **INPSCGND: INP to GND diagnostic flag**

This bit indicates a short from the INP pin to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit D1 **INNSCLED: INN to LED diagnostic flag**

This bit indicates a short from the INN pin to the LED cable.
0 = No fault (default after reset)
1 = Fault present

Bit D0 **INPSCLED: INP to LED diagnostic flag**

This bit indicates a short from the INP pin to the LED cable.
0 = No fault (default after reset)
1 = Fault present

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

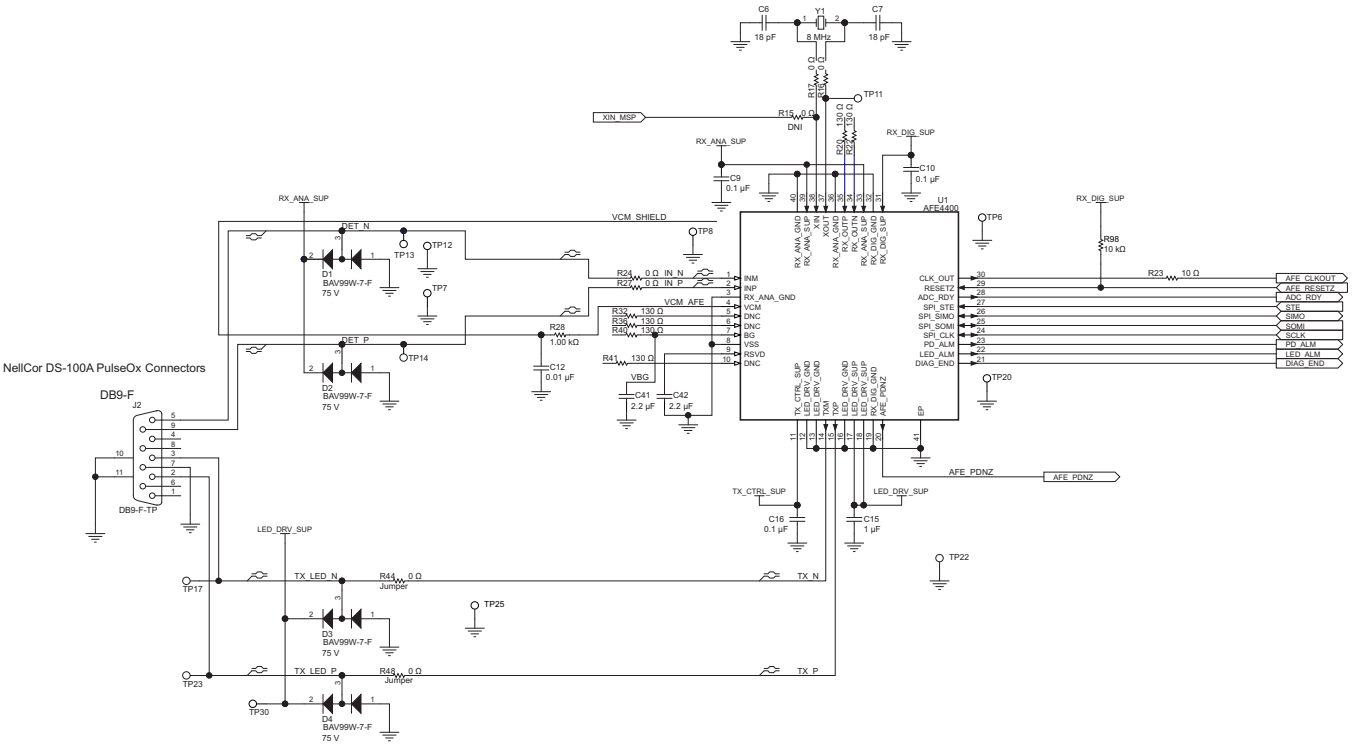
9.1 Application Information

The AFE4490 can be used for measuring SPO2 and for monitoring heart rate. The high dynamic range of the device enables measuring SPO2 with a high degree of accuracy even under low-perfusion (ac-to-dc ratio) conditions. An SPO2 measurement system involves two different wavelength LEDs—usually Red and IR. By computing the ratio of the ac to dc at the two different wavelengths, the SPO2 can be calculated. Heart rate monitoring systems can also benefit from the high dynamic range of the device, which enables capturing a high-fidelity pulsating signal even in cases where the signal strength is low.

For more information on application guidelines, refer to the *AFE44x0SPO2EVM User's Guide* (SLAU480).

9.2 Typical Application

Device connections in a typical application are shown in Figure 131. Refer to the *AFE44x0SPO2EVM User's Guide* (SLAU480) for more details. The schematic in Figure 131 is a part of the AFE44x0SPO2EVM and shows a cabled application in which the LEDs and photodiode are connected to the AFE4490 through a cable. However, in an application without cables, the LEDs and photodiode can be directly connected to the TXP, TXN and INP, INN pins directly, as shown in the *Design Requirements* section.



NOTE: The following signals must be considered as two sets of differential pains and routed as adjacent signals within each pair:
TXM, TXP and INM, INP.
INM and INP must be guarded with VCM_SHIELD the signal. Run the VCM_SHIELD signal to the DB9 connector and back to the device.

Figure 131. AFE44x0SPO2EVM: Connections to the AFE4490

Typical Application (continued)

9.2.1 Design Requirements

An SPO2 application usually involves a Red LED and an IR LED. These LEDs can be connected either in the common anode configuration or H-bridge configuration to the TXP, TXN pins. Figure 132 shows common anode configuration and Figure 133 shows H-bridge configuration.

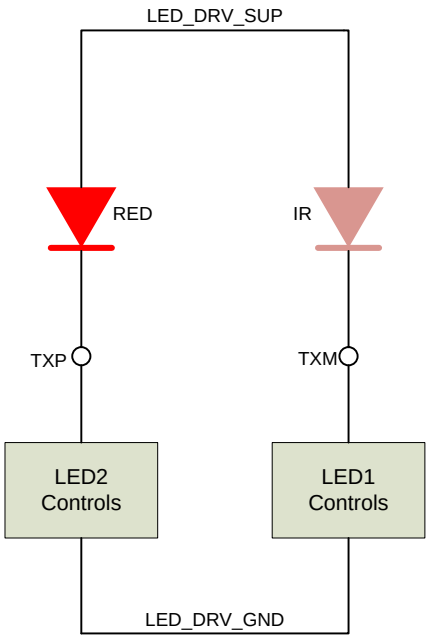


Figure 132. LEDs in Common Anode Configuration

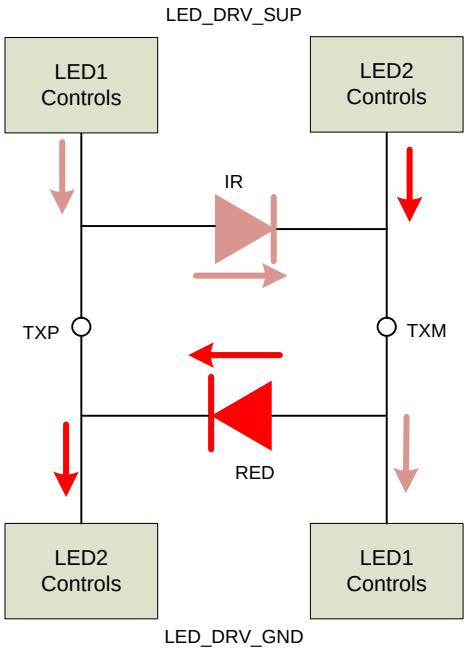


Figure 133. LEDs in H-Bridge Configuration

Typical Application (continued)

9.2.2 Detailed Design Procedure

The photodiode receives the light from both the Red and IR phases and usually has good sensitivities at both these wavelengths.

The photodiode connected in this manner operates in zero bias because of the negative feedback from the transimpedance amplifier. The connections of the photodiode to the AFE inputs are shown in Figure 134.

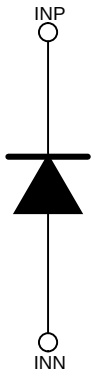


Figure 134. Photodiode Connection

The signal current generated by the photodiode is converted into a voltage by the transimpedance amplifier, which has a programmable transimpedance gain. The rest of the signal chain then presents a voltage to the ADC. The full-scale output of the transimpedance amplifier is ±1 V and the full-scale input to the ADC is ±1.2 V. An automatic gain control loop can be used to set the target dc voltage at the ADC input to approximately 50% of full scale. This type of AGC loop can control a combination of LED current and TIA gain to achieve this target value; see Figure 135.

Typical Application (continued)

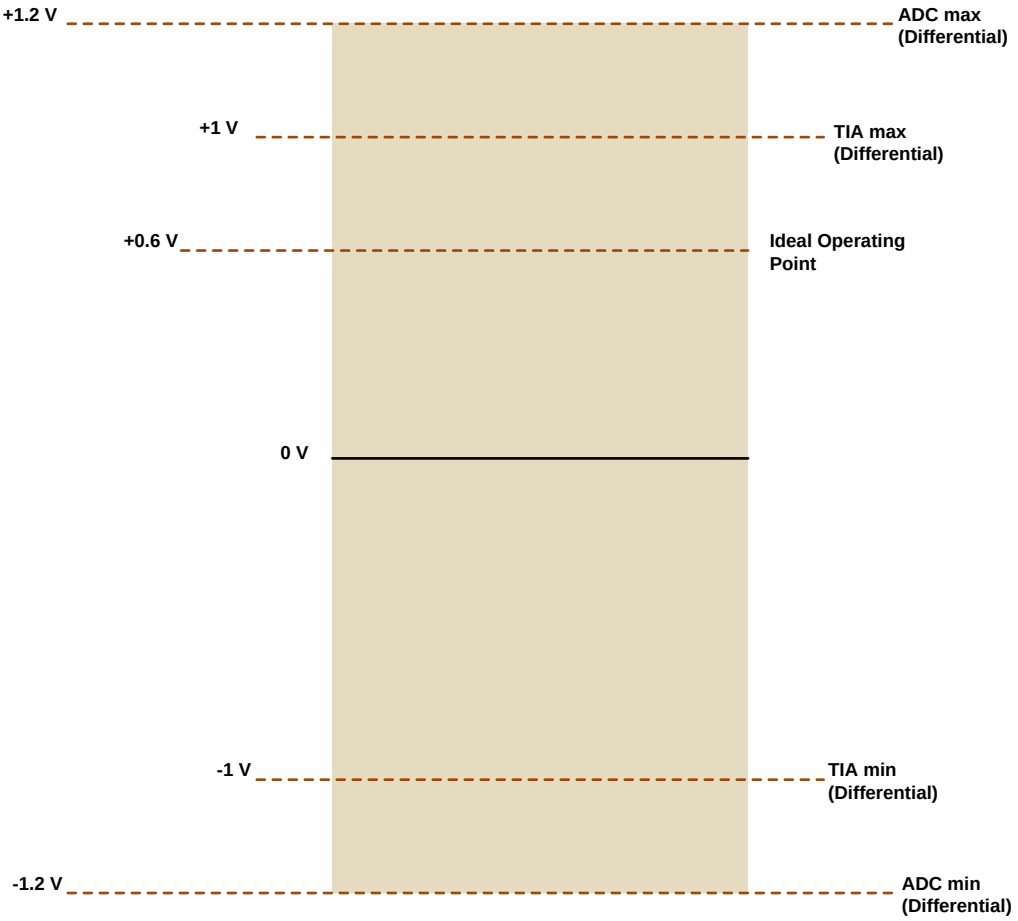


Figure 135. AGC Loop

The ADC output is a 22-bit code that is obtained by discarding the two MSBs of the 24-bit registers (for example the register with address 2Ah).

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
Ignore		22-Bit ADC Code, MSB to LSB									
R/W-0h		R/W-0h									
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
22-Bit ADC Code, MSB to LSB											
R/W-0h (TBD register correct?)											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7 shows the mapping of the input voltage to the ADC output code.

Table 7. Input Voltage Mapping

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT	22-BIT ADC OUTPUT CODE
–1.2 V	1000000000000000000000
(–1.2 / 2^{21}) V	1111111111111111111111
0	0000000000000000000000
(1.2 / 2^{21}) V	0000000000000000000001
1.2 V	0111111111111111111111

The data format is binary twos complement format, MSB first. TI recommends that the input to the ADC does not exceed ±1 V (which is approximately 80% full-scale) because the TIA has a full-scale range of ±1 V.

9.2.3 Application Curve

The dc component of the current from the PPG signal is referred to as *Pleth* (short for photoplethysmography) current. The input-referred noise current (referred differentially to the INP, INN inputs) as a function of the Pleth current is shown in Figure 136 at a PRF of 600 Hz and for various duty cycles of LED pulsing. For example, a duty cycle of 25% refers to a case where the LED is pulsed for 25% of the pulse repetition period and the receiver samples the photodiode current for the same period of time. The noise shown in Figure 136 is the integrated noise over a 20-Hz bandwidth from dc.

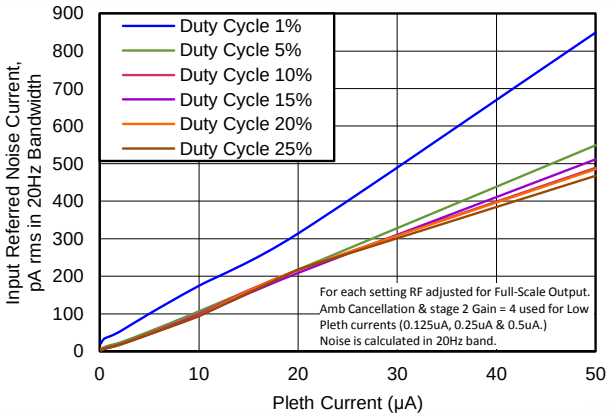


Figure 136. Input-Referred Noise Current vs Pleth Current (BW = 20Hz, PRF = 600 Hz)

10 Power-Supply Recommendations

The AFE4490 has two sets of supplies: the receiver supplies (RX_ANA_SUP, RX_DIG_SUP) and the transmitter supplies (TX_CTRL_SUP, LED_DRV_SUP). The receiver supplies can be between 2.0 V to 3.6 V whereas the transmitter supplies can be between 3.0 V to 5.25 V. Another consideration that determines the minimum allowed value of the transmitter supplies is the forward voltage of the LEDs being driven. The current source and switches inside the AFE require voltage headroom that mandates the transmitter supply to be a few hundred millivolts higher than the LED forward voltage. TX_REF is the voltage that governs the generation of the LED current from the internal reference voltage. Choosing the lowest allowed TX_REF setting reduces the additional headroom required but results in higher transmitter noise. Other than for the highest end clinical SPO2 applications, this extra noise resulting from a lower TX_REF setting might be acceptable.

The LED_DRV_SUP and TX_CTRL_SUP are recommended to be tied together to the same supply (between 3.0 V and 5.25 V). The external supply (connected to the common anode of the two LEDs) must be high enough to account for the forward drop of the LEDs as well as the voltage headroom required by the current source and switches inside the AFE. In most cases, this voltage is expected to fall below 5.25 V; thus the external supply can be the same as the LED_DRV_SUP. However, there might be cases (for instance when two LEDs are connected in series) where the voltage required on the external supply is higher than 5.25 V. Such a case must be handled with care to ensure that the voltage on the TXP and TXN pins stays less than 5.25 V and also never exceeds the supply voltage of LED_DRV_SUP, TX_CTRL_SUP by more than 0.3 V.

Many scenarios of power management are possible.

Case 1: LED forward voltage is such that a voltage of 3.3 V (for example) is acceptable on LED_DRV_SUP. In that case, a single 3.3-V supply can be used to drive all four pins (RX_ANA_SUP, RX_DIG_SUP, TX_CTRL_SUP, LED_DRV_SUP). Care must be taken to provide some isolation between the transmit and receive supplies because the LED_DRV_SUP carries the high switching current from the LEDs.

Case 2: A low-voltage supply (2.2 V for instance) is available in the system. In this case, a boost converter can be used to derive the voltage for the LED_DRV_SUP, as shown in Figure 137.

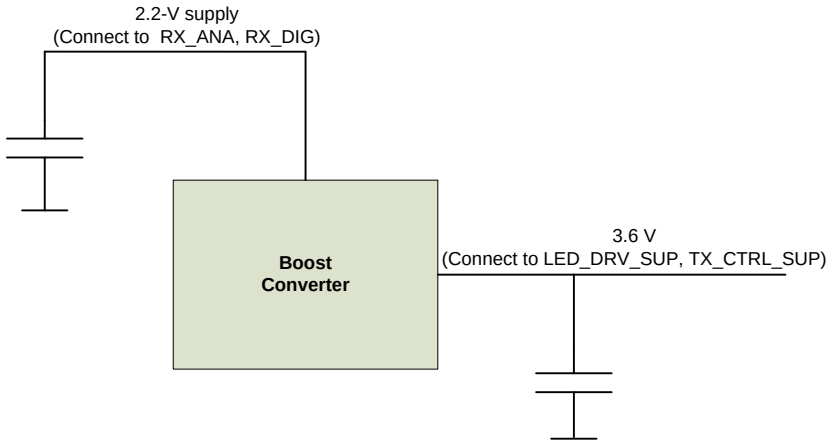


Figure 137. Boost Converter

The boost converter requires a clock (usually in the megahertz range) and there is usually a ripple at the boost converter output at this switching frequency. While this frequency is much higher than the signal frequency of interest (which is at maximum a few 10s of hertz around dc), a small fraction of this switching noise might possibly alias to the low-frequency band. Therefore, TI strongly recommends that the switching frequency of the boost converter be offset from every multiple of the PRF by at least 20 Hz, which can be ensured by choosing the appropriate PRF.

Case 3: In cases where a high voltage supply is available in the system, a buck converter or an LDO can be used to derive the voltage levels required to drive RX_ANA and RX_DIG. Such a scenario is shown in Figure 138.

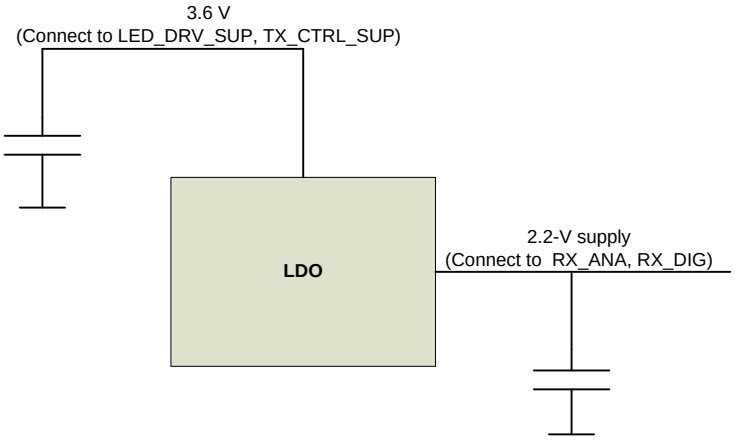


Figure 138. Buck Converter or an LDO

For more information on power-supply recommendations, see the *AFE44x0SPO2EVM User's Guide* (SLAU480).

11 Layout

11.1 Layout Guidelines

Some key layout guidelines are:

1. TXP, TXN are fast switching lines and must be routed away from sensitive reference lines as well as from the INP, INN inputs.
2. If required to route long, TI recommends that the VCM be used as a shield for the INP, INN lines.
3. The device can draw high switching currents from the LED_DRV_SUP pin. Therefore, having a decoupling capacitor electrically close to the pin is recommended.

11.2 Layout Example

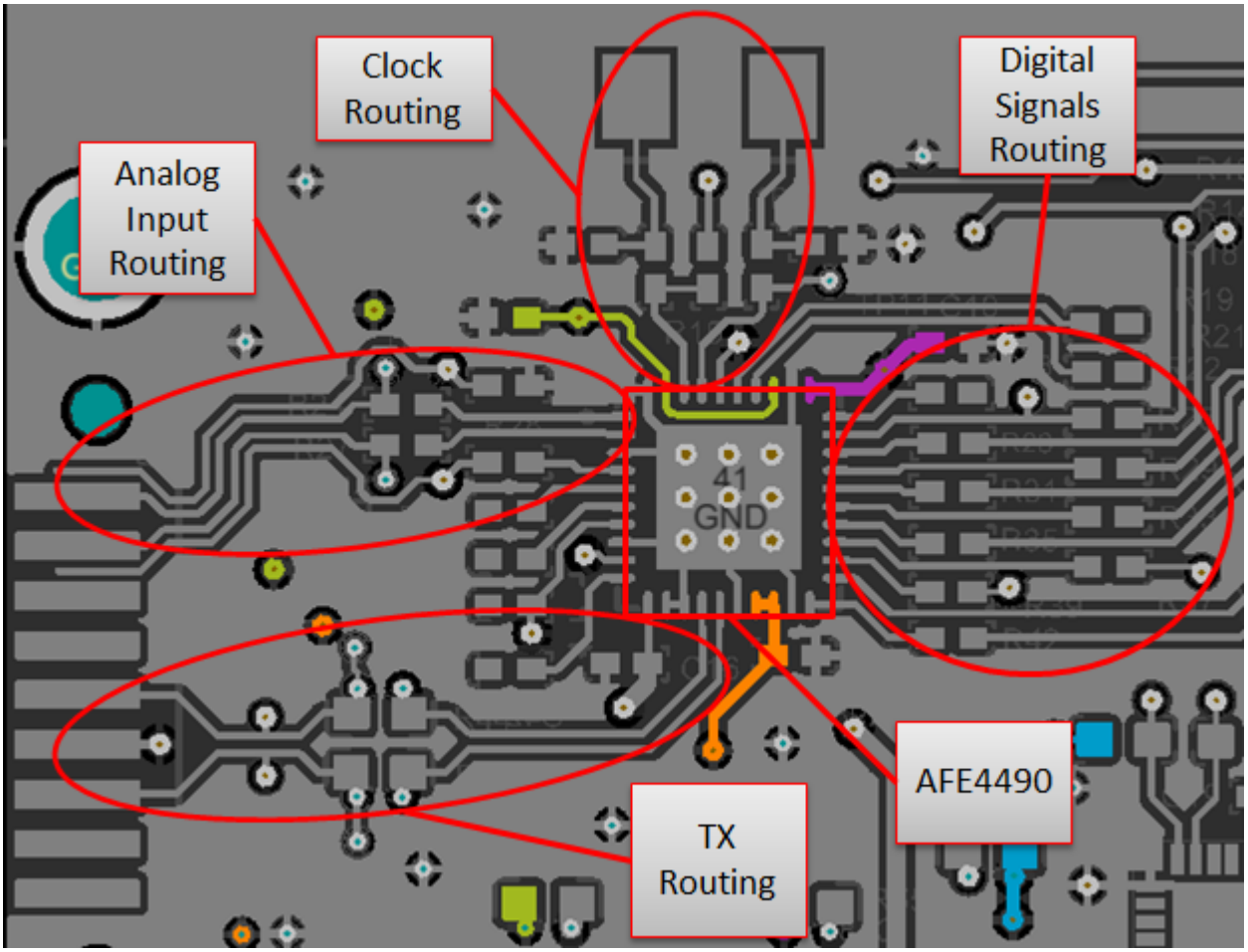


Figure 139. Typical Layout of the AFE4490 Board

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

AFE44x0SPO2EVM User's Guide, SLAU480

SpO Pulse Ox Wrist Oximeter Reference Design, TIDU124

12.2 Trademarks

SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE4490RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AFE4490	Samples
AFE4490RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AFE4490	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

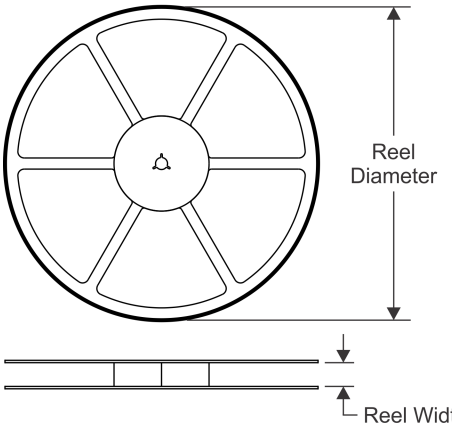
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

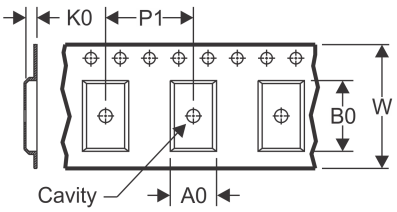
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

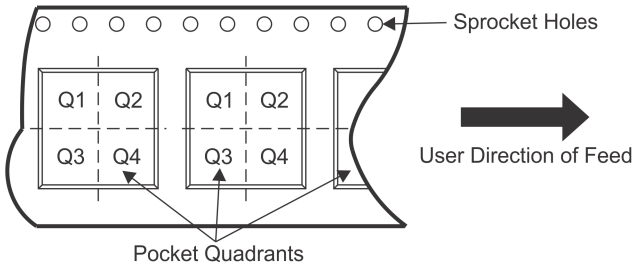


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

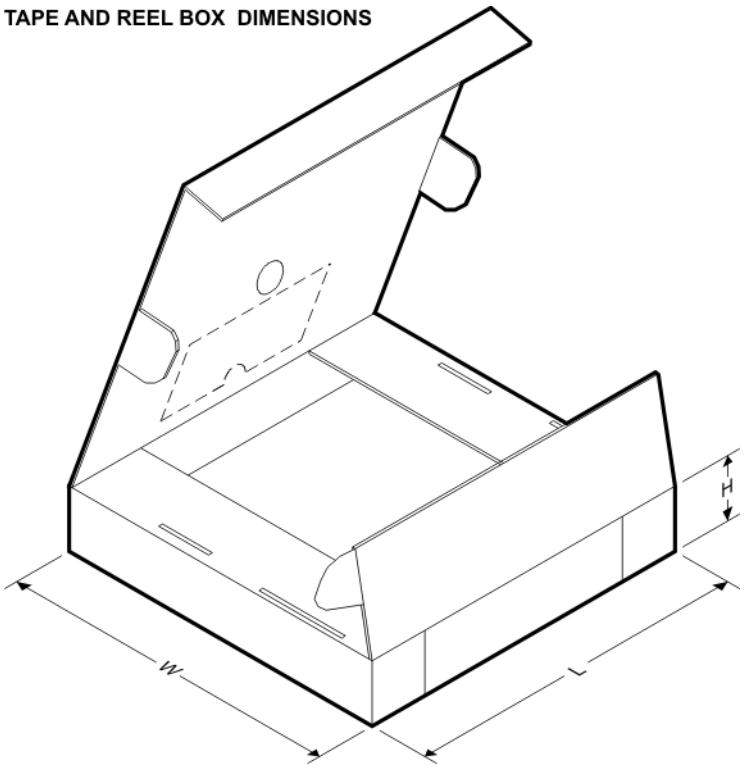
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE4490RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
AFE4490RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE4490RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
AFE4490RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

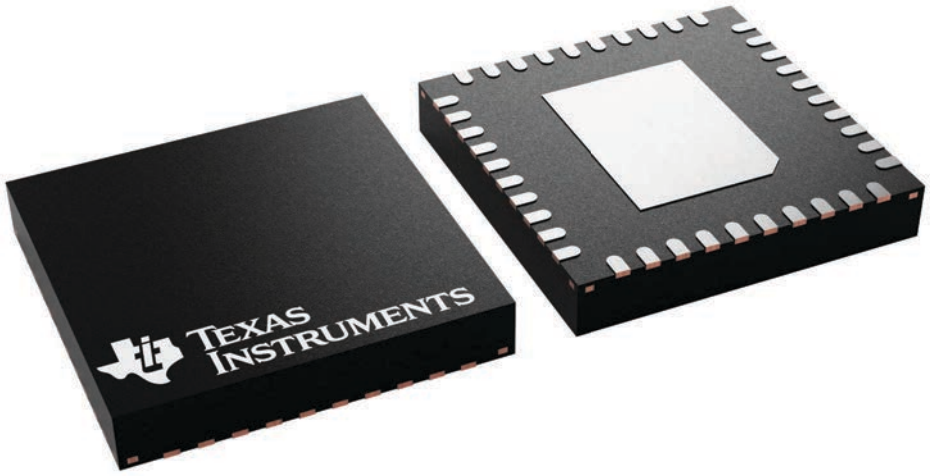
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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