THE DATASHEET OF

NSBC114TDXV6T1

www.win-source.net 0086-755-83957316

NSBC114EDXV6T1, NSBC114EDXV6T5

Preferred Devices

Dual Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSBC114EDXV6T1 series, two BRT devices are housed in the SOT−563 package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Lead−Free Solder Plating
- These are Pb−Free Devices

MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

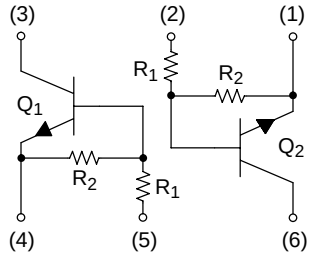
THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation; T_A = 25°C Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation; T_A = 25°C Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad

ON Semiconductor®

http://onsemi.com

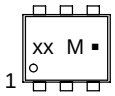


NSBC114EDXV6T1

MARKING DIAGRAM

1

SOT−563
CASE 463A
PLASTIC



xx = Device Code (Refer to Page 2)
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NSBC1xxxDXV6T1	SOT−563*	4000/Tape & Reel
NSBC1xxxDXV6T1G	SOT−563*	4000/Tape & Reel
NSBC1xxxDXV6T5	SOT−563*	8000/Tape & Reel
NSBC1xxxDXV6T5G	SOT−563*	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

© Semiconductor Components Industries, LLC, 2006

DEVICE MARKING, ORDERING, AND RESISTOR VALUES

Device†	Package*	Marking	R1 (kΩ)	R2 (kΩ)
NSBC114EDXV6T1	SOT−563	7A	10	10
NSBC124EDXV6T1	SOT−563	7B	22	22
NSBC144EDXV6T1	SOT−563	7C	47	47
NSBC114YDXV6T1	SOT−563	7D	10	47
NSBC114TDXV6T1 (Note 2)	SOT−563	7E	10	∞
NSBC143TDXV6T1 (Notes 2)	SOT−563	7F	4.7	∞
NSBC113EDXV6T1 (Note 2)	SOT−563	7G	1.0	1.0
NSBC123EDXV6T1 (Notes 2)	SOT−563	7H	2.2	2.2
NSBC143EDXV6T1 (Notes 2)	SOT−563	7J	4.7	4.7
NSBC143ZDXV6T1 (Notes 2)	SOT−563	7K	4.7	47
NSBC124XDXV6T1 (Notes 2)	SOT−563	7L	22	47
NSBC123JDXV6T1 (Note 2)	SOT−563	7M	2.2	47
NSBC115EDXV6T1 (Notes 2)	SOT−563	7N	100	100
NSBC144WDXV6T1 (Notes 2)	SOT−563	7P	47	22

†The “G’’ suffix indicates Pb−Free package available.
*This package is inherently Pb−Free.
2. New resistor combinations. Updated curves to follow in subsequent data sheets.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	NSBC114EDXV6T1	I_{EBO}	−	−	0.5	mAdc
	NSBC124EDXV6T1		−	−	0.2	
	NSBC144EDXV6T1		−	−	0.1	
	NSBC114YDXV6T1		−	−	0.2	
	NSBC114TDXV6T1		−	−	0.9	
	NSBC143TDXV6T1		−	−	1.9	
	NSBC113EDXV6T1		−	−	4.3	
	NSBC123EDXV6T1		−	−	2.3	
	NSBC143EDXV6T1		−	−	1.5	
	NSBC143ZDXV6T1		−	−	0.18	
	NSBC124XDXV6T1		−	−	0.13	
	NSBC123JDXV6T1		−	−	0.2	
	NSBC115EDXV6T1		−	−	0.05	
	NSBC144WDXV6T1		−	−	0.13	
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 4)						
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	NSBC114EDXV6T1	h_{FE}	35	60	–	
	NSBC124EDXV6T1		60	100	–	
	NSBC144EDXV6T1		80	140	–	
	NSBC114YDXV6T1		80	140	–	
	NSBC114TDXV6T1		160	350	–	
	NSBC143TDXV6T1		160	350	–	
	NSBC113EDXV6T1		3.0	5.0	–	
	NSBC123EDXV6T1		8.0	15	–	
	NSBC143EDXV6T1		15	30	–	
	NSBC143ZDXV6T1		80	200	–	
	NSBC124XDXV6T1		80	150	–	
	NSBC123JDXV6T1		80	140	–	
	NSBC115EDXV6T1		80	150	–	
	NSBC144WDXV6T1		80	140	–	
Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)		$V_{CE(sat)}$	–	–	0.25	Vdc
(I_C = 10 mA, I_B = 5 mA)	NSBC113EDXV6T1/NSBC123EDXV6T1					
(I_C = 10 mA, I_B = 1 mA)	NSBC114TDXV6T1/NSBC143TDXV6T1					
	NSBC143EDXV6T1/NSBC143ZDXV6T1/NSBC124XDXV6T1					
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	NSBC114EDXV6T1		–	–	0.2	
	NSBC124EDXV6T1		–	–	0.2	
	NSBC114YDXV6T1		–	–	0.2	
	NSBC114TDXV6T1		–	–	0.2	
	NSBC143TDXV6T1		–	–	0.2	
	NSBC113EDXV6T1		–	–	0.2	
	NSBC123EDXV6T1		–	–	0.2	
	NSBC143EDXV6T1		–	–	0.2	
	NSBC143ZDXV6T1		–	–	0.2	
	NSBC124XDXV6T1		–	–	0.2	
	NSBC123JDXV6T1		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	NSBC144EDXV6T1		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 5.5 V, R_L = 1.0 kΩ)	NSBC115EDXV6T1		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ)	NSBC144WDXV6T1		–	–	0.2	
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)		V_{OH}	4.9	–	–	Vdc
(V_{CC} = 5.0 V, V_B = 0.050 V, R_L = 1.0 kΩ)	NSBC113EDXV6T1					
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	NSBC114TDXV6T1					
	NSBC143TDXV6T1					
	NSBC143ZDXV6T1					
Input Resistor	NSBC114EDXV6T1	R1	7.0	10	13	k Ω
	NSBC124EDXV6T1		15.4	22	28.6	
	NSBC144EDXV6T1		32.9	47	61.1	
	NSBC114YDXV6T1		7.0	10	13	
	NSBC114TDXV6T1		7.0	10	13	
	NSBC143TDXV6T1		3.3	4.7	6.1	
	NSBC113EDXV6T1		0.7	1.0	1.3	
	NSBC123EDXV6T1		1.5	2.2	2.9	
	NSBC143EDXV6T1		3.3	4.7	6.1	
	NSBC143ZDXV6T1		3.3	4.7	6.1	
	NSBC124XDXV6T1		15.4	22	28.6	
	NSBC123JDXV6T1		1.54	2.2	2.86	
	NSBC115EDXV6T1		70	100	130	
	NSBC144WDXV6T1		32.9	47	61.1	
Resistor Ratio	NSBC114EDXV6T1/NSBC124EDXV6T1/ NSBC144EDXV6T1/NSBC115EDXV6T1	R1/R2	0.8	1.0	1.2	
	NSBC114YDXV6T1		0.17	0.21	0.25	
	NSBC114TDXV6T1/NSBC143TDXV6T1		–	–	–	
	NSBC113EDXV6T1/NSBC123EDXV6T1/NSBC143EDXV6T1		0.8	1.0	1.2	
	NSBC143ZDXV6T1		0.055	0.1	0.185	
	NSBC124XDXV6T1		0.38	0.47	0.56	
	NSBC123JDXV6T1		0.038	0.047	0.056	
	NSBC144WDXV6T1		1.7	2.1	2.6	

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

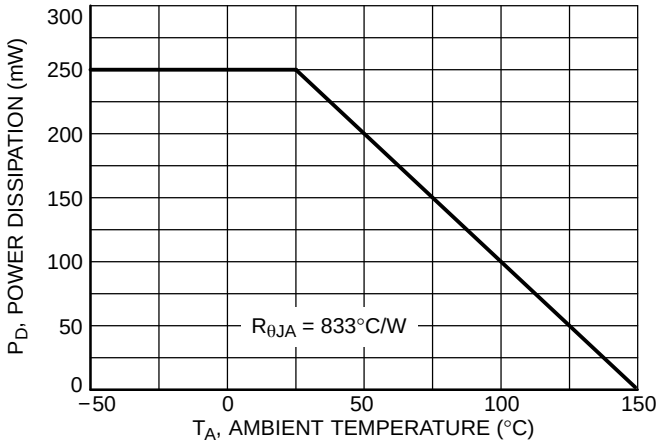


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS — NSBC114EDXV6T1

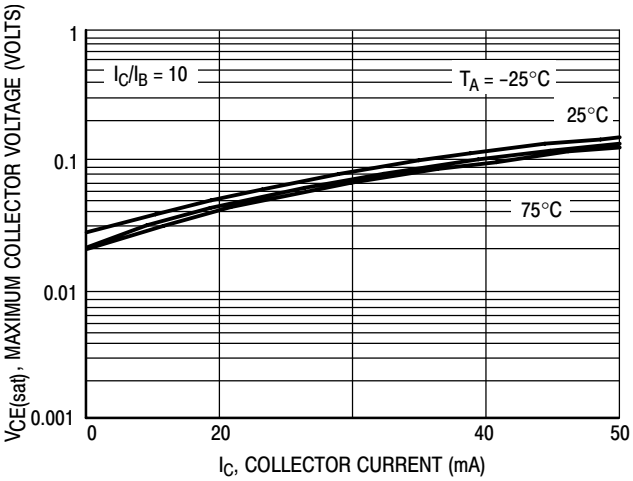


Figure 2. $V_{CE(sat)}$ versus I_C

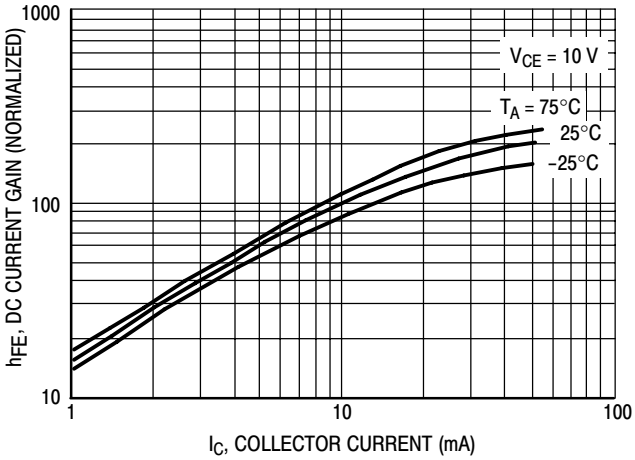


Figure 3. DC Current Gain

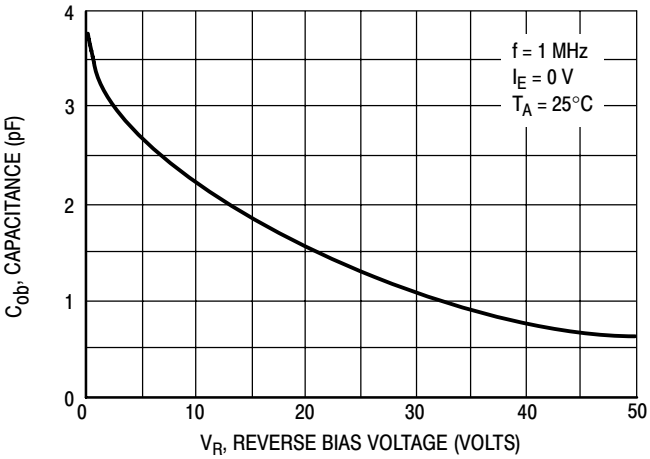


Figure 4. Output Capacitance

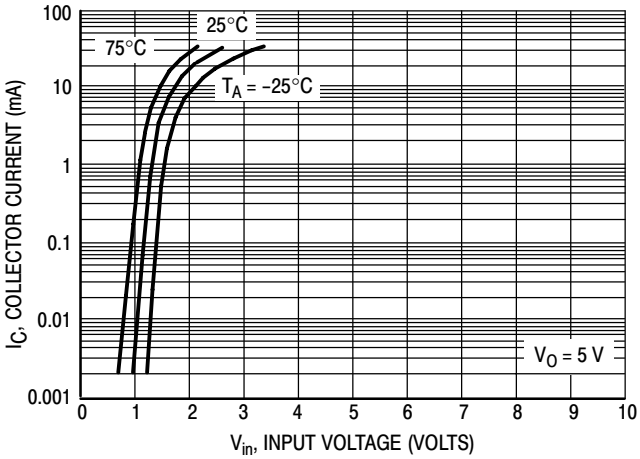


Figure 5. Output Current versus Input Voltage

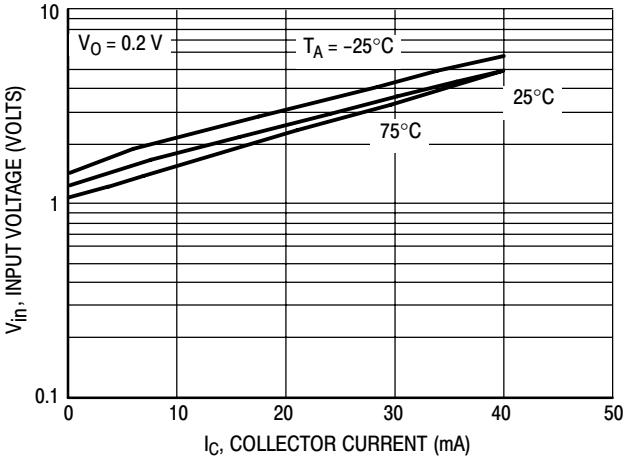


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBC124EDXV6T1

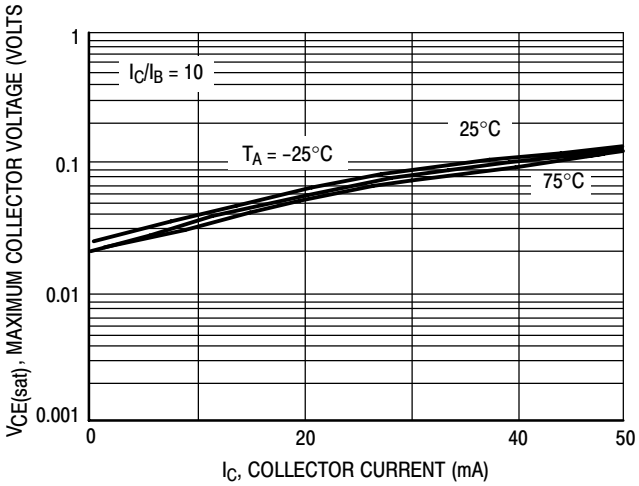


Figure 7. $V_{CE(sat)}$ versus I_C

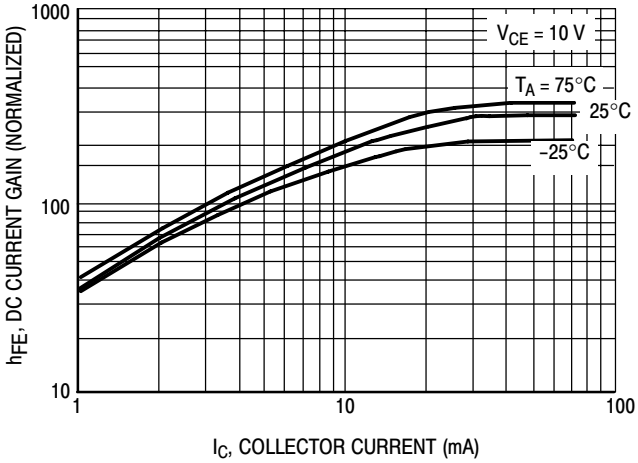


Figure 8. DC Current Gain

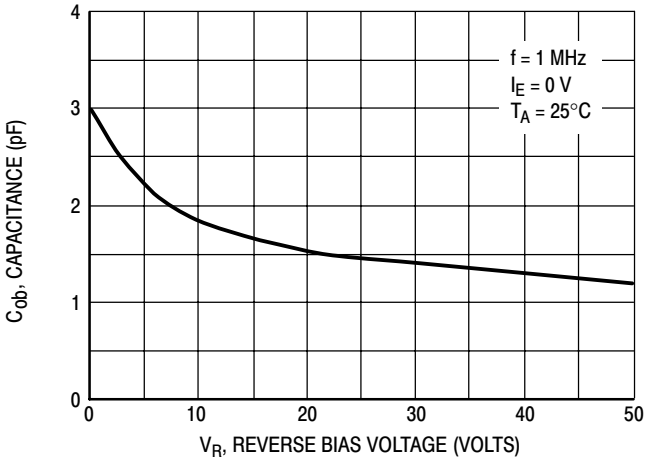


Figure 9. Output Capacitance

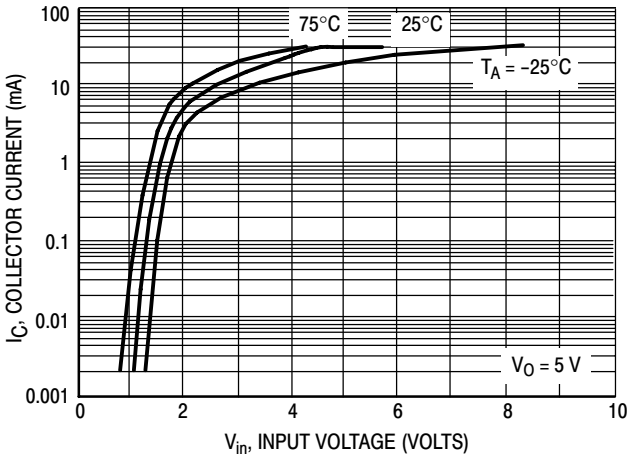


Figure 10. Output Current versus Input Voltage

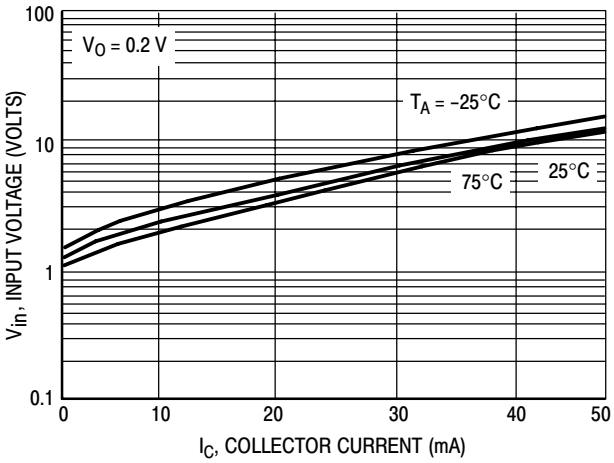


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBC144EDXV6T1

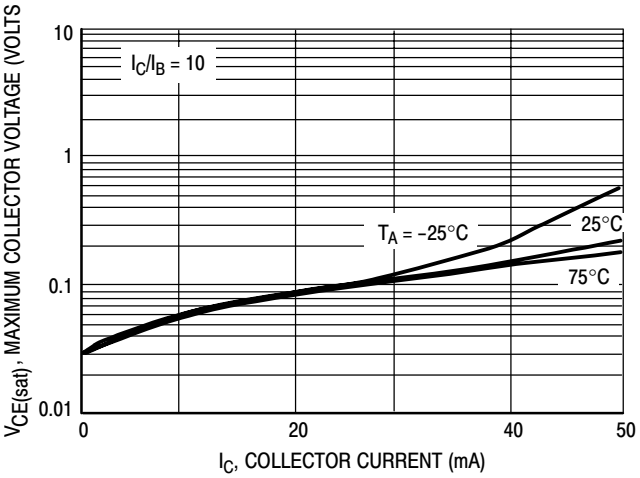


Figure 12. $V_{CE(sat)}$ versus I_C

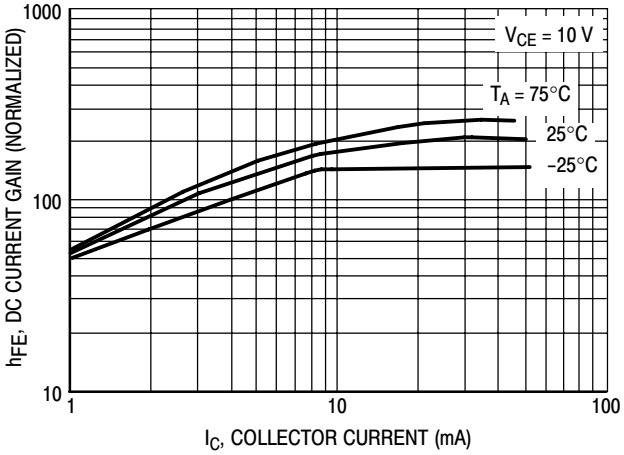


Figure 13. DC Current Gain

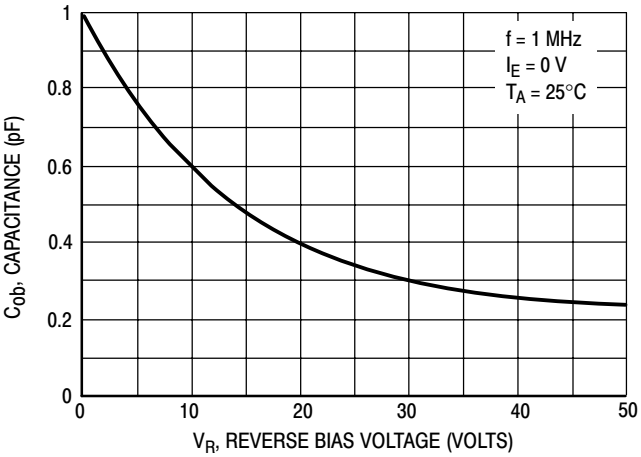


Figure 14. Output Capacitance

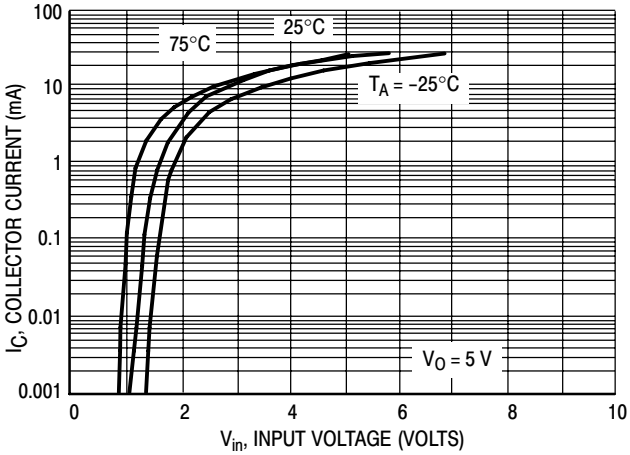


Figure 15. Output Current versus Input Voltage

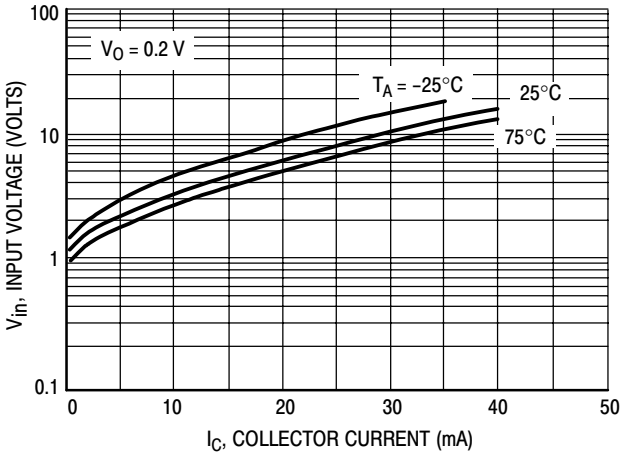


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBC114YDXV6T1

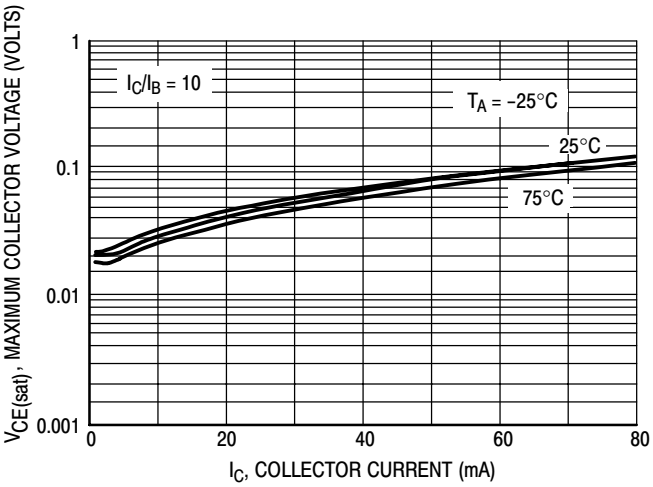


Figure 17. $V_{CE(sat)}$ versus I_C

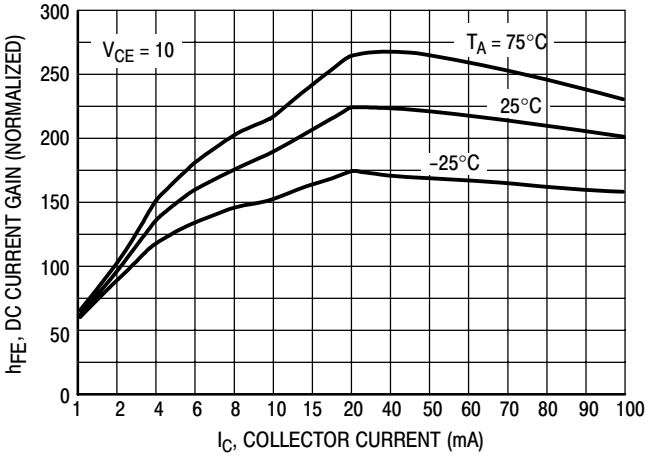


Figure 18. DC Current Gain

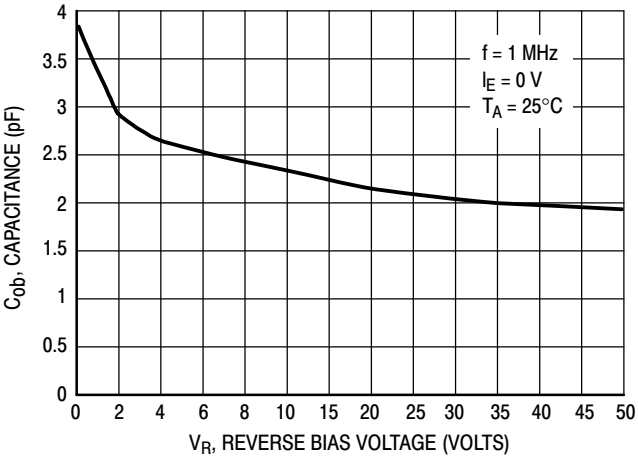


Figure 19. Output Capacitance

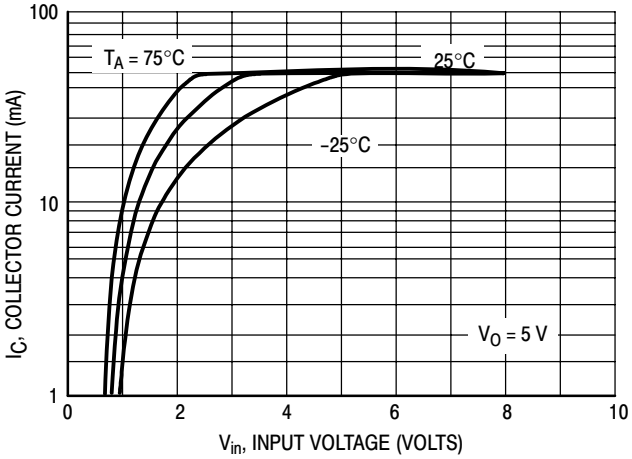


Figure 20. Output Current versus Input Voltage

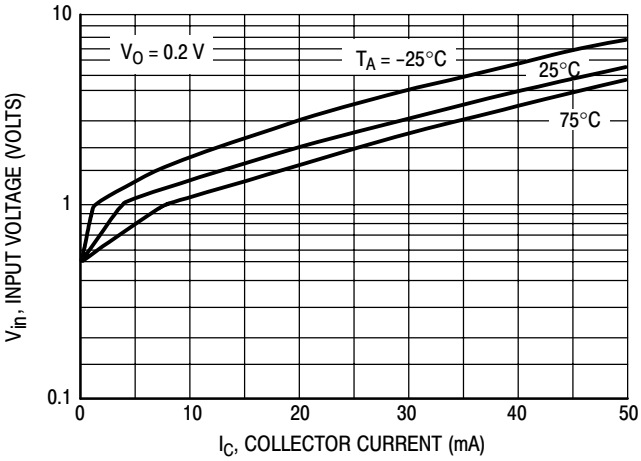
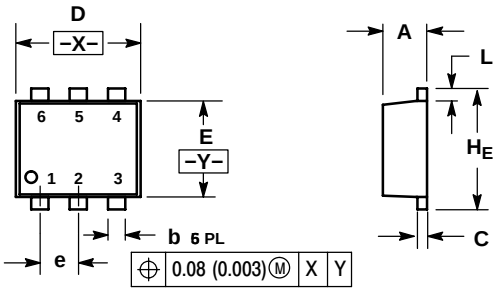


Figure 21. Input Voltage versus Output Current

PACKAGE DIMENSIONS

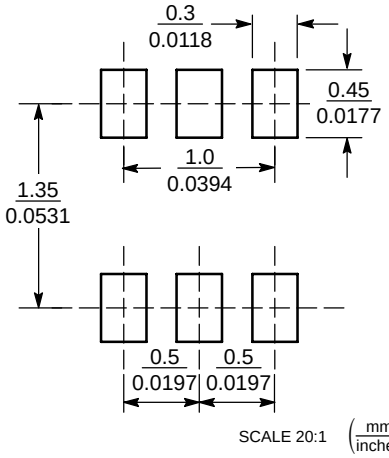
SOT−563, 6 LEAD
CASE 463A−01
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View NSBC114TDXV6T1 on WIN SOURCE
- ON Semiconductor Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management