THE DATASHEET OF

AD8479BRZ

www.win-source.net 0086-755-83957316

Very High Common-Mode Voltage Precision Difference Amplifier

Data Sheet **AD8479**

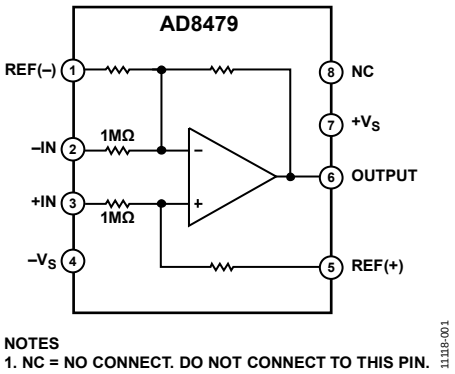
FEATURES

- ±600 V common-mode voltage range
- Rail-to-rail output
- Fixed gain of 1
- Wide power supply range of ±2.5 V to ±18 V
- 550 µA typical power supply current
- Excellent ac specifications
  - 90 dB minimum CMRR
  - 310 kHz bandwidth
- High accuracy dc performance
  - 5 ppm maximum gain nonlinearity
  - 10 µV/°C maximum offset voltage drift
  - 5 ppm/°C maximum gain drift

APPLICATIONS

- High voltage current sensing
- Battery cell voltage monitors
- Power supply current monitors
- Motor controls
- Isolation

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1.

GENERAL DESCRIPTION

The AD8479 is a difference amplifier with a very high input common-mode voltage range. The AD8479 is a precision device that allows the user to accurately measure differential signals in the presence of high common-mode voltages up to ±600 V.

The AD8479 can replace costly isolation amplifiers in applications that do not require galvanic isolation. The device operates over a ±600 V common-mode voltage range and has inputs that are protected from common-mode or differential mode transients up to ±600 V.

The AD8479 has low offset voltage, low offset voltage drift, low gain drift, low common-mode rejection drift, and excellent common-mode rejection ratio (CMRR) over a wide frequency range.

The AD8479 is available in a space-saving 8-lead SOIC package and is operational over the −40°C to +125°C temperature range.

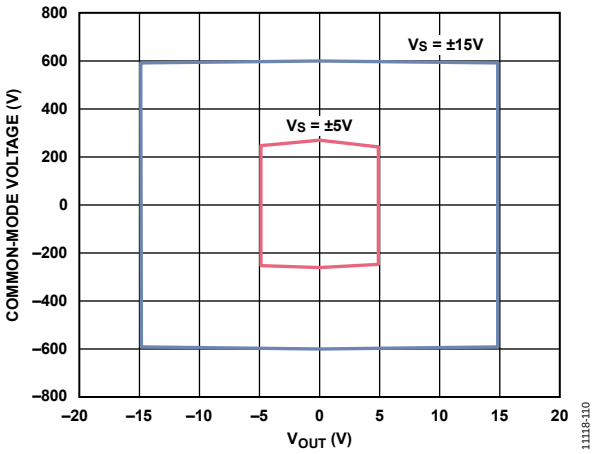


Figure 2. Input Common-Mode Voltage vs. Output Voltage

Rev. B
Document Feedback

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REVISION HISTORY

4/2019—Rev. A to Rev. B

Changes to Features Section ... 1
Changes to Specifications Section ... 3
Deleted Input Voltage Range Continuous, Table 2 ... 5
Added Thermal Resistance Section and Table 3, Renumbered Sequentially ... 5
Added Figure 3 and Figure 4, Renumbered Sequentially ... 5
Changes to Figure 6 to Figure 11 ... 7
Changes to Figure 12, Figure 16, and Figure 17 ... 8
Changes to Figure 20 to Figure 22 ... 9
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Added Figure 35 ... 11
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Changes to Ordering Guide ... 17

9/2015—Rev. 0 to Rev. A

Changes to Single-Supply Operation Section ... 12

4/2013—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V, REF(−) = REF(+) = 0 V, R_L = 2 kΩ, ambient temperature (T_A) = 25°C, unless otherwise noted.

Table 1.

		A Grade			B Grade			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
GAIN	V_{OUT} = ±10 V							
Nominal Gain			1			1		V/V
Gain Error[1]			0.01	0.02		0.005	0.01	%
Gain Nonlinearity			4	10		2	5	ppm
Gain Drift	$T_A = T_{MIN}$ to T_{MAX}		3	5		3	5	ppm/°C
OFFSET VOLTAGE								
Offset Voltage	V_S = ±15 V		0.5	3		0.5	1	mV
	V_S = ±5 V		0.5	3		0.5	1	mV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}		3	15		3	10	µV/°C
Power Supply Rejection Ratio (PSRR)	V_S = ±2.5 V to ±18 V	84	100		90	100		dB
INPUT								
Common-Mode Rejection Ratio (CMRR)[2]								
	T_A = 25°C, V_{CM} = ±10 V	80	90		90	96		dB
	Junction temperature (T_J) = 25°C, V_{CM} = ±600 V	80	90		90	96		dB
	T_J = 25°C, V_{CM} = 1200 V p-p, dc to 6 kHz	80			80			dB
CMRR Drift[2]	$T_J = T_{MIN}$ to T_{MAX}		−0.3	±1.5		−0.25	±1.3	ppm/°C
Operating Voltage Range	Common mode			±600			±600	V
	Differential			±14.7			±14.7	V
Input Operating Impedance	Common mode		500			500		kΩ
	Differential		2			2		MΩ
OUTPUT								
Output Voltage Swing		$-V_S$ + 0.3		$+V_S$ − 0.3	$-V_S$ + 0.3		$+V_S$ − 0.3	V
Output Short-Circuit Current			±55			±55		mA
Capacitive Load	Stable operation		500			500		pF
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth			310			310		kHz
Slew Rate			8.8			8.8		V/µs
Full Power Bandwidth	V_{OUT} = 20 V p-p		140			140		kHz
Settling Time	0.01%, V_{OUT} = 10 V step		5.9			5.9		µs
	0.001%, V_{OUT} = 10 V step		8.7			8.7		µs
OUTPUT VOLTAGE NOISE								
0.1 Hz to 10 Hz			30	40		30	40	µV p-p
Noise Spectral Density	100 Hz ≤ f ≤ 100 kHz		1.6			1.6		µV/√Hz

Parameter	Test Conditions/Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY								
Operating Voltage Range		±2.5		±18	±2.5		±18	V
Supply Current	V_{OUT} = 0 V		550	650		550	650	µA
	$T_A = T_{MIN}$ to T_{MAX}		850			850		µA
TEMPERATURE RANGE								
Specified Performance	$T_A = T_{MIN}$ to T_{MAX}	−40		+85	−40		+85	°C
Operational		−40		+125	−40		+125	°C

[1] See Figure 35 for gain error shift over lifetime.
[2] T_J is affected by V_{CM}. Use the values in Table 3 and the data shown in Figure 3 when estimating T_J.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_S	±18 V
Input Voltage Range, Common-Mode and Differential	
Continuous	600 V (magnitude)
10 sec	900 V (magnitude)
Output Short-Circuit Duration	Indefinite
REF(–) and REF(+)	$–V_S$ – 0.3 V to $+V_S$ + 0.3 V
Maximum Junction Temperature	150°C
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Ψ_{JT} is the junction-to-top-of-package characterization parameter.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	Ψ_{JT}	Unit
R-8	151.4	2.5	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board for θ_{JA} and Ψ_{JT}. See JEDEC JESD-51.

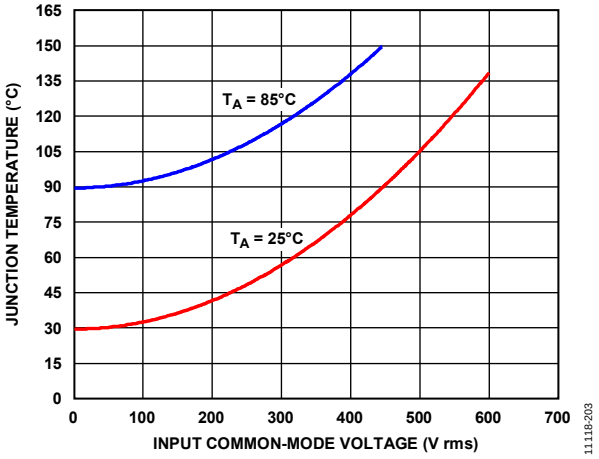


Figure 3. Junction Temperature (T_J) vs. Input Common-Mode Voltage

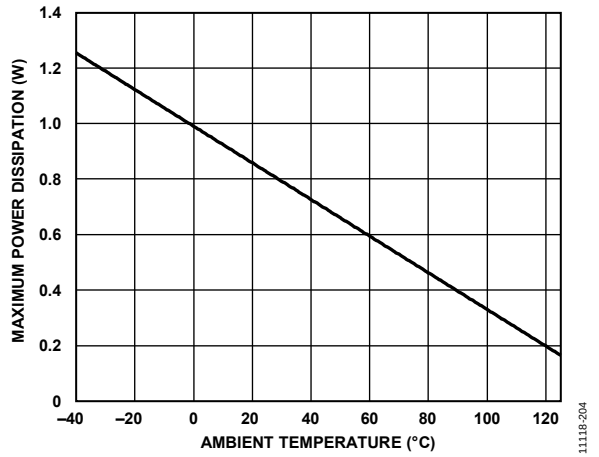
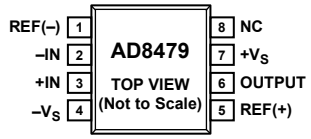


Figure 4. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

11118-002

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	REF(−)	Negative Reference Voltage Input.
2	−IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply Voltage.
5	REF(+)	Positive Reference Voltage Input.
6	OUTPUT	Output.
7	$+V_S$	Positive Supply Voltage.
8	NC	No Connect. Do not connect to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15 V, T_A = 25°C, unless otherwise noted.

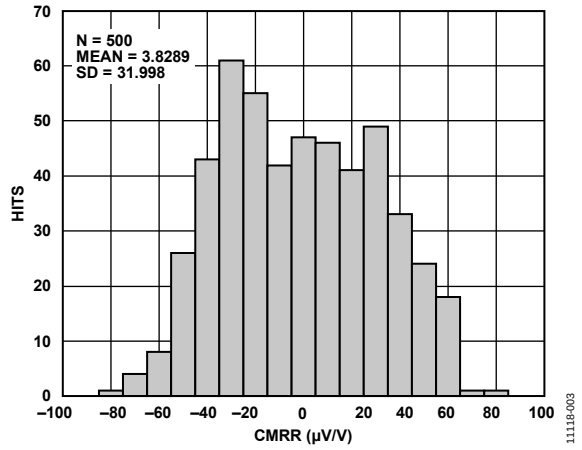


Figure 6. CMRR Distribution

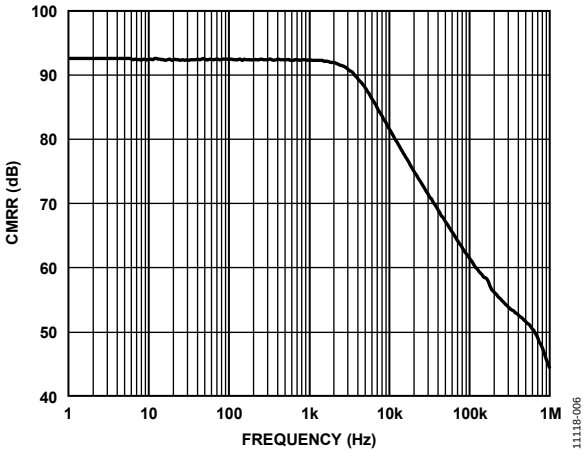


Figure 9. CMRR vs. Frequency

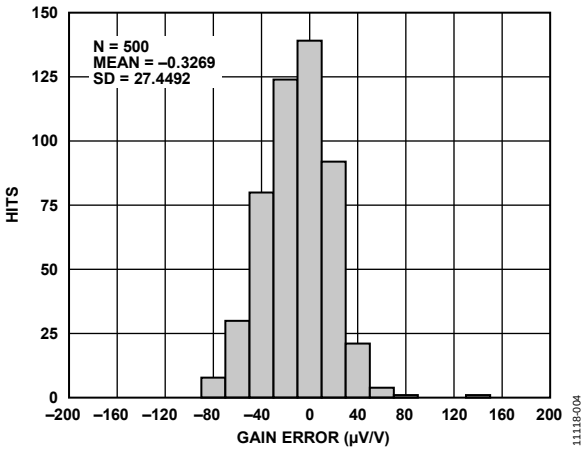


Figure 7. Gain Error Distribution

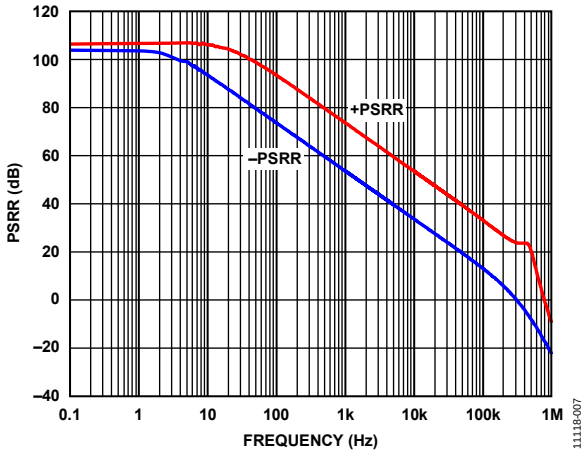


Figure 10. PSRR vs. Frequency

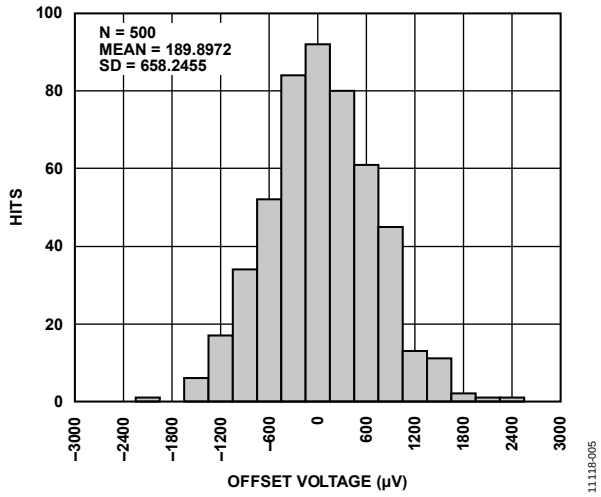


Figure 8. Offset Voltage Distribution

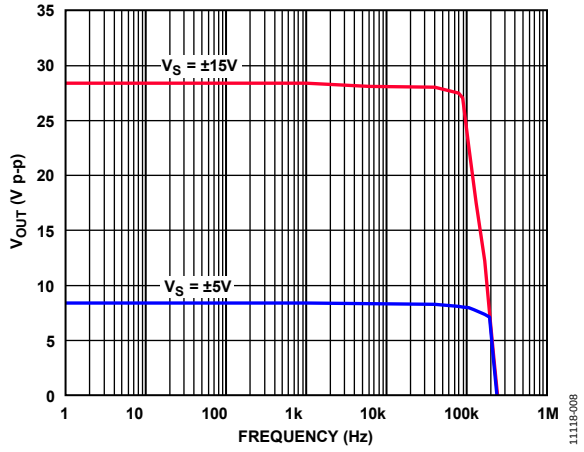


Figure 11. Large Signal Frequency Response

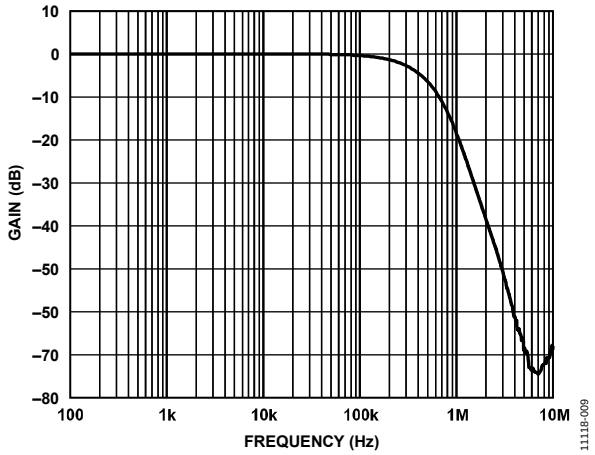


Figure 12. Small Signal Frequency Response

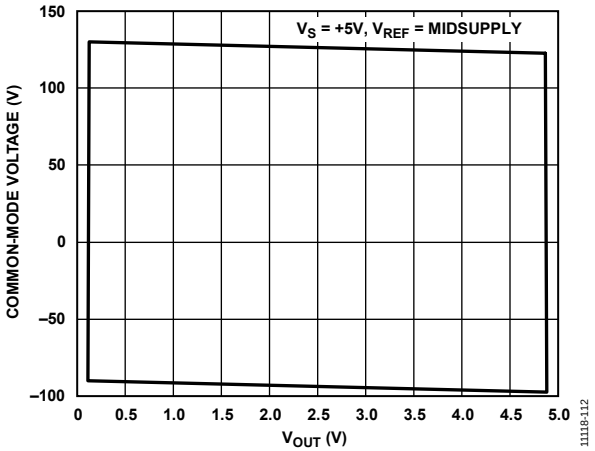


Figure 15. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = +5 V, V_{REF} = Midsupply

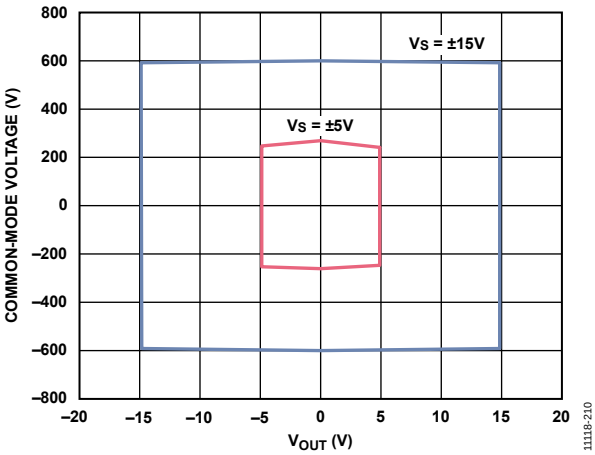


Figure 13. Input Common-Mode Voltage vs. Output Voltage, Dual Supplies, V_S = ±15 V, ±5 V

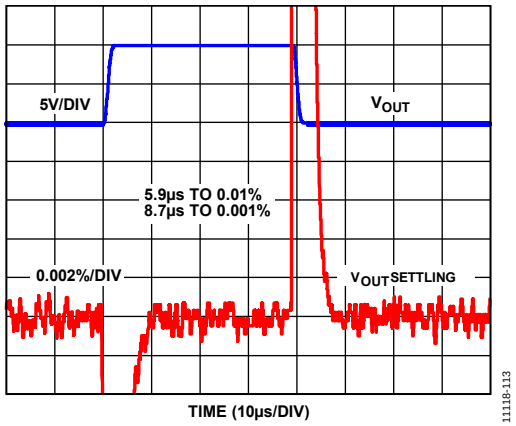


Figure 16. Settling Time

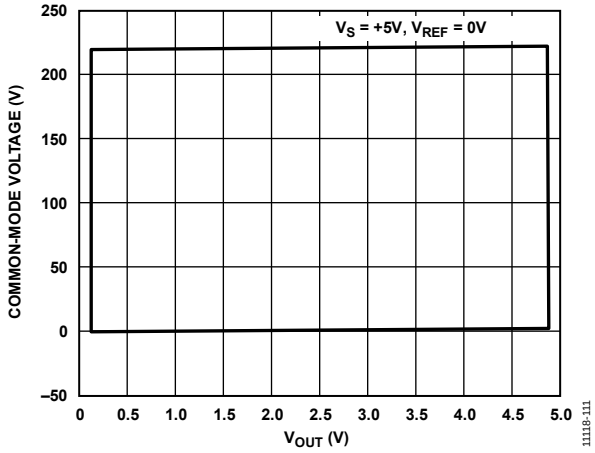


Figure 14. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = +5 V, V_{REF} = 0 V

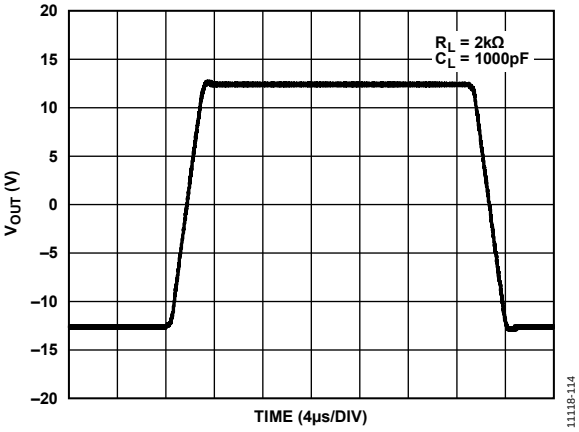


Figure 17. Large Signal Pulse Response

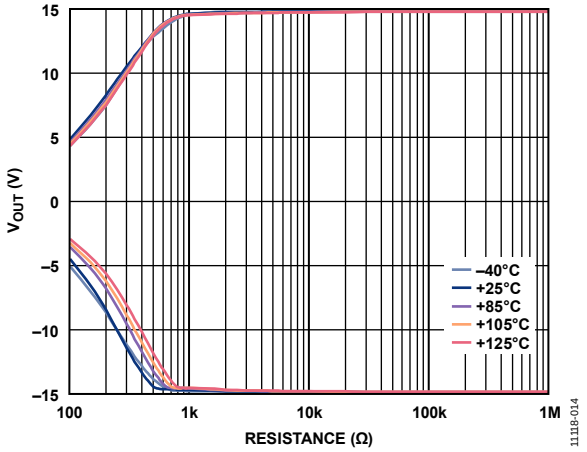


Figure 18. Output Voltage vs. Load over Temperature

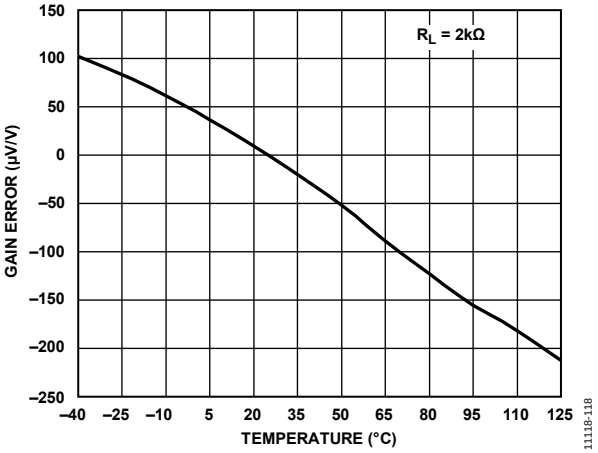


Figure 21. Gain Drift

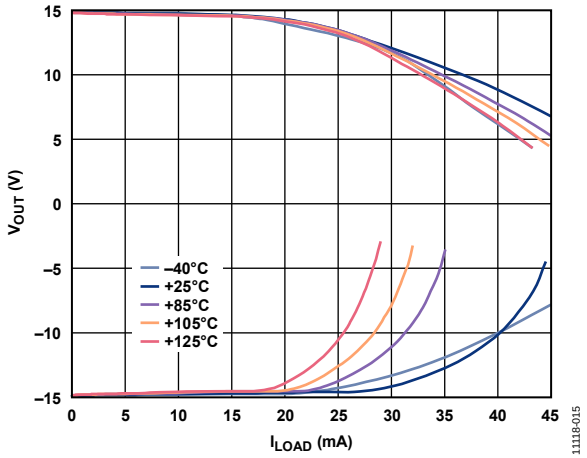


Figure 19. Output Voltage vs. Output Current over Temperature

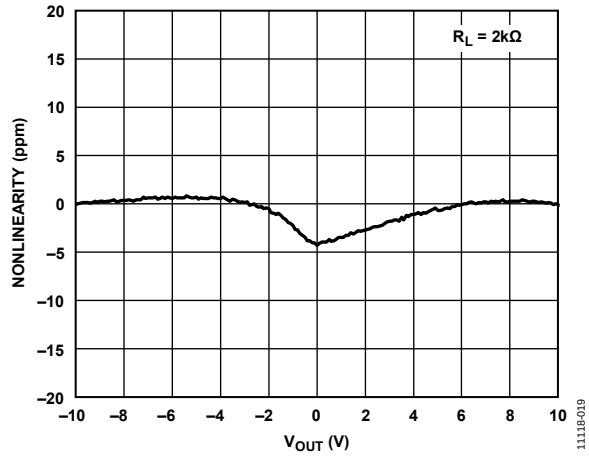


Figure 22. Gain Nonlinearity

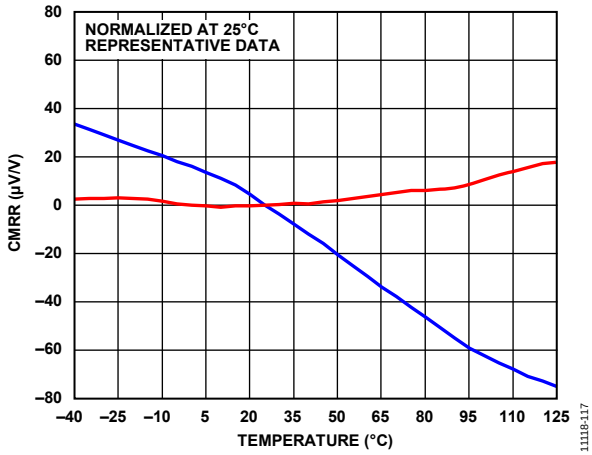


Figure 20. CMRR vs. Temperature, V_{CM} = ±20 V

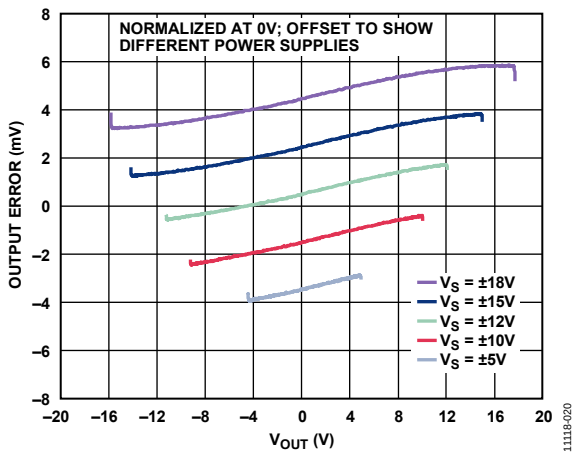


Figure 23. Output Error vs. Output Voltage, R_L = 10 kΩ

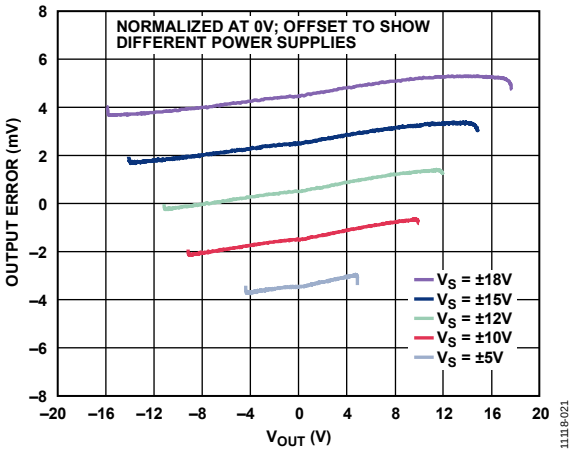


Figure 24. Output Error vs. Output Voltage, R_L = 2 kΩ

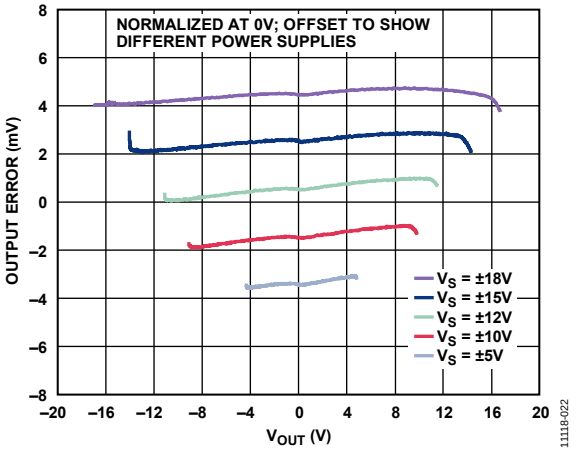


Figure 25. Output Error vs. Output Voltage, R_L = 1 kΩ

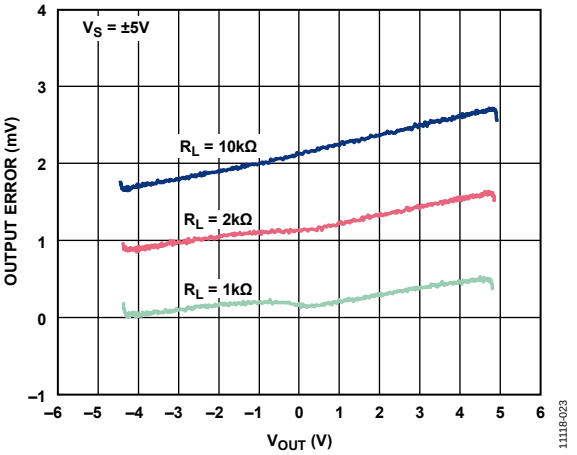


Figure 26. Output Error vs. Output Voltage, V_S = ±5 V

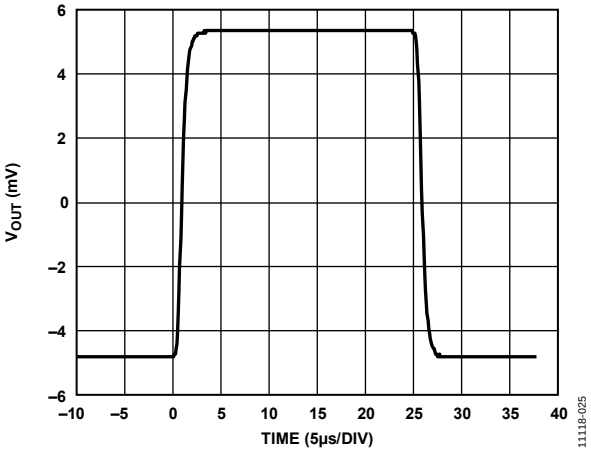


Figure 27. Small Signal Pulse Response

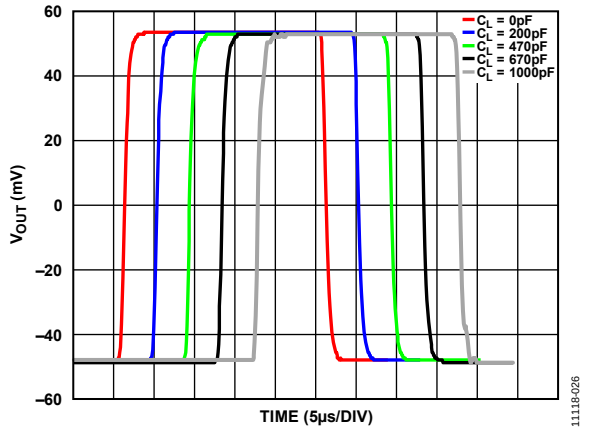


Figure 28. Small Signal Pulse Response vs. Capacitive Load

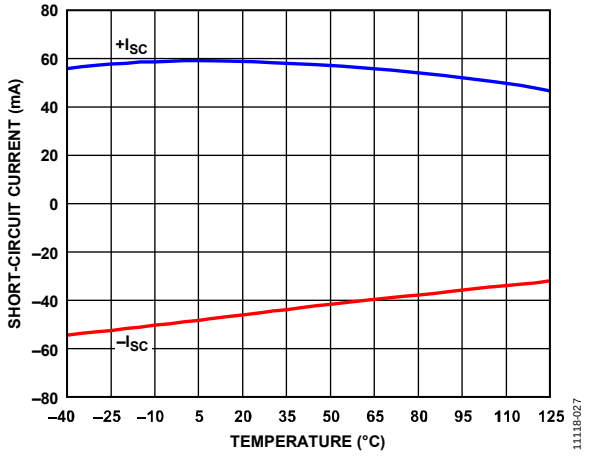


Figure 29. Short-Circuit Current vs. Temperature

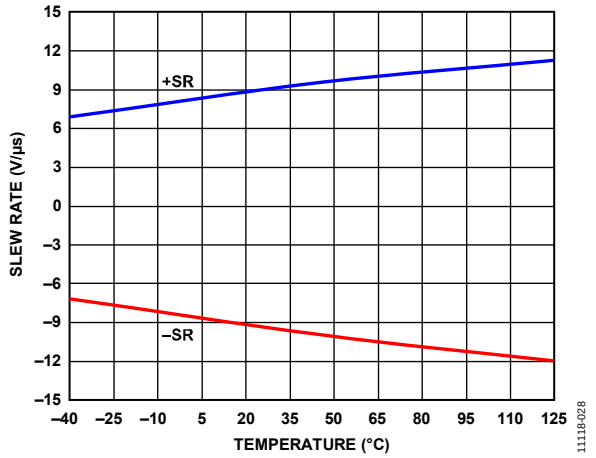


Figure 30. Slew Rate vs. Temperature

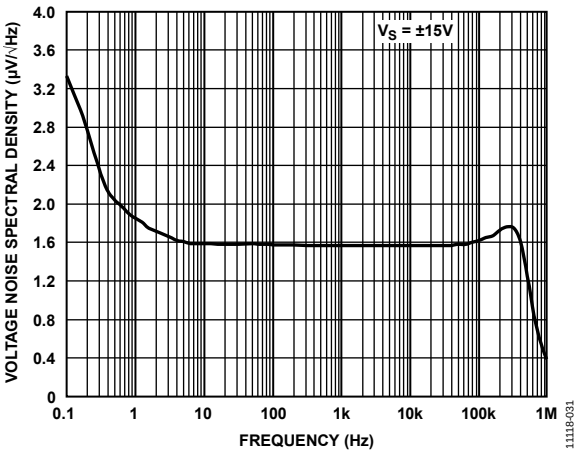


Figure 33. Voltage Noise Spectral Density vs. Frequency

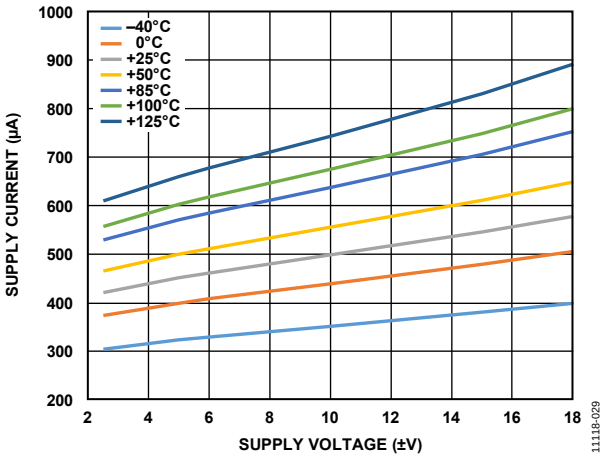


Figure 31. Supply Current vs. Supply Voltage

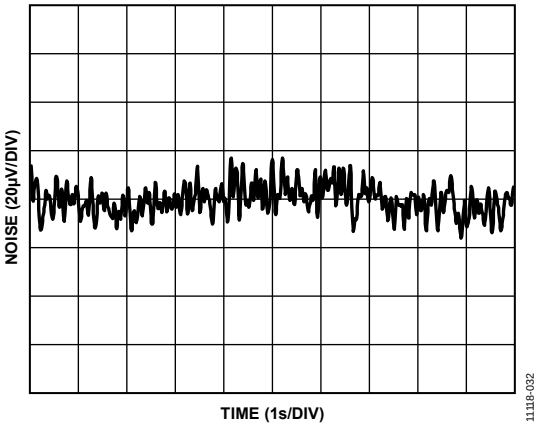


Figure 34. 0.1 Hz to 10 Hz Noise

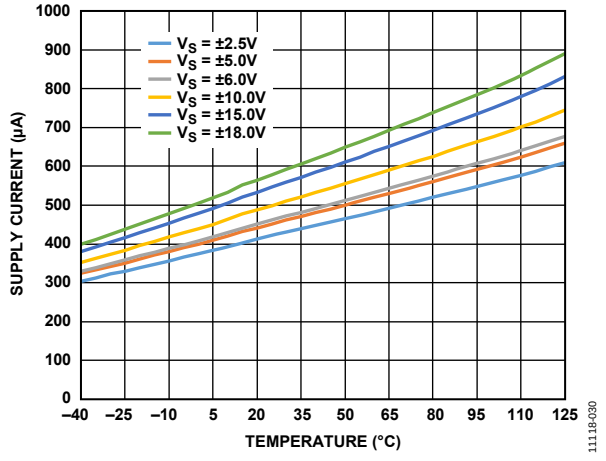


Figure 32. Supply Current vs. Temperature

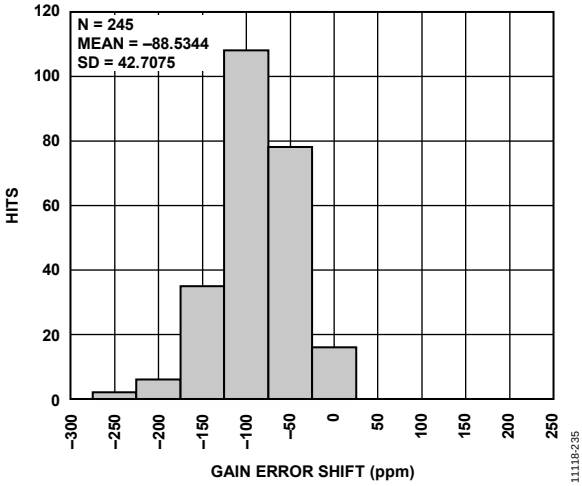


Figure 35. Gain Error Shift (ppm) Over Lifetime;
1000 Hours High Temperature Operating Life (HTOL) at ±600 V_{CM}, 125°C
Per JESD22-A108

THEORY OF OPERATION

The AD8479 is a unity-gain, differential-to-single-ended amplifier that can reject extremely high common-mode signals up to 600 V with ±15 V supplies. The AD8479 consists of an operational amplifier (op amp) and a resistor network (see Figure 36).

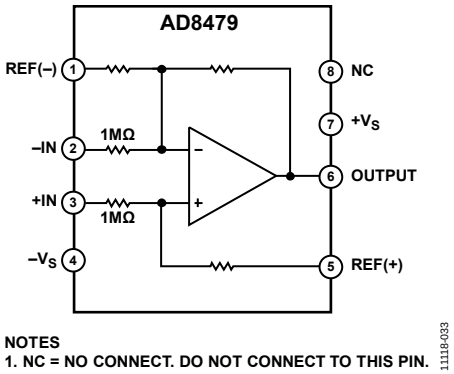


Figure 36. Functional Block Diagram

To achieve the high common-mode voltage range, an internal resistor divider—connected to Pin 3 and Pin 5—attenuates the noninverting signal by a factor of 60. The internal resistors at Pin 1 and Pin 2, as well as the feedback resistor, restore the gain to provide a differential gain of unity.

The complete transfer function is

$$V_{OUT} = V\,(+IN) - V\,(-IN)$$

Laser wafer-trimming provides resistor matching so that common-mode signals are rejected and differential input signals are amplified.

To reduce output voltage drift, the op amp uses super beta transistors in its input stage. The input offset current and its associated temperature coefficient contribute no appreciable output voltage offset or drift, which has the added benefit of reducing voltage noise because the corner where 1/f noise becomes dominant is below 5 Hz. To reduce the dependence of gain accuracy on the op amp, the open-loop voltage gain of the op amp exceeds 20 million V/V, and the PSRR exceeds 90 dB.

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APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 37 shows the basic connections for operating the AD8479 with a dual supply. A supply voltage from ±2.5 V to ±18 V is applied across Pin 7 and Pin 4. Both supplies should be decoupled close to the pins using 0.1 µF capacitors. Electrolytic capacitors of 10 µF, also located close to the supply pins, may be required if low frequency noise is present on the power supply. Although multiple amplifiers can be decoupled by a single set of 10 µF capacitors, each AD8479 should have its own set of 0.1 µF capacitors so that the decoupling point can be located directly at the IC power pins.

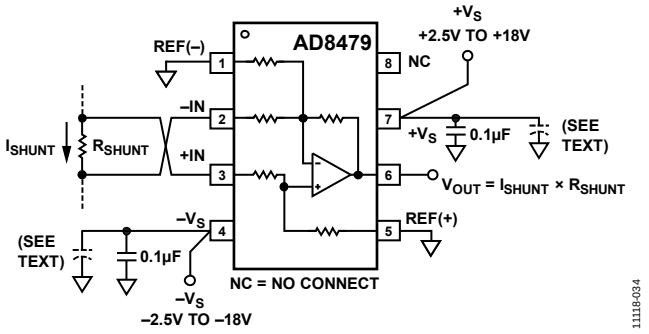

Figure 37. Basic Connections

The differential input signal, which typically results from a load current flowing through a small shunt resistor, is applied to Pin 2 and Pin 3 with the polarity shown in Figure 37 to obtain a positive gain. The common-mode voltage on the differential input signal can range from −600 V to +600 V, and the maximum differential voltage is ±14.7 V. When configured as shown in Figure 37, the device operates as a simple gain-of-1, differential-to-single-ended amplifier where the output voltage is the shunt resistance times the shunt current. The output is measured with respect to Pin 1 and Pin 5.

Pin 1 and Pin 5 (REF(−) and (REF(+)) should be grounded for a gain of unity and connected to the same low impedance ground plane. Failure to do this results in degraded common-mode rejection. Pin 8 is a no connect pin and should be left open.

SINGLE-SUPPLY OPERATION

Figure 38 shows the connections for operating the AD8479 with a single supply. Because the output can swing to within only about 0.3 V of either rail, an offset must be applied to the output. This offset can be applied by connecting REF(+) and REF(−) to a low impedance reference voltage that is capable of sinking current (some ADCs provide this voltage as an output). Therefore, for a single supply of 10 V, V_{REF} can be set to 5 V for a bipolar input signal, allowing the output to swing 9.4 V p-p around the central 5 V reference voltage. For unipolar input signals, V_{REF} can be set to approximately 1 V, allowing the output to swing from 1 V (for a 0 V input) to within 0.3 V of the positive rail.

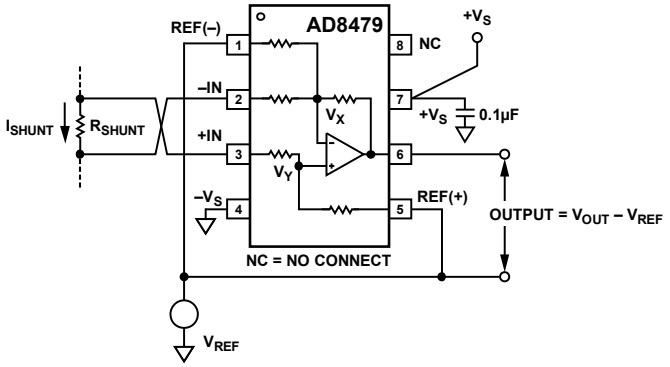

Figure 38. Operation with a Single Supply

When the AD8479 is operated with a single supply and a reference voltage is applied to REF(+) and REF(−), the input common-mode voltage range of the AD8479 is reduced. The reduced input common-mode range depends on the voltage at the inverting and noninverting inputs of the internal op amp, labeled V_X and V_Y in Figure 38. These nodes can swing to within 1 V of either rail. Therefore, for a single supply voltage of 10 V, V_X and V_Y can have a value from 1 V to 9 V. If V_{REF} is set to 5 V, the allowable common-mode voltage range is +245 V to −235 V. The common-mode voltage range can be calculated as follows:

$$V_{CM}(\pm) = 60 \times (V_X \text{ or } V_Y(\pm)) - (59 \times V_{REF})$$

SYSTEM-LEVEL DECOUPLING AND GROUNDING

The use of ground planes is recommended to minimize the impedance of ground returns and, therefore, the size of dc errors. Figure 39 shows how to use grounding in a mixed-signal environment, that is, with digital and analog signals present. To isolate low level analog signals from a noisy digital environment, many data acquisition components have separate analog and digital ground returns. All ground pins from mixed-signal components, such as ADCs, should return through a low impedance analog ground plane. Digital ground lines of mixed-signal converters should also be connected to the analog ground plane.

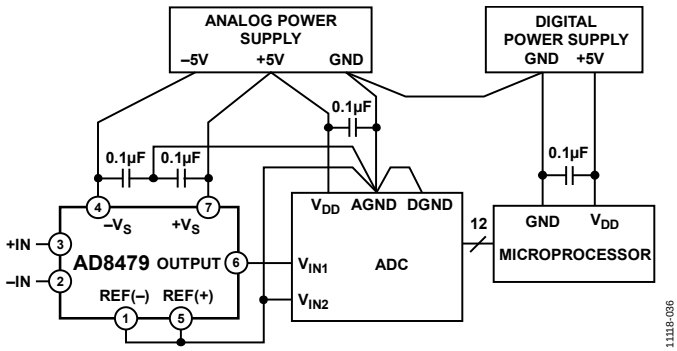

Figure 39. Optimal Grounding Practice for a Dual Supply Environment with Separate Analog and Digital Supplies

Typically, analog and digital grounds should be separated. At the same time, however, the voltage difference between digital and analog grounds on a converter must also be minimized to keep this difference as small as possible (typically <0.3 V). The increased noise—caused by the digital return currents of the converter flowing through the analog ground plane—is typically negligible.

Maximum isolation between analog and digital signals is achieved by connecting the ground planes back to the supplies. Note that Figure 39 suggests a star ground system for the analog circuitry, with all ground lines connected, in this case, to the analog ground of the ADC. However, when ground planes are used, it is sufficient to connect ground pins to the nearest point on the low impedance ground plane.

If only one power supply is available, it must be shared by both digital and analog circuitry. Figure 40 shows how to minimize interference between the digital and analog circuitry. In Figure 40, the reference of the ADC is used to drive the REF(+) and REF(−) pins of the AD8479. Therefore, the reference must be capable of sourcing and sinking a current equal to V_{CM}/500 kΩ.

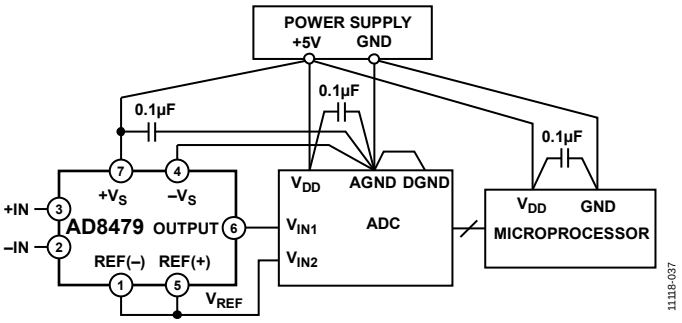

Figure 40. Optimal Grounding Practice for a Single-Supply Environment

As in the dual-supply environment, separate analog and digital ground planes should be used (although reasonably thick traces can be used as an alternative to a digital ground plane). These ground planes should connect at the ground pin of the power supply. Separate traces (or power planes) should run from the power supply to the supply pins of the digital and analog circuits. Ideally, each device should have its own power supply trace, but these traces can be shared by a number of devices, as long as a single trace is not used to route current to both digital and analog circuitry.

USING A LARGE SHUNT RESISTOR

The insertion of a large value shunt resistor across the input pins, Pin 2 and Pin 3, unbalances the input resistor network, thereby introducing common-mode error. The magnitude of the error depends on the common-mode voltage and the magnitude of the shunt resistor (R_{SHUNT}).

Table 5 shows some sample error voltages generated by a common-mode voltage of 600 V dc with shunt resistors from 20 Ω to 2000 Ω. Assuming that the shunt resistor is selected to use the full ±10 V output swing of the AD8479, the error voltage becomes quite significant as the value of R_{SHUNT} increases.

Table 5. Error Resulting from Large Values of R_{SHUNT} (Uncompensated Circuit)

R_{SHUNT} (Ω)	Error V_{OUT} (V)	Error Indicated (mA)
20	0.012	0.6
1000	0.583	0.6
2000	1.164	0.6

To measure low current or current near zero in a high common-mode voltage environment, an external resistor equal to the shunt resistor value can be added to the low impedance side of the shunt resistor, as shown in Figure 41.

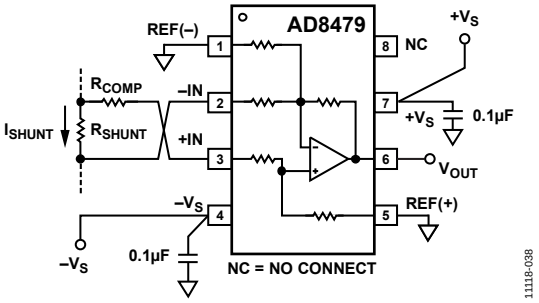

Figure 41. Compensating for Large Shunt Resistors

OUTPUT FILTERING

To limit noise at the output, a simple two-pole, low-pass Butterworth filter can be implemented using the ADA4077-2 after the AD8479, as shown in Figure 42.

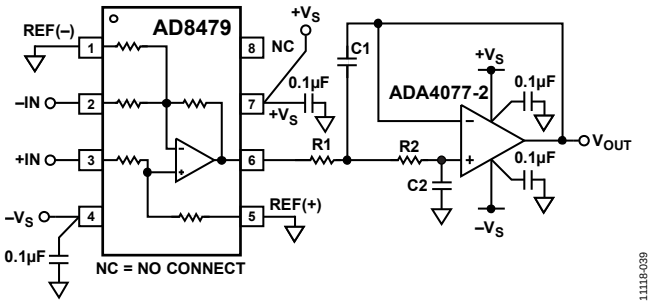

Figure 42. Filtering Output Noise Using a Two-Pole Butterworth Filter

Table 6 provides recommended component values for various corner frequencies and the peak-to-peak output noise for each case.

GAIN OF 60 DIFFERENTIAL AMPLIFIER

Low level signals can be connected directly to the –IN and +IN inputs of the AD8479. Differential input signals can also be connected to give a precise gain of 60 (see Figure 43); however, large common-mode voltages are no longer permissible. Cold junction compensation can be implemented using a temperature sensor, such as the AD590.

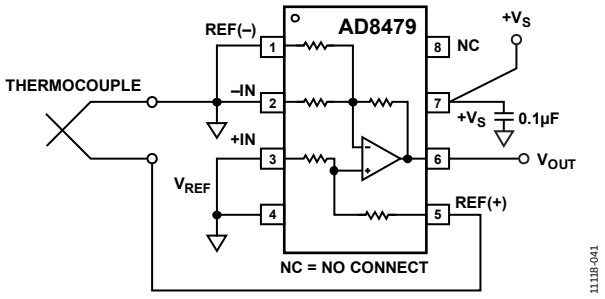

Figure 43. Gain of 60 Thermocouple Amplifier

Table 6. Recommended Values for Two-Pole Butterworth Filter

Corner Frequency	R1	R2	C1	C2	Output Noise (p-p)
50 kHz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	2.2 nF ± 10%	1 nF ± 10%	2.9 mV
5 kHz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	22 nF ± 10%	10 nF ± 10%	0.9 mV
500 Hz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	220 nF ± 10%	0.1 µF ± 10%	0.296 mV
50 Hz	2.7 kΩ ± 10%	1.58 kΩ ± 10%	2.2 µF ± 20%	0.1 µF ± 20%	0.095 mV
No Filter					4.7 mV

ERROR BUDGET ANALYSIS EXAMPLE

In the dc application described in this section, the 10 A output current from a device with a high common-mode voltage (such as a power supply or current-mode amplifier) is sensed across a 1 Ω shunt resistor (see Figure 44). The common-mode voltage is 600 V, and the resistor terminals are connected through a long pair of lead wires located in a high noise environment, for example, 50 Hz/60 Hz, 440 V ac power lines.

The calculations in Table 7 assume an induced noise level of 1 V p-p at 60 Hz on the lead wires, in addition to a full-scale dc differential voltage of 10 V. The error budget table quantifies the contribution of each error source. Note that the dominant error source in this example is due to the dc common-mode voltage.

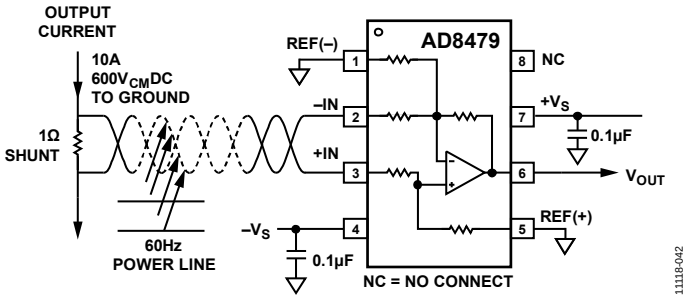

Figure 44. Error Budget Analysis Example: V_{IN} = 10 V Full Scale, V_{CM} = 600 V DC, R_{SHUNT} = 1 Ω, 1 V p-p, 60 Hz Power Line Interference

Table 7. Error Budget Analysis Example (V_{CM} = 600 V DC)

Error Source	Calculation of Error	Error (ppm of FS)
ACCURACY, T_A = 25°C		
Initial Gain Error	(0.0001 × 10)/10 V × 10^6	100
Offset Voltage	(0.001 V/10 V) × 10^6	100
DC CMRR	(32 × 10^{-6} × 600 V)/10 V × 10^6	1920
	Total Accuracy Error	2120
TEMPERATURE DRIFT (85°C)		
Gain Drift	5 ppm/°C × 60°C	300
Offset Voltage Drift	(10 µV/°C × 60°C) × 10^6/10 V	60
DC CMRR	1.3 ppm/°C × 60°C	78
	Total Temperature Drift Error	438
RESOLUTION		
Noise, Maximum, 0.1 Hz to 10 Hz, µV p-p	40 µV/10 V × 10^6	4
CMRR, 60 Hz	(32 × 10^{-6} × 1 V)/10 V × 10^6	3
Nonlinearity	(5 × 10^{-6} × 10 V)/10 V × 10^6	5
	Total Resolution Error	12
TOTAL	Total Error	2570

OUTLINE DIMENSIONS

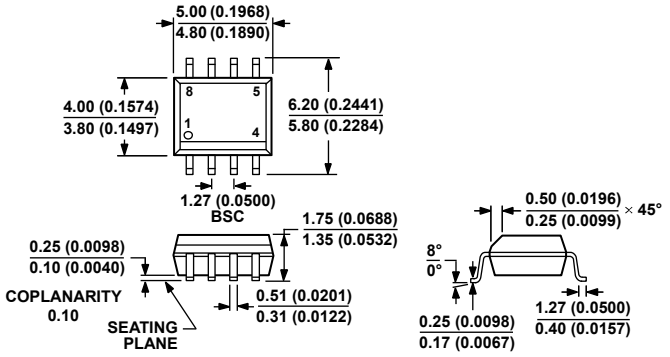

Figure 45. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Qty.
AD8479ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8479ARZ-RL	−40°C to +125°C	8-Lead SOIC_N, 13-Inch Tape and Reel	R-8	2,500 pieces
AD8479BRZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8479BRZ-RL	−40°C to +125°C	8-Lead SOIC_N, 13-Inch Tape and Reel	R-8	2,500 pieces
AD8479R-EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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