WINSOURCE
ELECTRONICS

# THE DATASHEET OF

# NCP716MT33TBG

# NCP716

## 80 mA Ultra-Low Iq, Wide Input Voltage Low Dropout Regulator

The NCP716 is 80 mA LDO Linear Voltage Regulator. It is a very stable and accurate device with ultra−low ground current consumption (4.7 μA over the full output load range) and a wide input voltage range (up to 24 V). The regulator incorporates several protection features such as Thermal Shutdown and Current Limiting.

### Features

- Operating Input Voltage Range: 2.5 V to 24 V
- Fixed Voltage Options Available:
  1.2 V to 5.0 V
- Ultra Low Quiescent Current: Max. 4.7 μA over Temperature
- ±2% Accuracy over Full Load, Line and Temperature Variations
- PSRR: 60 dB at 100 kHz
- Noise: 200 μ$V_{RMS}$ from 200 Hz to 100 kHz
- Thermal Shutdown and Current Limit Protection
- Available in WDFN6, 2x2x0.8 mm Package
- This is a Pb−Free Device

### Typical Applicaitons

- Portable Equipment
- Communication Systems

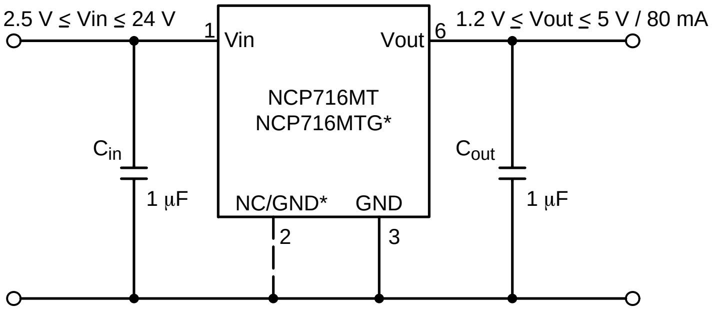

Figure 1. Typical Application Schematic

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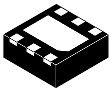
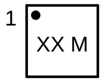
### MARKING DIAGRAMS

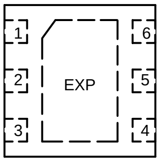


**WDFN6**
**CASE 511BR**



XX = Specific Device Code
M = Date Code

### PIN CONNECTIONS



WDFN6 2x2 mm
(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

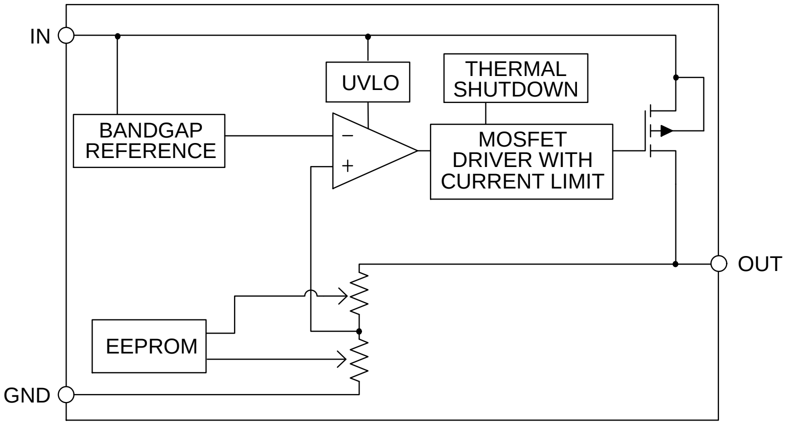


Figure 2. Simplified Block Diagram

### Table 1. PIN FUNCTION DESCRIPTION

| Pin No. wDFN6, 2 x 2 | Pin Name | Description |
|---|---|---|
| 6 | OUT | Regulated output voltage pin. A small 0.47 μF ceramic capacitor is needed from this pin to ground to assure stability. |
| 2 | NC/GND* | No connection at NCP716MT devices. This pin can be tied to ground to improve thermal dissipation or left disconnected. *Power supply ground at NCP716MTG devices. |
| 3, EXP | GND | Power supply ground. Exposed pad EXP must be tied with GND pin 3. |
| 4 | N/C | No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected. |
| 5 | N/C | No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected. |
| 1 | IN | Input pin. A small capacitor is needed from this pin to ground to assure stability. |

### Table 2. ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (Note 1) | $V_{IN}$ | −0.3 to 24 | V |
| Output Voltage | $V_{OUT}$ | −0.3 to 6 | V |
| Output Short Circuit Duration | $t_{SC}$ | Indefinite | s |
| Maximum Junction Temperature | $T_{J(MAX)}$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | −40 to 125 | °C |
| Storage Temperature Range | $T_{STG}$ | −55 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | $ESD_{HBM}$ | 2000 | V |
| ESD Capability, Machine Model (Note 2) | $ESD_{MM}$ | 200 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   ESD Charged Device Model tested per EIA/JESD22−C101E
   Latch up Current Maximum Rating tested per JEDEC standard: JESD78.

### Table 3. THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, WDFN6, 2 mm x 2 mm<br>Thermal Resistance, Junction−to−Air | $R_{\theta JA}$ | 120 | °C/W |

### Table 4. ELECTRICAL CHARACTERISTICS Voltage version 1.2 V

−40°C ≤ $T_J$ ≤ 125°C; $V_{IN}$ = 3.0 V; $I_{OUT}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at $T_J$ = +25°C. (Note 5)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Input Voltage | $I_{OUT}$ ≤ 10 mA | $V_{IN}$ | 2.5 | | 24 | V |
| | 10 mA < $I_{OUT}$ < 80 mA | | 3.0 | | 24 | |
| Output Voltage Accuracy | 3.0 V < $V_{IN}$ < 24 V, 0 < $I_{OUT}$ < 80 mA | $V_{OUT}$ | 1.164 | 1.2 | 1.236 | V |
| Turn−On Time | $I_{OUT}$ = 1 mA | $t_{ON}$ | − | 700 | − | μs |
| Undervoltage Lock−Out | $V_{IN}$ rising | UVLO | − | 2.1 | − | V |
| Line Regulation | 3.0 V ≤ $V_{IN}$ ≤ 24 V, $I_{OUT}$ = 1 mA | $Reg_{LINE}$ | | 30 | | mV |
| Load Regulation | $I_{OUT}$ = 0 mA to 80 mA | $Reg_{LOAD}$ | | 20 | | mV |
| Dropout voltage (Note 3) | | $V_{DO}$ | | | − | mV |
| Maximum Output Current | (Note 6) | $I_{OUT}$ | 110 | | | mA |
| Ground current | 0 < $I_{OUT}$ < 80 mA, −40 < $T_A$ < 85°C | $I_{GND}$ | | 3.2 | 4.2 | μA |
| | 0 < $I_{OUT}$ < 80 mA, $V_{IN}$ = 24 V | | | | 5.8 | μA |
| Power Supply Rejection Ratio | $V_{IN}$ = 3.0 V, $V_{OUT}$ = 1.2 V<br>$V_{PP}$ = 200 mV modulation<br>$I_{OUT}$ = 1 mA, $C_{OUT}$ = 10 μF<br>f = 100 kHz | PSRR | | 63 | | dB |
| Output Noise Voltage | $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 80 mA<br>f = 200 Hz to 100 kHz | $V_N$ | | 105 | | $\mu V_{rms}$ |
| Thermal Shutdown Temperature (Note 4) | Temperature increasing from $T_J$ = +25°C | $T_{SD}$ | | 155 | | °C |
| Thermal Shutdown Hysteresis (Note 4) | Temperature falling from $T_{SD}$ | $T_{SDH}$ | − | 25 | − | °C |

3. Not Characterized at $V_{IN}$ = 3.0 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 80 mA
4. Guaranteed by design and characterization.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. Respect SOA

### Table 5. ELECTRICAL CHARACTERISTICS Voltage version 1.5 V

−40°C ≤ $T_J$ ≤ 125°C; $V_{IN}$ = 3.0 V; $I_{OUT}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at $T_J$ = +25°C. (Note 9)

| Parameter | Test Conditions | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Input Voltage | $I_{OUT}$ ≤ 10 mA | | $V_{IN}$ | 2.5 | | 24 | V |
| | 10 mA < $I_{OUT}$ < 80 mA | | | 3.0 | | 24 | |
| Output Voltage Accuracy | 3.0 V < $V_{IN}$ < 24 V, 0 < $I_{OUT}$ < 80 mA | | $V_{OUT}$ | 1.455 | 1.5 | 1.545 | V |
| Turn−On Time | $I_{OUT}$ = 1 mA | | $t_{ON}$ | − | 700 | − | μs |
| Undervoltage Lock−Out | $V_{IN}$ rising | | UVLO | − | 2.1 | − | V |
| Line Regulation | 3.0 V ≤ $V_{IN}$ ≤ 24 V, $I_{OUT}$ = 1 mA | | $Reg_{LINE}$ | | 20 | | mV |
| Load Regulation | $I_{OUT}$ = 0 mA to 80 mA | | $Reg_{LOAD}$ | | 20 | | mV |
| Dropout voltage (Note 7) | | | | | | | |
| Maximum Output Current | (Note 10) | | $I_{OUT}$ | 110 | | | mA |
| Ground current | 0 < $I_{OUT}$ < 80 mA, −40 < $T_A$ < 85°C | | $I_{GND}$ | | 3.2 | 4.2 | μA |
| | 0 < $I_{OUT}$ < 80 mA, $V_{IN}$ = 24 V | | | | | 5.8 | μA |
| Power Supply Rejection Ratio | $V_{IN}$ = 3.0 V, $V_{OUT}$ = 1.5 V<br>$V_{PP}$ = 200 mV modulation<br>$I_{OUT}$ = 1 mA, $C_{OUT}$ = 10 μF | f = 100 kHz | PSRR | | 60 | | dB |
| Output Noise Voltage | $V_{OUT}$ = 1.5 V, $I_{OUT}$ = 80 mA<br>f = 200 Hz to 100 kHz | | $V_N$ | | 120 | | $\mu V_{rms}$ |
| Thermal Shutdown Temperature (Note 8) | Temperature increasing from $T_J$ = +25°C | | $T_{SD}$ | | 155 | | °C |
| Thermal Shutdown Hysteresis (Note 8) | Temperature falling from $T_{SD}$ | | $T_{SDH}$ | − | 25 | − | °C |

7. Not Characterized at $V_{IN}$ = 3.0 V, $V_{OUT}$ = 1.5 V, $I_{OUT}$ = 80 mA
8. Guaranteed by design and characterization.
9. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
10. Respect SOA

### Table 6. ELECTRICAL CHARACTERISTICS Voltage version 1.8 V

$-40°C \le T_J \le 125°C$; $V_{IN} = 3.0$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF, unless otherwise noted. Typical values are at $T_J = +25°C$. (Note 13)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Input Voltage | $I_{OUT} \le 10$ mA | $V_{IN}$ | 2.8 | | 24 | V |
| | 10 mA < $I_{OUT}$ < 80 mA | | 3.0 | | 24 | |
| Output Voltage Accuracy | 3.0 V < $V_{IN}$ < 24 V, 0 < $I_{OUT}$ < 80 mA | $V_{OUT}$ | 1.746 | 1.8 | 1.854 | V |
| Turn−On Time | $I_{OUT} = 1$ mA | $t_{ON}$ | − | 700 | − | µs |
| Undervoltage Lock−Out | $V_{IN}$ rising | UVLO | − | 2.1 | − | V |
| Line Regulation | 3.0 V ≤ $V_{IN}$ ≤ 24 V, $I_{OUT} = 1$ mA | $Reg_{LINE}$ | | 15 | | mV |
| Load Regulation | $I_{OUT} = 0$ mA to 80 mA | $Reg_{LOAD}$ | | 15 | | mV |
| Dropout voltage (Note 11) | | | | | | |
| Maximum Output Current | (Note 14) | $I_{OUT}$ | 110 | | | mA |
| Ground current | 0 < $I_{OUT}$ < 80 mA, −40 < $T_A$ < 85°C | $I_{GND}$ | | 3.2 | 4.2 | µA |
| | 0 < $I_{OUT}$ < 80 mA, $V_{IN} = 24$ V | | | | 5.8 | µA |
| Power Supply Rejection Ratio | $V_{IN} = 3.0$ V, $V_{OUT} = 1.8$ V<br>$V_{PP} = 200$ mV modulation<br>$I_{OUT} = 1$ mA, $C_{OUT} = 10$ µF<br>f = 100 kHz | PSRR | | 60 | | dB |
| Output Noise Voltage | $V_{OUT} = 1.8$ V, $I_{OUT} = 80$ mA<br>f = 200 Hz to 100 kHz | $V_N$ | | 140 | | $µV_{rms}$ |
| Thermal Shutdown Temperature (Note 12) | Temperature increasing from $T_J = +25°C$ | $T_{SD}$ | | 155 | | °C |
| Thermal Shutdown Hysteresis (Note 12) | Temperature falling from $T_{SD}$ | $T_{SDH}$ | − | 25 | − | °C |

11. Not Characterized at $V_{IN} = 3.0$ V, $V_{OUT} = 1.8$ V, $I_{OUT} = 80$ mA
12. Guaranteed by design and characterization.
13. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A = 25°C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
14. Respect SOA

### Table 7. ELECTRICAL CHARACTERISTICS Voltage version 2.5 V

−40°C ≤ $T_J$ ≤ 125°C; $V_{IN}$ = 3.5 V; $I_{OUT}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at $T_J$ = +25°C. (Note 17)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Input Voltage | 0 < $I_{OUT}$ < 80 mA | $V_{IN}$ | 3.5 | | 24 | V |
| Output Voltage Accuracy | 3.5 V < $V_{IN}$ < 24 V, 0 < $I_{OUT}$ < 80 mA | $V_{OUT}$ | 2.45 | 2.5 | 2.55 | V |
| Turn−On Time | $I_{OUT}$ = 1 mA | $t_{ON}$ | − | 700 | − | μs |
| Undervoltage Lock−Out | $V_{IN}$ rising | UVLO | − | 2.1 | − | V |
| Line Regulation | $V_{OUT}$ + 1 V ≤ $V_{IN}$ ≤ 24 V, $I_{OUT}$ = 1mA | $Reg_{LINE}$ | | 15 | | mV |
| Load Regulation | $I_{OUT}$ = 0 mA to 80 mA | $Reg_{LOAD}$ | | 15 | | mV |
| Dropout voltage (Note 15) | $V_{DO}$ = $V_{IN}$ – ($V_{OUT(NOM)}$ – 75 mV)<br>$I_{OUT}$ = 80 mA | $V_{DO}$ | | 400 | 640 | mV |
| Maximum Output Current | (Note 18) | $I_{OUT}$ | 110 | | | mA |
| Ground current | 0 < $I_{OUT}$ < 80 mA, −40 < $T_A$ < 85°C | $I_{GND}$ | | 3.2 | 4.2 | μA |
| | 0 < $I_{OUT}$ < 80 mA, $V_{IN}$ = 24 V | | | | 5.8 | μA |
| Power Supply Rejection Ratio | $V_{IN}$ = 3.5 V, $V_{OUT}$ = 2.5 V<br>$V_{PP}$ = 200 mV modulation<br>$I_{OUT}$ = 1 mA, $C_{OUT}$ = 10 μF<br>f = 100 kHz | PSRR | | 60 | | dB |
| Output Noise Voltage | $V_{OUT}$ = 2.5 V, $I_{OUT}$ = 80 mA<br>f = 200 Hz to 100 kHz | $V_N$ | | 160 | | $\mu V_{rms}$ |
| Thermal Shutdown Temperature (Note 16) | Temperature increasing from $T_J$ = +25°C | $T_{SD}$ | | 155 | | °C |
| Thermal Shutdown Hysteresis (Note 16) | Temperature falling from $T_{SD}$ | $T_{SDH}$ | − | 25 | − | °C |

15. Characterized when $V_{OUT}$ falls 75 mV below the regulated voltage and only for devices with $V_{OUT}$ = 2.5 V
16. Guaranteed by design and characterization.
17. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
18. Respect SOA

### Table 8. ELECTRICAL CHARACTERISTICS Voltage version 3.0 V

$-40°C \le T_J \le 125°C$; $V_{IN}$ = 4.0 V; $I_{OUT}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at $T_J$ = +25°C. (Note 21)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Input Voltage | 0 < $I_{OUT}$ < 80 mA | $V_{IN}$ | 4.0 | | 24 | V |
| Output Voltage Accuracy | 4.3 V < $V_{IN}$ < 24 V, 0 < $I_{OUT}$ < 80 mA | $V_{OUT}$ | 2.94 | 3.0 | 3.06 | V |
| Turn−On Time | $I_{OUT}$ = 1 mA | $t_{ON}$ | − | 700 | − | μs |
| Undervoltage Lock−Out | $V_{IN}$ rising | UVLO | − | 2.1 | − | V |
| Line Regulation | $V_{OUT}$ + 1 V ≤ $V_{IN}$ ≤ 24 V, $I_{OUT}$ = 1 mA | $Reg_{LINE}$ | | 4 | 10 | mV |
| Load Regulation | $I_{OUT}$ = 0 mA to 80 mA | $Reg_{LOAD}$ | | 10 | 30 | mV |
| Dropout voltage (Note 19) | $V_{DO}$ = $V_{IN}$ – ($V_{OUT(NOM)}$ – 90 mV)<br>$I_{OUT}$ = 80 mA | $V_{DO}$ | | 370 | 580 | mV |
| Maximum Output Current | (Note 22) | $I_{OUT}$ | 110 | | | mA |
| Ground current | 0 < $I_{OUT}$ < 80 mA, −40 < $T_A$ < 85°C | $I_{GND}$ | | 3.2 | 4.2 | μA |
| | 0 < $I_{OUT}$ < 80 mA, $V_{IN}$ = 24 V | | | | 5.8 | μA |
| Power Supply Rejection Ratio | $V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V<br>$V_{PP}$ = 200 mV modulation<br>$I_{OUT}$ = 1 mA, $C_{OUT}$ = 10 μF<br>f = 100 kHz | PSRR | | 58 | | dB |
| Output Noise Voltage | $V_{OUT}$ = 4.3 V, $I_{OUT}$ = 80 mA<br>f = 200 Hz to 100 kHz | $V_N$ | | 190 | | $\mu V_{rms}$ |
| Thermal Shutdown Temperature (Note 20) | Temperature increasing from $T_J$ = +25°C | $T_{SD}$ | | 155 | | °C |
| Thermal Shutdown Hysteresis (Note 20) | Temperature falling from $T_{SD}$ | $T_{SDH}$ | − | 25 | − | °C |

19. Characterized when $V_{OUT}$ falls 90 mV below the regulated voltage and only for devices with $V_{OUT}$ = 3.0 V
20. Guaranteed by design and characterization.
21. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
22. Respect SOA

### Table 9. ELECTRICAL CHARACTERISTICS Voltage version 3.3 V

−40°C ≤ $T_J$ ≤ 125°C; $V_{IN}$ = 4.3 V; $I_{OUT}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at $T_J$ = +25°C. (Note 25)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Input Voltage | 0 < $I_{OUT}$ < 80 mA | $V_{IN}$ | 4.3 | | 24 | V |
| Output Voltage Accuracy | 4.3 V < $V_{IN}$ < 24 V, 0 < $I_{OUT}$ < 80 mA | $V_{OUT}$ | 3.234 | 3.3 | 3.366 | V |
| Turn−On Time | $I_{OUT}$ = 1 mA | $t_{ON}$ | − | 700 | − | μs |
| Undervoltage Lock−Out | $V_{IN}$ rising | UVLO | − | 2.1 | − | V |
| Line Regulation | $V_{OUT}$ + 1 V ≤ $V_{IN}$ ≤ 24 V, $I_{OUT}$ = 1 mA | $Reg_{LINE}$ | | 4 | 10 | mV |
| Load Regulation | $I_{OUT}$ = 0 mA to 80 mA | $Reg_{LOAD}$ | | 10 | 30 | mV |
| Dropout voltage (Note 23) | $V_{DO}$ = $V_{IN}$ – ($V_{OUT(NOM)}$ – 99 mV)<br>$I_{OUT}$ = 80 mA | $V_{DO}$ | | 350 | 560 | mV |
| Maximum Output Current | (Note 26) | $I_{OUT}$ | 110 | | | mA |
| Ground current | 0 < $I_{OUT}$ < 80 mA, −40 < $T_A$ < 85°C | $I_{GND}$ | | 3.2 | 4.2 | μA |
| | 0 < $I_{OUT}$ < 80 mA, $V_{IN}$ = 24 V | | | | 5.8 | μA |
| Power Supply Rejection Ratio | $V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V<br>$V_{PP}$ = 200 mV modulation<br>$I_{OUT}$ = 1 mA, $C_{OUT}$ = 10 μF<br>f = 100 kHz | PSRR | | 60 | | dB |
| Output Noise Voltage | $V_{OUT}$ = 4.3 V, $I_{OUT}$ = 80 mA<br>f = 200 Hz to 100 kHz | $V_N$ | | 200 | | $\mu V_{rms}$ |
| Thermal Shutdown Temperature (Note 24) | Temperature increasing from $T_J$ = +25°C | $T_{SD}$ | | 155 | | °C |
| Thermal Shutdown Hysteresis (Note 24) | Temperature falling from $T_{SD}$ | $T_{SDH}$ | − | 25 | − | °C |

23. Characterized when $V_{OUT}$ falls 99 mV below the regulated voltage and only for devices with $V_{OUT}$ = 3.3 V
24. Guaranteed by design and characterization.
25. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
26. Respect SOA

**Table 10. ELECTRICAL CHARACTERISTICS Voltage version 5.0 V**
−40°C ≤ $T_J$ ≤ 125°C; $V_{IN}$ = 6.0 V; $I_{OUT}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at $T_J$ = +25°C. (Note 29)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Input Voltage | 0 < $I_{OUT}$ < 80 mA | $V_{IN}$ | 6.0 | | 24 | V |
| Output Voltage Accuracy | 6.0 V < $V_{IN}$ < 24 V, 0 < $I_{OUT}$ < 80 mA | $V_{OUT}$ | 4.9 | 5.0 | 5.1 | V |
| Turn−On Time | $I_{OUT}$ = 1 mA | $t_{ON}$ | − | 700 | − | μs |
| Undervoltage Lock−Out | $V_{IN}$ rising | UVLO | − | 2.1 | − | V |
| Line Regulation | $V_{OUT}$ + 1 V ≤ $V_{IN}$ ≤ 24 V, $I_{OUT}$ = 1 mA | $Reg_{LINE}$ | | 4 | 10 | mV |
| Load Regulation | $I_{OUT}$ = 0 mA to 80 mA | $Reg_{LOAD}$ | | 10 | 30 | mV |
| Dropout voltage (Note 27) | $V_{DO}$ = $V_{IN}$ – ($V_{OUT(NOM)}$ – 150 mV)<br>$I_{OUT}$ = 80 mA | $V_{DO}$ | | 310 | 500 | mV |
| Maximum Output Current | (Note 30) | $I_{OUT}$ | 110 | | | mA |
| Ground current | 0 < $I_{OUT}$ < 80 mA, −40 < $T_A$ < 85°C | $I_{GND}$ | | 3.2 | 4.2 | μA |
| | 0 < $I_{OUT}$ < 80 mA, $V_{IN}$ = 24 V | | | | 5.8 | μA |
| Power Supply Rejection Ratio | $V_{IN}$ = 6.0 V, $V_{OUT}$ = 5.0 V<br>$V_{PP}$ = 200 mV modulation<br>$I_{OUT}$ = 1 mA, $C_{OUT}$ =10 μF<br>f = 100 kHz | PSRR | | 54 | | dB |
| Output Noise Voltage | $V_{OUT}$ = 5.0 V, $I_{OUT}$ = 80 mA<br>f = 200 Hz to 100 kHz | $V_N$ | | 220 | | $\mu V_{rms}$ |
| Thermal Shutdown Temperature (Note 28) | Temperature increasing from $T_J$ = +25°C | $T_{SD}$ | | 155 | | °C |
| Thermal Shutdown Hysteresis (Note 28) | Temperature falling from $T_{SD}$ | $T_{SDH}$ | − | 25 | − | °C |

27. Characterized when $V_{OUT}$ falls 150 mV below the regulated voltage and only for devices with $V_{OUT}$ = 5.0 V
28. Guaranteed by design and characterization.
29. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
30. Respect SOA

## TYPICAL CHARACTERISTICS

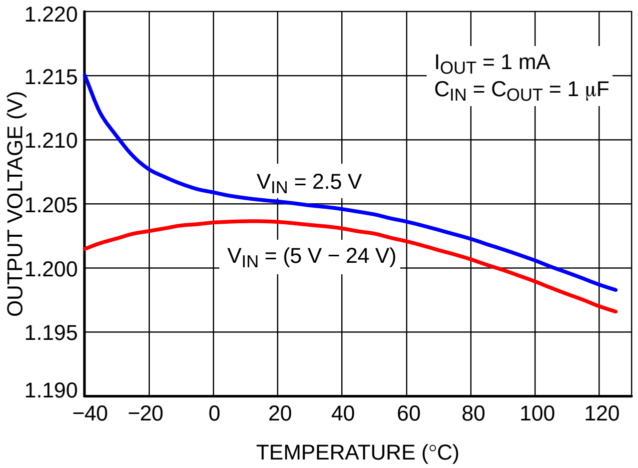


**Figure 3. NCP716x12xxx Output Voltage vs. Temperature**

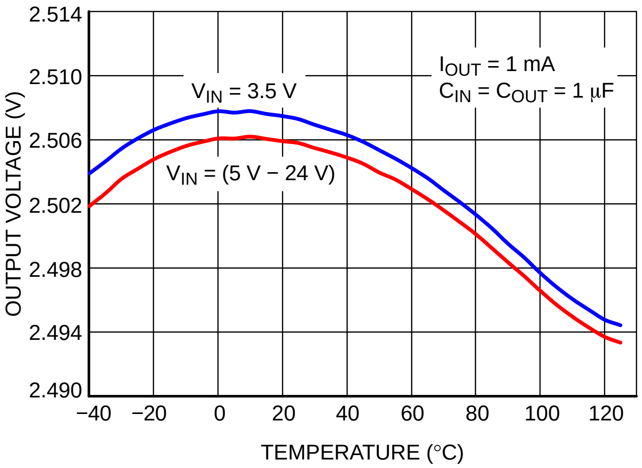


**Figure 4. NCP716x25xxx Output Voltage vs. Temperature**

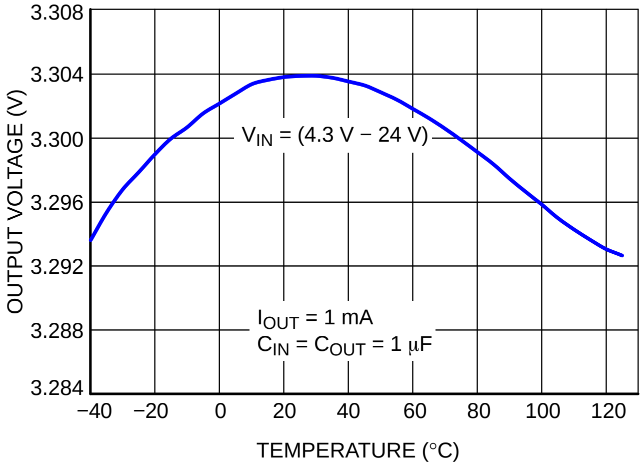


**Figure 5. NCP716x33xxx Output Voltage vs. Temperature**

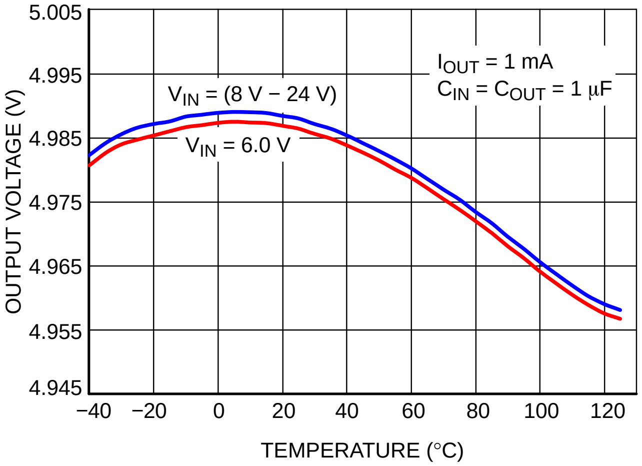


**Figure 6. NCP716x50xxx Output Voltage vs. Temperature**

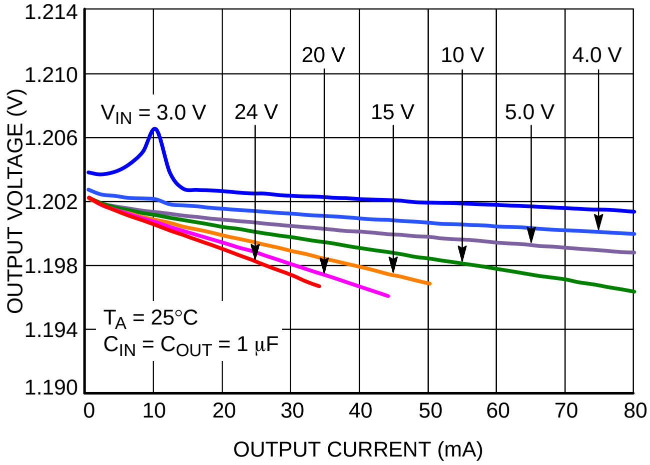


**Figure 7. NCP716x12xxx Output Voltage vs. Output Current**

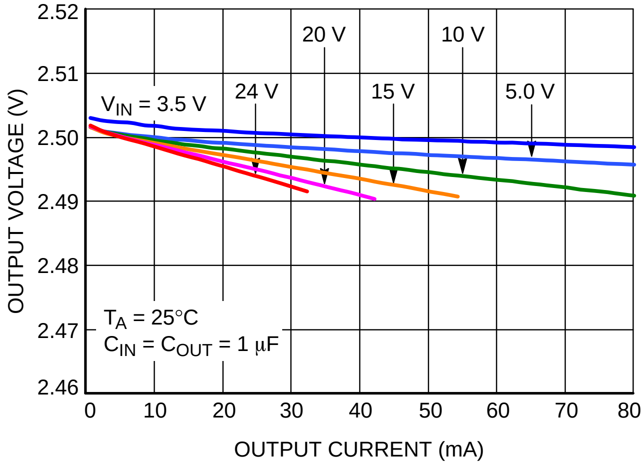


**Figure 8. NCP716x25xxx Output Voltage vs. Output Current**

## TYPICAL CHARACTERISTICS

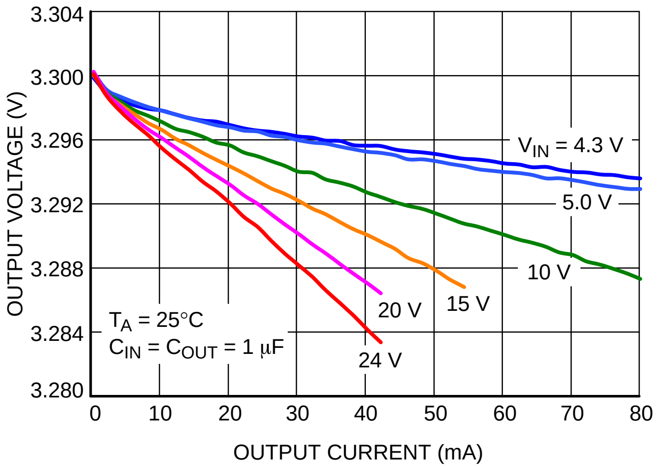


**Figure 9. NCP7163V3 Output Voltage vs. Output Current**

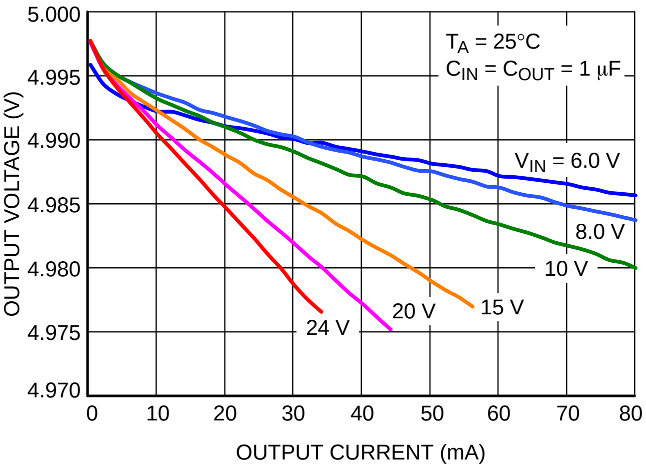


**Figure 10. NCP716x50xxx Output Voltage vs. Output Current**

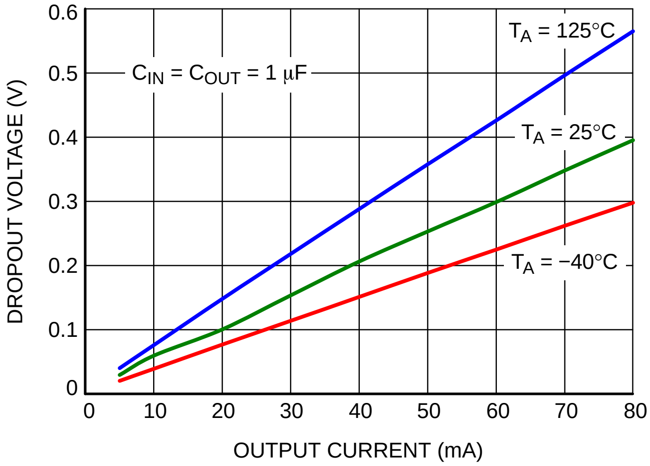


**Figure 11. NCP716x25xxx Dropout Voltage vs. Output Current**

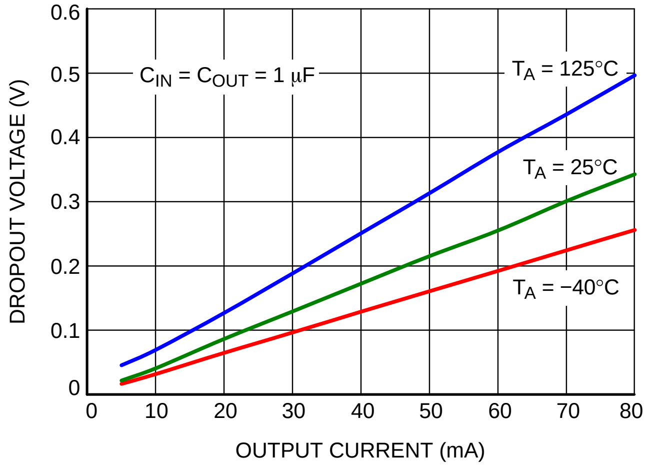


**Figure 12. NCP716x33xxx Dropout Voltage vs. Output Current**

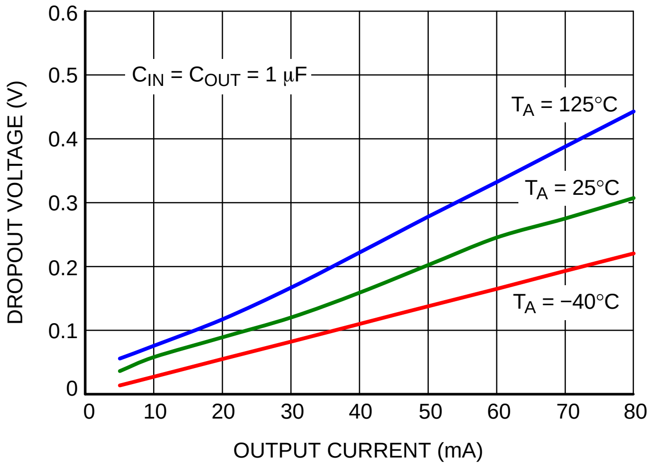


**Figure 13. NCP716x50xxx Dropout Voltage vs. Output Current**

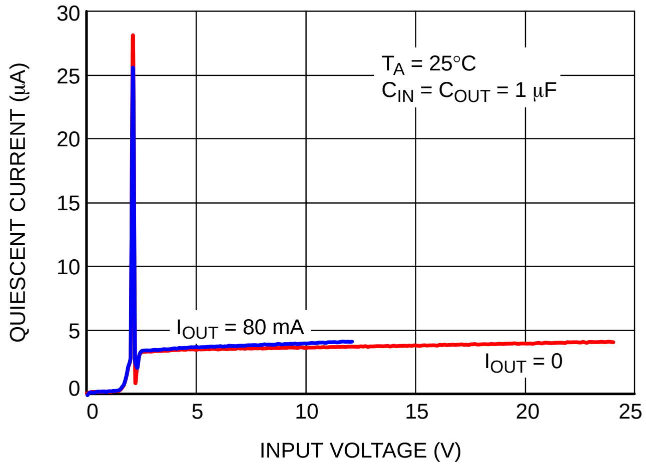


**Figure 14. NCP716x12xxx Ground Current vs. Input Voltage**

## TYPICAL CHARACTERISTICS

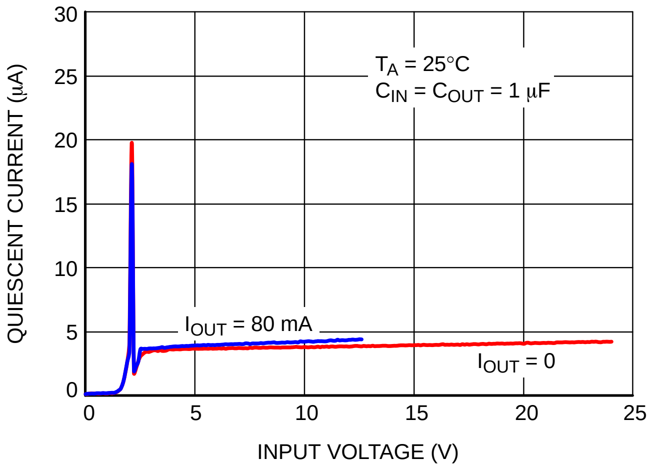


**Figure 15. NCP716x25xxx Ground Current vs. Input Voltage**

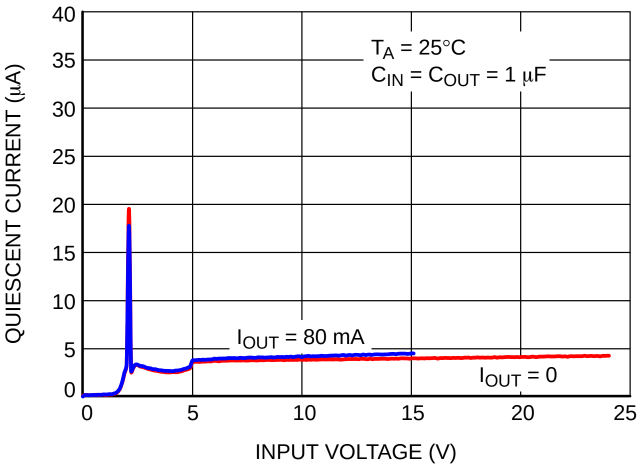


**Figure 16. NCP716x50xxx Ground Current vs. Input Voltage**

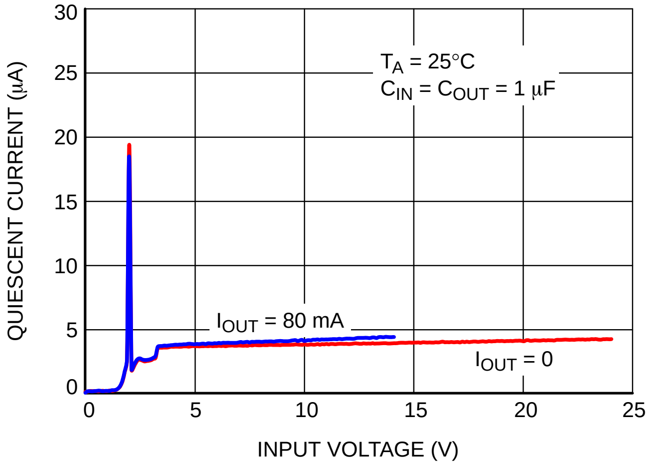


**Figure 17. NCP716x33xxx Ground Current vs. Input Voltage**

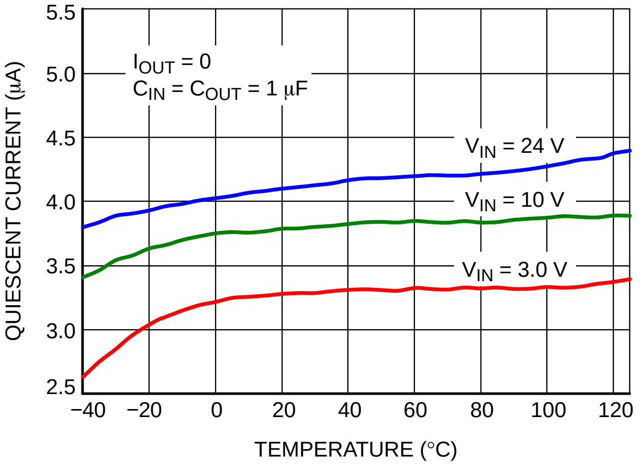


**Figure 18. NCP716x12xxx Quiescent Current vs. Temperature**

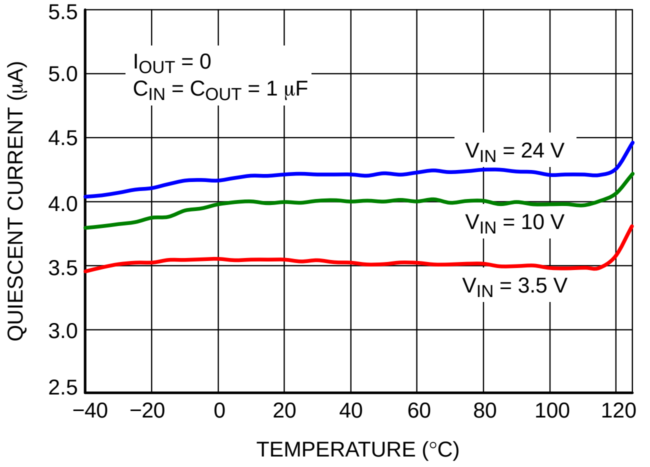


**Figure 19. NCP716x25xxx Quiescent Current vs. Temperature**

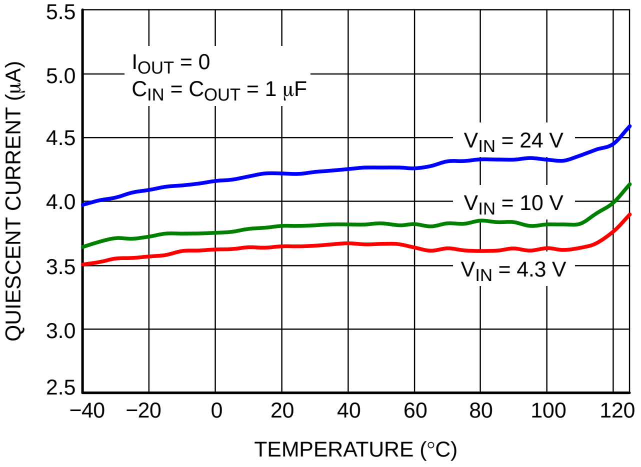


**Figure 20. NCP716x33xxx Quiescent Current vs. Temperature**

## TYPICAL CHARACTERISTICS

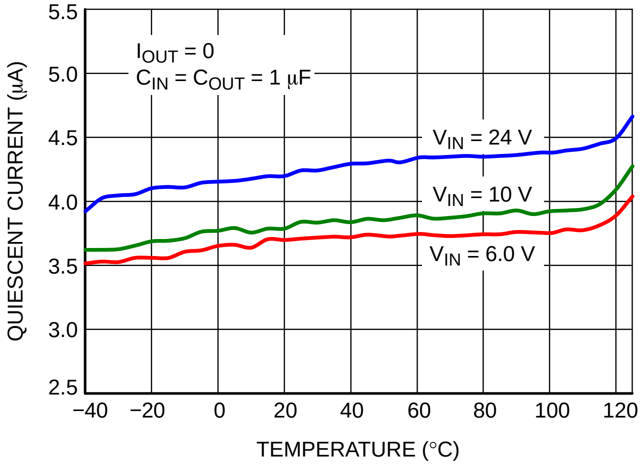


**Figure 21. NVP716x50xxx Quiescent Current vs. Temperature**

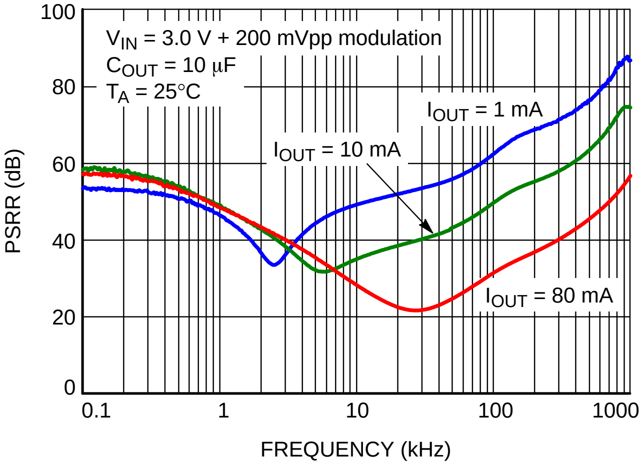


**Figure 22. NCP716x12xxx PSRR vs. Frequency**

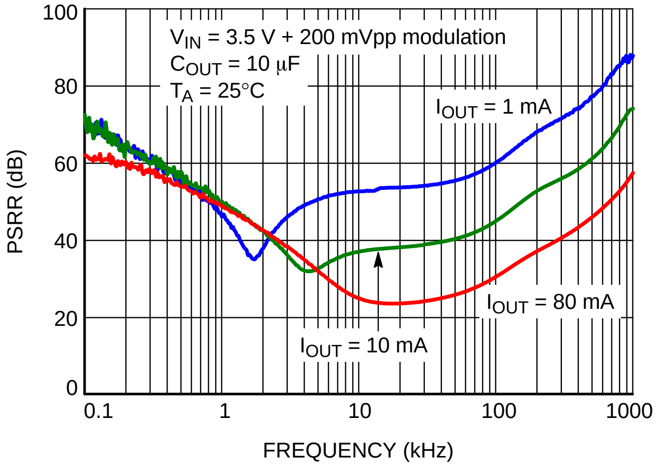


**Figure 23. NCP716x25xxx PSRR vs. Frequency**

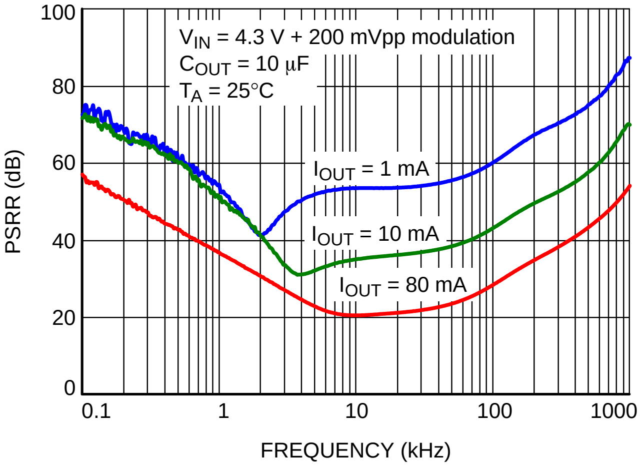


**Figure 24. NCP716x33xxx PSRR vs. Frequency**

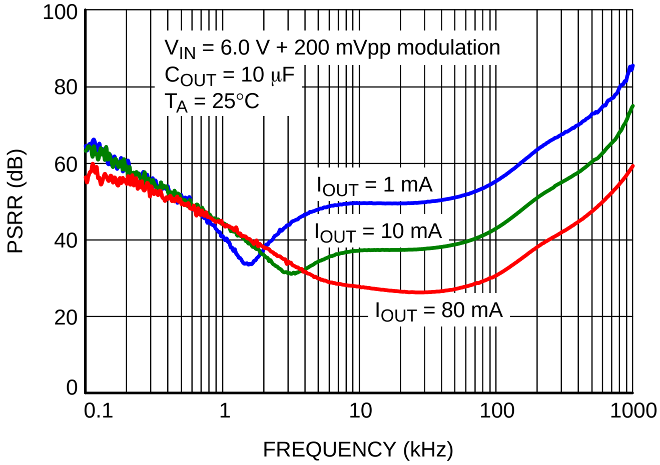


**Figure 25. NCP716x50xxx PSRR vs. Frequency**

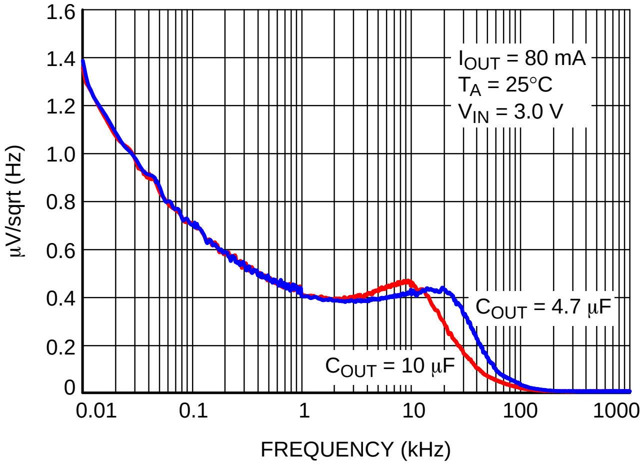


**Figure 26. NCP716x12xxx Output Spectral Noise Density vs. Frequency**

## TYPICAL CHARACTERISTICS

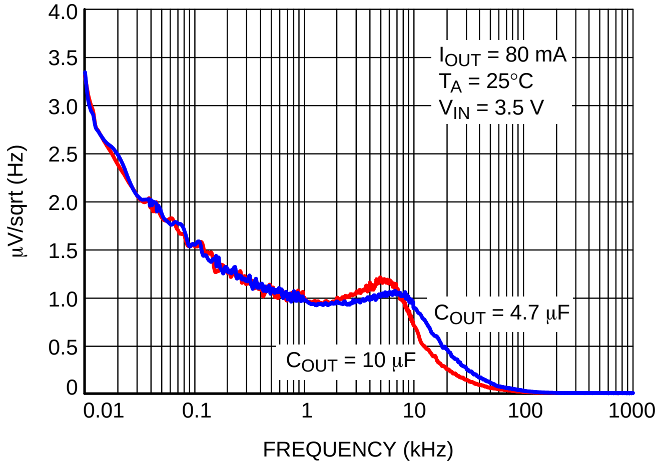


Figure 27. NCP716x25xxx Output Spectral Noise Density vs. Frequency

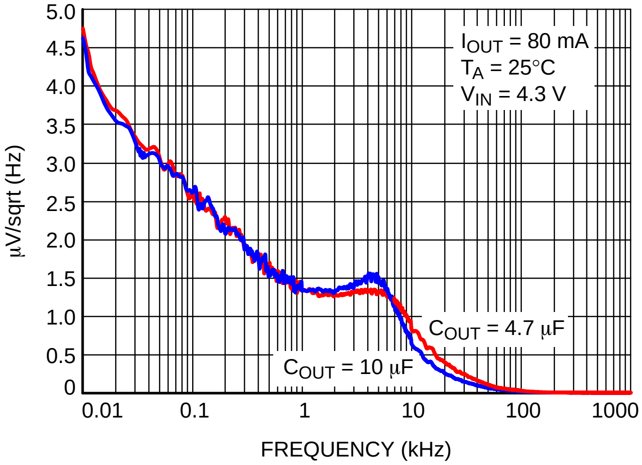


Figure 28. NCP716x33xxx Output Spectral Noise Density vs. Frequency

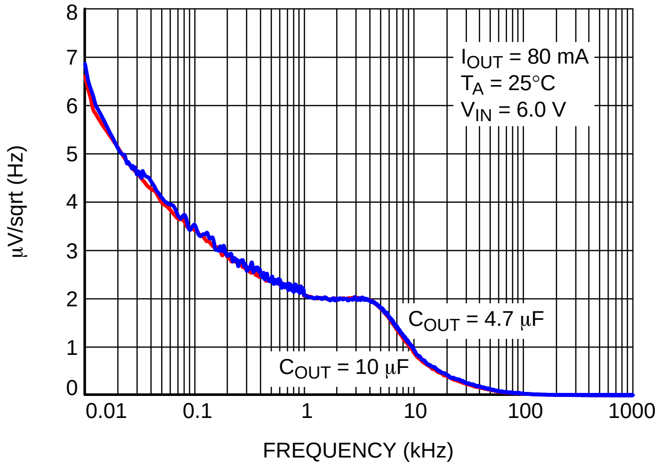


Figure 29. NCP716x50xxx Output Spectral Noise Density vs. Frequency

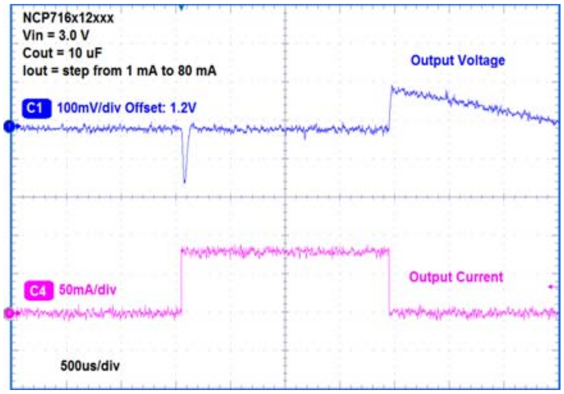


Figure 30. Load Transient Response

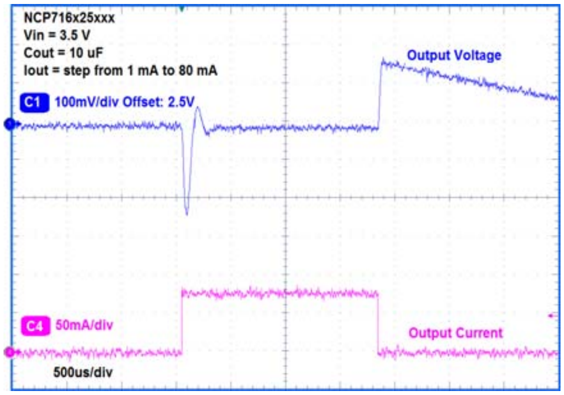


Figure 31. Load Transient Response

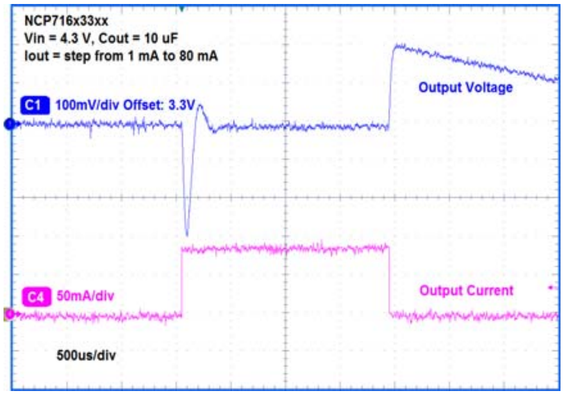


Figure 32. Load Transient Response

## TYPICAL CHARACTERISTICS

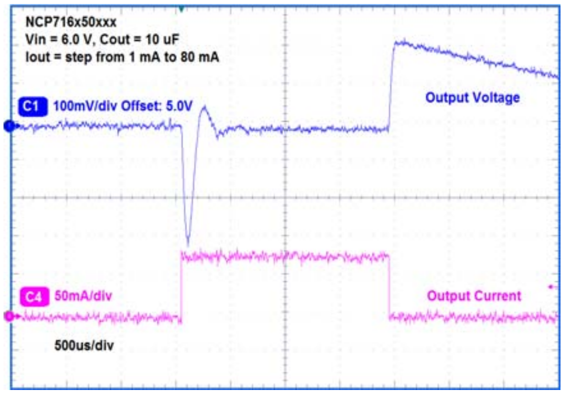


Figure 33. Load Transient Response

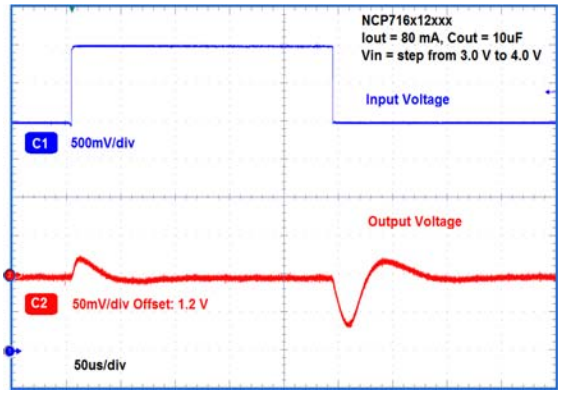


Figure 34. Line Transient Response

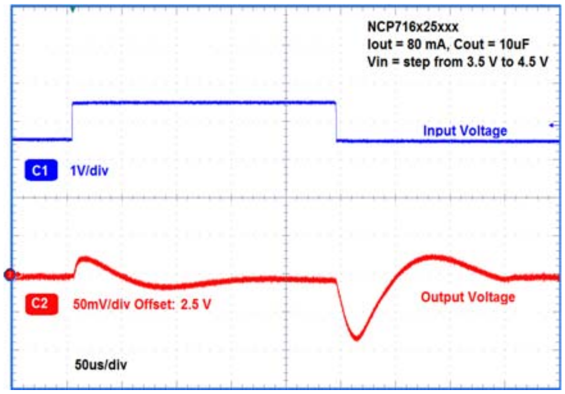


Figure 35. Line Transient Response

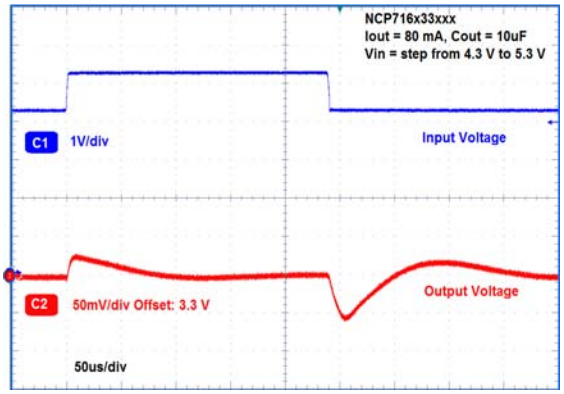


Figure 36. Line Transient Response

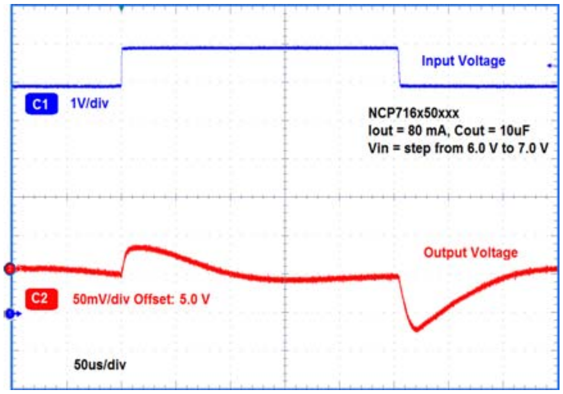


Figure 37. Line Transient Response

## TYPICAL CHARACTERISTICS

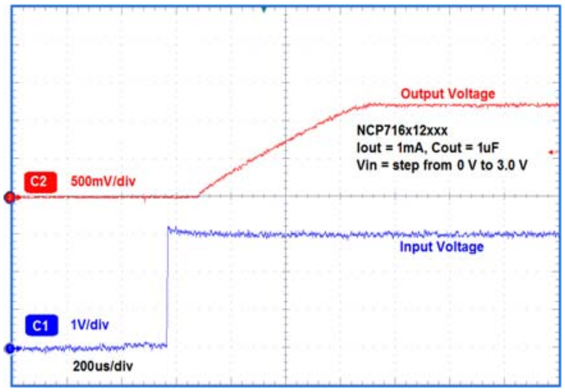


Figure 38. Input Voltage Turn−On Response

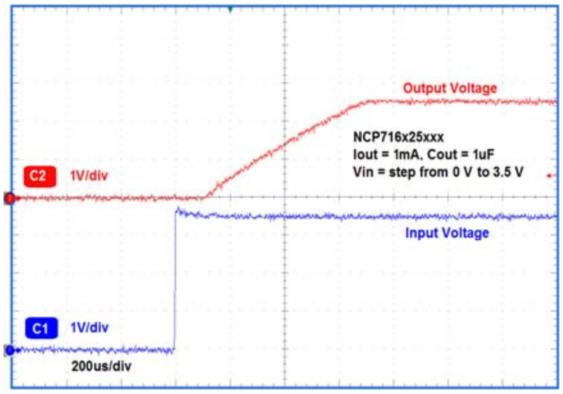


Figure 39. Input Voltage Turn−On Response

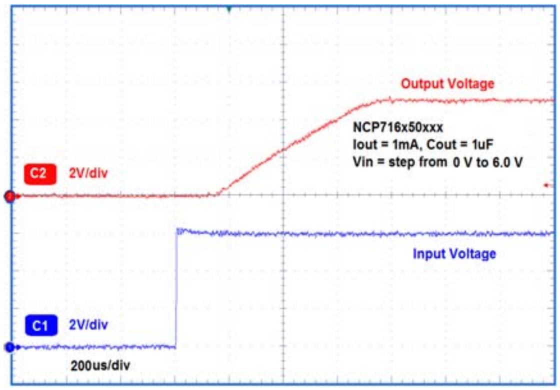


Figure 40. Input Voltage Turn−On Response

## APPLICATIONS INFORMATION

The NCP716 is the member of new family of Wide Input Voltage Range Low Dropout Regulators which delivers Ultra Low Ground Current consumption, Good Noise and Power Supply Rejection Ratio Performance.

### Input Decoupling ($C_{IN}$)

It is recommended to connect at least 0.1 μF Ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or Noise superimposed onto constant Input Voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes.

Higher capacitance and lower ESR Capacitors will improve the overall line transient response.

### Output Decoupling ($C_{OUT}$)

The NCP716 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 0.47 μF or greater up to 10 μF. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

### Power Dissipation and Heat sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the NCP716 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

The power dissipated by the NCP716 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}(I_{OUT})\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \qquad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \qquad \text{(eq. 3)}$$

For reliable operation, junction temperature should be limited to +125°C maximum.

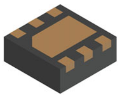
### Hints

VIN and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP716, and make traces as short as possible.

### ORDERING INFORMATION

| Device | Voltage Option | Marking | Package | Shipping† |
|---|---|---|---|---|
| NCP716MT12TBG | 1.2 V | 6A | WDFN6<br>(Pb−Free) | 3000 / Tape & Reel |
| NCP716MT15TG | 1.5 V | 6C | | |
| NCP716MT18TBG | 1.8 V | 6D | | |
| NCP716MT25TBG | 2.5 V | 6E | | |
| NCP716MT30TBG | 3.0 V | 6F | | |
| NCP716MT33TBG | 3.3 V | 6G | | |
| NCP716MT50TBG | 5.0 V | 6H | | |
| NCP716MTG50TBG | 5.0 V | GH | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

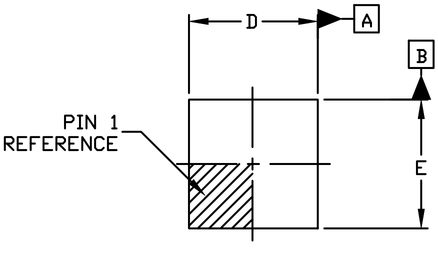


**WDFN6 2x2, 0.65P**
CASE 511BR
ISSUE C

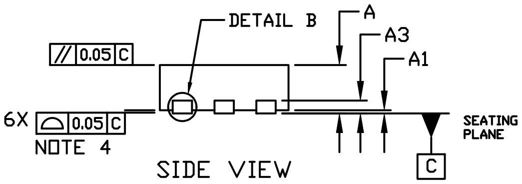
DATE 01 DEC 2021

NOTES:

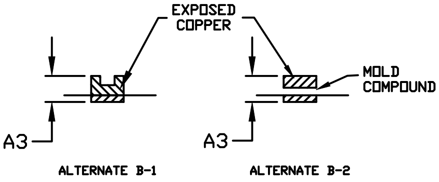
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



TOP VIEW



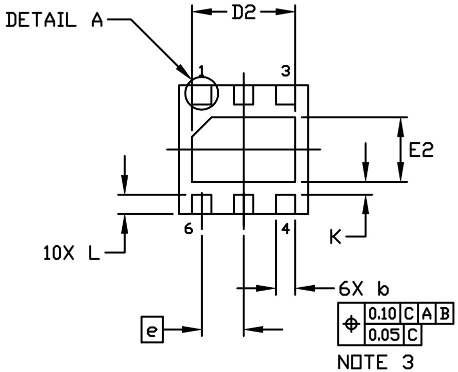
SIDE VIEW



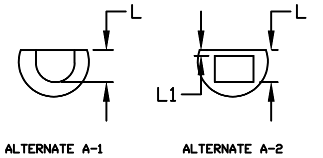
DETAIL B

ALTERNATE CONSTRUCTION

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | --- | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.25 | 0.30 | 0.35 |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.50 | 1.60 | 1.70 |
| E | 1.90 | 2.00 | 2.10 |
| E2 | 0.90 | 1.00 | 1.10 |
| e | 0.65 BSC | | |
| K | 0.20 REF | | |
| L | 0.20 | 0.30 | 0.40 |
| L1 | --- | --- | 0.15 |

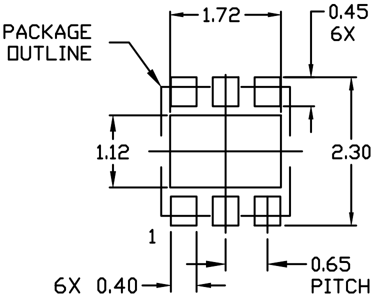


BOTTOM VIEW



DETAIL A

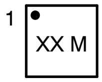
ALTERNATE CONSTRUCTIONS



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC**
**MARKING DIAGRAM***



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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