





# FDMF6700 Driver plus FET Multi-chip Module

## Benefits

- Fully optimized system efficiency. Higher efficiency levels are achievable compared with conventional discrete components.
- Space savings of up to 50% PCB versus discrete solutions.
- Higher frequency of operation.
- Simpler system design and board layout. Reduced time in component selection and optimization.

## Features

- 12V typical Input Voltage
- Output current up to 25A
- 500KHz switching frequency capable
- Internal adaptive gate drive
- Integrated bootstrap diode
- Peak Efficiency >85%
- Under-voltage Lockout
- Output disable for lost phase shutdown
- Low profile SMD package
- RoHS Compliant



## General Description

The FDMF6700 is a fully optimized integrated 12V Driver plus MOSFET power stage solution for high current synchronous buck DC-DC applications. The device integrates a driver IC and two Power MOSFETs into a space saving, 6mm x 6mm, 40-pin Power66™ package. Fairchild Semiconductor's integrated approach optimizes the complete switching power stage with regards to driver to FET dynamic performance, system inductance and overall solution ON resistance. Package parasitics and problematical layouts associated with conventional discrete solutions are greatly reduced. This integrated approach results in significant board space saving, therefore maximizing footprint power density. This solution is based on the Intel™ DrMOS specification.

## Applications

- Desktop and server VR11.x V-core and non V-core buck converters.
- CPU/GPU power train in game consoles and high end desktop systems.
- High-current DC-DC Point of Load (POL) converters
- Networking and telecom microprocessor voltage regulators
- Small form factor voltage regulator modules

## Powertrain Application Circuit

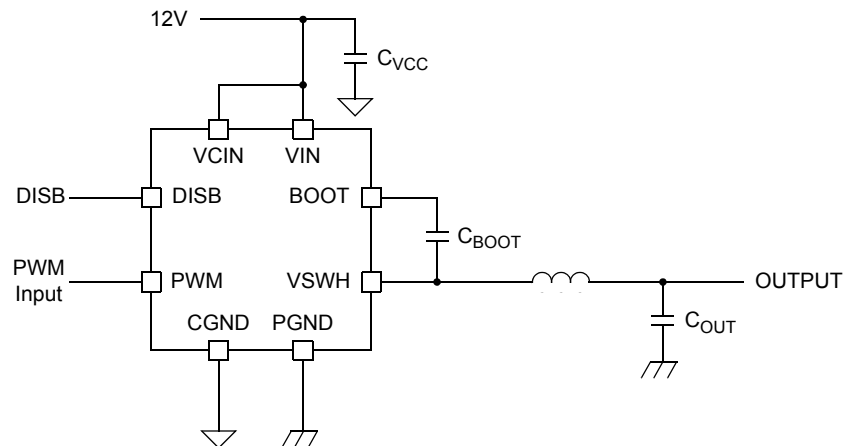


Figure 1. Powertrain Application Circuit

## Ordering Information

Part	Current Rating Max [A]	Input Voltage Typical [V]	Frequency Max [KHz]	Device Marking
FDMF6700	25	12	500	FDMF6700

### Functional Block Diagram

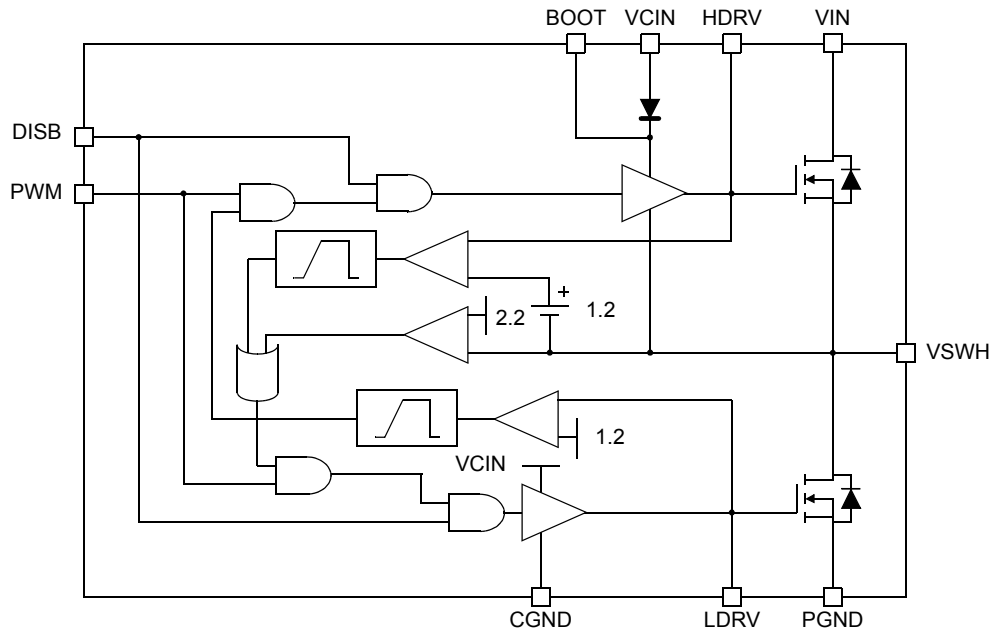


Figure 2. Functional Block Diagram

### Pin Configuration

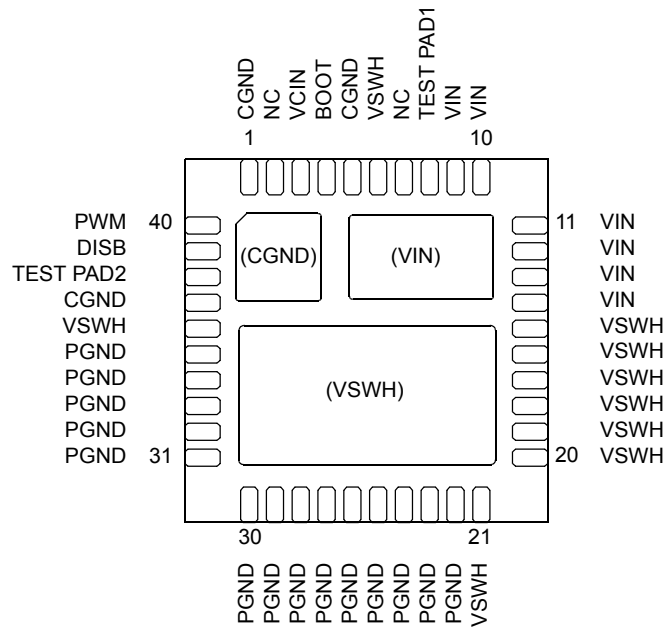


Figure 3. Power66 40L Bottom View

## Pin Description

Pin	Name	Function
1,5,37,A	CGND	IC Ground. Ground return for driver IC.
2,7	NC	No connect
3	VCIN	IC Supply. +12V chip bias power. Bypass with a 1 $\mu$ F ceramic capacitor.
4	BOOT	Bootstrap Supply Input. Provides voltage supply to high-side MOSFET driver. Connect bootstrap capacitor.
6,15-21,36,C	VSWH	Switch Node Input. SW Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-thru protection.
9-4,B	VIN	Power Input. Output stage supply voltage.
8	TEST PAD 1	For manufacturing test only. HDRV pin. This pin must be floated. Must not be connected to any pin.
22-35	PGND	Power ground. Output stage ground. Source pin of low side MOSFET(s).
38	TEST PAD 2	For manufacturing test only. LDRV pin. This pin must be floated. Must not be connected to any pin.
39	DISB	Output Disable. When low, this pin disable FET switching (HDRV and LDRV are held low).
40	PWM	PWM Signal Input. This pin accepts a logic-level PWM signal from the controller.

## Absolute Maximum Rating

Parameter	Min.	Max.	Units	
$V_{CIN}$ to PGND	-0.5	15	V	
$V_{IN}$ to PGND	-0.5	15	V	
PWM, DSIB to GND	-0.3	5.5	V	
$V_{SWH}$ to PGND	Continuous	-1	15	V
	Transient ( $t = 100\text{ns}$ , $f_{sw} = 500\text{KHz}$ )	-5	25	V
BOOT to VSWH	-0.3	15	V	
BOOT to PGND	Continuous	-0.3	30	V
	Transient ( $t = 100\text{ns}$ , $f_{sw} = 500\text{KHz}$ )	-0.3	33	V
$I_{O(AV)}$	$V_{IN} = 12\text{V}$ , $V_O = 1.3\text{V}$ , $f_{sw} = 500\text{KHz}$ , $T_{PCB} = 100^\circ\text{C}$		25	A
$I_{O(PK)}$	$V_{IN} = 12\text{V}$ , $t_{PULSE} = 10\mu\text{s}$		65	A
$R_{\theta JPCB}$	Junction to PCB Thermal Resistance (note 1)		6.5	$^\circ\text{C/W}$
$P_D$	$T_{PCB} = 100^\circ\text{C}$ (note 1)		7.7	W
Operating and Storage Junction Temperature Range		-55	150	$^\circ\text{C}$

## Recommended Operating Range

Parameter	Min.	Typ.	Max.	Units		
$V_{CIN}$	Control Circuit Supply Voltage		6.4	12	13.5	V
$V_{IN}$	Output Stage Supply Voltage		6.4	12	14	V

## Electrical Characteristics

$V_{IN} = 12\text{V}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Control Circuit Supply Current	$I_{CIN}$	$f_{sw} = 0\text{Hz}$ , $V_{DISB} = 0\text{V}$		3.5	8	mA
		$f_{sw} = 500\text{KHz}$ , $V_{DISB} = 5\text{V}$		18		
Undervoltage lockout threshold	$V_{TH(UVLO)}^{(2)}$	Turn-on		6		V
		Turn-off		5.25		V
PWM Input High Voltage	$V_{IH(PWM)}$		3.5			V

## Electrical Characteristics

$V_{IN} = 12V$ ,  $T_A = 25^\circ C$  unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
PWM Input Low Voltage	$V_{IL(PWM)}$				0.8	V
PWM Input Current	$I_{PWM}$		-1		1	$\mu A$
Output Disable Input High Voltage	$V_{IH(DISB)}$		2.5			V
Output Disable Input Low Voltage	$V_{IL(DISB)}$				0.8	V
Output Disable Input Current	$I_{DISB}$		-1		1	$\mu A$
Output Stage Leakage Current	$I_{IN\_LEAKAGE}$	$V_{DISB} = 0V$		250		$\mu A$
Propagation Delay	$t_{PDL(LDRV)}^{(3)}$	$V_{IN} = 12V$ , $V_{OUT} = 1.3V$ , $f_{sw} = 500KHz$ , $I_O = 25A$		41		ns
	$t_{PDL(HDRV)}^{(3)}$			37		ns
	$t_{PDH(LDRV)}^{(3)}$			34		ns
	$t_{PDH(HDRV)}^{(3)}$			53		ns

**Note 1:** Package power dissipation based on 4 layer, 2 square inch, 2 oz. copper pad.  $R_{\theta JPCB}$  is the steady state junction to PCB thermal resistance with PCB temperature referenced at VSWH pin.

**Note 2:** When combined with controller, driver UVLO must be less than that of controller.

**Note 3:**  $t_{PDL(LDRV/HDRV)}$  refers to HIGH-to-LOW transition,  $t_{PDH(LDRV/HDRV)}$  refers to LOW-to-HIGH transition.

## Typical Characteristics

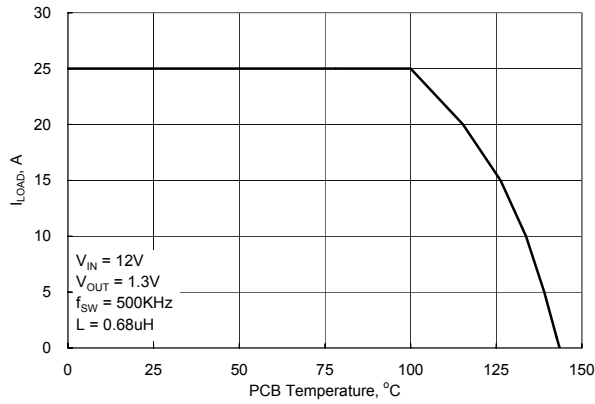


Figure 4. Safe Operating Area vs. PCB Temperature

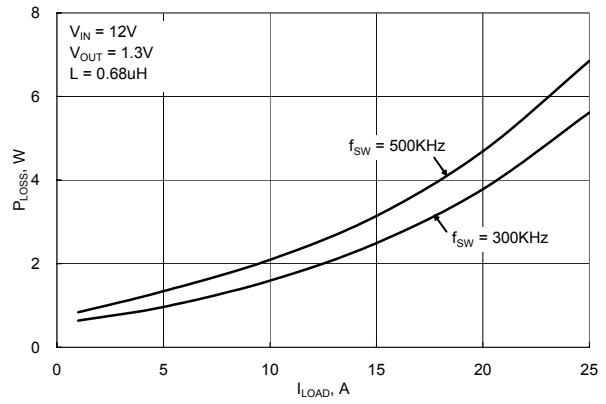


Figure 5. Module Power Loss vs. Output Current ( $V_O$  measured at VSWH pin)

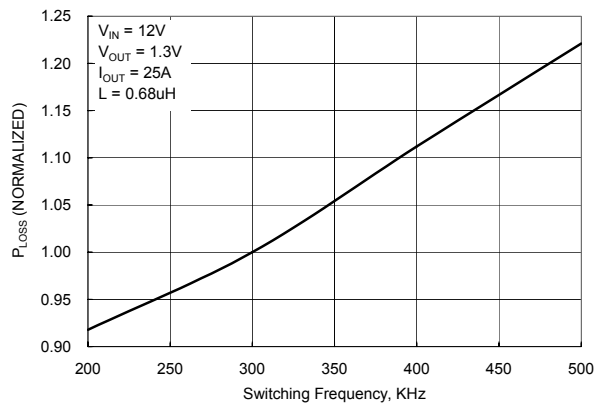


Figure 6. Power Loss vs. Switching Frequency

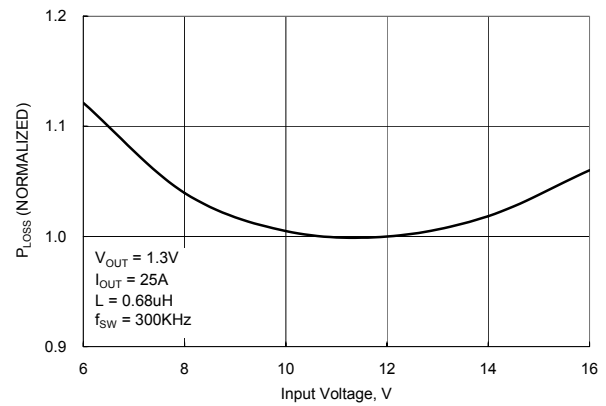


Figure 7. Power Loss vs. Input Voltage

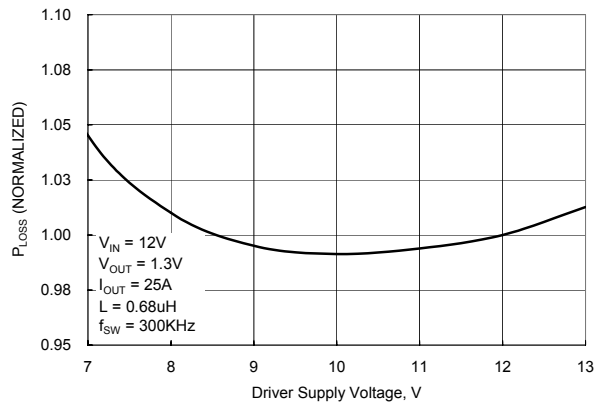


Figure 8. Power Loss vs. Supply Voltage

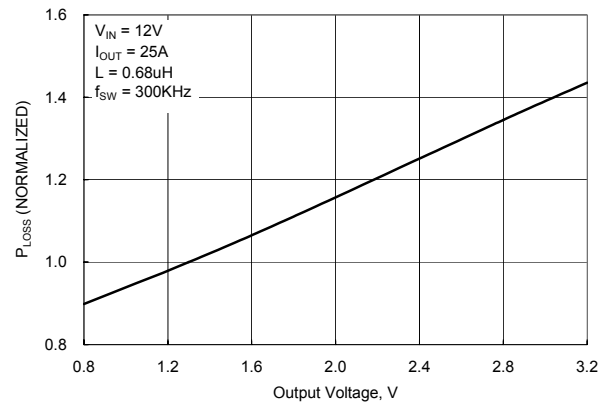


Figure 9. Power Loss vs. Output Voltage

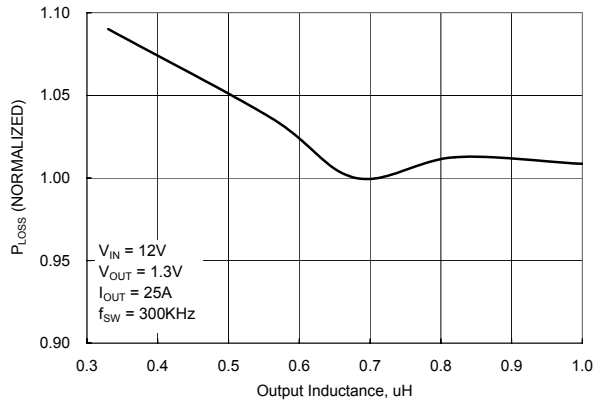


Figure 10. Power Loss vs. Output Inductance

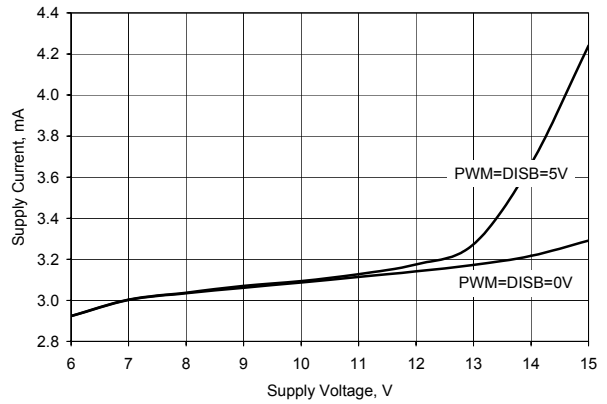


Figure 11. Supply Current vs. Supply Voltage

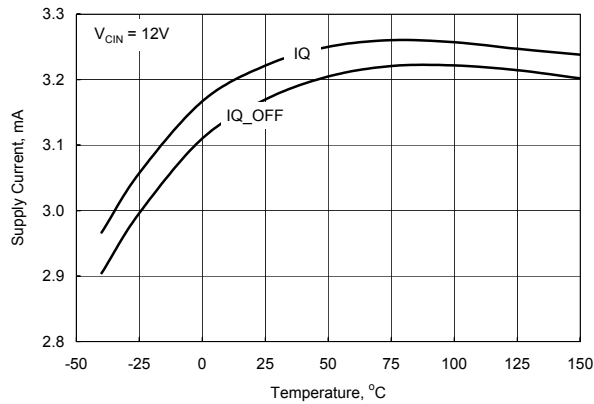


Figure 12. Supply Current vs. Temperature

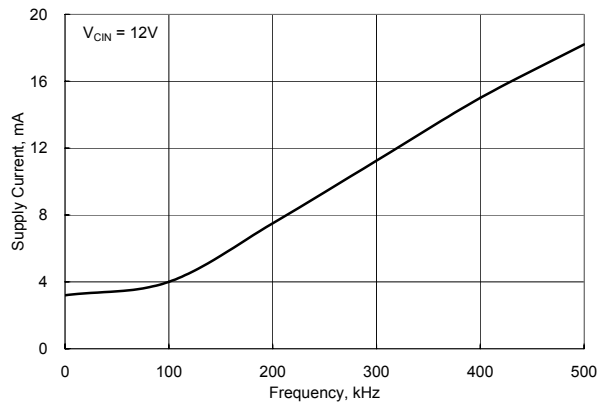


Figure 13. Supply Current vs. Frequency

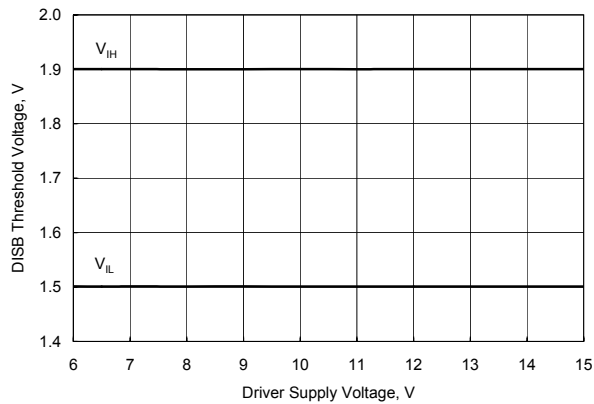


Figure 14. DISB Threshold Voltage vs. Driver Supply Voltage

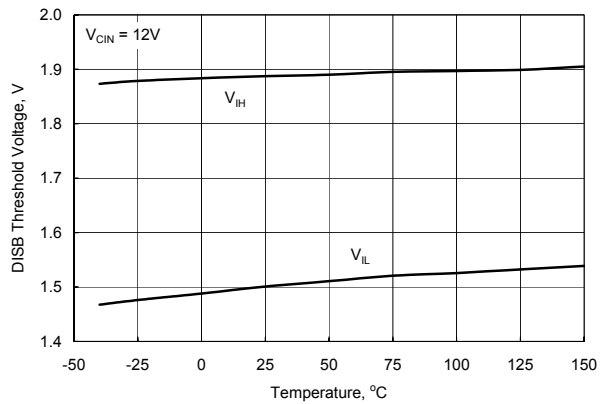


Figure 15. DISB Threshold Voltage vs. Temperature

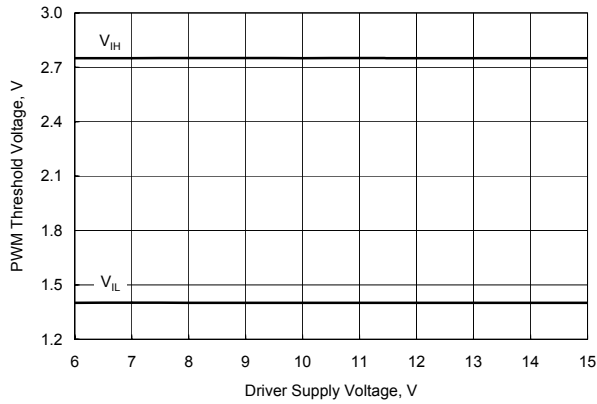


Figure 16. PWM Threshold Voltage vs. Driver Supply Voltage

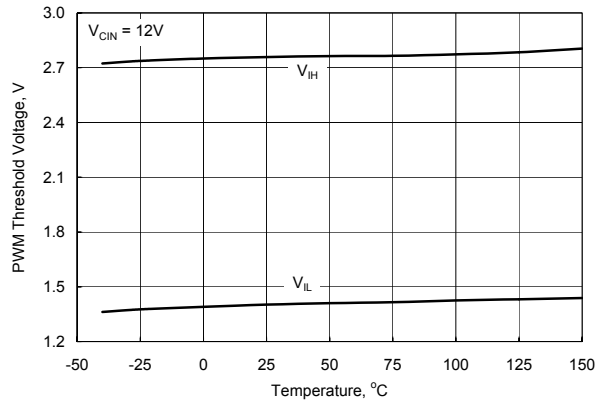


Figure 17. PWM Threshold Voltage vs. Temperature

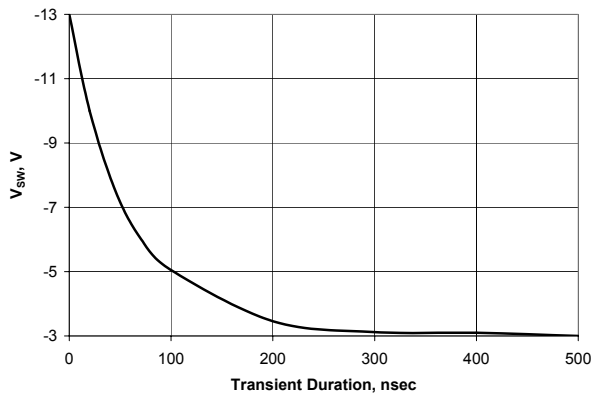


Figure 18. V<sub>SW</sub> vs. Transient Duration

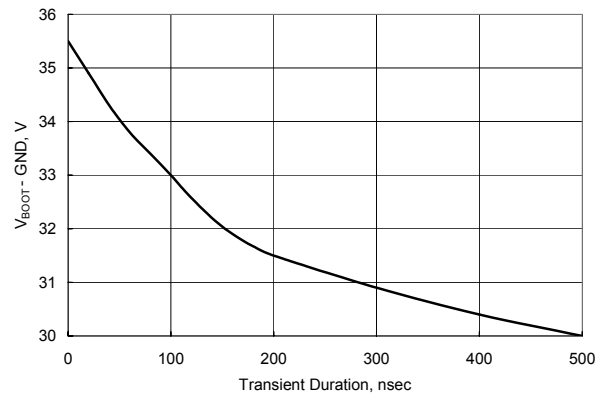


Figure 19. Boot to Ground Voltage vs. Transient Duration

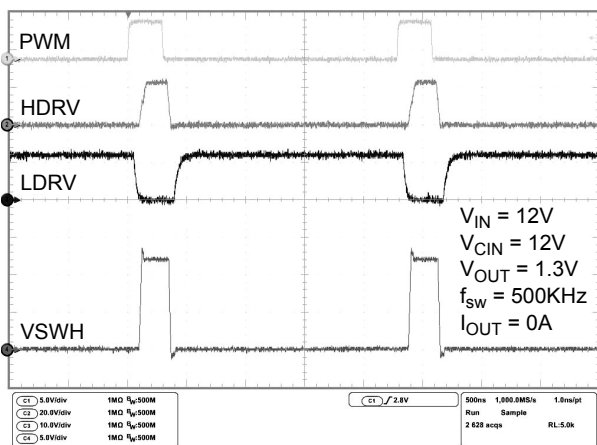


Figure 20. Switching Waveform at I<sub>out</sub> = 0A

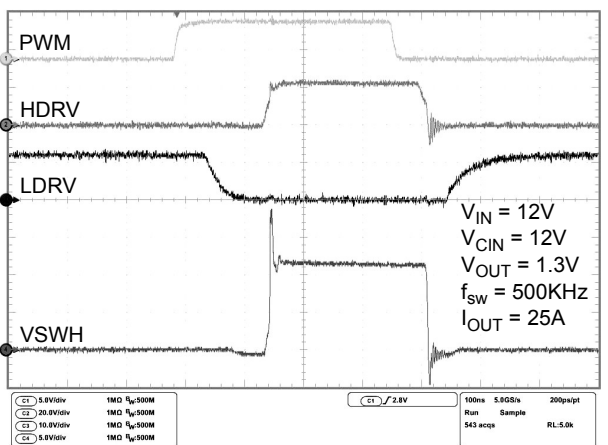


Figure 21. Switching Waveform at I<sub>out</sub> = 25A

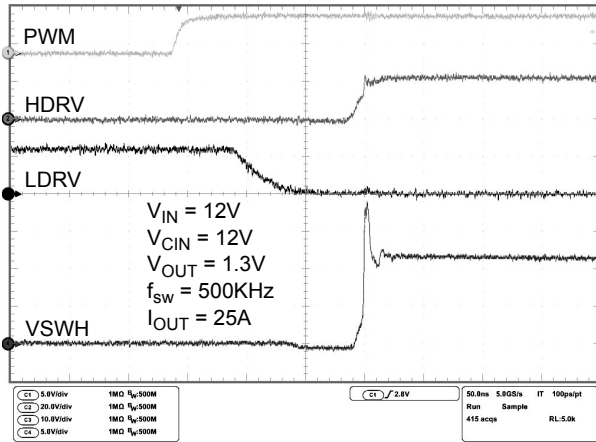


Figure 22. Switching Waveform (Rising edge)

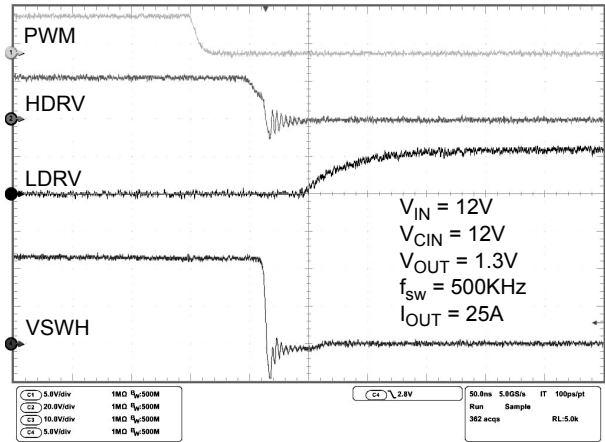


Figure 23. Switching Waveform (Falling Edge)



## Typical Application

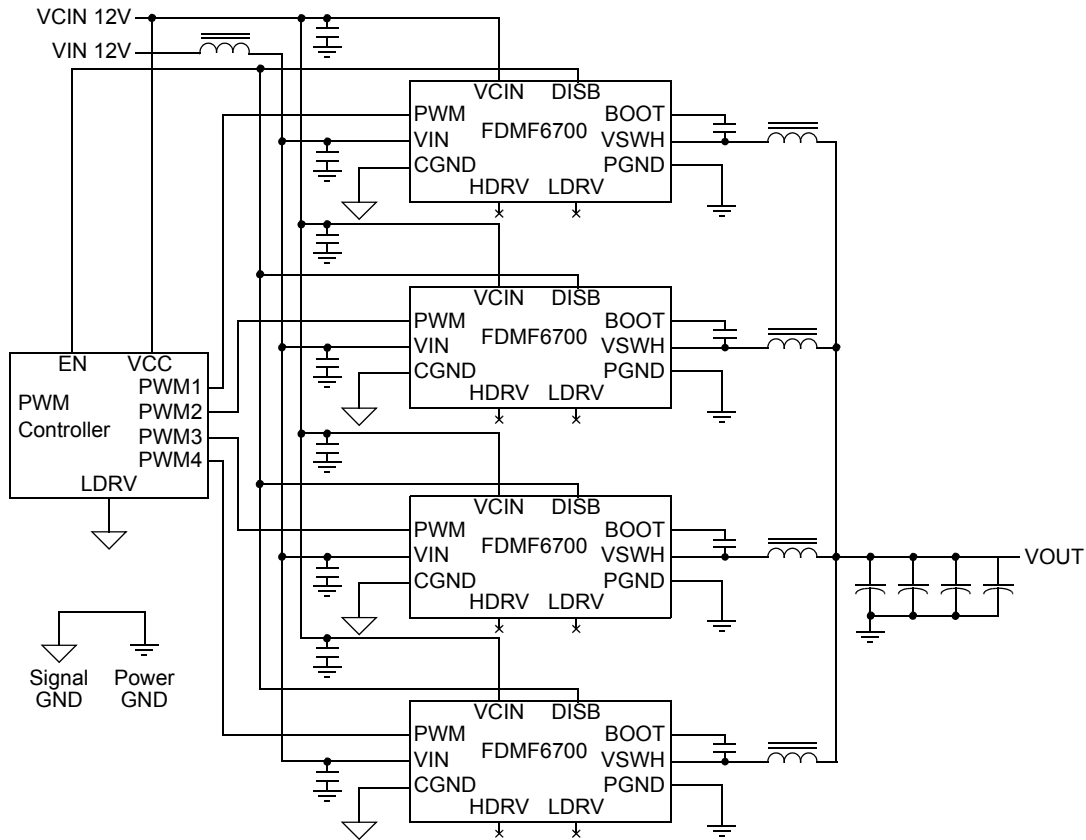


Figure 26. Typical Application

## Application Information

### Supply Capacitor Selection

For the supply input (VCIN) of the FDMF6700, a local ceramic bypass capacitor is recommended to reduce the noise and to supply the peak current. Use at least a 1µF, X7R or X5R capacitor. Keep this capacitor close to the FDMF6700 VCIN and CGND pins.

The average diode forward current,  $I_{F(AVG)}$ , can be estimated by:

$$I_{F(AVG)} = Q_G \times f_{SW} \quad (2)$$

### Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor ( $C_{BOOT}$ ) and the internal diode, as shown in Figure 26. Selection of these components should be done after the high-side MOSFET has been chosen. The required capacitance is determined using the following equation:

$$C_{BOOT} \geq \frac{Q_G}{\Delta V_{BOOT}} \quad (1)$$

where  $Q_G$  is the total gate charge of the high-side MOSFET, and  $\Delta V_{BOOT}$  is the voltage droop allowed on the high-side MOSFET drive. For example, the  $Q_G$  of the internal high-side MOSFET is about 21nC @ 12V<sub>GS</sub>. For an allowed droop of ~300mV, the required bootstrap capacitance is > 100nF. A good quality ceramic capacitor must be used.

where  $f_{SW}$  is the switching frequency of the controller. The peak surge current rating of the internal diode should be checked in-circuit, since this is dependent on the equivalent impedance of the entire bootstrap circuit, including the PCB traces. For applications requiring higher  $I_F$ , an external diode may be used in parallel to the internal diode.

## Module Power Loss Measurement and Calculation

Refer to Figure 27 for module power loss testing method. Power loss calculation are as follows:

- (a)  $P_{IN} = (V_{IN} \times I_{IN}) + (V_{CIN} \times I_{CIN})$  (W)
- (b)  $P_{OUT} = V_O \times I_{OUT}$  (W)
- (c)  $P_{LOSS} = P_{IN} - P_{OUT}$  (W)

## PCB Layout Guideline

Figure 28. shows a proper layout example of FDMF6700 and critical parts. All of high current flow path, such as  $V_{IN}$ , VSWH,  $V_{OUT}$  and GND copper, should be short and wide for better and stable current flow, heat radiation and system performance.

Following is a guideline which the PCB designer should consider:

1. Input bypass capacitors should be close to  $V_{IN}$  and GND pin of FDMF6700 to help reduce input current ripple component induced by switching operation.
2. It is critical that the VSWH copper has minimum area for lower switching noise emission. VSWH copper trace should also be wide enough for high current flow. Other signal routing path, such as PWM IN and BOOT signal, should be considered with care to avoid noise pickup from VSWH copper area.
3. Output inductor location should be as close as possible to the FDMF6700 for lower power loss due to copper trace.
4. Place ceramic bypass capacitor and boot capacitor as close to  $V_{CIN}$  and BOOT pin of FDMF6700 in order to supply stable power. Routing width and length should also be considered.
5. Use multiple Vias on each copper area to interconnect each top, inner and bottom layer to help smooth current flow and heat conduction. Vias should be relatively large and of reasonable inductance.

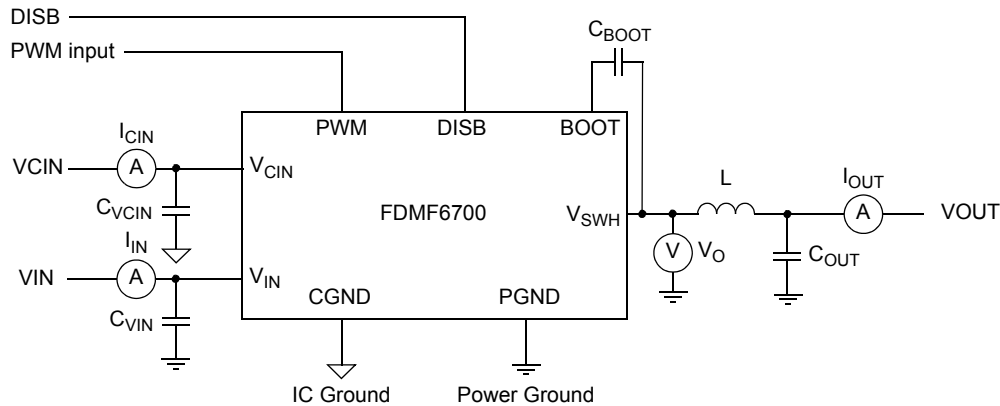


Figure 27. Power Loss Measurement Block Diagram

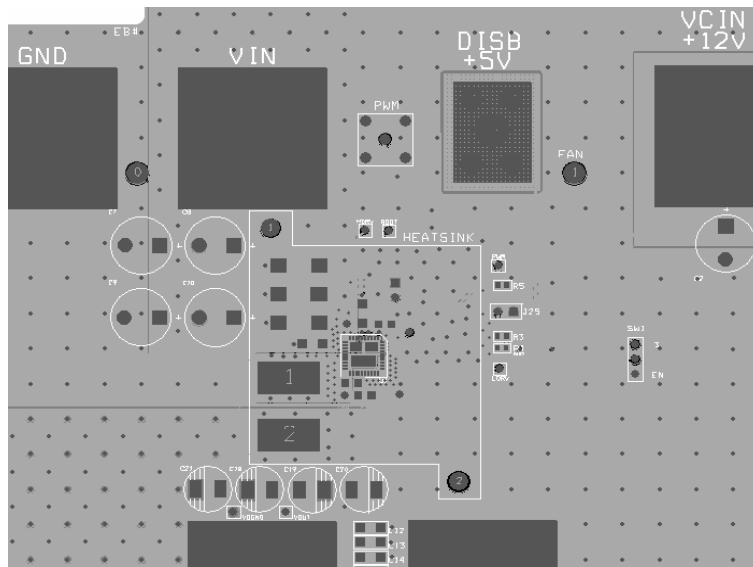
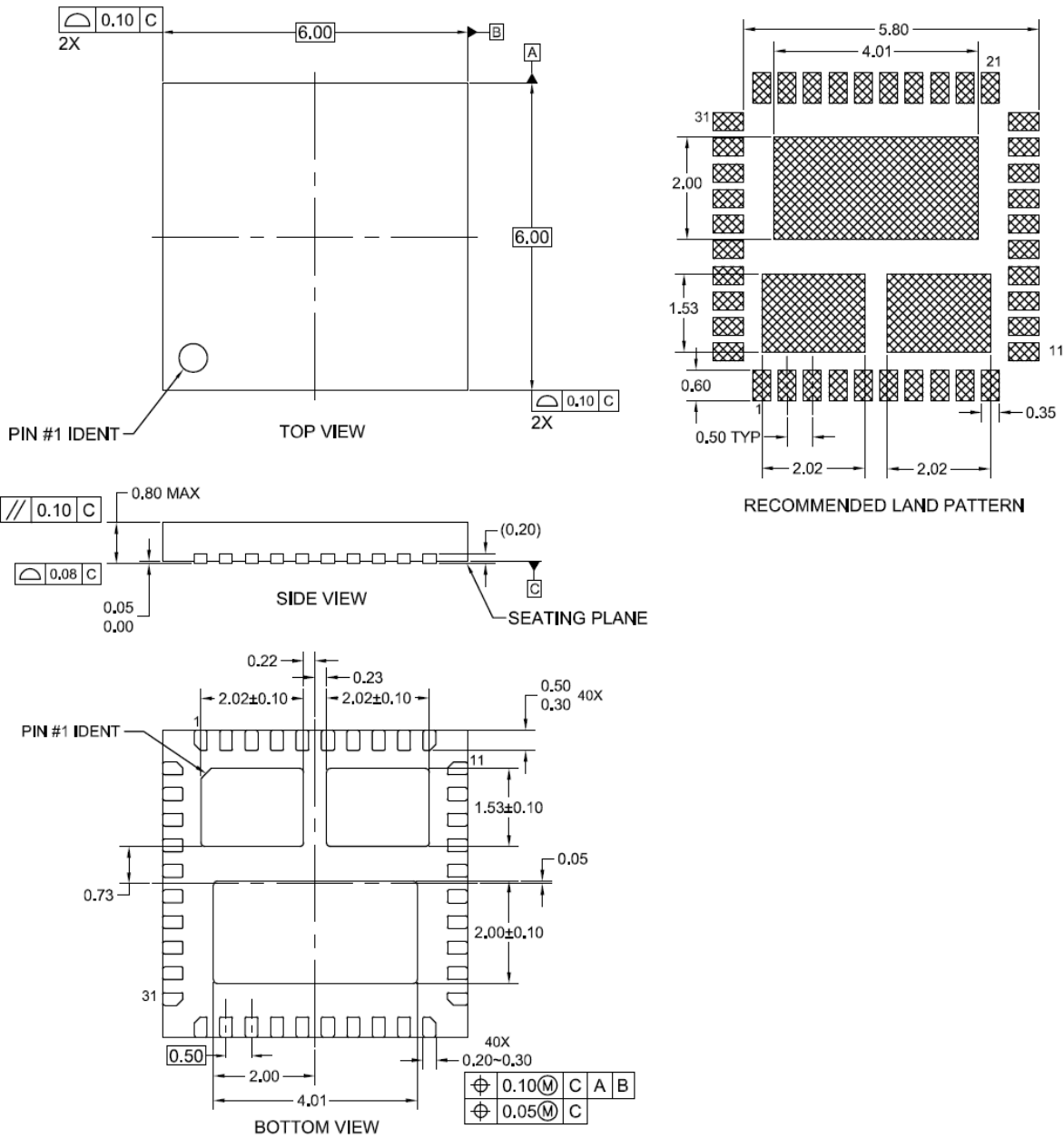


Figure 28. Typical PCB Layout Example (Top View)

## Dimensional Outline and Pad layout




### NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-220, DATED MAY/2005.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DRAWING FILE NAME: MLP40CREV1



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