



**THE DATASHEET OF
MM74HC151SJX**



MM74HC151 8-Channel Digital Multiplexer

General Description

The MM74HC151 high speed Digital multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output HIGH and the Y output LOW.

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

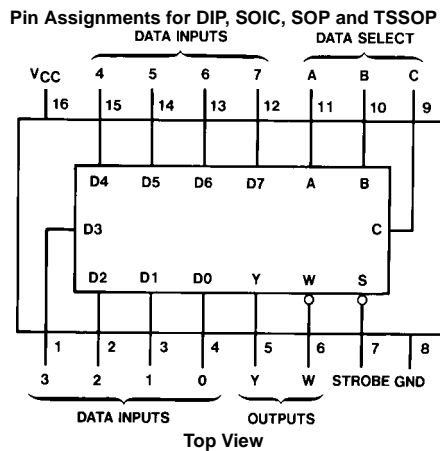
- Typical propagation delay data select to output Y: 26 ns
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent supply current: 80 μ A maximum (74HC)
- High output drive current: 4 mA minimum

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| MM74HC151M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC151SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC151MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC151N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



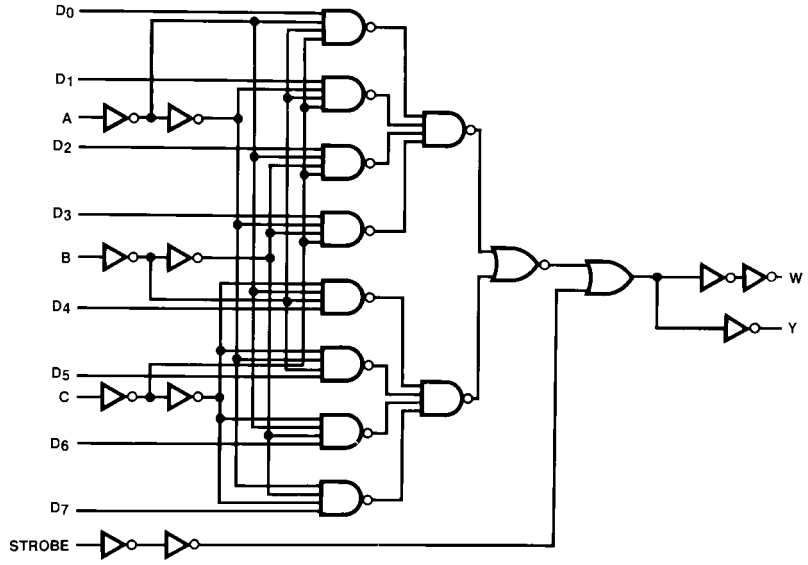
Truth Table

| Inputs | | | | Outputs | |
|--------|---|---|-------------|---------|-----------------|
| Select | | | Strobe S | Y | W |
| C | B | A | | | |
| X | X | X | H | L | H |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

H = HIGH Level, L = LOW Level, X = Don't Care
D0, D1...D7 = the level of the respective D input

MM74HC151

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|--|-------------------------|
| Supply Voltage (V_{CC}) | -0.5 to +7.0V |
| DC Input Voltage (V_{IN}) | -1.5 to $V_{CC} + 1.5V$ |
| DC Output Voltage (V_{OUT}) | -0.5 to $V_{CC} + 0.5V$ |
| Clamp Diode Current (I_{IK}, I_{OK}) | ± 20 mA |
| DC Output Current, per pin (I_{OUT}) | ± 25 mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | ± 50 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature (T_L) | 260°C |
| (Soldering 10 seconds) | |

Recommended Operating Conditions

| | Min | Max | Units |
|--|-----|----------|-------|
| Supply Voltage (V_{CC}) | 2 | 6 | V |
| DC Input or Output Voltage (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Operating Temperature Range (T_A) | -40 | +85 | °C |
| Input Rise or Fall Times (t_r, t_f) | | | |
| $V_{CC} = 2.0V$ | | 1000 | ns |
| $V_{CC} = 4.5V$ | | 500 | ns |
| $V_{CC} = 6.0V$ | | 400 | ns |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: — 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | | $T_A = -40 \text{ to } 85^\circ C$ | | | $T_A = -55 \text{ to } 125^\circ C$ | | | Units |
|----------|-----------------------------------|--|----------|--------------------|-------------------|-----------|------------------------------------|--|-------------------|-------------------------------------|---------|---|-------|
| | | | | Typ | Guaranteed Limits | | Guaranteed Limits | | Guaranteed Limits | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | | | | | V | |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | | | | V | | |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | | | | V | | |
| V_{IL} | Maximum LOW Level Input Voltage | | 2.0V | | 0.5 | 0.5 | 0.5 | | | | | V | |
| | | | 4.5V | | 1.35 | 1.35 | 1.35 | | | | V | | |
| | | | 6.0V | | 1.8 | 1.8 | 1.8 | | | | V | | |
| V_{OH} | Minimum HIGH Level Output Voltage | $V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT} \leq 20 \mu A$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | | | | | V | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | | | | V | | |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | | | | V | | |
| | | $V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT} \leq 4.0 \text{ mA}$ $ I_{OUT} \leq 5.2 \text{ mA}$ | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | | | | V | | |
| | | | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | | | | V | | |
| | | | | | | | | | | | | | |
| V_{OL} | Maximum LOW Level Output Voltage | $V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT} \leq 20 \mu A$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | | | | | V | |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | | | | V | | |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | | | | V | | |
| | | $V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT} \leq 4.0 \text{ mA}$ $ I_{OUT} \leq 5.2 \text{ mA}$ | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | | | | V | | |
| | | | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | | | | V | | |
| | | | | | | | | | | | | | |
| I_{IN} | Maximum Input Current | $V_{IN} = V_{CC} \text{ or } GND$ | 6.0V | | ± 0.1 | ± 1.0 | ± 1.0 | | | | μA | | |
| I_{CC} | Maximum Quiescent Supply Current | $V_{IN} = V_{CC} \text{ or } GND$ $I_{OUT} = 0 \mu A$ | 6.0V | | 8.0 | 80 | 160 | | | | μA | | |

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

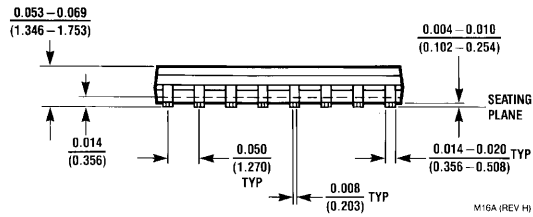
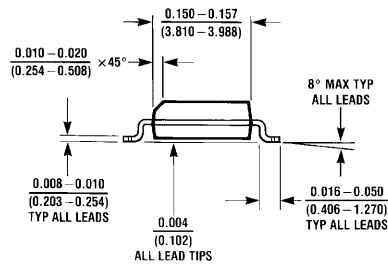
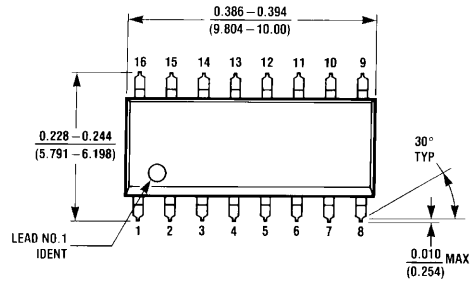
| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|-----------------------|---|------------|-----|------------------|-------|
| t_{PHL} , t_{PLH} | Maximum Propagation Delay A, B or C to Y | | 26 | 35 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay A, B or C to W | | 27 | 35 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Any D to Y | | 22 | 29 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay any D to W | | 24 | 32 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Strobe to Y | | 17 | 23 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Strobe to W | | 16 | 21 | ns |

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

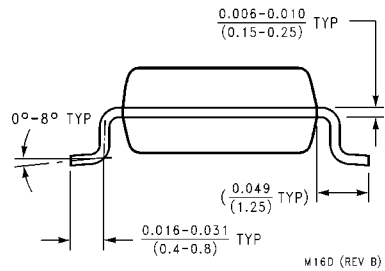
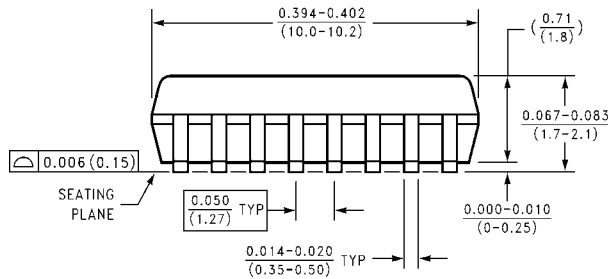
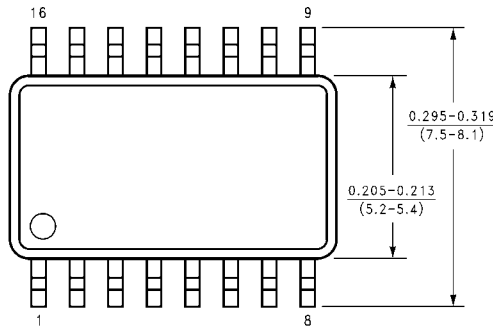
| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | $T_A = -40$ to $85^\circ C$ | $T_A = -55$ to $125^\circ C$ | Units |
|-----------------------|---|---------------|----------|--------------------|-------------------|-----------------------------|------------------------------|-------|
| | | | | Typ | Guaranteed Limits | | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay A, B or C to Y | | 2.0V | 90 | 205 | 256 | 300 | ns |
| | | | 4.5V | 31 | 41 | 51 | 60 | ns |
| | | | 6.0V | 26 | 35 | 44 | 51 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay A, B or C to W | | 2.0V | 95 | 205 | 256 | 300 | ns |
| | | | 4.5V | 32 | 41 | 51 | 60 | ns |
| | | | 6.0V | 27 | 35 | 44 | 51 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay any D to Y | | 2.0V | 70 | 195 | 244 | 283 | ns |
| | | | 4.5V | 27 | 39 | 49 | 57 | ns |
| | | | 6.0V | 23 | 33 | 41 | 48 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay any D to W | | 2.0V | 75 | 185 | 231 | 268 | ns |
| | | | 4.5V | 29 | 37 | 46 | 54 | ns |
| | | | 6.0V | 25 | 32 | 40 | 46 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Strobe to Y | | 2.0V | 50 | 140 | 175 | 203 | ns |
| | | | 4.5V | 21 | 28 | 35 | 41 | ns |
| | | | 6.0V | 18 | 24 | 30 | 35 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Strobe to W | | 2.0V | 45 | 127 | 159 | 185 | ns |
| | | | 4.5V | 20 | 25 | 32 | 37 | ns |
| | | | 6.0V | 17 | 22 | 28 | 32 | ns |
| t_{TLH} , t_{THL} | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns |
| | | | 4.5V | 8 | 15 | 19 | 22 | ns |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns |
| C_{PD} | Power Dissipation Capacitance (Note 5) | (per package) | | 110 | | | | pF |
| C_{IN} | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

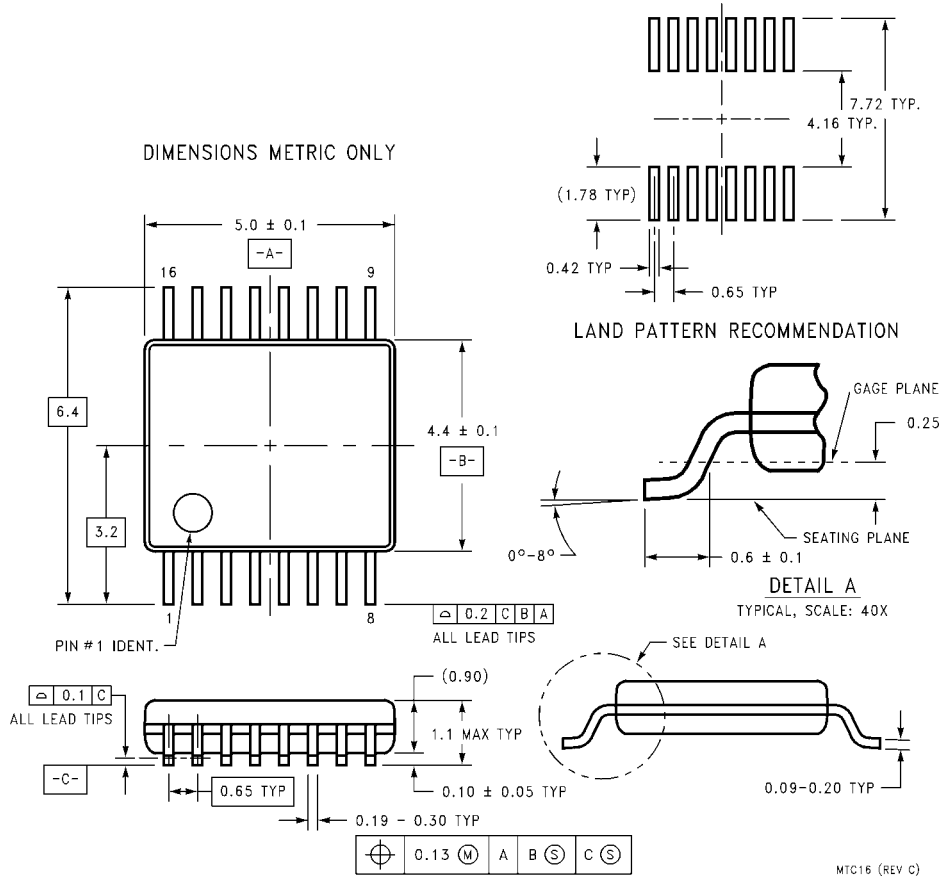


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**



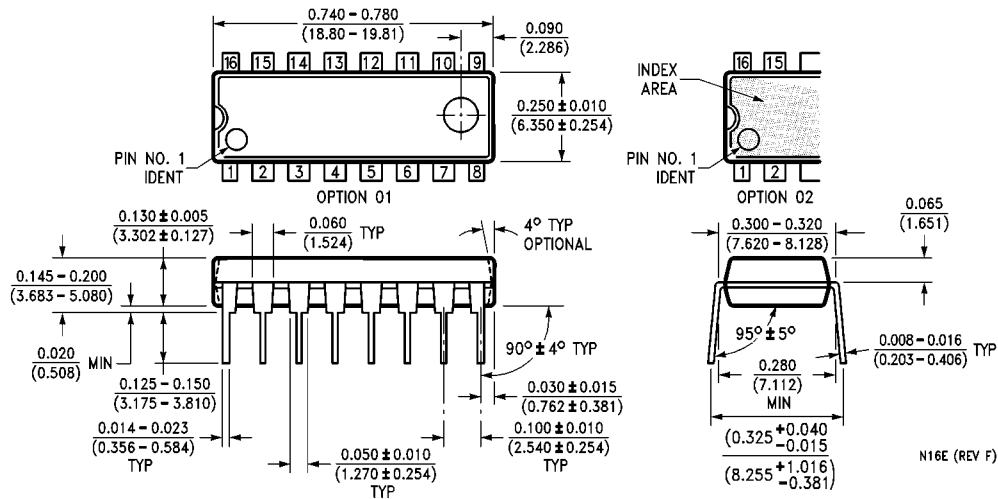
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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