



**THE DATASHEET OF
SN74ALS240A-1NSR**



SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SDAS214E – DECEMBER 1982 – REVISED AUGUST 2002

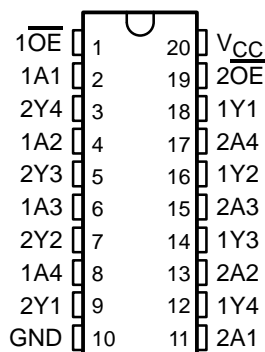
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading

SN54ALS240A, SN54AS240A . . . J OR W PACKAGE
SN74ALS240A . . . DB, DW, N, OR NS PACKAGE
SN74AS240A . . . DW OR N PACKAGE
(TOP VIEW)

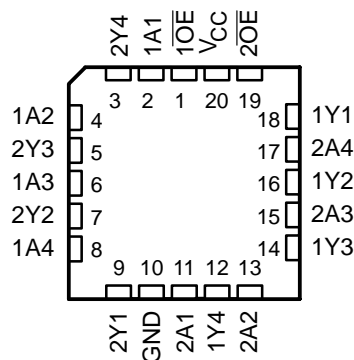
description/ordering information

These octal buffers/drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. When these devices are used with the 'ALS241, 'AS241A, 'ALS244, and 'AS244A devices, the circuit designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs. These devices feature high fan-out and improved fan-in.

The -1 version of SN74ALS240A is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is 48 mA. There is no -1 version of the SN54ALS240A.



SN54ALS240A, SN54AS240A . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|------------------|-----------|---------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN74ALS240AN | SN74ALS240AN |
| | | | SN74ALS240A-1N | SN74ALS240A-1N |
| | | | SN74AS240AN | SN74AS240AN |
| | SOIC – DW | Tube | SN74ALS240ADW | ALS240A |
| | | | SN74ALS240ADWR | |
| | | Tape and reel | SN74ALS240A-1DW | ALS240A-1 |
| | | | SN74ALS240A-1DWR | |
| | | Tube | SN74AS240ADW | AS240A |
| | | | SN74AS240ADWR | |
| | SOP – NS | Tape and reel | SN74ALS240ANSR | ALS240A |
| | | | SN74ALS240A-1NSR | ALS240A-1 |
| | SSOP – DB | Tape and reel | SN74ALS240ADBR | G240A |
| SN74ALS240A-1DBR | | | G240A-1 | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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description/ordering information (continued)

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|------|-----------------------|------------------|
| -55°C to 125°C | CDIP – J | Tube | SNJ54ALS240AJ | SNJ54ALS240AJ |
| | | | SNJ54AS240AJ | SNJ54AS240AJ |
| | CFP – W | Tube | SNJ54ALS240AW | SNJ54ALS240AW |
| | | | SNJ54AS240AW | SNJ54AS240AW |
| | LCCC – FK | Tube | SNJ54ALS240AFK | SNJ54ALS240AFK |
| | | | SNJ54AS240AFK | SNJ54AS240AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each buffer)

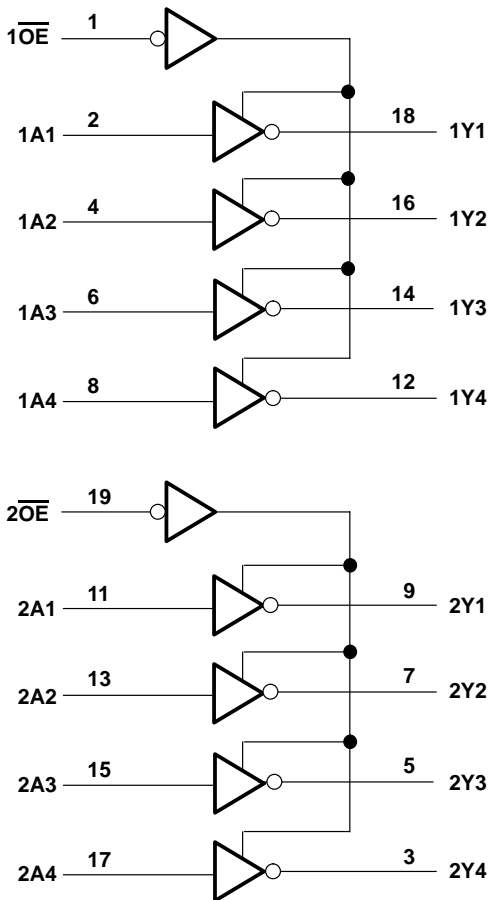
| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |



SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 1): | |
| DB package | 70°C/W |
| DW package | 58°C/W |
| N package | 70°C/W |
| NS package | 60°C/W |
| Storage temperature range, T_{Stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-------------------------|-----|-----|------|
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | | V |
| V _{IL} | Low-level input voltage | SN54ALS240A | | 0.7 | V |
| | | SN74ALS240A, 'AS240A | | 0.8 | |
| I _{OH} | High-level output current | SN54ALS240A, SN54AS240A | | -12 | mA |
| | | SN74ALS240A, SN74AS240A | | -15 | |
| I _{OL} | Low-level output current | SN54ALS240A | | 12 | mA |
| | | SN74ALS240A | | 24 | |
| | | | | 48† | |
| | | | | 64 | |
| T _A | Operating free-air temperature | SN54ALS240A, SN54AS240A | | -55 | °C |
| | | SN74ALS240A, SN74AS240A | | 0 | |

† Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54ALS240A | | SN74ALS240A | | UNIT | |
|------------------|---|--------------------------|------|---------------------|------|------|------|
| | | MIN | TYP‡ | MAX | MIN | | TYP‡ |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | V | |
| V _{OH} | V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA | V _{CC} - 2 | | V _{CC} - 2 | | V | |
| | V _{CC} = 4.5 V | I _{OH} = -3 mA | 2.4 | 3.2 | 2.4 | | 3.2 |
| | | I _{OH} = -12 mA | 2 | | | | |
| V _{OL} | V _{CC} = 4.5 V | I _{OL} = -15 mA | | | 2 | | |
| | | I _{OL} = 12 mA | 0.25 | 0.4 | 0.25 | 0.4 | |
| | | I _{OL} = 24 mA | | | 0.35 | 0.5 | |
| | | I _{OL} = 48 mA† | | | 0.35 | 0.5 | |
| I _{OZH} | V _{CC} = 5.5 V, V _O = 2.7 V | | | 20 | | μA | |
| I _{OZL} | V _{CC} = 5.5 V, V _O = 0.4 V | | | -20 | | μA | |
| I _I | V _{CC} = 5.5 V, V _I = 7 V | | | 0.1 | | mA | |
| I _{IH} | V _{CC} = 5.5 V, V _I = 2.7 V | | | 20 | | μA | |
| I _{IL} | V _{CC} = 5.5 V, V _I = 0.4 V | | | -0.1 | | mA | |
| I _{O§} | V _{CC} = 5.5 V, V _O = 2.25 V | -20 | | -112 | -30 | -112 | mA |
| I _{CC} | V _{CC} = 5.5 V | Outputs high | | 4 | 11 | 4 | 11 |
| | | Outputs low | | 13 | 23 | 13 | 23 |
| | | Outputs disabled | | 14 | 25 | 14 | 25 |

† Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.



SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54AS240A | | SN74AS240A | | UNIT |
|-----------------|--|---------------------------|----------------------|------|--------------|------|---------------|
| | | | MIN | TYP† | MAX | MIN | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | -1.2 | | -1.2 | | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ | $I_{OH} = -2\text{ mA}$ | $V_{CC} - 2$ | | $V_{CC} - 2$ | | V |
| | | $I_{OH} = -3\text{ mA}$ | 2.4 | 3.4 | 2.4 | 3.4 | |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -12\text{ mA}$ | 2.4 | | | | |
| | | $I_{OH} = -15\text{ mA}$ | | | 2.4 | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 48\text{ mA}$ | 0.27 | 0.55 | | | V |
| | | $I_{OL} = 64\text{ mA}$ | | | 0.31 | 0.55 | |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.7\text{ V}$ | 50 | | 50 | | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.4\text{ V}$ | -50 | | -50 | | μA |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | 0.1 | | 0.1 | | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | 20 | | 20 | | μA |
| I_{IL} | A inputs | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | | -1 | | mA |
| | \overline{OE} inputs | | | | -0.5 | | |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.25\text{ V}$ | -50 | -150 | -50 | -150 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | Outputs high | 11 | 17 | 11 | 17 | mA |
| | | Outputs low | 51 | 75 | 51 | 75 | |
| | | Outputs disabled | 24 | 38 | 24 | 38 | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$ | | | | UNIT |
|-----------|-----------------|-------------|---|-----|-------------|-----|------|
| | | | SN54ALS240A | | SN74ALS240A | | |
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 2 | 22 | 2 | 9 | ns |
| t_{PHL} | | | 2 | 11 | 2 | 9 | |
| t_{PZH} | \overline{OE} | Y | 4 | 34 | 5 | 13 | ns |
| t_{PZL} | | | 5 | 26 | 5 | 18 | |
| t_{PHZ} | \overline{OE} | Y | 1 | 15 | 2 | 10 | ns |
| t_{PLZ} | | | 3 | 24 | 3 | 12 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|-----------------|----------------|--|------|------------|-----|------|
| | | | SN54AS240A | | SN74AS240A | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | 1 | 7 | 1 | 6.5 | ns |
| t _{PHL} | | | 1.2 | 6.5 | 1.2 | 6.5 | |
| t _{PZH} | \overline{OE} | Y | 1 | 7 | 1 | 6.4 | ns |
| t _{PZL} | | | 1.1 | 9.5 | 1.1 | 9 | |
| t _{PHZ} | \overline{OE} | Y | 1.2 | 5.5 | 1.2 | 5 | ns |
| t _{PLZ} | | | 1.5 | 12.5 | 1.5 | 9.5 | |

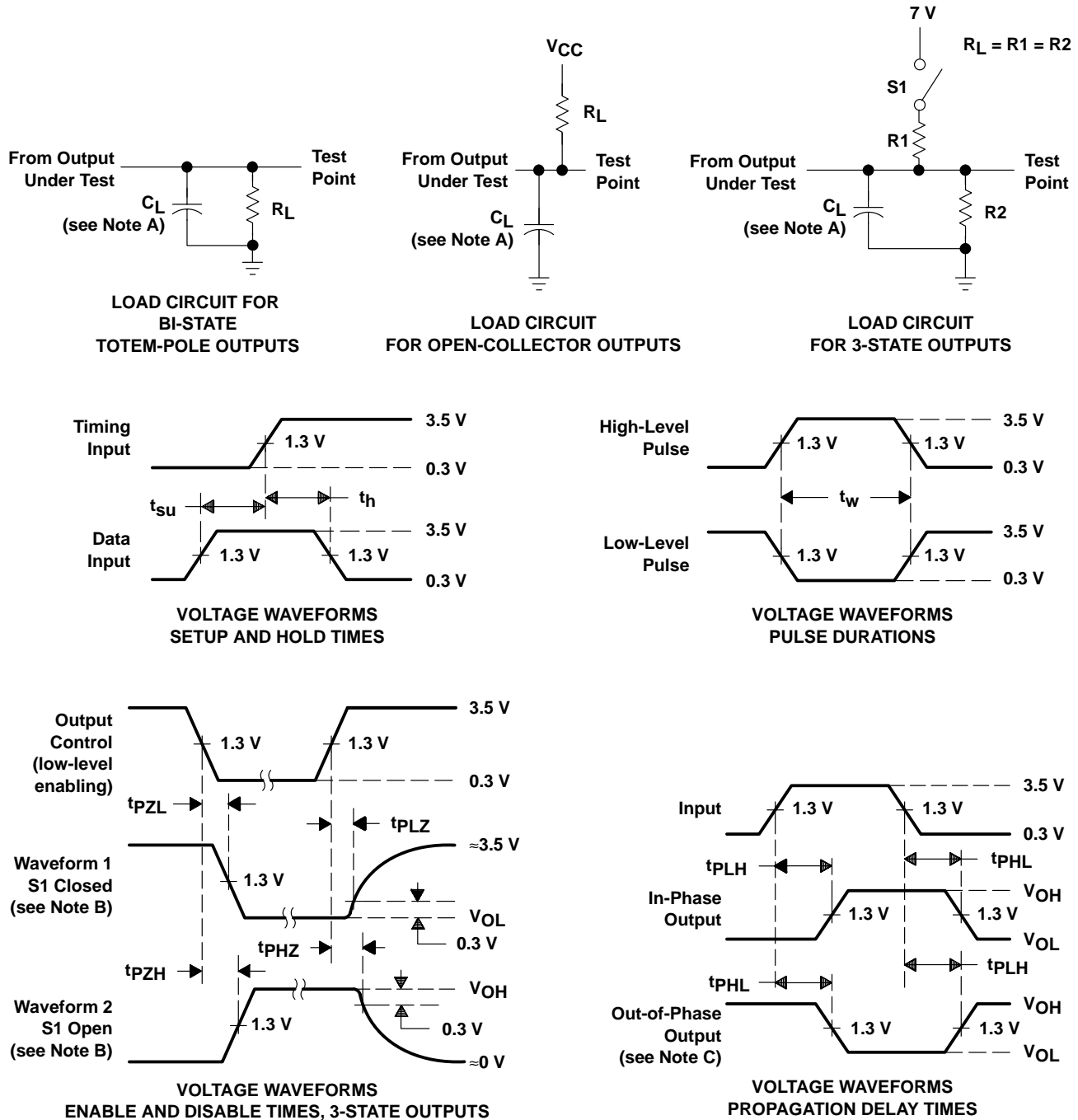
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 5962-8859101SA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8859101SA SNJ54ALS240AW | Samples |
| JM38510/38301B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 38301B2A | Samples |
| JM38510/38301BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 38301BRA | Samples |
| M38510/38301B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 38301B2A | Samples |
| M38510/38301BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 38301BRA | Samples |
| SN54ALS240AJ | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54ALS240AJ | Samples |
| SN74ALS240A-1DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS240A-1 | Samples |
| SN74ALS240A-1N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS240A-1N | Samples |
| SN74ALS240A-1NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS240A-1 | Samples |
| SN74ALS240ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | G240A | Samples |
| SN74ALS240ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS240A | Samples |
| SN74ALS240ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS240A | Samples |
| SN74ALS240AN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS240AN | Samples |
| SN74ALS240ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS240A | Samples |
| SN74AS240ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS240A | Samples |
| SN74AS240ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS240A | Samples |
| SN74AS240AN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS240AN | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| SN74AS240ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS240A | Samples |
| SNJ54ALS240AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54ALS 240AFK | Samples |
| SNJ54ALS240AJ | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54ALS240AJ | Samples |
| SNJ54ALS240AW | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8859101SA SNJ54ALS240AW | Samples |
| SNJ54AS240AJ | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54AS240AJ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS240A, SN54AS240A, SN74ALS240A, SN74AS240A :

- Catalog: [SN74ALS240A](#), [SN74AS240A](#)
- Military: [SN54ALS240A](#), [SN54AS240A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS240A-1NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74ALS240ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ALS240ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ALS240ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AS240ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AS240ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS240A-1NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ALS240ADBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74ALS240ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ALS240ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AS240ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AS240ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

EXAMPLE BOARD LAYOUT

DB0020A

TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/A 12/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/A 12/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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