



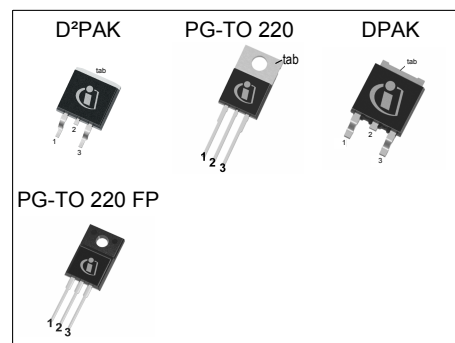
**THE DATASHEET OF
IPP60R380P6**



MOSFET

600V CoolMOS™ P6 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ P6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

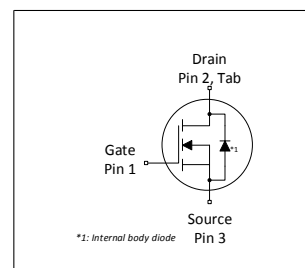


Features

- Increased MOSFET dv/dt ruggedness
- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound

Potential applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.



Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	380	mΩ
$Q_{g,typ}$	19	nC
$I_{D,pulse}$	29	A
$E_{oss@400V}$	2.7	μJ
Body diode di/dt	500	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPB60R380P6	PG-TO263-3	6R380P6	see Appendix A
IPP60R380P6	PG-TO220-3		
IPD60R380P6	PG-TO252-3		
IPA60R380P6	PG-TO220 FullPAK		

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600V CoolMOS™ P6 Power Transistor

IPB60R380P6, IPP60R380P6, IPD60R380P6, IPA60R380P6

1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	10.6 6.7	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	29	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	210	mJ	$I_D=1.8\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.32	mJ	$I_D=1.8\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, repetitive	I_{AR}	-	-	1.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation (Non FullPAK) TO-220, TO-247	P_{tot}	-	-	83	W	$T_C=25^\circ\text{C}$
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	31	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque (Non FullPAK) TO-220, TO-247	-	-	-	60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	9.2	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	29	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di _f /dt	-	-	500	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{ min}$

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics (Non FullPAK) TO-220, TO-247

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

Table 5 Thermal characteristics TO-252

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

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IPB60R380P6, IPP60R380P6, IPD60R380P6, IPA60R380P6

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4.0	4.5	V	$V_{DS}=V_{GS}, I_D=0.32mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=600, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.342 0.889	0.380	Ω	$V_{GS}=10V, I_D=3.8A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=3.8A, T_j=150^\circ\text{C}$
Gate resistance	R_G	-	7.8	-	Ω	$f=1\text{MHz}$, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	877	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Output capacitance	C_{oss}	-	42	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	33	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	135	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.8A,$ $R_G=3.4\Omega$; see table 9
Rise time	t_r	-	6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.8A,$ $R_G=3.4\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	33	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.8A,$ $R_G=3.4\Omega$; see table 9
Fall time	t_f	-	7	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.8A,$ $R_G=3.4\Omega$; see table 9

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	5.4	-	nC	$V_{DD}=400V, I_D=4.8A, V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	7	-	nC	$V_{DD}=400V, I_D=4.8A, V_{GS}=0$ to 10V
Gate charge total	Q_g	-	19	-	nC	$V_{DD}=400V, I_D=4.8A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	6.1	-	V	$V_{DD}=400V, I_D=4.8A, V_{GS}=0$ to 10V

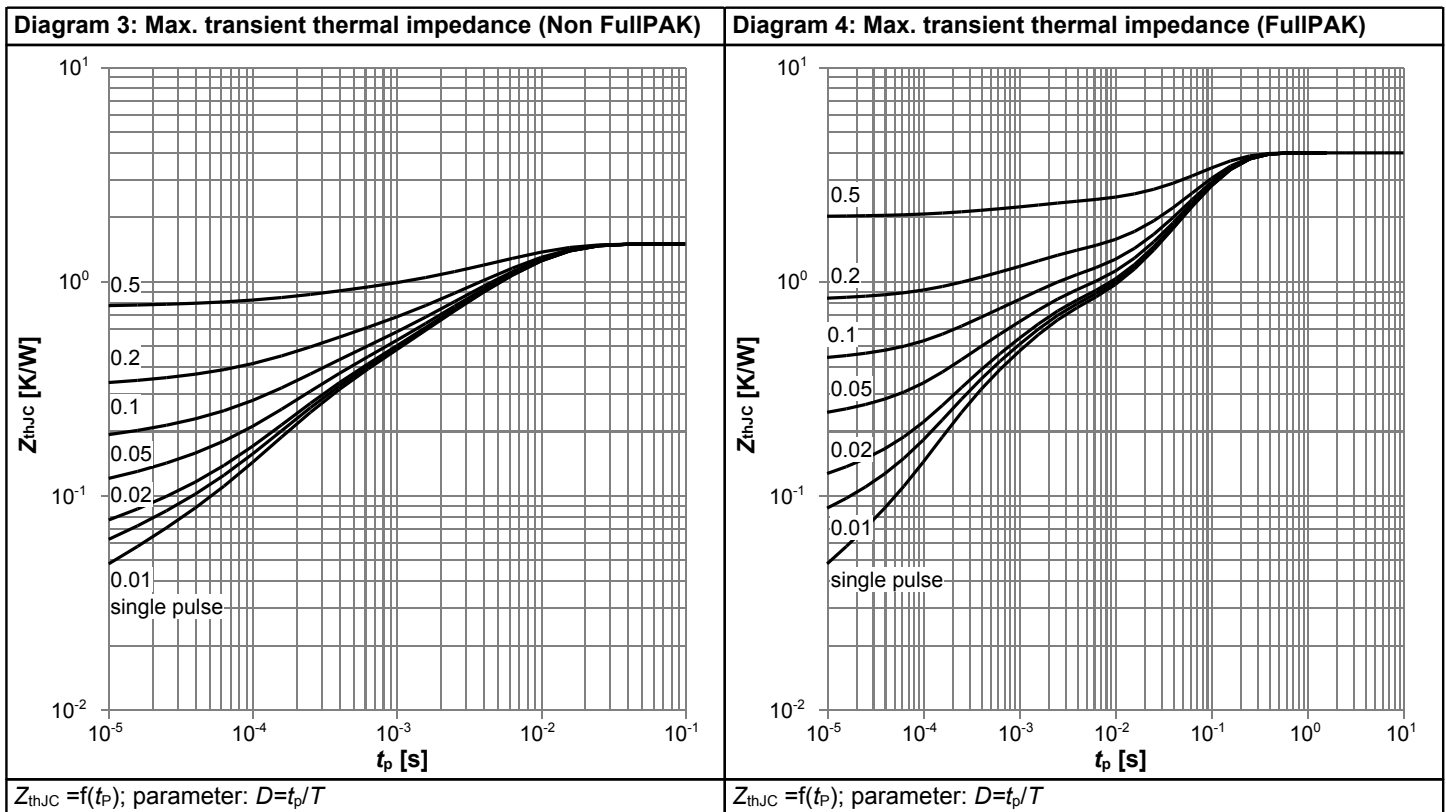
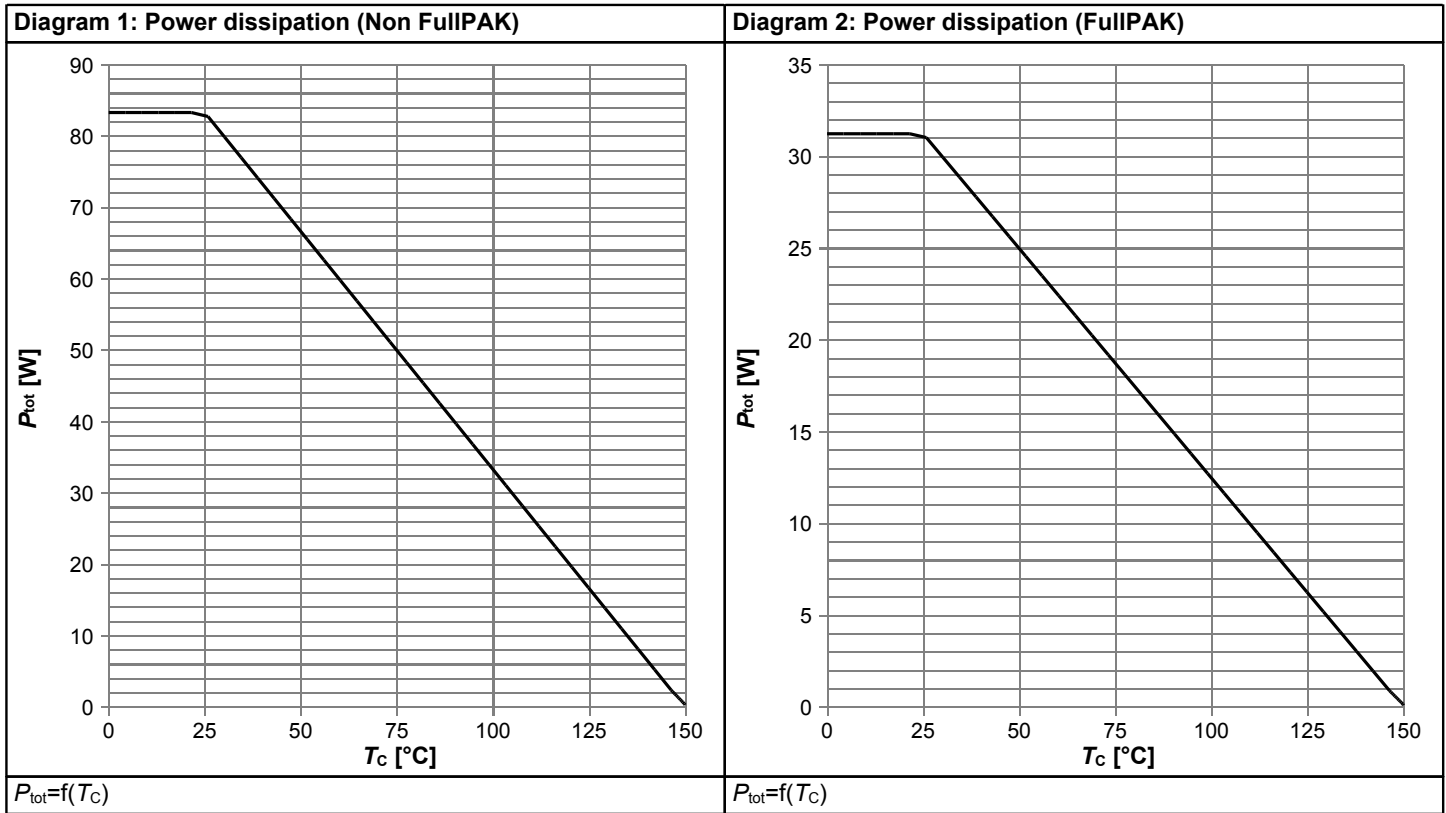
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=4.8A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	232	-	ns	$V_R=400V, I_F=4.8A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	2.1	-	μC	$V_R=400V, I_F=4.8A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	17	-	A	$V_R=400V, I_F=4.8A, di_F/dt=100A/\mu s$; see table 8

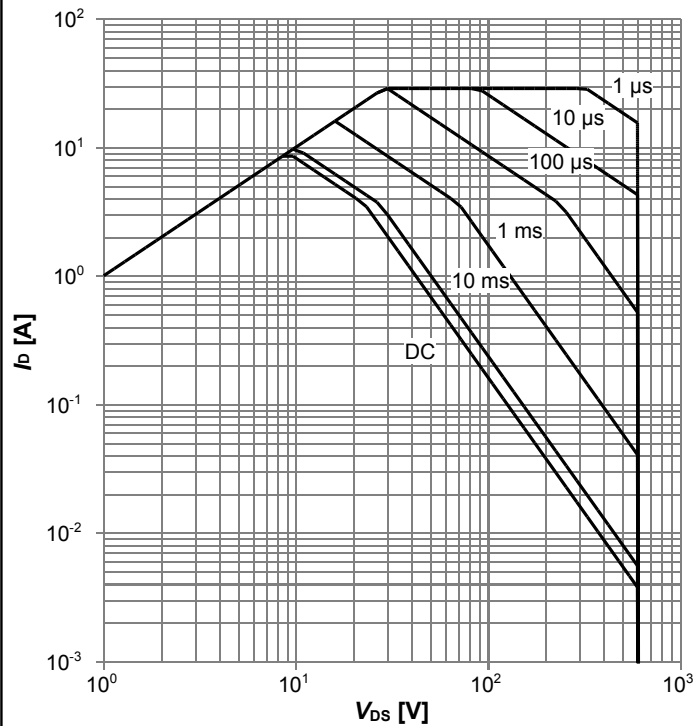
4 Electrical characteristics diagrams



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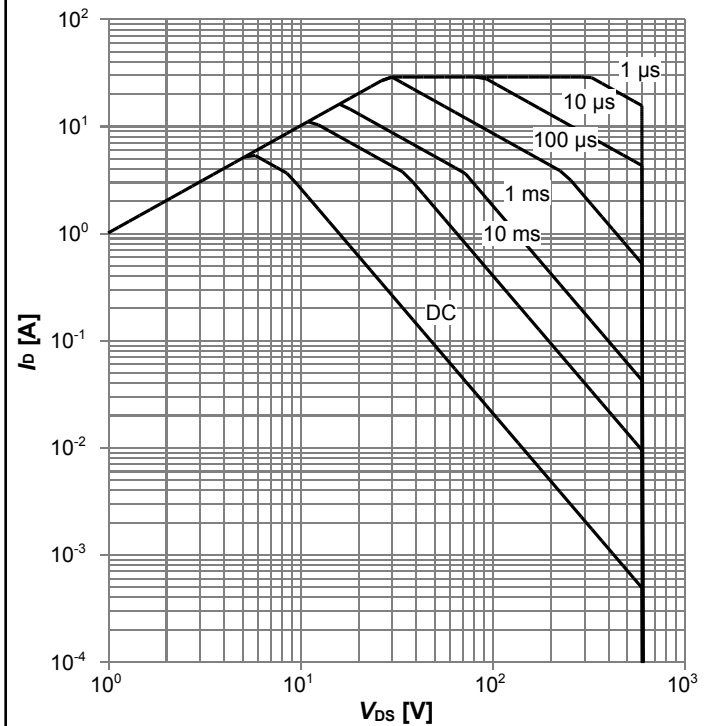
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Diagram 5: Safe operating area (Non FullIPAK)



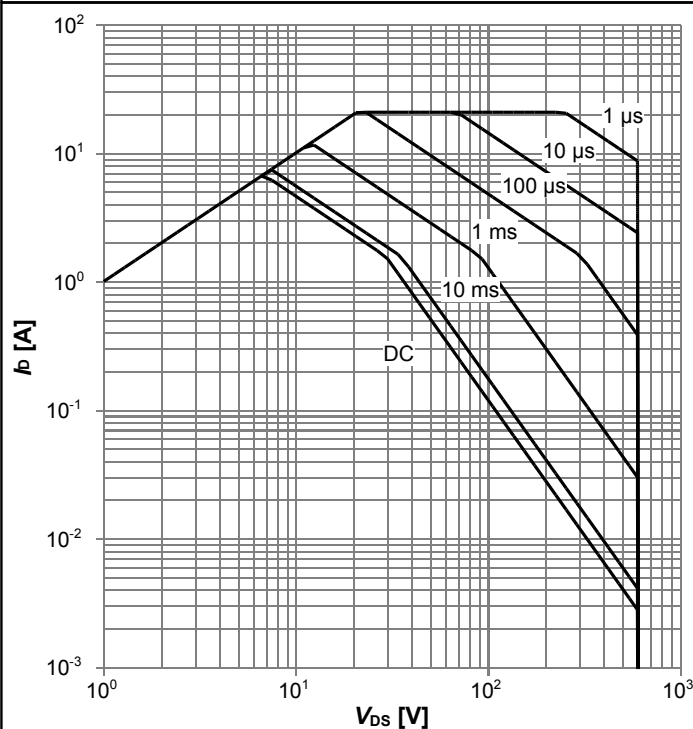
$I_D=f(V_{DS}); T_C=25^\circ\text{C}; D=0$; parameter: t_p

Diagram 6: Safe operating area (FullIPAK)



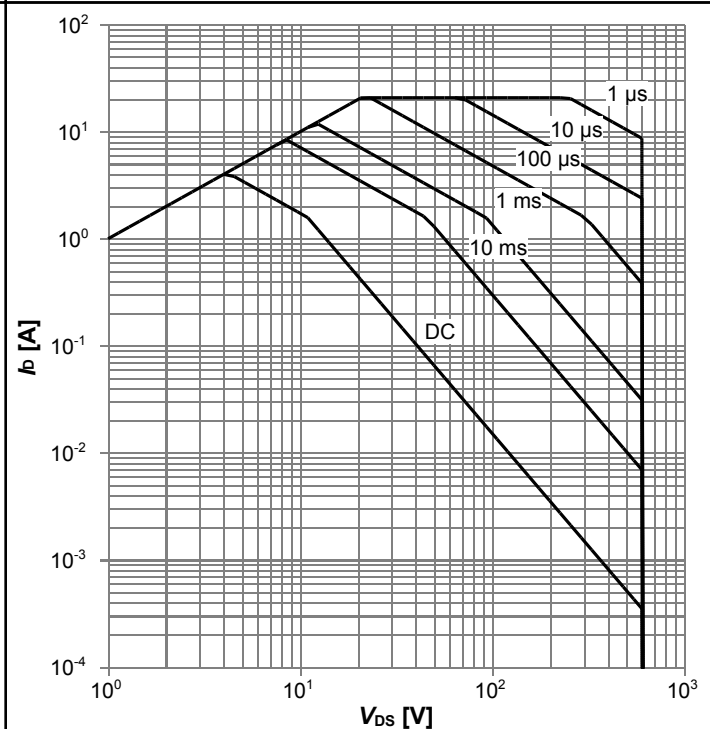
$I_D=f(V_{DS}); T_C=25^\circ\text{C}; D=0$; parameter: t_p

Diagram 7: Safe operating area (Non FullIPAK)



$I_D=f(V_{DS}); T_C=80^\circ\text{C}; D=0$; parameter: t_p

Diagram 8: Safe operating area (FullIPAK)

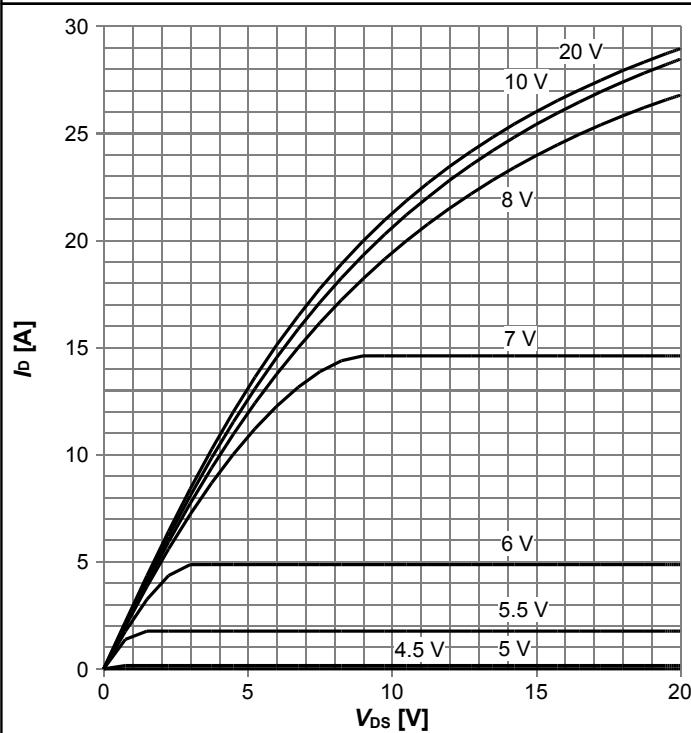


$I_D=f(V_{DS}); T_C=80^\circ\text{C}; D=0$; parameter: t_p

600V CoolMOS™ P6 Power Transistor

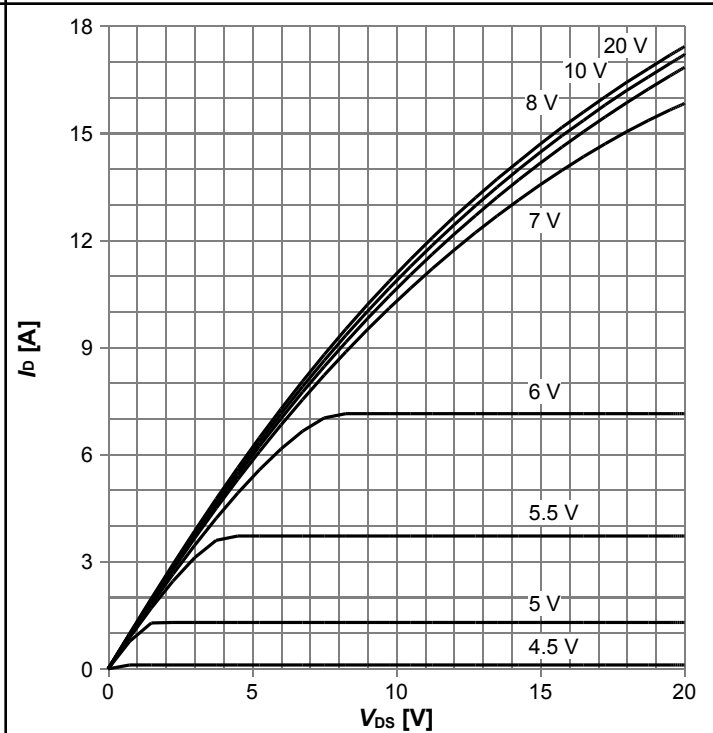
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Diagram 9: Typ. output characteristics



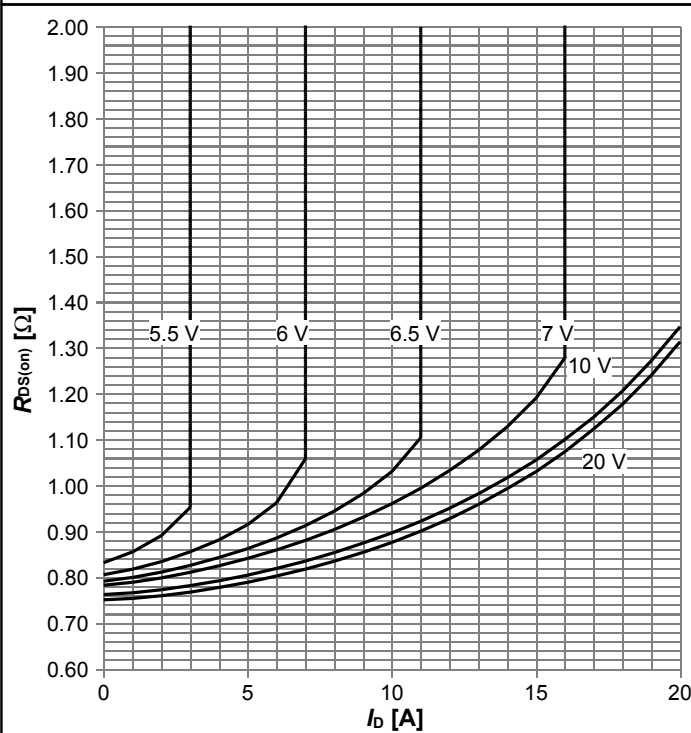
$I_D=f(V_{DS})$; $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 10: Typ. output characteristics



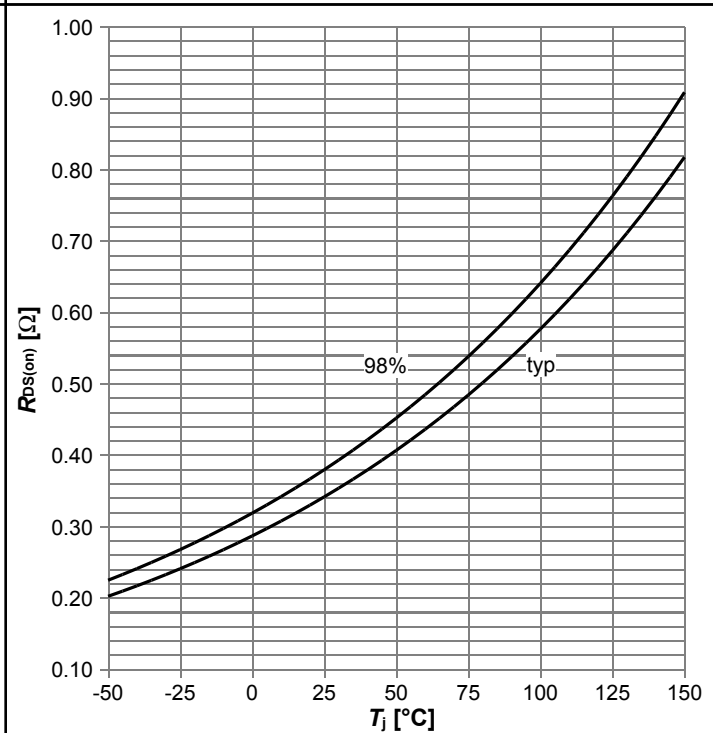
$I_D=f(V_{DS})$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D)$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

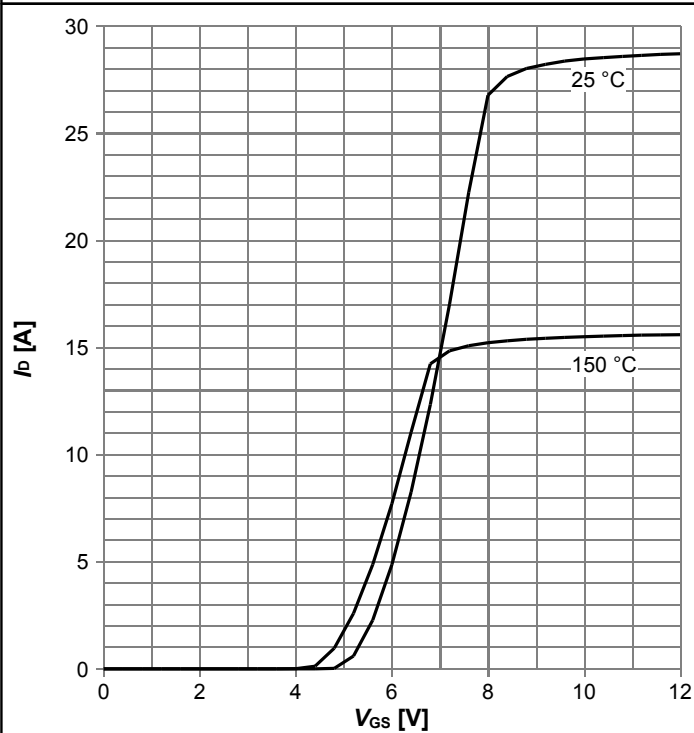
Diagram 12: Drain-source on-state resistance



$R_{DS(on)}=f(T_j)$; $I_D=3.8\text{ A}$; $V_{GS}=10\text{ V}$

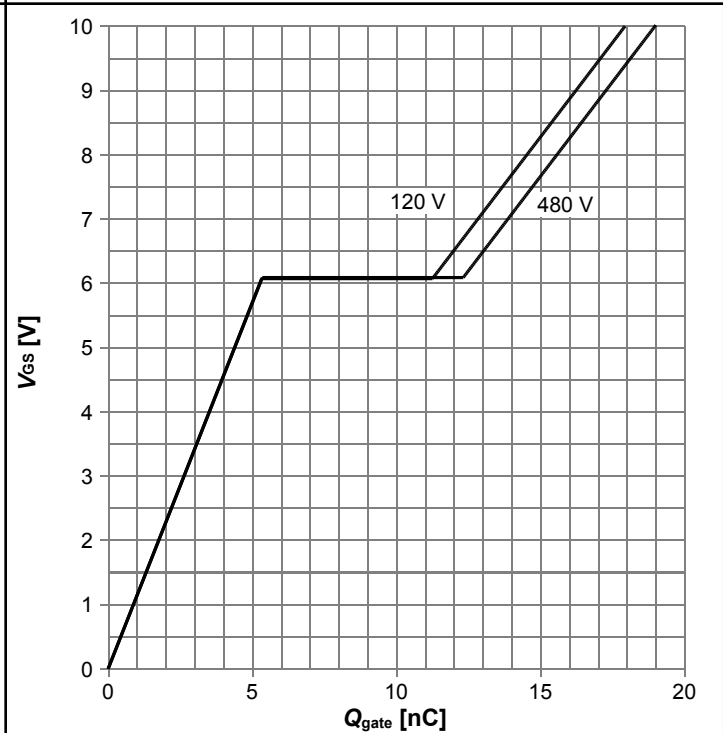
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Diagram 13: Typ. transfer characteristics



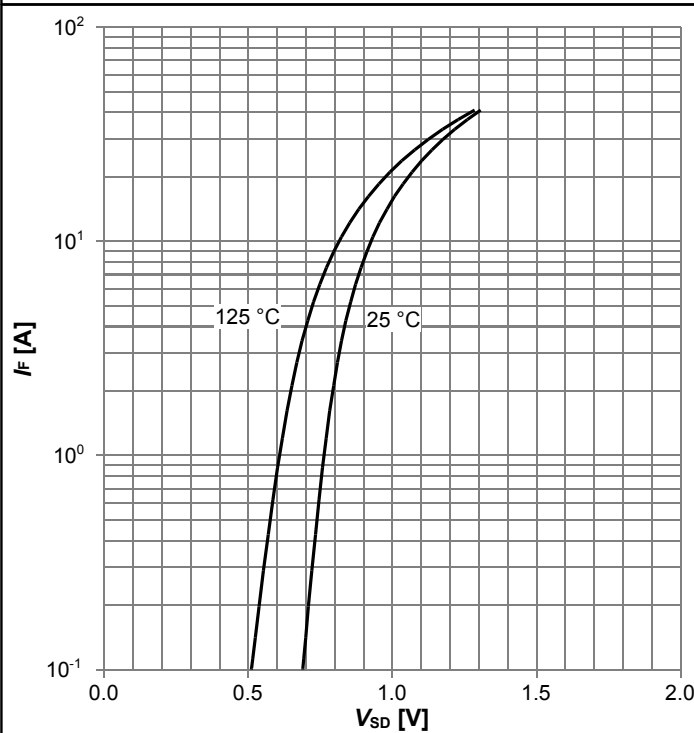
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 14: Typ. gate charge



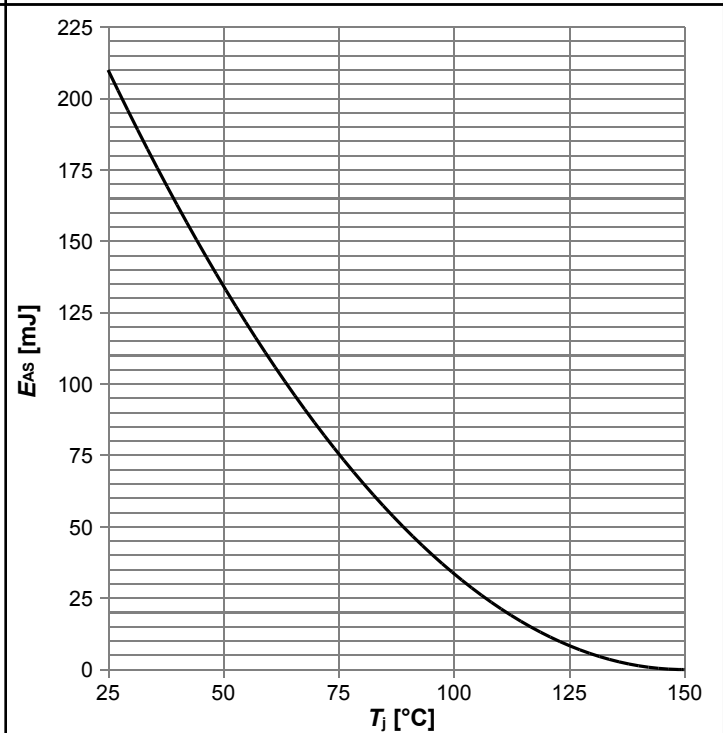
$V_{GS} = f(Q_{gate})$; $I_D = 4.8$ A pulsed; parameter: V_{DD}

Diagram 15: Forward characteristics of reverse diode



$I_F = f(V_{SD})$; parameter: T_j

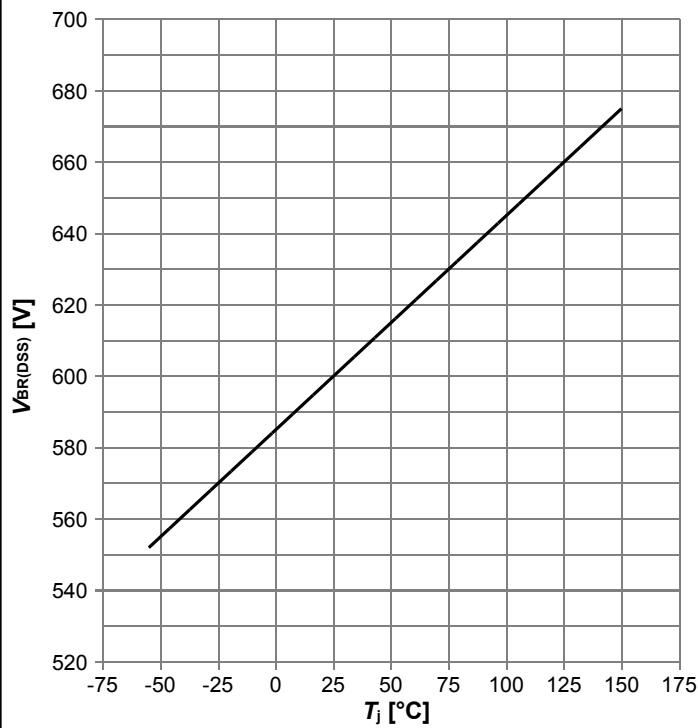
Diagram 16: Avalanche energy



$E_{AS} = f(T_j)$; $I_D = 1.8$ A; $V_{DD} = 50$ V

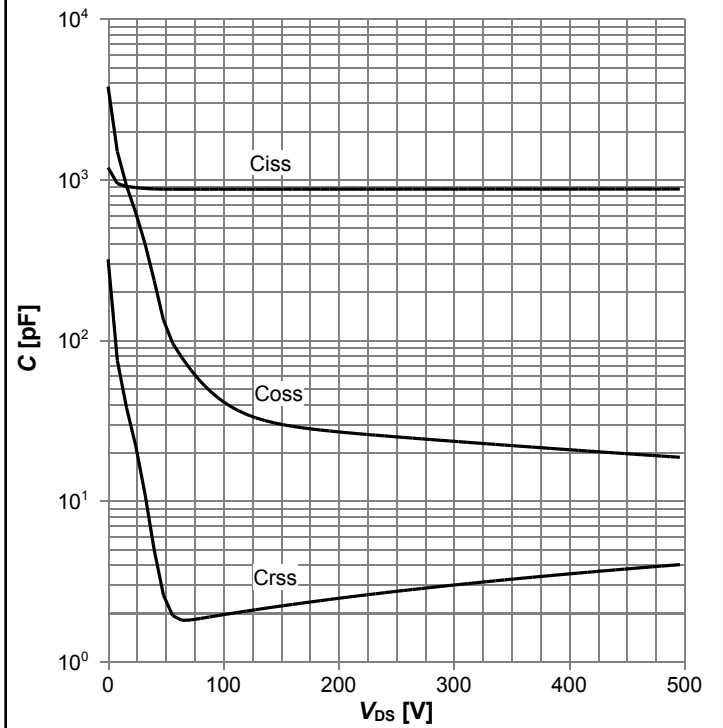
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Diagram 17: Drain-source breakdown voltage



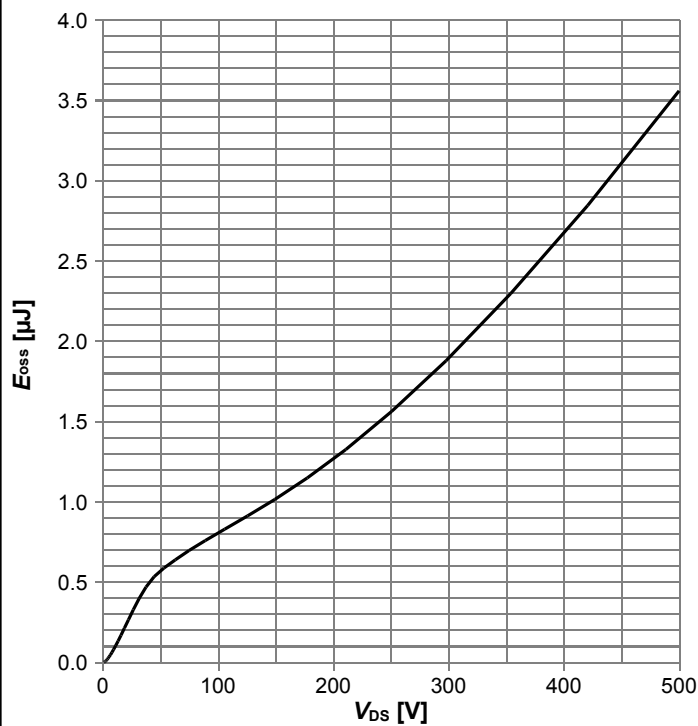
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 18: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 19: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 10 Diode characteristics

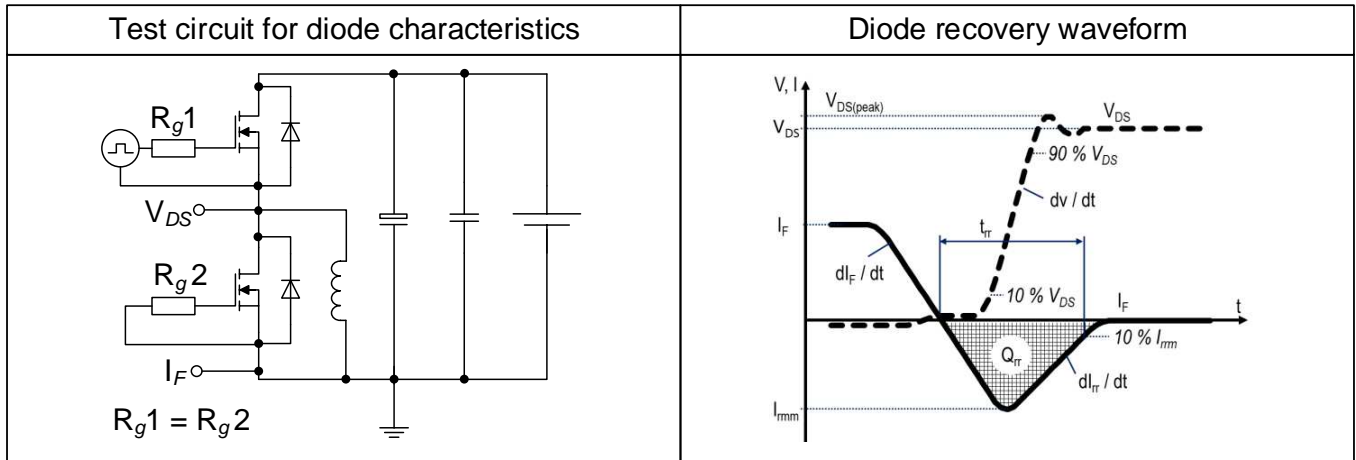


Table 11 Switching times

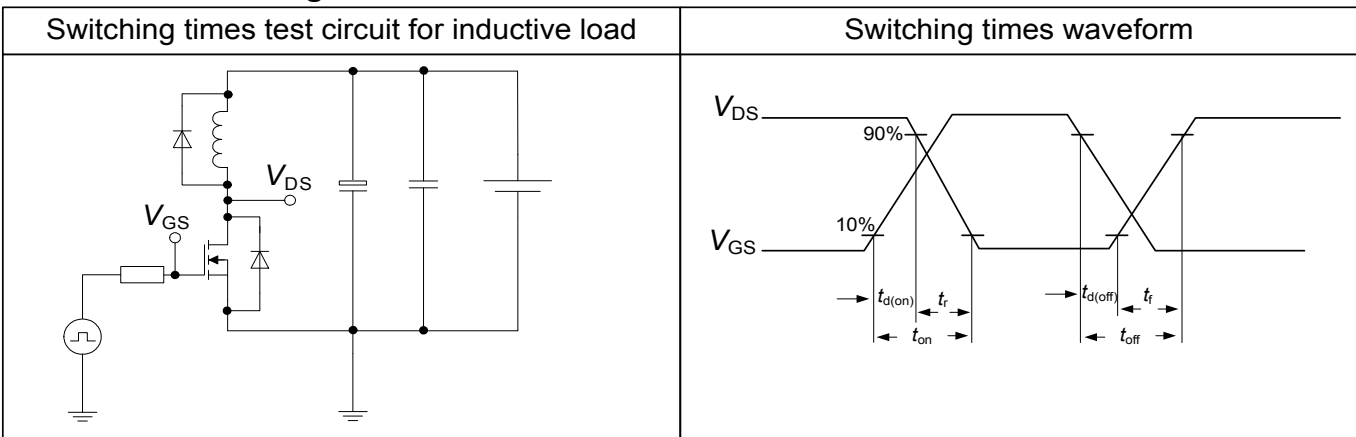
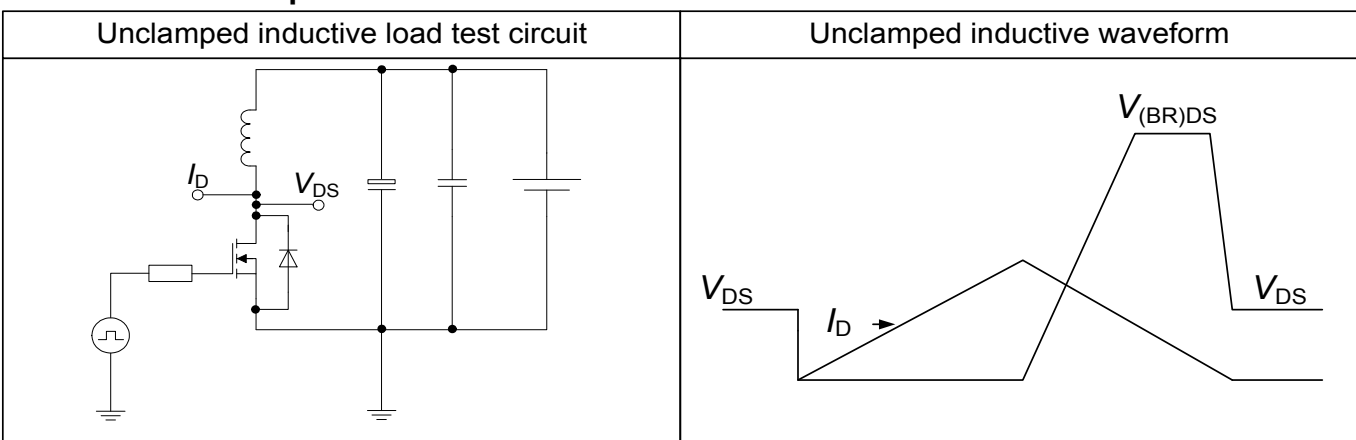


Table 12 Unclamped inductive load



6 Package Outlines

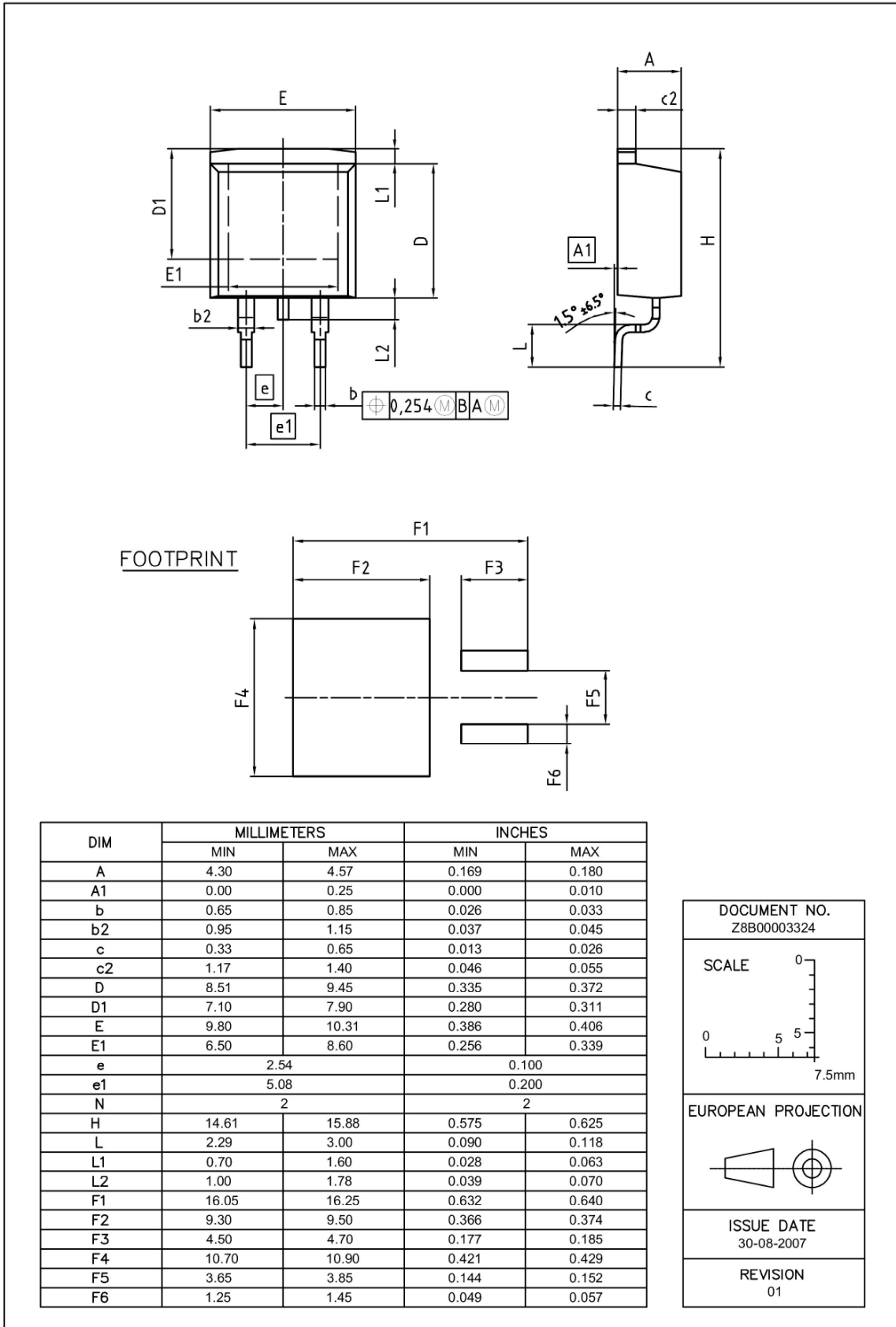


Figure 1 Outline PG-TO263-3, dimensions in mm/inches

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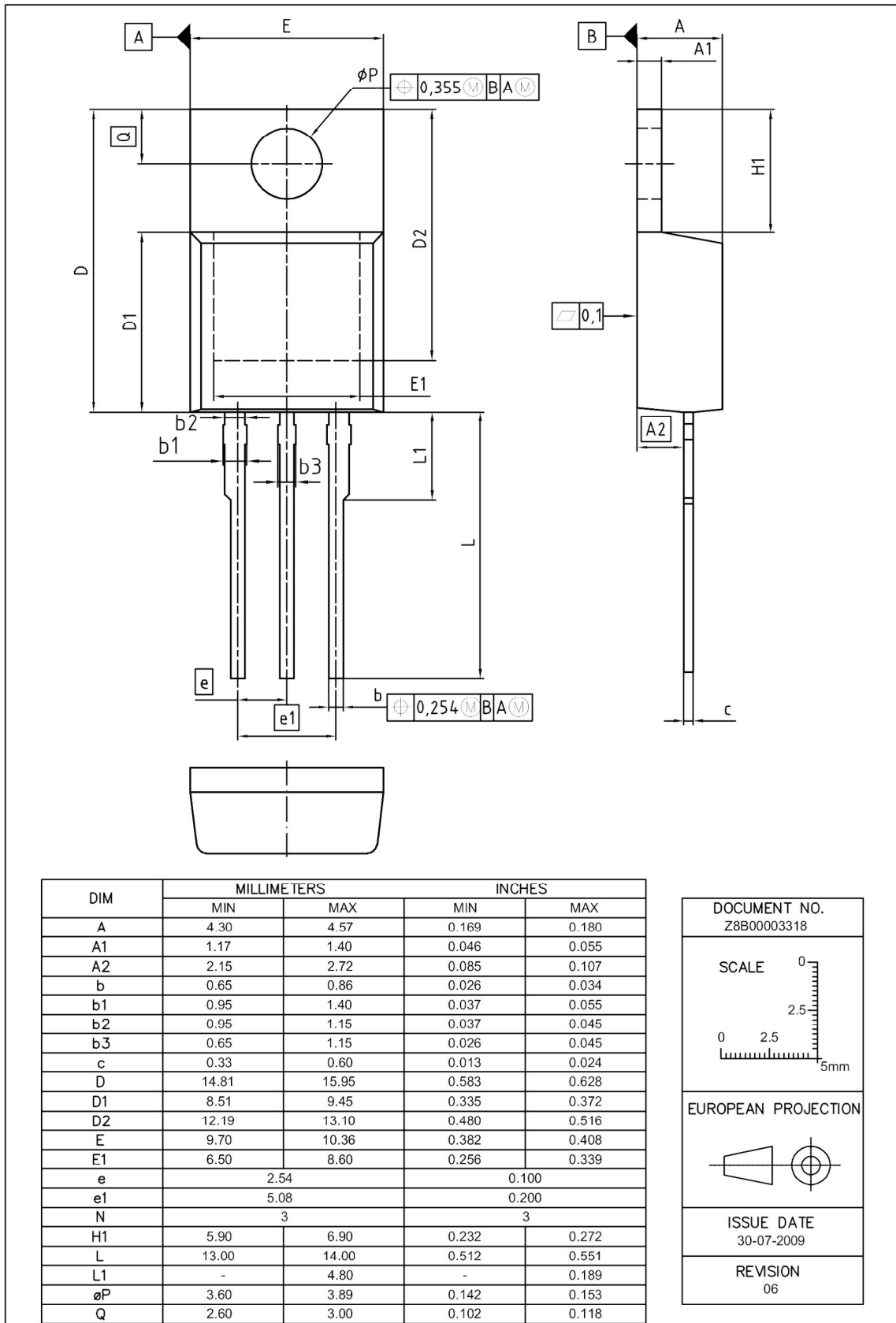
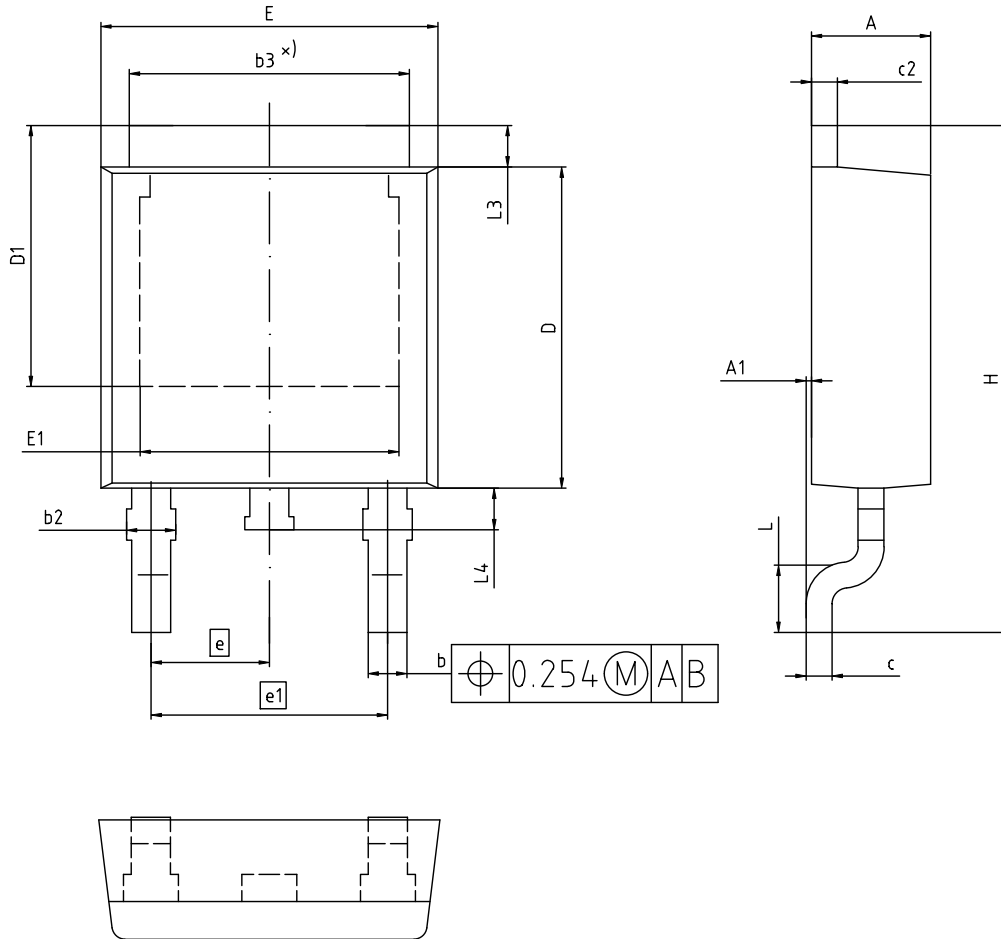


Figure 2 Outline PG-T0220-3, dimensions in mm/inches

PG-TO252-3 (DPAK)



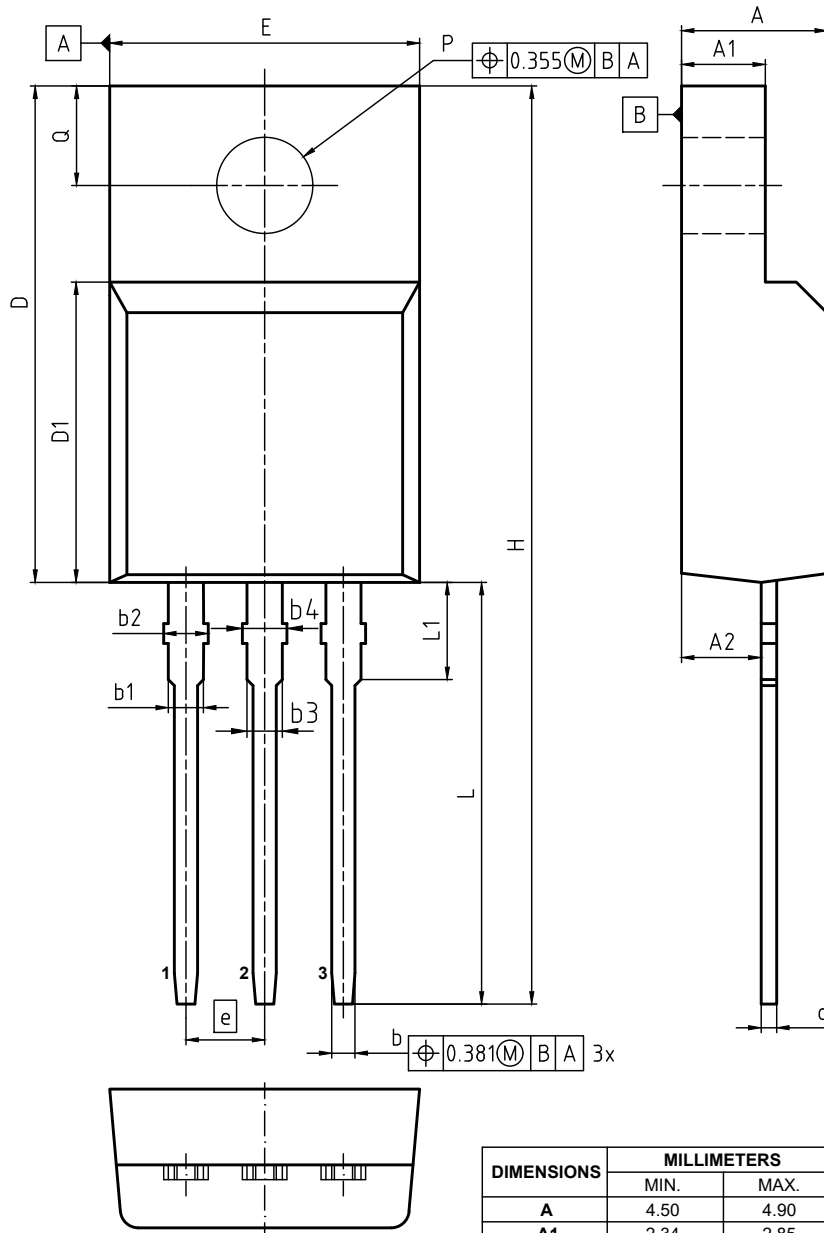
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

DOCUMENT NO. Z8B00003328
REVISION 07
SCALE: 10:1 0 1 2mm
EUROPEAN PROJECTION
ISSUE DATE 01.04.2020

Figure 3 Outline PG-TO252-3, dimensions in mm/inches

600V CoolMOS™ P6 Power Transistor
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NOTES:
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
 GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

DOCUMENT NO. Z8B00003319
REVISION 10
ISSUE DATE 21.03.2019
SCALE 5:1 0 1 2 3 4 5mm
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Figure 4 Outline PG-T0220 FullPAK, dimensions in mm

7 Appendix A

Table 13 Related Links

- IFX CoolMOS™ P6 Webpage: www.infineon.com
- IFX CoolMOS™ P6 application note: www.infineon.com
- IFX CoolMOS™ P6 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

600V CoolMOS™ P6 Power Transistor

IPB60R380P6, IPP60R380P6, IPD60R380P6, IPA60R380P6

Revision History

IPB60R380P6, IPP60R380P6, IPD60R380P6, IPA60R380P6

Revision: 2020-06-09, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-12-05	Release of final version
2.1	2013-12-05	Release of multi-package datasheet
2.2	2015-07-10	PG-TO 263 package added
2.3	2017-08-22	Updated TO220 Full PAK package drawing on page 16
2.4	2020-06-09	Update DPAK, FullPAK package drawing, symbol drawing

Trademarks

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Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.







The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

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