AK4373

Low Power Stereo DAC with HP/SPK-Amp

GENERAL DESCRIPTION

The AK4373 is a low power stereo 24bit DAC with an integrated stereo headphone amplifier and a monaural speaker driver. It can be used for a variety of portable audio and media player applications, including game consoles, dedicated headphone drivers, personal navigation devices, and portable media players. The output drivers can be configured for three unique use cases: mono speaker driver or single-ended ac-coupled headphones which can be used as stereo line-out, DC-coupled BTL headphones and Pseudo Cap-less. The AK4373 operates off of a low-voltage power supply, ranging from 2.2V to 3.6V. The output amplifiers operate at up to 4.0V of the headphone power supply. The device is packaged in a space-saving 32-pin QFN package.

FEATURES

- **Sampling Rate: 8 kHz ~ 48 kHz**
- **8-times Over sampling Digital Filter**
- **SCF with high tolerance to clock jitter**
- **Stereo Headphone Amplifier**
  - **65mW output (Single-ended mode) into 16Ω 3.3V**
  - **SNR: 96dB**
  - **130mW output (Differential mode) into 32Ω 3.3V**
  - **SNR: 96dB**
  - **60mW output (Pseudo cap-less mode) into 16Ω 3.3V**
  - **SNR: 86dB**
  - **Pop-noise free at power-up and reset**
- **Stereo Lineout**
  - **SNR: 96dB**
- **Mono Speaker Driver**
  - **Available for both Dynamic and Piezo Speaker**
  - **0.8W @ 8Ω HVDD = 4.0V**
  - **1.0W @ 4Ω HVDD = 4.0V**
  - **SNR: 97dB**
- **Digital Processing**
  - **HPF, LPF, 3D Enhance, Frequency Compensation, 5-BiQuads,**
  - **Digital ALC/Limiter: +36dB to -54dB, 0.375dB/step**
- **Digital Volume Control: +12dB to -115dB, 0.5dB/step, Mute**
- **Analog Mixing: Mono input**
- **PLL: Input Frequency: 27MHz, 25MHz, 24MHz, 13.5MHz, 12.288MHz, 12MHz, and 11.2896MHz (MCKI pin)**
  - **1fs (LRCK pin)**
  - **32fs or 64fs (BICK pin)**
  - **Input Level: CMOS or AC coupling Input**
- **Master Clock (MCKI pin): 256/512/1024fs**
- **Master Clock Output (MCKO pin): 32fs, 64fs, 128fs, 256fs**
- **µP Interface: 3-Wire serial, I^2C bus (version1.0, 400 KHz Fast-mode)**
- **Audio Interface Format: MSB First, 2's complement**
  - **16/20/24bit MSB justified, 16/20/24bit LSB justified,**
  - **16/20/24bit I^2S, 16/20/24bit DSP Mode**
- **CMOS Input Level**

☐ **Power Supply:**
Analog (AVDD): 2.2 to 3.6V
Digital (DVDD): 1.6 to 3.6V
Driver (HVDD): 2.2 to 4.0V
☐ **Power Consumption:**
11.9mW headphone playback
☐ **Ta = -30 ~ +85°C**
☐ **Package: 32-pin QFN (5mm x 5mm, 0.5mm pitch)**
☐ **Pin/Register compatible with AK4343**

■ Block Diagram

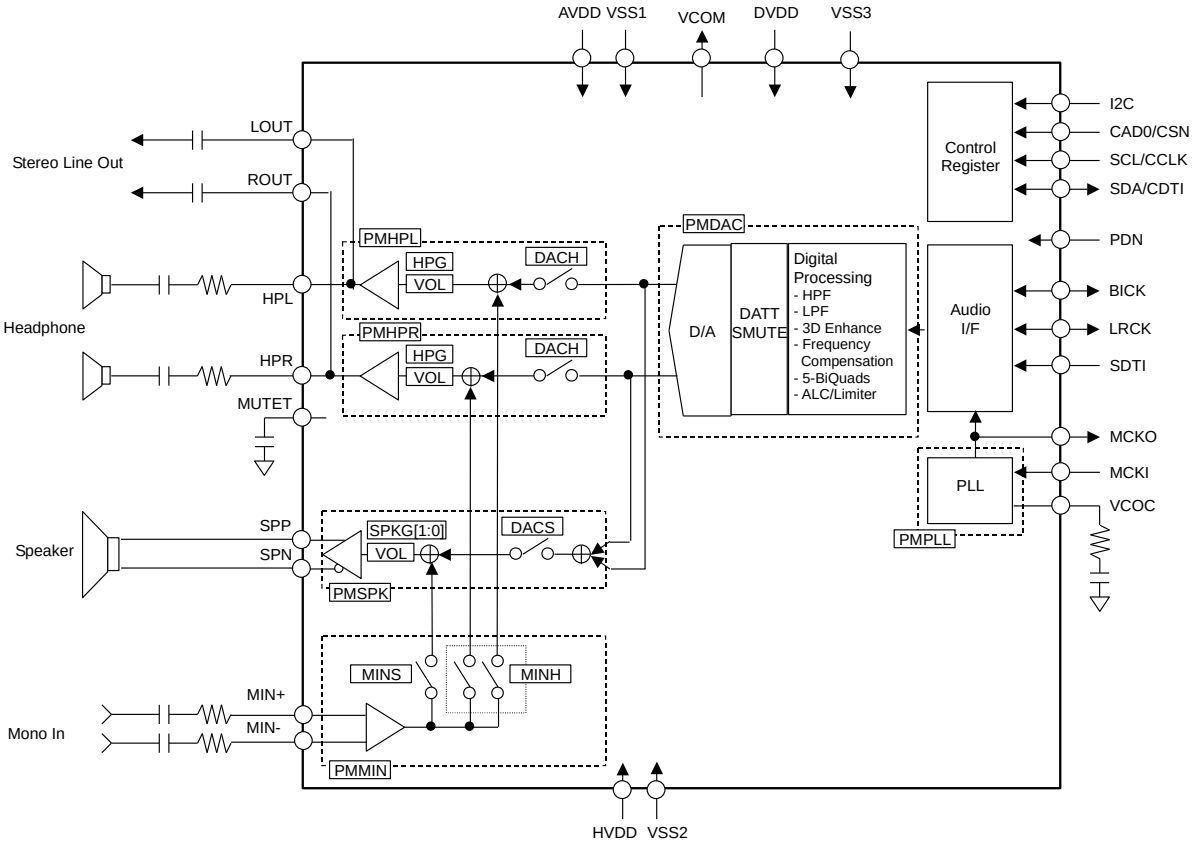


Figure 1. Block Diagram (Single-ended mode, HPBTL bit =PSEUDO bit = “0”)

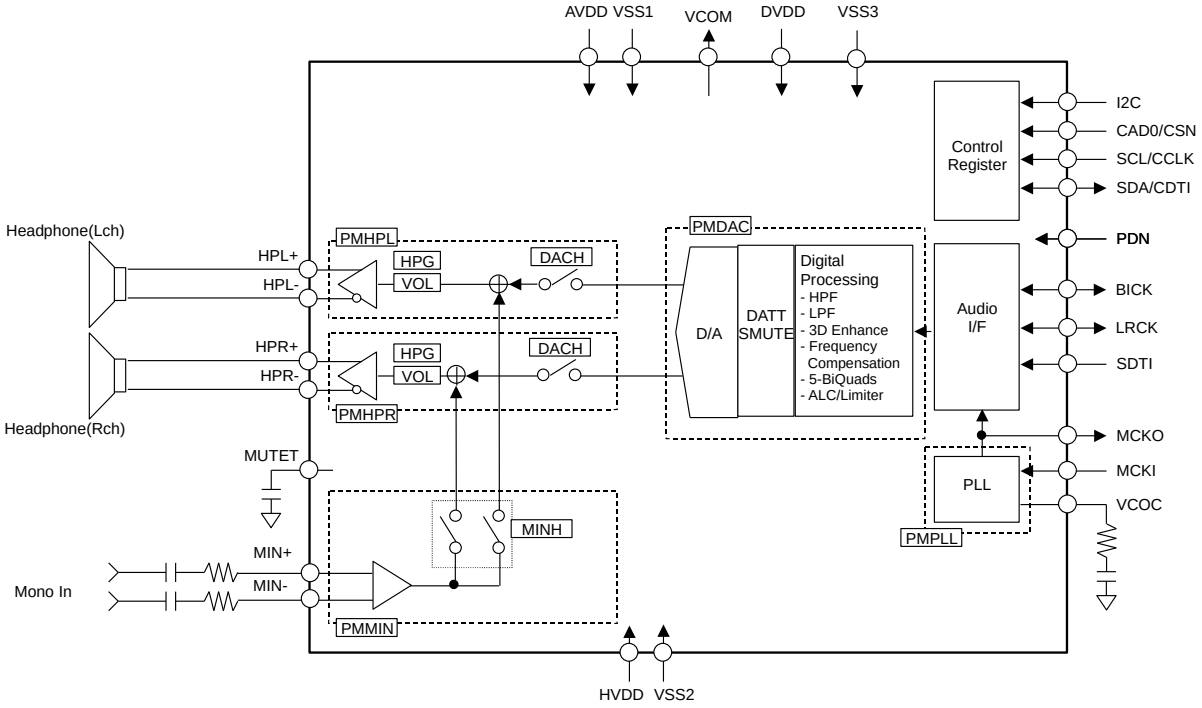


Figure 2. Block Diagram (Differential mode, HPBTL bit = “1”, PSEUDO bit = “0”)

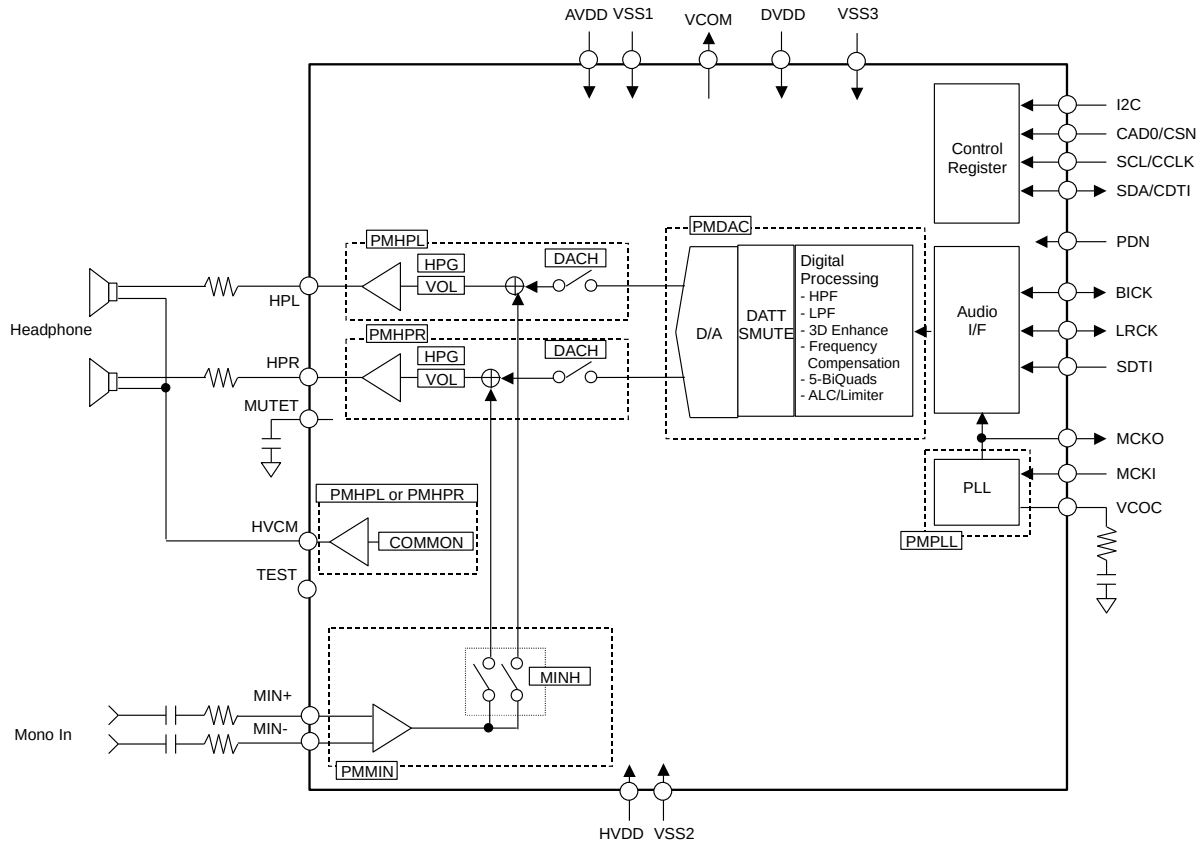
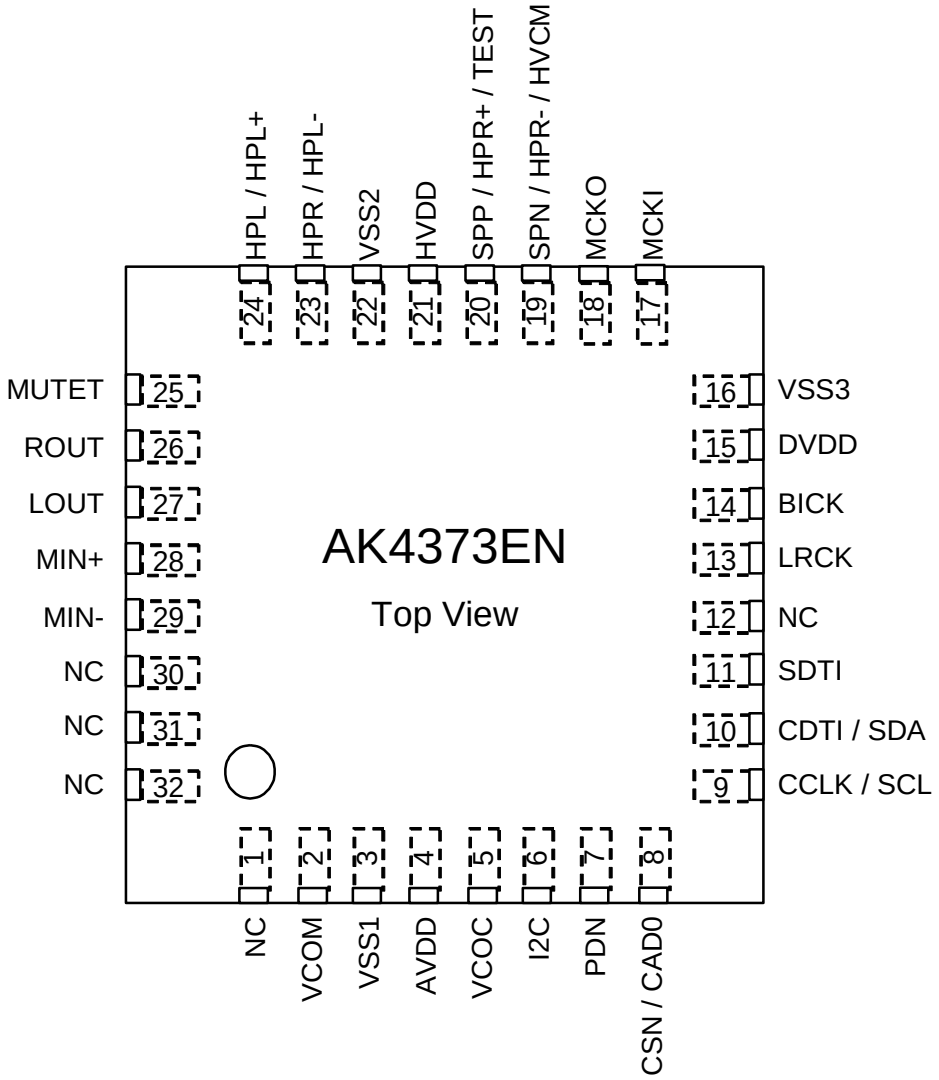


Figure 3. Block Diagram (Pseudo cap-less mode, HPBTL bit = “0”, PSEUDO bit = “1”)

■ Ordering Guide

AK4373EN	–30 ~ +85°C	32pin QFN (0.5mm pitch)
AKD4373	Evaluation board for AK4373	

■ Pin Layout



■ Comparison table between AK4343 and AK4373

1. Function

Function	AK4343	AK4373
DAC Resolution	16bit	24bit
HP-Amp S/N	90dB	96dB(single), 96dB(BTL)
HP-Amp Output Type	Single-ended	Single-ended, Differential or Pseudo cap-less
Five Programmable Biquads	No	Yes
Line Output Pins	Independent from HP/SPK	Shared with HPL/HPR
MCKI Input Level	CMOS	CMOS or 0.4Vpp AC coupling
Analog Mixing	3-Stereo	1-Mono (Single/Differential)
Receiver Amp	Yes	No
SPK AMP	1.2W@8Ω, 5V	1.0W@4Ω, 4.0V

2. Pin

Pin#	AK4343	AK4373
1	TEST1	NC
3	AVSS	VSS1
5	VCOC / RIN3	VCOC
12	TEST2	NC
16	DVSS	VSS3
19	SPN	SPN / HPR– / HVCM
20	SPP	SPP / HPR+ / TEST
22	HVSS	VSS2
23	HPR	HPR / HPL–
24	HPL	HPL / HPL+
28	MIN / LIN3	MIN+
29	RIN2 / IN2–	MIN-
30	LIN2 / IN2+	NC
31	LIN1 / IN1–	NC
32	RIN1 / IN1+	NC

3. Register

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMMIN	PMSPK	~~PMLO~~	PMDAC	0	0
01H	Power Management 2	0	HPMTN	PMHPL	PMHPR	M/S	MCKAC	MCKO	PMPLL
02H	Signal Select 1	SPPSN	MINS	DACS	~~DACL~~	HPBTL	~~PMMP~~	PSEUDO	~~MGAIN0~~
03H	Signal Select 2	~~LOVL~~	~~LOPS~~	~~MGAIN1~~	SPKG1	SPKG0	~~MINL~~	0	0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	DIF2	DIF1	DIF0
05H	Mode Control 2	PS1	PS0	FS3	MSBS	BCKP	FS2	FS1	FS0
06H	Timer Select	DVTM	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
07H	ALC Mode Control 1	0	0	ALC	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
08H	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
09H	Lch Input Volume Control	AVL7	AVL6	AVL5	AVL4	AVL3	AVL2	AVL1	AVL0
0AH	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	0	0	0	FRN	VBAT	0
0CH	Rch Input Volume Control	AVR7	AVR6	AVR5	AVR4	AVR3	AVR2	AVR1	AVR0
0DH	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
0EH	Mode Control 3	0	0	SMUTE	DVOLC	~~BST1~~	~~BST0~~	DEM1	DEM0
0FH	Mode Control 4	0	0	0	0	AVOLC	HPM	MINH	DACH
10H	Power Management 3	~~INR1~~	~~INL1~~	HPG	~~MDIF2~~	~~MDIF1~~	~~INR0~~	~~INL0~~	0
11H	Digital Filter Select 1	GN1	GN0	LPF	HPF	EQ	FIL3	0	0
12H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
13H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
14H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
15H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
16H	EQ Co-efficient 0	EQA7	EQA6	EQA5	EQA4	EQA3	EQA2	EQA1	EQA0
17H	EQ Co-efficient 1	EQA15	EQA14	EQA13	EQA12	EQA11	EQA10	EQA9	EQA8
18H	EQ Co-efficient 2	EQB7	EQB6	EQB5	EQB4	EQB3	EQB2	EQB1	EQB0
19H	EQ Co-efficient 3	0	0	EQB13	EQB12	EQB11	EQB10	EQB9	EQB8
1AH	EQ Co-efficient 4	EQC7	EQC6	EQC5	EQC4	EQC3	EQC2	EQC1	EQC0
1BH	EQ Co-efficient 5	EQC15	EQC14	EQC13	EQC12	EQC11	EQC10	EQC9	EQC8
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	~~F1AS~~	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
20H	Reserved	0	0	~~PMAINR3~~	~~PMAINL3~~	~~PMAINR2~~	~~PMAINL2~~	~~PMMICR~~	~~PMMICL~~
21H	Reserved	0	0	~~MICR3~~	~~MICL3~~	0	0	~~AIN3~~	~~RCV~~
22H	Reserved	0	0	0	0	~~RINR3~~	~~LINL3~~	~~RINR2~~	~~LINL2~~
23H	Reserved	0	0	0	0	~~RINH3~~	~~LINH3~~	~~RINH2~~	~~LINH2~~
24H	Reserved	0	0	0	0	~~RINS3~~	~~LINS3~~	~~RINS2~~	~~LINS2~~
25H	Reserved	0	0	0	0	0	0	0	0
26H	Reserved	0	0	0	0	0	0	0	0
27H	Reserved	0	0	0	0	0	0	0	0
28H	Reserved	0	0	0	0	0	0	0	0
29H	Reserved	0	0	0	0	0	0	0	0
2AH	Reserved	0	0	0	0	0	0	0	0
2BH	Reserved	0	0	0	0	0	0	0	0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

These bits were added to the AK4373.
These bits were removed from the AK4343.
These bits name were changed.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

These bits were added to the AK4373.
These bits were removed from the AK4343.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.
2	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of DAC outputs.
3	VSS1	-	Analog Ground Pin
4	AVDD	-	Analog Power Supply Pin 2.2 ~ 3.6V
5	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin must be connected to VSS1 with one resistor and capacitor in series.
6	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
7	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initialization of the control register. The AK4373 must be reset once upon power-up.
8	CSN	I	Chip Select Pin (I2C pin = "L": 3-wire Serial Mode)
	CAD0	I	Chip Address 1 Select Pin (I2C pin = "H": I^2C Bus Mode)
9	CCLK	I	Control Data Clock Pin (I2C pin = "L": 3-wire Serial Mode)
	SCL	I	Control Data Clock Pin (I2C pin = "H": I^2C Bus Mode)
10	CDTI	I	Control Data Input Pin (I2C pin = "L": 3-wire Serial Mode)
	SDA	I/O	Control Data Input Pin (I2C pin = "H": I^2C Bus Mode)
11	SDTI	I	Audio Serial Data Input Pin
12	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.
13	LRCK	I/O	Input / Output Channel Clock Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	DVDD	-	Digital Power Supply Pin. 1.6 ~ 3.6V
16	VSS3	-	Digital Ground Pin
17	MCKI	I	External Master Clock Input Pin
18	MCKO	O	Master Clock Output Pin

No.	Pin Name	I/O	Function
19	SPN	O	Speaker Amp Negative Output Pin Single-ended mode (HPBTL bit = PSEUDO bit = “0”)
	HPR–	O	Rch Headphone-Amp Negative Output Pin Differential mode (HPBTL bit = “1”, PSEUDO bit = “0”)
	HVCM	O	Common Output Voltage for Headphone-Amp Pin Pseudo cap-less mode (HPBTL bit = “0”, PSEUDO bit = “1”)
20	SPP	O	Speaker Amp Positive Output Pin Single-ended mode (HPBTL bit = PSEUDO bit = “0”)
	HPR+	O	Rch Headphone-Amp Positive Output Pin Differential mode (HPBTL bit = “1”, PSEUDO bit = “0”)
	TEST	O	This pin must be open. Pseudo cap-less mode (HPBTL bit = “0”, PSEUDO bit = “1”)
21	HVDD	-	Headphone & Speaker Amp Power Supply Pin. 2.2 ~ 4.0V
22	VSS2	-	Headphone & Speaker Amp Ground Pin
23	HPR	O	Rch Headphone-Amp Output Pin Single-ended mode (HPBTL bit = PSEUDO bit = “0”) Pseudo cap-less mode (HPBTL bit = “0”, PSEUDO bit = “1”)
	HPL–	O	Lch Headphone-Amp Negative Output Pin Differential mode (HPBTL bit = “1”, PSEUDO bit = “0”)
24	HPL	O	Lch Headphone-Amp Output Pin Single-ended mode (HPBTL bit = PSEUDO bit = “0”) Pseudo cap-less mode (HPBTL bit = “0”, PSEUDO bit = “1”)
	HPL+	O	Lch Headphone-Amp Positive Output Pin Differential mode (HPBTL bit = “1”, PSEUDO bit = “0”)
25	MUTET	O	Mute Time Constant Control Pin Connected to the VSS2 pin with a capacitor for mute time constant.
26	ROUT	O	Rch Line Output Pin This pin is internal connected to the HPR pin.
27	LOUT	O	Lch Line Output Pin This pin is internal connected to the HPL pin.
28	MIN+	I	Mono Signal Positive Input (Differential Input) or Mono Signal Input (Single-ended Input)
29	MIN-	I	Mono Signal Negative Input (Differential Input) If the MIN+ pin is used as single-ended, this pin should be connected to the VSS1 with a capacitor.
30	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.
31	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.
32	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.

Note 1. All input pins must not be left floating.
Note 2. DVDD or VSS3 voltage must be input to I2C pin.
Note 3. All analog input pins (MIN+/- pins) must be supplied signal via AC-coupling capacitor.
Note 4. Analog output pins (HPL, HPR, LOUT, and ROUT pins) must deliver signal via AC-coupling capacitor except speaker output (SPP, SPN pins) and headphone output in Differential mode (HPL+/- and HPR+/- pins) and headphone output in Pseudo cap-less mode (HPL and HPR pins).

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	VCOC, SPN/HPR–/HVCM, SPP/HPR+/TEST, HPR/HPL-, HPL/HPL+, MIN+, MIN-, MUTET	These pins must be open.
Digital	MCKO	This pin must be open.
	MCKI	This pin must be connected to VSS3.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; Note 5)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	Headphone-Amp / Speaker-Amp	HVDD	–0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 7)		VINA	–0.3	(AVDD+0.3) or 4.6	V
Digital Input Voltage (Note 8)		VIND	–0.3	(DVDD+0.3) or 4.6	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation	(Note 9)	Pd	-	511	mW

Note 5. All voltages are with respect to ground.
Note 6. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.
Note 7. I2C, MIN+, MIN- pin
Note 8. PDN, CSN/CAD0, CCLK/SCL, CDTI/SDA, SDTI, LRCK, BICK, MCKI pins
Pull-up resistors at SDA and SCL pins must be connected to (DVDD+0.3)V or less voltage.
Note 9. In case that the exposed pad is connected to the ground and PCB drawing density is 100%.This power is the AK4373 internal dissipation that does not include power of externally connected speaker and headphone.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V; Note 5)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 10)	Analog	AVDD	2.2	3.3	3.6	V
	Digital	DVDD	1.6	3.3	3.6	V
	HP / SPK-Amp	HVDD	2.2	3.3	4.0	V
	Difference1	DVDD – AVDD	-	-	+0.3	V
	Difference2	DVDD – HVDD	-	-	+0.3	V
	Difference3	AVDD – HVDD	-	-	+0.6	V

Note 5. All voltages are with respect to ground.
Note 10. The power-up sequence between AVDD, DVDD and HVDD is not critical. When only AVDD or HVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. DVDD must not be powered OFF while AVDD or HVDD is powered ON.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=HVDD=3.3V; VSS1=VSS2=VSS3=0V; fs=44.1kHz, BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
DAC Characteristics:					
Resolution		-	-	24	Bits
Stereo Line Output Characteristics: DAC → LOUT/ROUT pins, Single-ended mode (Figure 4), HPBTL bit = "0", PSEUDO bit = "0", HPG bit = "0", HVDD=3.3V, C=1µF, R_L=10kΩ, ALC=OFF, AVOL=0dB, DVOL=0dB; unless otherwise specified.					
Output Voltage (0dBFS) (Note 11)		1.78	1.98	2.18	Vpp
S/(N+D) (0dBFS)		-	77	-	dB
S/N (A-weighted)		86	96	-	dB
Interchannel Isolation		60	80	-	dB
Load Resistance	RL	10	-	-	kΩ
Load Capacitance	C1	-	-	30	pF

Note 11. Output voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ).

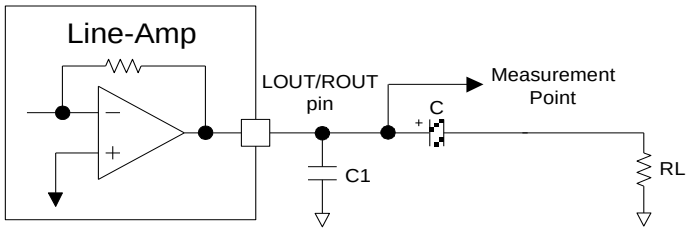


Figure 4. Line-Amp output circuit

Parameter		min	typ	max	Unit
Headphone-Amp Characteristics: DAC → HPL/HPR pins, Single-ended mode (Figure 5), HPBTL bit = "0", PSEUDO bit = "0", HPG bit = "0", HVDD=3.3V, C=47µF, R_L=22.8Ω, ALC=OFF, AVOL=0dB, DVOL=0dB; unless otherwise specified.					
Output Voltage (Note 12)	0dBFS	1.58	1.98	2.38	Vpp
	0dBFS (Note 13)	-	3.00	-	Vpp
	0dBFS (Note 14)	-	1.02	-	Vrms
S/(N+D)	–3dBFS	50	60	-	dB
	–3dBFS (Note 13)	-	65	-	dB
	0dBFS (Note 14)	-	20	-	dB
S/N (A-weighted)		86	96	-	dB
	(Note 13)	-	96	-	dB
Interchannel Isolation		60	75	-	dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance	R_L=R1+R2	16	-	-	Ω
Load Capacitance	C1	-	-	30	pF
	C2	-	-	300	pF

Note 12. Output voltage is proportional to AVDD voltage.
Vout = 0.6 x AVDD(typ)@HPG bit = "0", 0.91 x AVDD(typ)@HPG bit = "1".
Note 13. HPG bit = "1", HVDD=3.8V, C=47µF, R_L=100Ω.
Note 14. HPG bit = "1", HVDD=3.3V, C=47µF, R_L=16Ω.

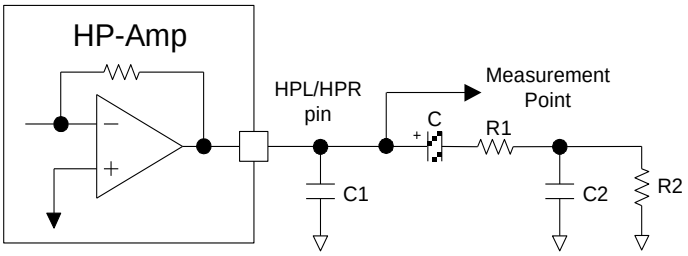


Figure 5. HP-Amp Output Circuit in single-ended mode

Parameter		min	typ	max	Unit
Headphone-Amp Characteristics: DAC → HPL+/-, HPR+/- pins, Differential mode(Figure 6), HPBTL bit = "1", PSEUDO bit = "0" , HPG bit = "0", HVDD=3.3V, R_L=32Ω, ALC=OFF, AVOL=0dB, DVOL=0dB; unless otherwise specified.					
Output Voltage (Note 15)	0dBFS	-	3.96	-	Vpp
	0dBFS (Note 16)	-	2.05	-	Vrms
S/(N+D)	–3dBFS	-	60	-	dB
	0dBFS (Note 16)	-	20	-	dB
S/N (A-weighted)		-	96	-	dB
Interchannel Isolation		-	75	-	dB
Interchannel Gain Mismatch		-	0.2	-	dB
Load Resistance	R_L =2 x R1 + R2	16	-	-	Ω
Load Capacitance	C1	-	-	30	pF
	C2	-	-	300	pF

Note 15. Output voltage is proportional to AVDD voltage.
Vout = 1.2 x AVDD(typ)@HPG bit = "0", 1.82 x AVDD(typ)@HPG bit = "1".
Note 16. HPG bit = "1", HVDD=3.3V, R_L=32Ω.

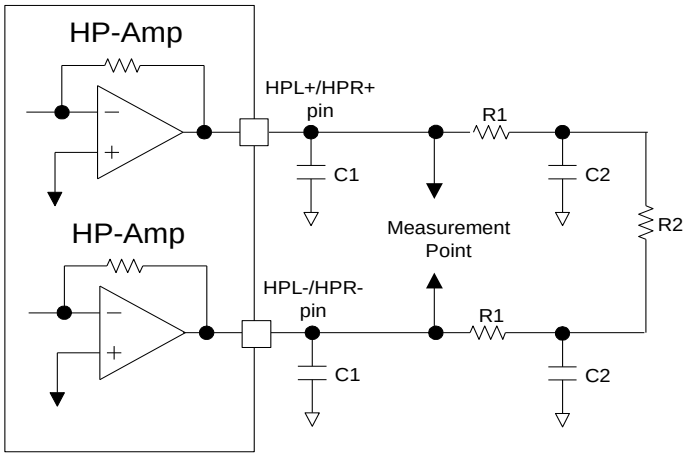
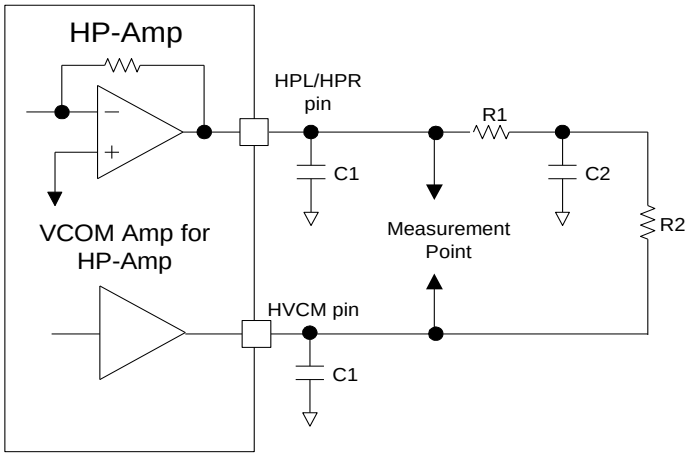


Figure 6. HP-Amp Output Circuit in differential mode

Parameter		min	typ	max	Unit
Headphone-Amp Characteristics: DAC → HPL/HPR pins, Pseudo cap-less mode(Figure 7), HPBTL bit = "0", PSEUDO bit = "1" , HPG bit = "0", HVDD=3.3V, R_L=22.8Ω, ALC=OFF, AVOL=0dB, DVOL=0dB; unless otherwise specified.					
Output Voltage (Note 17)	0dBFS	-	1.98	-	Vpp
	0dBFS (Note 18)	-	0.98	-	Vrms
S/(N+D)	–3dBFS	-	38	-	dB
	0dBFS (Note 18)	-	20	-	dB
S/N (A-weighted)		-	86	-	dB
Interchannel Isolation		-	38	-	dB
Interchannel Gain Mismatch		-	0	-	dB
Load Resistance	R_L = R1 + R2	16	-	-	Ω
Load Capacitance	C1	-	-	30	pF
	C2	-	-	300	pF

Note 17. Output voltage is proportional to AVDD voltage.
Vout = 0.6 x AVDD(typ)@HPG bit = "0", 0.91 x AVDD(typ)@HPG bit = "1".
Note 18. HPG bit = "1", HVDD=3.3V, R_L=16Ω.



Note: Impedance between headphone and the HVCM pin must be as low as possible. If the impedance is larger, crosstalk and distortion might be degraded.

Figure 7. HP-Amp Output Circuit in pseudo cap-less mode

Parameter			min	typ	max	Unit
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, AVOL=0dB, DVOL=0dB, R_L=8Ω, BTL, HVDD=3.3V; unless otherwise specified.						
Output Voltage (Note 19)						
	SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	3.11	-	Vpp
	SPKG1-0 bits = "01", –0.5dBFS (Po=240mW)		3.13	3.92	4.71	Vpp
	SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			2.04		Vrms
S/(N+D)						
	SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	50	-	dB
	SPKG1-0 bits = "01", –0.5dBFS (Po=240mW)		20	50	-	dB
	SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			20		dB
S/N (A-weighted)			87	97	-	dB
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	30	pF
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, AVOL=0dB, DVOL=0dB, C_L=3μF, R_{series}=20Ω x 2, BTL, HVDD=3.8V; unless otherwise specified. (Figure 53)						
Output Voltage (Note 19)	SPKG1-0 bits = "10", -0.5dBFS		–	6.37	–	Vpp
S/(N+D) (Note 20)	SPKG1-0 bits = "10", -0.5dBFS		–	58	-	dB
S/N (A-weighted)				97	-	dB
Load Resistance (Note 21)			50	-	-	Ω
Load Capacitance (Note 21)			-	-	3	μF
Mono Input: MIN+ pin (External Input Resistance=20kΩ) Single-ended Input MIN- pin is connected to VSS1 via input capacitor.						
Maximum Input Voltage (Note 22)			-	1.98	-	Vpp
Gain (Note 23)						
	MIN+ → HPL/HPR	HPBTL bit = "0" HPG bit = "0"	-	0	-	dB
	MIN+ → HPL/HPR	HPBTL bit = "0" HPG bit = "1"	-	+3.6	-	dB
	MIN+ → HPL+/-, HPR+/-	HPBTL bit = "1" HPG bit = "0"	-	+6	-	dB
	MIN+ → HPL+/-, HPR+/-	HPBTL bit = "1" HPG bit = "1"	-	+9.6	-	dB
	MIN → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	-0.07	+4.43	+8.93	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+6.43	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+10.65	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+6.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+8.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+14.65	-	dB

Mono Input: MIN+/MIN- pins (External Input Resistance=20kΩ) Differential Input						
Maximum Input Voltage (Note 24)			-	1.98	-	Vpp
Gain (Note 23)						
	MIN+/- → HPL/HPR	HPBTL bit = "0" HPG bit = "0"	-	0	-	dB
	MIN+/- → HPL/HPR	HPBTL bit = "0" HPG bit = "1"	-	+3.6	-	dB
	MIN+/- → HPL+/-, HPR+/-	HPBTL bit = "1" HPG bit = "0"	-	+6	-	dB
	MIN+/- → HPL+/-, HPR+/-	HPBTL bit = "1" HPG bit = "1"	-	+9.6	-	dB
	MIN+/MIN- → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	-0.07	+4.43	+8.93	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+6.43	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+10.65	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+6.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+8.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+14.65	-	dB

Note 19. Output voltage is proportional to AVDD voltage.
Vout = 1.00 x AVDD(typ)@SPKG1-0 bits = "00", 1.25 x AVDD(typ)@SPKG1-0 bits = "01", 2.04 x AVDD(typ)@SPKG1-0 bits = "10", 2.57 x AVDD(typ)@SPKG1-0 bits = "11" at Differential output.

Note 20. In case of measuring at SPP and SPN pins.

Note 21. Load impedance is total impedance of series resistance (R_{series}) and piezo speaker impedance at 1kHz in Figure 56. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 20Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Note 22. Maximum voltage is in proportion to both AVDD and external input resistance (Rin).
Vin = 0.6 x AVDD x 20kΩ (typ)/Rin.

Note 23. The gain is in inverse proportional to external resistance.

Note 24. The Maximum voltage is in proportion to both AVDD and external input resistance (Rin).
Vin = (MIN+) – (MIN-) = 0.6 x AVDD x 20kΩ (typ)/Rin.
The signals with same amplitude and inverted phase should be input to MIN+ and MIN- pins, respectively.

Parameter		min	typ	max	Unit
Power Supplies:					
Power-Up (PDN pin = "H")					
All Circuit Power-up:					
	AVDD+DVDD (Note 25)	-	7.8	-	mA
	AVDD+DVDD (Note 26)	-	8.1	12	mA
	HVDD: HP-Amp Normal Operation No Output (Note 27)	-	2.2	4	mA
	HVDD: SPK-Amp Normal Operation No Output (Note 28)	-	4.1	12	mA
Power-Down (PDN pin = "L") (Note 29)					
	AVDD+DVDD+HVDD	-	1	20	μA

Note 25. PLL Master Mode (MCKI=12.288MHz) and PMDAC = PMHPL = PMHPR = PMVCM = PMPLL = MCKO = M/S bits = "1", PMMIN bit = "0".
AVDD=3.9mA(typ), DVDD=3.9mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=3.1mA(typ), DVDD=2.7mA(typ).

Note 26. PLL Master Mode (MCKI=12.288MHz) and PMDAC = PMHPL = PMHPR = PMVCM = PMPLL = MCKO = M/S bits = "1", PMMIN bit = "1".
AVDD=4.2mA(typ), DVDD=3.9mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=3.5mA(typ), DVDD=2.7mA(typ).

Note 27. PMDAC = PMHPL = PMHPR = PMVCM = PMPLL = PMMIN bits = "1" and PMSPK bit = "0".

Note 28. PMDAC = PMSPK = PMVCM = PMPLL = PMMIN bits = "1" and PMHPL = PMHPR bits = "0".

Note 29. All digital input pins are fixed to DVDD or VSS3.

■ Power Consumption for each operation mode

Common Conditions: Ta=25°C; VSS1=VSS2=VSS3=0V; fs=44.1kHz, External Slave Mode, BICK=64fs; 1kHz, 0dBFS input; (PMMIN bit = "0")Headphone & Speaker = No output

Mode	Power Management Bit						Typical Current						
	00H				01H		AVDD		DVDD		HVDD		Total Power
	PMVCM	PMMIN	PMSPK	PMDAC	PMHPL	PMHPR	[V]	[mA]	[V]	[mA]	[V]	[mA]	[mW]
All Power-down	0	0	0	0	0	0	3.3	0	3.3	0	3.3	0	0
DAC → HP/Line Out	1	0	0	1	1	1	2.2	2.7	1.8	1.0	2.2	1.9	11.9
											4.0	2.6	18.1
							3.3	3.1	3.3	2.7	3.3	2.2	26.4
DAC → SPK	1	0	1	1	0	0	2.2	2.7	1.8	1.0	2.2	4.2	17.0
											4.0	5.2	28.5
							3.3	3.2	3.3	2.7	3.3	4.1	33.0

Table 1. Power Consumption for each operation mode (typ)

FILTER CHARACTERISTICS

(Ta=-30 ~ 85°C; AVDD=2.2 ~ 3.6V, DVDD=1.6 ~ 3.6V; HVDD=2.2 ~ 4.0V; fs=44.1kHz; DEM=OFF; HPF=LPF=FIL3=EQ=5-BiQuads=ALC=OFF)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF):						
Passband (Note 30)	-0.05dB –6.0dB	PB	0 -	- 22.05	20.0 -	kHz kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 31)		GD	-	25	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 30. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.454*fs (@–0.05dB). Each response refers to that of 1kHz.

Note 31. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data of both channels from the input register to the output of analog signal. HPF=LPF=FIL3=EQ=5-BiQuads=ALC=OFF.

DC CHARACTERISTICS

(Ta=-30 ~ 85°C; AVDD=2.2 ~ 3.6V, DVDD=1.6 ~ 3.6V; HVDD=2.2 ~ 4.0V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	2.2V≤DVDD≤3.6V	VIH	70%DVDD	-	-	V
	1.6V≤DVDD<2.2V	VIH	80%DVDD	-	-	V
Low-Level Input Voltage	2.2V≤DVDD≤3.6V	VIL	-	-	30%DVDD	V
	1.6V≤DVDD<2.2V	VIL	-	-	20%DVDD	V
Input Voltage at AC Coupling (Note 32)		VAC	0.4	-	-	Vpp
High-Level Output Voltage (Iout = –200μA)		VOH	DVDD–0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin: Iout = 200μA)		VOL	-	-	0.2	V
(SDA pin, 2.0V≤DVDD≤3.6V: Iout = 3mA)		VOL	-	-	0.4	V
(SDA pin, 1.6V≤DVDD<2.0V: Iout = 3mA)		VOL	-	-	20%DVDD	V
Input Leakage Current		Iin	-	-	±10	μA

Note 32. MCKI is connected to a capacitor. (Figure 8)

SWITCHING CHARACTERISTICS

(Ta=-30 ~ 85°C; AVDD=2.2 ~ 3.6V, DVDD=1.6 ~ 3.6V; HVDD=2.2 ~ 4.0V;C_L=20pF; unless otherwise specified)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width		tACW	18.5	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK–60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter		Symbol	min	typ	max	Unit
PLL Slave Mode (PLL Reference Clock = LRCK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK–60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK–60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period	PLL3-0 bits = “0010”	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = “0011”	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing						
Frequency	256fs	fs	7.35	-	48	kHz
	512fs	fs	7.35	-	26	kHz
	1024fs	fs	7.35	-	13	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK–60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	312.5	-	-	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = “0”	tBCK	-	1/(32fs)	-	ns
	BCKO bit = “1”	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (DSP Mode)					
Master Mode					
LRCK "↑" to BICK "↑" (Note 33)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
LRCK "↑" to BICK "↓" (Note 34)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK "↑" to BICK "↑" (Note 33)	tLRB	0.4 x tBCK	-	-	ns
LRCK "↑" to BICK "↓" (Note 34)	tLRB	0.4 x tBCK	-	-	ns
BICK "↑" to LRCK "↑" (Note 33)	tBLR	0.4 x tBCK	-	-	ns
BICK "↓" to LRCK "↑" (Note 34)	tBLR	0.4 x tBCK	-	-	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Audio Interface Timing (Right/Left justified & I^2S)					
Master Mode					
BICK "↓" to LRCK Edge (Note 35)	tMBLR	–40	-	40	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 35)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	50	-	-	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Note 33. MSBS, BCKP bits = "00" or "11".
Note 34. MSBS, BCKP bits = "01" or "10".
Note 35. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 37)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 37)	tCSH	50	-	-	ns
Control Interface Timing (I^2C Bus mode): (Note 36)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 38)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 39)	tPD	150	-	-	ns

Note 36. I^2C-bus is a trademark of NXP B.V.
Note 37. CCLK rising edge must not occur at the same time as CSN edge.
Note 38. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 39. The AK4373 can be reset by the PDN pin = "L".

■ Timing Diagram

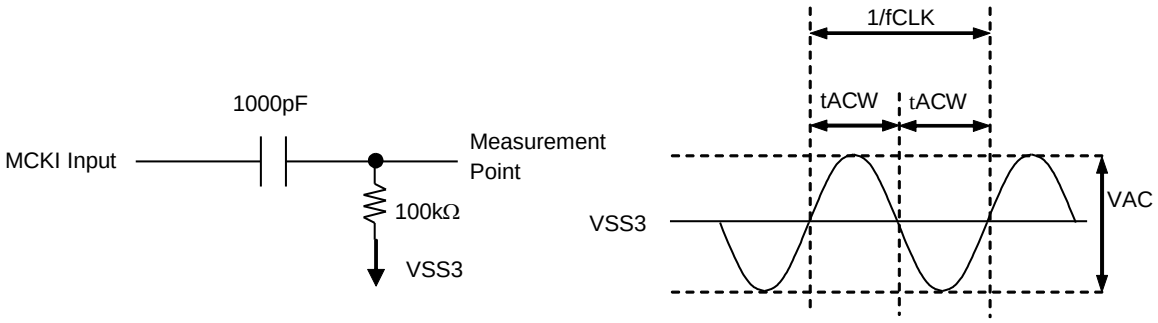


Figure 8. MCKI AC Coupling Timing

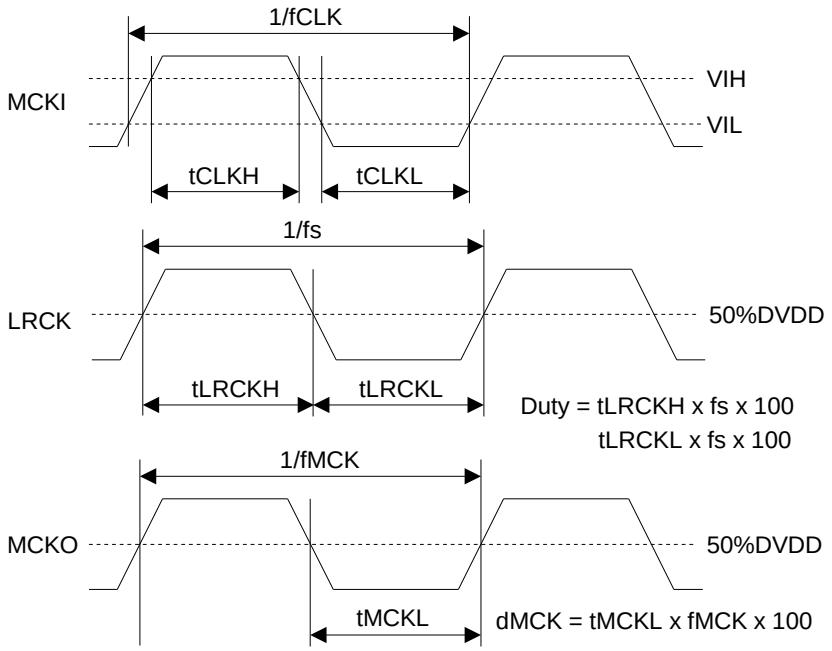


Figure 9. Clock Timing (PLL/EXT Master mode)

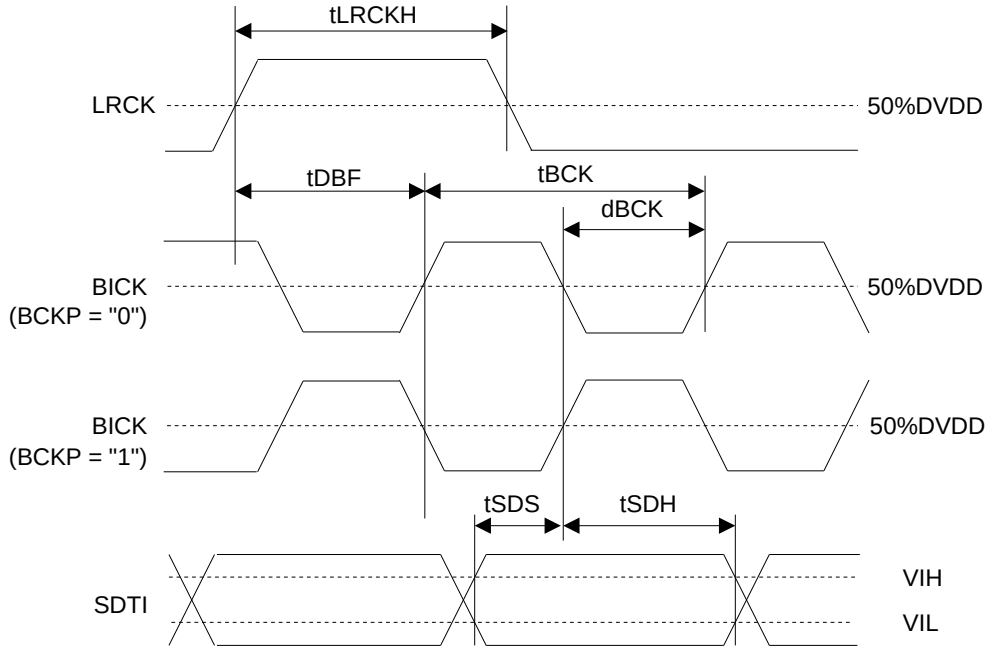


Figure 10. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = “0”)

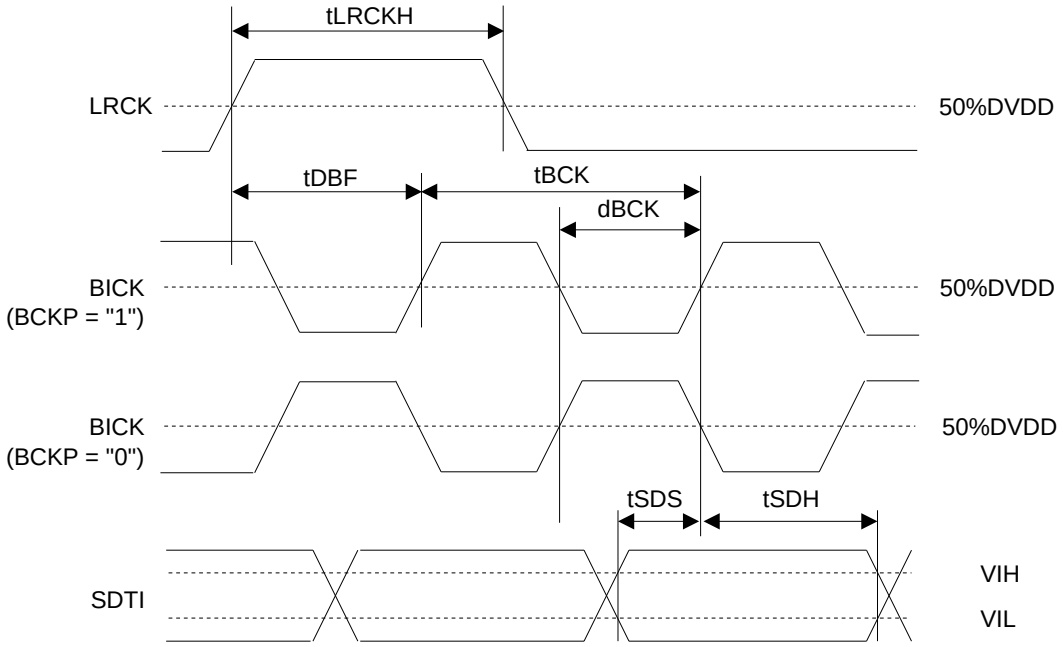


Figure 11. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = "1")

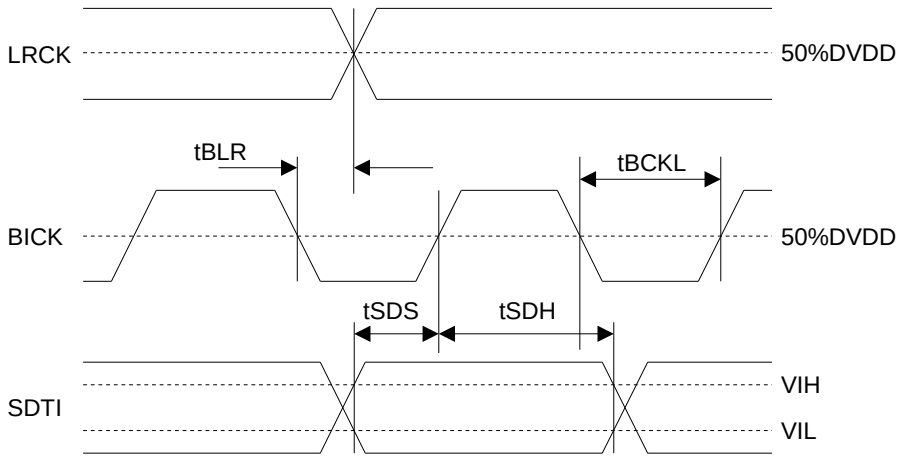


Figure 12. Audio Interface Timing (PLL/EXT Master mode, Except DSP mode)

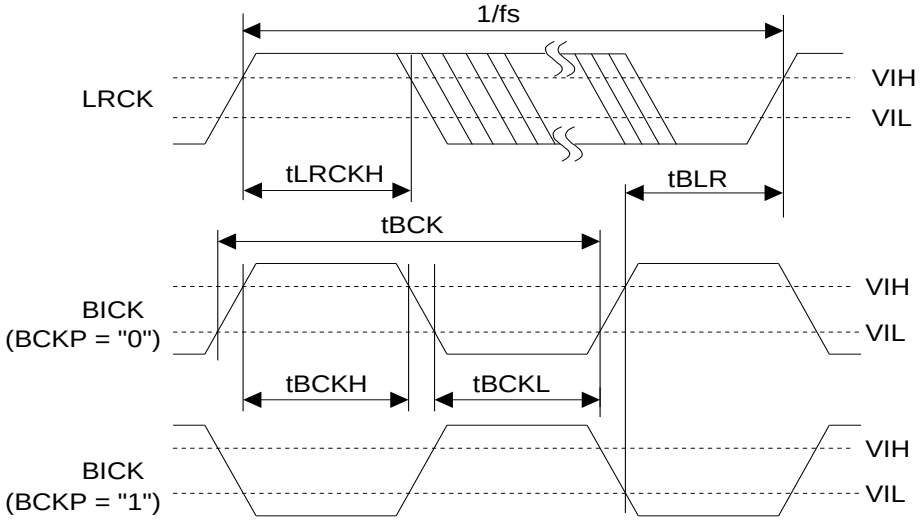


Figure 13. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = “0”)

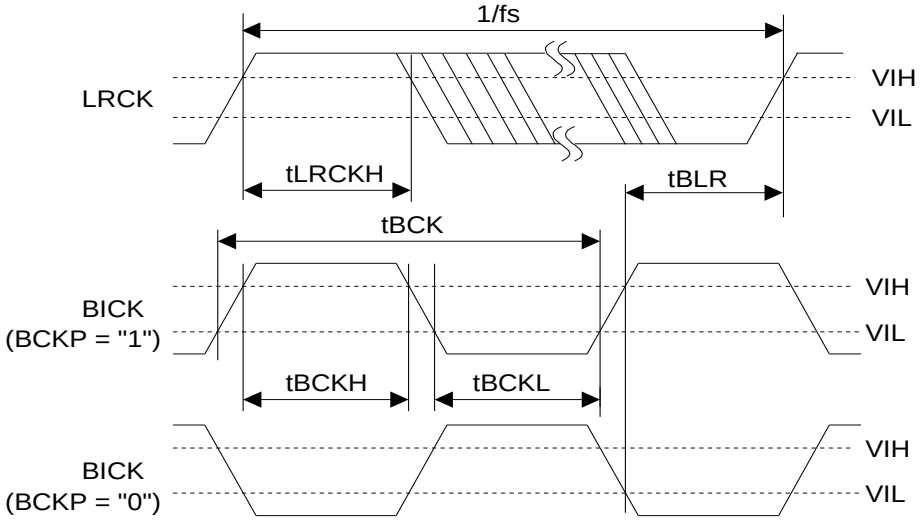


Figure 14. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = “1”)

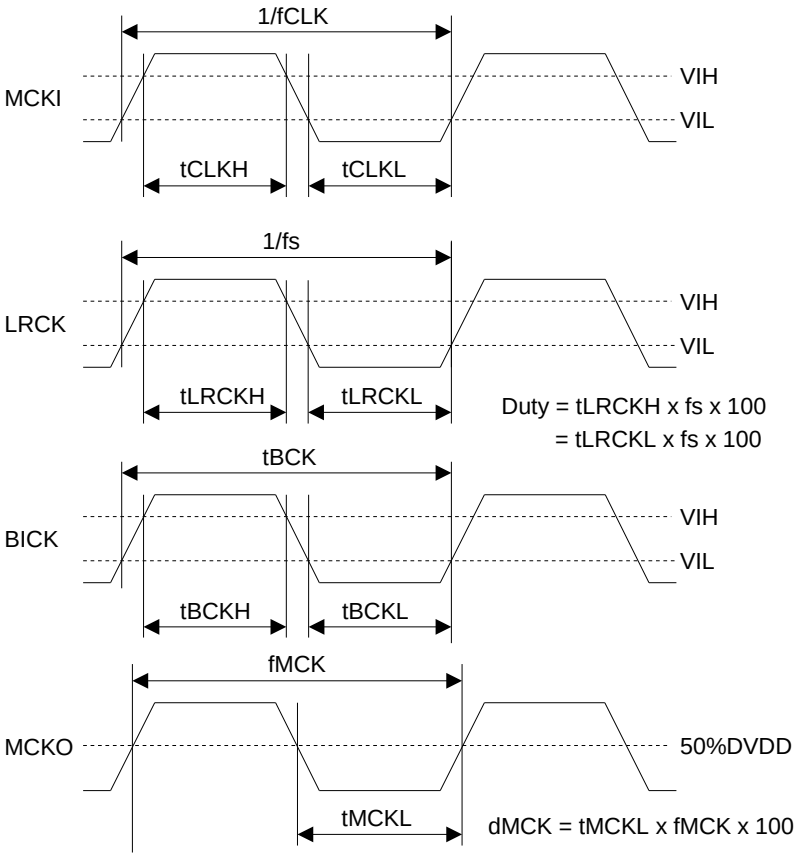


Figure 15. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin, Except DSP mode)

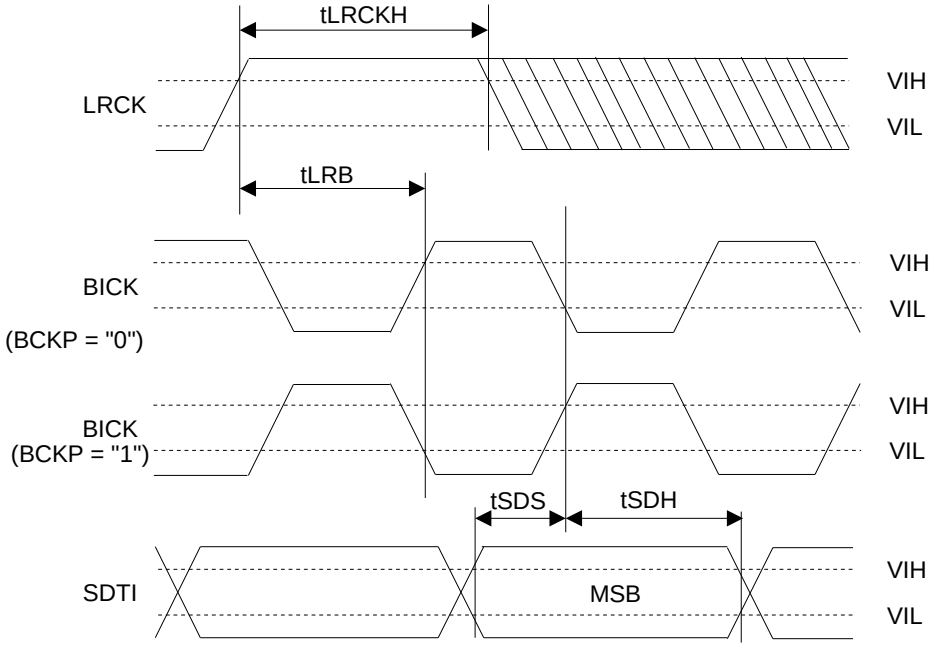


Figure 16. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = “0”)

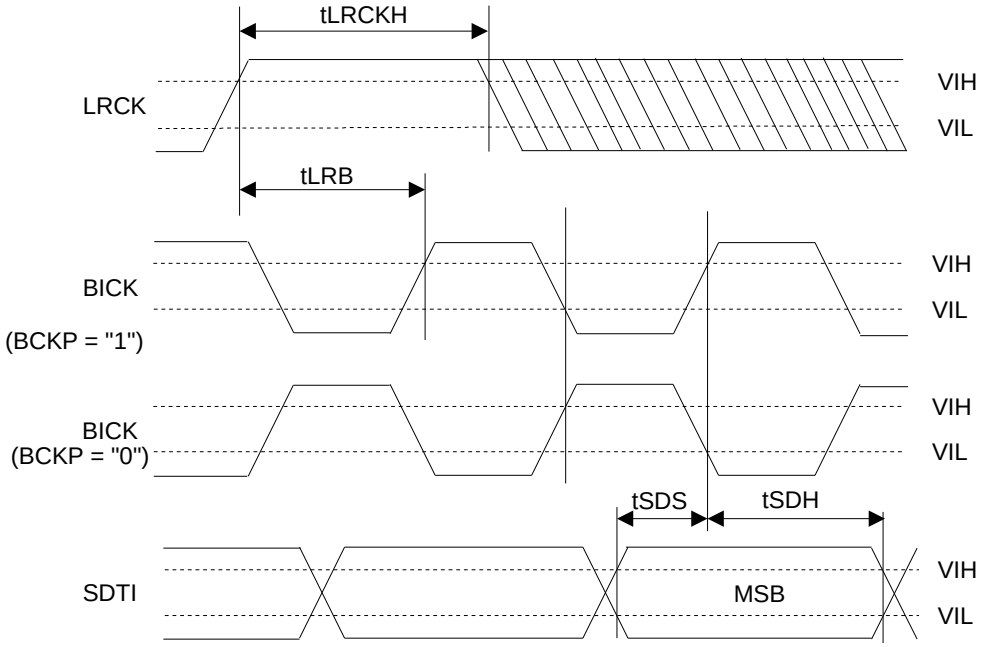


Figure 17. Audio Interface Timing (PLL Slave mode, DSP mode, MSBS = "1")

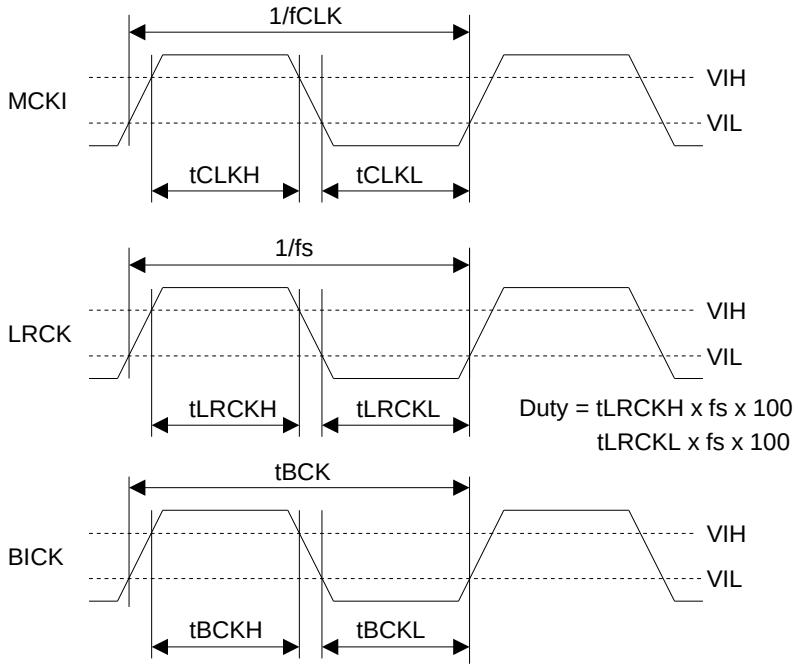


Figure 18. Clock Timing (EXT Slave mode)

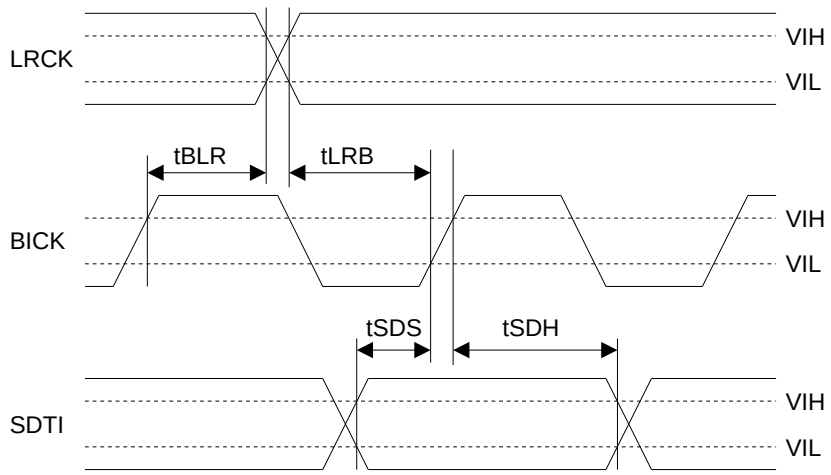


Figure 19. Audio Interface Timing (PLL/EXT Slave mode, Except DSP mode)

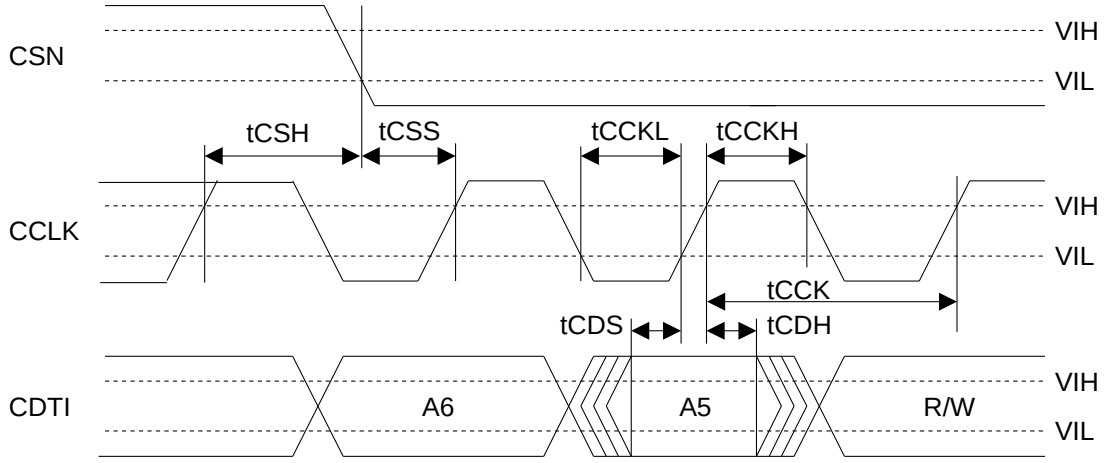


Figure 20. WRITE Command Input Timing

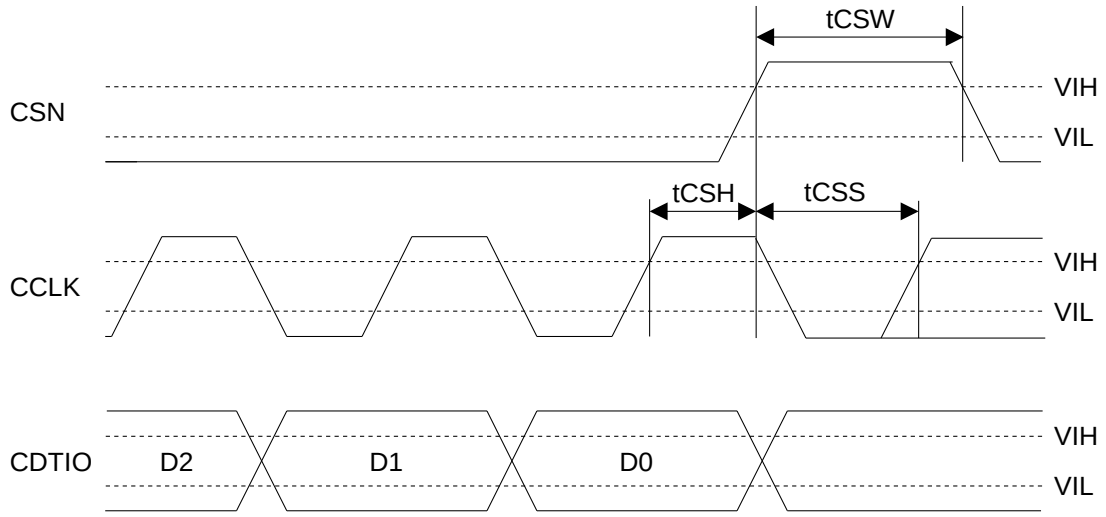


Figure 21. WRITE Data Input Timing

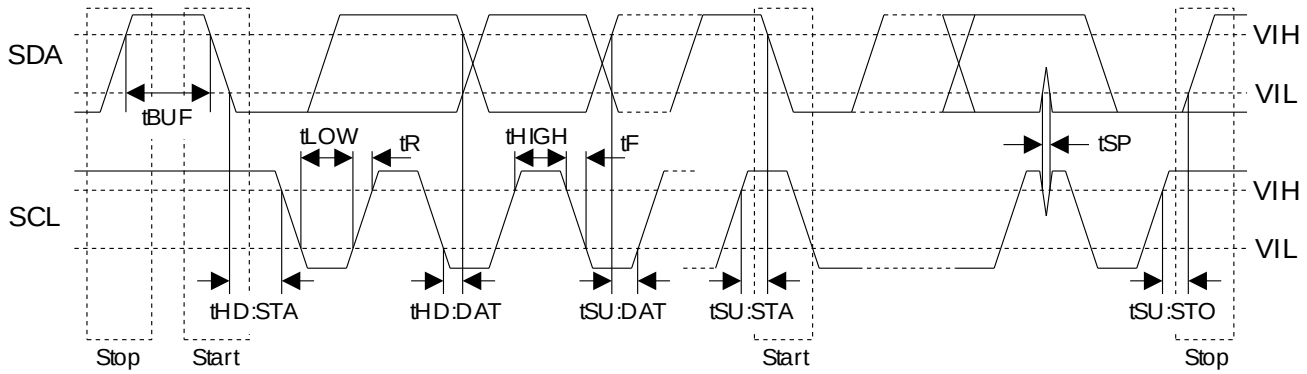


Figure 22. I^{2}C Bus Mode Timing

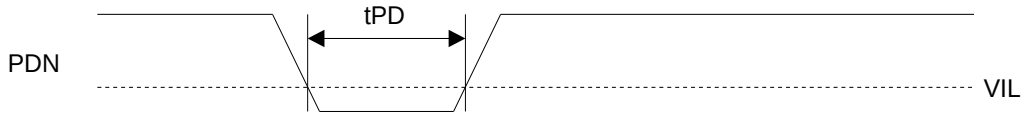


Figure 23. Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 2 and Table 3).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 40)	1	1	See Table 5	Figure 24
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 5	Figure 25
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	See Table 5	Figure 26 Figure 27
EXT Slave Mode	0	0	x	Figure 28
EXT Master Mode	0	1	x	Figure 29

Note 40. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO pin when MCKO bit is "1".

Table 2. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	0	L	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	0	L	Selected by FS1-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	L	Selected by FS1-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Table 3. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4373 is power-down mode (PDN pin = "L") and exits reset state, the AK4373 is slave mode. After exiting reset state, the AK4373 goes to master mode by changing M/S bit = "1".

When the AK4373 is in master mode, LRCK and BICK pins are a floating state until M/S bit becomes "1". LRCK and BICK pins of the AK4373 should be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 4. Select Master/Slave Mode

■ PLL Mode (PMPLL bit = "1")

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 5, whenever the AK4373 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	LRCK pin	1fs	6.8k	220n	160ms	(default)
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
							10k	10n	4ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
							10k	10n	4ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms	
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	40ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	40ms	
9	1	0	0	1	MCKI pin	25MHz	15k	330n	200ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
Others	Others				N/A					

Table 5. Setting of PLL Mode (*fs: Sampling Frequency) (N/A: Not Available)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is the MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 6.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	(default)
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz	
5	0	1	0	1	11.025kHz	
6	0	1	1	0	14.7kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz	
15	1	1	1	1	44.1kHz	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PMPLL bit = "1" (Reference Clock = MCKI pin) (N/A: Not Available)

When PLL2 bit is "0" (PLL reference clock input is the LRCK or BICK pin), the sampling frequency is selected by FS3 and FS2 bits. (Table 7).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz	(default)
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	
Others	Others				N/A	

(x: Don't care, N/A: Not available)

Table 7. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1" PLL Slave Mode 2 (PLL Reference: Clock: LRCK or BICK pin)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK and BICK pins go to "L" and irregular frequency clock is output from the MCKO pin at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin goes to "L" (Table 8).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, the BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except above case)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	See Table 10	See Table 11	1fs Output

Table 8. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". After that, the clock selected by Table 10 is output from the MCKO pin when PLL is locked. DAC output invalid data when the PLL is unlocked. The output signal should be muted by writing "0" to DACH and DACS bits.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 9. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 25MHz or 27MHz) is input to the MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 10) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 11).

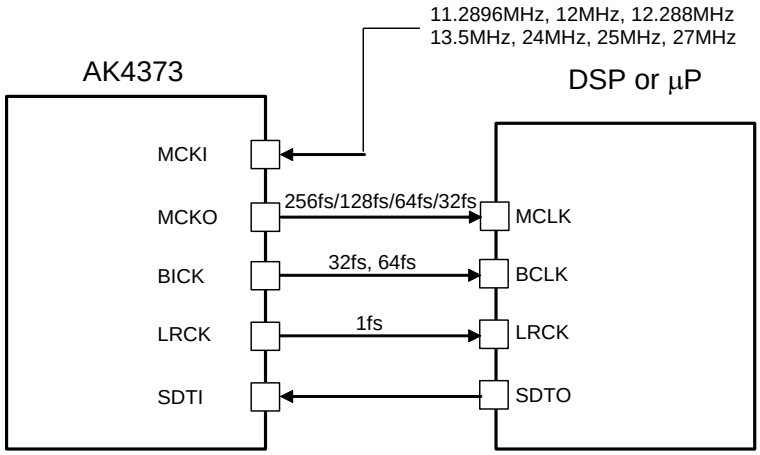


Figure 24. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 10. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 11. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pin. The required clock to the AK4373 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 5).

a) PLL reference clock: MCKI pin

BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 10) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 6).

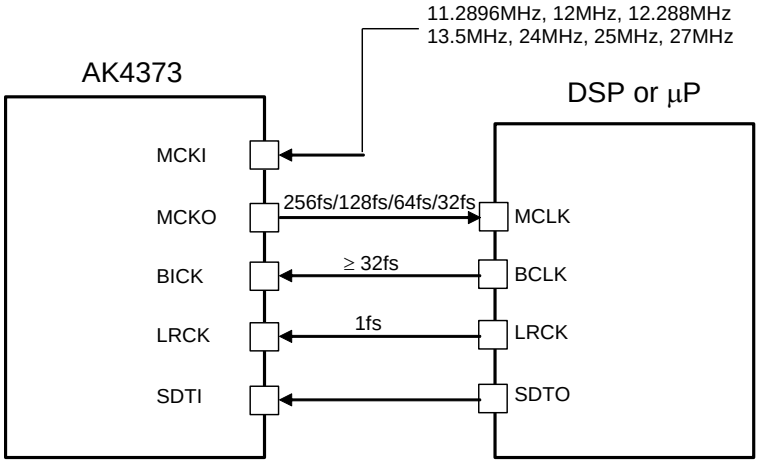


Figure 25. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK or LRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (Table 7).

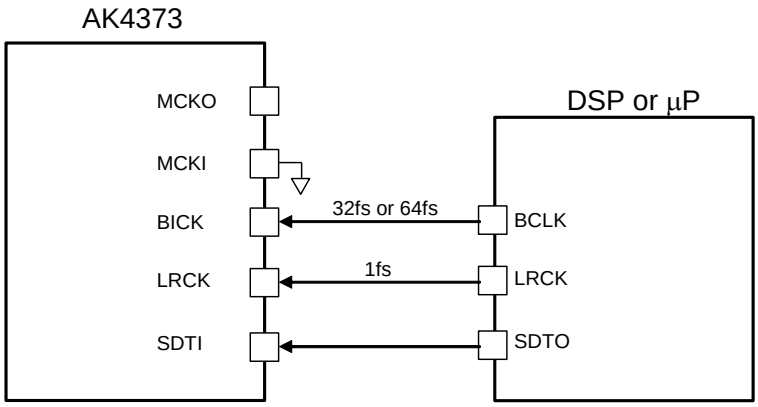


Figure 26. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

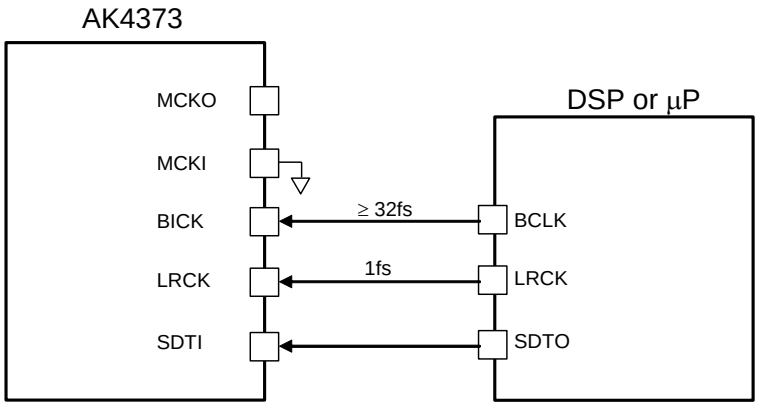


Figure 27. PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

The external clocks (BICK and LRCK) must always be present whenever the DAC is in operation (PMDAC bit = "1"). If these clocks are not provided, the AK4373 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the DAC must be in the power-down mode (PMDAC bit = "0").

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4373 changes to EXT mode. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of a normal audio DAC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by FS1-0 bits (Table 12).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	512fs	7.35kHz ~ 48kHz	

Table 12. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0") (x: Don't care)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through HPL/HPR pins at fs=8kHz is shown in Table 13.

Mode	MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
0	256fs	56dB
2	512fs	
3	512fs	75dB
1	1024fs	93dB

Table 13. Relationship between MCKI and S/N of HPL/HPR pins

The external clocks (MCKI, BICK and LRCK) should always be present whenever the DAC is in operation (PMDAC bit = "1"). If these clocks are not provided, the AK4373 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the DAC must be in the power-down mode (PMDAC bit = "0").

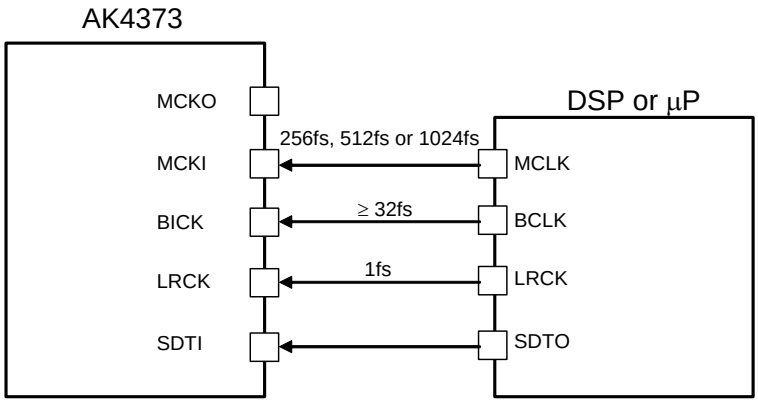


Figure 28. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4373 becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock is input from the MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 14).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	512fs	7.35kHz ~ 48kHz	

Table 14. MCKI Frequency at EXT Master Mode (PMPLL bit = "0", M/S bit = "1") (x: Don't care)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through the HPL/HPR pins at fs=8kHz is shown in Table 15.

Mode	MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
0	256fs	56dB
2	512fs	
3	512fs	75dB
1	1024fs	93dB

Table 15. Relationship between MCKI and S/N of HPL/HPR pins

MCKI should always be present whenever the DAC is in operation (PMDAC bit = "1"). If MCKI is not provided, the AK4373 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the DAC should be in the power-down mode (PMDAC bit = "0").

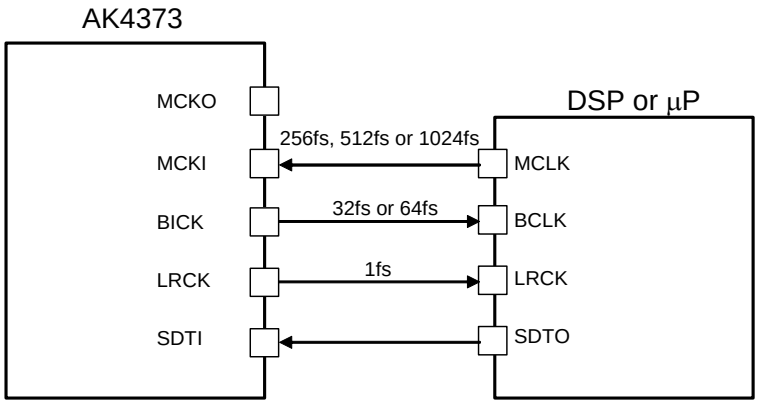


Figure 29. EXT Master Mode

■ MCKO output frequency

MCKO output frequency can be controlled by PS1/0 bits when MCKO bit is "1" regardless of any clock mode (PLL/EXT, Master/Slave).

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 16. MCKO Output Frequency (EXT Mode, MCKO bit = "1")

■ System Reset

The PDN pin must be held to "L" upon power-up. The 4373 should be reset by bringing PDN pin "L" for 150ns or more. All of the internal register values are initialized by the system reset. After exiting reset, VCOM, DAC, HPL, HPR, LOUT, ROUT, SPP and SPN switch to the power-down state. The contents of the control register are maintained until the reset is completed.

The DAC exits reset and power down states by MCKI after the PMDAC bit is changed to "1". The DAC is in power-down mode until MCKI is input.

■ Audio Interface Format

Three types of data formats are available and are selected by setting the DIF1-0 bits (Table 17). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4373 in master mode, but must be input to the AK4373 in slave mode.

Mode	DIF2 bit	DIF1 bit	DIF0 bit	SDTI (DAC)	BICK	Figure	
0	0	0	0	16 bit DSP Mode	≥32fs	Table 18	
1	0	0	1	16 bit LSB justified	≥32fs	Figure 34	
2	0	1	0	16/20/24 bit MSB justified	32fs or ≥48fs	Figure 36	(default)
3	0	1	1	16/20/24 bit I^2S compatible	32fs or ≥48fs	Figure 37	
4	1	0	0	20 bit LSB justified	≥40fs	Figure 35	
5	1	0	1	24 bit LSB justified	≥48fs	Figure 35	
6	1	1	0	20 bit DSP Mode	≥40fs	Table 18	
7	1	1	1	24 bit DSP Mode	≥48fs	Table 18	

Table 17. Audio Interface Format

In Modes 1- 5 the SDTI is latched on the rising edge ("↑") of BICK.

In Modes 0/6/7 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits (Table 18, Table 19 and Table 20).

DIF2	DIF1	DIF0	MSBS	BCKP	Audio Interface Format	Figure	
0	0	0	0	0	MSB of SDTI is latched by the falling edge ("↓") of the BICK just after the rising edge ("↑") of the first BICK after the rising edge ("↑") of LRCK.	Figure 30	(default)
			0	1	MSB of SDTI is latched by the rising edge ("↑") of the BICK just after the falling edge ("↓") of the first BICK after the rising edge ("↑") of LRCK.	Figure 31	
			1	0	MSB of SDTI is latched by the 2nd falling edge ("↓") of the BICK after the rising edge ("↑") of LRCK.	Figure 32	
			1	1	MSB of SDTI is latched by the 2nd rising edge ("↑") of the BICK after the rising edge ("↑") of LRCK..	Figure 33	

Table 18. Audio Interface Format in Mode 0

DIF2	DIF1	DIF0	MSBS	BCKP	Audio Interface Format	Figure	
1	1	0	0	0	MSB of SDTI is latched by the falling edge (“↓”) of the BICK just after the rising edge (“↑”) of the first BICK after the rising edge (“↑”) of LRCK.	Figure 38	(default)
			0	1	MSB of SDTI is latched by the rising edge (“↑”) of the BICK just after the falling edge (“↓”) of the first BICK after the rising edge (“↑”) of LRCK.	Figure 39	
			1	0	MSB of SDTI is latched by the 2nd falling edge (“↓”) of the BICK after the rising edge (“↑”) of LRCK.	Figure 40	
			1	1	MSB of SDTI is latched by the 2nd rising edge (“↑”) of the BICK after the rising edge (“↑”) of LRCK..	Figure 41	

Table 19. Audio Interface Format in Mode 6

DIF2	DIF1	DIF0	MSBS	BCKP	Audio Interface Format	Figure	
1	1	1	0	0	MSB of SDTI is latched by the falling edge (“↓”) of the BICK just after the rising edge (“↑”) of the first BICK after the rising edge (“↑”) of LRCK.	Figure 42	(default)
			0	1	MSB of SDTI is latched by the rising edge (“↑”) of the BICK just after the falling edge (“↓”) of the first BICK after the rising edge (“↑”) of LRCK.	Figure 43	
			1	0	MSB of SDTI is latched by the 2nd falling edge (“↓”) of the BICK after the rising edge (“↑”) of LRCK.	Figure 44	
			1	1	MSB of SDTI is latched by the 2nd rising edge (“↑”) of the BICK after the rising edge (“↑”) of LRCK..	Figure 45	

Table 20. Audio Interface Format in Mode 7

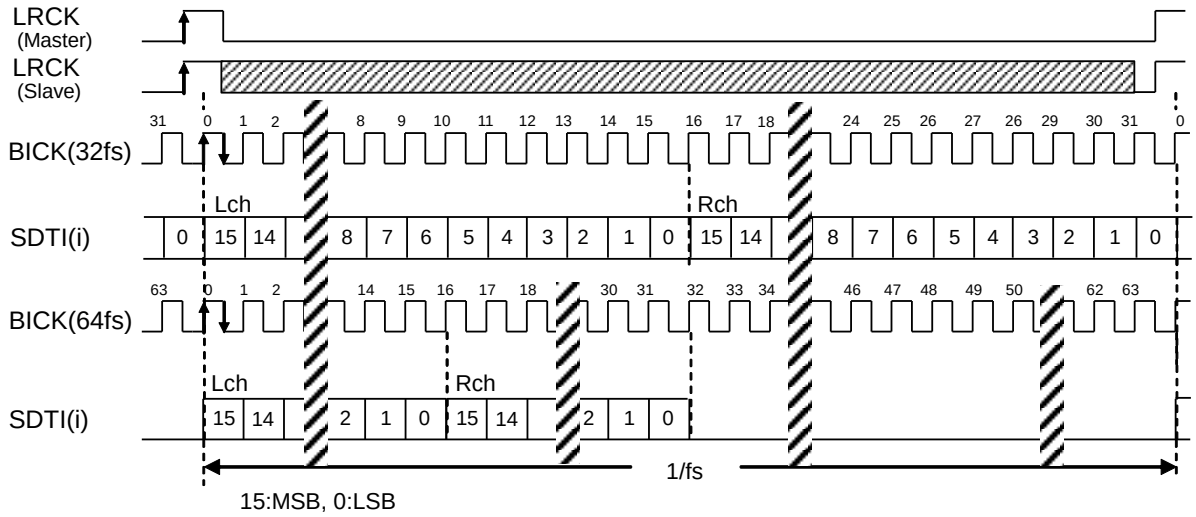


Figure 30. Mode 0 Timing (BCKP = "0", MSBS = "0")

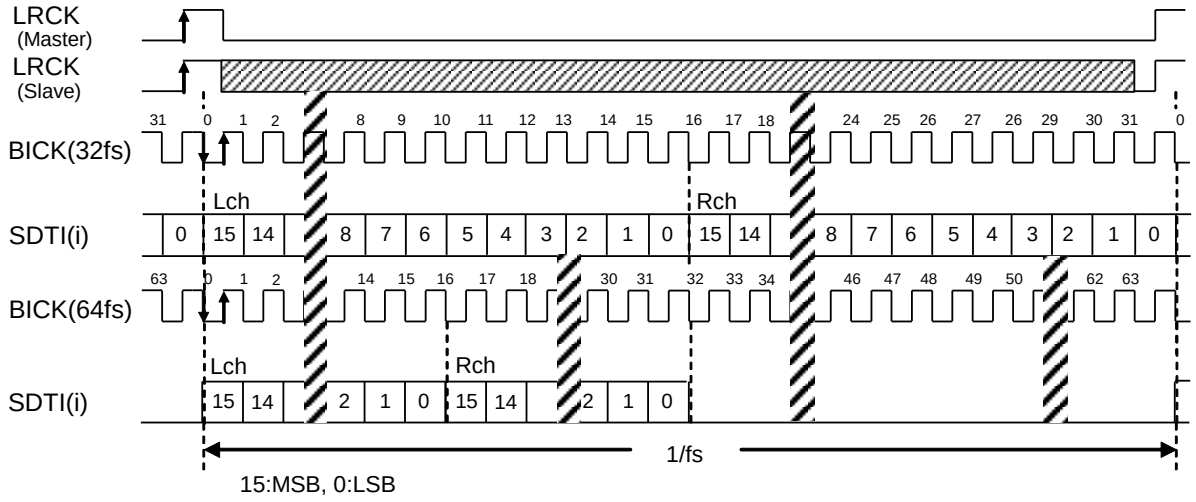


Figure 31. Mode 0 Timing (BCKP = "1", MSBS = "0")

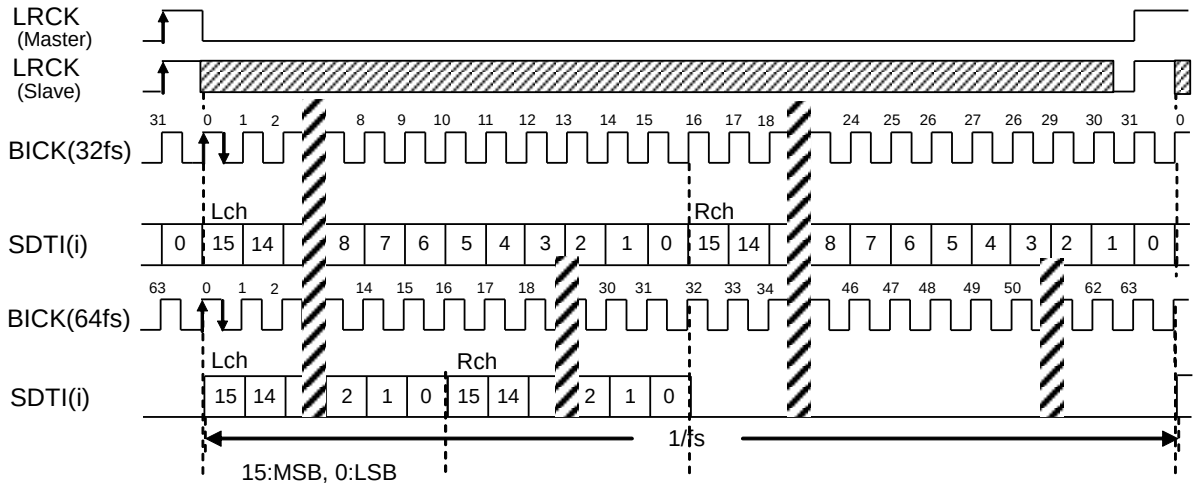


Figure 32. Mode 0 Timing (BCKP = "0", MSBS = "1")

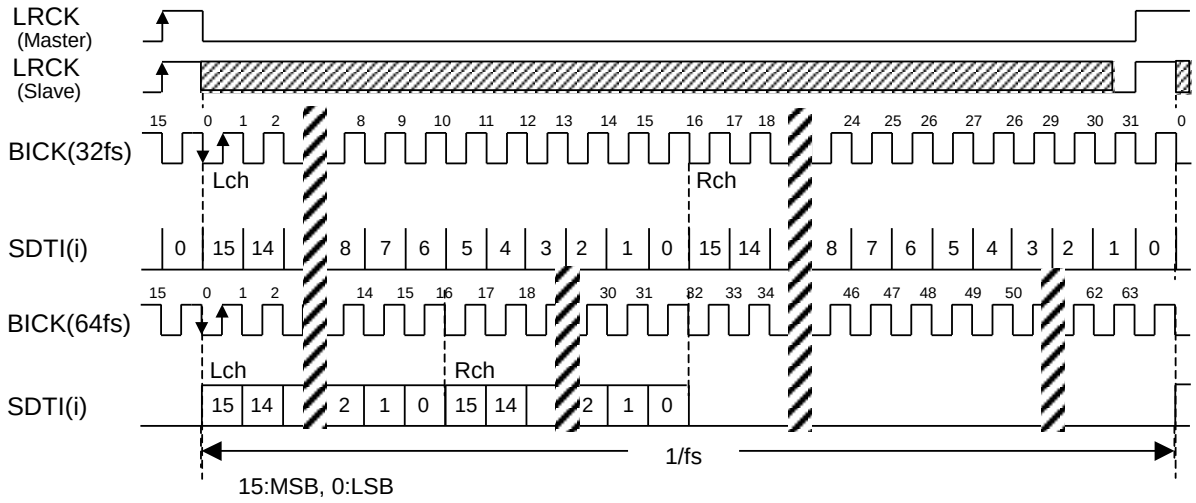


Figure 33. Mode 0 Timing (BCKP = "1", MSBS = "1")

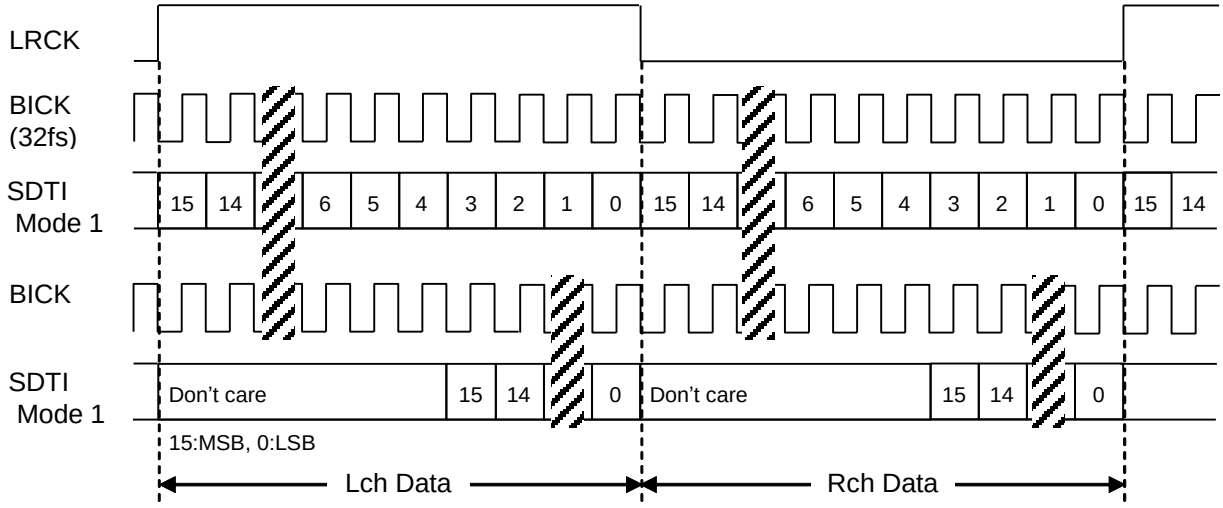


Figure 34. Mode 1 Timing

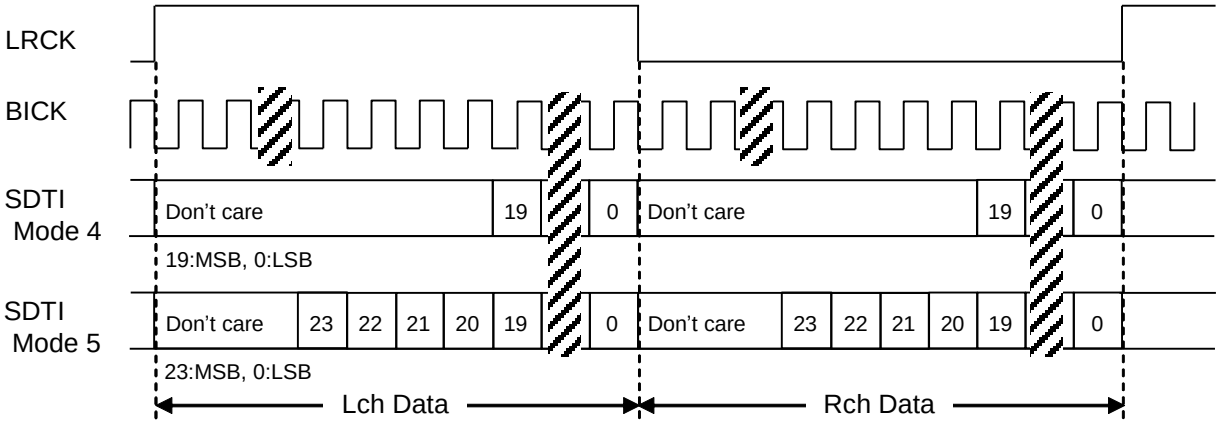


Figure 35. Mode 4, 5 Timing

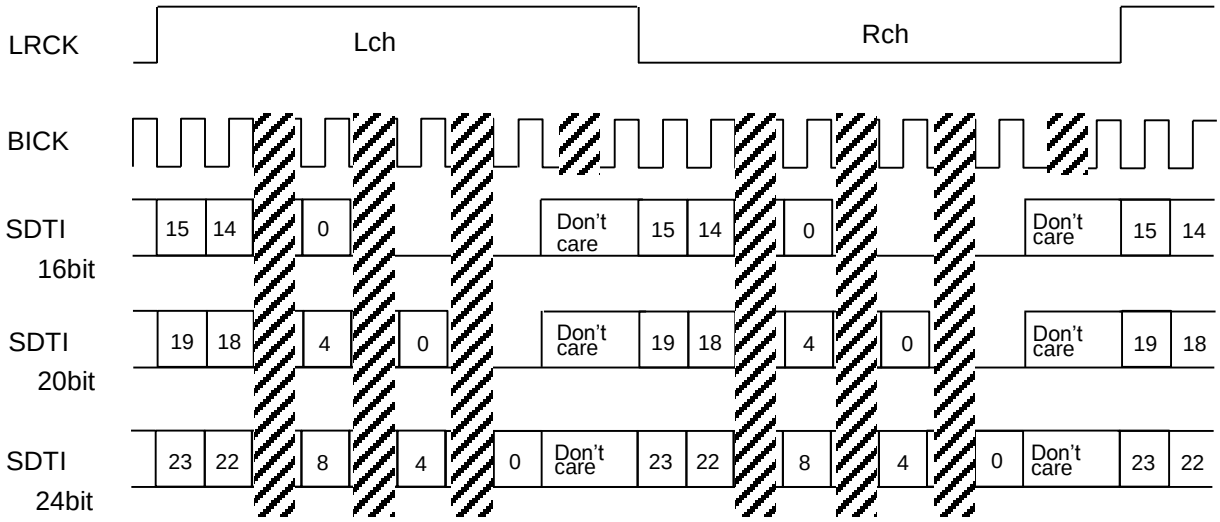


Figure 36. Mode 2 Timing

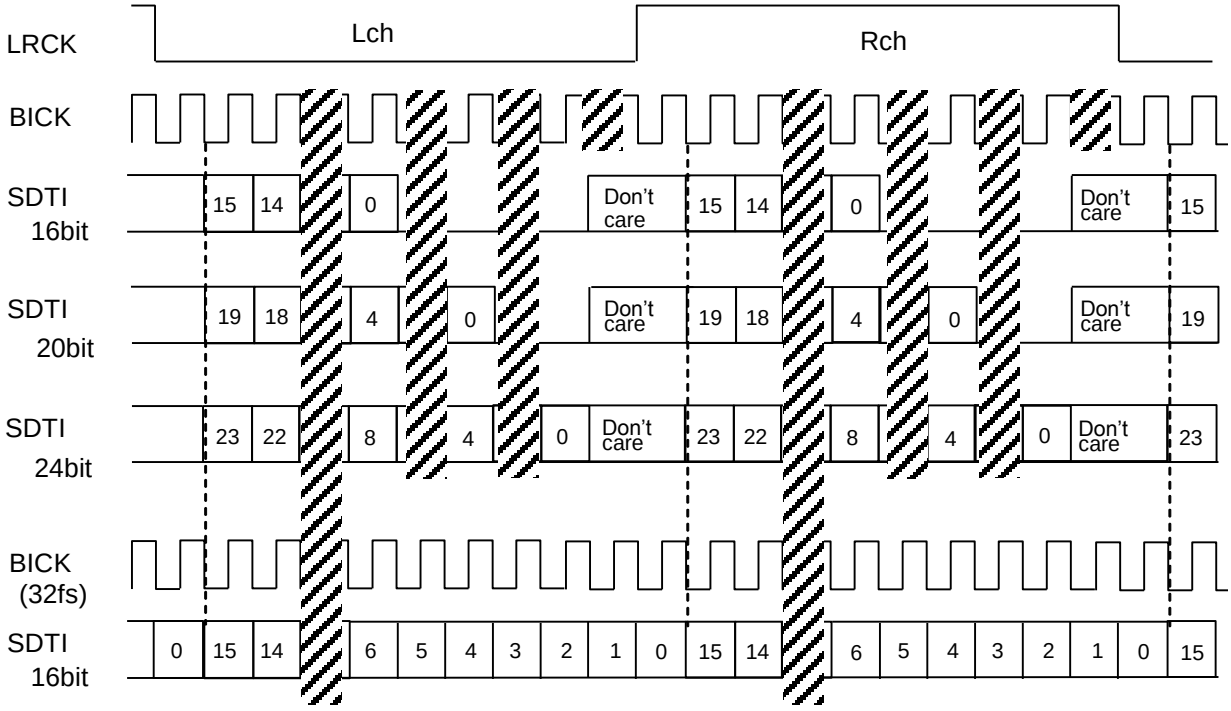


Figure 37. Mode 3 Timing

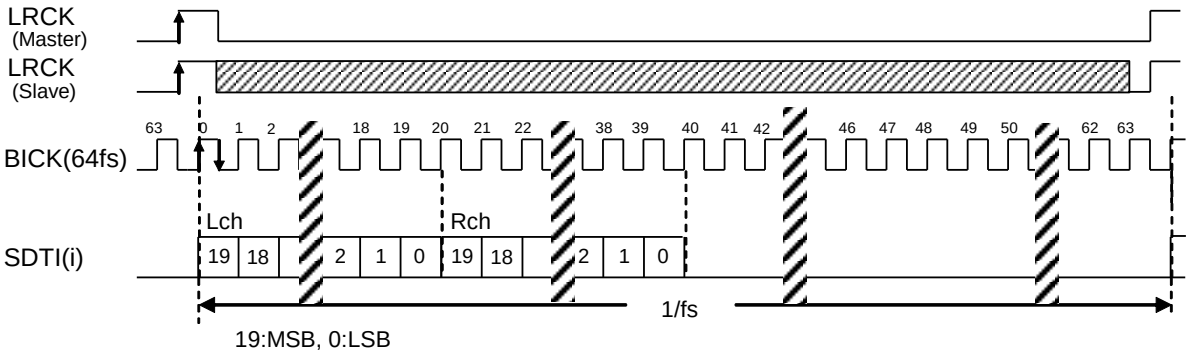


Figure 38. Mode 6 Timing (BCKP = "0", MSBS = "0")

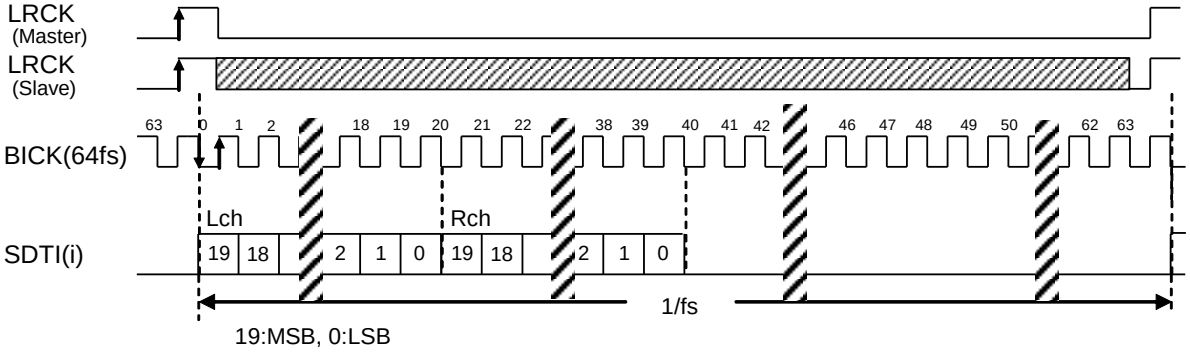


Figure 39. Mode 6 Timing (BCKP = "1", MSBS = "0")

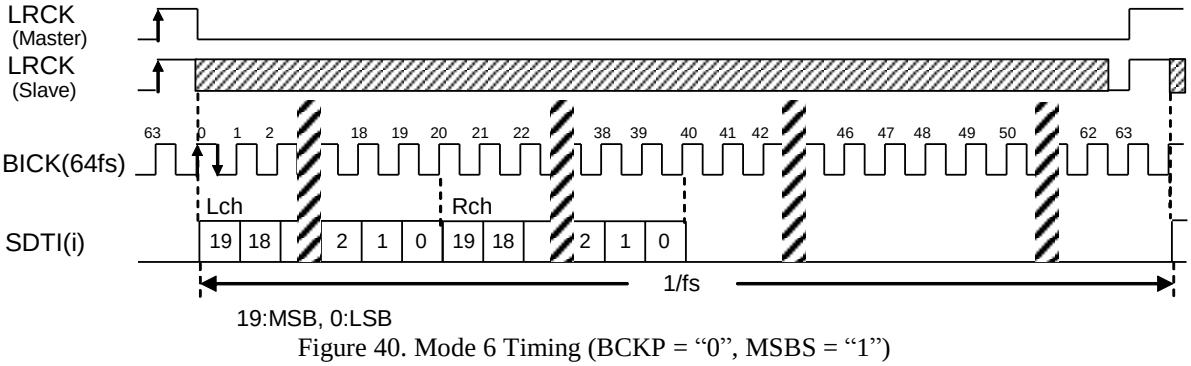


Figure 40. Mode 6 Timing (BCKP = "0", MSBS = "1")

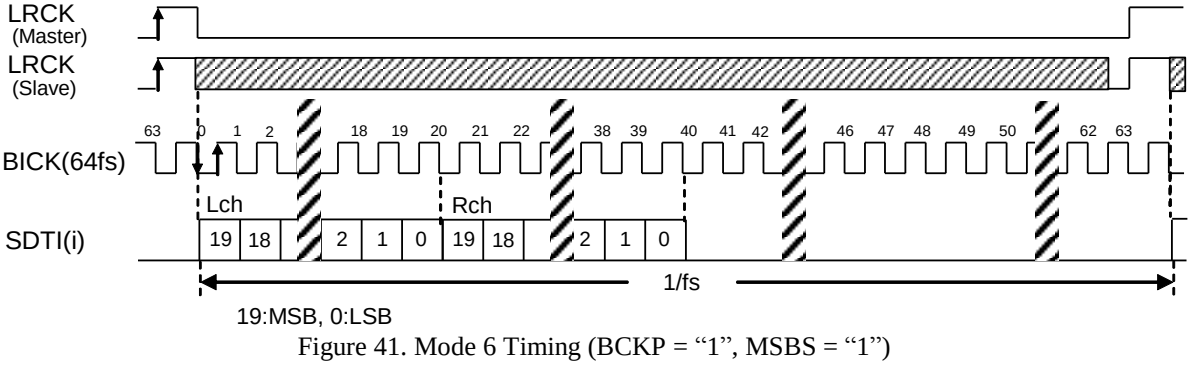


Figure 41. Mode 6 Timing (BCKP = "1", MSBS = "1")

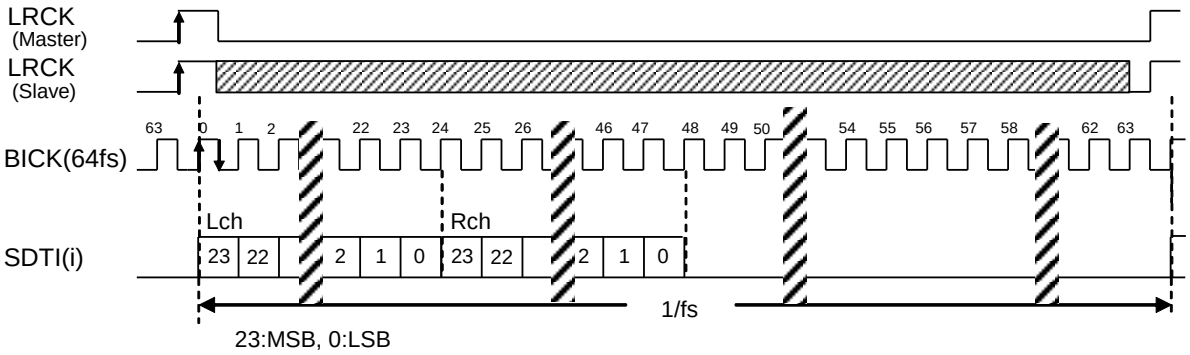


Figure 42. Mode 7 Timing (BCKP = "0", MSBS = "0")

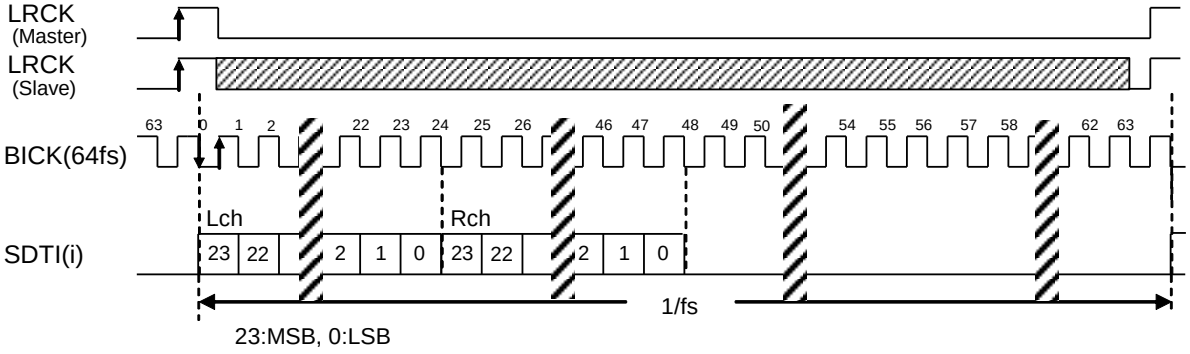


Figure 43. Mode 7 Timing (BCKP = "1", MSBS = "0")

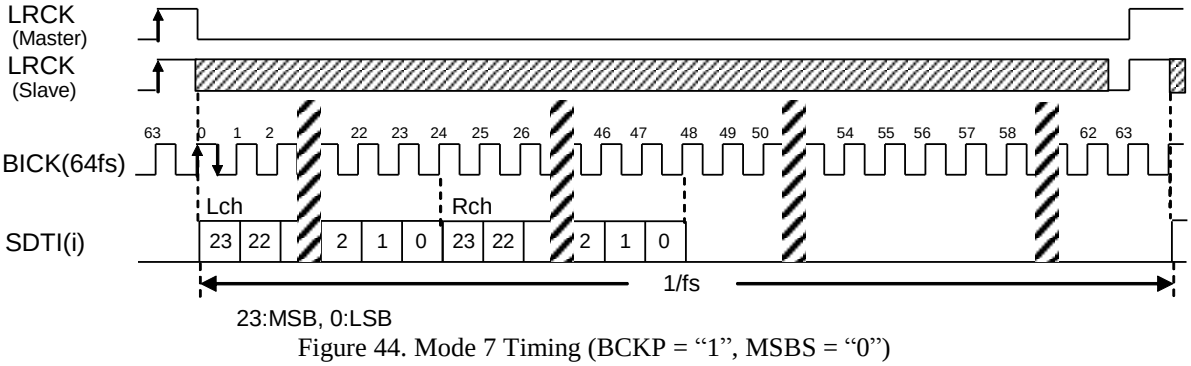


Figure 44. Mode 7 Timing (BCKP = "1", MSBS = "0")

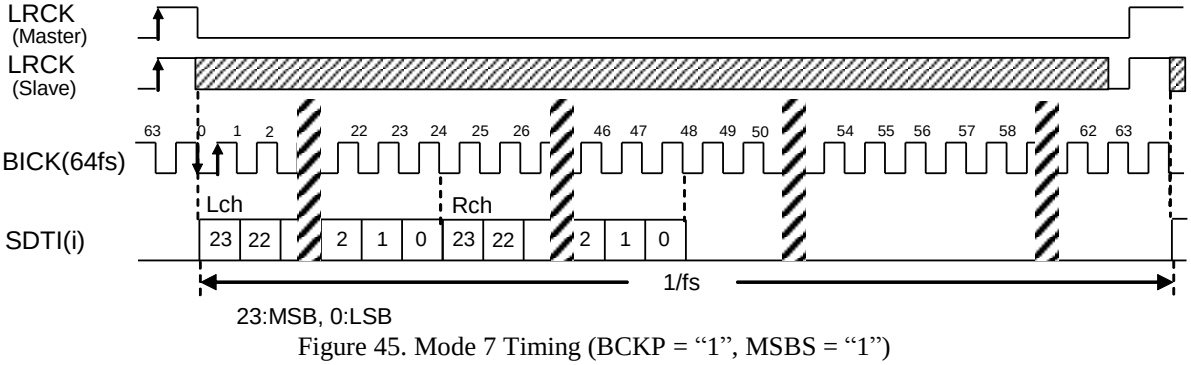


Figure 45. Mode 7 Timing (BCKP = "1", MSBS = "1")

■ Digital EQ/HPF/LPF

The AK4373 performs high/low pass filter, stereo separation emphasis, gain compensation, five programmable biquads, ALC (Automatic Level Control) and digital volume by digital domain for input data (Figure 46). HPF, LPF, FIL3, and EQ blocks are IIR filters of 1st order. The filter coefficient of HPF, LPF, FIL3, and EQ blocks can be set to any value.

Refer to the section of "Five Programmable Biquads", "ALC operation" and "Digital Output Volume" about five programmable biquads, ALC and digital volume, respectively.

FIL3 coefficient also sets the attenuation of the stereo separation emphasis.

The combination of GN1-0 bit (Table 21) and EQ coefficient set the compensation gain.

FIL3 block becomes HPF when F3AS bits are "0" and become LPF when F3AS bits are "1".

When EQ, HPF and LPF bits are "0", EQ, HPF and LPF blocks become "through" (0dB). When each filter coefficient is changed, each filter should be set to "through".

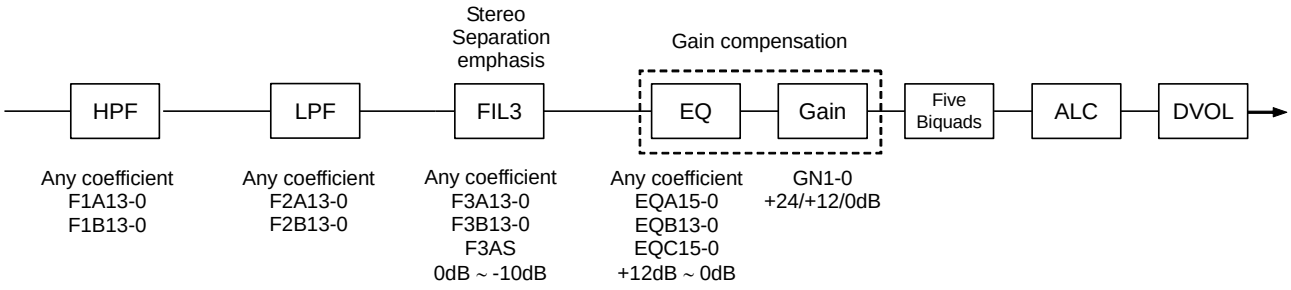


Figure 46. Digital EQ/HPF/LPF (default)

GN1	GN0	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 21. Gain select of gain block (x: Don't care)

[Filter Coefficient Setting]

(1) High Pass Filter (HPF)

fs: Sampling frequency
fc: Cut-off frequency
f: Input signal frequency

Register setting (Note 41)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function	Amplitude	Phase
$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$	$M(f) = A \sqrt{\frac{2 - 2\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$	$\theta(f) = \tan^{-1} \frac{(B+1)\sin(2\pi f/fs)}{1 - B + (B-1)\cos(2\pi f/fs)}$

(2) Low Pass Filter (LPF)

fs: Sampling frequency
fc: Cut-off frequency
f: Input signal frequency

Register setting (Note 41)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F2B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function	Amplitude	Phase
$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$	$M(f) = A \sqrt{\frac{2 + 2\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$	$\theta(f) = \tan^{-1} \frac{(B-1)\sin(2\pi f/fs)}{1 + B + (B+1)\cos(2\pi f/fs)}$

(3) Stereo Separation Emphasis Filter (FIL3)

1) When FIL3 is set to "HPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ –10dB)

Register setting (Note 41)
FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function	Amplitude	Phase
$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$	$M(f) = A \sqrt{\frac{2 - 2\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$	$\theta(f) = \tan^{-1} \frac{(B+1)\sin(2\pi f/fs)}{1 - B + (B-1)\cos(2\pi f/fs)}$

2) When FIL3 is set to "LPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ –10dB)

Register setting (Note 41)
FIL3: F3AS bit = "1", F3A [13:0] bits =A, F3B [13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function	Amplitude	Phase
$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$	$M(f) = A \sqrt{\frac{2 + 2\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$	$\theta(f) = \tan^{-1} \frac{(B-1)\sin(2\pi f/fs)}{1 + B + (B+1)\cos(2\pi f/fs)}$

(4) EQ

fs: Sampling frequency
fc_1: Pole frequency
fc_2: Zero-point frequency
f: Input signal frequency
K: Filter gain [dB] (Maximum +12dB)

Register setting (Note 41)
EQA[15:0] bits =A, EQB[13:0] bits =B, EQC[15:0] bits =C
(MSB=EQA15, EQB13, EQC15; LSB=EQA0, EQB0, EQC0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer function	Amplitude	Phase
$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$	$M(f) = \sqrt{\frac{A^2 + C^2 + 2AC\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$	$\theta(f) = \tan^{-1}\frac{(AB-C)\sin(2\pi f/fs)}{A + BC + (AB+C)\cos(2\pi f/fs)}$

Note 41. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sign bit.

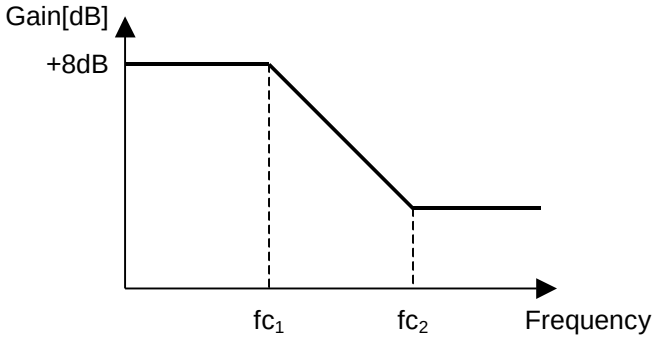
[Filter Coefficient Setting Example]

1) HPF block
   Example: fs=44.1kHz, fc=100Hz
   F1A[13:0] bits = 01 1111 1100 0110
   F1B[13:0] bits = 10 0000 0111 0100

2) LPF block
   Example: fs=44.1kHz, fc=10kHz
   F2A[13:0] bits = 01 0001 0010 1100
   F2B[13:0] bits = 00 0010 0101 0111

3) FIL3 block
   Example: fs=44.1kHz, fc=4kHz, Gain=-6dB, F3AS bit = "1" (LPF)
   F3A[13:0] bits = 00 0011 1010 0010
   F3B[13:0] bits = 10 1110 1000 0000

4) EQ block
   Example: fs=44.1kHz, fc_1=300Hz, fc_2=3000Hz, Gain=+8dB



   EQA[15:0] bits = 0000 1001 0110 1110
   EQB[13:0] bits = 10 0001 0101 1001
   EQC[15:0] bits = 1111 1001 1110 1111

■ Five Programmable Biquads

This block can be used as Equalizer or Notch Filter. 5-band Equalizer (EQ1, EQ2, EQ3, EQ4 and EQ5) is ON/OFF independently by EQ1, EQ2, EQ3, EQ4 and EQ5 bits. When the Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. E4A15-0, E4B15-0 and E4C15-0 bits set the coefficient of EQ4. E5A15-0, E5B15-0 and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1~5) coefficient should be set when EQx bit = "0" or PMDAC bit = "0".

fs: Sampling frequency
fo_1 ~ fo_5: Center frequency
fb_1 ~ fb_5: Band width where the gain is 3dB different from center frequency
K_1 ~ K_5 : Gain ($-1 \le K_n \le 3$)

Register setting (Note 42)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer function
$H(z) = 1 + h_1(z) + h_2(z) + h_3(z) + h_4(z) + h_5(z)$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency should be set as below.
$fo_n / fs < 0.497$

Note 42. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sign bit.

■ ALC Operation

The ALC (Automatic Level Control) is controlled by ALC block when ALC bit is "1".

1. ALC Limiter Operation

During ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 22), the AVL and AVR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (Table 23).

When ZELMN bit = "0" (zero cross detection is enabled), the AVL and AVR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 24). When ALC output level exceeds full-scale, IVL and IVR values are immediately (Period: 1/fs) changed. When ALC output level is less than full-scale, IVL and IVR values are changed at the individual zero crossing point of each channels or at the zero crossing timeout.

When ZELMN bit = "1" (zero cross detection is disabled), AVL and AVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuate operation is done continuously until the input signal level becomes ALC limiter detection level (Table 22) or less. After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

LMTH1	LMTH0	ALC Limier Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
0	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
1	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 22. ALC Limiter Detection Level / Recovery Counter Reset Level

LMAT1	LMAT0	ALC1 Limiter ATT Step (0.375dB/step)	
		ALC1 Output ≥ LMTH	
0	0	1	(default)
0	1	2	
1	0	2	
1	1	1	

Table 23. ALC Limiter ATT Step

ZTM1	ZTM0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 24. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

ALC recovery operation wait for the WTM2-0 bits (Table 25) to be set after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 22) during the wait time, ALC recovery operation is completed. The AVL and AVR values are automatically incremented by RGAIN1-0 bits (Table 26) up to the set reference level (Table 27) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 24). Then the AVL and AVR are set to the same value for both channels. ALC recovery operation is executed at a period set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, ALC recovery operation waits until WTM2-0 period and the next recovery operation is completed. If ZTM1-0 is longer than WTM2-0 and no zero crossing occurs, ALC recovery operation is made at a period set by ZTM1-0 bits.

For example, when the current AVOL value is 30H and RGAIN1-0 bits are set to "01", AVOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the AVOL value exceeds the reference level (REF7-0), the AVOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

ALC operation corresponds to the impulse noise. When the impulse noise is input, ALC recovery operation is faster than a normal recovery operation (Fast Recovery Operation). When large noise is input to microphone instantaneously, quality of small signal level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 28).

WTM2	WTM1	WTM0		ALC Recovery Operation Waiting Period			
				8kHz	16kHz	44.1kHz	
0	0	0	128/fs	16ms	8ms	2.9ms	(default)
0	0	1	256/fs	32ms	16ms	5.8ms	
0	1	0	512/fs	64ms	32ms	11.6ms	
0	1	1	1024/fs	128ms	64ms	23.2ms	
1	0	0	2048/fs	256ms	128ms	46.4ms	
1	0	1	4096/fs	512ms	256ms	92.9ms	
1	1	0	8192/fs	1024ms	512ms	185.8ms	
1	1	1	16384/fs	2048ms	1024ms	371.5ms	

Table 25. ALC Recovery Operation Waiting Period

RGAIN1	RGAIN0	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 26. ALC Recovery GAIN Step

REF7-0	GAIN(dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54.0		
00H	MUTE		

Table 27. Reference Level at ALC Recovery operation

RFST1 bit	RFST0 bit	Recovery Speed	
0	0	4 times	(default)
0	1	8 times	
1	0	16times	
1	1	N/A	

Table 28. Fast Recovery Speed Setting (N/A: not available)

3. Example of ALC Operation

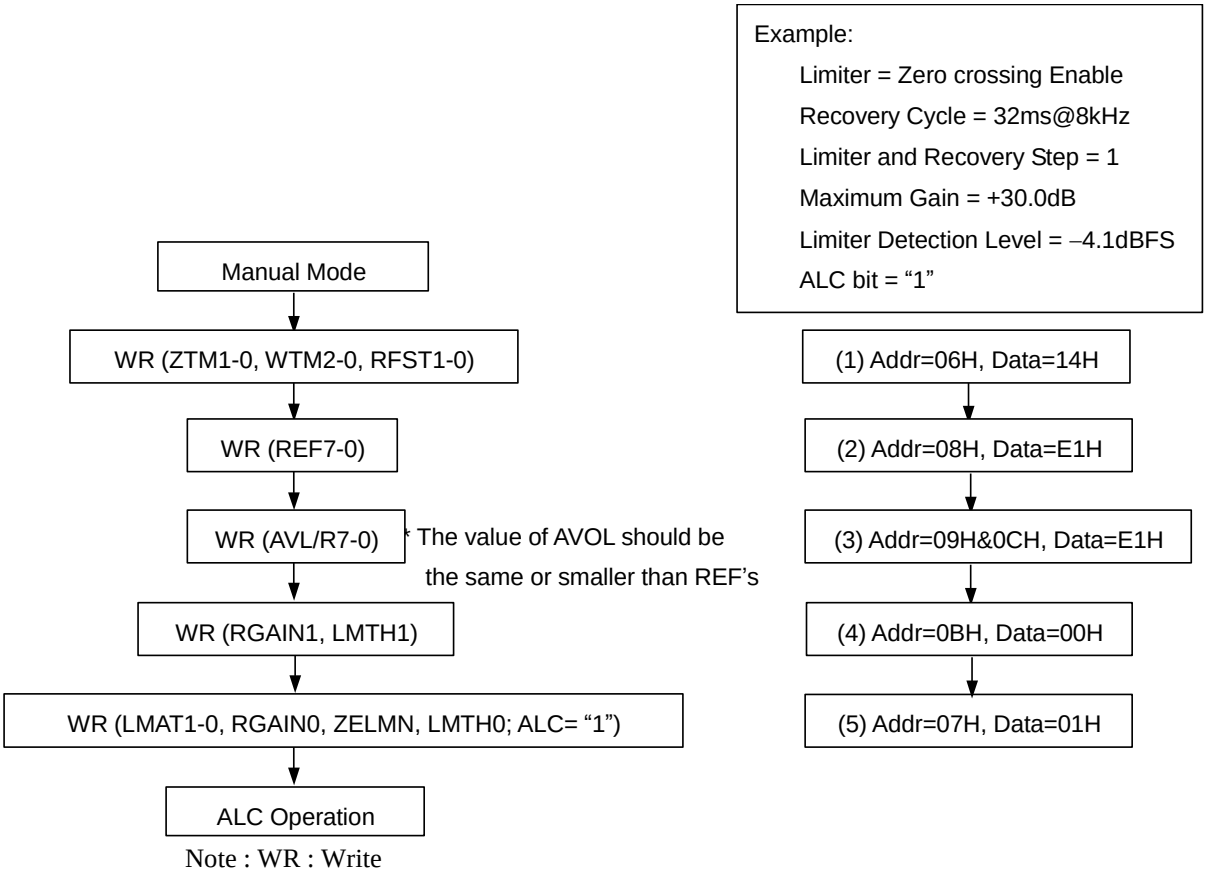
Table 29 shows the examples of the ALC setting.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same or longer data as ZTM1-0 bits.	001	32ms	011	23.2ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
AVL7-0, AVR7-0	Gain of AVOL	E1H	+30dB	E1H	+30dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC	ALC enable	1	Enable	1	Enable

Table 29. Example of the ALC setting

The following registers should not be changed during ALC operation. These bits should be changed after ALC operation is finished by ALC bit = “0” or PMDAC bit = “0”.

- **LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN, RFST1-0**



Note : WR : Write

Figure 47. Registers set-up sequence at ALC operation

■ Digital Volume at ALC Block (Manual Mode)

The digital volume at ALC block changes to a manual mode when ALC bit is "0". This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for ALC operation (ZTM1-0, LMTH1-0 and etc)
2. When the registers for ALC operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.

AVL7-0 and AVR7-0 bits set the gain of the volume control at ALC block (Table 30). The AVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits.

When ALC is not used, AVL7-0 and AVR7-0 bits should be set to "91H" (0dB).

AVL7-0 AVR7-0	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 30. ALC Block Digital Volume Setting

When writing to the AVL7-0 and AVR7-0 bits continuously, the control register should be written by an interval more than zero crossing timeout. If not, AVL and AVR are not changed since zero crossing counter is reset at every write operation. If the same register value as the previous write operation is written to AVL and AVR, this write operation is ignored and zero crossing counter is not reset. Therefore, AVL and AVR can be written by an interval less than zero crossing timeout.

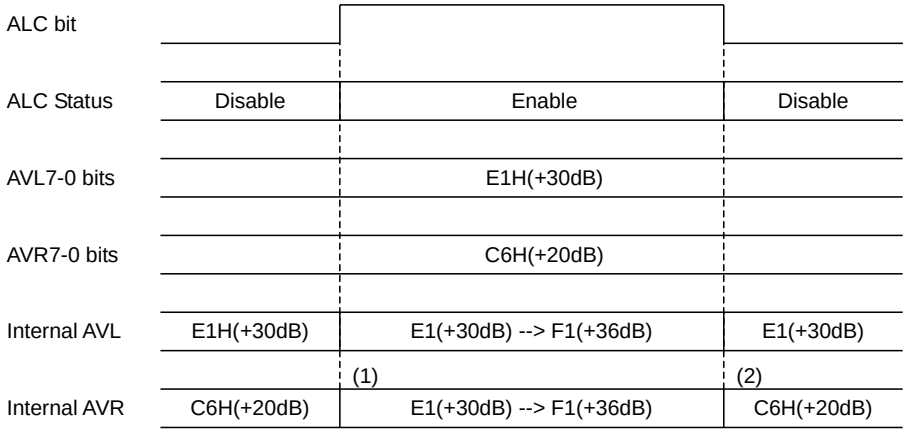


Figure 48. AVOL value during ALC operation

(1) The AVL value becomes the start value if the AVL and AVR are different when the ALC starts. The wait time from ALC bit = "1" to ALC operation start by AVL7-0 bits is at most recovery time (WTM2-0 bits) plus zero cross timeout period (ZTM1-0 bits).
(2) Writing to AVL and AVR registers (09H and 0CH) is ignored during ALC operation. After ALC is disabled, the AVOL changes to the last written data by zero crossing or timeout. When ALC is enabled again, ALC bit should be set to "1" by an interval more than zero crossing timeout period after ALC bit = "0".

■ De-emphasis Filter

The AK4373 includes the digital de-emphasis filter (tc = 50/15μs) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 31).

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 31. De-emphasis Control

■ Digital Output Volume

The AK4373 has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the DVL7-0 and DVR7-0 bits. The volume is included in front of a DAC block. The input data of DAC is changed from +12 to –115dB or MUTE. When the DVOLC bit = "1", the DVL7-0 bits control both Lch and Rch attenuation levels. When the DVOLC bit = "0", the DVL7-0 bits control Lch level and DVR7-0 bits control Rch level. This volume has a soft transition function. The DVTM bit sets the transition time between set values of DVL/R7-0 bits as either 1061/fs or 256/fs (Table 33). When DVTM bit = "0", a soft transition between the set values occurs (1062 levels). It takes 1061/fs (=24ms@fs=44.1kHz) from 00H (+12dB) to FFH (MUTE).

DVL/R7-0	Gain	
00H	+12.0dB	
01H	+11.5dB	
02H	+11.0dB	
:	:	
18H	0dB	(default)
:	:	
FDH	–114.5dB	
FEH	–115.0dB	
FFH	MUTE (–∞)	

Table 32. Digital Volume Code Table

DVTM bit	Transition time between DVL/R7-0 bits = 00H and FFH			
	Setting	fs=8kHz	fs=44.1kHz	
0	1061/fs	133ms	24ms	(default)
1	256/fs	32ms	6ms	

Table 33. Transition Time Setting of Digital Output Volume

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit changed to “1”, the output signal is attenuated by –∞ (“0”) during the cycle set by the DVTM bit. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the value set by the DVL/R7-0 bits during the cycle set of the DVTM bit. If the soft mute is cancelled within the cycle set by the DVTM bit after starting the operation, the attenuation is discontinued and returned to the value set by the DVL/R7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transmission (Figure 49).

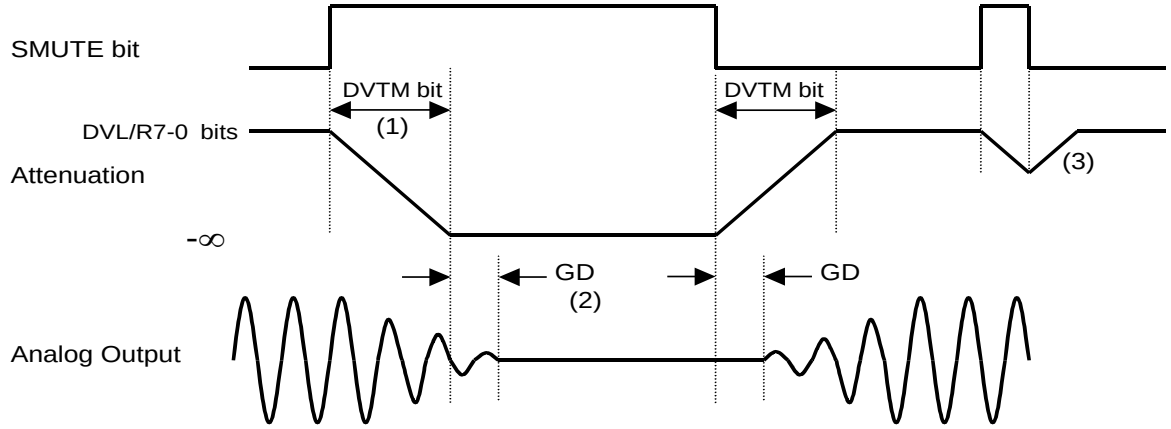


Figure 49. Soft Mute Function

(1) The output signal is attenuated until –∞ (“0”) by the cycle set by the DVTM bit.
(2) Analog output corresponding to digital input has group delay (GD).
(3) If the soft mute is cancelled within the cycle set by the DVTM bit, the attenuation is discounted and returned to the value set by the DVL/R7-0 bits.

■ Analog Mixing: Monaural input

When PMMIN bit is set to "1", the mono input is powered-up. When MINH/S bits are set to "1", the input signal from the MIN+/MIN- pin is output to HP-Amp/Speaker-Amp. The external resisters Ri adjust the signal gain of MIN+/MIN- input. If the Analog Mixing block will use as a single-ended, the MIN- pin should be connected to VSS1 in series with capacitor to avoid induced external noise.(Figure 51)
When the headphone output type is Differential (HPBTL bit = "1"), HVDD should be the same as the voltage of AVDD to use the path from MIN to HP-Amp(MINH bit = "1").

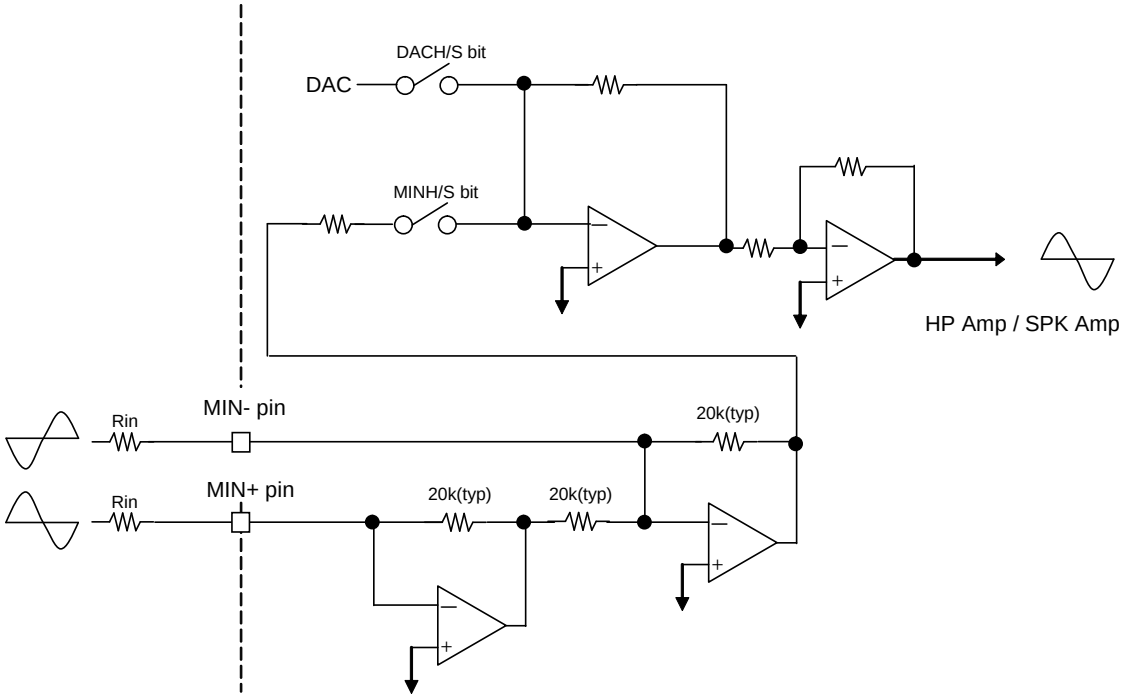


Figure 50. Block Diagram of Monaural input (Differential Input)

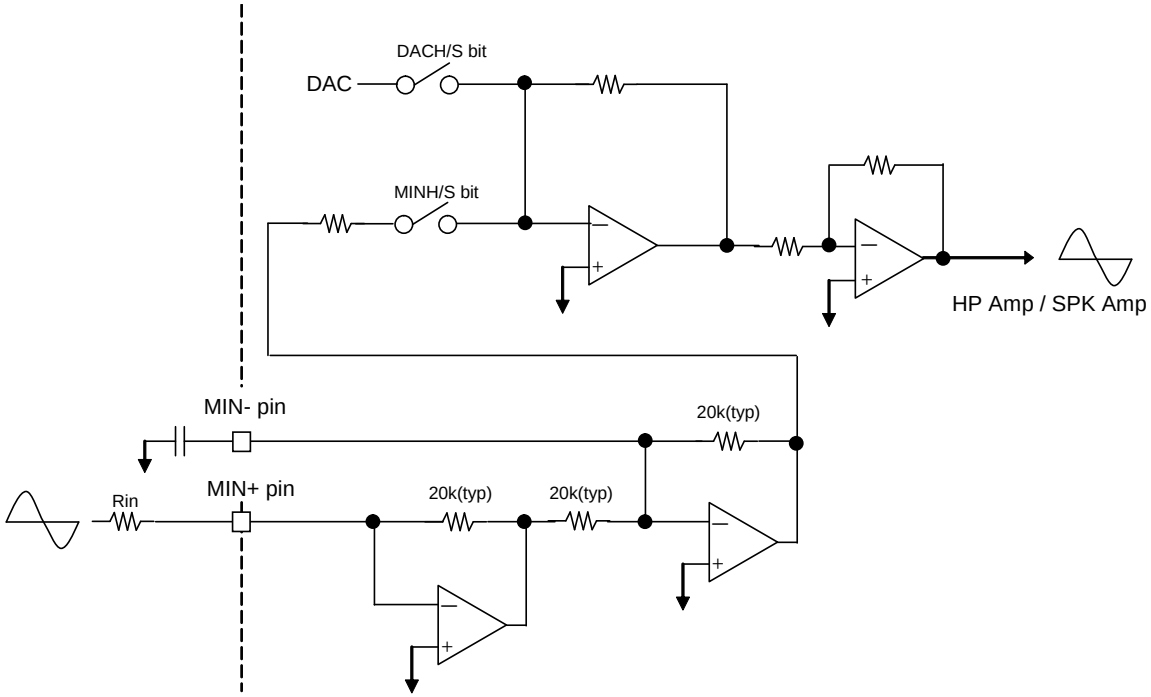


Figure 51. Block Diagram of Monaural input (Single Input)

■ Analog Output Control

HPBTL and PSEUDO bits select the output type, Single-ended, Differential or Pseudo cap-less (Table 34). Available pins and bits are changed at each output type.

HPBTL bit	PSEUDO bit	Headphone Output Type	Figure	Table
0	0	Single-ended (default)	Figure 1	Table 35
1	0	Differential	Figure 2	Table 36
0	1	Pseudo cap-less	Figure 3	Table 37
1	1	N/A		

Table 34. Headphone Output Type Select (N/A: Not Available)

Pin / Control	Available pin / bit	
Pin	**HPL/R, LOUT/ROUT**	**SPP/SPN**
Power management	PMHPL/R	PMSPK(SPPSN)
Switch Control from MIN to HP-Amp	MINH	MINS
Switch Control from DAC to HP-Amp	DACH	DACS
Gain Control	HPG	SPKG[1:0]

Table 35. Available pin / bit (Single-ended, HPBTL bit = PSEUDO bit = “0”)

Pin / Control	Available pin / bit	
Pin	**HPL+/-**	**HPR +/-**
Power management	PMHPL	PMHPR
Switch Control from MIN to HP-Amp	MINH	MINH
Switch Control from DAC to HP-Amp	DACH	DACH
Gain Control	HPG	HPG

Table 36. Available pin / bit (Differential, HPBTL bit = “1”, PSEUDO bit = “0”)

Pin / Control	Available pin / bit	
Pin	**HPL/R**	**HVCM**
Power management	PMHPL/R	PMHPL or PMHPR
Switch Control from MIN to HP-Amp	MINH	-
Switch Control from DAC to HP-Amp	DACH	-
Gain Control	HPG	-

Table 37. Available pin / bit (Pseudo cap-less, HPBTL bit = “0”, PSEUDO bit = “1”)

■ Stereo Line Output (LOUT/ROUT pins)

The common voltage is 0.5 x HVDD when VBAT bit = "0" (Table 40). The load resistance is 10kΩ (min).

Stereo line out amplifier is shared with Headphone amplifier (HPBTL bit = PSEUDO bit = "0" in Table 38). When PMHPL/R and HPMTN bits are "1", the stereo line output is powered-up (Figure 52).
Stereo line out amplifier is prohibited from using headphone output at the same time.

■ Headphone Output

The power supply voltage for the Headphone-Amp is supplied from the HVDD pin and the output level is centered on the HVDD/2 when VBAT bit = "0". If HVDD voltage becomes lower, the output signal might be distorted while the amplitude is maintained. The load resistance is 16Ω (min). HPBTL and PSEUDO bits select the output type, Single-ended or Differential or Pseudo cap-less. When the HPBTL bit is "1", HPL/HPR/SPP/SPN pins become HPL+/HPL-/HPR+/HPR- pins, respectively. When the PSEUDO bit is "1", the SPN pin become the HVCM pin. HPG bit selects the output voltage (Table 38).

HPBTL	PSEUDO	HPG	Output Type	Output pins	Output Voltage [Vpp]
0	0	0	Single-ended	HPL, HPR	0.6 x AVDD
0	0	1	Single-ended	HPL, HPR	0.91 x AVDD
1	0	0	Differential	HPL+/-, HPR+/-	1.2 x AVDD
1	0	1	Differential	HPL+/-, HPR+/-	1.82 x AVDD
0	1	0	Pseudo cap-less	HPL, HPR, HVCM	0.6 x AVDD
0	1	1	Pseudo cap-less	HPL, HPR, HVCM	0.91 x AVDD
1	1	x	N/A		

Table 38. Headphone-Amp Output Type and Output Voltage (x: Don't care, N/A: Not available)

When the HPMTN bit is "0", the common voltage of Headphone-Amp falls and the outputs (HPL/R and HPL+/- and HPR+/- and HVCM pins) go to "L" (VSS2). When the HPMTN bit is "1", the common voltage rises to HVDD/2 at VBAT bit = "0". A capacitor between the MUTET pin and ground reduces pop noise at power-up. Rise/Fall time constant is in proportional to HVDD voltage and the capacitor at MUTET pin.

[Example]: A capacitor between the MUTET pin and ground = 1.0μF±30%, HVDD=3.6V:
Rising time (0.8 x HVDD/2): 150ms(typ), 260ms(max) at HPMTN bit = "0" → "1"
Time until the common voltage goes to VSS2: 140ms(typ), 260ms(max) at HPMTN bit = "1" → "0"

When PMHPL and PMHPR bits are "0", the Headphone-Amp is powered-down, and the outputs (HPL and HPR pins) go to "L" (VSS2).

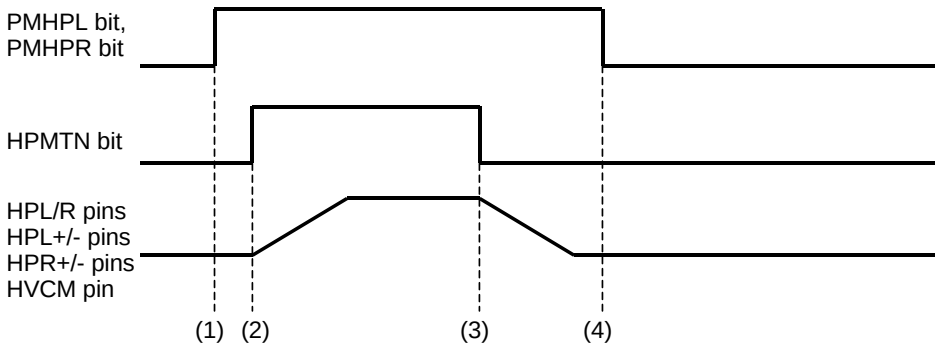


Figure 52. Power-up/Power-down Timing for Headphone-Amp

(1) Headphone-Amp power-up (PMHPL, PMHPR bit = "1"). The outputs are still VSS2.
(2) Headphone-Amp common voltage rises up (HPMTN bit = "1"). Common voltage of Headphone-Amp is rising.
(3) Headphone-Amp common voltage falls down (HPMTN bit = "0"). Common voltage of Headphone-Amp is falling.
(4) Headphone-Amp power-down (PMHPL, PMHPR bit = "0"). The outputs are VSS2. If the power supply is switched off or Headphone-Amp is powered-down before the common voltage changes to VSS2, POP noise occurs.

<External Circuit of Headphone-Amp>

1) Single-ended Output (HPBTL bit = "0", PSEUDO bit = "0")

The cut-off frequency (fc) of Headphone-Amp depends on an external resistor and a capacitor. Table 39 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at HVDD = 2.7, 3.3 and 3.8V. The output voltage of headphone is 0.6 x AVDD (Vpp).

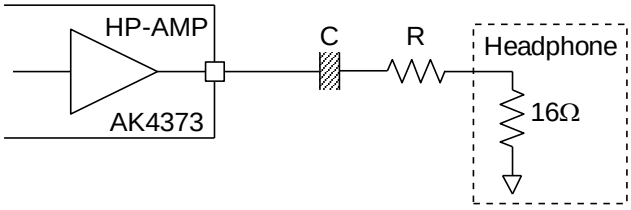


Figure 53. External Circuit Example of Headphone (Single-ended output)

HPG bit	R [Ω]	C [μF]	fc [Hz]	Output Power [mW]@0dBFS(Note 43)		
				HVDD=2.7V AVDD=2.7V	HVDD=3.3V AVDD=3.3V	HVDD=3.8V AVDD=3.3V
0	0	220	45	20	30	30
		100	100			
	6.8	100	70	10	15	15
		47	149			
	16	100	50	5.0	7.5	7.5
		47	106			
1	0	220	45	44 (Note 44)	67 (Note 44)	70
		100	100			
	100	22	62	0.9	1.3	1.3
		10	137			

Table 39. External Circuit Example (Single-ended output)

Note 43. Output power at 16Ω load.
Note 44. Output signal is clipped.

2) Differential Output (HPBTL bit = “1” PSEUDO bit = “0”)

For differential output, no external AC coupling capacitor is required.
Power management (power up/down control) of L/Rch is controlled by setting PMHPL/PMHPR bits respectively. The common voltage control of Headphone-Amp is controlled by setting HTMTN bit. The common voltage is shown in Table 40. HPBTL bit should be changed when both speaker and headphone amps are powered-down.

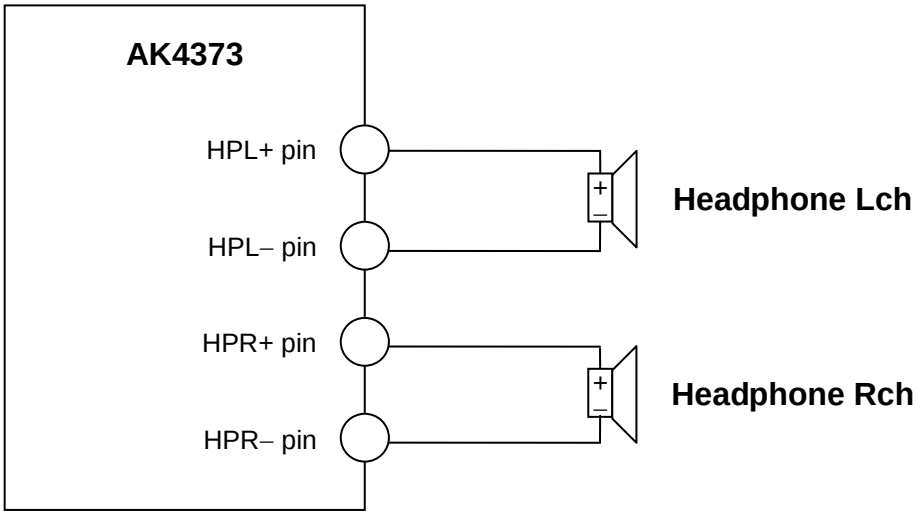


Figure 54. External Circuit Example of Headphone (Differential output)

3) Pseudo cap-less Output (HPBTL bit = “0”, PSEUDO bit =”1”)

In case of pseudo cap less, no external AC coupling capacitor is required as well as BTL mode. This pseudo cap less mode is also available for normal 3-pin headphone mini jack while BTL mode requires a closed system with 4-wire connection. Power management (power up/down control) of VCOM Amp for HP-Amp is controlled by setting PMHPL bit or PMHPR bit. The common voltage control of Headphone-Amp and VCOM-Amp is controlled by setting HTMTN bit. The common voltage is shown in Table 40. PSEUDO bit should be changed when both speaker and headphone amps are powered-down. In this mode, HPBTL and DACS and MINS bits must be “0”.

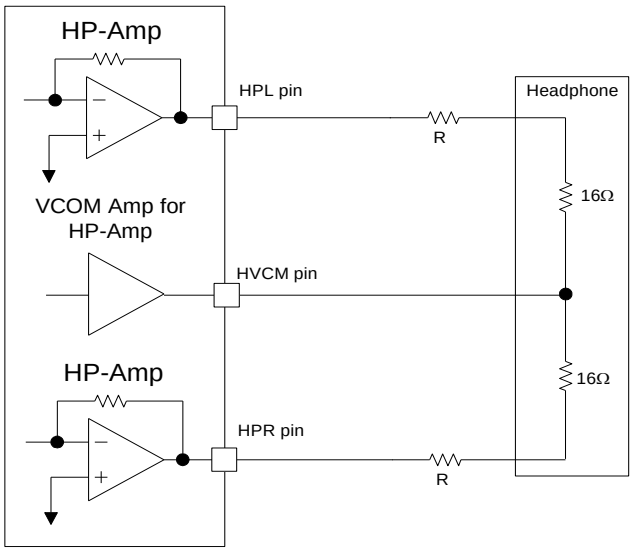


Figure 55. External Circuit Example of Headphone (pseudo cap-less output)

<Headphone-Amp PSRR>

When HVDD is directly supplied from the battery in the mobile phone system, RF noise may influences headphone output performance. When VBAT bit is set to “1”, HP-Amp PSRR for the noise applied to HVDD is improved. In this case, HP-Amp common voltage is 0.64 x AVDD (typ). When AVDD is 3.3V, common voltage is 2.1V. Therefore, when HVDD voltage becomes lower than 4.2V, the output signal will be clipped easily.

VBAT bit	0	1
Common Voltage [V]	0.5 x HVDD	0.64 x AVDD

Table 40. HP-Amp Common Voltage

■ Speaker Output (SPP/SPN pins)

Recommended power supply range is 2.6V to 4.0V. If HVDD voltage becomes low, the output signal might be distorted while the amplitude is maintained. Speaker-Amp is available at HPBTL bit = PSEUDO bit = "0".

Speaker Type	Dynamic Speaker	Piezo (Ceramic) Speaker
Load Resistance (min)	8Ω	50Ω
Load Capacitance (max)	30pF	3μF

Note 21. Load impedance is total impedance of series resistance (Rseries) and piezo speaker impedance at 1kHz in Figure 56. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 20Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Table 41. Speaker Type and Power Supply Range

The DAC signal is input to the Speaker-amp as [(L+R)/2]. The Speaker-amp is mono and BTL output. The gain is set by SPKG1-0 bits. Output level depends on AVDD voltage and SPKG1-0 bits.

SPKG1-0 bits	Gain		
	ALC bit = "0"	ALC bit = "1"	
00	+4.43dB	+6.43dB	(default)
01	+6.43dB	+8.43dB	
10	+10.65dB	+12.65dB	
11	+12.65dB	+14.65dB	

Table 42. SPK-Amp Gain

AVDD	HVDD	SPKG1-0 bits	SPK-Amp Output (DAC Input = 0dBFS)	
			ALC bit = "0"	ALC bit = "1" (LMTH1-0 bits = "00")
3.3V	3.3V	00	3.30Vpp	3.11Vpp
		01	4.15Vpp (Note 45)	3.92Vpp
		10	6.75Vpp (Note 45)	6.37Vpp (Note 45)
		11	8.50Vpp (Note 45)	8.02Vpp (Note 45)
	4.0V	00	3.30Vpp	3.11Vpp
		01	4.15Vpp	3.92Vpp
		10	6.75Vpp (Note 45)	6.37Vpp (Note 45)
		11	8.50Vpp (Note 45)	8.02Vpp (Note 45)

Note 45. The output level is calculated by assuming that output signal is not clipped. In actual case, output signal may be clipped when DAC outputs 0dBFS signal. DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is 4.0Vpp (HVDD=3.3V) or 4.8Vpp (HVDD=4V) or less and output signal is not clipped.

Table 43. SPK-Amp Output Level

<ALC Operation Example of Speaker Playback>

Register Name	Comment	fs=44.1kHz	
		Data	Operation
LMTH1-0	Limiter detection Level	00	–2.5dBFS
ZELMN	Limiter zero crossing detection	0	Enable
ZTM1-0	Zero crossing timeout period	10	11.6ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same or longer data as ZTM1-0 bits	011	23.2ms
REF7-0	Maximum gain at recovery operation	C1H	+18dB
AVL7-0, AVR7-0	Gain of AVOL	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step
ALC	ALC enable	1	Enable

Table 44. ALC Operation Example of Speaker Playback

<Caution for using Piezo Speaker>

When a piezo speaker is used, two resistances more than 20Ω should be connected between SPP/SPN pins and speaker in series, respectively, as shown in Figure 56. Zener diodes should be inserted between speaker and GND as shown in Figure 56, in order to protect SPK-Amp of the AK4373 from the power that the piezo speaker outputs when the speaker is pressured. Zener diodes of the following zener voltage should be used.

0.92 x HVDD ≤ Zener voltage of zener diodo (ZD in Figure 56) ≤ HVDD+0.3V
Ex) In case of HVDD = 3.8V: 3.5V ≤ ZD ≤ 4.1V
For example, zener diode which zener voltage is 3.9V (Min: 3.7V, Max: 4.1V) can be used.

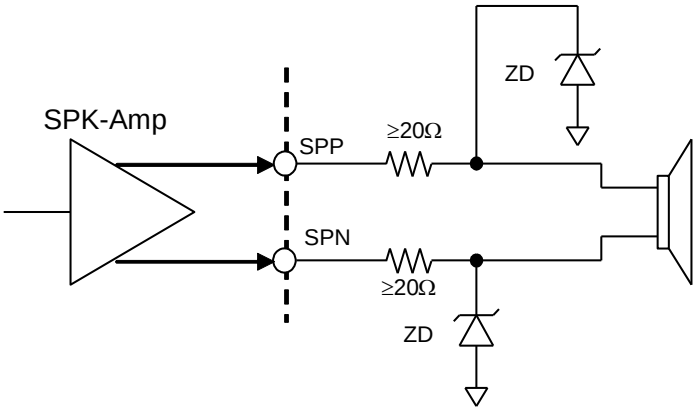


Figure 56. Speaker Output Circuit (Load Capacitance > 30pF)

<Speaker-Amp Control Sequence>

Speaker-Amp is powered-up/down by PMSPK bit. When PMSPK bit is "0", both SPP and SPN pin are in Hi-Z state. When PMSPK bit is "1" and SPPSN bit is "0", the Speaker-Amp enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin changes to HVDD/2 voltage. Power-save mode can reduce pop noise at power-up and power-down.

PMSPK	SPPSN	Mode	SPP	SPN	
0	x	Power-down	VSS2	VSS2	(default)
1	0	Power-save	Hi-Z	HVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 45. Speaker-Amp Mode Setting (x: Don't care)

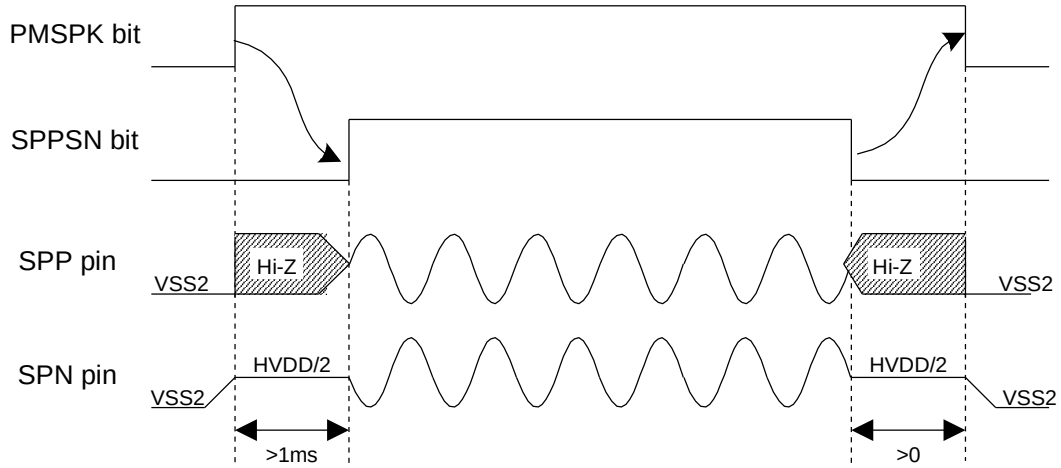
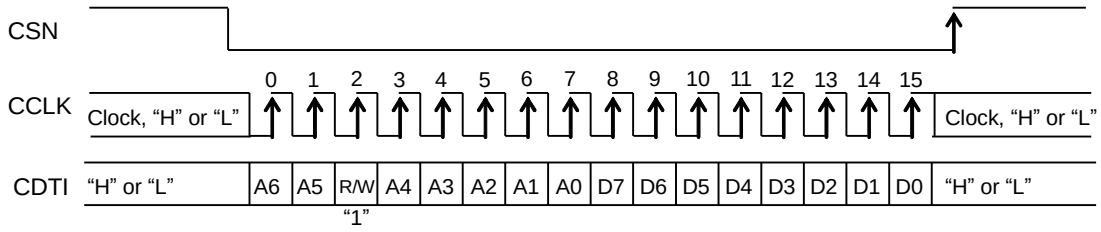


Figure 57. Power-up/Power-down Timing for Speaker-Amp

■ Serial Control Interface

(1) 3-wire Serial Control Mode (I2C pin = "L") Write Only

Internal registers may be written by using the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of Read/Write (Fixed to "1"), Register address (MSB first, 7bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Address and data are latched on the 16th CCLK rising edge ("↑") after CSN falling edge("↓"). Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by PDN pin = "L".



R/W: READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A6-A0: Register Address
D7-D0: Control data

Figure 58. Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4373 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 59 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 65). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 60). If the slave address matches that of the AK4373, the AK4373 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 66). R/W bit value of "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4373. The format is MSB first, and those most significant bit is fixed to zeros (Figure 61). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 62). The AK4373 generates an acknowledge after each byte is received. A data transfer is always terminated by STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 65).

The AK4373 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4373 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 4FH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 67) except for the START and STOP conditions.

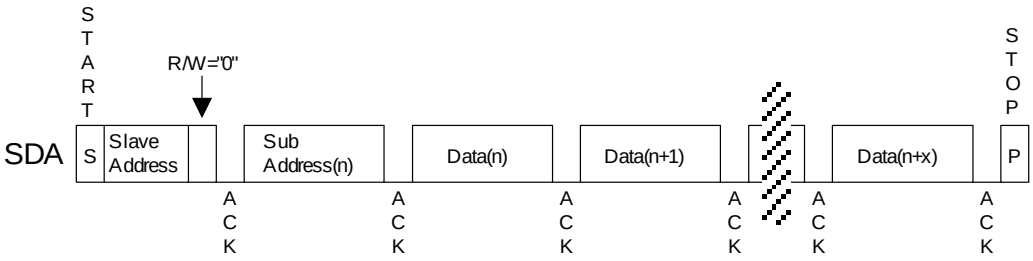


Figure 59. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	1	CAD0	R/W

(CAD0 must match with the CAD0 pin)

Figure 60. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 61. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 62. Byte Structure after The Second Byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4373. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 4FH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4373 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4373 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4373 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates stop condition instead, the AK4373 ceases transmission.

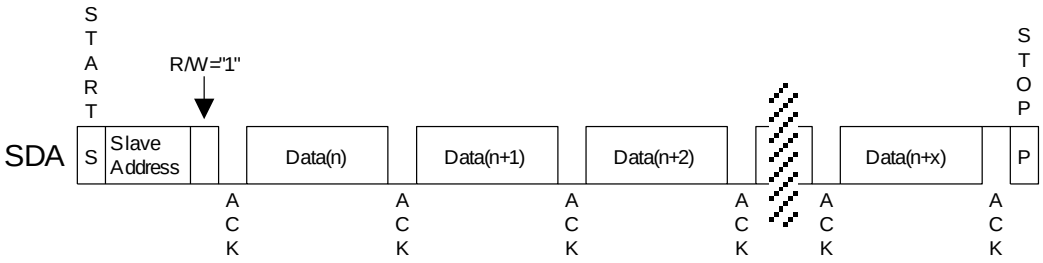


Figure 63. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4373 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates stop condition instead, the AK4373 ceases transmission.

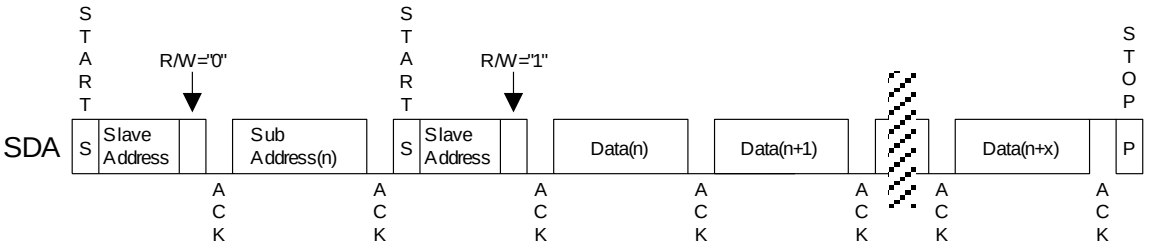


Figure 64. RANDOM ADDRESS READ

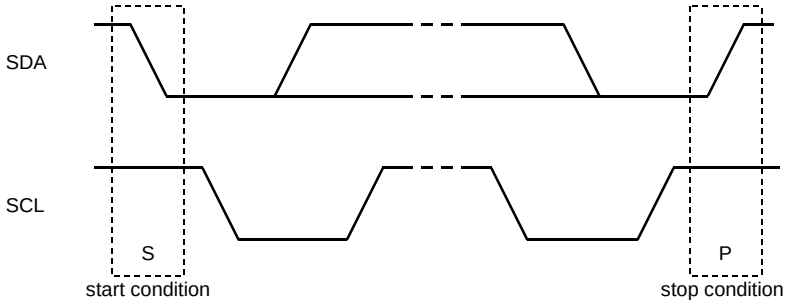


Figure 65. START and STOP Conditions

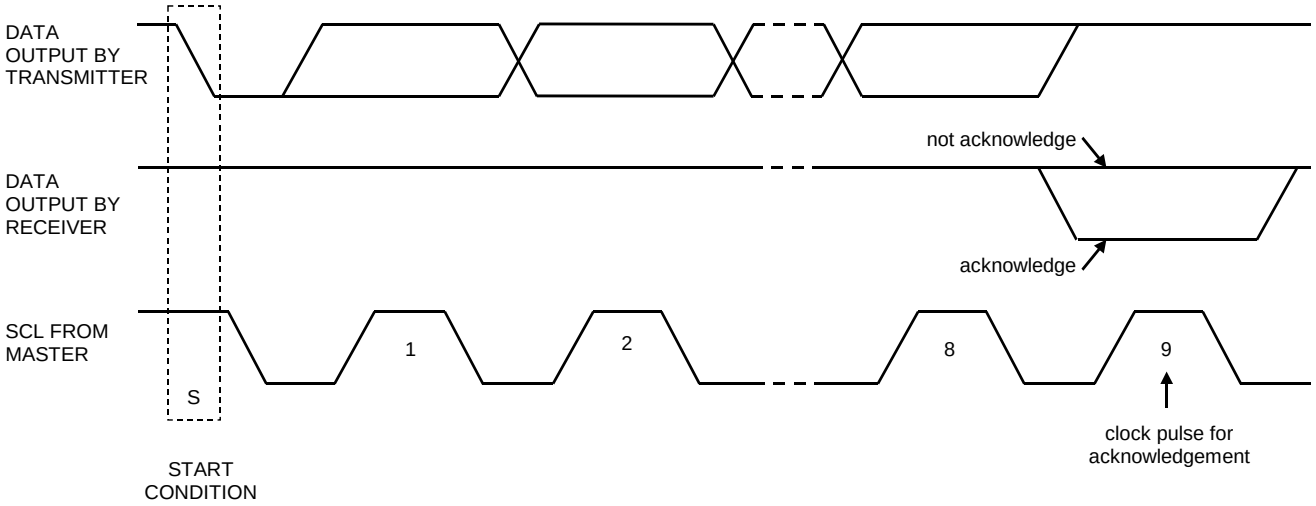


Figure 66. Acknowledge on the I^2C-Bus

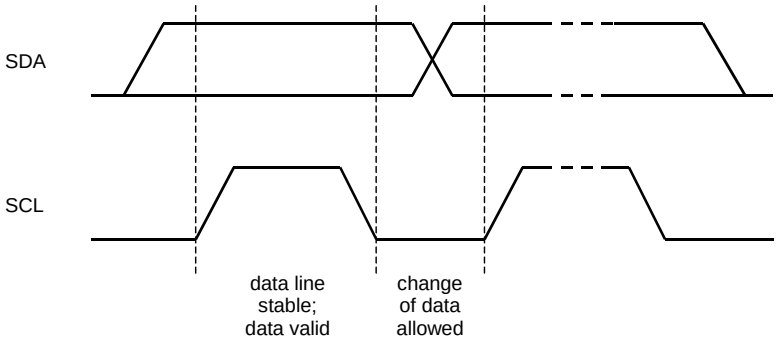


Figure 67. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMMIN	PMSPK	0	PMDAC	0	0
01H	Power Management 2	0	HPMTN	PMHPL	PMHPR	M/S	MCKAC	MCKO	PMPLL
02H	Signal Select 1	SPPSN	MINS	DACS	0	HPBTL	0	PSEUDO	0
03H	Signal Select 2	0	0	0	SPKG1	SPKG0	0	0	0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	DIF2	DIF1	DIF0
05H	Mode Control 2	PS1	PS0	FS3	MSBS	BCKP	FS2	FS1	FS0
06H	Timer Select	DVTM	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
07H	ALC Mode Control 1	0	0	ALC	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
08H	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
09H	Lch Input Volume Control	AVL7	AVL6	AVL5	AVL4	AVL3	AVL2	AVL1	AVL0
0AH	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	0	0	0	FRN	VBAT	0
0CH	Rch Input Volume Control	AVR7	AVR6	AVR5	AVR4	AVR3	AVR2	AVR1	AVR0
0DH	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
0EH	Mode Control 3	0	0	SMUTE	DVOLC	0	0	DEM1	DEM0
0FH	Mode Control 4	0	0	0	0	AVOLC	HPM	MINH	DACH
10H	Power Management 3	0	0	HPG	0	0	0	0	0
11H	Digital Filter Select 1	GN1	GN0	LPF	HPF	EQ	FIL3	0	PFSEL
12H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
13H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
14H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
15H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
16H	EQ Co-efficient 0	EQA7	EQA6	EQA5	EQA4	EQA3	EQA2	EQA1	EQA0
17H	EQ Co-efficient 1	EQA15	EQA14	EQA13	EQA12	EQA11	EQA10	EQA9	EQA8
18H	EQ Co-efficient 2	EQB7	EQB6	EQB5	EQB4	EQB3	EQB2	EQB1	EQB0
19H	EQ Co-efficient 3	0	0	EQB13	EQB12	EQB11	EQB10	EQB9	EQB8
1AH	EQ Co-efficient 4	EQC7	EQC6	EQC5	EQC4	EQC3	EQC2	EQC1	EQC0
1BH	EQ Co-efficient 5	EQC15	EQC14	EQC13	EQC12	EQC11	EQC10	EQC9	EQC8
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
20H	Reserved	0	0	0	0	0	0	0	0
21H	Reserved	0	0	0	0	0	0	0	0
22H	Reserved	0	0	0	0	0	0	0	0
23H	Reserved	0	0	0	0	0	0	0	0
24H	Reserved	0	0	0	0	0	0	0	0
25H	Reserved	0	0	0	0	0	0	0	0
26H	Reserved	0	0	0	0	0	0	0	0
27H	Reserved	0	0	0	0	0	0	0	0
28H	Reserved	0	0	0	0	0	0	0	0
29H	Reserved	0	0	0	0	0	0	0	0
2AH	Reserved	0	0	0	0	0	0	0	0
2BH	Reserved	0	0	0	0	0	0	0	0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

Note 46. PDN pin = “L” resets the registers to their default values.

Note 47. Unused bits indicated “0” must contain a “0” value.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMMIN	PMSPK	0	PMDAC	0	0
Default		0	0	0	0	0	0	0	0

PMDAC: DAC Power Management
0: Power-down (default)
1: Power-up

PMSPK: Speaker-Amp Power Management
0: Power-down (default)
1: Power-up

PMMIN: MIN Input Power Management
0: Power-down (default)
1: Power-up
The PMMIN bit must be set to "1" at the same time when the PMHPL bit, PMHPR bit or PMSPK bit is set to "1".

PMVCM: VCOM Power Management
0: Power-down (default)
1: Power-up
When any blocks are powered-up, the PMVCM bit must be set to "1". The PMVCM bit can be set to "0" only when all power management bits of 00H, 01H and MCKO bits are "0".

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless of the setting of this address. In this case, register is initialized to the default value.

When all power management bits are "0" in the 00H, 01H addresses and MCKO bit is "0", all blocks are powered-down. The register values remain unchanged. The register values remain unchanged. Power supply current is 20μA(typ) in this case. For fully shut down (typ. 1μA), PDN pin must be "L".

When DAC is not used, external clocks may not be present. When DAC is used, external clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	HPMTN	PMHPL	PMHPR	M/S	MCKAC	MCKO	PMPLL
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power-Down (default)
1: PLL Mode and Power-up

MCKO: Master Clock Output Enable on all clock mode (PLL Master/Slave Mode1, 2 /EXT Master, Slave Mode)
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

MCKAC: MCKI Input Mode Select
0: CMOS input (default)
1: AC coupling input

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

PMHPR: Headphone-Amp Rch Power Management
0: Power-down (default)
1: Power-up

PMHPL: Headphone-Amp Lch Power Management
0: Power-down (default)
1: Power-up

HPMTN: Headphone-Amp Mute Control
0: Mute (default)
1: Normal operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SPPSN	MINS	DACS	0	HPBTL	0	PSEUDO	0
Default		0	0	0	0	0	0	0	0

PSEUDO, HPBTL: Headphone Output Type Select

HPBTL bit	PSEUDO bit	Headphone Output Type	Figure	Table
0	0	Single-ended (default)	Figure 1	Table 35
1	0	Differential	Figure 2	Table 36
0	1	Pseudo cap-less	Figure 3	Table 37
1	1	N/A		

Table 46. Headphone Output Type Select (N/A: Not Available)

DACS: Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

MINS: Switch Control from MIN to Speaker-Amp
0: OFF (default)
1: ON
When MINS bit is "1", monaural signal is input to Speaker-Amp.

SPPSN: Speaker-Amp Power-Save Mode
0: Power-Save Mode (default)
1: Normal Operation
When SPPSN bit is "0", Speaker-Amp is in power-save mode. In this mode, the SPP pin goes to Hi-Z and the SPN pin is outputs HVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	0	0	0	SPKG1	SPKG0	0	0	0
Default		0	0	0	0	0	0	0	0

SPKG1-0: Speaker-Amp Output Gain Select (Table 42)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	DIF2	DIF1	DIF0
Default		0	0	0	0	0	0	1	0

DIF2-0: Audio Interface Format (Table 17)
Default: "010" (Left justified)

BCKO: BICK Output Frequency Select at Master Mode (Table 11)

PLL3-0: PLL Reference Clock Select (Table 5)
Default: "0000" (LRCK pin)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 2	PS1	PS0	FS3	MSBS	BCKP	FS2	FS1	FS0
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency Select (Table 6 and Table 7) and MCKI Frequency Select (Table 12)
FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

BCKP: BICK Polarity at DSP Mode (Table 18)
"0": SDTO is output by the rising edge ("↑") of BICK and SDTI is latched by the falling edge ("↓"). (default)
"1": SDTO is output by the falling edge ("↓") of BICK and SDTI is latched by the rising edge ("↑").

MSBS: LRCK Polarity at DSP Mode (Table 18)
"0": The rising edge ("↑") of LRCK is half clock of BICK before the channel change. (default)
"1": The rising edge ("↑") of LRCK is one clock of BICK before the channel change.

PS1-0: MCKO Output Frequency Select (Table 10)
Default: "00" (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Timer Select	DVTM	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
Default		0	0	0	0	0	0	0	0

RFST1-0: ALC First recovery Speed (Table 28)
Default: "00"(4times)

WTM2-0: ALC Recovery Waiting Period (Table 25)
Default: "000" (128/fs)

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (Table 24)
Default: "00" (128/fs)

DVTM: Digital Volume Transition Time Setting (Table 33)
0: 1061/fs (default)
1: 256/fs
This is the transition time between DVL/R7-0 bits = 00H and FFH.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	ALC Mode Control 1	0	0	ALC	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 22)
Default: "00"
LMTH1 bit is D6 bit of 0BH.

RGAIN1-0: ALC Recovery GAIN Step (Table 26)
Default: "00"
RGAIN1 bit is D7 bit of 0BH.

LMAT1-0: ALC Limiter ATT Step (Table 23.)
Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
0: Enable (default)
1: Disable

ALC: ALC Enable
0: ALC Disable (default)
1: ALC Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
Default		1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 27)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Lch Input Volume Control	AVL7	AVL6	AVL5	AVL4	AVL3	AVL2	AVL1	AVL0
0CH	Rch Input Volume Control	AVR7	AVR6	AVR5	AVR4	AVR3	AVR2	AVR1	AVR0
Default		1	1	1	0	0	0	0	1

AVL7-0, AVR7-0: ALC Block Digital Volume; 0.375dB step, 242 Level (Table 30)
Default:"E1H" (+30dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
0DH	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
Default		0	0	0	1	1	0	0	0

DVL7-0, DVR7-0: Output Digital Volume (Table 32)
Default: "18H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	0	0	0	FRN	VBAT	0
Default		0	0	0	0	0	0	0	0

VBAT: HP-Amp Common Voltage (Table 40)
0: 0.5 x HVDD (default)
1: 0.64 x AVDD

FRN: Fast Recovery Enable
0: Enable(default)
1:Disable

LMTH1: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 22)

RGAIN1: ALC Recovery GAIN Step (Table 26)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Mode Control 3	0	0	SMUTE	DVOLC	0	0	DEM1	DEM0
Default		0	0	0	1	0	0	0	1

DEM1-0: De-emphasis Frequency Select (Table 31)
Default: "01" (OFF)

DVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When DVOLC bit = "1", DVL7-0 bits control both Lch and Rch volume level, while register values of DVL7-0 bits are not written to DVR7-0 bits. When DVOLC bit = "0", DVL7-0 bits control Lch level and DVR7-0 bits control Rch level, respectively.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Mode Control 4	0	0	0	0	AVOLC	HPM	MINH	DACH
Default		0	0	0	0	1	0	0	0

DACH: Switch Control from DAC to Headphone-Amp
0: OFF (default)
1: ON

MINH: Switch Control from MIN to HP-Amp
0: OFF (default)
1: ON
When MINH bit is "1", monaural signal is input to HP-Amp.

HPM: Headphone-Amp Mono Output Select
0: Stereo (default)
1: Mono
When the HPM bit = "1", DAC output signal is output to Lch and Rch of the Headphone-Amp as (L+R)/2. HPM bit must be changed when DAC is powered-down.

AVOLC: ALC Block Digital Volume Control Mode Select
0: Independent
1: Dependent (dfault)
When AVOLC bit = "1", AVL7-0 bits control both Lch and Rch volume level, while register values of AVL7-0 bits are not written to AVR7-0 bits. When AVOLC bit = "0", AVL7-0 bits control Lch level and AVR7-0 bits control Rch level, respectively.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Power Management 3	0	0	HPG	0	0	0	0	0
Default		0	0	0	0	0	0	0	0

HPG: Headphone-Amp Gain Select (Table 38)
0: 0dB (default)
1: +3.6dB
HPG bit must be changed when the Headphone-Amp is powered-down.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Digital Filter Select 1	GN1	GN0	LPF	HPF	EQ	FIL3	0	0
Default		0	0	0	0	0	0	0	0

FIL3: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL3 bit is "1", the settings of F3A13-0 and F3B13-0 bits are valid. When FIL3 bit is "0", FIL3 block is through (0dB).

EQ: EQ (Gain Compensation Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ bit is "1", the settings of EQA15-0, EQB13-0 and EQC15-0 bits are valid. When EQ bit is "0", EQ block is through (0dB).

HPF: High pass filter Coefficient Setting Enable
0: Disable (default)
1: Enable
When HPF bit is "1", the settings of F1A13-0 and F1B13-0 bits are valid. When HPF bit is "0", HPF block is through (0dB).

LPF: Low pass filter Coefficient Setting Enable
0: Disable (default)
1: Enable
When LPF bit is “1”, the settings of F2A13-0 and F2B13-0 bits are valid. When LPF bit is “0”, LPF block is through (0dB).

GN1-0: Gain Select at GAIN block (Table 21)
Default: “00”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
13H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
14H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
15H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
16H	EQ Co-efficient 0	EQA7	EQA6	EQA5	EQA4	EQA3	EQA2	EQA1	EQA0
17H	EQ Co-efficient 1	EQA15	EQA14	EQA13	EQA12	EQA11	EQA10	EQA9	EQA8
18H	EQ Co-efficient 2	EQB7	EQB6	EQB5	EQB4	EQB3	EQB2	EQB1	EQB0
19H	EQ Co-efficient 3	0	0	EQB13	EQB12	EQB11	EQB10	EQB9	EQB8
1AH	EQ Co-efficient 4	EQC7	EQC6	EQC5	EQC4	EQC3	EQC2	EQC1	EQC0
1BH	EQ Co-efficient 5	EQC15	EQC14	EQC13	EQC12	EQC11	EQC10	EQC9	EQC8
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: "0000H"

F3AS: FIL3 (Stereo Separation Emphasis Filter) Select
0: HPF (default)
1: LPF

EQA15-0, EQB13-0, EQC15-C0: EQ (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)
Default: "0000H"

F1A13-0, F1B13-0: High pass filer Coefficient (14bit x 2)
Default: "0000H"

F2A13-0, F2B13-0: Low pass filer Coefficient (14bit x 2)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is "1", the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is "0", EQ1 block is through (0dB).

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is "1", the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is "0", EQ2 block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is "1", the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is "0", EQ3 block is through (0dB).

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is "1", the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is "0", EQ4 block is through (0dB).

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is "1", the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is "0", EQ5 block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
default: “0000H”

E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
default: “0000H”

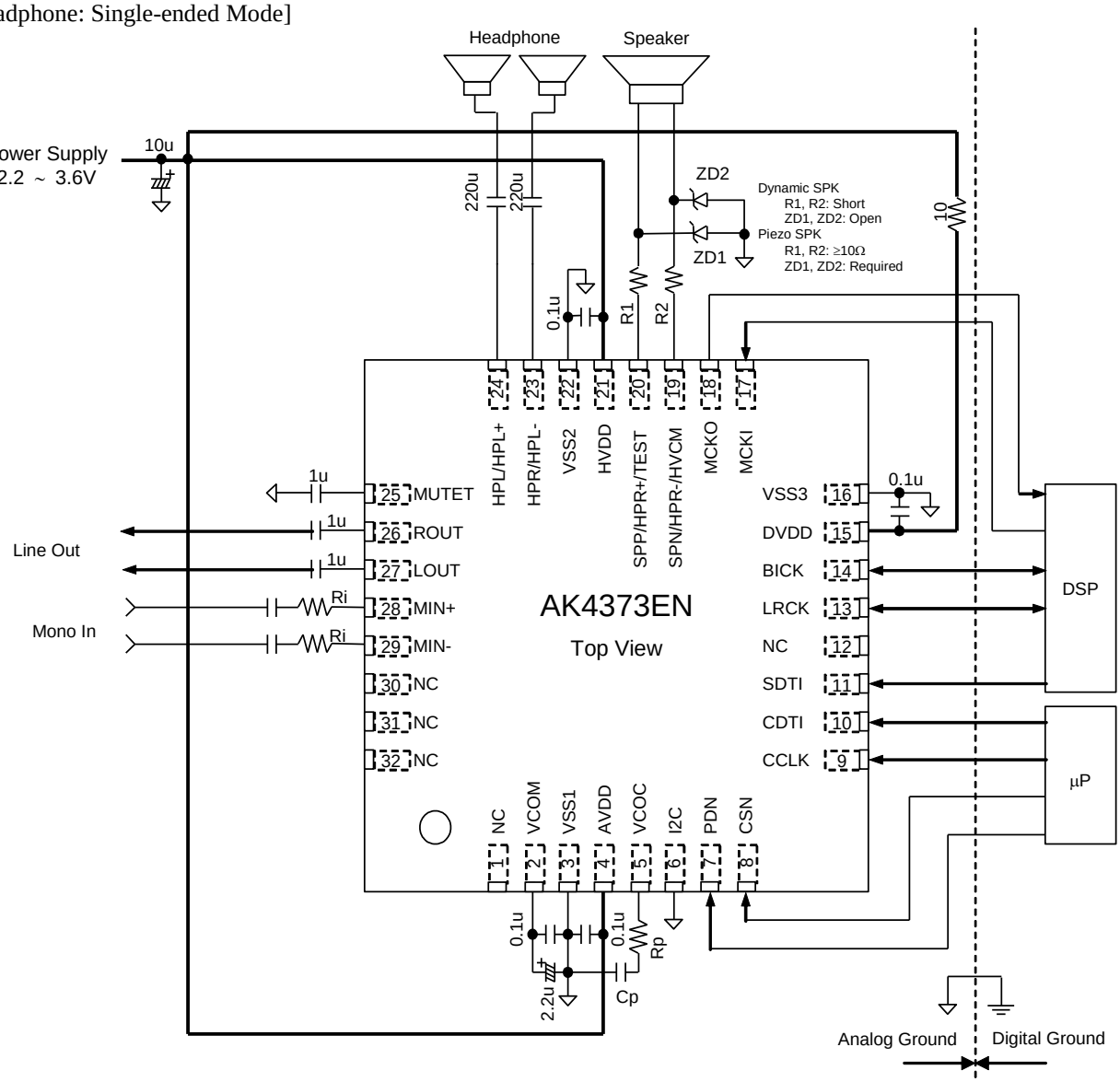
E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
default: “0000H”

SYSTEM DESIGN

Figure 68, Figure 69 and Figure 70 shows the system connection diagram for the AK4373. The evaluation board [AKD4373] demonstrates the optimum layout, power supply arrangements and measurement results.

[Headphone: Single-ended Mode]

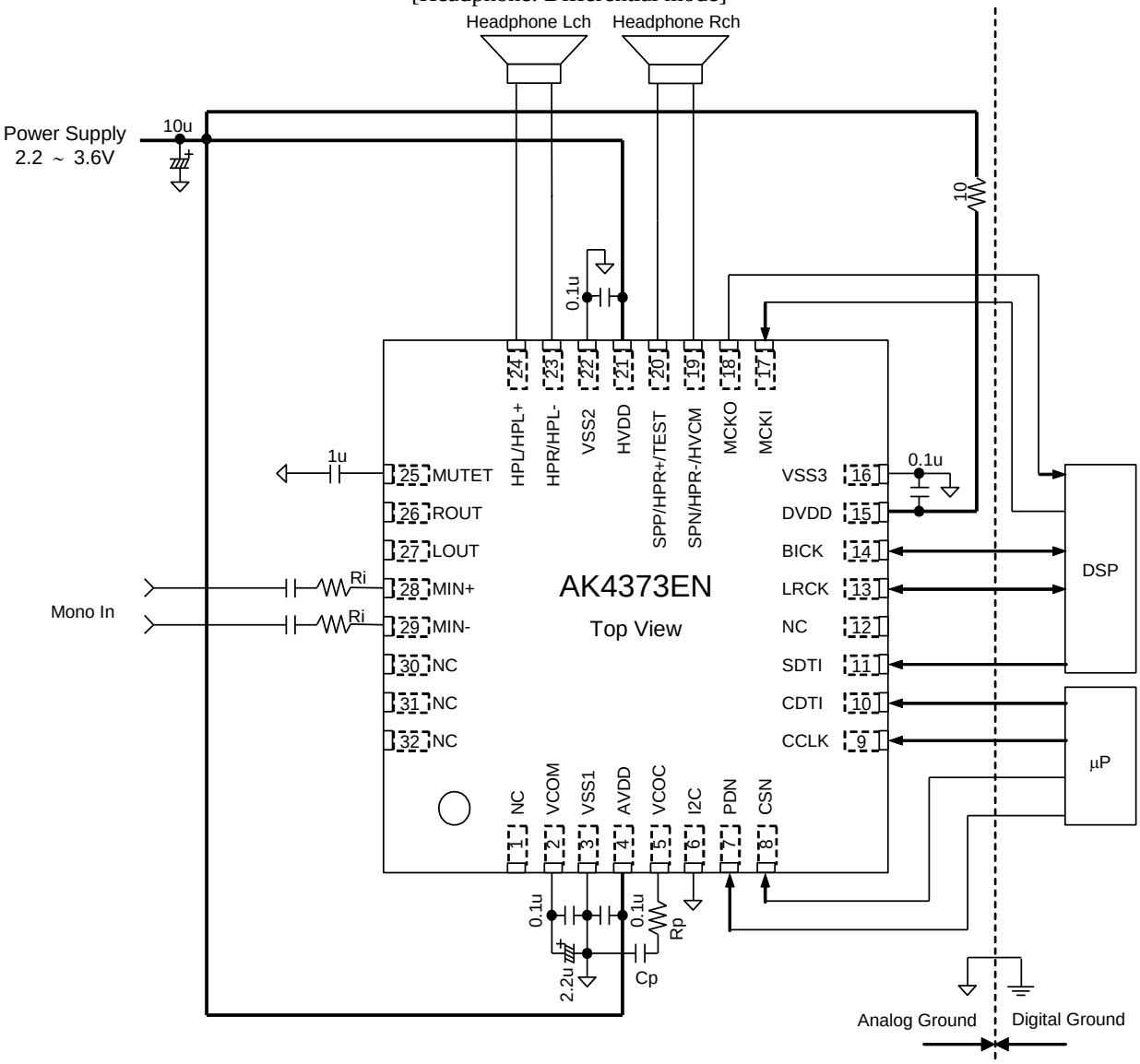


Notes:

- VSS1, VSS2 and VSS3 of the AK4373 must be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK4373 is EXT mode (PMPLL bit = "0"), a resistor and a capacitor of the VCOC pin are not needed.
- When the AK4373 is PLL mode (PMPLL bit = "1"), a resistor and a capacitor of the VCOC pin are shown in Table 5.
- When piezo speaker is used, 2.6 ~ 4.0V power must be supplied to HVDD and 20Ω or more series resistors must be connected to both SPP and SPN pins, respectively.
- When the AK4373 is used at master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor must be connected to LRCK and BICK pins of the AK4373.
- If the Analog Mixing block is used as a single-ended, the MIN- pin must be connected to VSS1 in series with a capacitor to avoid induced external noise.

Figure 68. Typical Connection Diagram (Single-ended mode, HPBTL bit = PSEUDO bit = "0")

[Headphone: Differential mode]

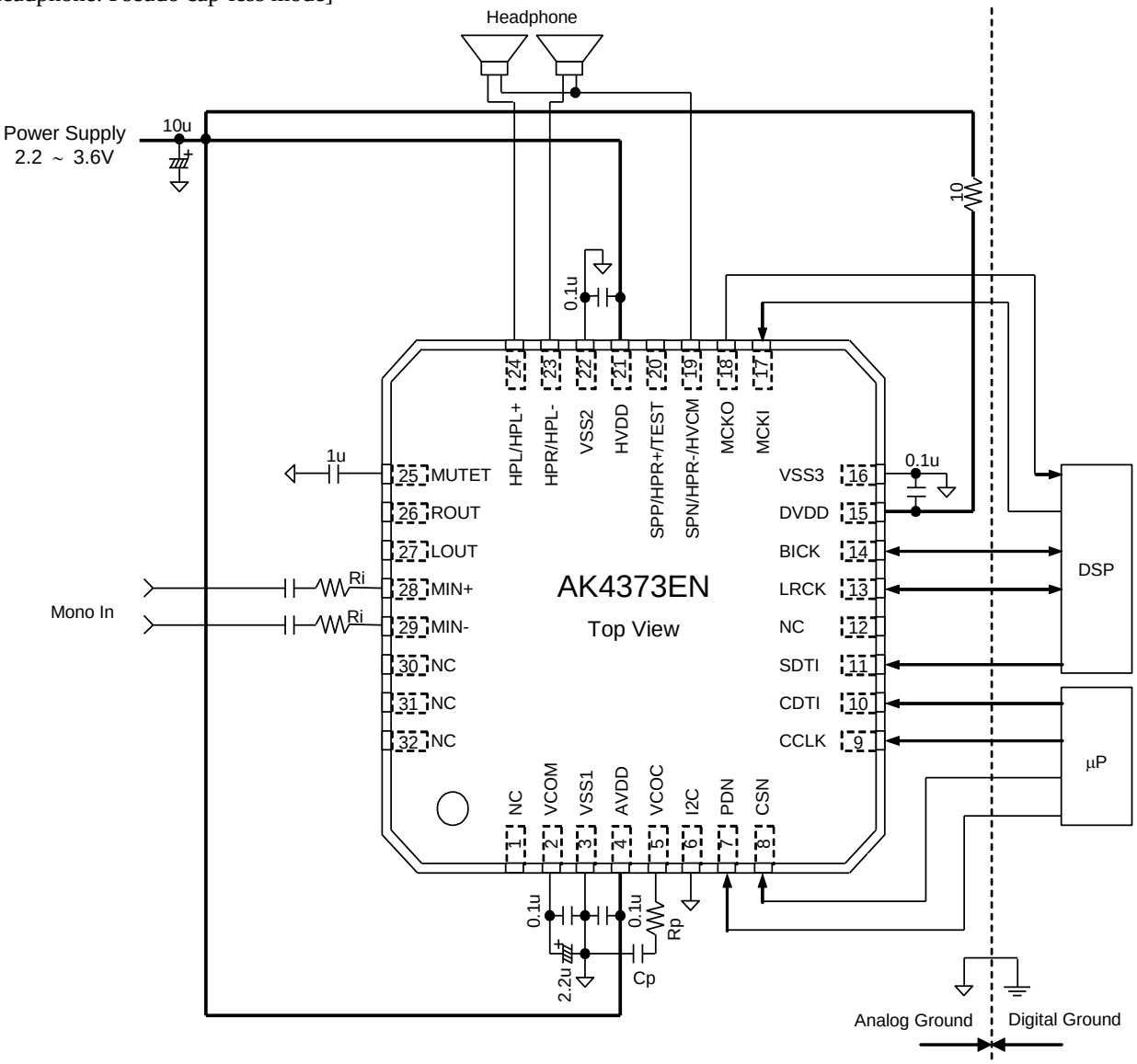


Notes:

- VSS1, VSS2 and VSS3 of the AK4373 must be distributed separately from the ground of external controllers.
- All digital input pins must not be left floating.
- When the AK4373 is EXT mode (PMPLL bit = "0"), a resistor and a capacitor of the VCOC pin are not needed.
- When the AK4373 is PLL mode (PMPLL bit = "1"), a resistor and a capacitor of the VCOC pin are shown in Table 5.
- When the AK4373 is used at master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor must be connected to LRCK and BICK pins of the AK4373.
- If the Analog Mixing block will is used as a single-ended, the MIN- pin must be connected to VSS1 in series with a capacitor to avoid induced external noise.

Figure 69. Typical Connection Diagram (Differential mode, HPBTL bit = "1", PSEUDO bit = "0")

[Headphone: Pseudo cap-less mode]



Notes:

- VSS1, VSS2 and VSS3 of the AK4373 must be distributed separately from the ground of external controllers.
- All digital input pins must not be left floating.
- When the AK4373 is EXT mode (PMPLL bit = "0"), a resistor and a capacitor of the VCOC pin are not needed.
- When the AK4373 is PLL mode (PMPLL bit = "1"), a resistor and a capacitor of the VCOC pin are shown in Table 5.
- When the AK4373 is used at master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor must be connected to LRCK and BICK pins of the AK4373.
- If the Analog Mixing block is used as a single-ended, the MIN- pin must be connected to VSS1 in series with a capacitor to avoid induced external noise.

Figure 70. Typical Connection Diagram (Pseudo cap-less mode, HPBTL bit = "0", PSEUDO bit = "1")

1. Grounding and Power Supply Decoupling

The AK4373 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and HVDD are usually supplied from the system's analog supply. If AVDD, DVDD and HVDD are supplied separately, the power-up sequence is not critical. VSS1, VSS2 and VSS3 of the AK4373 must be connected to the analog ground plane. System analog ground and digital ground must be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors must be as close to the AK4373 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4373.

3. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The Line Output-Amp, Headphone-Amp and Speaker-Amp outputs are centered at HVDD/2 when VBAT bit is "0". (Table 40)

CONTROL SEQUENCE

■ Clock Set up

When DAC is powered-up, the clocks must be supplied.

1. PLL Master Mode.

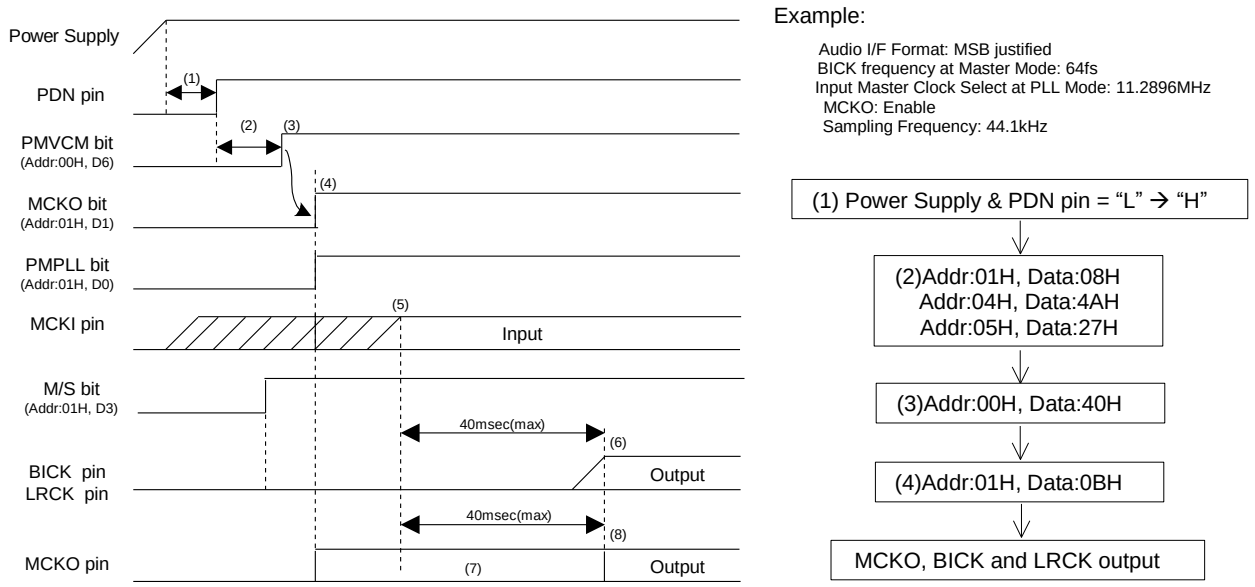


Figure 71. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin = "L" → "H"
"L" time of 150ns or more is needed to reset the AK4373.

(2) DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered-up before the other block operates.

(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(5) PLL lock time is 40ms(max) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.

(6) The AK4373 starts to output the LRCK and the BICK clocks after the PLL becomes stable. Then normal operation starts.

(7) The invalid frequency is output from the MCKO pin during this period if MCKO bit = "1".

(8) The normal clock is output from the MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (LRCK or BICK pin)

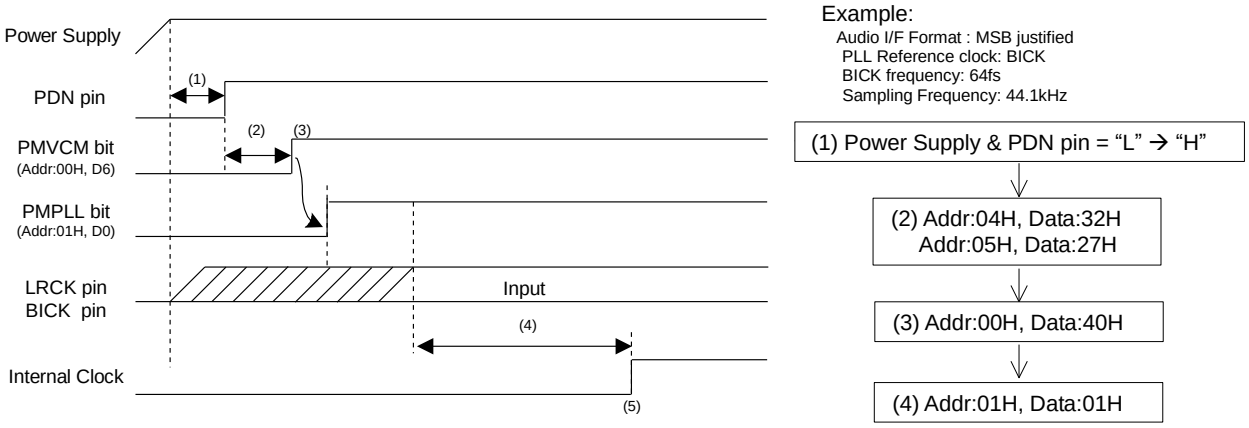


Figure 72. Clock Set Up Sequence (2)

<Example>

(2) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4373.

(3) DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.

(4) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered up before the other block operates.

(5) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (LRCK or BICK pin) is supplied. PLL lock time is 160ms(max) when LRCK is a PLL reference clock. And PLL lock time is 4ms(max) when BICK is a PLL reference clock.

(6) Normal operation stats after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

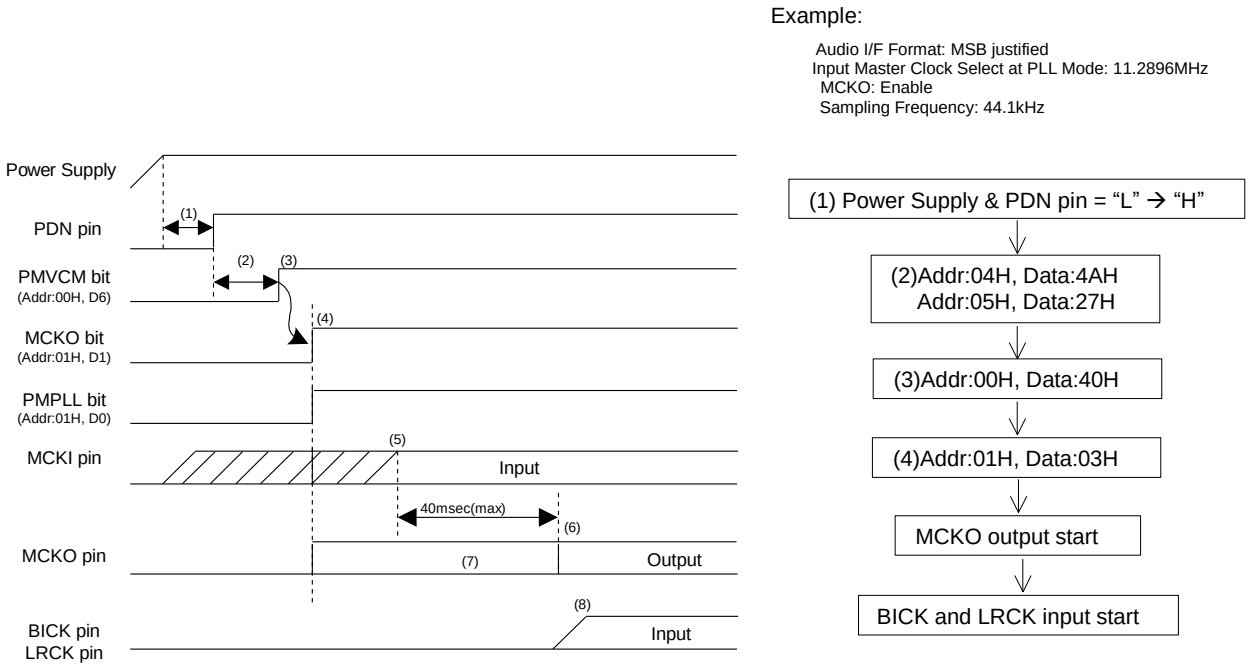


Figure 73. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4373.
(2) DIF1-0, PLL3-0 and FS3-0 bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered up before the other block operates.
(4) Enable MCKO output: MCKO bit = "1"
(5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied. PLL lock time is 40ms(max).
(6) The normal clock is output from MCKO after PLL is locked.
(7) The invalid frequency is output from MCKO during this period.
(8) BICK and LRCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

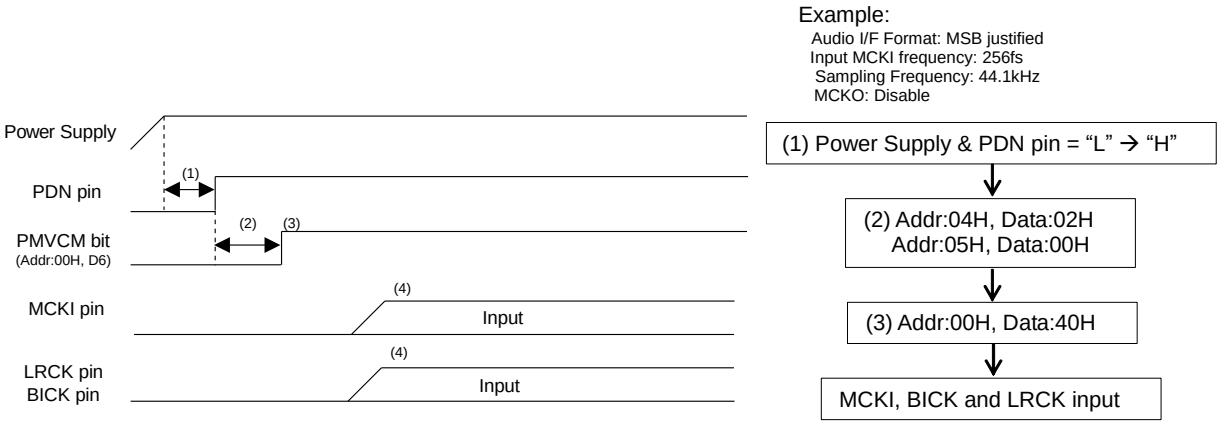


Figure 74. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4373.

(2) DIF1-0 and FS1-0 bits must be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered up before the other block operates.

(4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

5. EXT Master Mode

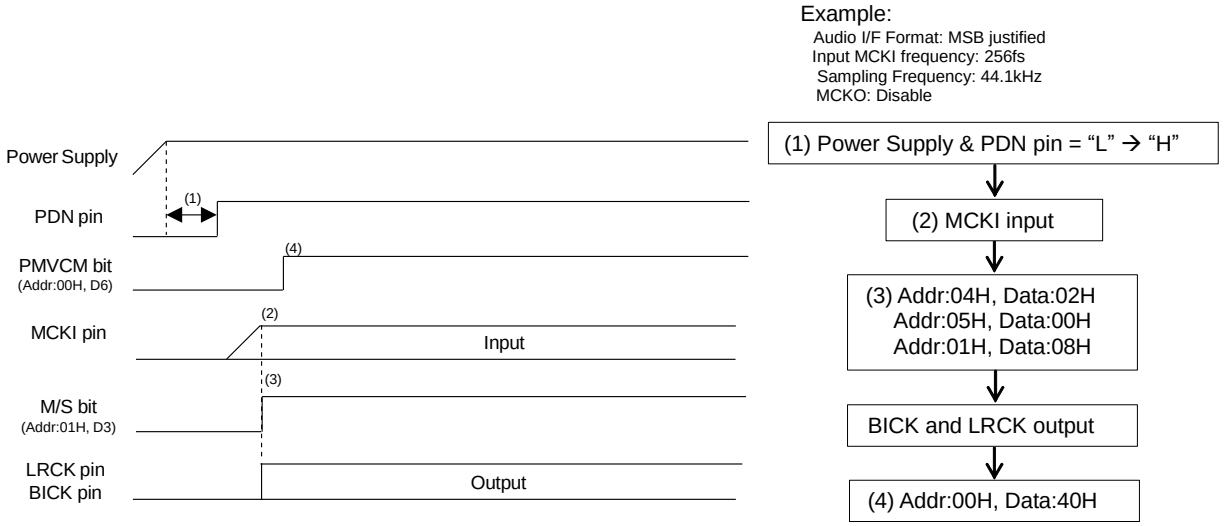


Figure 75. Clock Set Up Sequence (5)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4373.

(2) MCKI must be input.

(3) After DIF1-0 and FS1-0 bits are set, M/S bit should be set to "1". Then LRCK and BICK are output.

(4) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

■ Speaker-amp Output

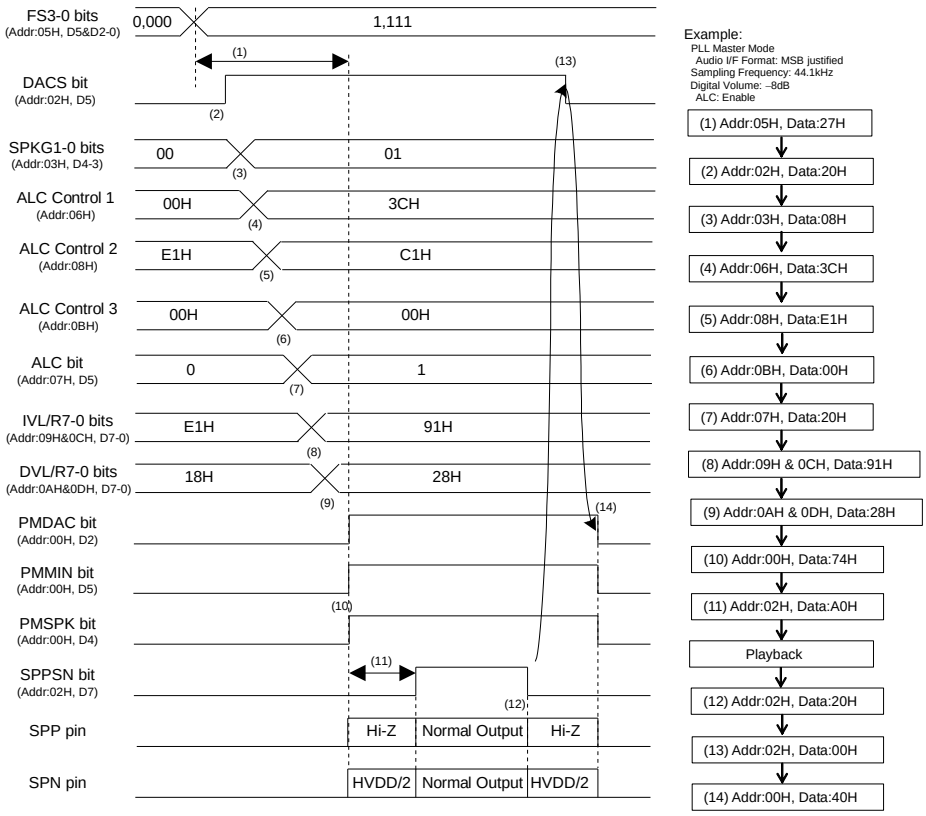


Figure 76. Speaker-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4373 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up the path of "DAC → SPK-Amp": DACS bit = "0" → "1"
(3) SPK-Amp gain setting: SPKG1-0 bits = "00" → "01"
(4) Set up Timer Select for ALC (Addr: 06H)
(5) Set up REF value for ALC (Addr: 08H)
(6) Set up LMTH1 and RGAIN1 bits (Addr: 0BH)
(7) Set up LMTH0, RGAIN0, LMAT1-0 and ALC bits (Addr: 07H)
(8) Set up the ALC Block Digital Volume (Addr: 09H and 0CH)
AVL7-0 and AVR7-0 bits should be set to "91H"(0dB).
(9) Set up the output digital volume (Addr: 0AH and 0DH).
When DVOLC bit is "1" (default), DVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
(10) Power Up of DAC and Speaker-Amp: PMDAC = PMSPK bits = "0" → "1"
When ALC bit is "1", ALC operation starts from the gain set by AVL/R7-0 bits.
(11) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"
(12) Enter the power-save-mode of Speaker-Amp: SPPSN bit = "1" → "0"
(13) Disable the path of "DAC → SPK-Amp": DACS bit = "1" → "0"
(14) Power Down DAC and Speaker-Amp: PMDAC = PMSPK bits = "1" → "0"

■ Headphone-amp Output (Single-Ended or Differential or Pseudo cap-less)

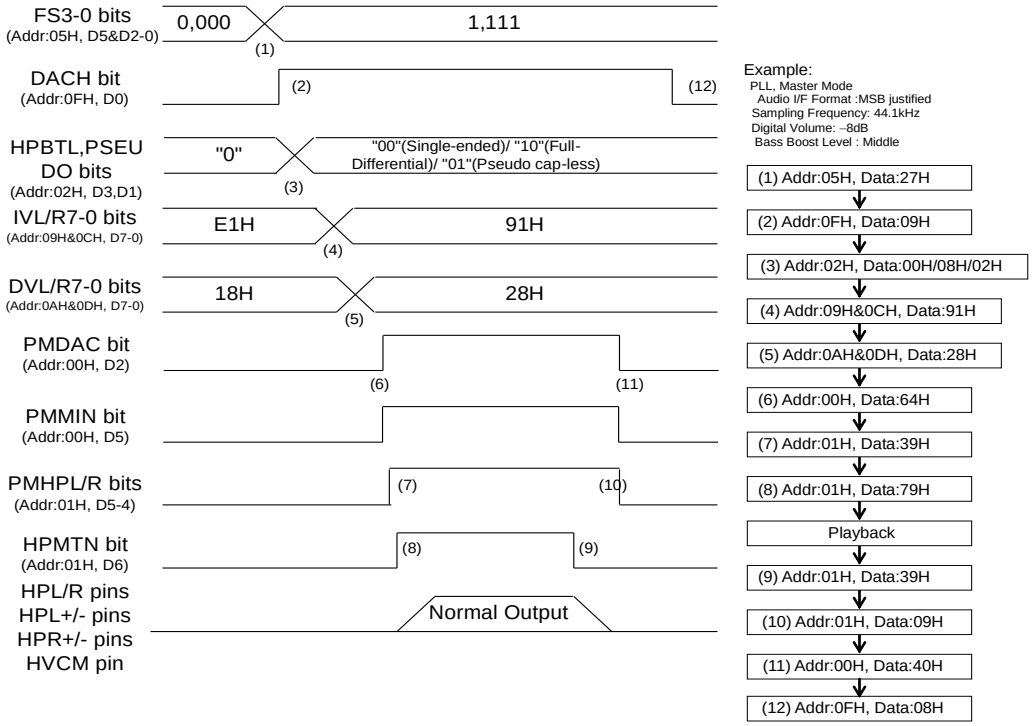


Figure 77. Headphone-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4373 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → HP-Amp": DACH bit = "0" → "1"

(3) Select output type of the headphone (HPBTL and PSEUDO bits "00"= Single-ended, "10"=Differential, "01"=Pseudo cap-less)

(4) Set up the ALC Block Digital Volume (Addr: 09H and 0CH)
AVL7-0 and AVR7-0 bits should be set to "91H"(0dB).

(5) Set up the output digital volume (Addr: 0AH and 0DH)
When DVOLC bit is "1" (default), DVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.

(6) Power up DAC: PMDAC bit = "0" → "1"
When ALC bit is "1", ALC operation starts from the gain set by AVL/R7-0 bits.

(7) Power up headphone-amp: PMHPL = PMHPR bits = "0" → "1"
Output voltage of headphone-amp is still VSS2.

(8) Rise up the common voltage of headphone-amp: HPMTN bit = "0" → "1"
The rise time depends on HVDD and the capacitor value which connected with the MUTET pin. When HVDD=3.3V and the capacitor value is 1.0μF, the time constant is τ_r = 100ms(typ), 250ms(max).

(9) Fall down the common voltage of headphone-amp: HPMTN bit = "1" → "0"
The fall time depends on HVDD and the capacitor value which connected with the MUTET pin. When HVDD=3.3V and the capacitor value is 1.0μF, the time constant is τ_f = 100ms(typ), 250ms(max).
If the power supply is powered-off or headphone-Amp is powered-down before the common voltage changes to GND, the pop noise occurs. It takes twice of τ_f that the common voltage changes to GND.

(10) Power down headphone-amp: PMHPL = PMHPR bits = "1" → "0"

(11) Power down DAC: PMDAC bit = "1" → "0"

(12) Disable the path of "DAC → HP-Amp": DACH bit = "1" → "0"

■ Stop of Clock

Master clock can be stopped when DAC is not used.

1. PLL Master Mode

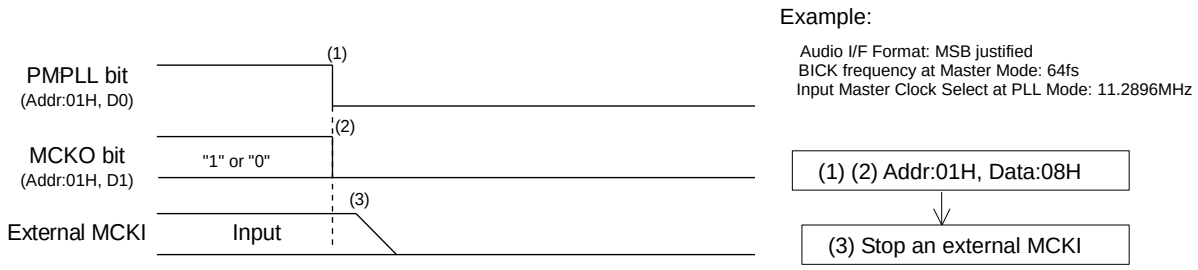


Figure 78. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (LRCK or BICK pin)

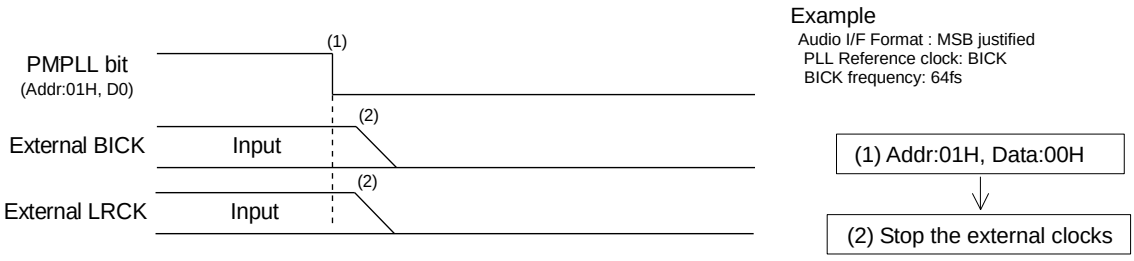


Figure 79. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and LRCK clocks

3. PLL Slave (MCKI pin)

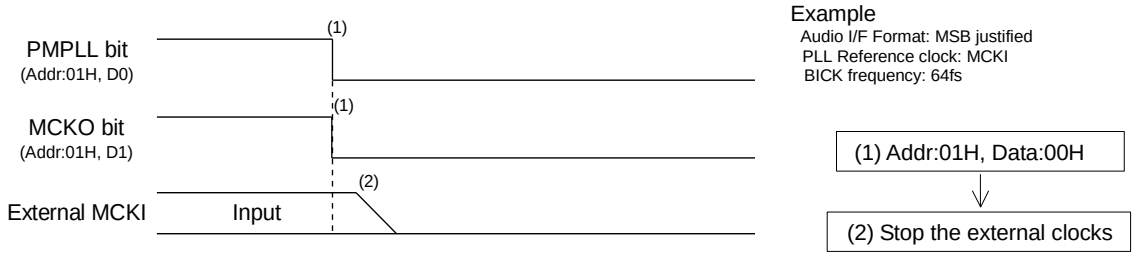


Figure 80. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
(2) Stop the external master clock.

4. EXT Slave Mode

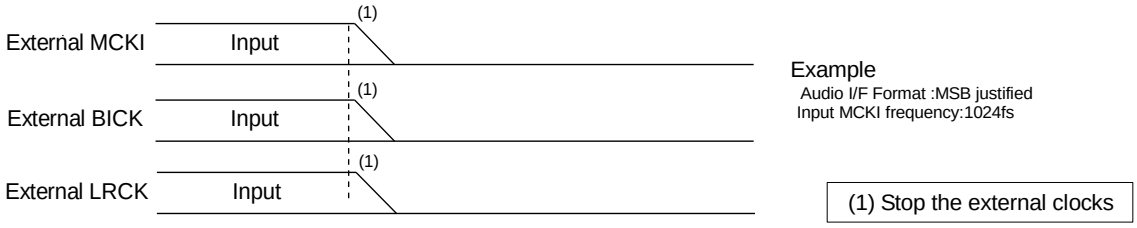


Figure 81. Clock Stopping Sequence (4)

<Example>
(1) Stop the external MCKI, BICK and LRCK clocks.

5. EXT Master Mode

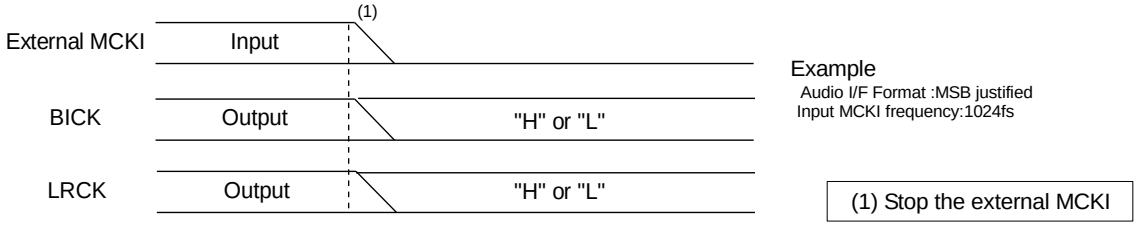


Figure 82. Clock Stopping Sequence (5)

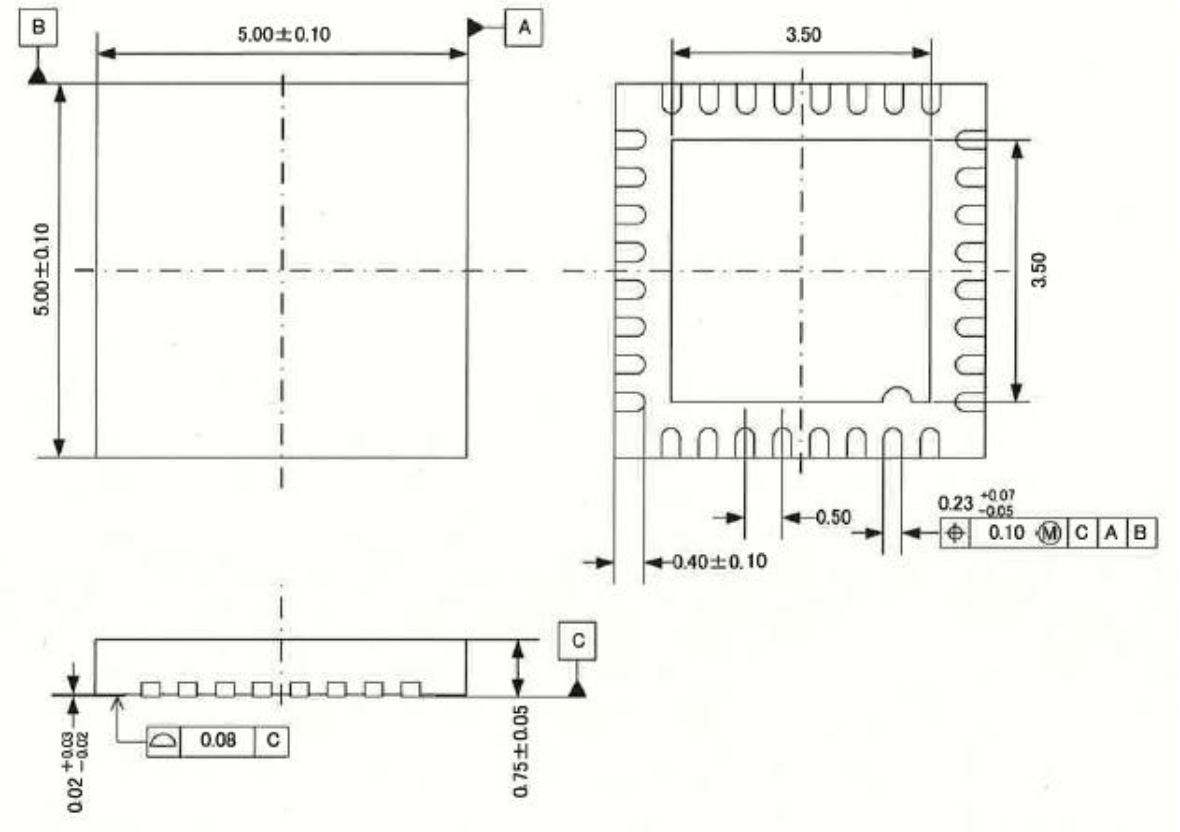
<Example>
(1) Stop MCKI clock. BICK and LRCK are fixed to “H” or “L”.

■ Power down

Power supply current can also be shut down (typ. 1μA) by stopping clocks and setting PDN pin = “L”. When PDN pin = “L”, the registers are initialized.

PACKAGE

●32pin QFN(Unit: mm)

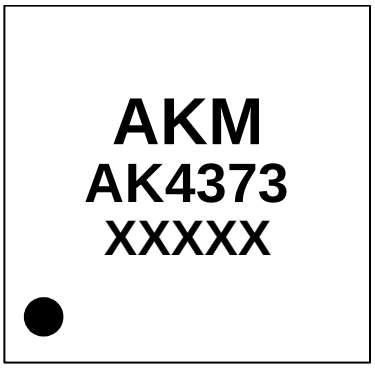


Note) The exposed pad on the bottom surface of the package must be open or connected to the ground.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXX : Date code identifier (5 digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/09/09	00	First Edition		
10/05/24	01	Specification Addition	10	RECOMMENDED OPERATING CONDITIONS AVDD – HVDD was added: 0.6V (max)
14/09/22	02	Specification change	97, 98	PACKAGE, MARKING Package dimensions, Making were changed.

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