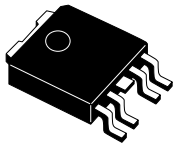
THE DATASHEET OF

VN800PTTR-E

VN800PT-E

High-side driver

Datasheet – production data



PPAK

GAPGRI00182

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN800PT-E	135 mΩ	0.7 A	36 V

- CMOS compatible input
- Thermal shutdown
- Current limitation
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low stand-by current
- Reverse battery protection
- Compliant with European directive 2002/95/EC

Description

The VN800PT-E is a monolithic device manufactured using STMicroelectronics® VIPower® M0-3 technology, intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes.

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload.

Device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in norms conformity with IEC1131 (Programmable Controllers International Standard).

Table 1. Device summary

Package	Order code	
	Tube	Tape and reel
PPAK	VN800PT-E	VN800PTTR-E

Contents

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1 Block diagram and pin description

Figure 1. Block diagram

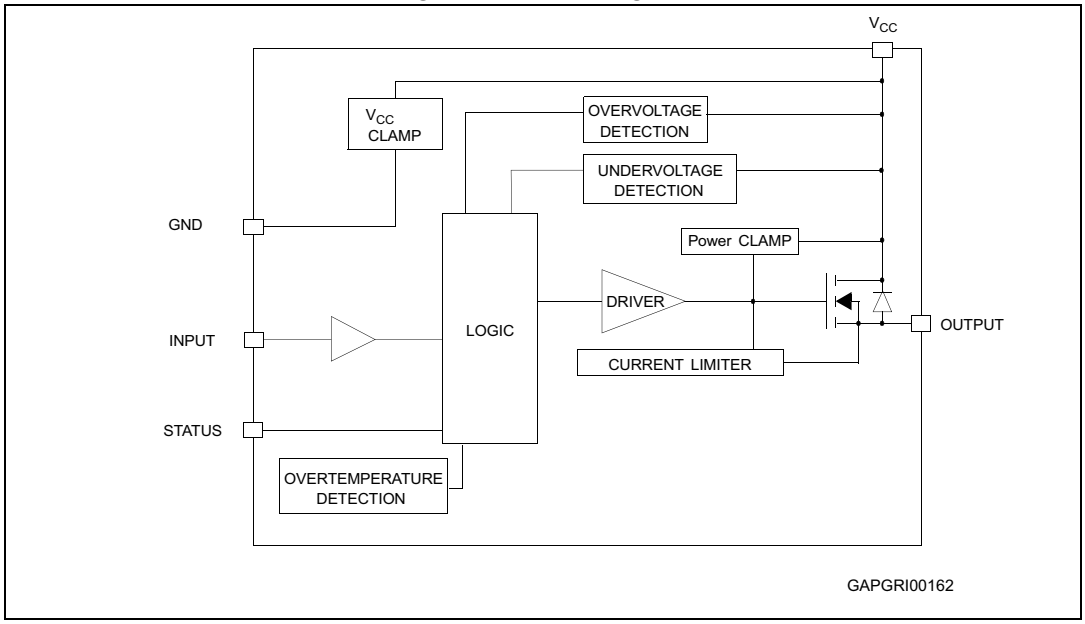


Figure 2. Configuration diagram (top view)

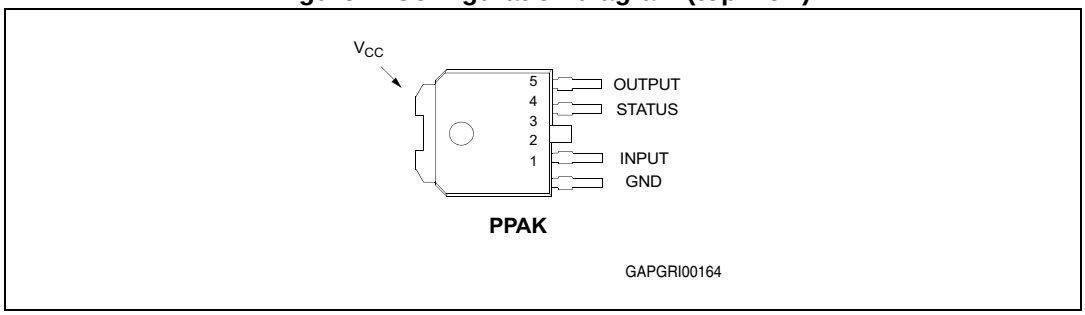


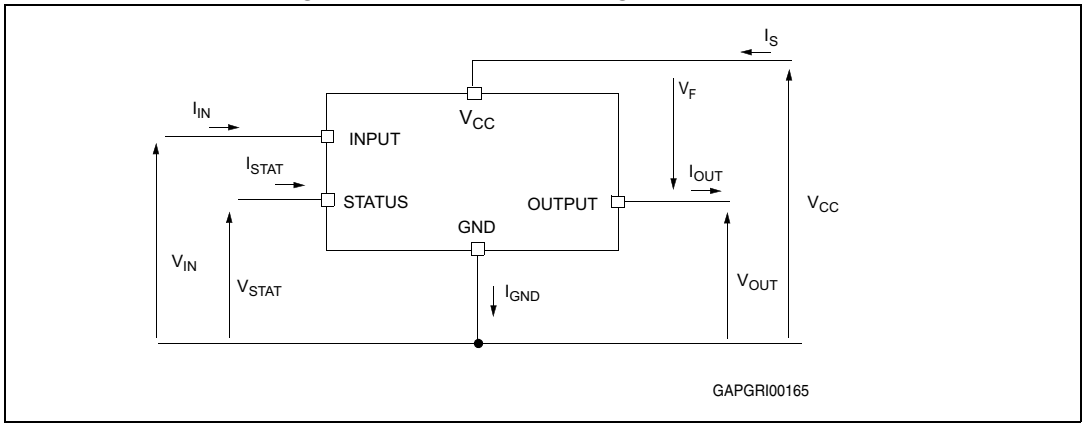
Table 2. Suggested connections for unused and n.c. pins

Connection / Pin	Status	N.C.	Output	Input
Floating	X(1)	X	X	X
To ground		X		Through 10 kΩ resistor

1. X: do not care.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the*Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-6	A
I_{IN}	DC input current	+/- 10	mA
V_{IN}	Input voltage range	$-3/+V_{CC}$	V
V_{STAT}	DC Status voltage	$+ V_{CC}$	V
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 kΩ; C = 100 pF) – INPUT – STATUS – OUTPUT – V_{CC}	 4000 4000 5000 5000	 V V V V
P_{tot}	Power dissipation T_C = 25 °C	41.7	W
E_{MAX}	Maximum switching energy (L = 125 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_L = 1.5 A)	195	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C
L_{max}	Max inductive load (V_{CC} = 30 V; I_{LOAD} = 0.5 A; T_{amb} = 100 °C; $Rth_{case>ambient} \leq$ 25 °C/W)	2	H

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value (Max)	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	3	°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead	—	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	78(1)	°C/W
		45(2)	°C/W

1. When mounted on FR4 printed circuit board with 2 cm^2 of copper area (at least 35 m thick).
2. When mounted on FR4 printed circuit board with 6 cm^2 of copper area (at least 35 m thick).

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 36 V; -40 °C < T_j < 150 °C unless otherwise specified.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5		36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36	42		V
R_{ON}	On-state resistance	I_{OUT} = 0.5 A; T_j = 25 °C			135	mΩ
		I_{OUT} = 0.5 A			270	mΩ
I_S	Supply current	Off-state; V_{CC} = 24V; T_{case} = 25°C		10	20	µA
		On-state; V_{CC} = 24 V		1.5	3.5	mA
		On-state; V_{CC} = 24 V; T_{case} = 100 °C			2.6	mA
I_{LGND}	Output current at turn-off	V_{CC} = V_{STAT} = V_{IN} = V_{GND} = 24 V; V_{OUT} = 0 V			1	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13 V; T_j = 125 °C			5	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0V; V_{CC} = 13 V; T_j = 25 °C			3	µA

Table 6. Switching (V_{CC} = 24 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 48 Ω from V_{IN} rising edge to V_{OUT} = 2.4 V	—	10	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 48 Ω from V_{IN} falling edge to V_{OUT} = 21.6V	—	40	—	µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 48 Ω from V_{OUT} = 2.4 V to V_{OUT} = 19.2 V	—	See *Figure 17*	—	V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 48 Ω from V_{OUT} = 21.6 V to V_{OUT} = 2.4 V	—	See *Figure 18*	—	V/µs

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{INL}	Input low level				1.25	V
I_{INL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{INH}	Input high level		3.25			V

Table 7. Input pin (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{INH}	High level input current	V_{IN} = 3.25 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
I_{IN}	Input current	$V_{IN} = V_{CC}$ = 36 V			200	µA

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$-I_{OUT}$ = 0.6 A; T_j = 150 °C	—	—	0.6	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6 mA	—	—	0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = V_{CC}$ = 36 V	—	—	10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5 V	—	—	30	pF

Table 10. Protections

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down temperature	—	150	175	200	°C
T_R	Reset temperature	—	135			°C
T_{hyst}	Thermal hysteresis	—	7	15		°C
T_{SDL}	Status delay in overload condition	$T_j > T_{jsh}$			20	µs
I_{lim}	DC short circuit current	V_{CC} = 24 V; R_{LOAD} = 10 mΩ	0.7		2	A
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 0.5 A; L = 6 mH	V_{CC} - 47	V_{CC} - 52	V_{CC} - 57	V

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Figure 4. Status timings

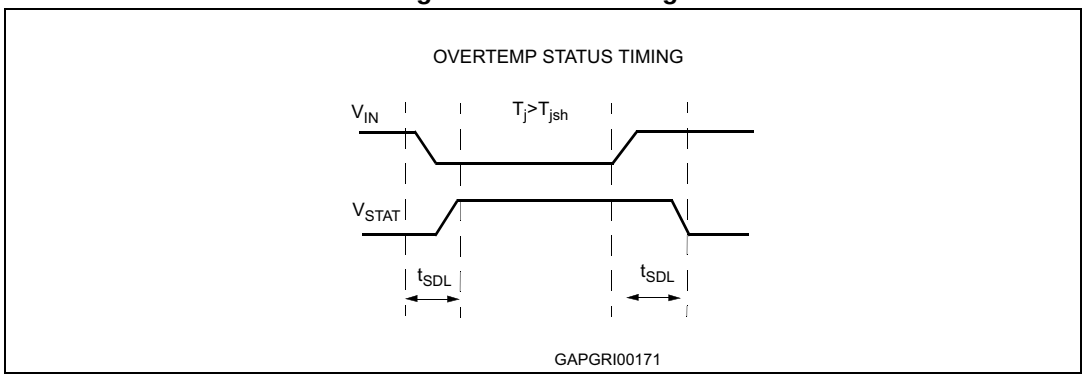


Figure 5. Switching time waveforms

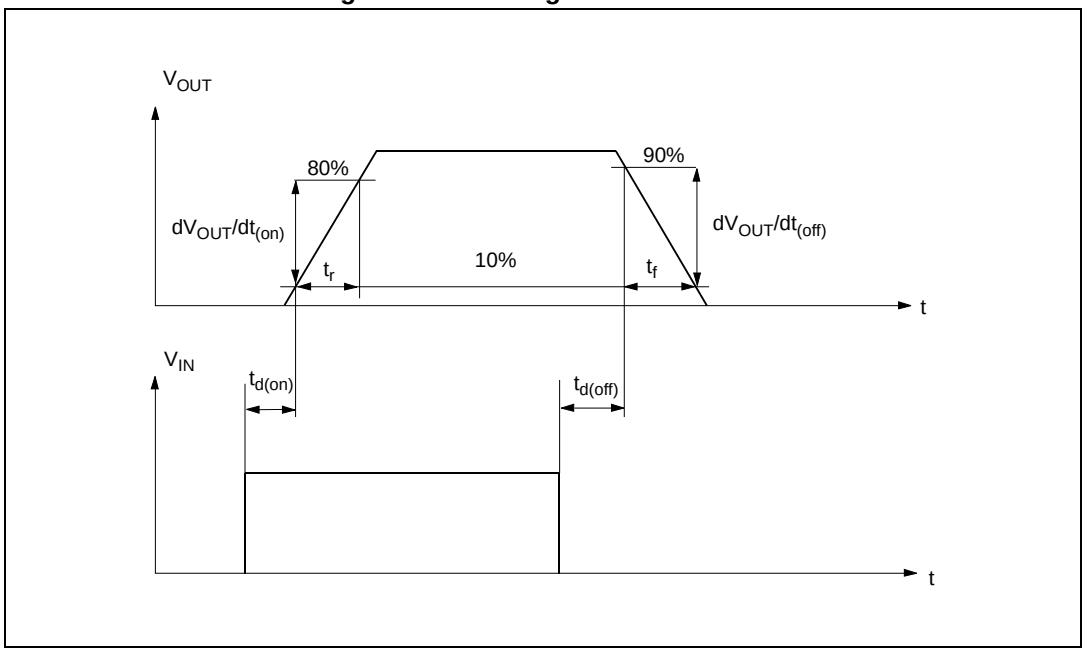


Table 11. Truth table

Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H

Table 12. Electrical transient requirements on V_{CC} pin (part 1/3)

ISO T/R 7637/1 Test Pulse	Test levels				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms, 10Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms, 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs, 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

Table 13. Electrical transient requirements on V_{CC} pin (part 2/3)

ISO T/R 7637/1 Test Pulse	TEST LEVELS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 14. Electrical transient requirements on V_{CC} pin (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Peak short circuit current test circuit

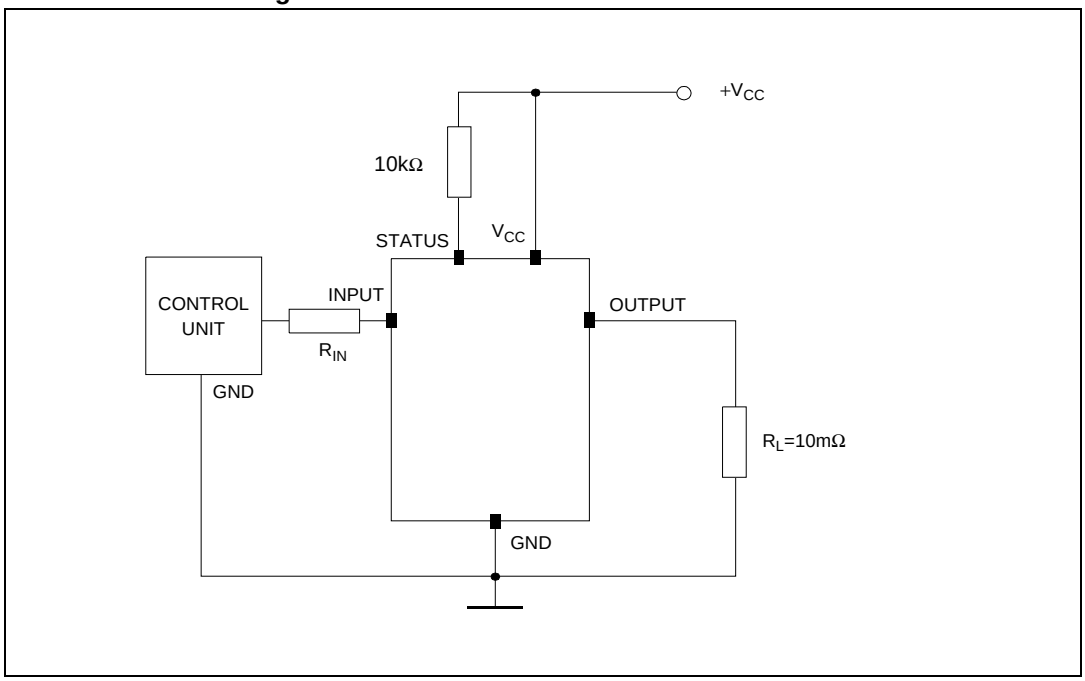


Figure 7. Avalanche energy test circuit

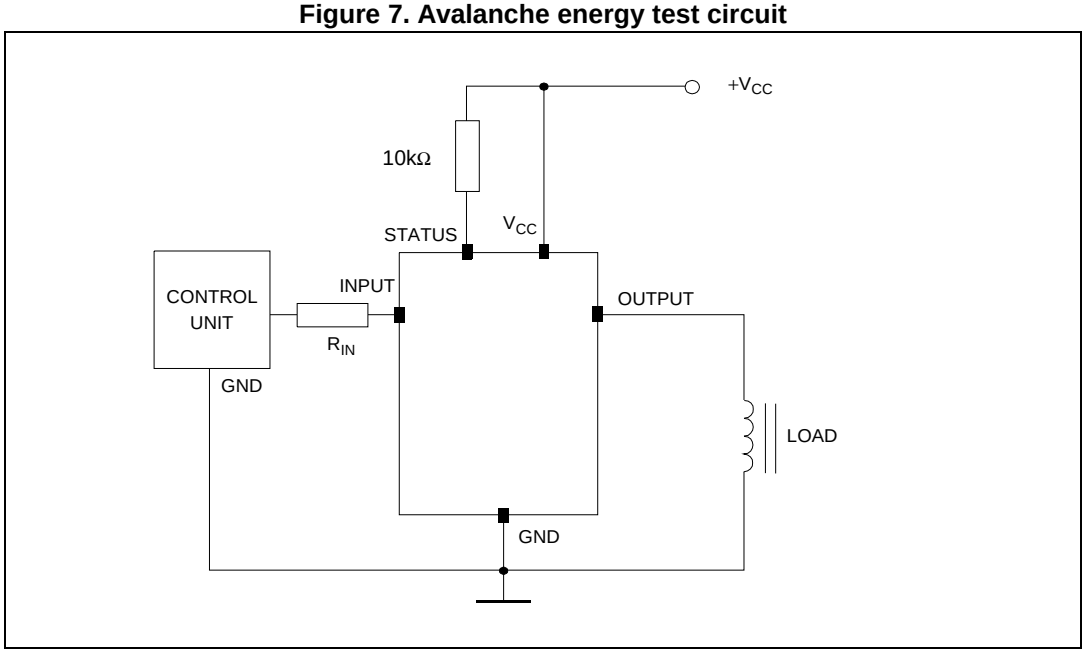
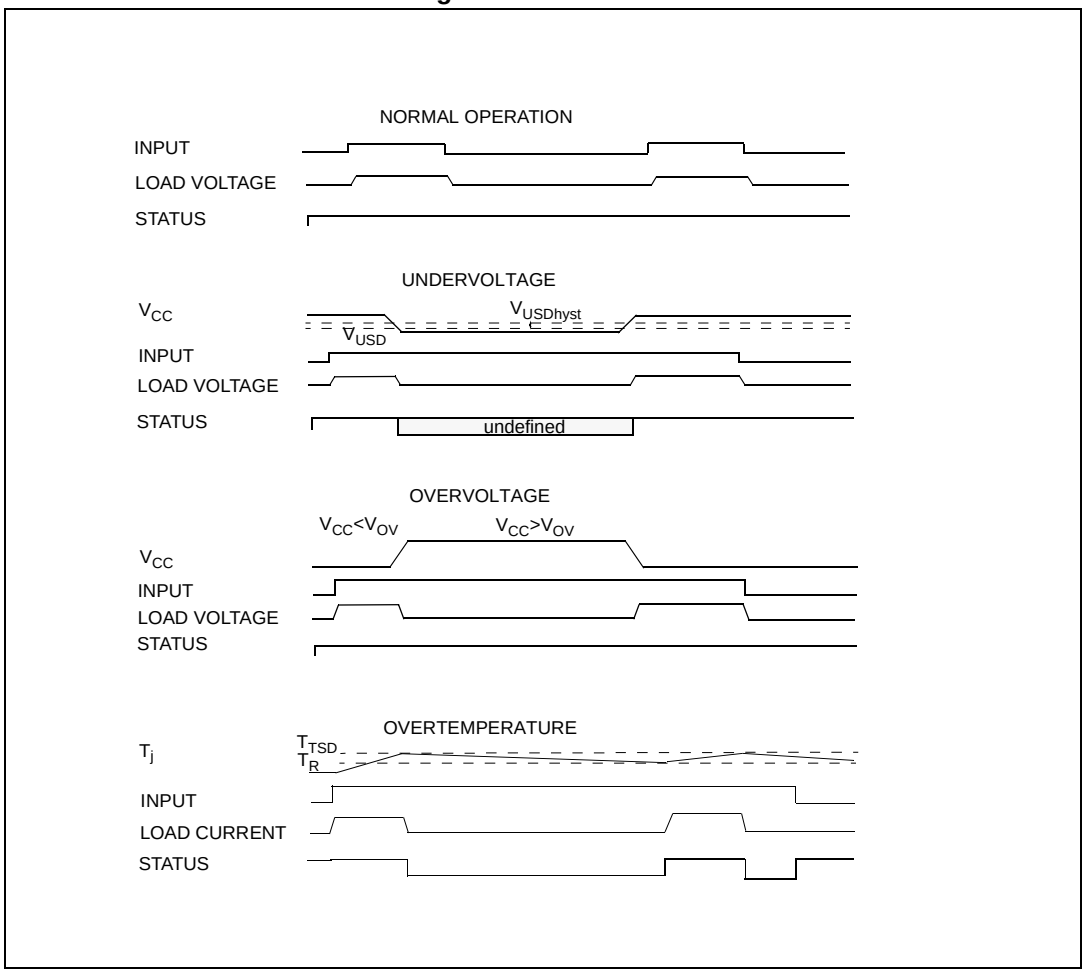


Figure 8. Waveforms



3 Electrical characteristics curves

Figure 9. Off-state output current

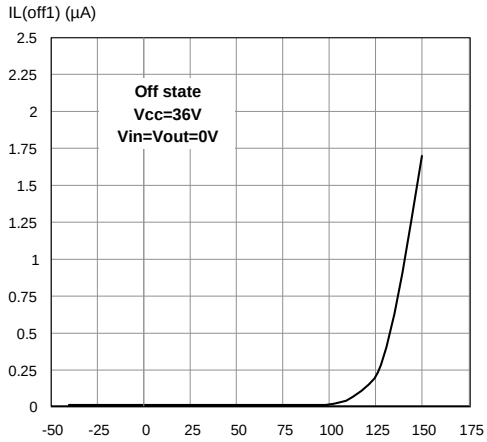


Figure 10. High level input current

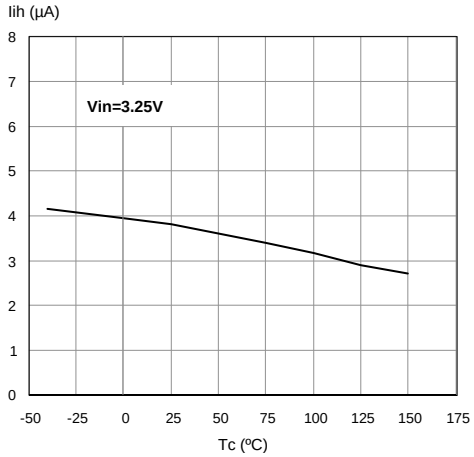


Figure 11. Status leakage current

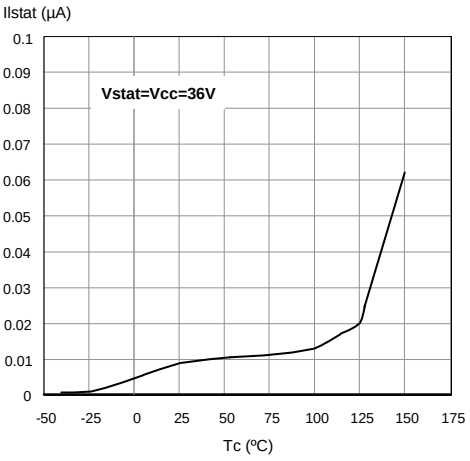


Figure 12. On-state resistance vs V_{CC}

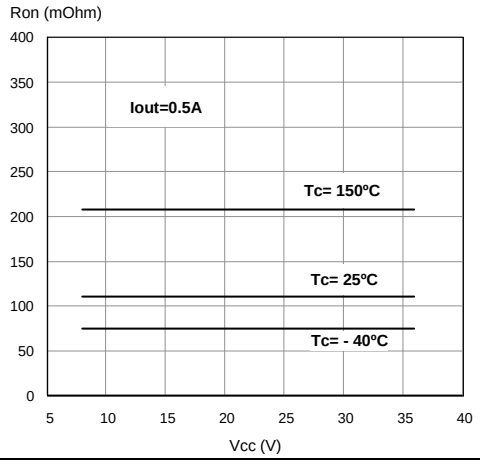


Figure 13. On-state resistance vs T_{case}

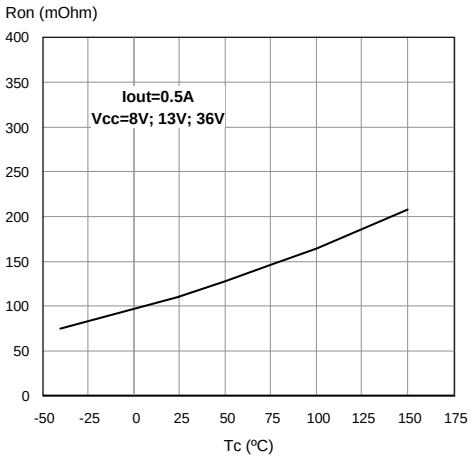


Figure 14. Input high level

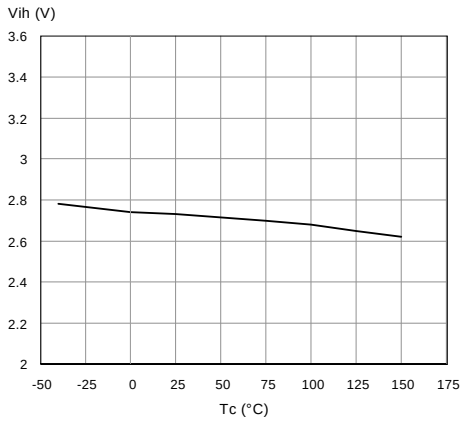


Figure 15. Input low level

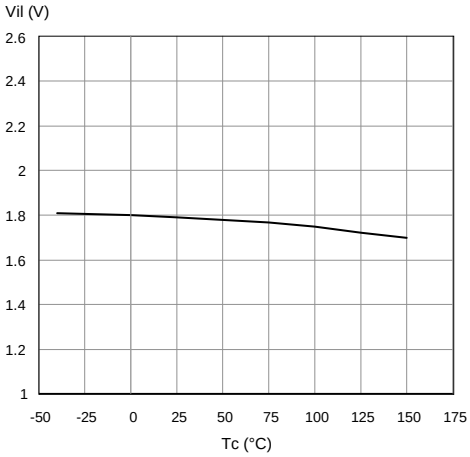


Figure 16. Input hysteresis voltage

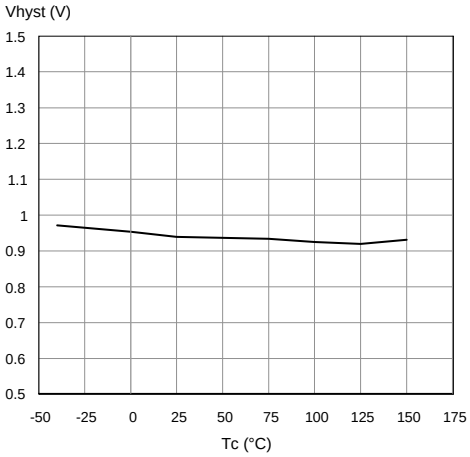


Figure 17. Turn-on voltage slope

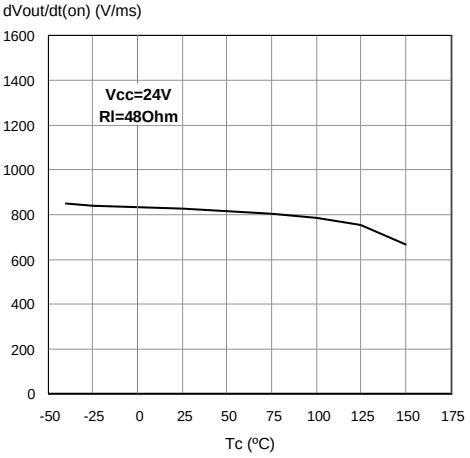


Figure 18. Turn-off voltage slope

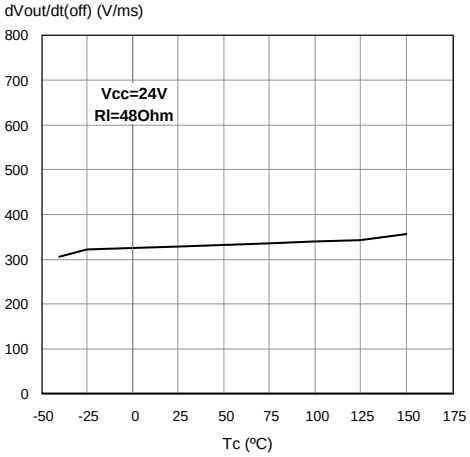


Figure 19. Overvoltage shutdown

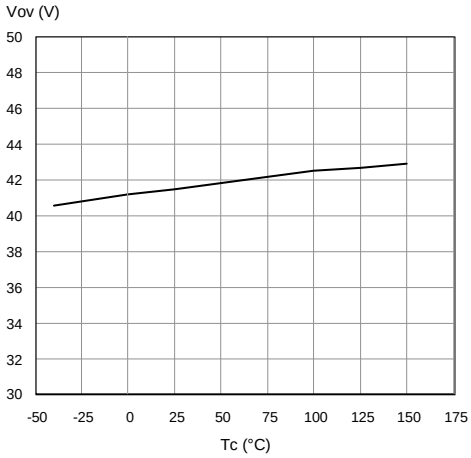
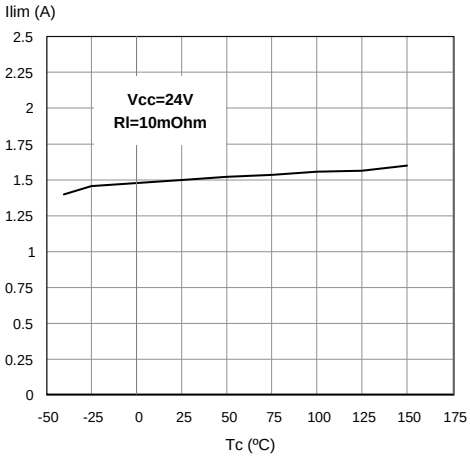
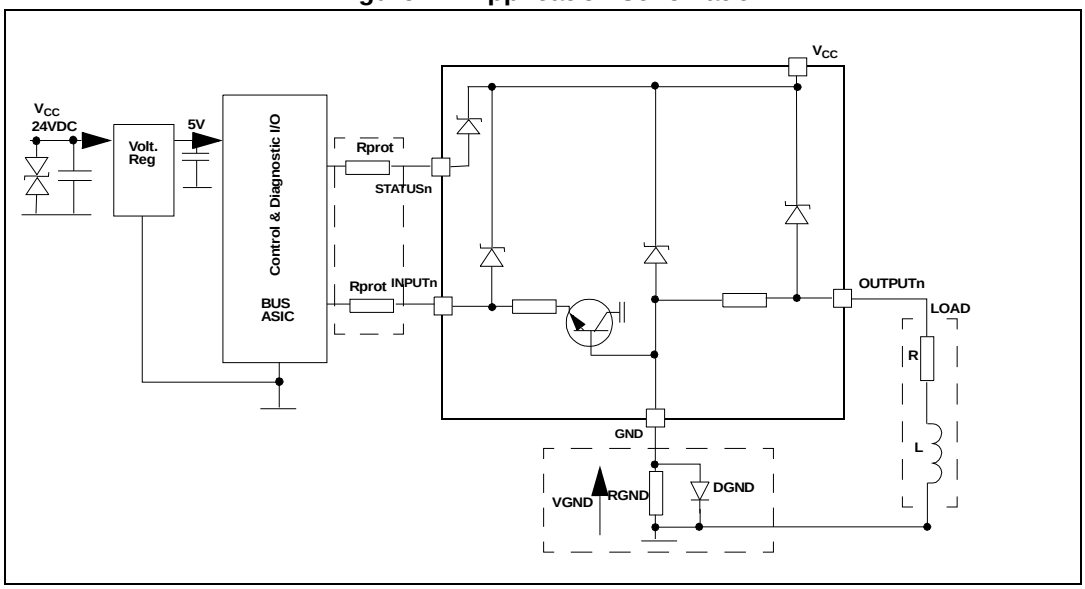


Figure 20. I_{LIM} vs T_{case}



3.1 Application information

Figure 21. Application schematic



3.2 GND protection network against reverse battery

3.2.1 Solution 1: resistor in the ground line (R_{GND} only).

This solution can be used with any type of load

The following is an indication on how to set the dimension of the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on the number of devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize *Section 3.3*.

3.3 Solution 2: a diode (DGND) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device is driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.3.1 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

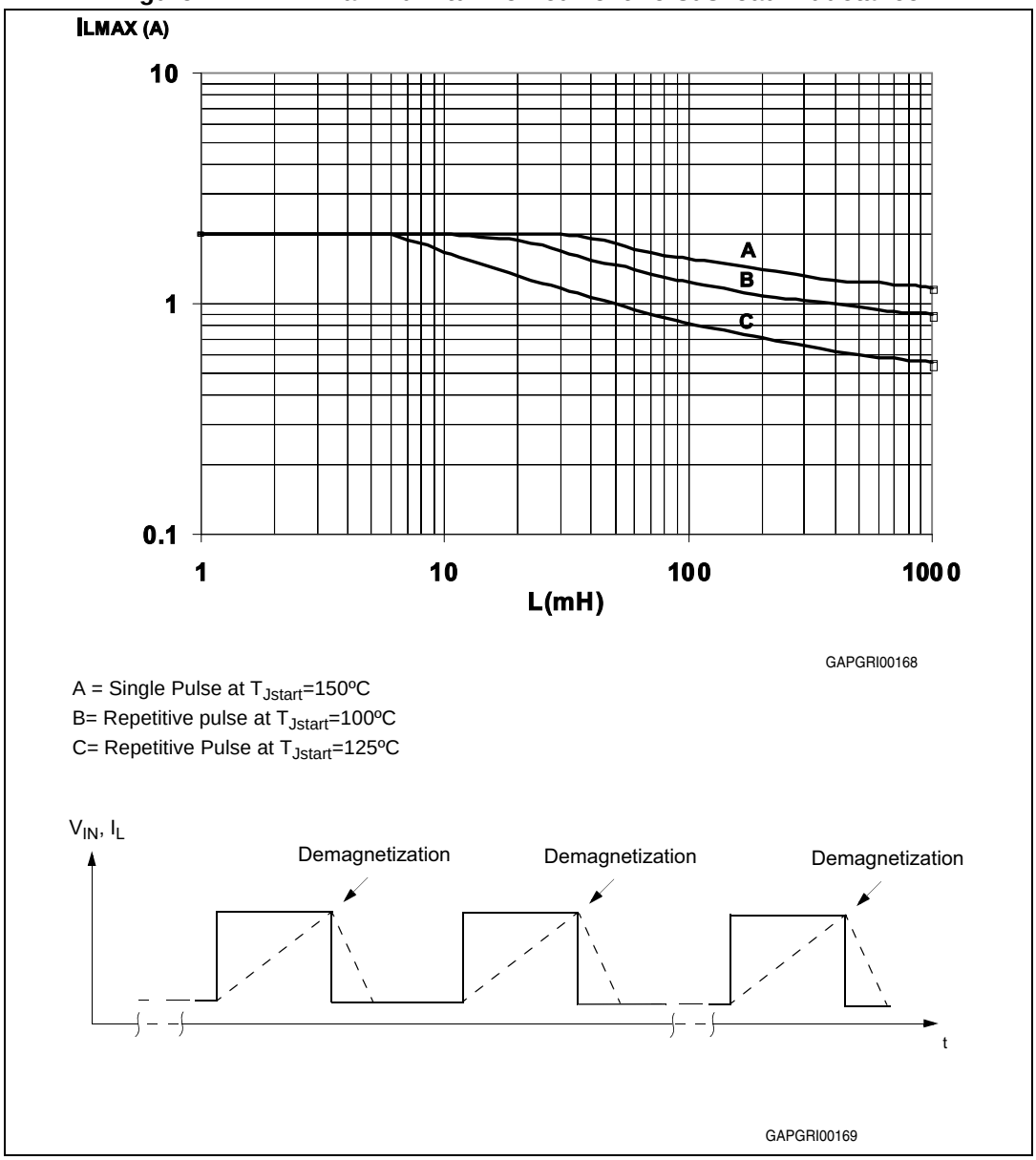
For V_{CCpeak} = -100 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

5 kΩ ≤ R_{prot} ≤ 65 kΩ.

Recommended R_{prot} value is 10 kΩ.

3.4 PPAK maximum demagnetization energy (V_{CC} = 13.5 V)

Figure 22. PPAK maximum turn-off current versus load inductance

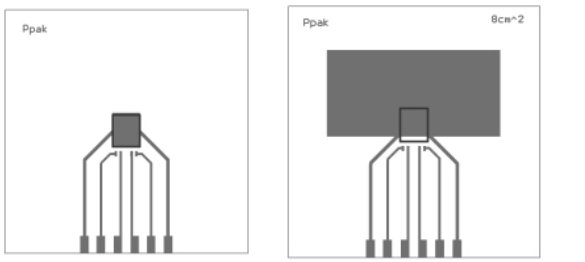


Note: Values are generated with R_L = 0 Ω. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 PPAK thermal data

Figure 23. PPAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness = 35 µm, Copper areas: 0.44 cm^2, 8 cm^2).

Figure 24. PPAK $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

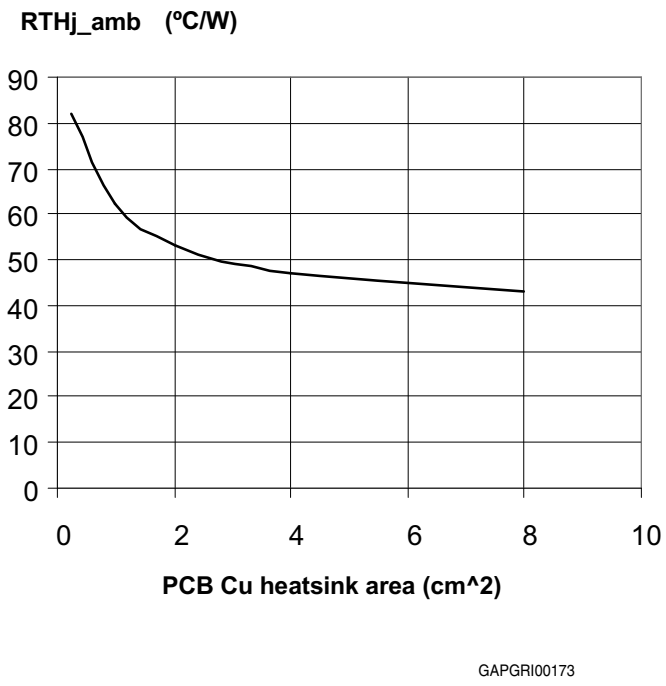
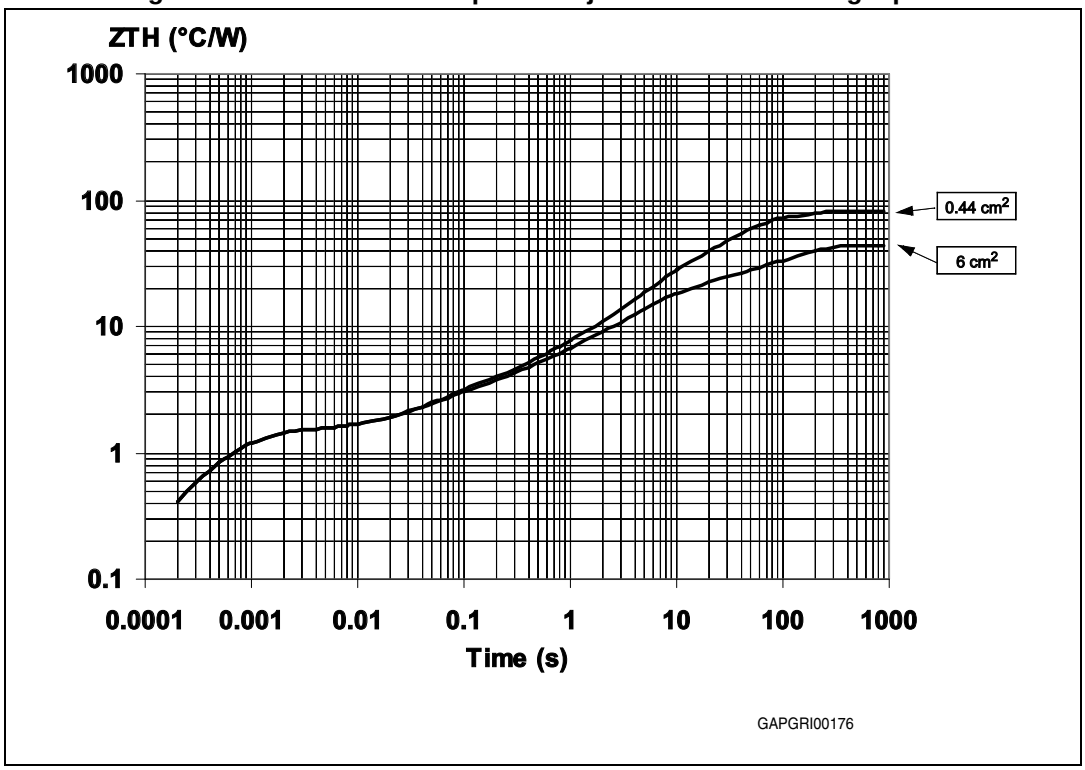


Figure 25. PPAK thermal impedance junction ambient single pulse



Equation 1: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 26. Thermal fitting model of a single channel HSD in PPAK

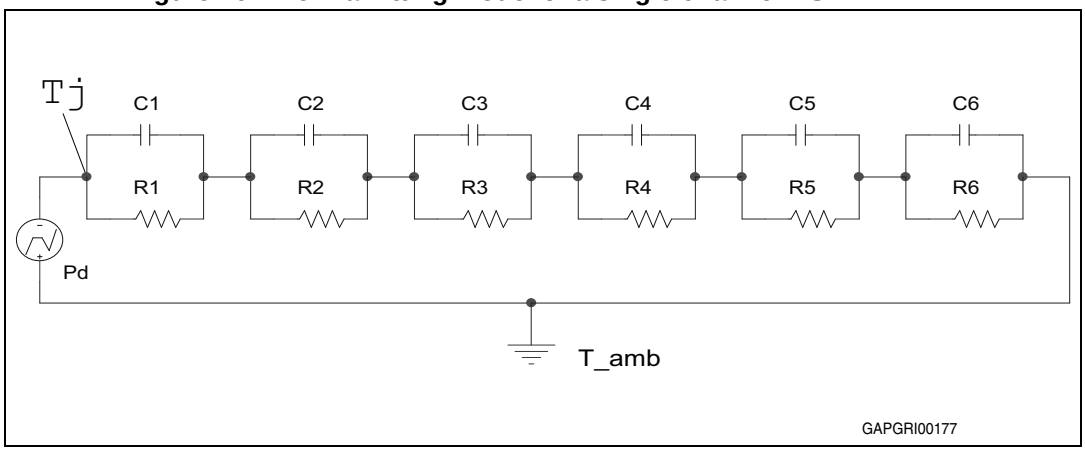


Table 15. Thermal parameter

Ara/island (cm^2)	0.44	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	0.007	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 PPAK package mechanical data

Figure 27. PPAK package dimensions

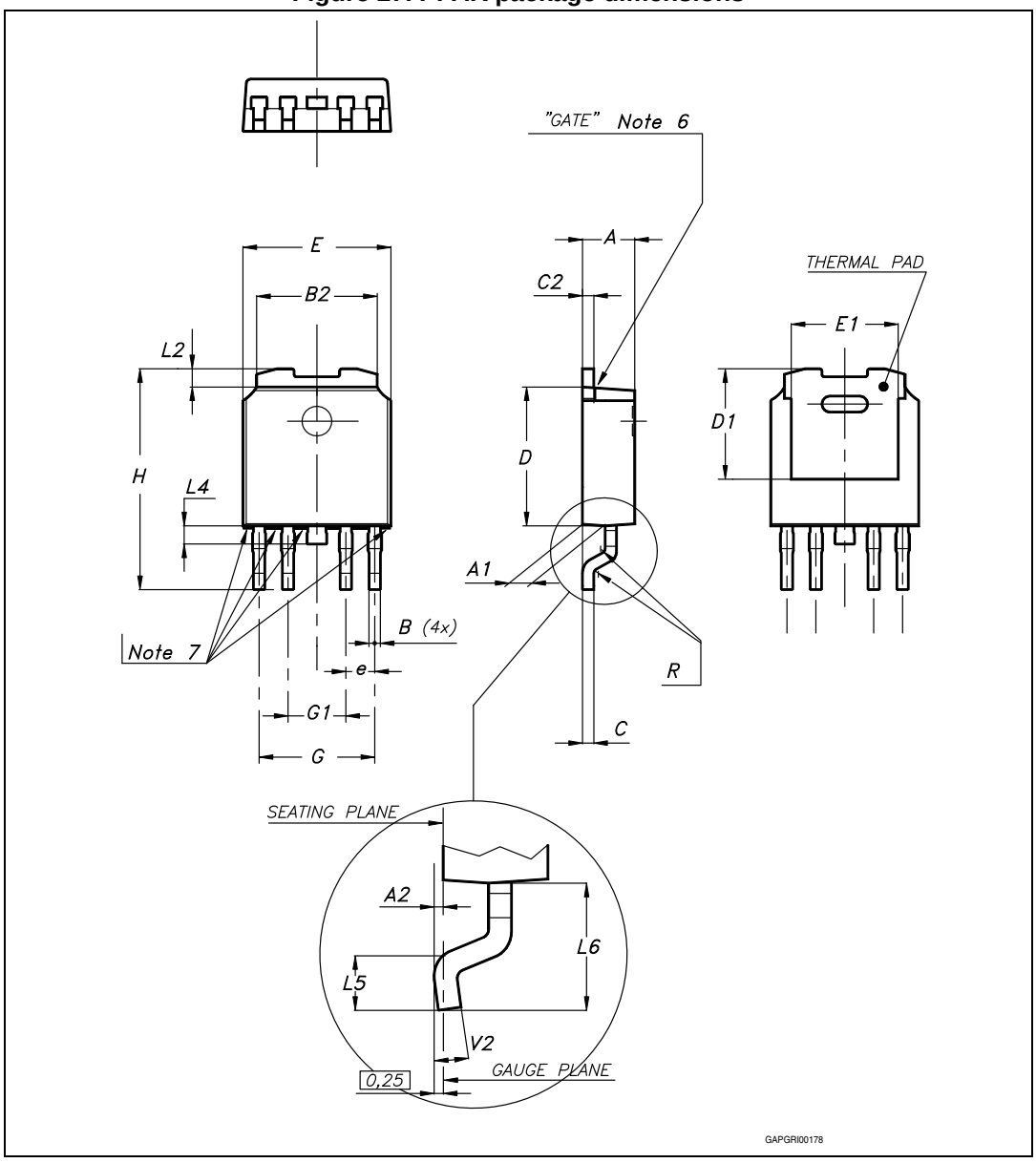
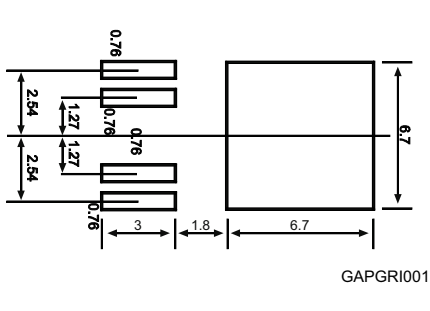


Table 16. PPAK mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
L5	1		—
L6		2.80	
R		0.20	
V2	0º		8º
Package Weight	Gr. 0.3		

5.2.1 PPAK packing information

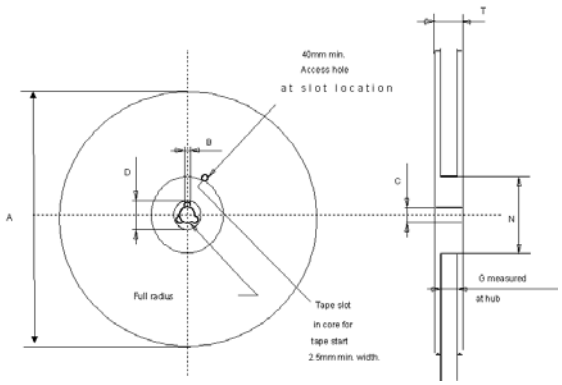
Figure 28. PPAK suggested pad layout and tube shipment (no suffix)



All dimensions are in mm.

Base Q.ty	75
Bulk Q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

Figure 29. PPAK tape and reel shipment (suffix "TR")



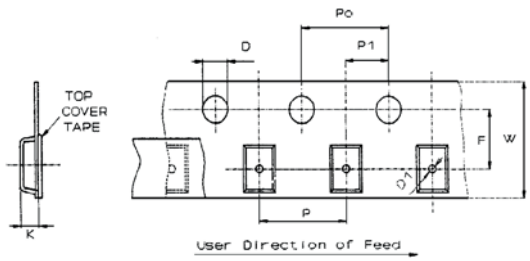
REEL DIMENSIONS

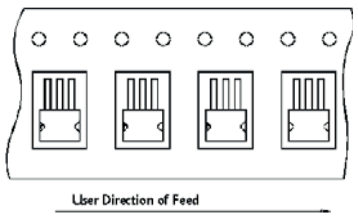
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / - 0)	16.4

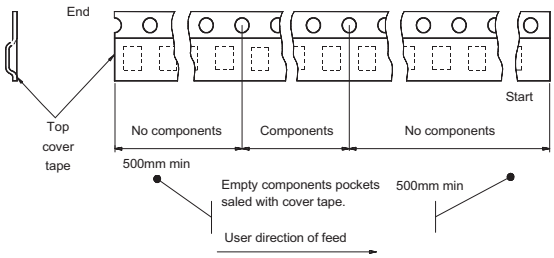
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	2.75







GAPGRI00181

6 Revision history

Table 17. Revision history

Date	Revision	Changes
7-Oct-2004	1	Initial release.
02-May-2012	2	Update entire document following new ST template. Update *Figure 27* and *Table 16*.
20-Sep-2013	3	Updated Disclaimer.
21-Oct-2014	4	The part number VN800S-E has been moved to a separate datasheet. Removed SO-8 package.

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