THE DATASHEET OF

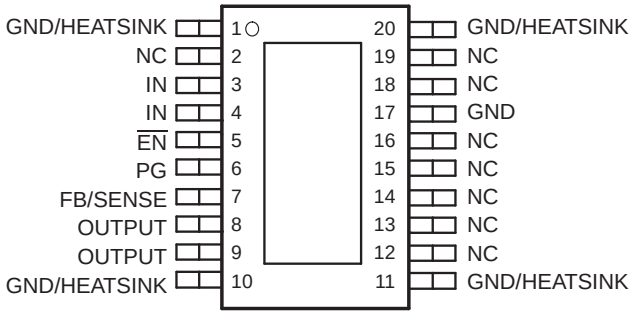
TPS75125MPWPREP

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **1.5 A Low Dropout Voltage Regulator**
- **Available in 2.5 V Fixed Output**
- **Open Drain Power Good (PG) Status Output**
- **Ultra Low 75 µA Typical Quiescent Current**
- **Fast Transient Response**
- **3% Tolerance Over Specified Conditions for Fixed Output Version**
- **20 Pin TSSOP (PWP) PowerPAD™ Package**
- **Thermal Shutdown Protection**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PWP PACKAGE
(TOP VIEW)



NC − No internal connection

DESCRIPTION/ORDERING INFORMATION

TPS75125-EP is a low-dropout regulator with a power good (PG) function. Quiescent current is 75 µA at full load and drops down to 1 µA when the device is disabled. TPS75125-EP is designed to have fast transient response for larger load current changes.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 75 µA over the full range of output current, 1 mA to 1.5 A). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The device is enabled when the enable ($\overline{EN}$) input is connected to a low-level voltage. This low dropout (LDO) device also features a sleep mode; applying a TTL high signal to $\overline{EN}$ shuts down the regulator, reducing the quiescent current to less than 1 µA at T_J = 25°C.

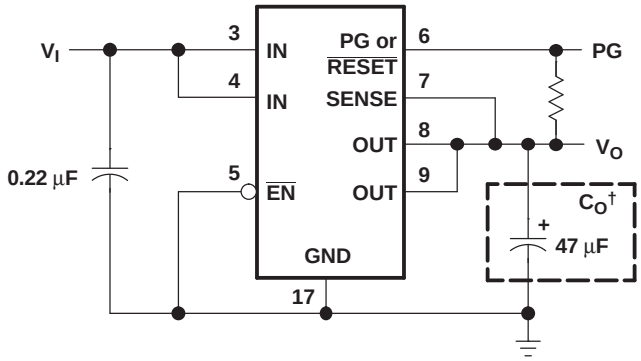
The TPS75125-EP power good (PG) terminal is an active-high, open-drain output that can be used to implement a power-on reset or a low-battery indicator.

The TPS75125-EP is offered in a 2.5 V fixed-voltage version. Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS75125-EP is available in a 20-pin TSSOP (PWP) package.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	TSSOP – PWP	TPS75125MPWPREP	75125MEP

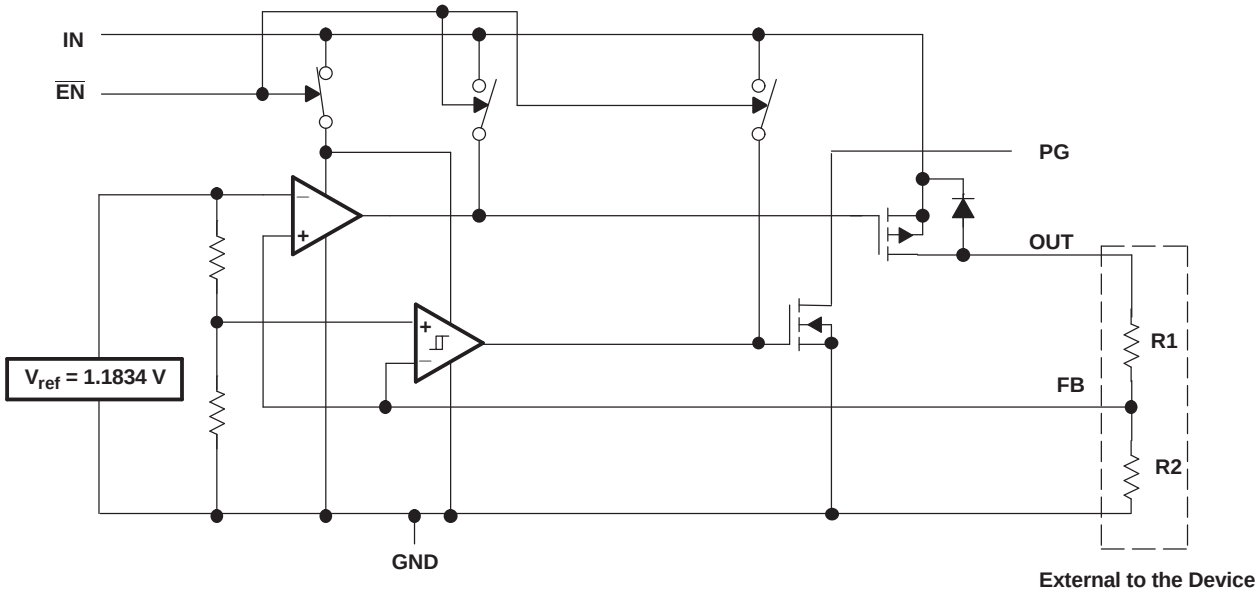
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



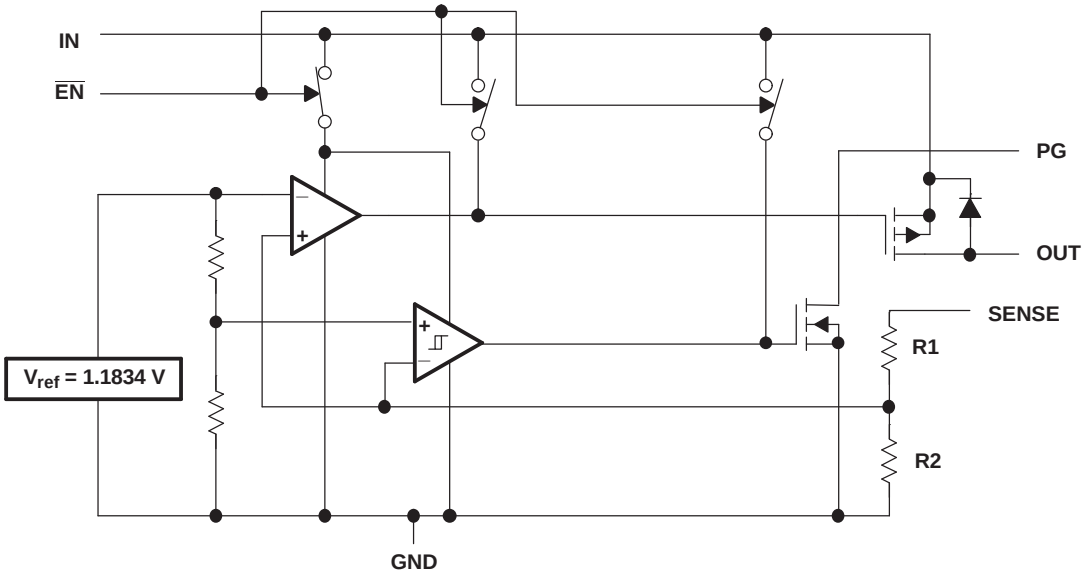
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration (for Fixed-Output Option)

FUNCTIONAL BLOCK DIAGRAM — ADJUSTABLE VERSION



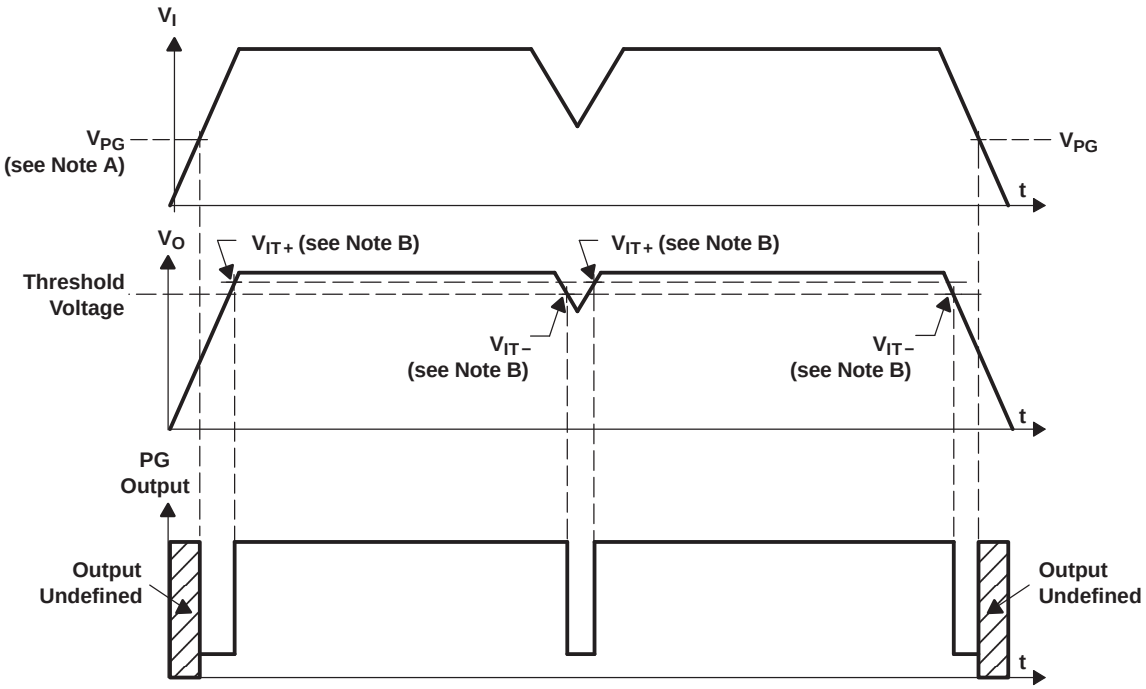
FUNCTIONAL BLOCK DIAGRAM — FIXED-VOLTAGE VERSION



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	5	I	Enable
FB/SENSE	7	I	Feedback input voltage for adjustable device (sense input for fixed option)
GND	17		Regulator ground
GND/HEATSINK	1, 10, 11, 20		Ground/heatsink
IN	3, 4	I	Input voltage
NC	2, 12–16, 18, 19		No connection
OUTPUT	8, 9	O	Regulated output voltage
PG	6	O	Power good

PG TIMING DIAGRAM



NOTES: A. V_{PG} is the minimum input voltage for a valid PG. The symbol V_{PG} currently is not listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} − Trip voltage typically is 17% lower than the output voltage (83% V_O). V_{IT-} to V_{IT+} is the hysteresis voltage.

Absolute Maximum Ratings(1)

over operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range(2)		–0.3	6	V
	Voltage range at $\overline{EN}$		–0.3	16.5	V
	Maximum PG voltage			16.5	V
	Peak output current			Internally limited	
	Continuous total power dissipation			See dissipation rating tables	
V_O	Output voltage	OUTPUT, FB		5.5	V
T_J	Operating virtual junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–65	150	°C
	ESD rating	Human-Body Model		2	kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE — FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
PWP(1)	0	2.9 W	23.5 mW/°C	1.9 W	0.55 W
	300	4.3 W	34.6 mW/°C	2.8 W	0.84 W
PWP(2)	0	3 W	23.8 mW/°C	1.9 W	0.62 W
	300	7.2 W	57.9 mW/°C	4.6 W	1.41 W

(1) This parameter is measured with the recommended copper heatsink pattern on a one-layer PCB, 5 in × 5 in PCB, 1 oz copper, 2-in × 2-in coverage (4 in^2).
(2) This parameter is measured with the recommended copper heatsink pattern on an eight-layer PCB, 1.5 in × 2 in PCB, 1 oz copper with layers one, two, four, five, seven, and eight at 5% coverage (0.9 in^2) and layers three and six at 100% coverage (6 in^2). For more information, refer to TI technical brief SLMA002.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_I(1)	Input voltage	2.7	5.5	V
V_O	Output voltage	1.5	5	V
I_O	Output current	0	1.5	A
T_A	Operating ambient temperature	–55	125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following equation:
V_I min = V_O max + V_{DO} max load.

Electrical Characteristics

over recommended operating ambient temperature range (T_A = –55°C to 125°C), $V_I = V_O$ typ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_O = 47 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage(1)(2)	2.5-V fixed version	T_J = 25°C,	3.5 V < V_{IN} < 5.5 V		2.5		V
		3.5 V < V_{IN} < 5.5 V		2.450		2.575	
Quiescent current (GND current)(3)		T_J = 25°C(2)			75		µA
		(2)				125	
Output voltage line regulation ($\Delta V_O/V_O$)(1)(3)		V_O + 1 V < V_I ≤ 5.5 V,	T_J = 25°C		0.01		%/V
		V_O + 1 V < V_I < 5.5 V				0.14	
Load regulation(2)(3)					1		mV
Output noise voltage		BW = 300 Hz to 50 kHz, C_O = 100 µF,	V_O = 1.5 V, T_J = 25°C		60		µVrms
Output current limit		V_O = 0 V			3.3	4.5	A
Thermal-shutdown junction temperature					150		°C
Standby current		$\overline{EN}$ = V_I	T_J = 25°C		1		µA
						10	
FB input current		FB = 1.5 V		–1		1	µA
High-level enable input voltage				2			V
Low-level enable input voltage						0.7	V
Power-supply ripple rejection(3)		f = 100 Hz, T_J = 25°C,	C_O = 100 µF, I_O = 1.5 A(1)		63		dB
PG	Minimum input voltage for valid PG	$I_{O(PG)}$ = 300 µA,	$V_{(PG)}$ ≤ 0.8 V		1	1.3	V
	Trip threshold voltage	V_O decreasing		80		86	%V_O
	Hysteresis voltage	Measured at V_O			0.5		%V_O
	Output low voltage	V_I = 2.7 V,	$I_{O(PG)}$ = 1 mA		0.15	0.4	V
	Leakage current	$V_{(PG)}$ = 5.5 V				1	µA
Input current ($\overline{EN}$)		$\overline{EN}$ = V_I		–1		1	µA
		$\overline{EN}$ = 0 V		–1	0	1	µA
High-level $\overline{EN}$ input voltage				2			V
Low-level $\overline{EN}$ input voltage						0.7	V
Dropout voltage (3.3-V output)(4)		I_O = 1.5 A, V_I = 3.2 V,	T_J = 25°C		160		mV
		I_O = 1.5 A,	V_I = 3.2 V			400	

(1) Minimum IN operating voltage is 2.7 V or V_O typ + 1 V, whichever is greater. Maximum IN voltage 5.5 V.
(2) I_O = 1 mA to 1.5 A
(3) If V_O ≤ 1.8 V, V_I min = 2.7 V, V_I max = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_I \text{max} - 2.7\ V\right)}{100} \times 1000$$

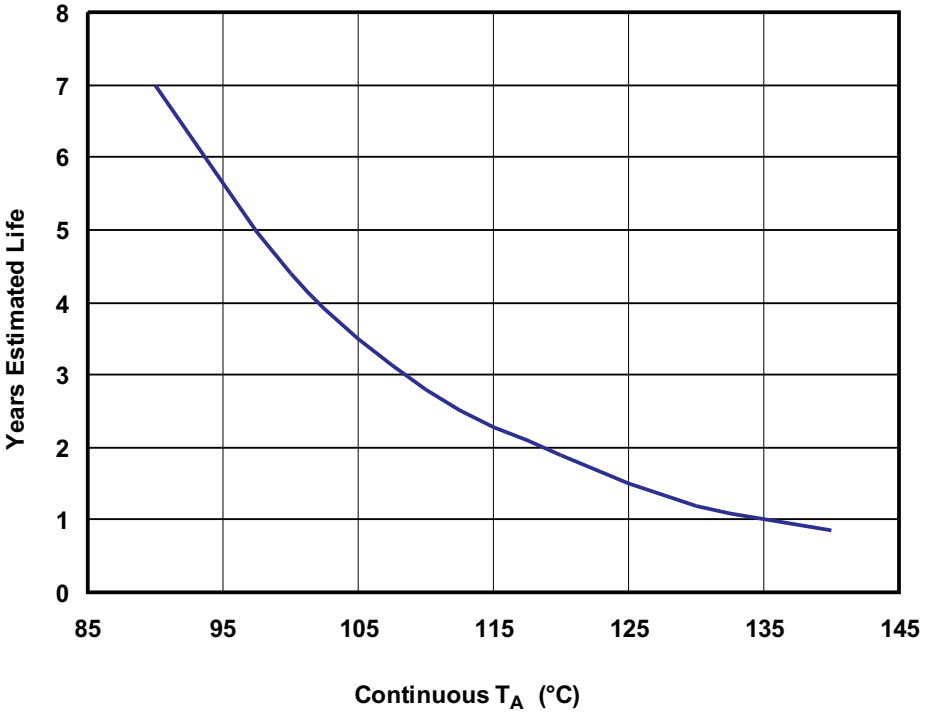
If V_O ≥ 2.5 V, V_I min = V_O + 1 V, V_I max = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left[V_I \text{ max} - \left(V_O + 1\ V\right)\right]}{100} \times 1000$$

(4) IN voltage equals V_O typ – 100 mV; dropout voltage limited by input voltage range limitations.

TYPICAL CHARACTERISTICS

Estimated Device Life at Elevated Temperatures Wirebond Voiding Fail Modes



GROUND CURRENT vs JUNCTION TEMPERATURE

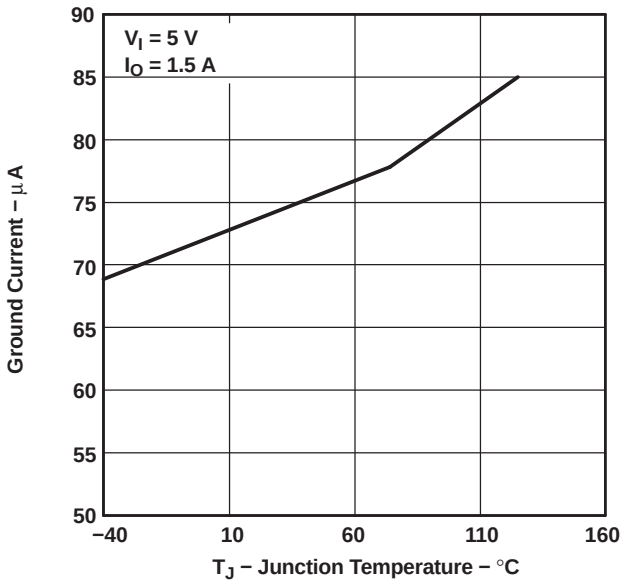


Figure 2.

INPUT VOLTAGE (MIN) vs OUTPUT VOLTAGE

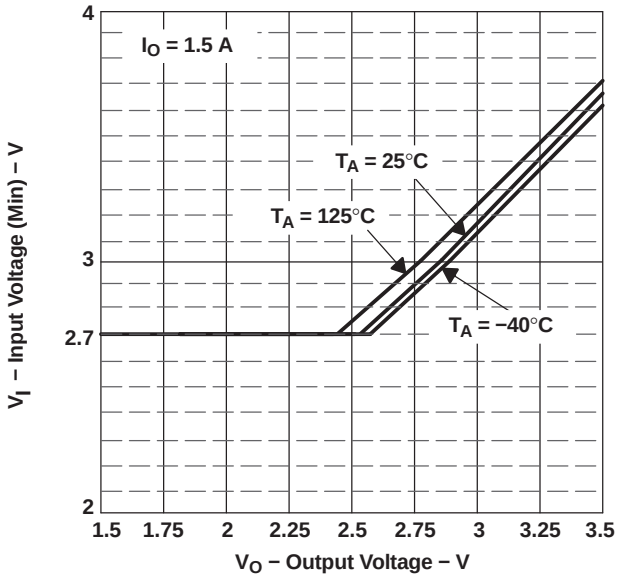


Figure 3.

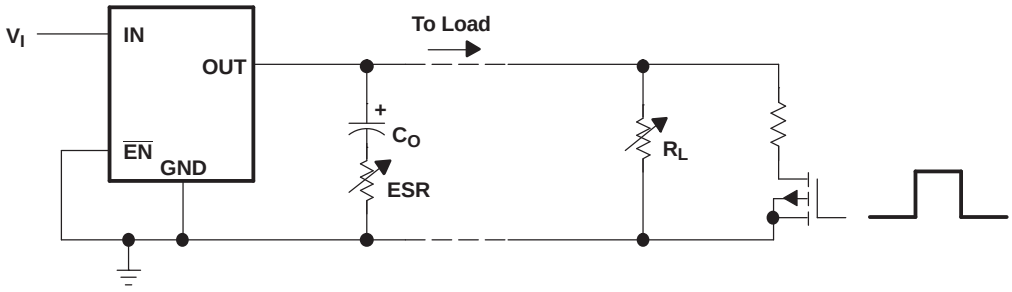
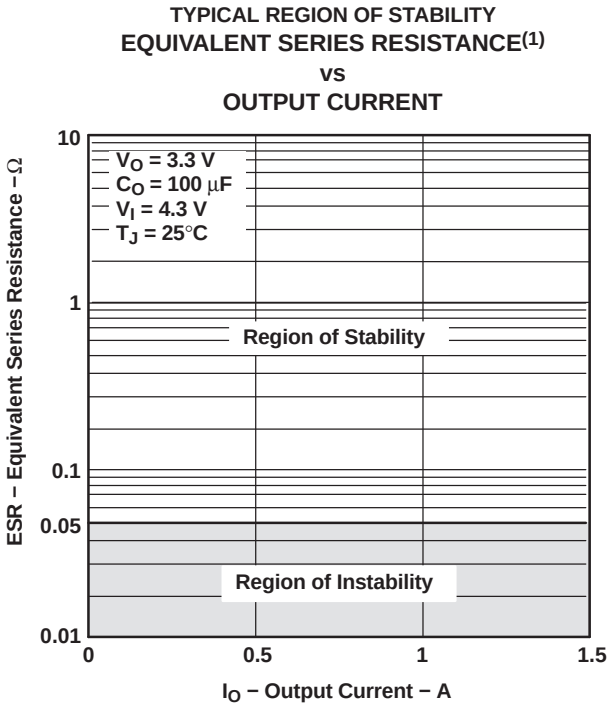
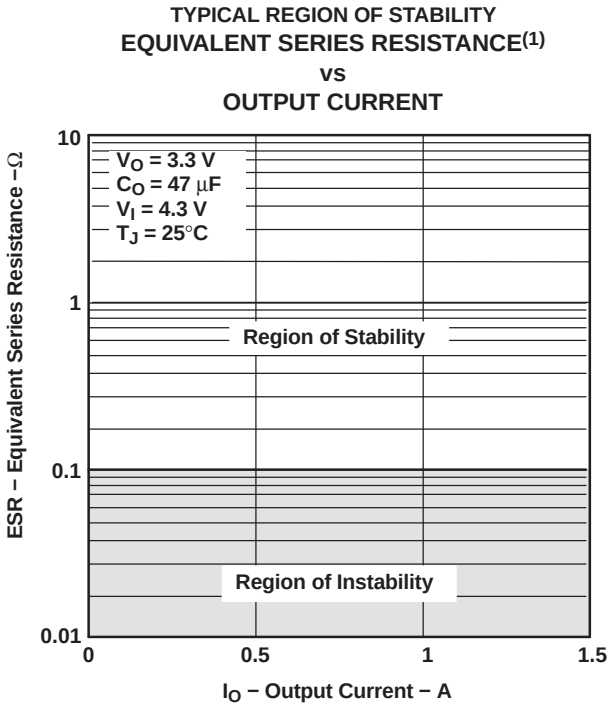


Figure 4. Test Circuit for Typical Regions of Stability (see Figures 5 and 6) (Fixed-Output Option)



(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

Figure 5.



(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

Figure 6.

APPLICATION INFORMATION

The TPS75125-EP is a fixed-output voltage regulator (2.5 V).

Minimum Load Requirements

The TPS75125-EP is stable, even at no load; no minimum load is required for operation.

Pin Functions

Enable ($\overline{EN}$)

The $\overline{EN}$ terminal is an input that enables or shuts down the device. If $\overline{EN}$ is a logic high, the device is in shutdown mode. When $\overline{EN}$ goes to logic low, the device is enabled.

Power Good (PG)

The PG terminal is an open-drain, active-high output that indicates the status of V_O (output of the LDO). When V_O reaches 83% of the regulated voltage, PG goes to a high-impedance state. PG goes to a low-impedance state when V_O falls below 83% (i.e., overload condition) of the regulated voltage. The open-drain output of PG requires a pullup resistor.

Sense (SENSE)

The SENSE terminal of the fixed-output option must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance, wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between SENSE and V_O to filter noise is not recommended because it may cause the regulator to oscillate.

Feedback (FB)

FB is an input terminal used for the adjustable-output option and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB and V_O to filter noise is not recommended because it may cause the regulator to oscillate.

GND/HEATSINK

All GND/HEATSINK terminals are connected directly to the mount pad for thermal-enhanced operation. These terminals could be connected to GND or left floating.

Input Capacitor

For a typical application, an input bypass capacitor (0.22 µF – 1 µF) is recommended for device stability. This capacitor should be as close to the input pins as possible. For fast transient condition, where droop at the input of the LDO may occur due to high in-rush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor is dependant on the output current and response time of the main power supply as well as the distance to the load (LDO).

Output Capacitor

As with most LDO regulators, the TPS75125-EP requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 47 µF, and the equivalent series resistance (ESR) must be between 100 mΩ and 10 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described in this section. Larger capacitors provide a wider range of stability and better load transient response.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements, along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet these guidelines.

APPLICATION INFORMATION (continued)

ESR and Transient Response

LDOs typically require an external output capacitor for stability. In fast transient-response applications, capacitors are used to support the load current while the LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called equivalent series resistance (ESR), and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can, therefore, be drawn as shown in Figure 7.

Figure 7. ESR and ESL

In most cases, the effect of inductive impedance ESL can be neglected. Therefore, the following application focuses mainly on the parasitic-resistance ESR.

Figure 8 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

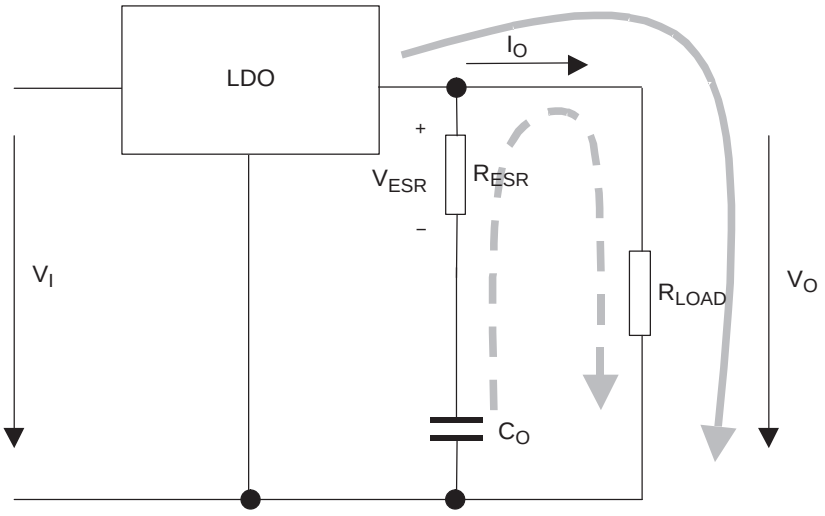


Figure 8. LDO Output Stage With Parasitic Resistances ESR and ESL

APPLICATION INFORMATION (continued)

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage [$V(C_O) = V_O$]. This means no current is flowing into the C_O branch. If I_O suddenly increases (transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 9). Therefore, capacitor C_O provides the current for the new load condition (dashed arrow). C_O now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop occurs at R_{ESR}. This voltage is shown as V_{ESR} in Figure 8.
- When C_O is conducting current to the load, initial voltage at the load is $V_O = V(C_O) – V_{ESR}$. Due to the discharge of C_O, the output voltage V_O drops continuously until the response time t_1 of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 9.

Figure 9 also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs, where number 1 displays the lowest and number 3 displays the highest ESR.

From the previous description, these conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

Conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output-voltage requirement.

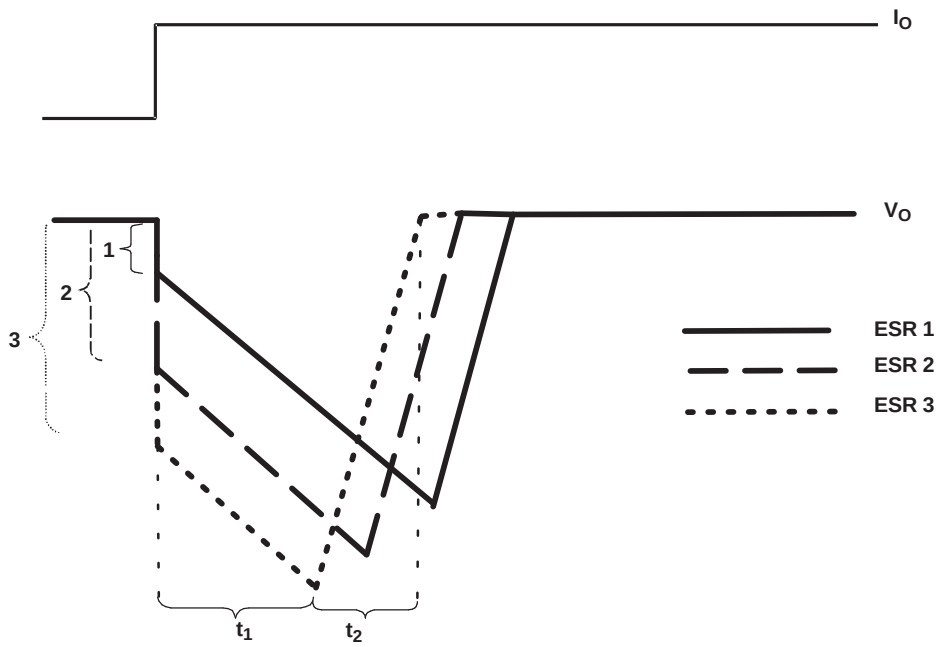


Figure 9. Correlation of Different ESRs and Their Influence to Regulation of V_O at a Load Step From Low-to-High Output Current

APPLICATION INFORMATION (continued)

Regulator Protection

The TPS75125-EP PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS75125-EP also features internal current limiting and thermal protection. During normal operation, the device limits output current to approximately 3.3 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power-dissipation ratings of the package. If the temperature of the device exceeds 150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power-dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J\,max - T_A}{R_{\theta JA}} \quad (1)$$

Where:

T_J max = Maximum allowable junction temperature

$R_{\theta JA}$ = Thermal resistance junction-to-ambient for the package, i.e., 34.6°C/W for the 20-terminal PWP with no airflow (see Table 1)

T_A = Ambient temperature

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

THERMAL INFORMATION

Thermally-Enhanced TSSOP-20 (PWP – PowerPad™ Package)

The thermally-enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad (see Figure 10c) to provide an effective thermal contact between the IC and the printed wiring board (PWB).

Traditionally, surface mount and power have been mutually-exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings – they do not address the very low profile requirements (< 2 mm) of many of today's advanced systems, and they do not offer a pin count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally-enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal-conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

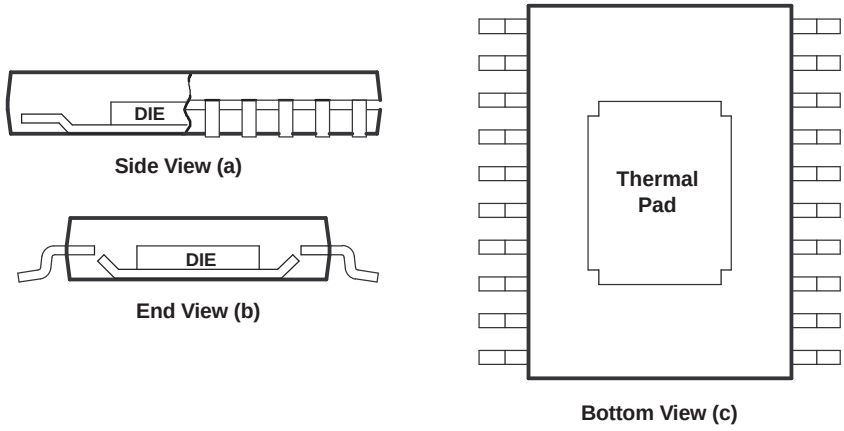


Figure 10. Views of Thermally-Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heatsink surface) that is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 12a, 8 cm^2 of copper heatsink and natural convection). Increasing the heatsink size increases the power-dissipation range for the component. The power-dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figure 11 and Figure 12). The line drawn at 0.3 cm^2 in Figure 11 and Figure 12 indicates performance at the minimum recommended heatsink size shown in Figure 14.

The thermal pad is directly connected to the substrate of the IC, which for the TPS75125PWP is a secondary electrical connection to device ground. The heatsink surface that is added to the PWP can be a ground plane or be left electrically isolated. In TO220-type surface-mount packages, the thermal connection also is the primary electrical connection for a given terminal, which is not always ground. The PWP package provides up to 16 independent leads that can be used as inputs and outputs (Note: leads 1, 10, 11, and 20 are connected internally to the thermal pad and the IC substrate).

THERMAL INFORMATION (continued)

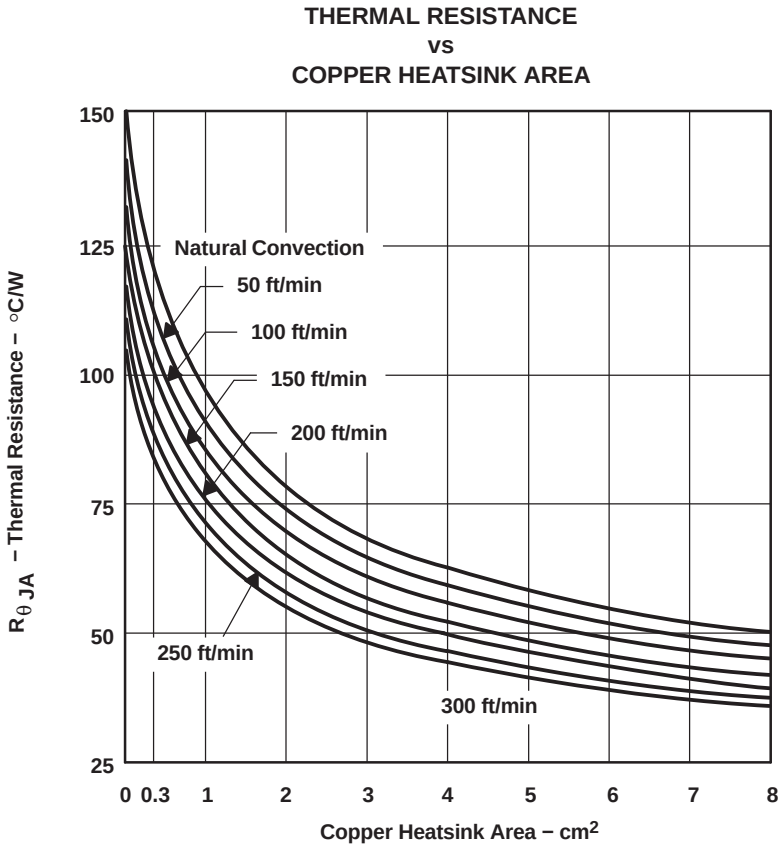


Figure 11.

THERMAL INFORMATION (continued)

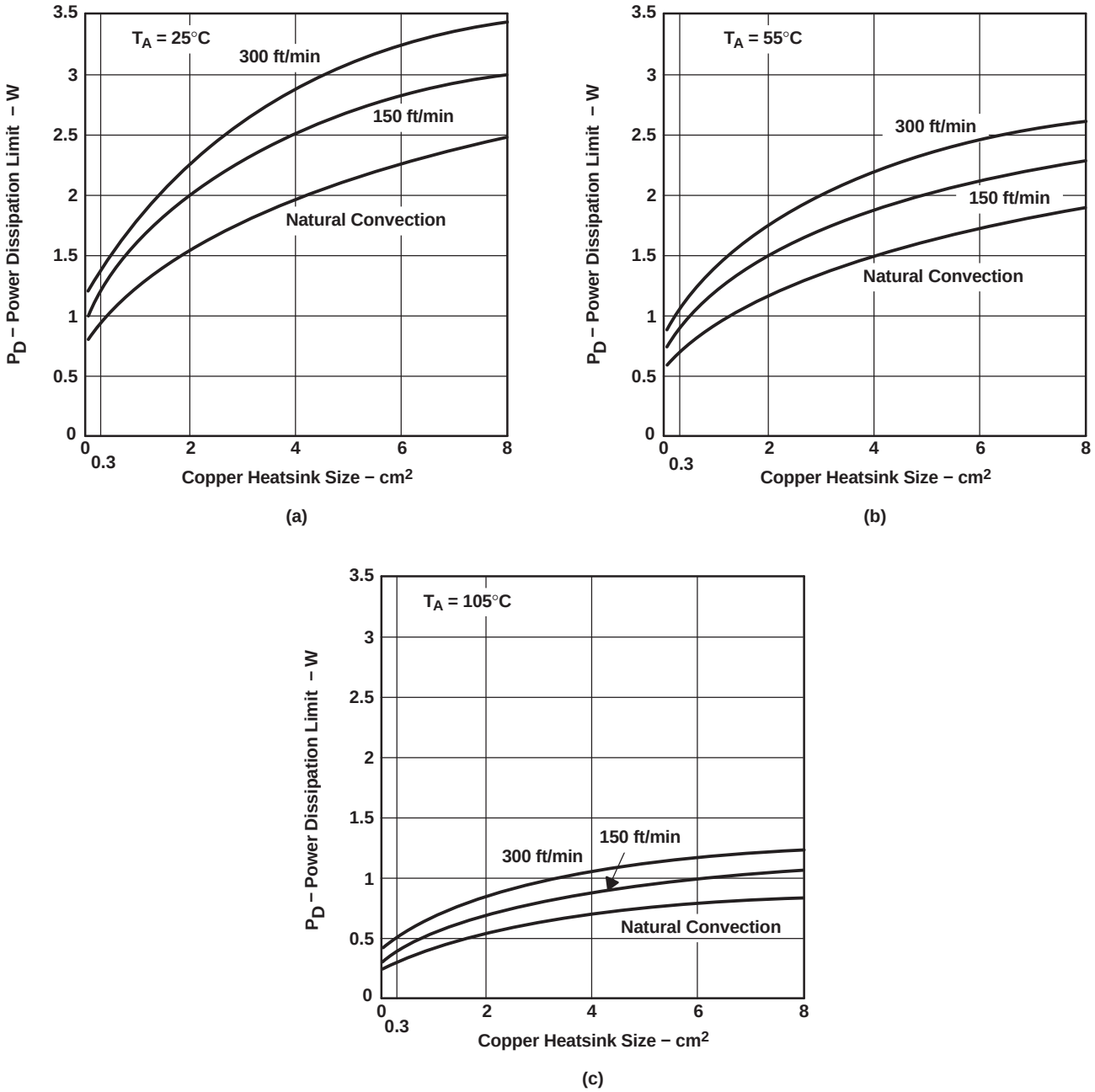
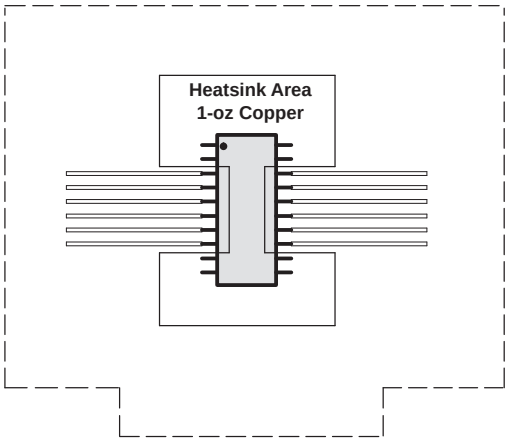


Figure 12. PWP Package Power Ratings at Ambient Temperatures of 25°C, 55°C, and 105°C

Figure 13 is an example of a thermally-enhanced PWB layout for use with the PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figure 11 and Figure 12. As previously discussed, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is shown in Figure 11 as a function of heatsink area. A family of curves is included to show the effect of airflow introduced into the system.

THERMAL INFORMATION (continued)



Board thickness	62 mils
Board size	3.2 in × 3.2 in
Board material	FR4
Copper trace/heatsink	1 oz
Exposed pad mounting	63/67 tin/lead solder

Figure 13. PWB Layout (Including Copper Heatsink Area) for Thermally-Enhanced PWP Package

From Figure 11, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_J\ max - T_A}{R_{\theta JA(system)}} \quad (3)$$

Where:

T_J max = Maximum specified junction temperature
(150°C absolute maximum limit, 125°C recommended operating limit)
T_A = Ambient temperature

For the case where T_A = 55°C, airflow = 200 ft/min, copper heatsink area = 4 cm^2, the maximum power-dissipation limit can be calculated. First, from Figure 11, the system $R_{\theta JA}$ is 50°C/W, therefore, the maximum power dissipation limit is:

$$P_{D(max)} = \frac{T_J\ max - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{50°C/W} = 1.4\ W \quad (4)$$

If the system implements a TPS75133QPWP regulator, where V_I = 5 V and I_O = 800 mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \times I_O = (5 - 3.3) \times 0.8 = 1.36\ W \quad (5)$$

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made – raising the power-dissipation limit by increasing the airflow or the heatsink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the previous calculations should be repeated with the new system parameters.

THERMAL INFORMATION (continued)

Mounting Information

The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder connection is not desirable, up to 50% voiding is acceptable. The data included in Figure 11 and Figure 12 is for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 14 shows the solder-mask land pattern for the PWP package. The minimum recommended heatsink area also is shown. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 10, 11, and 20.

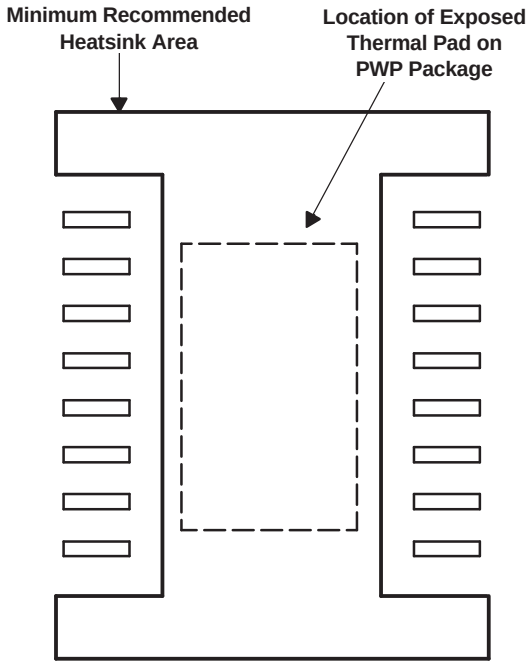


Figure 14. PWP Package Land Pattern

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75125MPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	75125MEP	Samples
V62/03636-14XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	75125MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS75125-EP :

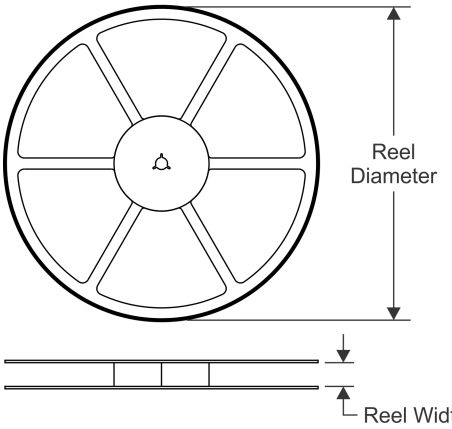
- Catalog: TPS75125

NOTE: Qualified Version Definitions:

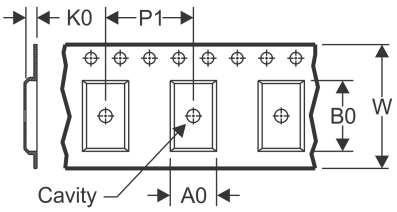
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

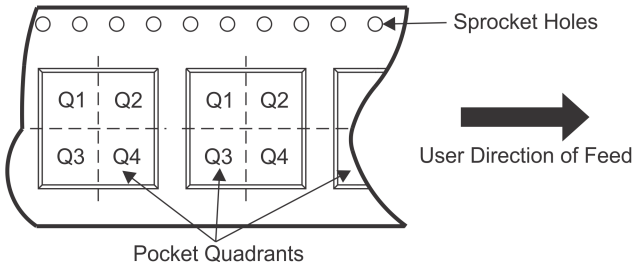


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

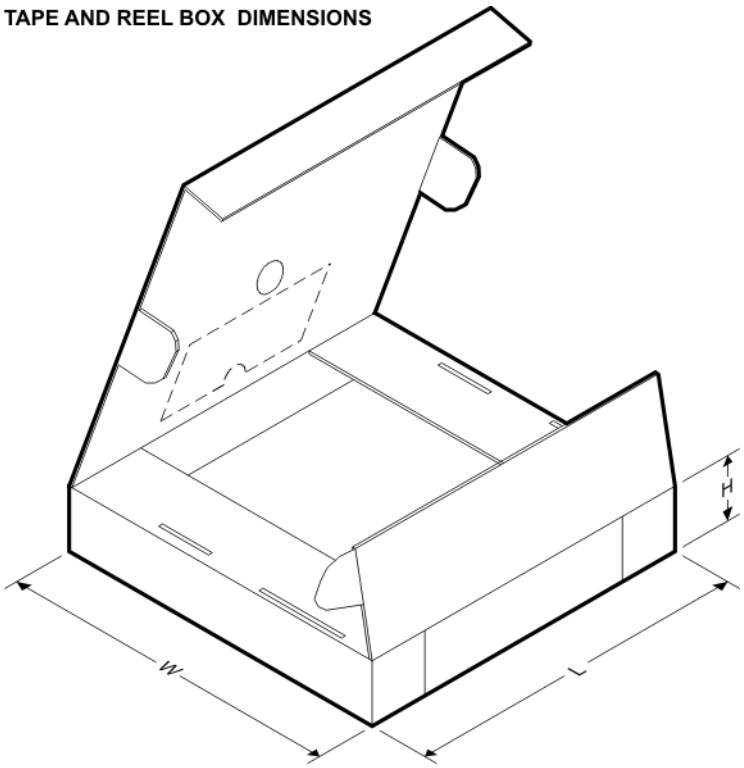
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75125MPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

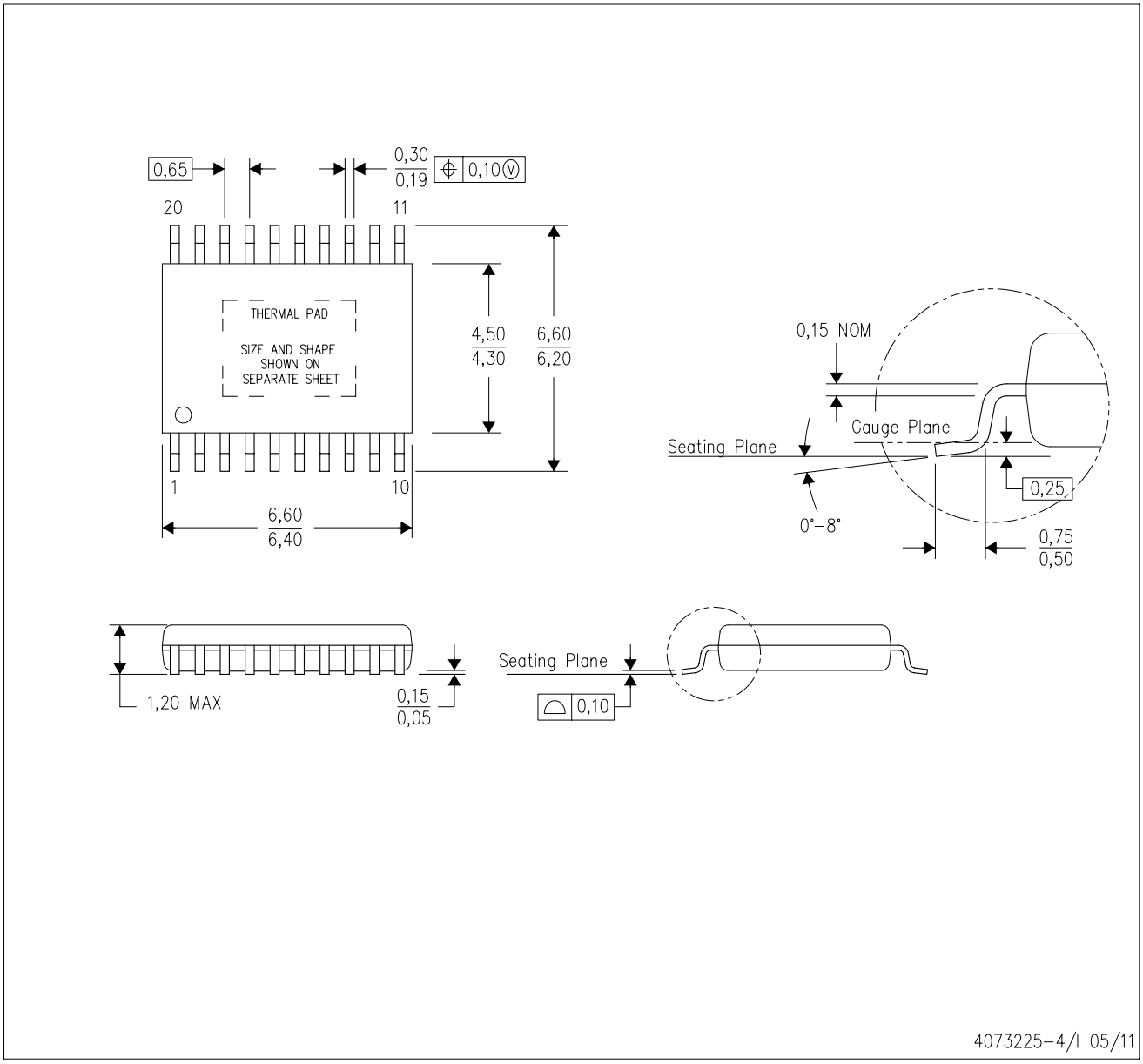
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75125MPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

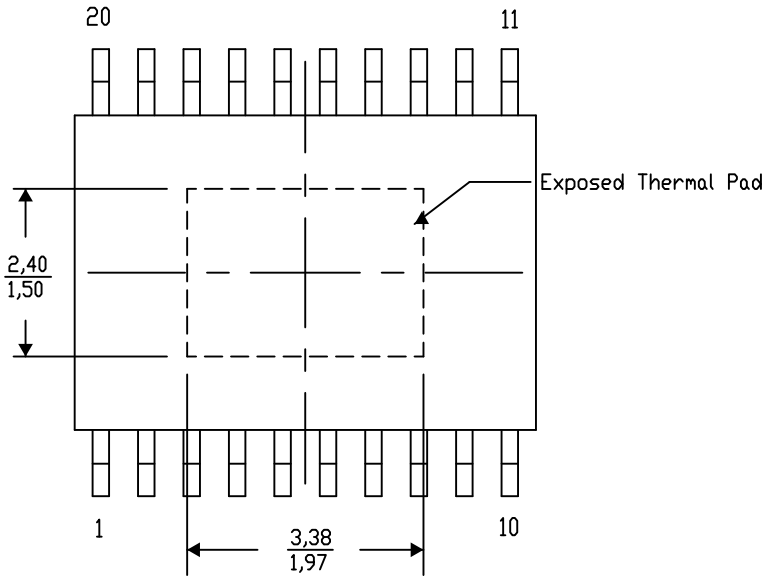
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

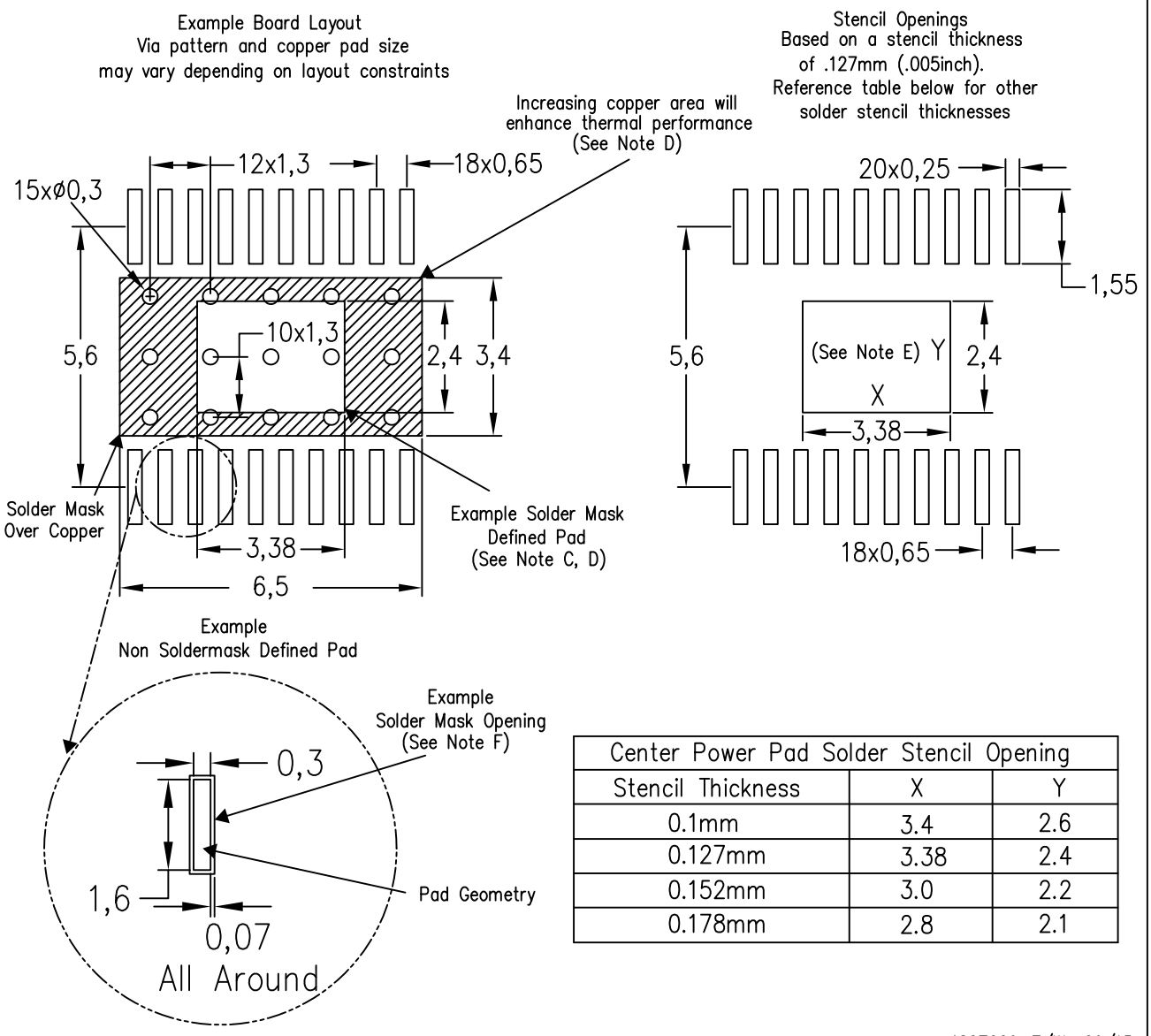
Exposed Thermal Pad Dimensions

4206332–19/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.4	2.6
0.127mm	3.38	2.4
0.152mm	3.0	2.2
0.178mm	2.8	2.1

4207609–7/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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