



**THE DATASHEET OF
SN74CB3T16211GQLR**



24-BIT FET BUS SWITCH

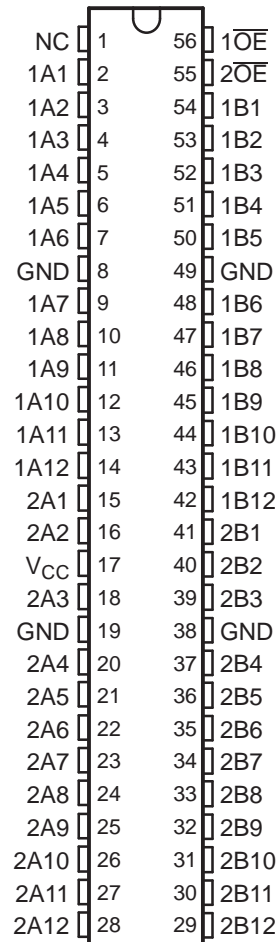
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

Check for Samples: [SN74CB3T16211](#)

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
 - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V V_{CC}
 - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 5 \Omega$ Typ)
- Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)} = 5 \text{ pF}$ Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 70 \mu\text{A}$ Max)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, PCI Interface, Bus Isolation
- Ideal for Low-Power Portable Equipment

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC - No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

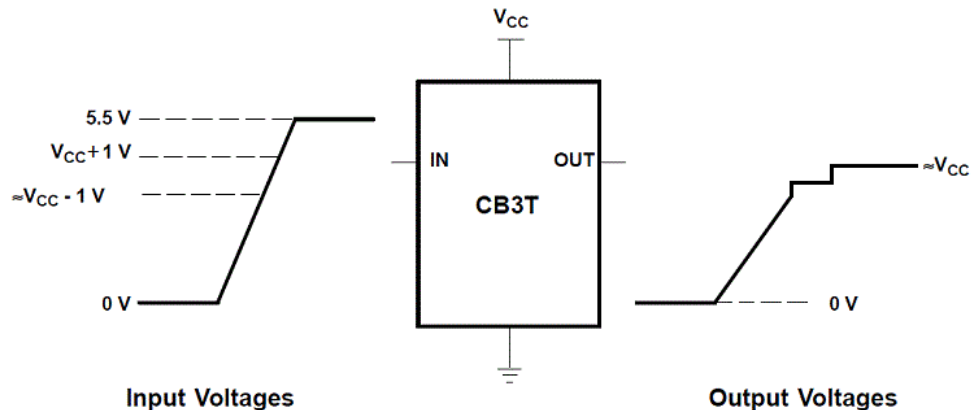
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DESCRIPTION/ORDERING INFORMATION

The SN74CB3T16211 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T16211 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

DESCRIPTION/ORDERING INFORMATION (CONTINUED)



If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} + 1V$, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

The I/O port of this device has a pullup current source that maintains the output voltage at V_{CC} when the device is ON, and the input is greater than or equal to $V_{CC} - 1$. Because of the pullup current source, the output voltage level may be less than V_{CC} when the operating frequency is low and the I/O port is connected to a pulldown resistor. In order to maintain the output voltage at V_{CC} , a pullup resistor must be connected to V_{CC} instead of a pulldown resistor to ground.

The SN74CB3T16211 is organized as two 12-bit bus switches with separate output-enable ($\overline{1OE}$, $\overline{2OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-----------------------|------------------------|-------------------|-----------------------|------------------|
| -40°C to 85°C | SSOP – DL | Tube | SN74CB3T16211DL | CB3T16211 |
| | | Tape and reel | SN74CB3T16211DLR | |
| | TSSOP – DGG | Tube | SN74CB3T16211DGG | CB3T16211 |
| | | Tape and reel | SN74CB3T16211DGGR | |
| | TVSOP – DGV | Tape and reel | SN74CB3T16211DGVR | KR211 |
| | VFBGA – GQL (Pb-free) | Tape and reel | SN74CB3T16211GQLR | KR211 |
| VFBGA – ZQL (Pb-free) | Tape and reel | SN74CB3T16211ZQLR | KR211 | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

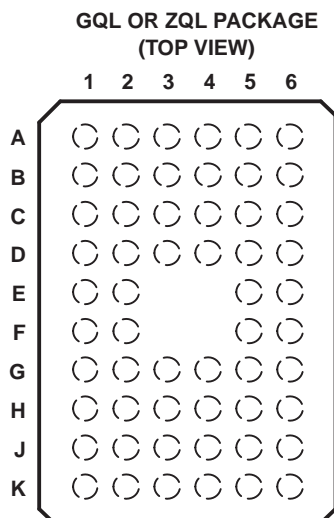


Table 2. TERMINAL ASSIGNMENTS

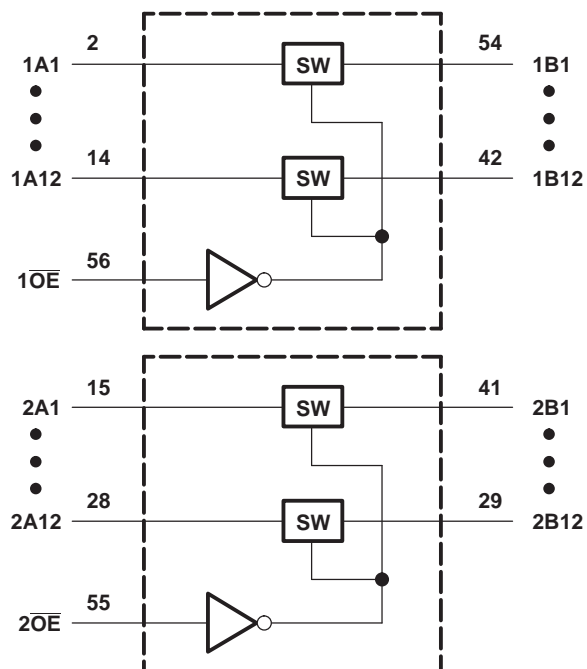
| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----------------|------|-------------------|-------------------|-------------------|------|
| A | 1A2 | 1A1 | NC ⁽¹⁾ | 1 \overline{OE} | 2 \overline{OE} | 1B1 |
| B | 1A5 | 1A4 | 1A3 | 1B2 | 1B3 | 1B4 |
| C | 1A7 | GND | 1A6 | 1B5 | GND | 1B6 |
| D | 1A10 | 1A8 | 1A9 | 1B8 | 1B7 | 1B9 |
| E | 1A12 | 1A11 | | | 1B10 | 1B11 |
| F | 2A1 | 2A2 | | | 2B1 | 1B12 |
| G | V _{CC} | GND | 2A3 | 2B3 | GND | 2B2 |
| H | 2A4 | 2A5 | 2A6 | 2B6 | 2B5 | 2B4 |
| J | 2A7 | 2A8 | 2A9 | 2B9 | 2B8 | 2B7 |
| K | 2A10 | 2A11 | 2A12 | 2B12 | 2B11 | 2B10 |

(1) NC – No internal connection

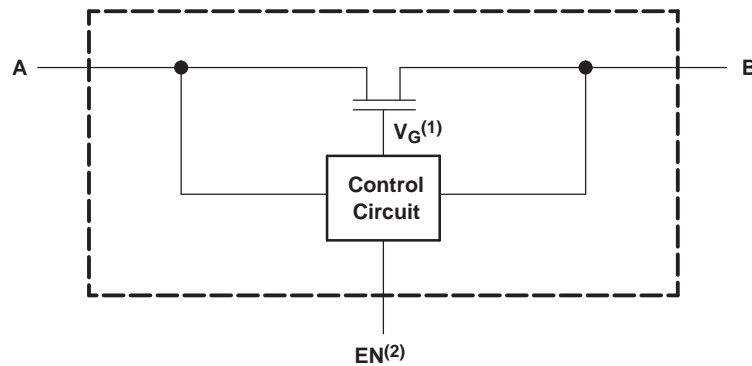
**Table 3. FUNCTION TABLE
(EACH 12-BIT BUS SWITCH)**

| INPUT \overline{OE} | INPUT/OUTPUT A | FUNCTION |
|--------------------------|-------------------|-----------------|
| L | B | A port = B port |
| H | Z | Disconnect |

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



- (1) Gate voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
 (2) Internal enable signal applied to the switch

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-----------------|------|------|
| V_{CC} | Supply voltage range ⁽²⁾ | -0.5 | 7 | V |
| V_{IN} | Control input voltage range ⁽²⁾ (3) | -0.5 | 7 | V |
| $V_{I/O}$ | Switch I/O voltage range ⁽²⁾ (3) (4) | -0.5 | 7 | V |
| I_{IK} | Control input clamp current | $V_{IN} < 0$ | -50 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{I/O} < 0$ | -50 | mA |
| $I_{I/O}$ | ON-state switch current ⁽⁵⁾ | | ±128 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁶⁾ | DGG package | 64 | °C/W |
| | | DGV package | 48 | |
| | | DL package | 56 | |
| | | GQL/ZQL package | 42 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 (2) All voltages are with respect to ground, unless otherwise specified.
 (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 (4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 (5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------|----------------------------------|---------------------------|-----|------|---|
| V_{CC} | Supply voltage | 2.3 | 3.6 | V | |
| V_{IH} | High-level control input voltage | $V_{CC} = 2.3$ V to 2.7 V | 1.7 | 5.5 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2 | 5.5 | |
| V_{IL} | Low-level control input voltage | $V_{CC} = 2.3$ V to 2.7 V | 0 | 0.7 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 0 | 0.8 | |
| $V_{I/O}$ | Data input/output voltage | 0 | 5.5 | V | |
| T_A | Operating free-air temperature | -40 | 85 | °C | |

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT | |
|--------------------------------|----------------|---|--|--------------------|------|------|---|
| V_{IK} | | $V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | V | |
| V_{OH} | | See Figure 3 and Figure 4 | | | | | |
| I_{IN} | Control inputs | $V_{CC} = 3.6\text{ V}$, $V_{IN} = 3.6\text{ V to } 5.5\text{ V or GND}$ | | | ±10 | µA | |
| I_I | | $V_{CC} = 3.6\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND | $V_I = V_{CC} - 0.7\text{ V to } 5.5\text{ V}$ | | ±20 | µA | |
| | | | $V_I = 0.7\text{ V to } V_{CC} - 0.7\text{ V}$ | | -40 | | |
| | | | $V_I = 0\text{ to } 0.7\text{ V}$ | | ±5 | | |
| I_{OZ} ⁽³⁾ | | $V_{CC} = 3.6\text{ V}$, $V_O = 0\text{ to } 5.5\text{ V}$, $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND | | | ±10 | µA | |
| I_{off} | | $V_{CC} = 0$, $V_O = 0\text{ to } 5.5\text{ V}$, $V_I = 0$ | | | 10 | µA | |
| I_{CC} | | $V_{CC} = 3.6\text{ V}$, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND | $V_I = V_{CC}$ or GND | | 70 | µA | |
| | | | $V_I = 5.5\text{ V}$ | | 70 | | |
| ΔI_{CC} ⁽⁴⁾ | Control inputs | $V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND | | | 300 | µA | |
| C_{in} | Control inputs | $V_{CC} = 3.3\text{ V}$, $V_{IN} = V_{CC}$ or GND | | 4 | | pF | |
| $C_{io(OFF)}$ | | $V_{CC} = 3.3\text{ V}$, $V_{I/O} = 5.5\text{ V}$, 3.3 V , or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND | | 5 | | pF | |
| $C_{io(ON)}$ | | $V_{CC} = 3.3\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND | $V_{I/O} = 5.5\text{ V or } 3.3\text{ V}$ | | 5 | pF | |
| | | | $V_{I/O} = \text{GND}$ | | 13 | | |
| r_{on} ⁽⁵⁾ | | $V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$, $V_I = 0$ | $I_O = 24\text{ mA}$ | | 5 | 9.5 | Ω |
| | | | $I_O = 16\text{ mA}$ | | 5 | 9.5 | |
| | | $V_{CC} = 3\text{ V}$, $V_I = 0$ | $I_O = 64\text{ mA}$ | | 5 | 8.5 | |
| | | | $I_O = 32\text{ mA}$ | | 5 | 8.5 | |

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

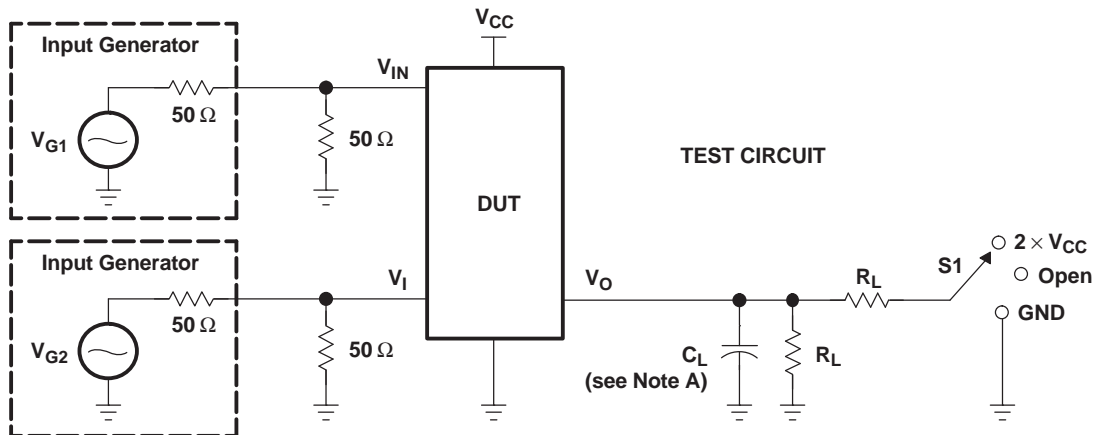
Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

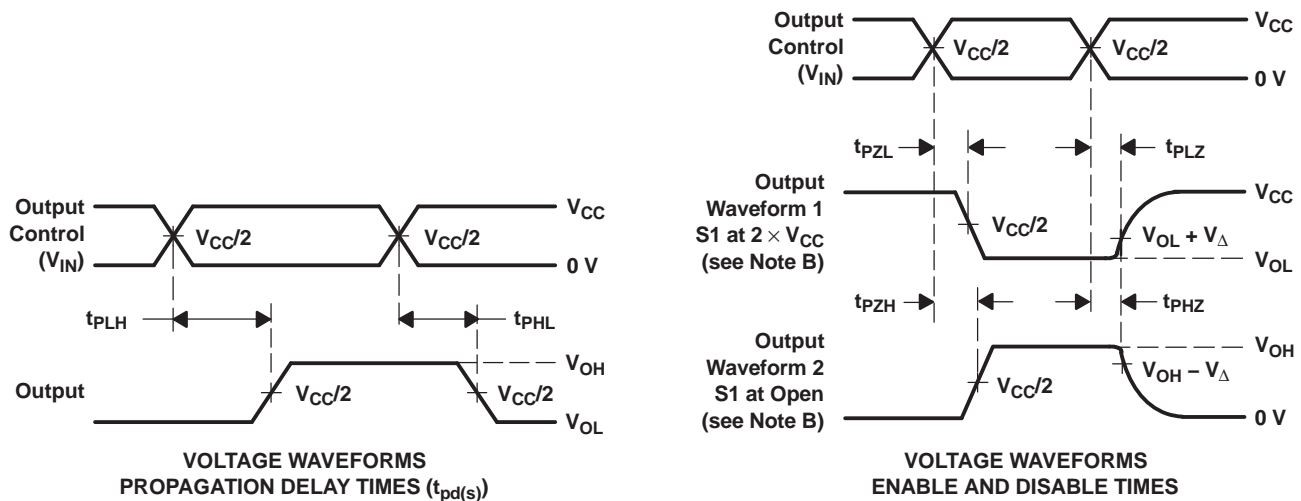
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | UNIT |
|-------------------------|-----------------|----------------|---|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{pd} ⁽¹⁾ | A or B | B or A | 0.15 | | 0.25 | | ns |
| t_{en} | \overline{OE} | A or B | 1 | 12 | 1 | 10 | ns |
| t_{dis} | \overline{OE} | A or B | 1 | 7.5 | 1 | 8.5 | ns |

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



| TEST | V _{CC} | S1 | R _L | V _I | C _L | V _Δ |
|------------------------------------|-----------------|---------------------|----------------|----------------|----------------|----------------|
| t _{pd(s)} | 2.5 V ± 0.2 V | Open | 500 Ω | 3.6 V or GND | 30 pF | |
| | 3.3 V ± 0.3 V | Open | 500 Ω | 5.5 V or GND | 50 pF | |
| t _{PLZ} /t _{PZL} | 2.5 V ± 0.2 V | 2 × V _{CC} | 500 Ω | GND | 30 pF | 0.15 V |
| | 3.3 V ± 0.3 V | 2 × V _{CC} | 500 Ω | GND | 50 pF | 0.3 V |
| t _{PHZ} /t _{PZH} | 2.5 V ± 0.2 V | Open | 500 Ω | 3.6 V | 30 pF | 0.15 V |
| | 3.3 V ± 0.3 V | Open | 500 Ω | 5.5 V | 50 pF | 0.3 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

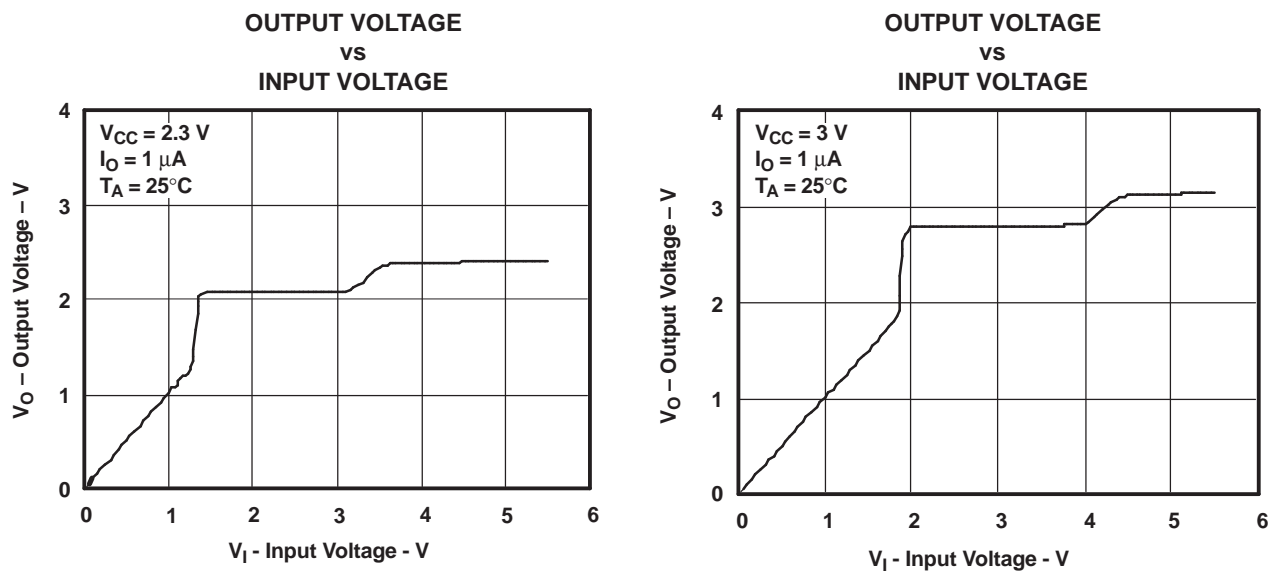
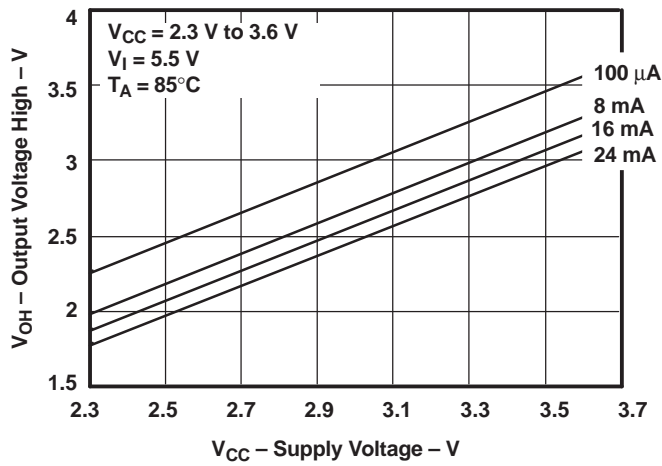


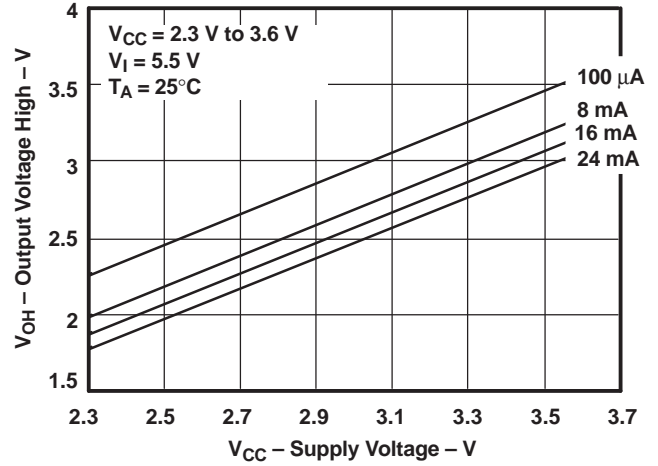
Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

**OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE**



**OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE**



**OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE**

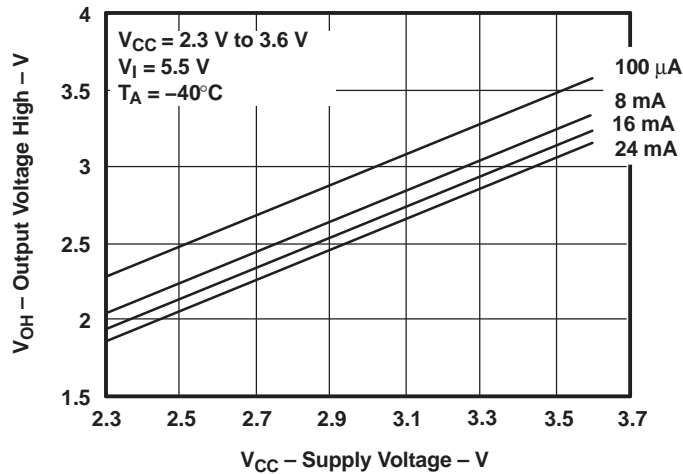


Figure 4. V_{OH} Values

REVISION HISTORY

| Changes from Revision B (January 2006) to Revision C | Page |
|---|-------------------|
| • Updated graphic and note in figure 1. | 2 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|----------------------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74CB3T16211DGGRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16211 | Samples |
| SN74CB3T16211DGGR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16211 | Samples |
| SN74CB3T16211DGVR | ACTIVE | TVSOP | DGV | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KR211 | Samples |
| SN74CB3T16211DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16211 | Samples |
| SN74CB3T16211DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T16211 | Samples |
| SN74CB3T16211ZQLR | LIFEBUY | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | KR211 | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CB3T16211DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74CB3T16211ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.5 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| SN74CB3T16211DLR | SSOP | DL | 56 | 1000 | 367.0 | 367.0 | 55.0 |
| SN74CB3T16211ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 350.0 | 350.0 | 43.0 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



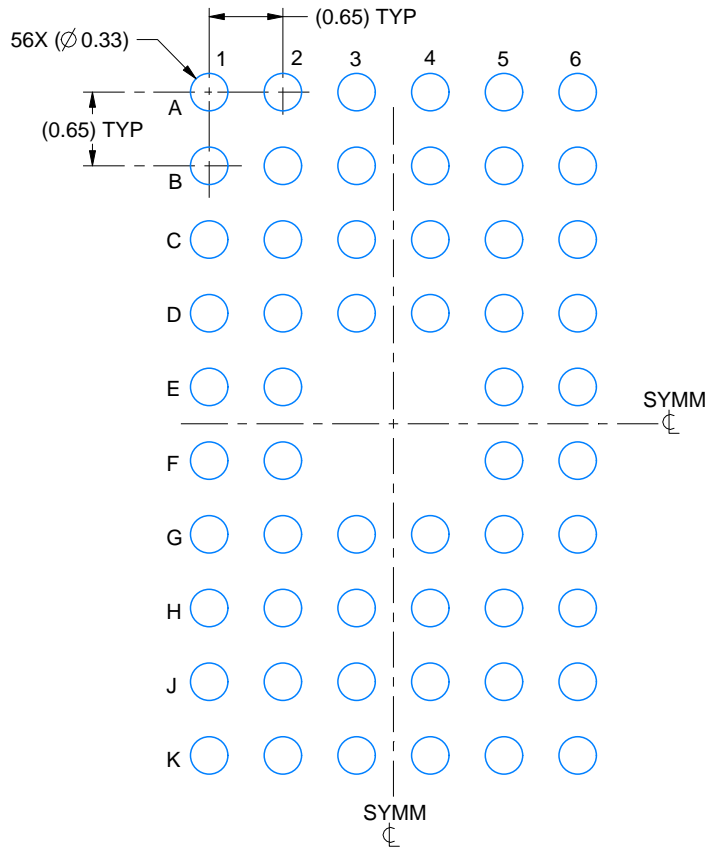
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

EXAMPLE BOARD LAYOUT

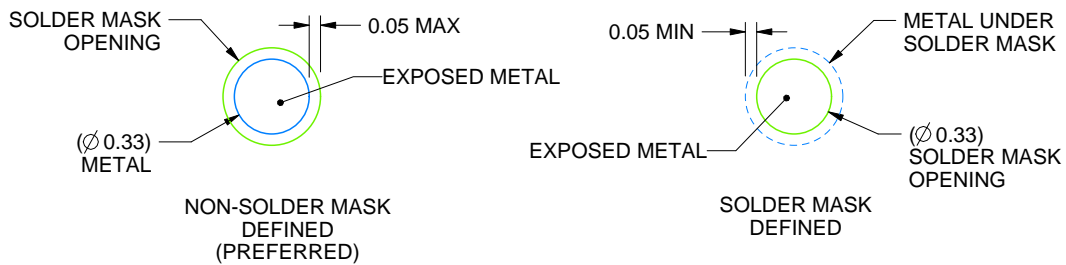
ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

4219711/B 01/2017

NOTES: (continued)

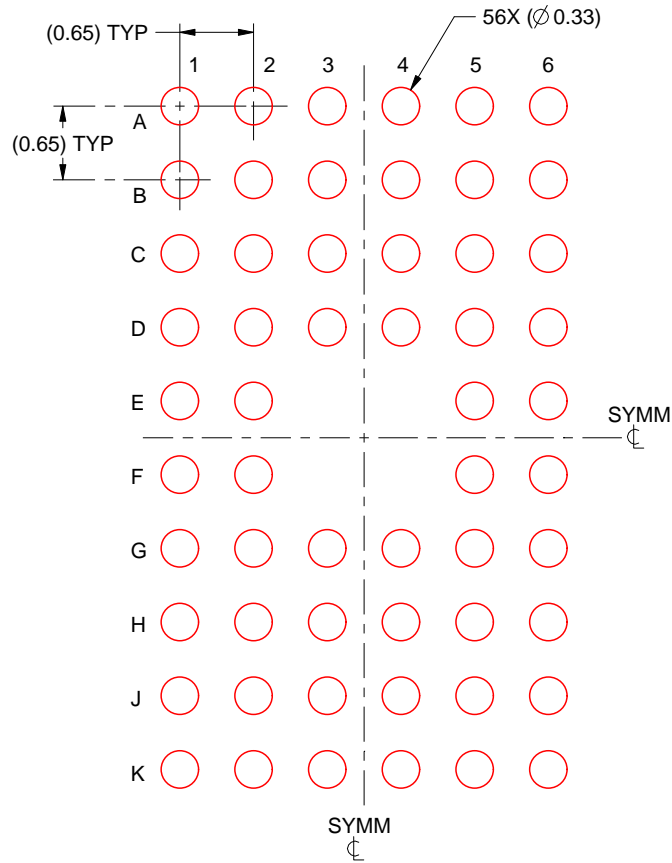
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4219711/B 01/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

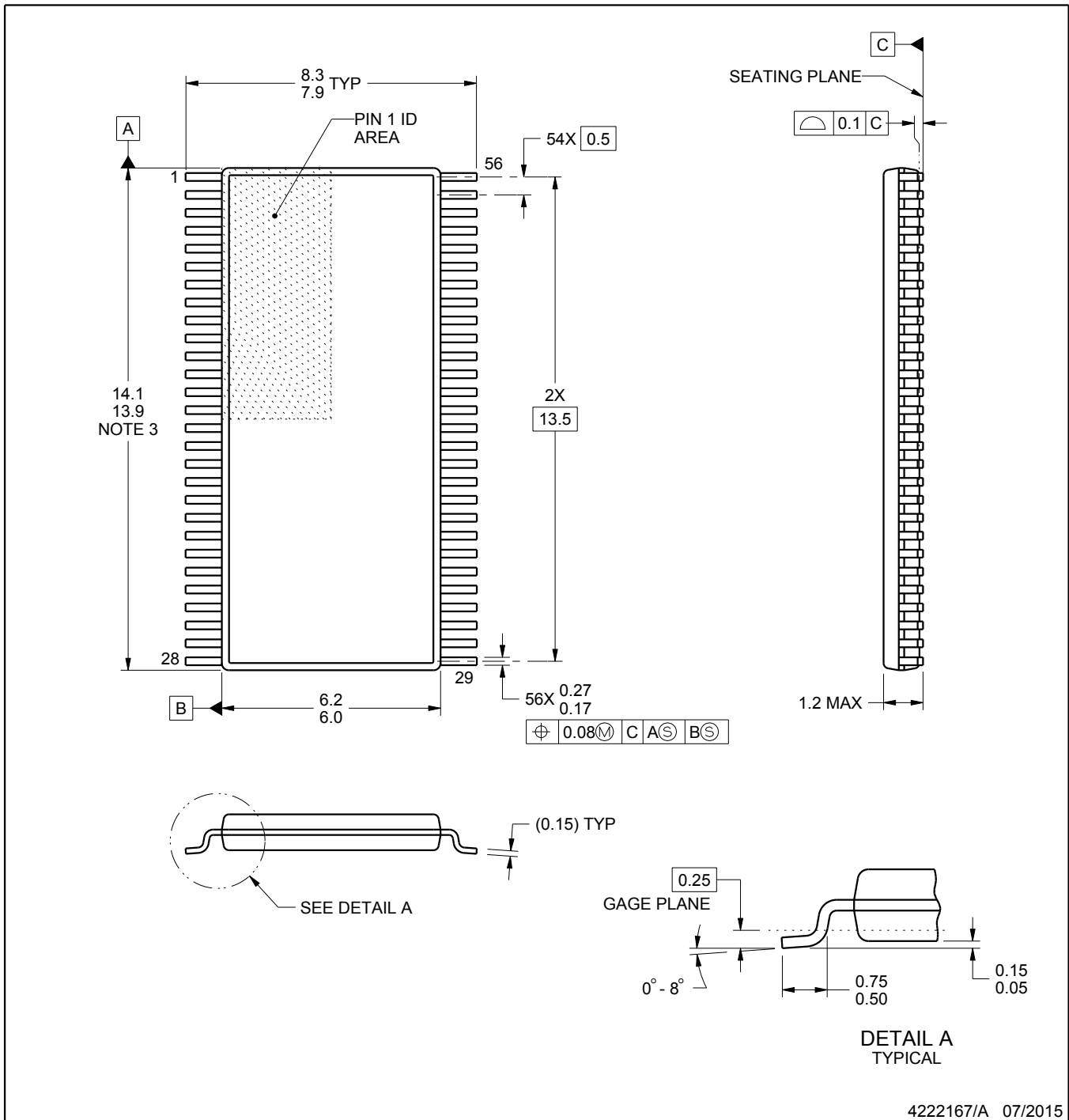
DGG0056A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

NOTES:

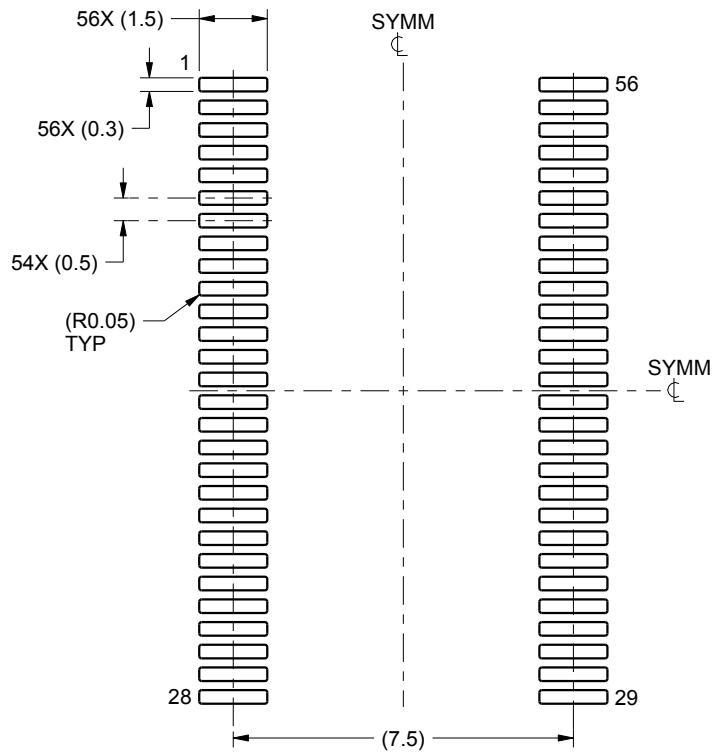
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

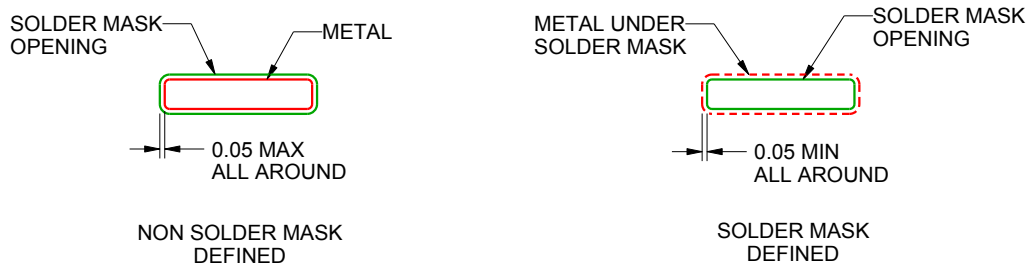
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

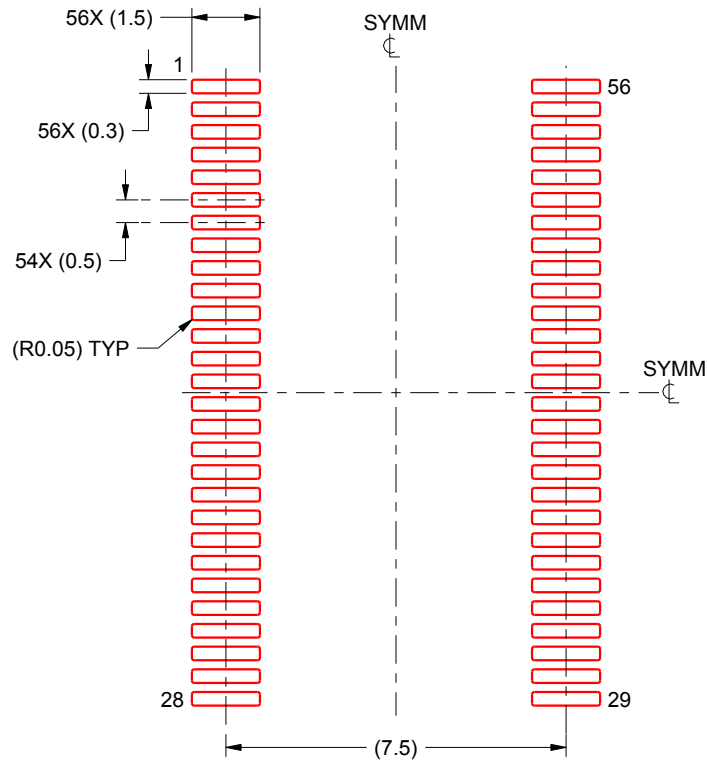
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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