



# AK5703

## 4-Channel 24-bit ADC with PLL & MIC-AMP

### GENERAL DESCRIPTION

The AK5703 is a 4-channel 24-bit A/D converter with programmable microphone amplifiers and ALC (Automatic Level Control) circuit. It is designed for consumer microphone array applications. An integrated PLL operates from a wide variety of clocks, enabling high design flexibility. Microphone power outputs are included for biasing external microphones. Wide dynamic range is achieved, at 83dB with a microphone gain setting of +30dB. The AK5703 is packaged in a space-saving 28-pin QFN package.

### FEATURES

1. **Recording Function**
  - 4-Channel ADC
  - Full-differential or Single-ended Input
  - Microphone Amplifier (+36dB/+30dB/+24dB/+18dB/+15dB/+12dB/+8dB/0dB)
  - Input Voltage: 1.8Vpp@AVDD=3.0V (= 0.6 x AVDD)
  - ADC Performance:
    - S/(N+D): 85dB, DR, S/N: 96dB@MGAIN=0dB, Single-ended Input
    - S/(N+D): 78dB, DR, S/N: 83dB@MGAIN=+30dB, Full Differential Input
  - Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)
  - Microphone Sensitivity Correction (+3dB ~ -3dB, 0.75dB Step)
  - Digital ALC (Automatic Level Control)
  - Input Digital Volume (+36dB ~ -52.5dB, 0.375dB Step, Mute)
  - Programmable Output Data Delay
    - Delay Time: 0 to 64/64fs (1/64fs Step)
2. **Sampling Frequency:**
  - PLL Slave Mode (BICK pin): 8kHz ~ 48kHz
  - PLL Slave Mode (MCKI pin):
    - 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
  - PLL Master Mode:
    - 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
  - EXT Master/Slave Mode:
    - 8kHz ~ 48kHz (256fs), 8kHz ~ 24kHz (512fs), 8kHz ~ 12kHz (1024fs)
3. **PLL Input Clock:**
  - MCKI pin:
    - 27MHz, 26MHz, 24MHz, 19.2MHz, 13.5MHz, 13MHz, 12.288MHz, 12MHz, 11.2896MHz
  - BICK pin: 32fs/64fs
4. **Master/Slave Mode**
5. **Audio Interface Format: MSB First, 2's complement**
  - 24/16-bit MSB justified, 24/16-bit I<sup>2</sup>S, TDM Mode
6. **μP I/F: 3-wire Serial Control or I<sup>2</sup>C Bus (Ver 1.0, 400kHz Mode)**
7. **Power Supply:**
  - AVDD: 2.4 ~ 3.6V
  - DVDD: 1.6 ~ 1.98V
  - TVDD: 1.6 or (DVDD-0.2) ~ 3.6V
8. **Power Supply Current: 9.0mA (EXT Slave Mode)**
9. **Ta = -30 ~ 85°C**
10. **Package: 28pin QFN (4mm x 4mm, 0.4mm pitch)**

■ Block Diagram

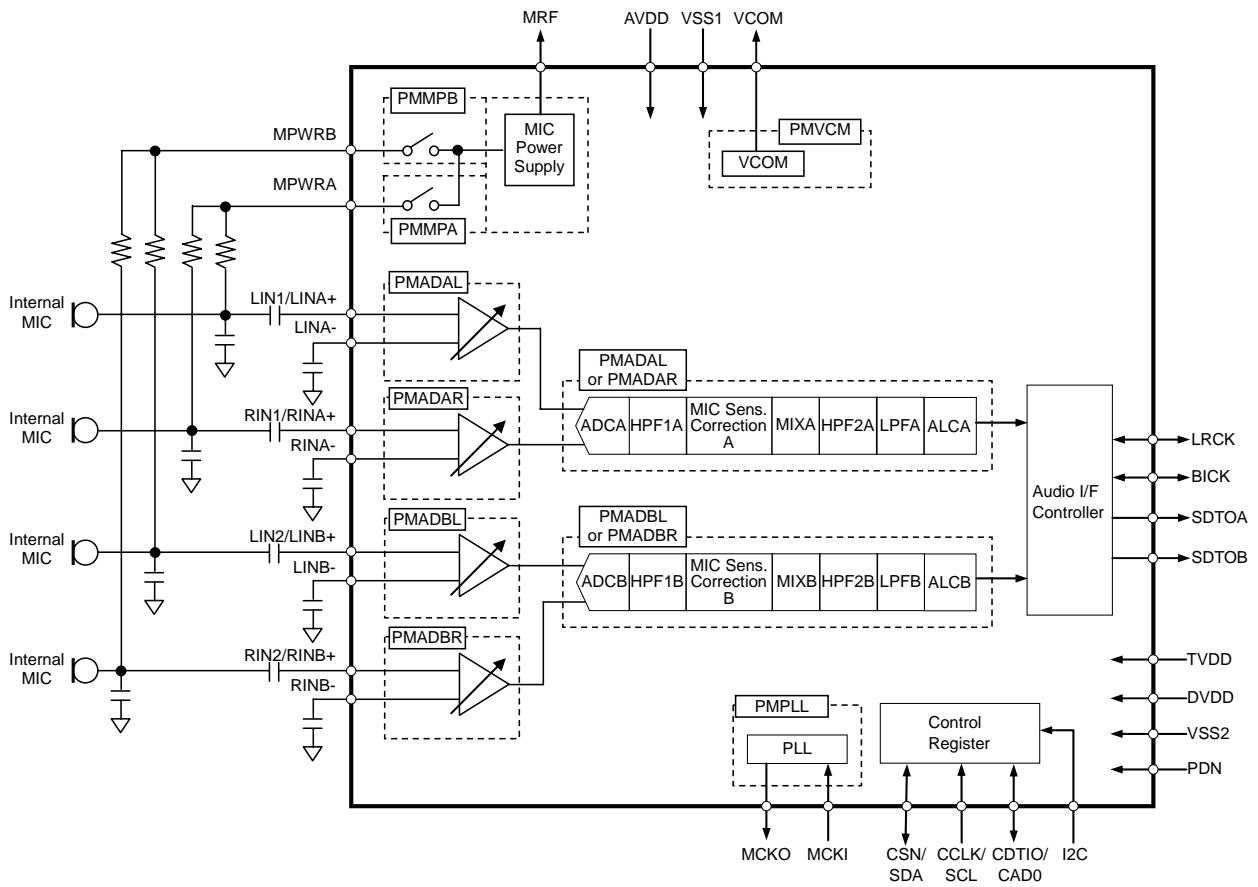


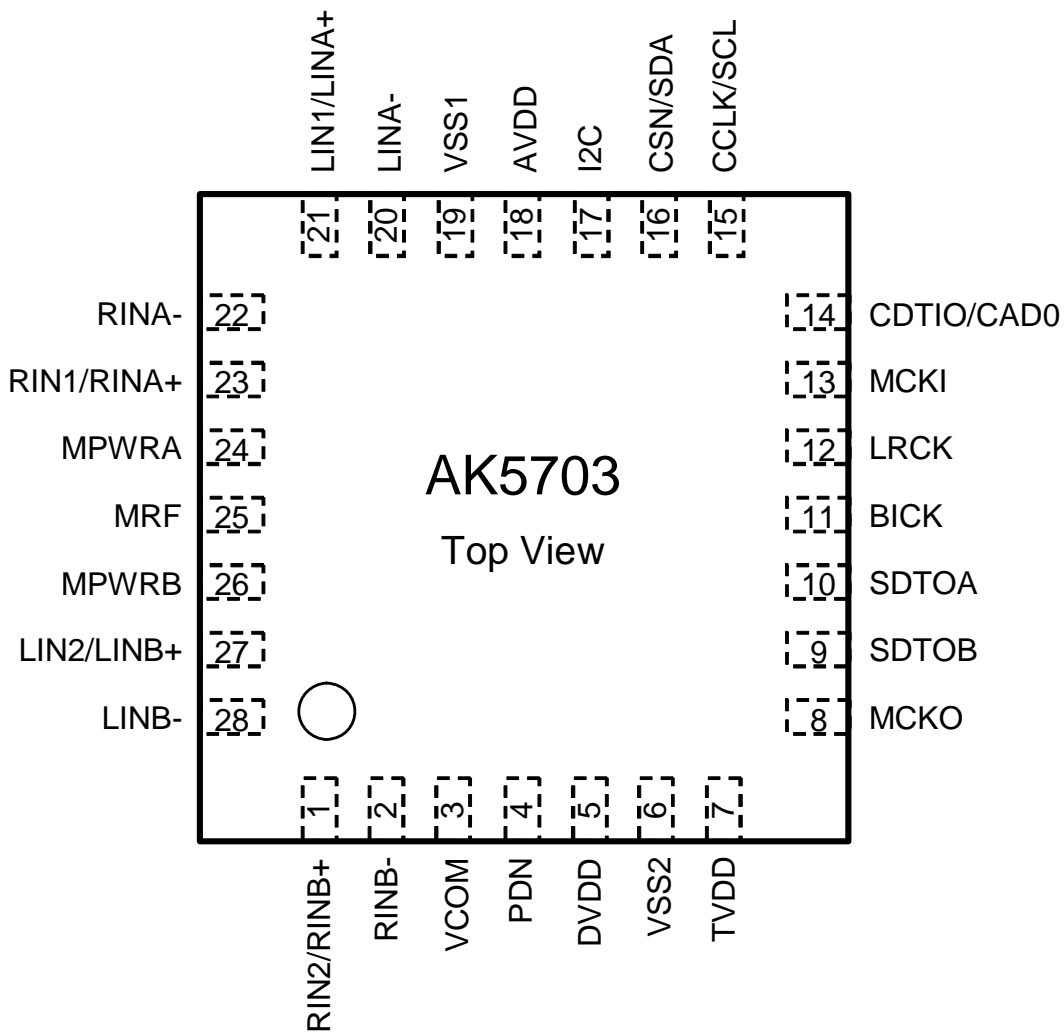
Figure 1. Block Diagram

■ Ordering Guide

AK5703EN  
AKD5703

-30 ~ +85°C      28pin QFN (0.4mm pitch)  
Evaluation Board for AK5703

■ Pin Layout



### ■ Comparison with AK5702

| Function                          |                  | AK5702                                | AK5703  |
|-----------------------------------|------------------|---------------------------------------|---|
| ADC Resolution                    |                  | 16-bit                                | 24-bit  |
| 3:1 Stereo Input Selector         |                  | Yes                                   | No  |
| MIC Amplifier                     | Gain             | +36dB, +30dB, +15dB, 0dB              | +36dB, +30dB, +24dB, +18dB, +15dB, +12dB, +8dB, 0dB |
|                                   | Input Resistance | 30kΩ<br>@MGAIN=+15dB, +30dB, +36dB    | 100kΩ   |
| DR, S/N (Full Differential Input) |                  | 74dB@MGAIN=+30dB                      | 83dB@MGAIN=+30dB                                    |
| Audio Interface                   | DSP Mode         | Yes                                   | No  |
|                                   | TDM Mode         | Yes                                   | Yes   |
|                                   | Cascade TDM Mode | Yes                                   | No  |
| MIC Sensitivity Correction        |                  | No                                    | Yes (+3dB ~ -3dB)                                   |
| Programmable Output Data Delay    |                  | No                                    | Yes (0 ~ 64/64fs)                                   |
| PLL                               | LRCK Reference   | Yes                                   | No  |
|                                   | VCOC pin         | Yes                                   | No  |
| Package                           |                  | 32pin QFN<br>(5mm x 5mm, 0.5mm pitch) | 28pin QFN<br>(4mm x 4mm, 0.4mm pitch)               |

| PIN/FUNCTION |          |     |  |
|--------------|----------|-----|--|
| No.          | Pin Name | I/O | Function   |
| 1            | RIN2     | I   | Rch Analog Input 2 Pin (MDIFB bit = "0": Single-ended Input)   |
|              | RINB+    | I   | Rch Positive Input B Pin (MDIFB bit = "1": Full-differential Input)  |
| 2            | RINB-    | I   | Rch Negative Input B Pin (MDIFB bit = "0": Single-ended Input)<br>This pin must be connected to VSS1 with a capacitor in series. (Refer to <a href="#">Figure 50</a> ) |
|              |          |     | Rch Negative Input B Pin Rch Negative Input B Pin  |
| 3            | VCOM     | O   | Common Voltage Output Pin, 0.5 x AVDD<br>Bias voltage of ADC inputs.<br>This pin must be connected to VSS1 with 1μF±50% capacitor in series.                           |
| 4            | PDN      | I   | Power-Down Mode Pin<br>"H": Power-up, "L": Power-down, reset and initializes the control register.   |
| 5            | DVDD     | -   | Digital Power Supply Pin, 1.6 ~ 1.98V  |
| 6            | VSS2     | -   | Digital Ground Pin   |
| 7            | TVDD     | -   | Digital I/O Power Supply Pin, 1.6 ~ 3.6V   |
| 8            | MCKO     | O   | Master Clock Output Pin  |
| 9            | SDTOB    | O   | ADCB/TDM Audio Serial Data Output Pin  |
| 10           | SDTOA    | O   | ADCA Audio Serial Data Output Pin  |
| 11           | BICK     | I/O | Audio Serial Data Clock Pin  |
| 12           | LRCK     | I/O | Input / Output Channel Clock Pin   |
| 13           | MCKI     | I   | External Master Clock Input Pin  |
| 14           | CDTIO    | I/O | Control Data Input/Output Pin (I2C pin = "L": 3-wire Serial Mode)  |
|              | CAD0     | I   | Chip Address 0 Select Pin (I2C pin = "H": I <sup>2</sup> C Bus Mode)   |
| 15           | CCLK     | I   | Control Data Clock Pin (I2C pin = "L": 3-wire Serial Mode)   |
|              | SCL      | I   | Control Data Clock Pin (I2C pin = "H": I <sup>2</sup> C Bus Mode)  |
| 16           | CSN      | I   | Chip Select Pin (I2C pin = "L": 3-wire Serial Mode)  |
|              | SDA      | I/O | Control Data Input Pin (I2C pin = "H": I <sup>2</sup> C Bus Mode)  |
| 17           | I2C      | I   | Control Mode Select Pin<br>"H": I <sup>2</sup> C, "L": 3-wire serial   |
| 18           | AVDD     | -   | Analog Power Supply Pin, 2.4 ~ 3.6V  |
| 19           | VSS1     | -   | Analog Ground Pin  |
| 20           | LINA-    | I   | Lch Negative Input A Pin (MDIFA bit = "0": Single-ended Input)<br>This pin must be connected to VSS1 with a capacitor in series. (Refer to <a href="#">Figure 50</a> ) |
|              |          |     | Lch Negative Input A Pin (MDIFA bit = "1": Full-differential Input)  |
| 21           | LIN1     | I   | Lch Analog Input 1 Pin (MDIFA bit = "0": Single-ended Input)   |
|              |          |     | Lch Positive Input A Pin (MDIFA bit = "1": Full-differential Input)  |
| 22           | RINA-    | I   | Rch Negative Input A Pin (MDIFA bit = "0": Single-ended Input)<br>This pin must be connected to VSS1 with a capacitor in series. (Refer to <a href="#">Figure 50</a> ) |
|              |          |     | Rch Negative Input A Pin (MDIFB bit = "1": Full-differential Input)  |
| 23           | RIN1     | I   | Rch Analog Input 1 Pin (MDIFA bit = "0": Single-ended Input)   |
|              |          |     | Rch Positive Input A Pin (MDIFA bit = "1": Full-differential Input)  |
| 24           | MPWRA    | O   | Microphone Power Supply A Pin  |
| 25           | MRF      | O   | Microphone Power Supply Ripple Filter Pin<br>This pin must be connected to VSS1 with 1μF±50% capacitor in series.  |
| 26           | MPWRB    | O   | Microphone Power Supply B Pin  |
| 27           | LIN2     | I   | Lch Analog Input 2 Pin (MDIFB bit = "0": Single-ended Input)   |
|              |          |     | Lch Positive Input B Pin (MDIFB bit = "1": Full-differential Input)  |
| 28           | LINB-    | I   | Lch Negative Input B Pin (MDIFB bit = "0": Single-ended Input)<br>This pin must be connected to VSS1 with a capacitor in series. (Refer to <a href="#">Figure 50</a> ) |
|              |          |     | Lch Negative Input B Pin (MDIFB bit = "1": Full-differential Input)  |

Note 1. All input pins except analog input pins (LIN1-2, RIN1-2, LINA+/-, RINA+/-, LINB+/-, RINB+/-) must not be allowed to float.

## ■ Handling of Unused Pin

The unused I/O pins must be connected appropriately.

| Classification | Pin Name  | Setting                                     |
|----------------|---|---|
| Analog         | MPWRA, MPWRB, MRF,<br>LIN1/LINA+, LINA-, RIN1/RINA+, RINA-,<br>LIN2/LINB+, LINB-, RIN2/RINB+, RINB- | Open  |
|                | LINA-, RINA-, LINB-, RINB-<br>(When single-ended inputs are used.)                                  | Connect to VSS1 with a capacitor in series. |
| Digital        | SDTOA, SDTOB, MCKO  | Open  |
|                | MCKI  | Connect to VSS2                             |

### ABSOLUTE MAXIMUM RATINGS

(VSS1, VSS2 = 0V; Note 2)

| Parameter                              | Symbol | min  | max      | Unit |
|--|--------|------|----------|------|
| Power Supplies:                        |        |      |          |      |
| Analog                                 | AVDD   | -0.3 | 6.0      | V    |
| Digital                                | DVDD   | -0.3 | 2.5      | V    |
| Digital I/O                            | TVDD   | -0.3 | 6.0      | V    |
| Input Current, Any Pin Except Supplies | IIN    | -    | ±10      | mA   |
| Analog Input Voltage (Note 3)          | VINA   | -0.3 | AVDD+0.3 | V    |
| Digital Input Voltage (Note 4)         | VIND   | -0.3 | TVDD+0.3 | V    |
| Ambient Temperature (powered applied)  | Ta     | -30  | 85       | °C   |
| Storage Temperature                    | Tstg   | -65  | 150      | °C   |

Note 2. All voltages are with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.

Note 3. LIN1/LINA+, LINA-, RIN1/RINA+, RINA-, LIN2/LINB+, LINB-, RIN2/RINB+, RINB- pins

Note 4. PDN, CSN/SDA, CCLK/SCL, CDTIO/CAD0, MCKI, LRCK, BICK, I2C pins

Pull-up resistors at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

### RECOMMENDED OPERATING CONDITIONS

(VSS1, VSS2=0V; Note 2)

| Parameter            | Symbol | min             | typ | max  | Unit |
|----------------------|--------|-----------------|-----|------|------|
| Power Supplies       |        |                 |     |      |      |
| Analog               | AVDD   | 2.4             | 3.0 | 3.6  | V    |
| Digital              | DVDD   | 1.6             | 1.8 | 1.98 | V    |
| Digital I/O (Note 6) | TVDD   | 1.6 or DVDD-0.2 | 3.0 | 3.6  | V    |

Note 2. All voltages are with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.

Note 5. The power-up sequence between AVDD, DVDD and TVDD is not critical. The PDN pin must be "L" upon power-up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

Note 6. The minimum value is higher voltage between DVDD-0.2V and 1.6V.

**\* When TVDD is powered ON and the PDN pin is "L", AVDD or DVDD can be powered ON/OFF. The PDN pin must be set to "H" after all power supplies are ON when the AK5703 is powered-up from power-down state.**

\* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

|                               |
|-------------------------------|
| <b>ANALOG CHARACTERISTICS</b> |
|-------------------------------|

(Ta=25°C; AVDD=TVDD=3.0V, DVDD=1.8V; VSS1=VSS2=0V; EXT Slave Mode; MCKI=11.2896MHz, fs=44.1kHz, BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement bandwidth =20Hz ~ 20kHz; unless otherwise specified)

| Parameter  |   | min   | typ   | max   | Unit |
|--|---|-------|-------|-------|------|
| <b>Microphone Amplifier: LIN1/RIN1/LIN2/RIN2 pins</b>  |   |       |       |       |      |
| Input Resistance   |   | 70    | 100   | 130   | kΩ   |
| Gain   | MGAIN2-0 bits = "000"                     | -1    | 0     | +1    | dB   |
|  | MGAIN2-0 bits = "001"                     | +7    | +8    | +9    | dB   |
|  | MGAIN2-0 bits = "010"                     | +11   | +12   | +13   | dB   |
|  | MGAIN2-0 bits = "011"                     | +14   | +15   | +16   | dB   |
|  | MGAIN2-0 bits = "100"                     | +17   | +18   | +19   | dB   |
|  | MGAIN2-0 bits = "101"                     | +23   | +24   | +25   | dB   |
|  | MGAIN2-0 bits = "110"                     | +29   | +30   | +31   | dB   |
|  | MGAIN2-0 bits = "111"                     | +35   | +36   | +37   | dB   |
| <b>Microphone Power Supply: MPWRA, MPWRB pins</b>  |   |       |       |       |      |
| Output Voltage (Note 7)  |   | 2.16  | 2.40  | 2.64  | V    |
| Output Noise Level (A-weighted)  |   | -     | -114  | -     | dBV  |
| PSRR (fin = 1kHz) (Note 8)   |   | -     | 70    | -     | dB   |
| Load Resistance  |   | 0.5   | -     | -     | kΩ   |
| Load Capacitance   |   | -     | -     | 30    | pF   |
| <b>ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2 pins (Single-ended Input) → ADC → Programmable Filter (IVOL=0dB, ALC=OFF) → SDTOA/SDTOB</b> |   |       |       |       |      |
| Resolution   |   | -     | -     | 24    | Bits |
| Input Voltage (Note 9)   | MGAIN= +30dB                              | 0.048 | 0.057 | 0.065 | Vpp  |
|  | MGAIN= 0dB                                | 1.53  | 1.80  | 2.07  | Vpp  |
| S/(N+D) (-1dBFS)   | MGAIN= +30dB                              | 68    | 78    | -     | dB   |
|  | MGAIN= 0dB                                | -     | 85    | -     | dB   |
|  | MGAIN= +30dB<br>(Full Differential Input) | -     | 78    | -     | dB   |
| D-Range<br>(-60dBFS,<br>A-weighted)  | MGAIN= +30dB                              | 73    | 83    | -     | dB   |
|  | MGAIN= 0dB                                | -     | 96    | -     | dB   |
|  | MGAIN= +30dB<br>(Full Differential Input) | -     | 83    | -     | dB   |
| S/N (A-weighted)   | MGAIN= +30dB                              | 73    | 83    | -     | dB   |
|  | MGAIN= 0dB                                | -     | 96    | -     | dB   |
|  | MGAIN= +30dB<br>(Full Differential Input) | -     | 83    | -     | dB   |
| Interchannel Isolation   | MGAIN= +30dB                              | 70    | 80    | -     | dB   |
|  | MGAIN= 0dB                                | -     | 100   | -     | dB   |
| Interchannel<br>Gain Mismatch  | MGAIN= +30dB                              | -     | 0     | 1.0   | dB   |
|  | MGAIN= 0dB                                | -     | 0     | 0.5   | dB   |

Note 7. The output voltage is proportional to AVDD. (typ. 0.8 x AVDD V)

Note 8. PSRR is applied to AVDD with 100mpVpp sine wave.

Note 9. The full-scale input voltage is proportional to AVDD.

Single-ended Input: Vin = 0.6 x AVDD Vpp(typ)

Full Differential Input: Vin = (IN+) - (IN-) = 0.6 x AVDD Vpp(typ)

| Parameter                                       |           | min | typ  | max  | Unit |
|---|-----------|-----|------|------|------|
| <b>Power Supply Current:</b>                    |           |     |      |      |      |
| Power Up (PDN pin = "H", All Circuits Power-up) |           |     |      |      |      |
| AVDD + DVDD + TVDD                              | (Note 10) | -   | 9.0  | -    | mA   |
|   | (Note 11) | -   | 12.0 | 18.0 | mA   |
| Power Down (PDN pin = "L") (Note 12)            |           |     |      |      |      |
| AVDD + DVDD + TVDD                              |           | -   | 0    | 10   | μA   |

Note 10. When EXT Slave Mode (MCKI=11.2896MHz, fs=44.1kHz), and PMADAL = PMADAR = PMADBL = PMADBR = PMVCM = PMMPA = PMMPB bits = "1", PMPLL = M/S = MCKO bits = "0", TDM1-0 bits = "00". In this case, the MPWRA and MPWRB pins output 0mA.

AVDD=7.1mA(typ), DVDD=1.7mA(typ), TVDD=0.2mA(typ).

Note 11. When PLL Master Mode (MCKI=12MHz, fs=44.1kHz), and PMADAL = PMADAR = PMADBL = PMADBR = PMVCM = PMMPA = PMMPB = PMPLL = M/S = MCKO bits = "1", TDM1-0 bits = "11". In this case, the MPWRA and MPWRB pins output 0mA.

AVDD=7.7mA(typ), DVDD=1.8mA(typ), TVDD=2.5mA(typ).

Note 12. All digital input pins are fixed to TVDD or VSS2.

|                               |
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| <b>FILTER CHARACTERISTICS</b> |
|-------------------------------|

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 1.98V; TVDD=1.6 ~ 3.6V; fs=44.1kHz)

| Parameter   | Symbol  | min  | typ | max   | Unit |     |
|---|---------|------|-----|-------|------|-----|
| <b>ADC Digital Filter (Decimation LPF):</b>   |         |      |     |       |      |     |
| Passband (Note 13)  | ±0.16dB | PB   | 0   | -     | 17.3 | kHz |
|   | -0.66dB |      | -   | 19.4  | -    | kHz |
|   | -1.1dB  |      | -   | 19.9  | -    | kHz |
|   | -7.1dB  |      | -   | 22.1  | -    | kHz |
| Stopband (Note 13)  | SB      | 26.1 | -   | -     | kHz  |     |
| Passband Ripple   | PR      | -    | -   | ±0.16 | dB   |     |
| Stopband Attenuation  | SA      | 73   | -   | -     | dB   |     |
| Group Delay (Note 14)   | GD      | -    | 19  | -     | 1/fs |     |
| Group Delay Distortion  | ΔGD     | -    | 0   | -     | μs   |     |
| <b>ADC Digital Filter (HPF): HPFADA=HPFADB bits = "1", HPFA1-0= HPFB1-0 bits = "00"</b> |         |      |     |       |      |     |
| Frequency Response (Note 13)  | -3.0dB  | FR   | -   | 3.4   | -    | Hz  |
|   | -0.5dB  |      | -   | 10    | -    | Hz  |
|   | -0.1dB  |      | -   | 22    | -    | Hz  |

Note 13. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 14. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register.

|                           |
|---------------------------|
| <b>DC CHARACTERISTICS</b> |
|---------------------------|

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 1.98V; TVDD=1.6 ~ 3.6V)

| Parameter  | Symbol | min      | typ | max     | Unit |
|--|--------|----------|-----|---------|------|
| <b>Audio Interface &amp; Serial μP Interface</b><br>(CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, MCKI pins) |        |          |     |         |      |
| High-Level Input Voltage<br>(TVDD ≥ 2.2V)  | VIH    | 70%TVDD  | -   | -       | V    |
| (TVDD < 2.2V)  |        | 80%TVDD  | -   | -       | V    |
| Low-Level Input Voltage<br>(TVDD ≥ 2.2V)   | VIL    | -        | -   | 30%TVDD | V    |
| (TVDD < 2.2V)  |        | -        | -   | 20%TVDD | V    |
| <b>Audio Interface &amp; Serial μP Interface (CDTIO, SDA, MCKO, BICK, LRCK, SDTOA, SDTOB pins Output)</b>            |        |          |     |         |      |
| High-Level Output Voltage<br>(Iout = -80μA)  | VOH    | TVDD-0.2 | -   | -       | V    |
| Low-Level Output Voltage<br>(Except SDA pin : Iout = 80μA)   | VOL1   | -        | -   | 0.2     | V    |
| (SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout = 3mA)  | VOL2   | -        | -   | 0.4     | V    |
| (SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)  | VOL2   | -        | -   | 20%TVDD | V    |
| Input Leakage Current  | Iin    | -        | -   | ±10     | μA   |

|                                  |
|----------------------------------|
| <b>SWITCHING CHARACTERISTICS</b> |
|----------------------------------|

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 1.98V; TVDD=1.6 ~ 3.6V; CL=20pF)

| Parameter   | Symbol                               | min        | typ      | max         | Unit     |   |
|---|--------------------------------------|------------|----------|-------------|----------|---|
| <b>PLL Master Mode (PLL Reference Clock = MCKI pin)</b> |                                      |            |          |             |          |   |
| <b>MCKI Input Timing</b>                                |                                      |            |          |             |          |   |
| Frequency   | fCLK                                 | 11.2896    | -        | 27          | MHz      |   |
| Pulse Width Low   | tCLKL                                | 0.4/fCLK   | -        | -           | s        |   |
| Pulse Width High  | tCLKH                                | 0.4/fCLK   | -        | -           | s        |   |
| <b>MCKO Output Timing</b>                               |                                      |            |          |             |          |   |
| Frequency   | fMCK                                 | 0.256      | -        | 12.288      | MHz      |   |
| Duty Cycle  | dMCK                                 | 40         | 50       | 60          | %        |   |
| <b>LRCK Output Timing</b>                               |                                      |            |          |             |          |   |
| Frequency   | fs                                   | -          | Table 6  | -           | kHz      |   |
| Stereo Mode: Duty Cycle                                 | Duty                                 | -          | 50       | -           | %        |   |
| TDM64, TDM128 Mode:                                     |                                      |            |          |             |          |   |
| I <sup>2</sup> S compatible: Pulse Width Low            | tLRCKL                               | -          | 1/(4fs)  | -           | s        |   |
| MSB justified: Pulse Width High                         | tLRCKH                               | -          | 1/(4fs)  | -           | s        |   |
| <b>BICK Output Timing</b>                               |                                      |            |          |             |          |   |
| Period  | BCKO1-0 bits = "00"                  | tBCK       | -        | 1/(32fs)    | s        |   |
|   | BCKO1-0 bits = "01"                  | tBCK       | -        | 1/(64fs)    | s        |   |
|   | BCKO1-0 bits = "10"<br>(TDM128 Mode) | tBCK       | -        | 1/(128fs)   | s        |   |
| Duty Cycle  | dBCK                                 | -          | 50       | -           | %        |   |
| <b>PLL Slave Mode (PLL Reference Clock = MCKI pin)</b>  |                                      |            |          |             |          |   |
| <b>MCKI Input Timing</b>                                |                                      |            |          |             |          |   |
| Frequency   | fCLK                                 | 11.2896    | -        | 27          | MHz      |   |
| Pulse Width Low   | tCLKL                                | 0.4/fCLK   | -        | -           | s        |   |
| Pulse Width High  | tCLKH                                | 0.4/fCLK   | -        | -           | s        |   |
| <b>MCKO Output Timing</b>                               |                                      |            |          |             |          |   |
| Frequency   | fMCK                                 | 0.256      | -        | 12.288      | MHz      |   |
| Duty Cycle  | dMCK                                 | 40         | 50       | 60          | %        |   |
| <b>LRCK Input Timing</b>                                |                                      |            |          |             |          |   |
| Frequency   | fs                                   | -          | Table 6  | -           | kHz      |   |
| Stereo Mode: Duty Cycle                                 | Duty                                 | 45         | -        | 55          | %        |   |
| TDM64 Mode:   |                                      |            |          |             |          |   |
| I <sup>2</sup> S compatible: Pulse Width Low            | tLRCKL                               | 1/(64fs)   | -        | 63/(64fs)   | s        |   |
| MSB justified: Pulse Width High                         | tLRCKH                               | 1/(64fs)   | -        | 63/(64fs)   | s        |   |
| TDM128 Mode:  |                                      |            |          |             |          |   |
| I <sup>2</sup> S compatible: Pulse Width Low            | tLRCKL                               | 1/(128fs)  | -        | 127/(128fs) | s        |   |
| MSB justified: Pulse Width High                         | tLRCKH                               | 1/(128fs)  | -        | 127/(128fs) | s        |   |
| <b>BICK Input Timing</b>                                |                                      |            |          |             |          |   |
| Period  | Stereo Mode                          | tBCK       | 1/(64fs) | -           | 1/(32fs) | s |
|   | TDM64 Mode                           | tBCK       | -        | 1/(64fs)    | s        |   |
|   | TDM128 Mode                          | tBCK       | -        | 1/(128fs)   | s        |   |
| Pulse Width Low   | tBCKL                                | 0.4 x tBCK | -        | -           | s        |   |
| Pulse Width High  | tBCKH                                | 0.4 x tBCK | -        | -           | s        |   |

| Parameter  | Symbol               | min       | typ        | max         | Unit        |     |
|--|----------------------|-----------|------------|-------------|-------------|-----|
| <b>PLL Slave Mode (PLL Reference Clock = BICK pin)</b> |                      |           |            |             |             |     |
| <b>MCKO Output Timing</b>                              |                      |           |            |             |             |     |
| Frequency  | fMCK                 | 0.256     | -          | 12.288      | MHz         |     |
| Duty Cycle   | dMCK                 | 40        | 50         | 60          | %           |     |
| <b>LRCK Input Timing</b>                               |                      |           |            |             |             |     |
| Frequency  | fs                   | 8         | -          | 48          | kHz         |     |
| Stereo Mode: Duty Cycle                                | Duty                 | 45        | -          | 55          | %           |     |
| TDM64 Mode:  |                      |           |            |             |             |     |
| I <sup>2</sup> S compatible: Pulse Width Low           | tLRCKL               | 1/(64fs)  | -          | 63/(64fs)   | s           |     |
| MSB justified: Pulse Width High                        | tLRCKH               | 1/(64fs)  | -          | 63/(64fs)   | s           |     |
| TDM128 Mode:   |                      |           |            |             |             |     |
| I <sup>2</sup> S compatible: Pulse Width Low           | tLRCKL               | 1/(128fs) | -          | 127/(128fs) | s           |     |
| MSB justified: Pulse Width High                        | tLRCKH               | 1/(128fs) | -          | 127/(128fs) | s           |     |
| <b>BICK Input Timing</b>                               |                      |           |            |             |             |     |
| Period   | Stereo Mode          |           | tBCK       | -           | 1/(32fs)    | s   |
|  | PLL3-0 bits = "0010" |           |            |             |             |     |
|  | PLL3-0 bits = "0011" |           | tBCK       | -           | 1/(64fs)    | s   |
|  | TDM64 Mode           |           | tBCK       | -           | 1/(64fs)    | s   |
| PLL3-0 bits = "0011"                                   |                      |           |            |             |             |     |
| TDM128 Mode  |                      | tBCK      | -          | 1/(128fs)   | s           |     |
| PLL3-0 bits = "0001"                                   |                      |           |            |             |             |     |
| Pulse Width Low  |                      | tBCKL     | 0.4 x tBCK | -           | s           |     |
| Pulse Width High                                       |                      | tBCKH     | 0.4 x tBCK | -           | s           |     |
| <b>External Slave Mode</b>                             |                      |           |            |             |             |     |
| <b>MCKI Input Timing</b>                               |                      |           |            |             |             |     |
| Frequency  | 256fs                | fCLK      | 2.048      | -           | 12.288      | MHz |
|  | 512fs                | fCLK      | 4.096      | -           | 12.288      | MHz |
|  | 1024fs               | fCLK      | 8.192      | -           | 12.288      | MHz |
| Pulse Width Low  |                      | tCLKL     | 0.4/fCLK   | -           | s           |     |
| Pulse Width High                                       |                      | tCLKH     | 0.4/fCLK   | -           | s           |     |
| <b>LRCK Input Timing</b>                               |                      |           |            |             |             |     |
| Frequency  | 256fs                | fs        | 8          | -           | 48          | kHz |
|  | 512fs                | fs        | 8          | -           | 24          | kHz |
|  | 1024fs               | fs        | 8          | -           | 12          | kHz |
| Stereo Mode: Duty Cycle                                |                      | Duty      | 45         | -           | 55          | %   |
| TDM64 Mode:  |                      |           |            |             |             |     |
| I <sup>2</sup> S compatible: Pulse Width Low           |                      | tLRCKL    | 1/(64fs)   | -           | 63/(64fs)   | s   |
| MSB justified: Pulse Width High                        |                      | tLRCKH    | 1/(64fs)   | -           | 63/(64fs)   | s   |
| TDM128 Mode:   |                      |           |            |             |             |     |
| I <sup>2</sup> S compatible: Pulse Width Low           |                      | tLRCKL    | 1/(128fs)  | -           | 127/(128fs) | s   |
| MSB justified: Pulse Width High                        |                      | tLRCKH    | 1/(128fs)  | -           | 127/(128fs) | s   |
| <b>BICK Input Timing</b>                               |                      |           |            |             |             |     |
| Period   | Stereo Mode          |           | tBCK       | 325.52      | -           | ns  |
|  | TDM Mode             |           | tBCK       | 162.76      | -           | ns  |
| Pulse Width Low  | Stereo Mode          |           | tBCKL      | 130         | -           | ns  |
|  | TDM Mode             |           | tBCKL      | 65          | -           | ns  |
| Pulse Width High                                       | Stereo Mode          |           | tBCKH      | 130         | -           | ns  |
|  | TDM Mode             |           | tBCKH      | 65          | -           | ns  |

| Parameter   | Symbol                               | min      | typ     | max       | Unit   |     |
|---|--------------------------------------|----------|---------|-----------|--------|-----|
| <b>External Master Mode</b>   |                                      |          |         |           |        |     |
| <b>MCKI Input Timing</b>  |                                      |          |         |           |        |     |
| Frequency   | 256fs                                | fCLK     | 2.048   | -         | 12.288 | MHz |
|   | 512fs                                | fCLK     | 4.096   | -         | 12.288 | MHz |
|   | 1024fs                               | fCLK     | 8.192   | -         | 12.288 | MHz |
| Pulse Width Low   | tCLKL                                | 0.4/fCLK | -       | -         | s      |     |
| Pulse Width High  | tCLKH                                | 0.4/fCLK | -       | -         | s      |     |
| <b>LRCK Output Timing</b>   |                                      |          |         |           |        |     |
| Frequency   | fs                                   | 8        | -       | 48        | kHz    |     |
| Stereo Mode: Duty Cycle   | Duty                                 | -        | 50      | -         | %      |     |
| TDM64, TDM128 Mode:   |                                      |          |         |           |        |     |
| I <sup>2</sup> S compatible: Pulse Width Low                        | tLRCKL                               | -        | 1/(4fs) | -         | s      |     |
| MSB justified: Pulse Width High                                     | tLRCKH                               | -        | 1/(4fs) | -         | s      |     |
| <b>BICK Output Timing</b>   |                                      |          |         |           |        |     |
| Period  | BCKO1-0 bits = "00"                  | tBCK     | -       | 1/(32fs)  | -      | s   |
|   | BCKO1-0 bits = "01"                  | tBCK     | -       | 1/(64fs)  | -      | s   |
|   | BCKO1-0 bits = "10"<br>(TDM128 Mode) | tBCK     | -       | 1/(128fs) | -      | s   |
| Duty Cycle  | dBCK                                 | -        | 50      | -         | %      |     |
| <b>Audio Interface Timing (Left justified &amp; I<sup>2</sup>S)</b> |                                      |          |         |           |        |     |
| <b>Master Mode</b>  |                                      |          |         |           |        |     |
| BICK "↓" to LRCK Edge (Note 15)                                     | tMBLR                                | -40      | -       | 40        | ns     |     |
| LRCK Edge to SDTO (MSB)<br>(Except I <sup>2</sup> S mode)           | tLRD                                 | -70      | -       | 70        | ns     |     |
| BICK "↓" to SDTO  | tBSD                                 | -70      | -       | 70        | ns     |     |
| <b>Slave Mode</b>   |                                      |          |         |           |        |     |
| LRCK Edge to BICK "↑" (Note 15)                                     | tLRB                                 | 50       | -       | -         | ns     |     |
| BICK "↑" to LRCK Edge (Note 15)                                     | tBLR                                 | 50       | -       | -         | ns     |     |
| LRCK Edge to SDTO (MSB)<br>(Except I <sup>2</sup> S mode)           | tLRD                                 | -        | -       | 80        | ns     |     |
| BICK "↓" to SDTO  | tBSD                                 | -        | -       | 80        | ns     |     |
| <b>Audio Interface Timing (TDM64 Mode)</b>                          |                                      |          |         |           |        |     |
| <b>Master Mode</b>  |                                      |          |         |           |        |     |
| BICK "↓" to LRCK  | tMBLR                                | -40      | -       | 40        | ns     |     |
| BICK "↓" to SDTOB (Note 16)   | tBSD                                 | -70      | -       | 70        | ns     |     |
| <b>Slave Mode</b>   |                                      |          |         |           |        |     |
| LRCK Edge to BICK "↑" (Note 15)                                     | tLRB                                 | 50       | -       | -         | ns     |     |
| BICK "↑" to LRCK Edge (Note 15)                                     | tBLR                                 | 50       | -       | -         | ns     |     |
| BICK "↓" to SDTOB (Note 16)   | tBSD                                 | -        | -       | 80        | ns     |     |
| <b>Audio Interface Timing (TDM128 Mode)</b>                         |                                      |          |         |           |        |     |
| <b>Master Mode</b>  |                                      |          |         |           |        |     |
| BICK "↓" to LRCK  | tMBLR                                | -24      | -       | 24        | ns     |     |
| BICK "↓" to SDTOB (Note 16)   | tBSD                                 | -40      | -       | 40        | ns     |     |
| <b>Slave Mode</b>   |                                      |          |         |           |        |     |
| LRCK Edge to BICK "↑" (Note 15)                                     | tLRB                                 | 40       | -       | -         | ns     |     |
| BICK "↑" to LRCK Edge (Note 15)                                     | tBLR                                 | 40       | -       | -         | ns     |     |
| BICK "↓" to SDTOB (Note 16)   | tBSD                                 | -        | -       | 50        | ns     |     |

Note 15. BICK rising edge must not occur at the same time as LRCK edge.

Note 16. SDTOA is fixed to "L".

| Parameter   | Symbol  | min | typ  | max | Unit |
|---|---------|-----|------|-----|------|
| <b>Control Interface Timing (3-wire mode):</b>                      |         |     |      |     |      |
| CCLK Period   | tCCK    | 200 | -    | -   | ns   |
| CCLK Pulse Width Low  | tCCKL   | 80  | -    | -   | ns   |
| Pulse Width High  | tCCKH   | 80  | -    | -   | ns   |
| CDTIO Setup Time  | tCDS    | 40  | -    | -   | ns   |
| CDTIO Hold Time   | tCDH    | 40  | -    | -   | ns   |
| CSN "H" Time  | tCSW    | 150 | -    | -   | ns   |
| CSN Edge to CCLK "↑" (Note 17)                                      | tCSS    | 50  | -    | -   | ns   |
| CCLK "↑" to CSN Edge (Note 17)                                      | tCSH    | 50  | -    | -   | ns   |
| CCLK "↓" to CDTIO (at Read Command)                                 | tDCD    | -   | -    | 70  | ns   |
| CSN "↑" to CDTIO (Hi-Z) (at Read Command) (Note 19)                 | tCCZ    | -   | -    | 70  | ns   |
| <b>Control Interface Timing (I<sup>2</sup>C Bus mode) (Note 18)</b> |         |     |      |     |      |
| SCL Clock Frequency   | fSCL    | -   | -    | 400 | kHz  |
| Bus Free Time Between Transmissions                                 | tBUF    | 1.3 | -    | -   | μs   |
| Start Condition Hold Time (prior to first clock pulse)              | tHD:STA | 0.6 | -    | -   | μs   |
| Clock Low Time  | tLOW    | 1.3 | -    | -   | μs   |
| Clock High Time   | tHIGH   | 0.6 | -    | -   | μs   |
| Setup Time for Repeated Start Condition                             | tSU:STA | 0.6 | -    | -   | μs   |
| SDA Hold Time from SCL Falling (Note 20)                            | tHD:DAT | 0   | -    | -   | μs   |
| SDA Setup Time from SCL Rising                                      | tSU:DAT | 0.1 | -    | -   | μs   |
| Rise Time of Both SDA and SCL Lines                                 | tR      | -   | -    | 0.3 | μs   |
| Fall Time of Both SDA and SCL Lines                                 | tF      | -   | -    | 0.3 | μs   |
| Setup Time for Stop Condition                                       | tSU:STO | 0.6 | -    | -   | μs   |
| Pulse Width of Spike Noise Suppressed by Input Filter               | tSP     | 0   | -    | 50  | ns   |
| Capacitive Load on Bus  | Cb      | -   | -    | 400 | pF   |
| <b>Power-down &amp; Reset Timing</b>                                |         |     |      |     |      |
| PDN Accept Pulse Width (Note 21)                                    | tAPD    | 1.0 | -    | -   | μs   |
| PDN Reject Pulse Width (Note 21)                                    | tRPD    | -   | -    | 50  | ns   |
| PMADAL or PMADAR or PMADBL or PMADBR "↑" to SDTO valid (Note 22)    |         |     |      |     |      |
| ADRSTA/B1-0 bits = "00"   | tPDV    | -   | 1059 | -   | 1/fs |
| ADRSTA/B1-0 bits = "01"   | tPDV    | -   | 267  | -   | 1/fs |
| ADRSTA/B1-0 bits = "10"   | tPDV    | -   | 2115 | -   | 1/fs |
| ADRSTA/B1-0 bits = "11"   | tPDV    | -   | 531  | -   | 1/fs |

Note 17. CCLK rising edge must not occur at the same time as CSN edge.

Note 18. I<sup>2</sup>C-bus is a trademark of NXP B.V.

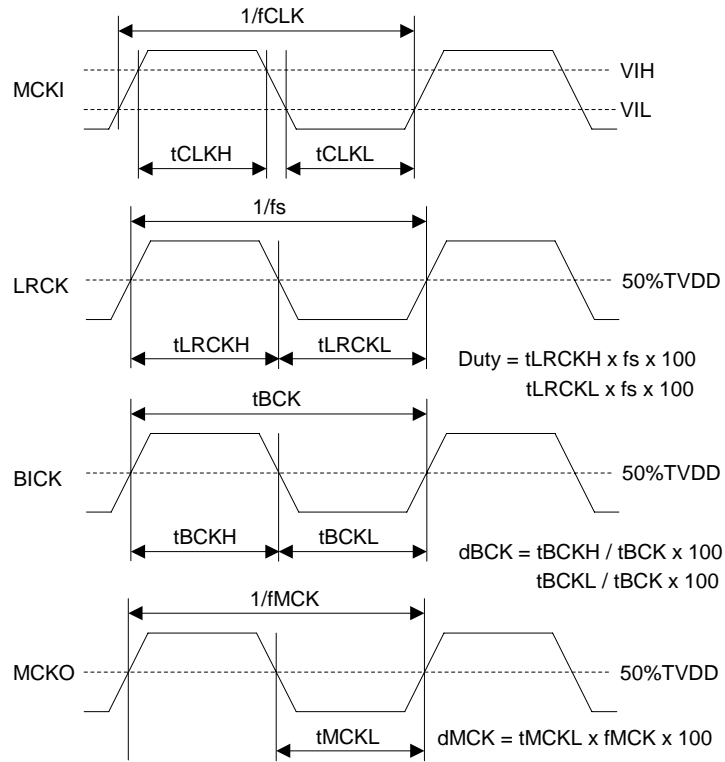
Note 19. R<sub>L</sub>=1kΩ/10% change (pull-up to TVDD)

Note 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 21. The AK5703 can be reset by bringing the PDN pin "L" upon power-up. The PDN pin must held "L" for more than 1μs for a certain reset. The AK5703 is not reset by the "L" pulse less than 50ns.

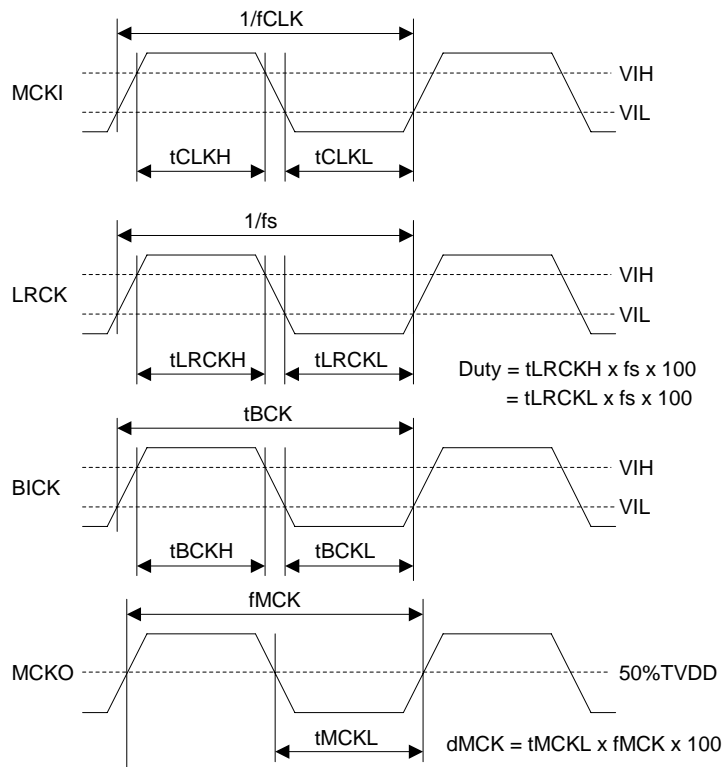
Note 22. This is the count of LRCK "↑" from the PMADAL, PMADAR, PMADBL or PMADBR bit = "1".

■ Timing Diagram



Note 23. MCKO is not available at EXT Master Mode.

Figure 2. Clock Timing (PLL/EXT Master mode)



Note 24. The MCKI pin is "L" level when PLL reference clock is the BICK pin.

Figure 3. Clock Timing (PLL Slave mode)

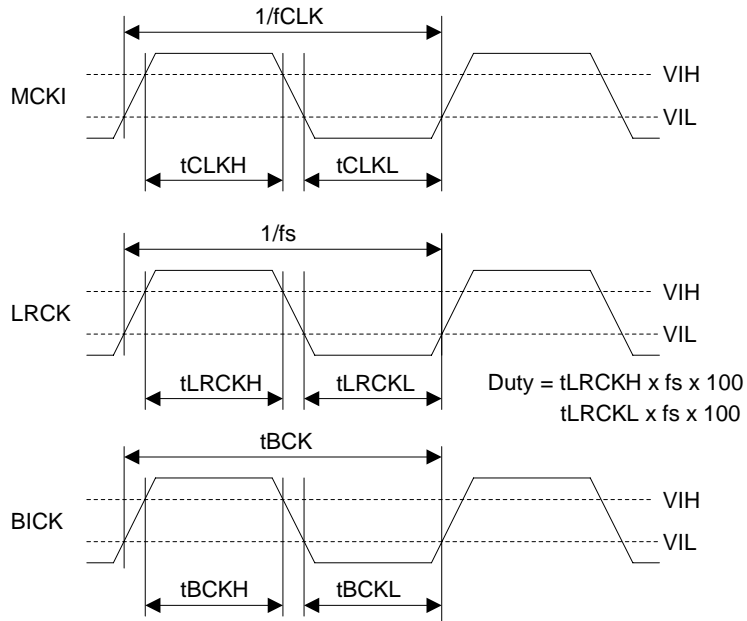


Figure 4. Clock Timing (EXT Slave mode)

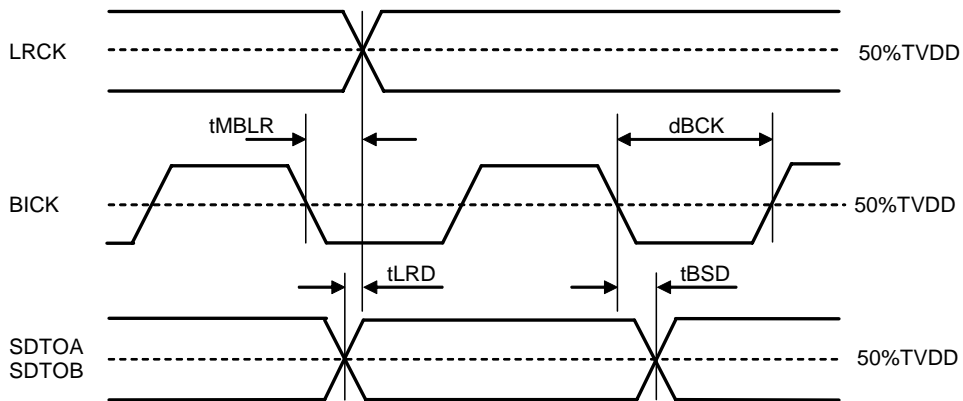


Figure 5. Audio Interface Timing (PLL/EXT Master mode & Normal Mode)

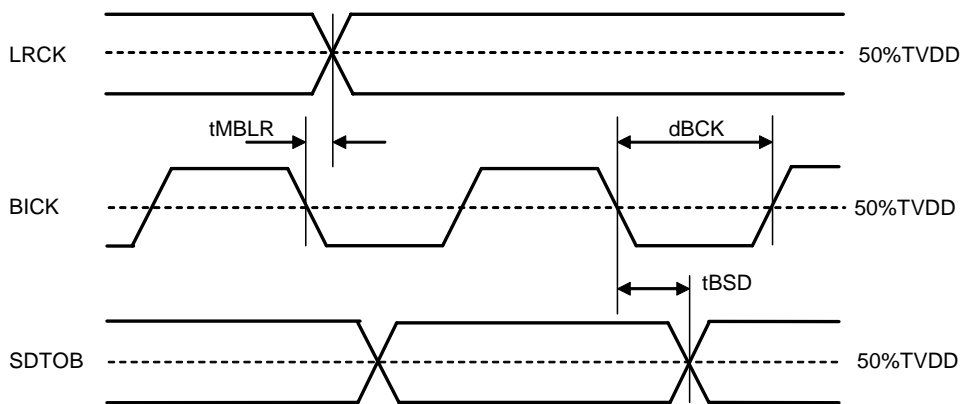


Figure 6. Audio Interface Timing (PLL/EXT Master mode & TDM mode)

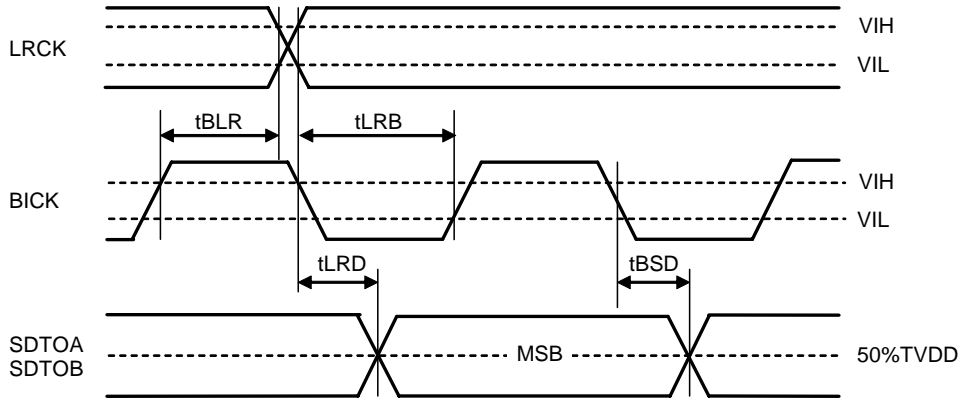


Figure 7. Audio Interface Timing (PLL/EXT Slave mode & Normal mode)

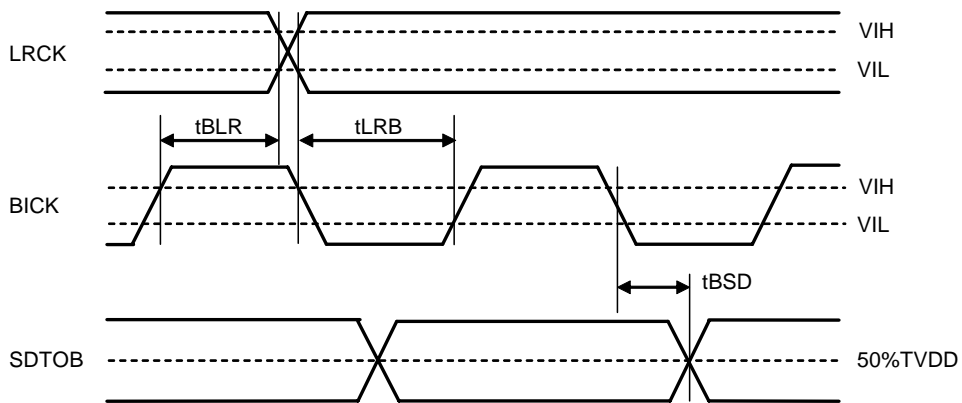


Figure 8. Audio Interface Timing (PLL/EXT Slave mode & TDM mode)

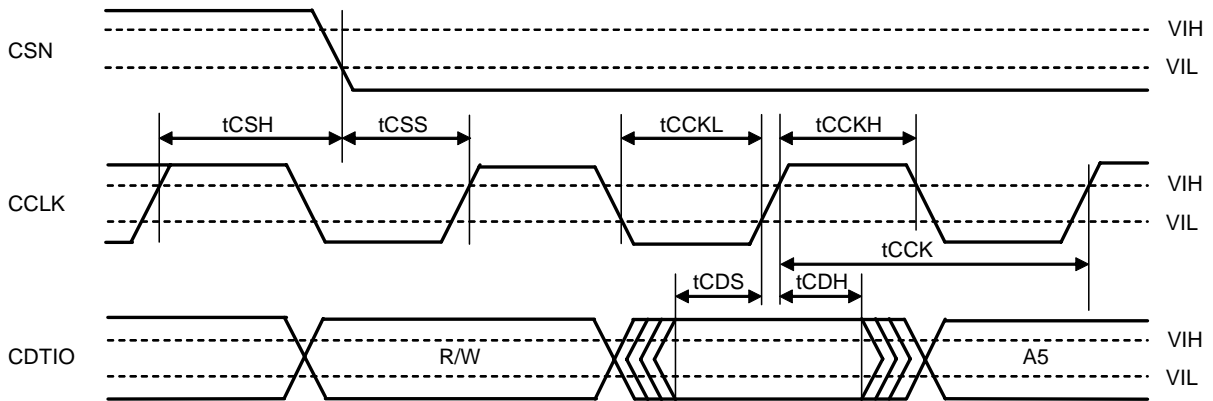


Figure 9. WRITE Command Input Timing

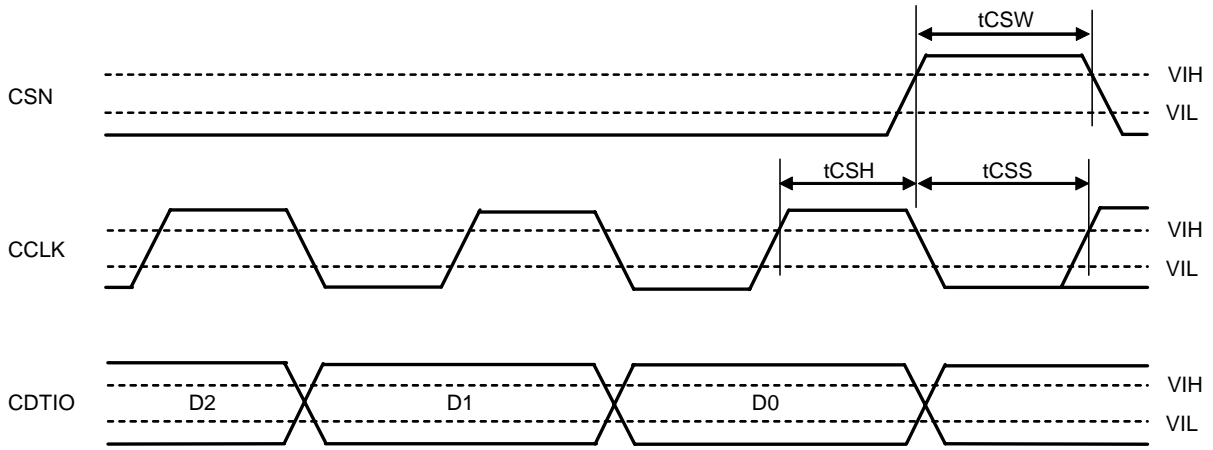


Figure 10. WRITE Data Input Timing

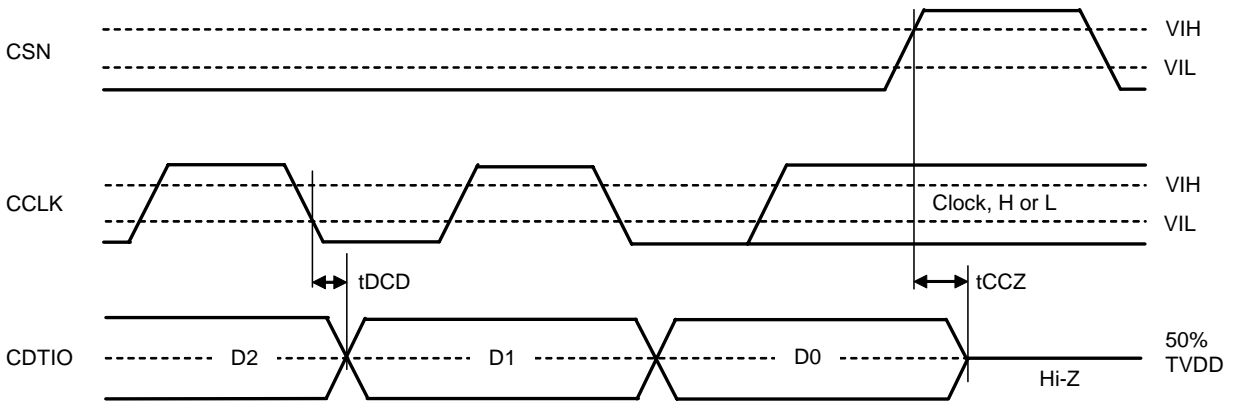


Figure 11. Read Data Output Timing

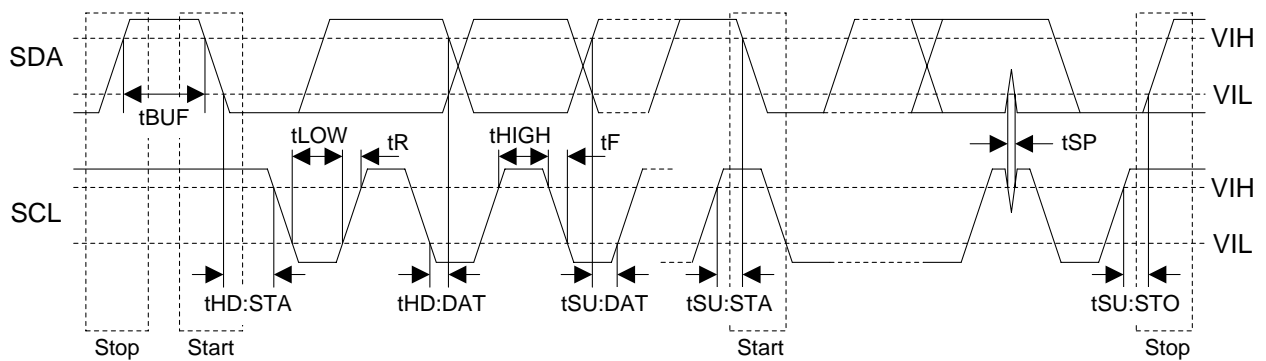


Figure 12. I<sup>2</sup>C Bus Mode Timing

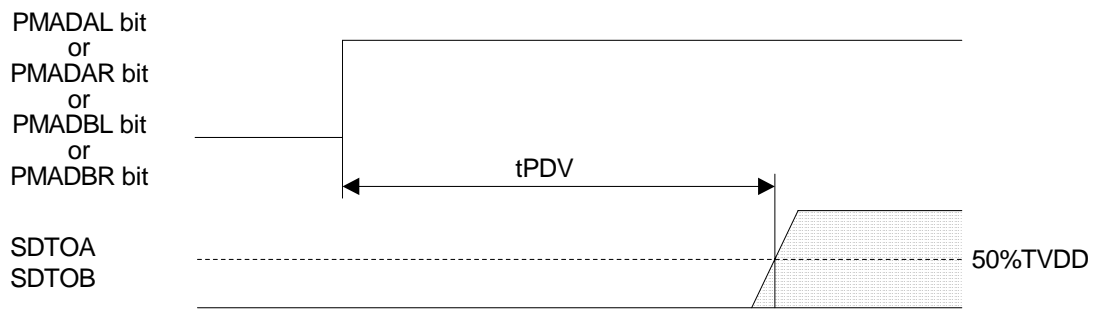


Figure 13. Power Down & Reset Timing 1

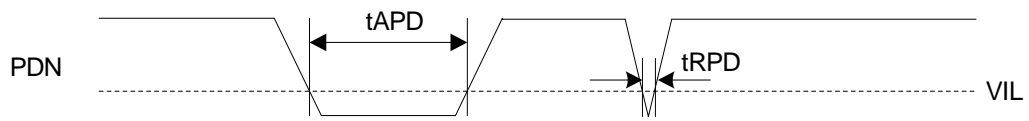


Figure 14. Power Down & Reset Timing 2

|                           |
|---------------------------|
| <b>OPERATION OVERVIEW</b> |
|---------------------------|

### ■ System Clock

There are the following five clock modes to interface with external devices (Table 1, Table 2).

| Mode  | PMPLL bit | M/S bit | PLL3-0 bits | Figure    |
|---|-----------|---------|-------------|-----------|
| PLL Master Mode (Note 25)                           | 1         | 1       | Table 4     | Figure 15 |
| PLL Slave Mode 1<br>(PLL Reference Clock: MCKI pin) | 1         | 0       | Table 4     | Figure 16 |
| PLL Slave Mode 2<br>(PLL Reference Clock: BICK pin) | 1         | 0       | Table 4     | Figure 17 |
| EXT Slave Mode                                      | 0         | 0       | x           | Figure 18 |
| EXT Master Mode                                     | 0         | 1       | x           | Figure 19 |

Note 25. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin.

Table 1. Clock Mode Setting (x: Don't care)

| Mode  | MCKO bit | MCKO pin                  | MCKI pin                   | BICK pin                                | LRCK pin        |
|---|----------|---------------------------|----------------------------|---|-----------------|
| PLL Master Mode                                     | 0        | "L"                       | Selected by<br>PLL3-0 bits | Output<br>(Selected by<br>BCKO1-0 bits) | Output<br>(1fs) |
|   | 1        | Selected by<br>PS1-0 bits |                            |   |                 |
| PLL Slave Mode 1<br>(PLL Reference Clock: MCKI pin) | 0        | "L"                       | Selected by<br>PLL3-0 bits | Input<br>(≥ 32fs)                       | Input<br>(1fs)  |
|   | 1        | Selected by<br>PS1-0 bits |                            |   |                 |
| PLL Slave Mode 2<br>(PLL Reference Clock: BICK pin) | 0        | "L"                       | GND                        | Input<br>(Selected by<br>PLL3-0 bits)   | Input<br>(1fs)  |
|   | 1        | Selected by<br>PS1-0 bits |                            |   |                 |
| EXT Slave Mode                                      | 0        | "L"                       | Selected by<br>CM1-0 bits  | Input<br>(≥ 32fs)                       | Input<br>(1fs)  |
|   | 1        | N/A                       |                            |   |                 |
| EXT Master Mode                                     | 0        | "L"                       | Selected by<br>CM1-0 bits  | Output<br>(Selected by<br>BCKO1-0 bits) | Output<br>(1fs) |
|   | 1        | N/A                       |                            |   |                 |

Table 2. Clock pins state in Clock Mode (N/A: Not Available)

### ■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK5703 is in power-down mode (PDN pin = "L") and when exits reset state, the AK5703 is in slave mode. After exiting reset state, the AK5703 goes to master mode by changing M/S bit = "1".

When the AK5703 is in master mode, the LRCK and BICK pins are a Hi-Z state until M/S bit becomes "1". The LRCK and BICK pins of the AK5703 must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

| M/S bit | Mode        |
|---------|-------------|
| 0       | Slave Mode  |
| 1       | Master Mode |

(default)

Table 3. Select Master/Slave Mode

## ■ PLL Mode

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by the PLL2-0 and FS3-0 bits. The PLL lock times, when the AK5703 is supplied stable clocks or the sampling frequency is changed after PLL is powered-up (PMPLL bit = “0” → “1”), are shown in [Table 4](#).

### 1) PLL Mode Setting

| Mode   | PLL3 bit | PLL2 bit | PLL1 bit | PLL0 bit | PLL Reference Clock Input Pin | Input Frequency | PLL Lock Time (max) |
|--------|----------|----------|----------|----------|-------------------------------|-----------------|---------------------|
| 1      | 0        | 0        | 0        | 1        | BICK pin                      | 128fs           | 2ms                 |
| 2      | 0        | 0        | 1        | 0        | BICK pin                      | 32fs            | 2ms                 |
| 3      | 0        | 0        | 1        | 1        | BICK pin                      | 64fs            | 2ms                 |
| 4      | 0        | 1        | 0        | 0        | MCKI pin                      | 11.2896MHz      | 10ms                |
| 5      | 0        | 1        | 0        | 1        | MCKI pin                      | 12.288MHz       | 10ms                |
| 6      | 0        | 1        | 1        | 0        | MCKI pin                      | 12MHz           | 10ms                |
| 7      | 0        | 1        | 1        | 1        | MCKI pin                      | 24MHz           | 10ms                |
| 8      | 1        | 0        | 0        | 0        | MCKI pin                      | 19.2MHz         | 10ms                |
| 10     | 1        | 0        | 1        | 0        | MCKI pin                      | 13MHz           | 10ms                |
| 11     | 1        | 0        | 1        | 1        | MCKI pin                      | 26MHz           | 10ms                |
| 12     | 1        | 1        | 0        | 0        | MCKI pin                      | 13.5MHz         | 10ms                |
| 13     | 1        | 1        | 0        | 1        | MCKI pin                      | 27MHz           | 10ms                |
| Others | Others   |          |          | N/A      |                               |                 |                     |

Table 4. Setting of PLL Mode (fs: Sampling Frequency), (N/A: Not Available)

### 2) Setting of sampling frequency in PLL Mode

When the PLL reference clock input is the MCKI pin or the BICK pin, the sampling frequency is selected by FS3-0 bits as defined in [Table 5](#).

| Mode   | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency ( <a href="#">Note 26</a> ) |
|--------|---------|---------|---------|---------|--|
| 0      | 0       | 0       | 0       | 0       | 8kHz mode                                      |
| 1      | 0       | 0       | 0       | 1       | 12kHz mode                                     |
| 2      | 0       | 0       | 1       | 0       | 16kHz mode                                     |
| 3      | 0       | 0       | 1       | 1       | 24kHz mode                                     |
| 5      | 0       | 1       | 0       | 1       | 11.025kHz mode                                 |
| 7      | 0       | 1       | 1       | 1       | 22.05kHz mode                                  |
| 10     | 1       | 0       | 1       | 0       | 32kHz mode                                     |
| 11     | 1       | 0       | 1       | 1       | 48kHz mode                                     |
| 15     | 1       | 1       | 1       | 1       | 44.1kHz mode                                   |
| Others | Others  |         |         |         | N/A  |

Table 5. Setting of Sampling Frequency at PMPLL bit = “1” (N/A: Not Available)

Note 26. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to [Table 6](#) for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in [Table 6](#). When the BICK pin is the PLL reference clock input, the sampling frequency generated by PLL is the same sampling frequency of mode name.

| Input Frequency<br>MCKI[MHz] | Sampling Frequency<br>Mode   | Sampling Frequency<br>generated by PLL [kHz](Note 27) |
|------------------------------|--|---|
| 11.2896                      | 8kHz mode  | 8.000000  |
|                              | 12kHz mode   | 12.000000   |
|                              | 16kHz mode   | 16.000000   |
|                              | 24kHz mode   | 24.000000   |
|                              | 32kHz mode   | 32.000000   |
|                              | 48kHz mode   | 48.000000   |
|                              | 11.025kHz mode   | 11.025000   |
|                              | 22.05kHz mode  | 22.050000   |
| 44.1kHz mode                 | 44.100000  |   |
| 12.288                       | 8kHz mode  | 8.000000  |
|                              | 12kHz mode   | 12.000000   |
|                              | 16kHz mode   | 16.000000   |
|                              | 24kHz mode   | 24.000000   |
|                              | 32kHz mode   | 32.000000   |
|                              | 48kHz mode   | 48.000000   |
|                              | 11.025kHz mode   | 11.025000   |
|                              | 22.05kHz mode  | 22.050000   |
| 44.1kHz mode                 | 44.100000  |   |
| 12                           | 8kHz mode  | 8.000000  |
|                              | 12kHz mode   | 12.000000   |
|                              | 16kHz mode   | 16.000000   |
|                              | 24kHz mode   | 24.000000   |
|                              | 32kHz mode   | 32.000000   |
|                              | 48kHz mode   | 48.000000   |
|                              | 11.025kHz mode   | 11.024877   |
|                              | 22.05kHz mode  | 22.049753   |
| 44.1kHz mode                 | 44.099507  |   |
| 24                           | 8kHz mode  | 8.000000  |
|                              | 12kHz mode   | 12.000000   |
|                              | 16kHz mode   | 16.000000   |
|                              | 24kHz mode   | 24.000000   |
|                              | 32kHz mode   | 32.000000   |
|                              | 48kHz mode   | 48.000000   |
|                              | 11.025kHz mode   | 11.024877   |
|                              | 22.05kHz mode  | 22.049753   |
| 44.1kHz mode                 | 44.099507  |   |
|                              | Sampling frequency that differs from sampling frequency of mode name |   |

Note 27. These are rounded off to six decimal places.

Table 6. Sampling Frequency at PLL mode (Reference clock is MCKI)

| Input Frequency<br>MCKI[MHz] | Sampling Frequency<br>Mode   | Sampling Frequency<br>generated by PLL [kHz](Note 27) |
|------------------------------|--|---|
| 19.2                         | 8kHz mode  | 8.000000  |
|                              | 12kHz mode   | 12.000000   |
|                              | 16kHz mode   | 16.000000   |
|                              | 24kHz mode   | 24.000000   |
|                              | 32kHz mode   | 32.000000   |
|                              | 48kHz mode   | 48.000000   |
|                              | 11.025kHz mode   | 11.025000   |
|                              | 22.05kHz mode  | 22.050000   |
| 44.1kHz mode                 | 44.100000  |   |
| 13                           | 8kHz mode  | 7.999786  |
|                              | 12kHz mode   | 11.999679   |
|                              | 16kHz mode   | 15.999572   |
|                              | 24kHz mode   | 23.999358   |
|                              | 32kHz mode   | 31.999144   |
|                              | 48kHz mode   | 47.998716   |
|                              | 11.025kHz mode   | 11.024877   |
|                              | 22.05kHz mode  | 22.049753   |
| 44.1kHz mode                 | 44.099507  |   |
| 26                           | 8kHz mode  | 7.999786  |
|                              | 12kHz mode   | 11.999679   |
|                              | 16kHz mode   | 15.999572   |
|                              | 24kHz mode   | 23.999358   |
|                              | 32kHz mode   | 31.999144   |
|                              | 48kHz mode   | 47.998716   |
|                              | 11.025kHz mode   | 11.024877   |
|                              | 22.05kHz mode  | 22.049753   |
| 44.1kHz mode                 | 44.099507  |   |
| 13.5                         | 8kHz mode  | 8.000300  |
|                              | 12kHz mode   | 12.000451   |
|                              | 16kHz mode   | 16.000601   |
|                              | 24kHz mode   | 24.000901   |
|                              | 32kHz mode   | 32.001202   |
|                              | 48kHz mode   | 48.001803   |
|                              | 11.025kHz mode   | 11.025218   |
|                              | 22.05kHz mode  | 22.050436   |
| 44.1kHz mode                 | 44.100871  |   |
| 27                           | 8kHz mode  | 8.000300  |
|                              | 12kHz mode   | 12.000451   |
|                              | 16kHz mode   | 16.000601   |
|                              | 24kHz mode   | 24.000901   |
|                              | 32kHz mode   | 32.001202   |
|                              | 48kHz mode   | 48.001803   |
|                              | 11.025kHz mode   | 11.025218   |
|                              | 22.05kHz mode  | 22.050436   |
| 44.1kHz mode                 | 44.100871  |   |
|                              | Sampling frequency that differs from sampling frequency of mode name |   |

Note 27. These are rounded off to six decimal places.

Table 6. Sampling Frequency at PLL mode (Reference clock is MCKI)

## ■PLL Unlock State

### 1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK and BICK pin go to "L", and an irregular frequency clock is output from the MCKO pin when MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin outputs "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit "0".

| PLL State                      | MCKO pin       |                | BICK pin   | LRCK pin   |
|--------------------------------|----------------|----------------|------------|------------|
|                                | MCKO bit = "0" | MCKO bit = "1" |            |            |
| After that PMPLL bit "0" → "1" | "L" Output     | Invalid        | "L" Output | "L" Output |
| PLL Unlock (except above case) | "L" Output     | Invalid        | Invalid    | Invalid    |
| PLL Lock                       | "L" Output     | Table 9        | Table 10   | 1fs Output |

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

### 2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC output invalid data when the PLL is unlocked.

| PLL State                      | MCKO pin       |                |
|--------------------------------|----------------|----------------|
|                                | MCKO bit = "0" | MCKO bit = "1" |
| After that PMPLL bit "0" → "1" | "L" Output     | Invalid        |
| PLL Unlock (except above case) | "L" Output     | Invalid        |
| PLL Lock                       | "L" Output     | Table 9        |

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates MCKO, BICK and LRCK clocks. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs, 64fs or 128fs, by BCKO1-0 bits (Table 10).

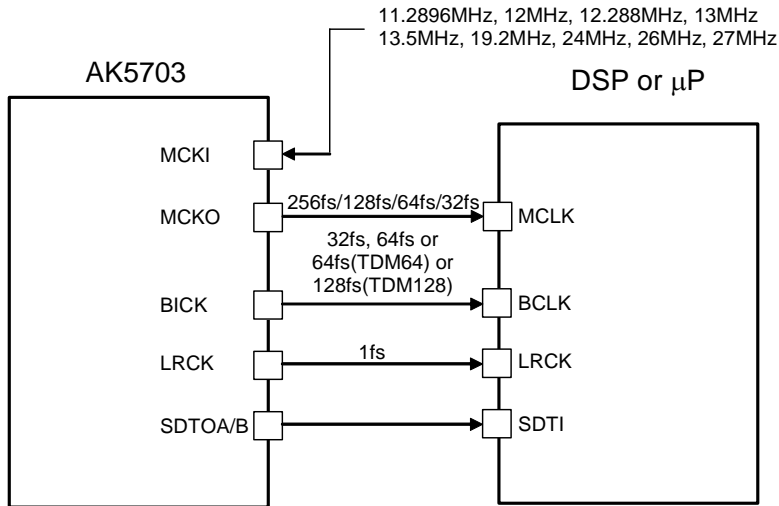


Figure 15. PLL Master Mode

| Mode | PS1 bit | PS0 bit | MCKO pin |
|------|---------|---------|----------|
| 0    | 0       | 0       | 256fs    |
| 1    | 0       | 1       | 128fs    |
| 2    | 1       | 0       | 64fs     |
| 3    | 1       | 1       | 32fs     |

(default)

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = “1”)

| Mode | BCKO1 bit | BCKO0 bit | BICK Output Frequency  |
|------|-----------|-----------|------------------------|
| 0    | 0         | 0         | 32fs                   |
| 1    | 0         | 1         | 64fs                   |
| 2    | 1         | 0         | 128fs<br>(TDM128 Mode) |
| 3    | 1         | 1         | N/A                    |

(default)

Note 28. 128fs is only available in TDM mode.

Table 10. BICK Output Frequency at Master Mode (N/A: Not Available)

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to MCKI or BICK pin. The required clock to the AK5703 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL Slave Mode 1 (PLL reference clock: MCKI pin)

The BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

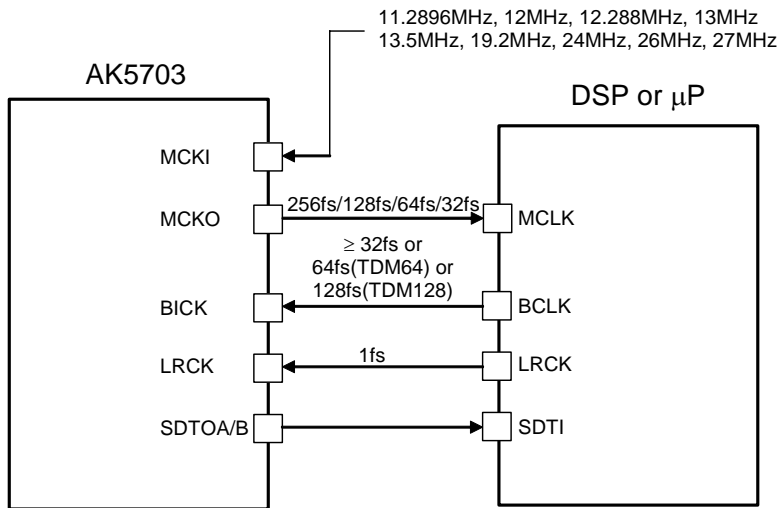


Figure 16. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL Slave Mode 2 (PLL reference clock: BICK pin)

The sampling frequency corresponds to a range from 8kHz to 48kHz by changing FS3-0 bits (Table 5). The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit.

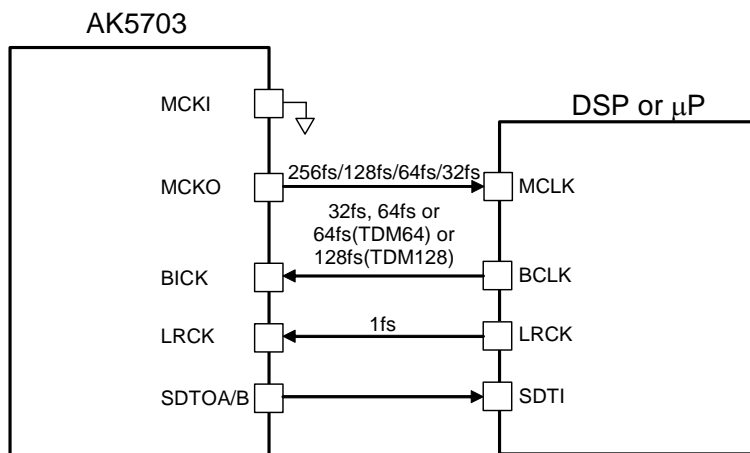


Figure 17. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

■ EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

When PMPLL bit is “0”, the AK5703 becomes EXT mode. Master clock can be input to the internal ADC directly from the MCKI pin without internal PLL circuit operation. This mode is compatible with I/F of a normal audio CODEC. The clocks required to operate the AK5703 are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK ( $\geq 32$ fs). The master clock (MCKI) must be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by CM1-0 bits (Table 11) and sampling frequency is selected by FS3-0 bits (Table 12).

| Mode | CM1 bit | CM0 bit | MCKI Input Frequency | Sampling Frequency Range |
|------|---------|---------|----------------------|--------------------------|
| 0    | 0       | 0       | 256fs                | 24kHz ~ 48kHz            |
| 1    | 0       | 1       | 512fs                | 8kHz ~ 24kHz             |
| 2    | 1       | 0       | 1024fs               | 8kHz ~ 12kHz             |
| 3    | 1       | 1       | 256fs                | 8kHz ~ 24kHz             |

(default)

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

| Mode   | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency |
|--------|---------|---------|---------|---------|--------------------|
| 0      | 0       | 0       | 0       | 0       | 8kHz               |
| 1      | 0       | 0       | 0       | 1       | 12kHz              |
| 2      | 0       | 0       | 1       | 0       | 16kHz              |
| 3      | 0       | 0       | 1       | 1       | 24kHz              |
| 5      | 0       | 1       | 0       | 1       | 11.025kHz          |
| 7      | 0       | 1       | 1       | 1       | 22.05kHz           |
| 10     | 1       | 0       | 1       | 0       | 32kHz              |
| 11     | 1       | 0       | 1       | 1       | 48kHz              |
| 15     | 1       | 1       | 1       | 1       | 44.1kHz            |
| Others | Others  |         |         |         | N/A                |

(default)

Table 12. Setting of Sampling Frequency (N/A: Not Available)

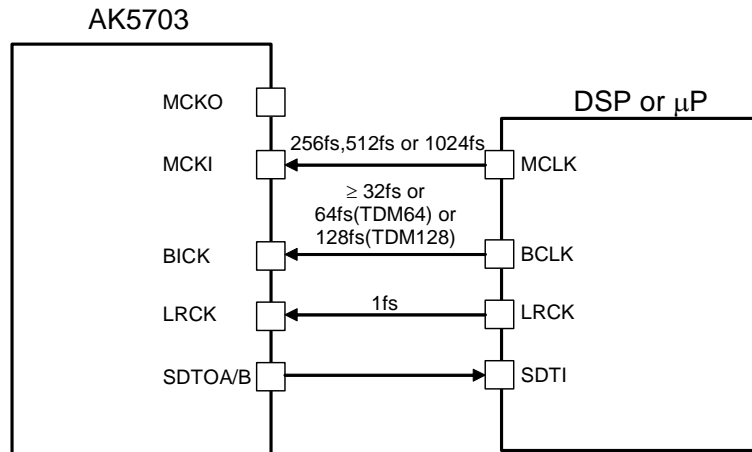


Figure 18. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The AK5703 becomes EXT Master Mode by setting PMPLL bit = “0” and M/S bit = “1”. Master clock can be input to the internal ADC directly from the MCKI pin without the internal PLL circuit operation. The clock required to operate is MCKI (256fs, 512fs, or 1024fs). The input frequency of MCKI is selected by CM1-0 bits (Table 13) and sampling frequency is selected by FS3-0 bits (Table 14). The BICK output frequency is selected between 32fs, 64fs or 128fs, by BCKO1-0 bits (Table 15).

| Mode | CM1 bit | CM0 bit | MCKI Input Frequency | Sampling Frequency Range |
|------|---------|---------|----------------------|--------------------------|
| 0    | 0       | 0       | 256fs                | 24kHz ~ 48kHz            |
| 1    | 0       | 1       | 512fs                | 8kHz ~ 24kHz             |
| 2    | 1       | 0       | 1024fs               | 8kHz ~ 12kHz             |
| 3    | 1       | 1       | 256fs                | 8kHz ~ 24kHz             |

Table 13. MCKI Frequency at EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

| Mode   | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency |
|--------|---------|---------|---------|---------|--------------------|
| 0      | 0       | 0       | 0       | 0       | 8kHz               |
| 1      | 0       | 0       | 0       | 1       | 12kHz              |
| 2      | 0       | 0       | 1       | 0       | 16kHz              |
| 3      | 0       | 0       | 1       | 1       | 24kHz              |
| 5      | 0       | 1       | 0       | 1       | 11.025kHz          |
| 7      | 0       | 1       | 1       | 1       | 22.05kHz           |
| 10     | 1       | 0       | 1       | 0       | 32kHz              |
| 11     | 1       | 0       | 1       | 1       | 48kHz              |
| 15     | 1       | 1       | 1       | 1       | 44.1kHz            |
| Others | Others  |         |         |         | N/A                |

Table 14. Setting of Sampling Frequency (N/A: Not Available)

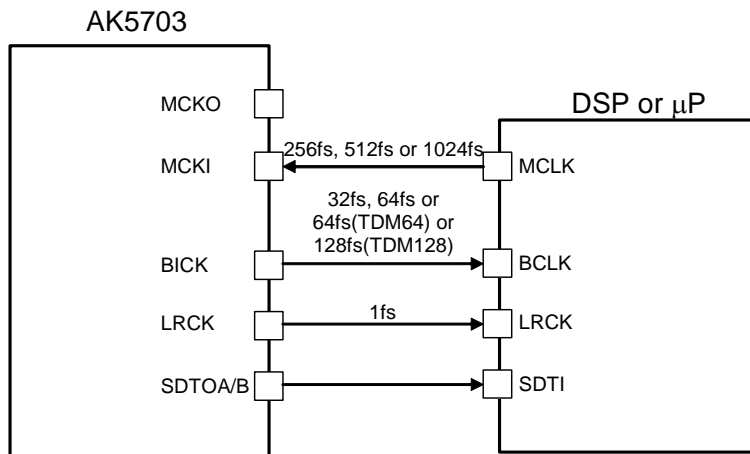


Figure 19. EXT Master Mode

| Mode | BCKO1 bit | BCKO0 bit | BICK Output Frequency  |
|------|-----------|-----------|------------------------|
| 0    | 0         | 0         | 32fs                   |
| 1    | 0         | 1         | 64fs                   |
| 2    | 1         | 0         | 128fs<br>(TDM128 Mode) |
| 3    | 1         | 1         | N/A                    |

Note 28. 128fs is only available in TDM mode.

Table 15. BICK Output Frequency at Master Mode (N/A: Not Available)

■ SYSTEM RESET

Upon power-up, the AK5703 must be reset by bringing the PDN pin = “L”. This reset is released when a dummy command is input after the PDN pin = “H”. This ensures that all internal registers reset to their initial value. Dummy command is executed by writing all “0” to the register address 00H (In fact, after 16 times rising edge of CCLK/SCL.). It is recommended to set the PDN pin = “L” before power up the AK5703.

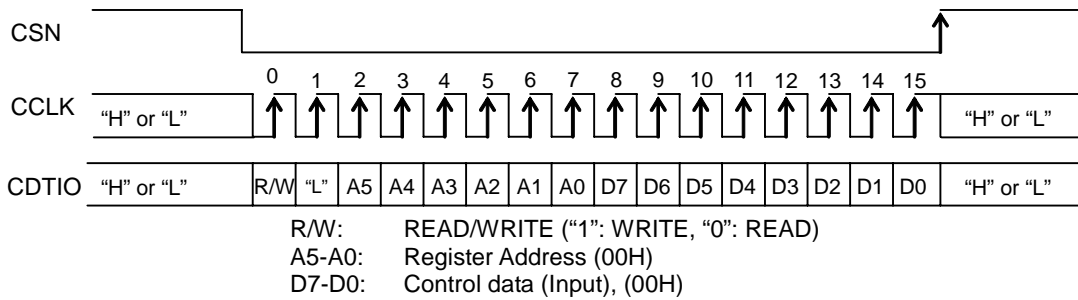


Figure 20. Dummy Command in 3-wired Serial Mode

In I<sup>2</sup>C mode, the AK5703 does not return an ACK after receiving a slave address by a dummy command as shown in Figure 21. Therefore, the slave address needs to be sent twice if the I<sup>2</sup>C transmitting stops after the first slave address. In the actual case, initializing cycle starts by 16 SCL clocks during the PDN pin = “H” regardless of the SDA line. Executing a write or read command to the other device that is connected to the same I<sup>2</sup>C-bus also resets the AK5703.

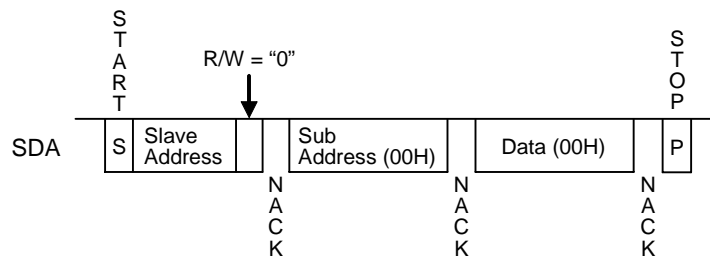


Figure 21. Dummy Command in I<sup>2</sup>C-bus Mode

The ADCA enters an initialization cycle when the PMADAL or PMADAR bit is changed from “0” to “1” on the condition of PMADAL = PMADAR bits = “0”. The initialization cycle time is set by ADRSTA1-0 bits (Table 16). The ADCB enters an initialization cycle when the PMADBL or PMADBR bit is changed from “0” to “1” on the condition of PMADBL = PMADBR bits = “0”. The initialization cycle time is set by ADRSTB1-0 bits (Table 16). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2’s complement, “0”. The ADC output reflects the analog input signal after the initialization cycle is complete.

Note 29. The initial data of ADC has offset data that depends on the condition of the microphone and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRSTA/B1-0 bits or do not use the initial data of ADC.

| ADRSTA1 bit<br>ADRSTB1 bit | ADRSTA0 bit<br>ADRSTB0 bit | Initialization Cycle |              |               |                |
|----------------------------|----------------------------|----------------------|--------------|---------------|----------------|
|                            |                            | Cycle                | fs = 44.1kHz | fs = 22.05kHz | fs = 11.025kHz |
| 0                          | 0                          | 1059/fs              | 24.0ms       | 48.0ms        | 96.1ms         |
| 0                          | 1                          | 267/fs               | 6.1ms        | 12.1ms        | 24.2ms         |
| 1                          | 0                          | 2115/fs              | 48.0ms       | 95.9ms        | 191.8ms        |
| 1                          | 1                          | 531/fs               | 12.0ms       | 24.1ms        | 48.2ms         |

(default)

Table 16. ADC Initialization Cycle

## ■ Audio Interface Format

Eight types of data formats are available and selected by setting the TDM1-0 and DIF1-0 bits (Table 17, Table 18 and Table 19). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK5703 in master mode, but must be input to the AK5703 in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK.

In TDM64 Mode at master operation, BICK output frequency is set 64fs by BCKO1-0 bits = "01".

In TDM128 Mode at master operation, BICK output frequency is set 128fs by BCKO1-0 bits = "10".

In TDM Mode, SDTOB outputs 4-ch data and SDTOA is fixed "L" output.

| Mode | TDM1 bit | TDM0 bit | DIF1 bit | DIF0 bit | SDTOA/B                           | BICK   | Figure                              |
|------|----------|----------|----------|----------|-----------------------------------|--------|-------------------------------------|
| 0    | 0        | 0        | 0        | 0        | 16bit MSB justified               | ≥ 32fs | <a href="#">Figure 22</a>           |
| 1    | 0        | 0        | 0        | 1        | 16bit I <sup>2</sup> S compatible | ≥ 32fs | <a href="#">Figure 23</a>           |
| 2    | 0        | 0        | 1        | 0        | 24bit MSB justified               | ≥ 48fs | <a href="#">Figure 24</a>           |
| 3    | 0        | 0        | 1        | 1        | 24bit I <sup>2</sup> S compatible | ≥ 48fs | <a href="#">Figure 25</a> (default) |

Table 17. Audio Interface Format (Stereo Mode) (N/A: Not Available)

| Mode | TDM1 bit | TDM0 bit | DIF1 bit | DIF0 bit | SDTOB                             | BICK | Figure                    |
|------|----------|----------|----------|----------|-----------------------------------|------|---------------------------|
| 4    | 0        | 1        | 0        | 0        | N/A                               | -    | -                         |
| 5    | 0        | 1        | 0        | 1        | N/A                               | -    | -                         |
| 6    | 0        | 1        | 1        | 0        | 16bit MSB justified               | 64fs | <a href="#">Figure 26</a> |
| 7    | 0        | 1        | 1        | 1        | 16bit I <sup>2</sup> S compatible | 64fs | <a href="#">Figure 27</a> |

Table 18. Audio Interface Format (TDM64 Mode) (N/A: Not Available)

| Mode | TDM1 bit | TDM0 bit | DIF1 bit | DIF0 bit | SDTOB                             | BICK  | Figure                    |
|------|----------|----------|----------|----------|-----------------------------------|-------|---------------------------|
| 8    | 1        | 1        | 0        | 0        | N/A                               | -     | -                         |
| 9    | 1        | 1        | 0        | 1        | N/A                               | -     | -                         |
| 10   | 1        | 1        | 1        | 0        | 24bit MSB justified               | 128fs | <a href="#">Figure 28</a> |
| 11   | 1        | 1        | 1        | 1        | 24bit I <sup>2</sup> S compatible | 128fs | <a href="#">Figure 29</a> |

Table 19. Audio Interface Format (TDM128 Mode) (N/A: Not Available)

If 24 or 16-bit data, the output of ADC, is converted to an 8-bit data by removing LSB 16 or 8-bit, "-1" data is converted to "-1" of 8-bit data. And when the DAC plays back this 8-bit data, "-1" of 8-bit data will be converted to "-65536" or "-256" of 24 or 16-bit data which is a large offset. This offset can be removed by adding the offset of "32768" or "128" to 24 or 16-bit data, respectively before converting to 8-bit data. ADC.

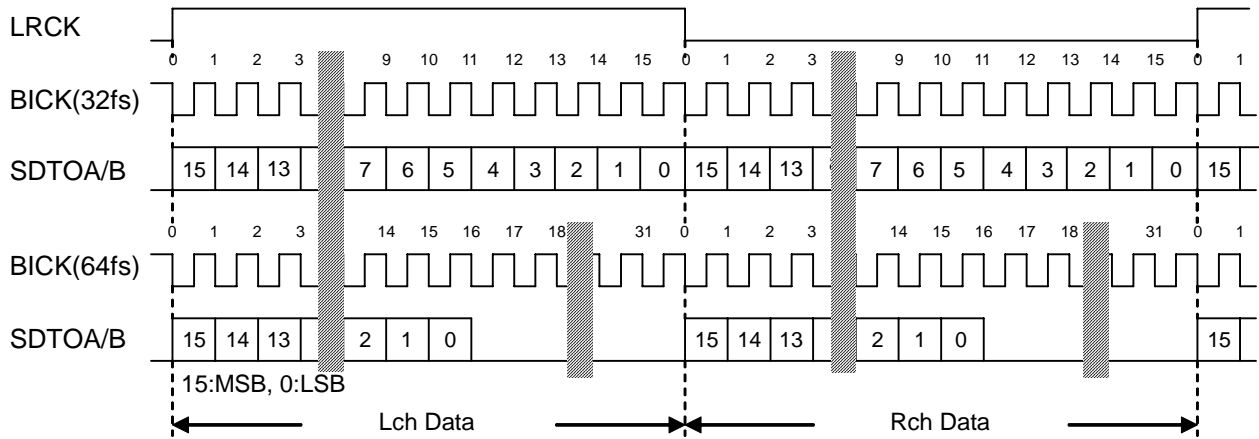


Figure 22. Mode 0 Timing (Stereo Mode, 16bit MSB justified)

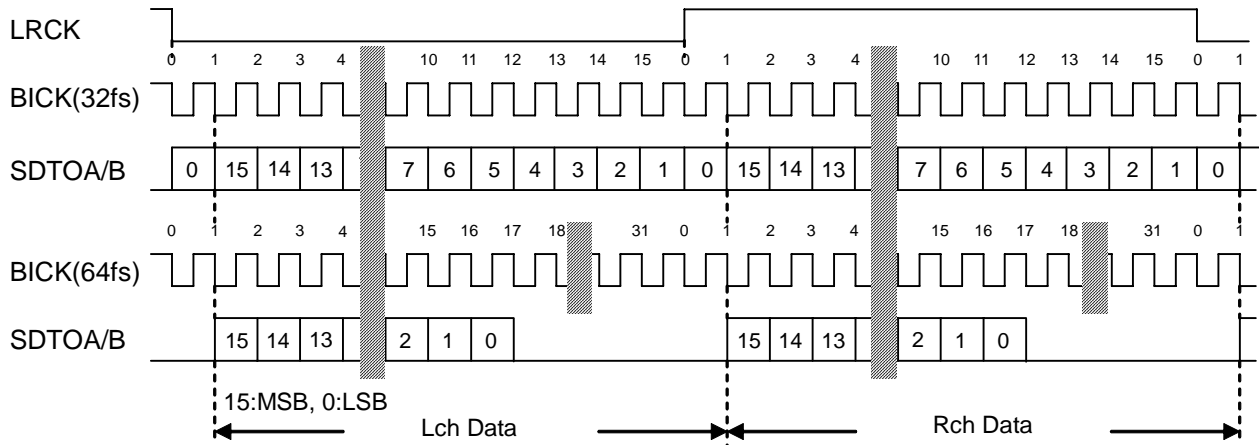


Figure 23. Mode 1 Timing (Stereo Mode, 16bit I<sup>2</sup>S compatible)

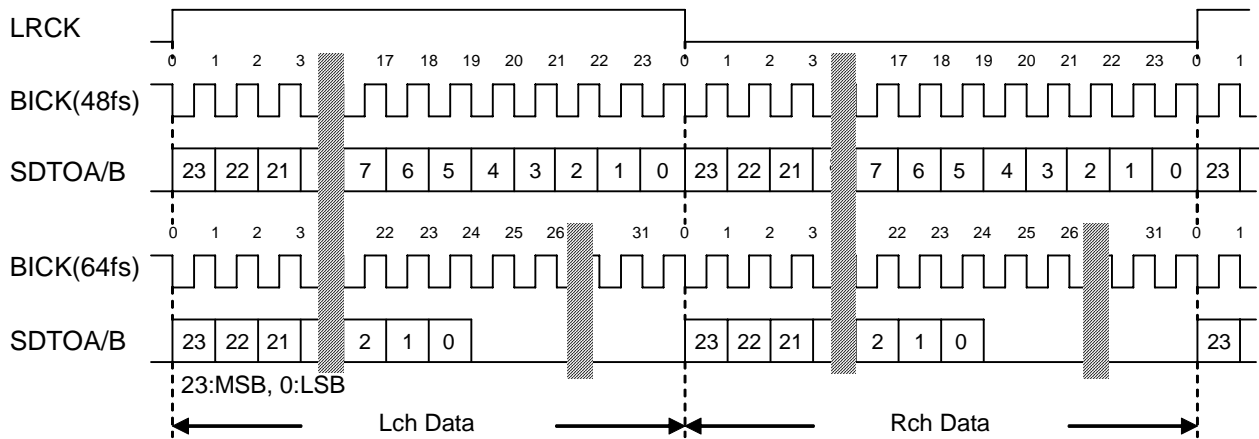


Figure 24. Mode 2 Timing (Stereo Mode, 24bit MSB justified)

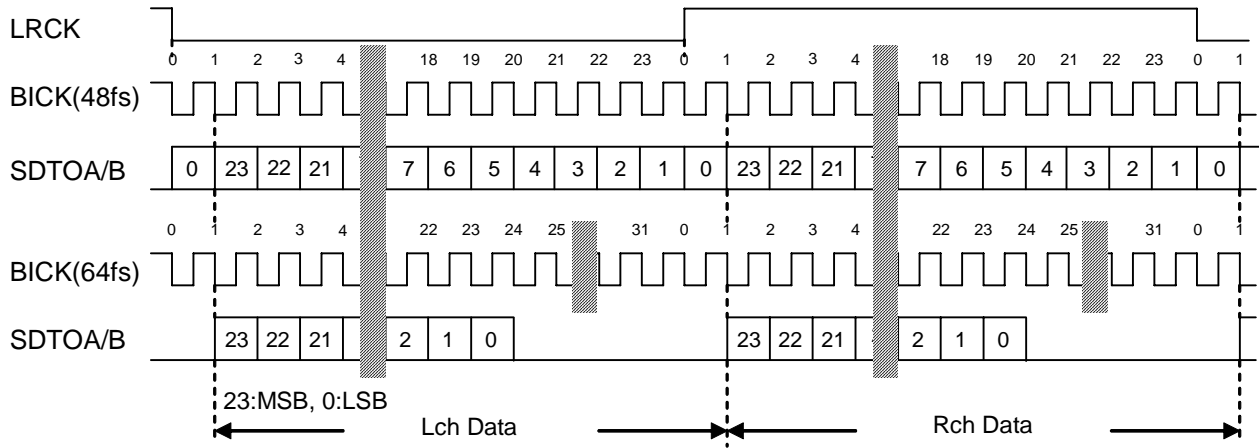


Figure 25. Mode 3 Timing (Stereo Mode, 24bit I<sup>2</sup>S compatible)

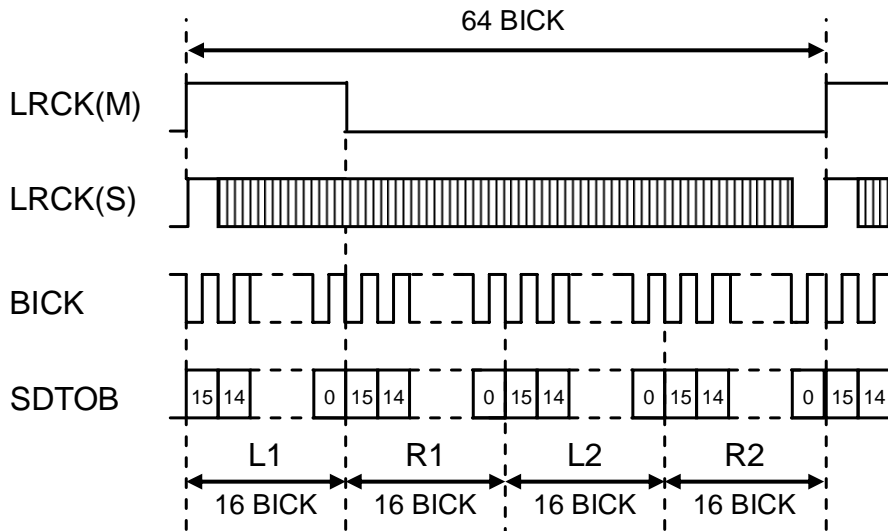


Figure 26. Mode 6 Timing (TDM64 mode, MSB justified)

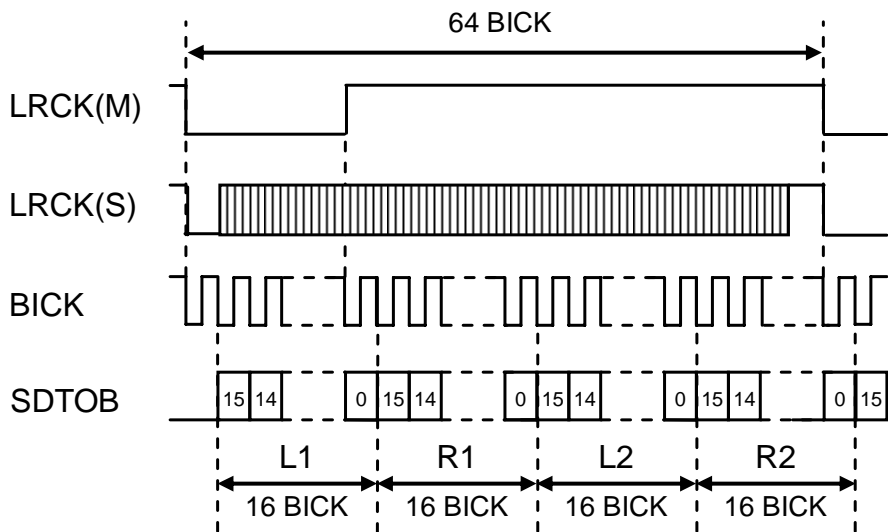


Figure 27. Mode 7 Timing (TDM64 mode, I<sup>2</sup>S compatible)

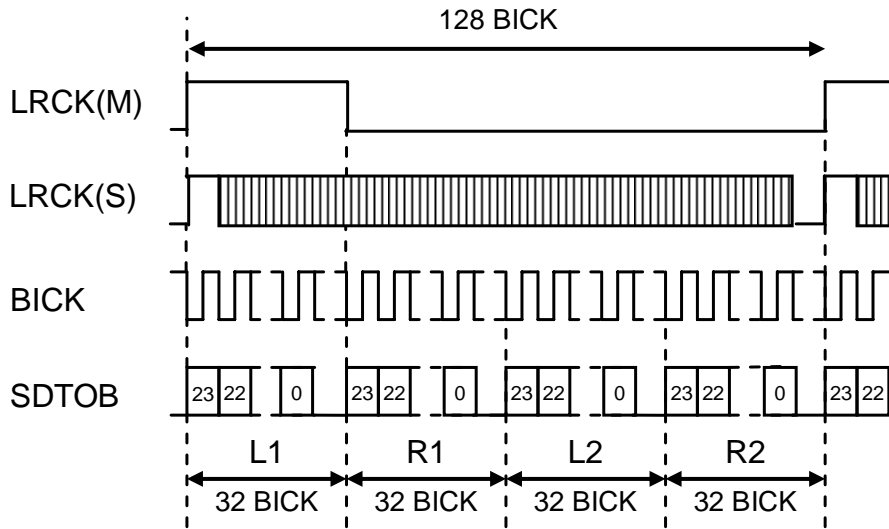


Figure 28. Mode 10 Timing (TDM128 Mode, MSB justified)

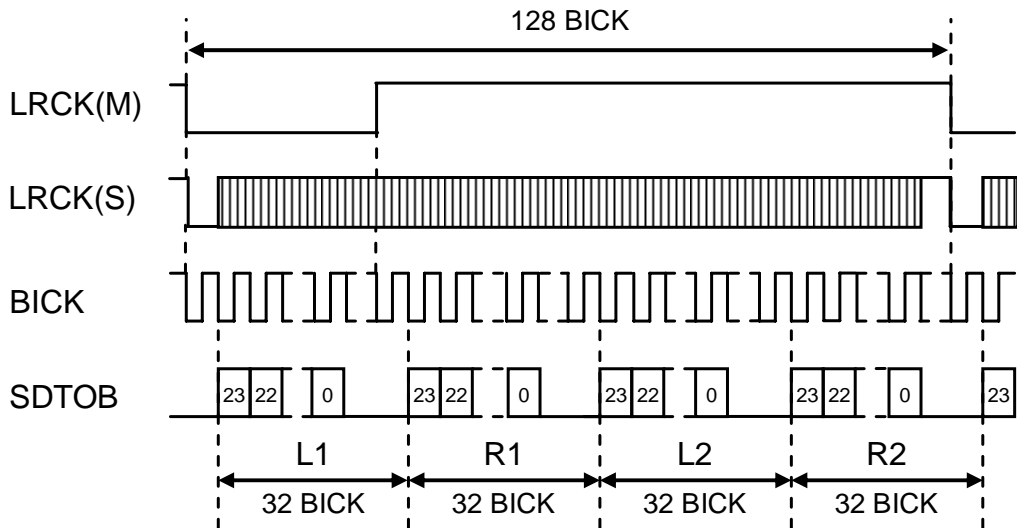


Figure 29. Mode 11 Timing (TDM128 mode, I<sup>2</sup>S compatible)

## ■ Microphone/LINE Input

The AK5703 can be selected single-ended or full differential inputs. When MDIFA1, MDIFA2, MDIFB1 and MDIFB2 bits are “0”, LIN1, RIN1, LIN2 and RIN2 pins support single-ended inputs (). When MDIFA1, MDIFA2, MDIFB1 and MDIFB2 bits are “1”, LIN1, RIN1, LIN2 and RIN2 pins become LINA+, RINA+, LINB+ and RINB+ pins, respectively. In this case, full-differential input is available in combination with LINA–, RINA–, LINB– and RINB– pins, respectively (Figure 31).

| MDIFA1 bit | MDIFA2 bit | Lch     | Rch     |           |
|------------|------------|---------|---------|-----------|
| 0          | 0          | LIN1    | RIN1    | (default) |
|            | 1          | LIN1    | RINA+/- |           |
| 1          | 0          | LINA+/- | RIN1    |           |
|            | 1          | LINA+/- | RINA+/- |           |

Table 20. ADCA MIC/Line Input Select

| MDIFB1 bit | MDIFB2 bit | Lch     | Rch     |           |
|------------|------------|---------|---------|-----------|
| 0          | 0          | LIN2    | RIN2    | (default) |
|            | 1          | LIN2    | RINB+/- |           |
| 1          | 0          | LINB+/- | RIN2    |           |
|            | 1          | LINB+/- | RINB+/- |           |

Table 21. ADCB MIC/Line Input Select

## ■ Microphone Gain Amplifier

The AK5703 has a gain amplifier for microphone input. The gain of MIC-Amp Lch and Rch is independently selected by the MGAINA2-0 and MGAINB2-0 bits (Table 22). The typical input resistance is 100kΩ.

| MGAINA2 bit<br>MGAINB2 bit | MGAINA1 bit<br>MGAINB1 bit | MGAINA0 bit<br>MGAINB0 bit | Input Gain |           |
|----------------------------|----------------------------|----------------------------|------------|-----------|
| 0                          | 0                          | 0                          | 0dB        |           |
| 0                          | 0                          | 1                          | +8dB       |           |
| 0                          | 1                          | 0                          | +12dB      |           |
| 0                          | 1                          | 1                          | +15dB      |           |
| 1                          | 0                          | 0                          | +18dB      |           |
| 1                          | 0                          | 1                          | +24dB      |           |
| 1                          | 1                          | 0                          | +30dB      | (default) |
| 1                          | 1                          | 1                          | +36dB      |           |

Table 22. Microphone Input Gain

■ Microphone Power

When PMMPA bit (PMMPB bit) = “1”, the MPWRA pin (MPWRB pin) supplies power for the microphone independently. This output voltage is typically 2.4V (0.8 x AVDD) and the load resistance is minimum 0.5kΩ. In case of using two sets of stereo microphones, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWRA and MPWRB pins (Figure 30, Figure 31).

| PMMPA bit<br>PMMPB bit | MPWRA pin<br>MPWRB pin |
|------------------------|------------------------|
| 0                      | Hi-Z                   |
| 1                      | Output                 |

(default)

Table 23. Microphone Power

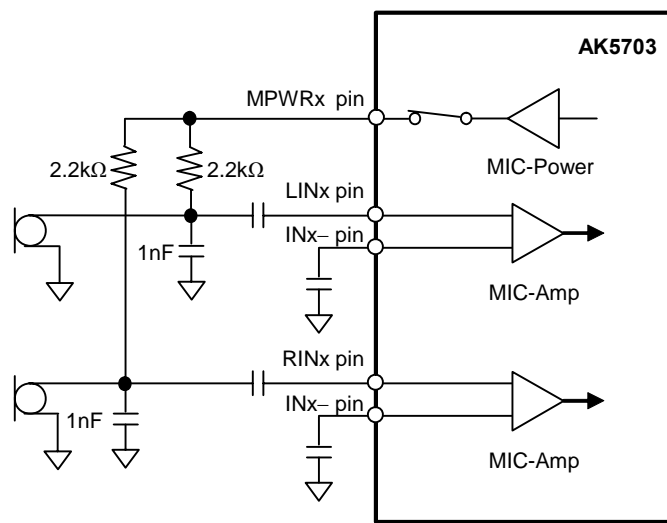


Figure 30. Connection Example for Single-ended Microphone Input

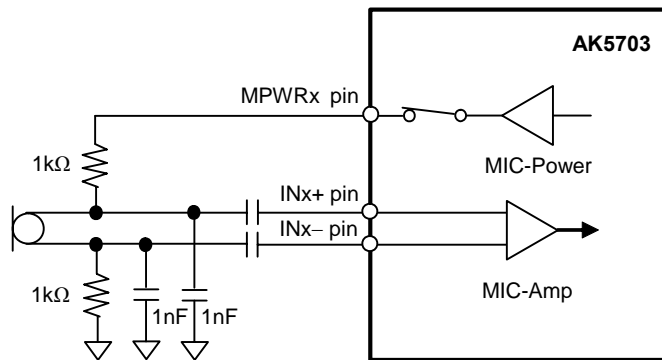


Figure 31. Connection Example for Full-differential Microphone Input (MDIFx1/2 bits = “1”)

■ Programmable Output Data Delay

Output data is independently delayed in state of 64/fs before the Decimation Filter to adjust the phase shift of each 4ch analog inputs into 4ch ADC. Setting resolution of delay amount is 1/64fs and setting range is from 1/64fs to 64/64fs. Delay function of LIN1 channel, RIN1 channel, LIN2 channel and RIN2 channel are independently controlled ON/OFF by DLY1L bit, DLY1R bit, DLY2L bit and DLY2R bits, respectively. When DLYxx bit = “0”, data delay is disable. When DLYxx bit = “1”, data delay is enable.

- DLY1L5-0 bits: Setting the amount of delay for LIN1 channel.
- DLY1R5-0 bits: Setting the amount of delay for RIN1 channel.
- DLY2L5-0 bits: Setting the amount of delay for LIN2 channel.
- DLY2R5-0 bits: Setting the amount of delay for RIN2 channel.

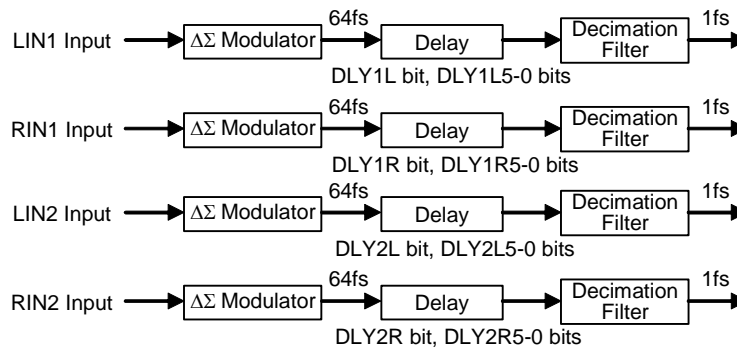


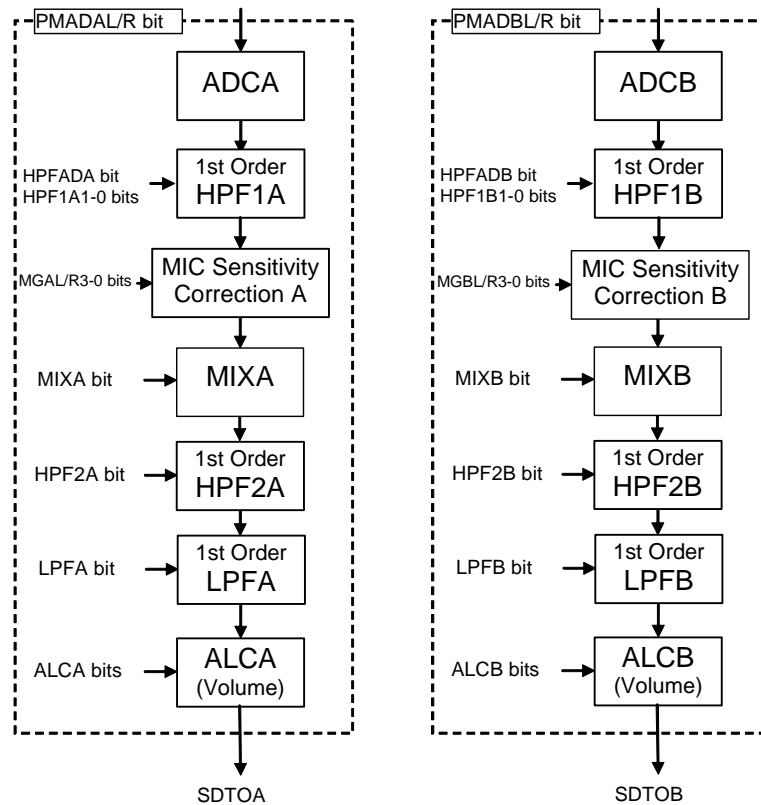
Figure 32. Programmable Output Data Delay

| DLY1L5-0 bits<br>DLY1R5-0 bits<br>DLY2L5-0 bits<br>DLY2R5-0 bits | Delay            |
|--|------------------|
| 3FH  | 64/64fs          |
| 3EH  | 63/64fs          |
| 3DH  | 62/64fs          |
| ⋮  | ⋮                |
| 02H  | 3/64fs           |
| 01H  | 2/64fs           |
| 00H  | 1/64fs (default) |

Table 24. Programmable Output Data Delay setting

## ■ Digital Block

The digital block consists of the blocks shown in [Figure 33](#). When HPFADA/B = HPF2A/B = LPFA/B bits = “1”, HPF1A/B, HPF2A/B and LPFA/B are available. When HPF2A/B = LPFA/B bits = “0”, ADCA/B data bypass the HPF2A/B and LPFA/B and is input to ALCA/B.



- (1) ADCA/B: Includes the Digital Filter (LPF) for ADC as shown in “[FILTER CHARACTERISTICS](#)” and the Programmable Output Data Delay as shown in “[Programmable Output Data Delay](#)”.
- (2) HPF1A/B: Includes the Digital Filter (HPF) for ADC as shown in “[Digital HPF1A/B](#)”.
- (3) Microphone Sensitivity Correction A/B:  
Includes the Microphone Sensitivity Correction as shown in “[Microphone Sensitivity Correction](#)”.
- (4) MIXA/B: Mono/Stereo Mode (See “[Mono/Stereo Mode \(MIXA/B\)](#)”)
- (5) HPF2A/B: High Pass Filter (See “[High Pass Filter \(HPF2A/B\)](#)”)
- (6) LPFA/B: Low Pass Filter (See “[Low Pass Filter \(LPFA/B\)](#)”)
- (7) ALCA/B(Volume): Digital Volume with ALC Function (See “[Input Digital Volume \(Manual Mode\)](#)” and “[ALC Operation](#)”)

Figure 33. Digital Block Path Select

### ■ Digital HPF1A/B

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. When HPFADA/B bits = “1”, HPF1A/B are available (while using ADC, HPFADA/B bit should be set to “1”). The cut-off frequencies of the HPF1A (HPF1B) are set by HPF1A1-0 (HPF1B1-0) bits (Table 25). It is proportional to the sampling frequency ( $f_s$ ) and default is 3.4Hz (@ $f_s = 44.1\text{kHz}$ ).

| HPF1A1 bit<br>HPF1B1 bit | HPF1A0 bit<br>HPF1B0 bit | fc                   |                       |                        | (default) |
|--------------------------|--------------------------|----------------------|-----------------------|------------------------|-----------|
|                          |                          | $f_s=44.1\text{kHz}$ | $f_s=22.05\text{kHz}$ | $f_s=11.025\text{kHz}$ |           |
| 0                        | 0                        | 3.4Hz                | 1.7Hz                 | 0.85Hz                 |           |
| 0                        | 1                        | 6.8Hz                | 3.4Hz                 | 1.7Hz                  |           |
| 1                        | 0                        | 13.6Hz               | 6.8Hz                 | 3.4Hz                  |           |
| 1                        | 1                        | 219.3Hz              | 109.7Hz               | 54.8Hz                 |           |

Table 25. HPF1A/B Cut-off Frequency

### ■ Microphone Sensitivity Correction

The AK5703 has microphone sensitivity correction function controlled by MGxx3-0 bits. ADCA Lch gain is controlled by MGAL3-0 bits, ADCA Rch gain is controlled by MGAR3-0 bits, ADCB Lch gain is controlled by MGBL3-0 bits and ADCB Rch gain is controlled by MGBR3-0 bits (Table 26).

| MGAL3-0 bits<br>MGAR3-0 bits<br>MGBL3-0 bits<br>MGBR3-0 bits | GAIN (dB) | Step | (default) |
|--|-----------|------|-----------|
| 1000   | +3        | 0.75 |           |
| 0111   | +2.25     |      |           |
| 0110   | +1.5      |      |           |
| 0101   | +0.75     |      |           |
| 0100   | 0         |      |           |
| 0011   | -0.75     |      |           |
| 0010   | -1.5      |      |           |
| 0001   | -2.25     |      |           |
| 0000   | -3        |      |           |
| Others   | N/A       |      |           |

Table 26. Microphone Sensitivity Correction (N/A: Not available)

### ■ Mono/Stereo Mode (MIXA/B)

PMADAL, PMADAR and MIXA bits select mono or stereo mode of ADCA output data. PMADBL, PMADBR and MIXB bits select mono or stereo mode of ADCB output data. ALC operation (ALCA/B or ALC4 bit = "1") or digital volume operation (ALCA/B = ALC4 bits = "0") is applied to the data in [Table 27](#) and [Table 28](#).

| PMADAL bit | PMADAR bit | MIXA bit | ADCA Lch data    | ADCA Rch data    |
|------------|------------|----------|------------------|------------------|
| 0          | 0          | x        | All "0"          | All "0"          |
| 0          | 1          | x        | Rch Input Signal | Rch Input Signal |
| 1          | 0          | x        | Lch Input Signal | Lch Input Signal |
| 1          | 1          | 0        | Lch Input Signal | Rch Input Signal |
|            |            | 1        | (L+R)/2          | (L+R)/2          |

(default)

Table 27. ADCA Mono/Stereo Mode (x: Don't care)

| PMADBL bit | PMADBR bit | MIXB bit | ADCB Lch data    | ADCB Rch data    |
|------------|------------|----------|------------------|------------------|
| 0          | 0          | x        | All "0"          | All "0"          |
| 0          | 1          | x        | Rch Input Signal | Rch Input Signal |
| 1          | 0          | x        | Lch Input Signal | Lch Input Signal |
| 1          | 1          | 0        | Lch Input Signal | Rch Input Signal |
|            |            | 1        | (L+R)/2          | (L+R)/2          |

(default)

Table 28. ADCB Mono/Stereo Mode (x: Don't care)

### ■ High Pass Filter (HPF2A/B)

This is composed 1st order HPF. The coefficient of HPF2A is set by FA1A13-0 bits and FA1B13-0 bits. The coefficient of HPF2B is set by FB1A13-0 bits and FB1B13-0 bits. HPF2A bit controls ON/OFF of the HPF2A and HPF2B bit controls ON/OFF of the HPF2B. When the HPF2A/B is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when HPFA = HPF2B bits = "0". The HPF2A/B starts operation  $4/fs(\max)$  after when HPF2A bit = "1" (HPF2B bit = "1") is set.

fs: Sampling frequency

fc: Cut-off frequency

Register setting ([Note 30](#))

HPF: Fx1A[13:0] bits =A, Fx1B[13:0] bits =B  
(MSB=Fx1A13, Fx1B13; LSB=Fx1A0, Fx1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.

$$fc/fs \geq 0.0001 \quad (fc \text{ min} = 4.41\text{Hz at } 44.1\text{kHz})$$

### ■ Low Pass Filter (LPFA/B)

This is composed with 1st order LPF. FA2A13-0 bits and FA2B13-0 bits set the coefficient of LPFA. FB2A13-0 bits and FB2B13-0 bits set the coefficient of LPFB. LPFA bit controls ON/OFF of the LPFA and LPFB bit controls ON/OFF of the LPFB. When the LPFA/B is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when LPFA = LPFB bits = "0". The LPFA/B starts operation  $4/f_s(\text{max})$  after when LPFA bit = "1" (LPFB bit = "1") is set.

$f_s$ : Sampling frequency

$f_c$ : Cut-off frequency

Register setting (Note 30)

LPF: Fx2A[13:0] bits =A, Fx2B[13:0] bits =B  
(MSB=Fx2A13, Fx2B13; LSB=Fx2A0, Fx2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.

$$f_c / f_s \geq 0.05 \quad (f_c \text{ min} = 2205\text{Hz at } 44.1\text{kHz})$$

Note 30. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]

$$X = (\text{Real number of filter coefficient calculated by the equations above}) \times 2^{13}$$

X must be rounded to integer, and then should be translated to binary code (2's complement).

MSB of each filter coefficient setting register is sign bit.

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALCA (2ch) block when ALCA bit is “1” and operated by ALCB (2ch) block when ALCB bit is “1”. In this case, both Lch and Rch VOL values are changed together. When ALC4 bit = “0” and ALCA = ALCB bits = “1”, ALC of ADCA and ADCB are independently operated. When ALC4 bit = “1” regardless of ALCA and ALCB bits, ALC is operated for all 4ch of the ADCA and ADCB. In this case, the VOL value is always changed in common with all channels. 4ch Link ALC is operated by the register setting of ADCA (LMTHA1-0, RGAINA2-0, REFA7-0 and RFSTA1-0 bits). In this case, ALC setting of ADCB (LMTHB1-0, RGAINB2-0, REFB7-0 and RFSTB1-0 bits) is invalid.

The ALC block consists of these blocks shown below. ALC limiter detection level and ALC recovery wait counter reset level are monitored at Level Detection 2 block after EQ block. The Level Detection 1 block also monitors clipping detection level (+0.53dBFS).

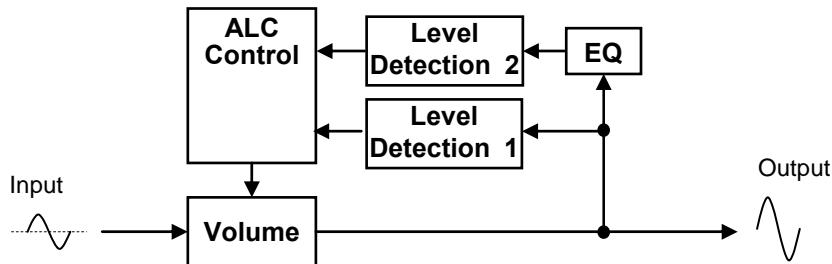


Figure 34. ALC Block

The polar ( $fc_1$ ) and zero-point ( $fc_2$ ) frequencies of EQ block are dependent on the sampling frequency. The coefficient is changed automatically according to the sampling frequency range setting. When ALC EQ block is OFF (ALCEQ bit = “1”), these level detection are off.

| Sampling Frequency Range                                | Polar Frequency ( $fc_1$ ) | Zero-point Frequency ( $fc_2$ ) |                 |
|---|----------------------------|---------------------------------|-----------------|
| 8kHz ≤ $f_s$ ≤ 12kHz<br>(FS1 bit = “0”)                 | 150Hz                      | 100Hz                           | $f_s=11.025kHz$ |
| 12kHz < $f_s$ ≤ 24kHz<br>(FS3 bit = “0”, FS1 bit = “1”) | 150Hz                      | 100Hz                           | $f_s=22.05kHz$  |
| 24kHz < $f_s$ ≤ 48kHz<br>(FS3 bit = “1”, FS1 bit = “1”) | 150Hz                      | 100Hz                           | $f_s=44.1kHz$   |

Table 29. ALCEQ Frequency Setting

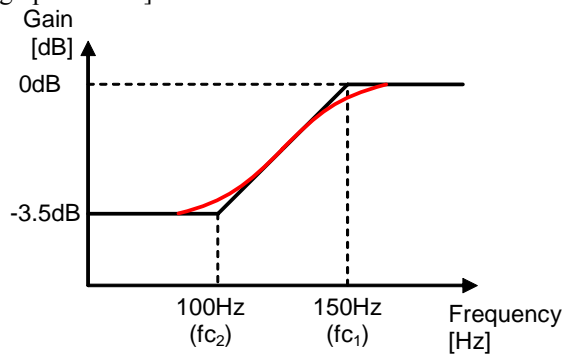
$f_s$ : Sampling Frequency  
 $fc_1$ : Polar Frequency  
 $fc_2$ : Zero-point Frequency

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2 / f_s)}{1 + 1 / \tan(\pi fc_1 / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1 / f_s)}{1 + 1 / \tan(\pi fc_1 / f_s)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2 / f_s)}{1 + 1 / \tan(\pi fc_1 / f_s)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

[ ALCEQ: First order zero pole high pass filter ]



Note 31. Black: Diagrammatic Line, Red: Actual Curve  
Figure 35. Frequency Response (fs = 44.1kHz)

1. ALC Limiter Operation

During 2ch Link ALC limiter operation, when either L or R channel output level exceeds the ALC limiter detection level (Table 31), the VOL value (same value for both L and R) is attenuated automatically according to the output level (Table 32). The volume is attenuated by the step amount shown in Table 32 at every sampling. During 4ch Link ALC limiter operation, when either L or R channel output level of ADCA or ADCB exceeds the ALC limiter detection level (Table 31), the VOL value (same value for both L and R) is attenuated automatically according to the output level (Table 32). The volume is attenuated by the step amount shown in Table 32 at every sampling. This attenuation is repeated for sixteen times once ALC limiter operation is executed.

After completing the attenuate operation, unless ALC operation is changed to manual mode, the operation repeats when the input signal level exceeds ALC limiter detection level.

| Mode | ALC4 bit | ALCB bit | ALCA bit | ALCB Operation | ALCA Operation |
|------|----------|----------|----------|----------------|----------------|
| 0    | 0        | 0        | 0        | Manual         | Manual         |
| 1    | 0        | 0        | 1        | Manual         | 2ch Link       |
| 2    | 0        | 1        | 0        | 2ch Link       | Manual         |
| 3    | 0        | 1        | 1        | 2ch Link       | 2ch Link       |
| 4    | 1        | x        | x        | 4ch Link       |                |

(default)

Note 32. ALC4 bit must be set when ALCA = ALCB bits = “0” or PMADAL = PMADAR = PMADBL = PMADBR bits = “0”. When ALC4 bit = “1”, only either ADCA or ADCB must not be power down.

Table 30. ALC Mode

| LMTHA/B1 bits | LMTHA/B0 bits | ALC Limiter Detection Level (LM-LEVEL) | ALC Recovery Waiting Counter Reset Level |
|---------------|---------------|--|--|
| 0             | 0             | ALC Output $\geq$ -2.5dBFS             | -2.5dBFS > ALC Output $\geq$ -4.1dBFS    |
| 0             | 1             | ALC Output $\geq$ -4.1dBFS             | -4.1dBFS > ALC Output $\geq$ -6.0dBFS    |
| 1             | 0             | ALC Output $\geq$ -6.0dBFS             | -6.0dBFS > ALC Output $\geq$ -8.5dBFS    |
| 1             | 1             | ALC Output $\geq$ -8.5dBFS             | -8.5dBFS > ALC Output $\geq$ -12dBFS     |

(default)

Table 31. ALC Limiter Detection Level / Recovery Counter Reset Level

| Output Level   | ATT Step [dB] |
|--|---------------|
| +0.53dBFS $\leq$ Output Level (Level Detection 1)                | 0.38148       |
| -1.16dBFS $\leq$ EQ Output Level (Level Detection 2) < +0.53dBFS | 0.06812       |
| LM-LEVEL $\leq$ EQ Output Level (Level Detection 2) < -1.16dBFS  | 0.02548       |

Table 32. ALC Limiter ATT Amount

## 2. ALC Recovery Operation

ALC recovery operation waits for the time set by WTM1-0 bits (Table 33) after completing ALC limiter operation. If the input signal does not exceed “ALC recovery waiting counter reset level” (Table 31) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by the amount set by RGAINA/B2-0 bits (Table 34) up to the set reference level (Table 35) in every one sampling. When the VOL value exceeds the reference level (REFA/B7-0), the VOL values are not increased.

When

“ALC recovery waiting counter reset level  $\leq$  Output Signal  $<$  ALC limiter detection level” during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When

“ALC recovery waiting counter reset level  $>$  Output Signal”, the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFSTA/B1-0 bits (Table 36). The ATT amount for reference volume of fast recovery operation is set by FRATT bit (Table 37).

| WTM1 bit | WTM0 bit | Recovery Wait Time |
|----------|----------|--------------------|
| 0        | 0        | 128/fs             |
| 0        | 1        | 256/fs             |
| 1        | 0        | 512/fs             |
| 1        | 1        | 1024/fs            |

(default)

Table 33. ALC Recovery Operation Waiting Period

| RGAINA/B2 bits | RGAINA/B1 bits | RGAINA/B0 bits | GAIN Step [dB] | GAIN Switching Timing |
|----------------|----------------|----------------|----------------|-----------------------|
| 0              | 0              | 0              | 0.00424        | 1/fs                  |
| 0              | 0              | 1              | 0.00212        | 1/fs                  |
| 0              | 1              | 0              | 0.00106        | 1/fs                  |
| 0              | 1              | 1              | 0.00106        | 2/fs                  |
| 1              | 0              | 0              | 0.00106        | 4/fs                  |
| 1              | 0              | 1              | 0.00106        | 8/fs                  |
| 1              | 1              | 0              | 0.00106        | 16/fs                 |
| 1              | 1              | 1              | 0.00106        | 32/fs                 |

(default)

Table 34. ALC Recovery GAIN Step

| REFA/B7-0 bits | GAIN [dB] | Step                  |
|----------------|-----------|-----------------------|
| F1H            | +36.0     | 0.375 dB<br>(default) |
| E0H            | +35.625   |                       |
| EFH            | +35.25    |                       |
| :              | :         |                       |
| E1H            | +30.0     |                       |
| :              | :         |                       |
| 92H            | +0.375    |                       |
| 91H            | 0.0       |                       |
| 90H            | -0.375    |                       |
| :              | :         |                       |
| 06H            | -52.125   |                       |
| 05H            | -52.5     |                       |
| 04H ~ 00H      | MUTE      |                       |

Table 35. Reference Level at ALC Recovery Operation

| RFSTA/B1-0 bits | Fast Recovery Gain Step [dB] |
|-----------------|------------------------------|
| 00              | 0.0032                       |
| 01              | 0.0042                       |
| 10              | 0.0064                       |
| 11              | 0.0127                       |

Table 36. Fast Recovery Gain Step

| FRATT bit | ATT Amount [dB] | ATT Change Timing |
|-----------|-----------------|-------------------|
| 0         | -0.00106        | 4/fs              |
| 1         | -0.00106        | 16/fs             |

Table 37. ATT Amount for Reference Volume of Fast Recovery

3. Example of ALC Setting

Table 38 shows the examples of the ALC setting for recording path.

| Register Name           | Comment                            | fs=8kHz |           | fs=44.1kHz |                     |
|-------------------------|------------------------------------|---------|-----------|------------|---------------------|
|                         |                                    | Data    | Operation | Data       | Operation           |
| LMTHA/B1-0              | Limiter detection Level            | 01      | -4.1dBFS  | 01         | -4.1dBFS            |
| WTM1-0                  | Recovery waiting period            | 01      | 32ms      | 11         | 23.2ms              |
| REFA/B7-0               | Maximum gain at recovery operation | E1H     | +30dB     | E1H        | +30dB               |
| IVA/BL7-0,<br>IVA/BR7-0 | Gain of IVOL                       | E1H     | +30dB     | E1H        | +30dB               |
| RGAINA/B2-0             | Recovery GAIN                      | 000     | 0.00424dB | 011        | 0.00106dB<br>(2/fs) |
| RFSTA/B1-0              | Fast Recovery GAIN                 | 11      | 0.0127dB  | 00         | 0.0032dB            |
| ALCEQN                  | ALC EQ disable                     | 0       | Enable    | 0          | Enable              |
| ALCA/B                  | ALC enable                         | 1       | Enable    | 1          | Enable              |

Table 38. Example of the ALC Setting

4. Example of registers set-up sequence of ALC Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is finished by ALCA/B = ALC4 bits = "0". The volume is changed by soft transition to each gain of IVOL (IVA/BL7-0, IVA/BR7-0 bits) until manual mode starts after ALCA/B = ALC4 bits are set to "0".

**LMTHA/B1-0, WTM1-0, REFA/B7-0, RGAINA/N2-0, RFSTA/B1-0, FRATT and ALCEQN bits**

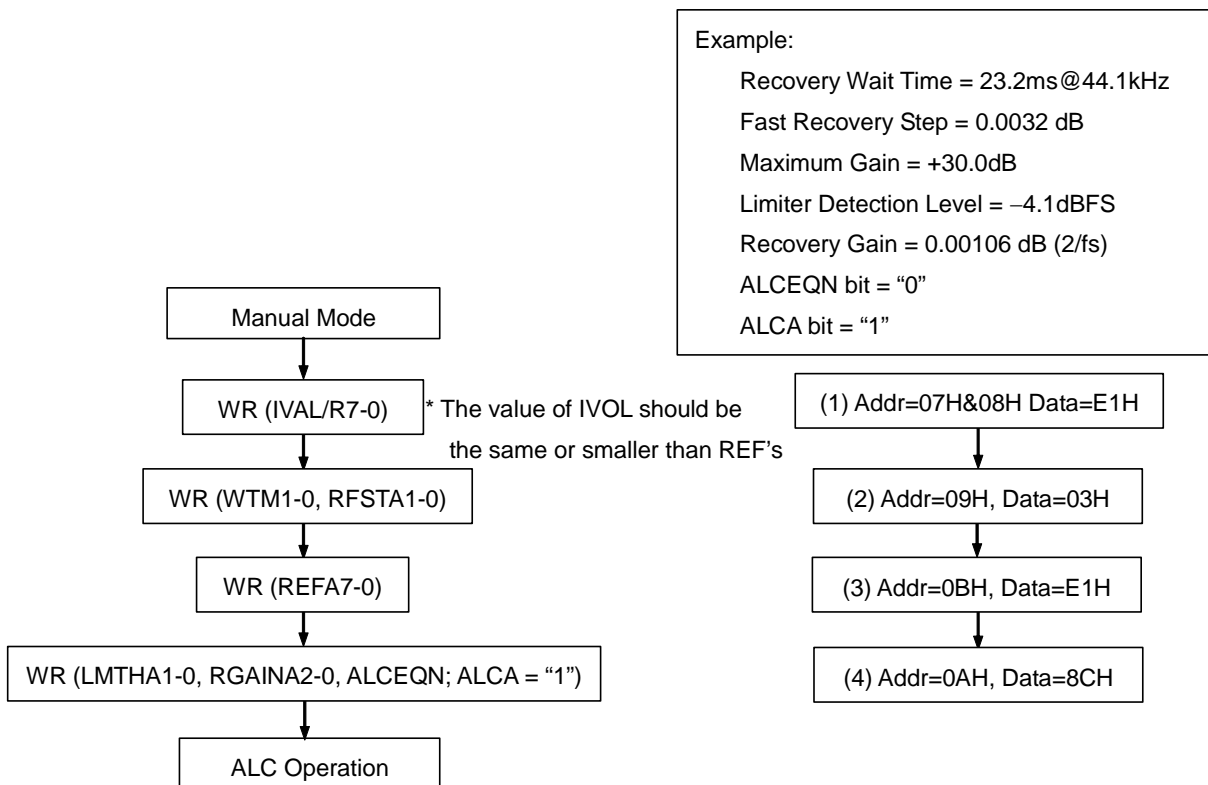


Figure 36. Registers Set-up Sequence in ALC Operation

### ■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode by setting ALCA/B = ALC bits = “0”. This mode is used in the case shown below.

1. After exiting reset state, when setting up the registers for ALC operation (such as LMTHA/B bits and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed.  
For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IVA/BL7-0 and IVA/BR7-0 bits set the gain of the digital input volume (Table 39). ALch and ARch volumes are set individually by IVAL7-0 and IVAR7-0 bits when IVOLAC bit = “0”. IVAL7-0 bits control both ALch and ARch volumes together when IVOLAC bit = “1”. BLch and BRch volumes are set individually by IVBL7-0 and IVBR7-0 bits when IVOLBC bit = “0”. IVBL7-0 bits control both BLch and BRch volumes together when IVOLBC bit = “1”. This volume has a soft transition function at 0.09375dB/fs (IVTM bit = “1”). Therefore no switching noise occurs during the transition. When IVTM bit = “01”, it takes 944/fs (21.4ms@fs=44.1kHz) from F1H(+36dB) to 05H(-52.5dB). The volume is muted after transitioned to -72dB (208/fs=4.7ms @fs=44.1kHz) in the period set by IVTM bit when changing the volume from 05H (-52.5dB) to 00H (MUTE). When IVA/BL7-0 bits and IVA/BR bits are set in series, should be set at soft transition time interval

If IVA/BL7-0 or IVA/BR7-0 bits are written during PMADA/BL = PMADA/BR bits = “0”, IVOL operation starts with the written values after PMADA/BL or PMADA/BR bits are changed to “1” waiting the ADC initialization cycle time.

| IVA/BL7-0 bits<br>IVA/BR7-0 bits | GAIN [dB] | Step                  |
|----------------------------------|-----------|-----------------------|
| F1H                              | +36.0     | 0.375 dB<br>(default) |
| E0H                              | +35.625   |                       |
| EFH                              | +35.25    |                       |
| :                                | :         |                       |
| E1H                              | +30.0     |                       |
| :                                | :         |                       |
| 92H                              | +0.375    |                       |
| 91H                              | 0.0       |                       |
| 90H                              | -0.375    |                       |
| :                                | :         |                       |
| 06H                              | -52.125   |                       |
| 05H                              | -52.5     |                       |
| 04H ~ 00H                        | MUTE      |                       |

Table 39. Input Digital Volume Setting

| IVTM bit | Transition Time from F1H to 05H (IVA/BL7-0, IVA/BR7-0 bits) |         |            |
|----------|---|---------|------------|
|          | Setting   | fs=8kHz | fs=44.1kHz |
| 0        | 236/fs  | 29.5ms  | 5.4ms      |
| 1        | 944/fs  | 118ms   | 21.4ms     |

Table 40. Transition Time Setting of Input Digital Volume

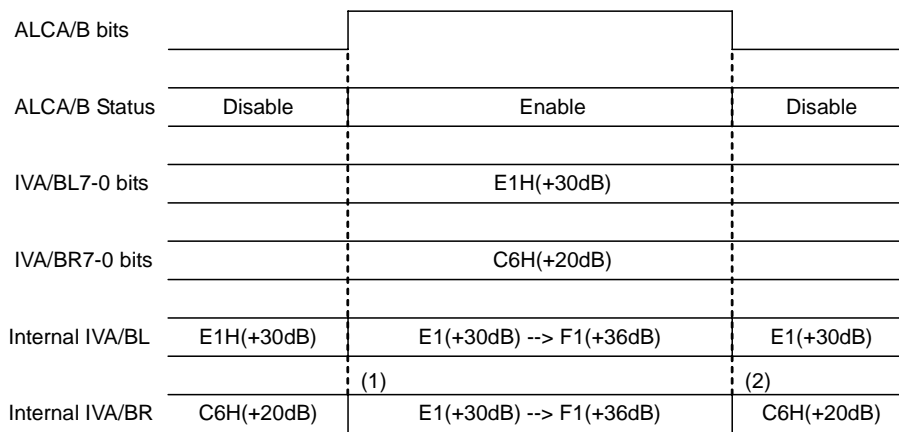


Figure 37. Example of IVOL value during 2ch ALC (ALC4 bit = “0”)

- (1) The IVA/BL value becomes the start value if the IVA/BL and IVA/BR are different when an ALC operation starts. The wait time from ALCA/B bits = “1” to ALC operation start by IVA/BL7-0 bits is at most recovery time (WTM1-0 bits).
- (2) Writing to IVA/BL and IVA/BR registers (07H, 08H, 17H and 18H) is ignored during ALC operation. After ALC is disabled, the IVOL changes to each IVA/BL or IVA/BR value by soft transition. When ALC is enabled again, ALCA/B bit should be set to “1” with an interval more than soft transition time after ALCA/B bit = “0”.

■ ALC 4ch Link Mode sequence

Figure 38 shows the 4ch Link ALC Mode sequence at ALCA bit = ALCB bit = “0”, when ALC4 bit = “0” → “1”.

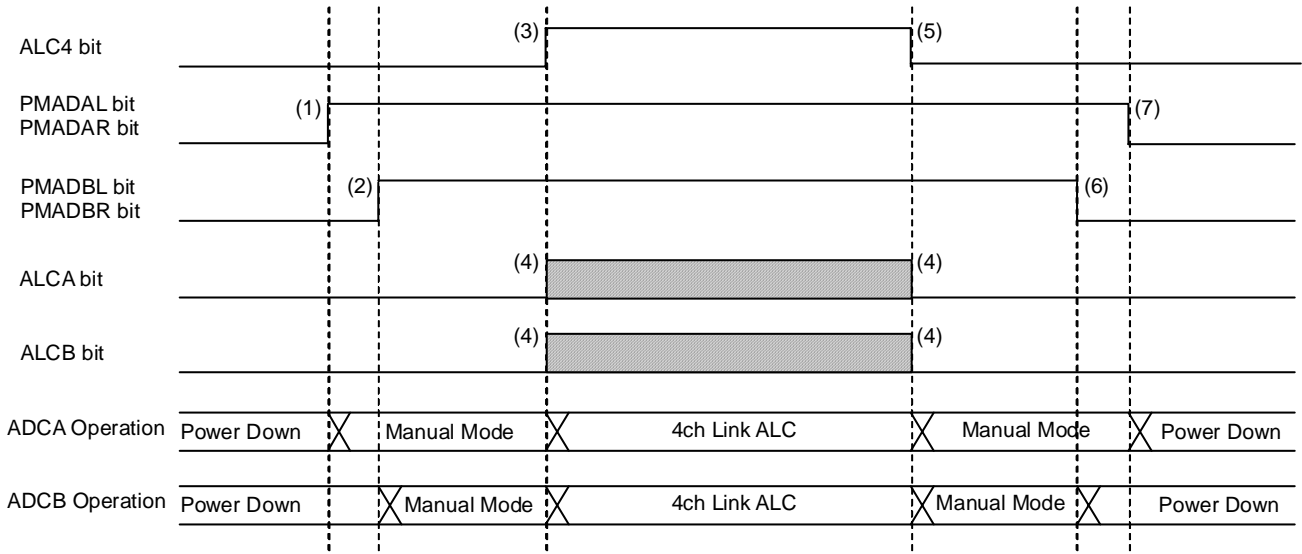


Figure 38. 4ch Link ALC Mode Sequence (ALC4 bit = “1”)

- (1) ADCA is powered up by PMADAL bit and PMADAR bit are changed from “0” to “1”.
- (2) ADCB is powered up by PMADBL bit and PMADBR bit are changed from “0” to “1”.
- (3) Both ADCA and ADCB start ALC operation together (4ch Link ALC) by changing ALC4 bit from “0” to “1”. At this point the start value of ALC is Lch of ADCA (IVAL7-0 bits).
- (4) When ALC4 bit = “1”, ALCA bit and ALCB bit become invalid. But these bits should be “0”, when ALC4 bit is changed.
- (5) When ALC4 bit = “1” → “0”, ADCA and ADCB become Manual Mode. 2ch link mode can also be set without stopping operation by setting ALCA and ALCB bits = “1”.
- (6) ADCB is powered down by setting PMADBL bit and PMADBR bit “0”.
- (7) ADCA is powered down by setting PMADAL bit and PMADAR bit “0”.



Note 33. When CSN “↑” was written before “↑” of 8th CCLK in continuous data writing mode, the previous data writing address becomes valid and the writing address is ignored.

Note 34. After 8bits data in the last address became valid, put the CSN pin “H” to complete the write command. If the CDTIO and CCLK inputs are continued when the CSN pin = “L”, the data in the next address, which is incremented, is over written.

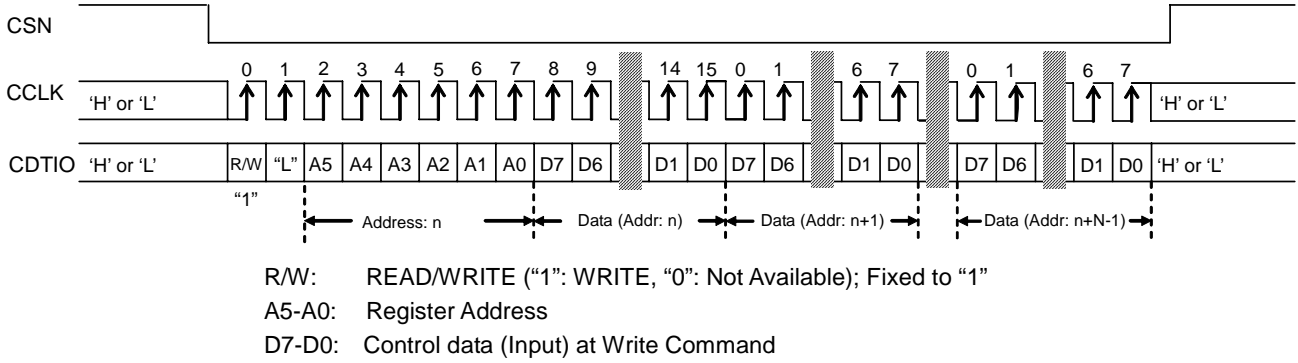


Figure 40. Serial Control Interface Timing 2 (Continuous Writing Mode)

(2) I2C-bus Control Mode (I2C pin = "H")

The AK5703 supports the fast-mode I<sup>2</sup>C-bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to (TVDD+0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 41 shows the data transfer sequence for the I<sup>2</sup>C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 47). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 42). If the slave address matches that of the AK5703, the AK5703 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 48). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5703. The format is MSB first, and those most significant 2bit is fixed to zero (Figure 43). The data after the third byte contains control data. The format is MSB first, 8bits (Figure 44). The AK5703 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 47).

The AK5703 can perform more than one byte write operation per sequence. After receipt of the third byte the AK5703 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "37H" prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 49) except for the START and STOP conditions.

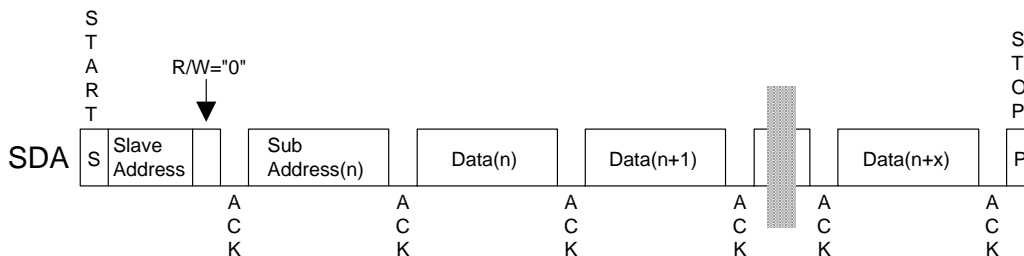


Figure 41. Data Transfer Sequence at I<sup>2</sup>C Bus Mode

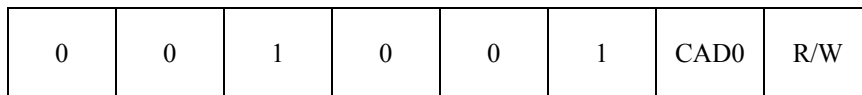


Figure 42. The First Byte

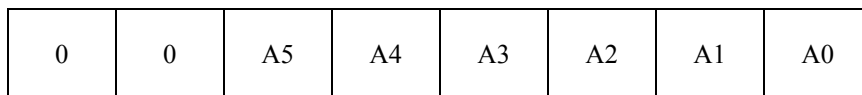


Figure 43. The Second Byte

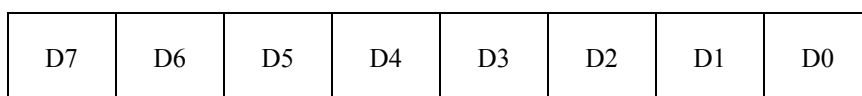


Figure 44. The Third Byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK5703. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 37H prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK5703 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK5703 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK5703 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5703 ceases the transmission.

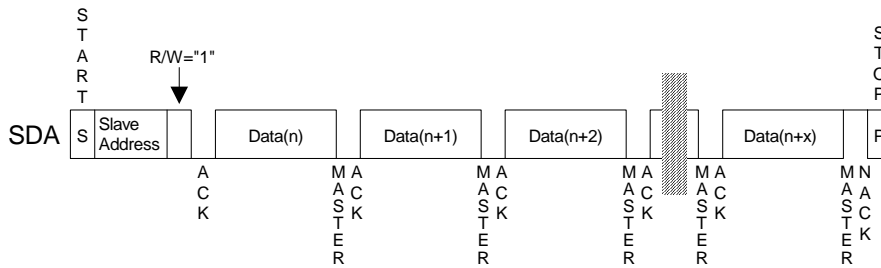


Figure 45. Current Address Read

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK5703 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK5703 ceases the transmission.

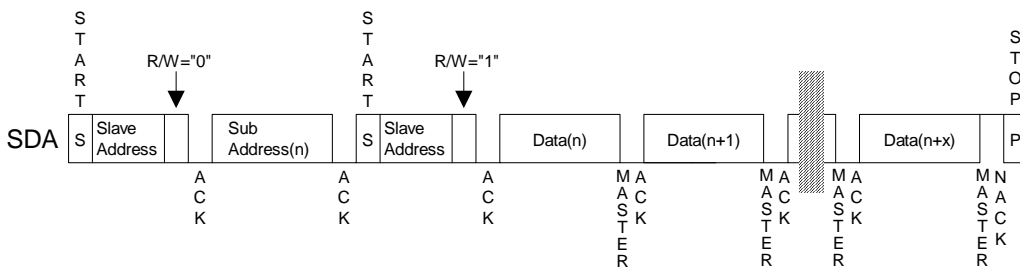


Figure 46. Random Address Read

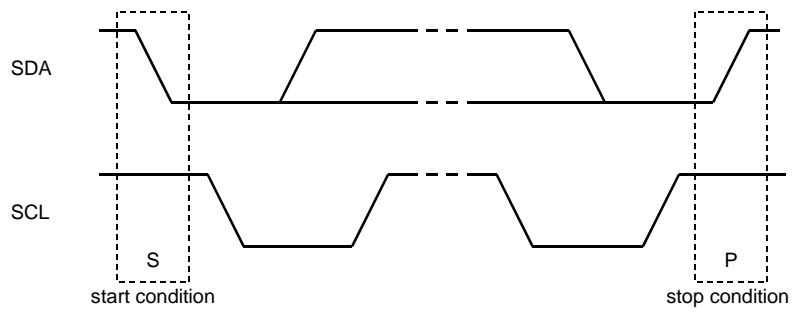


Figure 47. Start Condition and Stop Condition

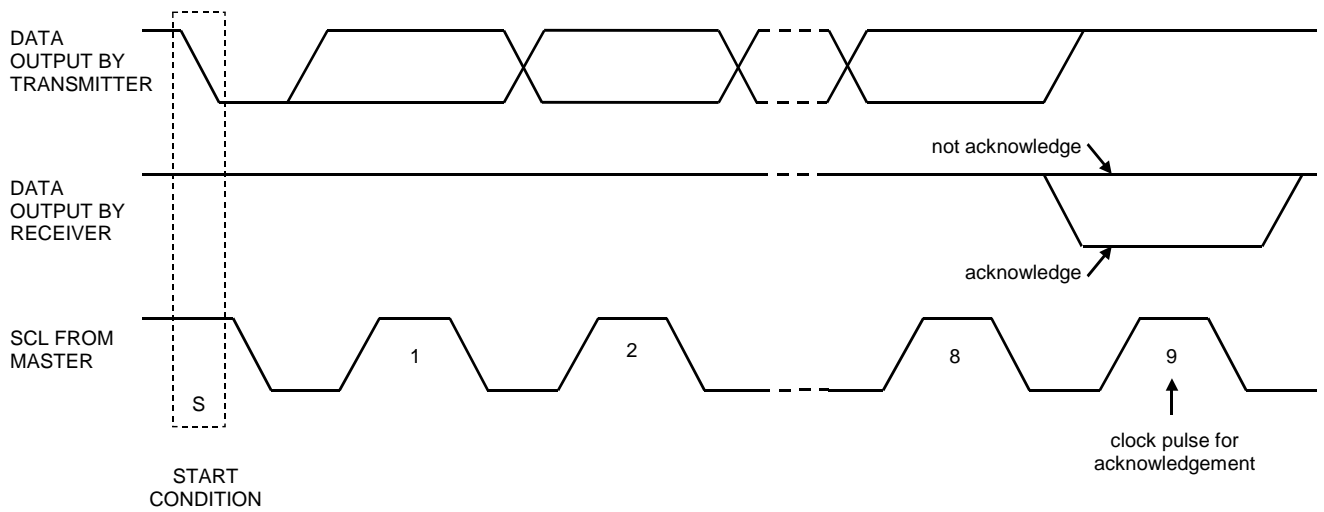


Figure 48. Acknowledge (I<sup>2</sup>C Bus)

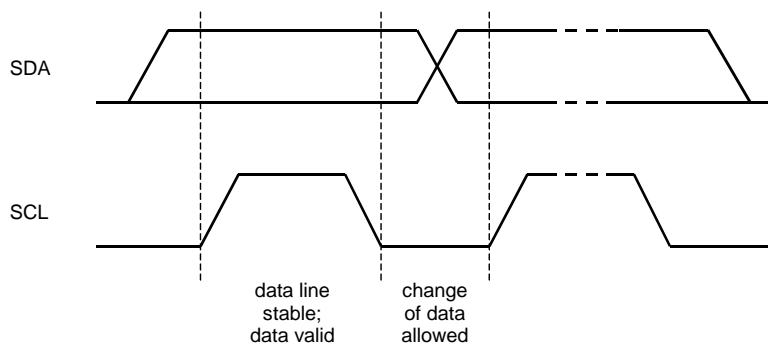


Figure 49. Bit Transfer (I<sup>2</sup>C Bus)

## ■ Register Map

| Addr | Register Name                | D7      | D6      | D5      | D4      | D3      | D2      | D1     | D0     |
|------|------------------------------|---------|---------|---------|---------|---------|---------|--------|--------|
| 00H  | Power Management A           | 0       | MIXA    | 0       | 0       | PMMPA   | PMVCM   | PMADAR | PMADAL |
| 01H  | PLL Control A                | READ    | 0       | PLL3    | PLL2    | PLL1    | PLL0    | M/S    | PMPLL  |
| 02H  | Signal & Mic Gain Select A   | HPFADA  | MGAINA2 | MGAINA1 | MGAINA0 | 0       | 0       | MDIFA2 | MDIFA1 |
| 03H  | Mic Gain Adjust A0           | DIF1    | DIF0    | 0       | 0       | MGAL3   | MGAL2   | MGAL1  | MGAL0  |
| 04H  | Mic Gain Adjust A1           | TDM1    | TDM0    | BCKO1   | BCKO0   | MGAR3   | MGAR2   | MGAR1  | MGAR0  |
| 05H  | fs Select & Filter Control A | HPFA1   | HPFA0   | LPFA    | HPF2A   | FS3     | FS2     | FS1    | FS0    |
| 06H  | Clock Output Select A        | ADRSTA1 | ADRSTA0 | CM1     | CM0     | 0       | MCKO    | PS1    | PS0    |
| 07H  | Lch Input Volume Control A   | IVAL7   | IVAL6   | IVAL5   | IVAL4   | IVAL3   | IVAL2   | IVAL1  | IVAL0  |
| 08H  | Rch Input Volume Control A   | IVAR7   | IVAR6   | IVAR5   | IVAR4   | IVAR3   | IVAR2   | IVAR1  | IVAR0  |
| 09H  | Timer Select A               | IVOLAC  | 0       | RFSTA1  | RFSTA0  | FRATT   | IVTM    | WTM1   | WTM0   |
| 0AH  | ALC Mode Control A0          | ALCA    | ALC4    | ALCEQN  | RGAINA2 | RGAINA1 | RGAINA0 | LMTHA1 | LMTHA0 |
| 0BH  | ALC Mode Control A1          | REFA7   | REFA6   | REFA5   | REFA4   | REFA3   | REFA2   | REFA1  | REFA0  |
| 0CH  | L1 Ch Output Delay Control   | DLY1L   | 0       | DLY1L5  | DLY1L4  | DLY1L3  | DLY1L2  | DLY1L1 | DLY1L0 |
| 0DH  | R1 Ch Output Delay Control   | DLY1R   | 0       | DLY1R5  | DLY1R4  | DLY1R3  | DLY1R2  | DLY1R1 | DLY1R0 |
| 0EH  | Reserved                     | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      |
| 0FH  | Reserved                     | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      |

| Addr | Register Name              | D7      | D6      | D5      | D4      | D3      | D2      | D1     | D0     |
|------|----------------------------|---------|---------|---------|---------|---------|---------|--------|--------|
| 10H  | Power Management B         | 0       | MIXB    | 0       | 0       | PMMPB   | 0       | PMADBR | PMADBL |
| 11H  | Reserved                   | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      |
| 12H  | Signal & Mic Gain Select B | HPFADB  | MGAINB2 | MGAINB1 | MGAINB0 | 0       | 0       | MDIFB2 | MDIFB1 |
| 13H  | Mic Gain Adjust B0         | 0       | 0       | 0       | 0       | MGBL3   | MGBL2   | MGBL1  | MGBL0  |
| 14H  | Mic Gain Adjust B1         | 0       | 0       | 0       | 0       | MGBR3   | MGBR2   | MGBR1  | MGBR0  |
| 15H  | Filter Control B           | HPFB1   | HPFB0   | LPFB    | HPF2B   | 0       | 0       | 0      | 0      |
| 16H  | Clock Output Select B      | ADRSTB1 | ADRSTB0 | 0       | 0       | 0       | 0       | 0      | 0      |
| 17H  | Lch Input Volume Control B | IVBL7   | IVBL6   | IVBL5   | IVBL4   | IVBL3   | IVBL2   | IVBL1  | IVBL0  |
| 18H  | Rch Input Volume Control B | IVBR7   | IVBR6   | IVBR5   | IVBR4   | IVBR3   | IVBR2   | IVBR1  | IVBR0  |
| 19H  | Timer Select B             | IVOLBC  | 0       | RFSTB1  | RFSTB0  | 0       | 0       | 0      | 0      |
| 1AH  | ALC Mode Control B0        | ALCB    | 0       | 0       | RGAINB2 | RGAINB1 | RGAINB0 | LMTHB1 | LMTHB0 |
| 1BH  | ALC Mode Control B1        | REFB7   | REFB6   | REFB5   | REFB4   | REFB3   | REFB2   | REFB1  | REFB0  |
| 1CH  | L2 Ch Output Delay Control | DLY2L   | 0       | DLY2L5  | DLY2L4  | DLY2L3  | DLY2L2  | DLY2L1 | DLY2L0 |
| 1DH  | R2 Ch Output Delay Control | DLY2R   | 0       | DLY2R5  | DLY2R4  | DLY2R3  | DLY2R2  | DLY2R1 | DLY2R0 |
| 1EH  | Reserved                   | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      |
| 1FH  | Reserved                   | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      |

| Addr         | Register Name        | D7    | D6    | D5     | D4     | D3     | D2     | D1    | D0    |
|--------------|----------------------|-------|-------|--------|--------|--------|--------|-------|-------|
| 20H          | HPFA2 Co-efficient 0 | FA1A7 | FA1A6 | FA1A5  | FA1A4  | FA1A3  | FA1A2  | FA1A1 | FA1A0 |
| 21H          | HPFA2 Co-efficient 1 | 0     | 0     | FA1A13 | FA1A12 | FA1A11 | FA1A10 | FA1A9 | FA1A8 |
| 22H          | HPFA2 Co-efficient 2 | FA1B7 | FA1B6 | FA1B5  | FA1B4  | FA1B3  | FA1B2  | FA1B1 | FA1B0 |
| 23H          | HPFA2 Co-efficient 3 | 0     | 0     | FA1B13 | FA1B12 | FA1B11 | FA1B10 | FA1B9 | FA1B8 |
| 24H          | LPFA Co-efficient 0  | FA2A7 | FA2A6 | FA2A5  | FA2A4  | FA2A3  | FA2A2  | FA2A1 | FA2A0 |
| 25H          | LPFA Co-efficient 1  | 0     | 0     | FA2A13 | FA12   | FA2A11 | FA2A10 | FA2A9 | FA2A8 |
| 26H          | LPFA Co-efficient 2  | FA2B7 | FA2B6 | FA2B5  | FA2B4  | FA2B3  | FA2B2  | FA2B1 | FA2B0 |
| 27H          | LPFA Co-efficient 3  | 0     | 0     | FA2B13 | FB12   | FA2B11 | FA2B10 | FA2B9 | FA2B8 |
| 28H<br>~ 2FH | Reserved             | 0     | 0     | 0      | 0      | 0      | 0      | 0     | 0     |

| Addr | Register Name        | D7    | D6    | D5     | D4     | D3     | D2     | D1    | D0    |
|------|----------------------|-------|-------|--------|--------|--------|--------|-------|-------|
| 30H  | HPFB2 Co-efficient 0 | FB1A7 | FB1A6 | FB1A5  | FB1A4  | FB1A3  | FB1A2  | FB1A1 | FB1A0 |
| 31H  | HPFB2 Co-efficient 1 | 0     | 0     | FB1A13 | FB1A12 | FB1A11 | FB1A10 | FB1A9 | FB1A8 |
| 32H  | HPFB2 Co-efficient 2 | FB1B7 | FB1B6 | FB1B5  | FB1B4  | FB1B3  | FB1B2  | FB1B1 | FB1B0 |
| 33H  | HPFB2 Co-efficient 3 | 0     | 0     | FB1B13 | FB1B12 | FB1B11 | FB1B10 | FB1B9 | FB1B8 |
| 34H  | LPFB Co-efficient 0  | FB2A7 | FB2A6 | FB2A5  | FB2A4  | FB2A3  | FB2A2  | FB2A1 | FB2A0 |
| 35H  | LPFB Co-efficient 1  | 0     | 0     | FB2A13 | FA12   | FB2A11 | FB2A10 | FB2A9 | FB2A8 |
| 36H  | LPFB Co-efficient 2  | FB2B7 | FB2B6 | FB2B5  | FB2B4  | FB2B3  | FB2B2  | FB2B1 | FB2B0 |
| 37H  | LPFB Co-efficient 3  | 0     | 0     | FB2B13 | FB12   | FB2B11 | FB2B10 | FB2B9 | FB2B8 |

Note 35. PDN pin = "L" resets the registers to their default values.

Note 36. The bits defined as 0 must contain a "0" value.

## ■ Register Definitions

| Addr | Register Name      | D7 | D6   | D5 | D4 | D3    | D2    | D1     | D0     |
|------|--------------------|----|------|----|----|-------|-------|--------|--------|
| 00H  | Power Management A | 0  | MIXA | 0  | 0  | PMMPA | PMVCM | PMADAR | PMADAL |
|      | R/W                | R  | R/W  | R  | R  | R/W   | R/W   | R/W    | R/W    |
|      | Default            | 0  | 0    | 0  | 0  | 0     | 0     | 0      | 0      |

PMADAL: MIC-Amp A Lch and ADCA Lch Power Management

0: Power down (default)

1: Power up

PMADAR: MIC-Amp A Rch and ADCA Rch Power Management

0: Power down (default)

1: Power up

When the PMADAL or PMADAR bit is changed from “0” to “1”, the initialization cycle (1059/fs=24ms @44.1kHz, ADRSTA1-0 bits = “00”) starts. After initializing, digital data of the ADC is output.

PMVCM: VCOM Power Management

0: Power down (default)

1: Power up

PMVCM bit must be “1” when one of blocks is powered-up. PMVCM bit can only be “0” when all power management bits (PMADAL, PMADAR, PMADBL, PMADBR, PMMPA, PMMPB, PMPL and MCKO) are “0”.

PMMPA: MPWRA pin Power Management

0: Power down: Hi-Z (default)

1: Power up

MIXA: ADCA Output Data Select ([Table 27](#))

0: Normal operation (default)

1: (L+R)/2

Each block can be powered-down respectively by writing “0” in each bit of this address. When the PDN pin is “L”, all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When PMVCM, PMADAL, PMADAR, PMADBL, PMADBR, PMMPA, PMMPB, PMPLL and MCKO bits are “0”, all blocks are powered-down. The register values remain unchanged.

When the all ADC is powered-down, external clocks may not be present. When one of the ADC is powered -up, external clocks must always be present.

| Addr | Register Name | D7   | D6 | D5   | D4   | D3   | D2   | D1  | D0    |
|------|---------------|------|----|------|------|------|------|-----|-------|
| 01H  | PLL Control A | READ | 0  | PLL3 | PLL2 | PLL1 | PLL0 | M/S | PMPLL |
|      | R/W           | R/W  | R  | R/W  | R/W  | R/W  | R/W  | R/W | R/W   |
|      | Default       | 0    | 0  | 0    | 1    | 1    | 0    | 0   | 0     |

PMPLL: PLL Power Management

0: EXT Mode and Power Down (default)

1: PLL Mode and Power up

M/S: Master / Slave Mode Select

0: Slave Mode (default)

1: Master Mode

PLL3-0: PLL Reference Clock Select ([Table 4](#))

Default: “0110” (MCKI pin=12MHz)

READ: Read Function Enable

0: Disable (default)

1: Enable

| Addr | Register Name              | D7     | D6      | D5      | D4      | D3 | D2 | D1     | D0     |
|------|----------------------------|--------|---------|---------|---------|----|----|--------|--------|
| 02H  | Mic Gain & Signal Select A | HPFADA | MGAINA2 | MGAINA1 | MGAINA0 | 0  | 0  | MDIFA2 | MDIFA1 |
|      | R/W                        | R/W    | R/W     | R/W     | R/W     | R  | R  | R/W    | R/W    |
|      | Default                    | 0      | 1       | 1       | 0       | 0  | 0  | 0      | 0      |

MDIFA1: ADCA Lch Input Type Select

0: Single-ended Input (LIN1 pin: Default)

1: Full-differential Input (LINA+/LINA– pins)

MDIFA2: ADCA Rch Input Type Select

0: Single-ended Input (RIN1 pin: Default)

1: Full-differential Input (RINA+/RINA– pins)

MGAINA2-0: MIC-Amp A Gain Control ([Table 22](#))

Default: “110” (+30dB)

HPFADA: HPF1A Enable

0: Disable (default)

1: Enable

While using ADCA, HPFADA bit should be set to “1”.

| Addr | Register Name      | D7   | D6   | D5 | D4 | D3    | D2    | D1    | D0    |
|------|--------------------|------|------|----|----|-------|-------|-------|-------|
| 03H  | Mic Gain Adjust A0 | DIF1 | DIF0 | 0  | 0  | MGAL3 | MGAL2 | MGAL1 | MGAL0 |
|      | R/W                | R/W  | R/W  | R  | R  | R/W   | R/W   | R/W   | R/W   |
|      | Default            | 1    | 1    | 0  | 0  | 0     | 1     | 0     | 0     |

MGAL3-0: ADCA Lch MIC Gain Adjust ([Table 26](#))

Default: “4H” (0dB)

DIF1-0: Audio Interface Format ([Table 17](#), [Table 18](#), [Table 19](#))

Default: “11” (24bit/16bit I<sup>2</sup>S compatible)

| Addr | Register Name      | D7   | D6   | D5    | D4    | D3    | D2    | D1    | D0    |
|------|--------------------|------|------|-------|-------|-------|-------|-------|-------|
| 04H  | Mic Gain Adjust A1 | TDM1 | TDM0 | BCKO1 | BCKO0 | MGAR3 | MGAR2 | MGAR1 | MGAR0 |
|      | R/W                | R/W  | R/W  | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
|      | Default            | 0    | 0    | 0     | 0     | 0     | 1     | 0     | 0     |

MGAR3-0: ADCA Rch Gain Adjust (Table 26)

Default: "4H" (0dB)

BCKO1-0: BCLK Output Frequency Select at Master Mode (Table 10, Table 15)

Default: "00" (32fs)

TDM1-0: TDM Format Select (Table 17, Table 18, Table 19)

Default: "00" (Stereo Mode)

| Addr | Register Name                | D7     | D6     | D5   | D4    | D3  | D2  | D1  | D0  |
|------|------------------------------|--------|--------|------|-------|-----|-----|-----|-----|
| 05H  | Filter Control A & fs Select | HPF1A1 | HPF1A0 | LPFA | HPF2A | FS3 | FS2 | FS1 | FS0 |
|      | R/W                          | R/W    | R/W    | R/W  | R/W   | R/W | R/W | R/W | R/W |
|      | Default                      | 0      | 0      | 0    | 0     | 1   | 1   | 1   | 1   |

FS3-0: Sampling Frequency (Table 5, Table 12, Table 14)

Default: "1111" (44.1kHz)

HPF2A: HPF2A Coefficient Setting Enable

0: Disable (default)

1: Enable

When HPF2A bit is "1", the settings of FA1A13-0 and FA1B13-0 bits are enabled. When HPF2A bit is "0", the audio data passes the HPF2A block by is 0dB gain.

LPFA: LPFA Coefficient Setting Enable

0: Disable (default)

1: Enable

When LPFA bit is "1", the settings of FA2A13-0 and FA2B13-0 bits are enabled. When LPFA bit is "0", the audio data passes the LPFA block by is 0dB gain.

HPF1A1-0: Cut-off Frequency Setting of HPF1A (Table 25)

Default: "00" ( $f_c=3.4\text{Hz}@f_s=44.1\text{kHz}$ )

| Addr | Register Name         | D7      | D6      | D5  | D4  | D3 | D2   | D1  | D0  |
|------|-----------------------|---------|---------|-----|-----|----|------|-----|-----|
| 06H  | Clock Output Select A | ADRSTA1 | ADRSTA0 | CM1 | CM0 | 0  | MCKO | PS1 | PS0 |
|      | R/W                   | R/W     | R/W     | R/W | R/W | R  | R/W  | R/W | R/W |
|      | Default               | 0       | 0       | 0   | 0   | 0  | 0    | 0   | 0   |

PS1-0: MCKO Output Frequency Select (Table 9)

Default: "00" (256fs)

MCKO: Master Clock Output Enable

0: Disable: MCKO pin = "L" (default)

1: Enable: Output frequency is selected by PS1-0 bits.

CM1-0: MCKI Input Frequency Select at EXT Mode (Table 9)

Default: "00" (256fs; 24kHz ~ 48kHz)

ADRSTA1-0: ADCA Initialization Cycle (Table 16)

Default: "00" (1059/fs)

| Addr | Register Name              | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|------|----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 07H  | Lch Input Volume Control A | IVAL7 | IVAL6 | IVAL5 | IVAL4 | IVAL3 | IVAL2 | IVAL1 | IVAL0 |
| 08H  | Rch Input Volume Control A | IVAR7 | IVAR6 | IVAR5 | IVAR4 | IVAR3 | IVAR2 | IVAR1 | IVAR0 |
|      | R/W                        | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
|      | Default                    | 1     | 0     | 0     | 1     | 0     | 0     | 0     | 1     |

IVAL7-0, IVAR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 39)  
Default: "91H" (0dB)

| Addr | Register Name  | D7     | D6 | D5     | D4     | D3    | D2   | D1   | D0   |
|------|----------------|--------|----|--------|--------|-------|------|------|------|
| 09H  | Timer Select A | IVOLAC | 0  | RFSTA1 | RFSTA0 | FRATT | IVTM | WTM1 | WTM0 |
|      | R/W            | R/W    | R  | R/W    | R/W    | R/W   | R/W  | R/W  | R/W  |
|      | Default        | 1      | 0  | 0      | 0      | 0     | 1    | 0    | 0    |

WTM1-0: ALC Recovery Waiting Period (Table 33)  
Default: "00" (128/fs)

IVTM: Input Digital Volume Soft Transition Time Setting (Table 40)  
0: 236/fs  
1: 944/fs (default)

FRATT: ATT Amount for Reference Volume of Fast Recovery (Table 37)  
0: -0.00106dB (4/fs) (default)  
1: -0.00106dB (16/fs)

RFSTA1-0: ALCA First recovery Speed (Table 36)  
Default: "00" (0.0032dB)

IVOLAC: Input Digital Volume A Control Mode Select  
0: Independent  
1: Dependent (default)

When IVOLAC bit = "1", IVAL7-0 bits control both Lch and Rch volume levels, while register values of IVAL7-0 bits are not written to IVAR7-0 bits. When IVOLAC bit = "0", IVAL7-0 bits control Lch level and IVAR7-0 bits control Rch level, respectively.

| Addr | Register Name       | D7   | D6   | D5     | D4      | D3      | D2      | D1     | D0     |
|------|---------------------|------|------|--------|---------|---------|---------|--------|--------|
| 0AH  | ALC Mode Control A0 | ALCA | ALC4 | ALCEQN | RGAINA2 | RGAINA1 | RGAINA0 | LMTHA1 | LMTHA0 |
|      | R/W                 | R/W  | R/W  | R/W    | R/W     | R/W     | R/W     | R/W    | R/W    |
|      | Default             | 0    | 0    | 0      | 0       | 0       | 0       | 0      | 0      |

LMTHA1-0: ALCA Limiter Detection Level / Recovery Counter Reset Level (Table 31)

Default: "00"

RGAINA2-0: ALCA Recovery Gain Step (Table 34)

Default: "000" (0.00424dB)

ALCEQN: ALC EQ Disable

0: ALC EQ Enable (default)

1: ALC EQ Disable

ALC4: ALC 4ch Link Enable (Table 30)

0: ALC 4ch Link Disable (default)

1: ALC 4ch Link Enable

ALCA: ALCA Enable (Table 30)

0: ALCA Disable (default)

1: ALCA Enable

| Addr | Register Name       | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0BH  | ALC Mode Control A1 | REFA7 | REFA6 | REFA5 | REFA4 | REFA3 | REFA2 | REFA1 | REFA0 |
|      | R/W                 | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
|      | Default             | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 1     |

REFA7-0: Reference Value at ALCA Recovery Operation; 0.375dB step, 242 Level (Table 35)

Default: "E1H" (+30.0dB)

| Addr | Register Name              | D7    | D6 | D5     | D4     | D3     | D2     | D1     | D0     |
|------|----------------------------|-------|----|--------|--------|--------|--------|--------|--------|
| 0CH  | L1 Ch Output Delay Control | DLY1L | 0  | DLY1L5 | DLY1L4 | DLY1L3 | DLY1L2 | DLY1L1 | DLY1L0 |
|      | R/W                        | R/W   | R  | R/W    | R/W    | R/W    | R/W    | R/W    | R/W    |
|      | Default                    | 0     | 0  | 0      | 0      | 0      | 0      | 0      | 0      |

DLY1L5-0: Programmable Output Data Delay (Table 24)

"00H": 1/64fs (default)

DLY1L: Programmable Output Data Delay Enable for L1 Channel

0: Disable (default)

1: Enable

When DLY1L bit is "1", the settings of DLY1L5-0 bits are enabled. When DLY1L bit is "0", the audio data of the L1 channel block is not delayed.

| Addr | Register Name              | D7    | D6 | D5     | D4     | D3     | D2     | D1     | D0     |
|------|----------------------------|-------|----|--------|--------|--------|--------|--------|--------|
| 0DH  | R1 Ch Output Delay Control | DLY1R | 0  | DLY1R5 | DLY1R4 | DLY1R3 | DLY1R2 | DLY1R1 | DLY1R0 |
|      | R/W                        | R/W   | R  | R/W    | R/W    | R/W    | R/W    | R/W    | R/W    |
|      | Default                    | 0     | 0  | 0      | 0      | 0      | 0      | 0      | 0      |

DLY1R5-0: Programmable Output Data Delay ([Table 24](#))

“00H”: 1/64fs (default)

DLY1R: Programmable Output Data Delay Enable for R1 Channel

0: Disable (default)

1: Enable

When DLY1R bit is “1”, the settings of DLY1R5-0 bits are enabled. When DLY1R bit is “0”, the audio data of the R1 channel block is not delayed.

| Addr | Register Name      | D7 | D6   | D5 | D4 | D3    | D2 | D1     | D0     |
|------|--------------------|----|------|----|----|-------|----|--------|--------|
| 10H  | Power Management B | 0  | MIXB | 0  | 0  | PMMPB | 0  | PMADBR | PMADBL |
|      | R/W                | R  | R/W  | R  | R  | R/W   | R  | R/W    | R/W    |
|      | Default            | 0  | 0    | 0  | 0  | 0     | 0  | 0      | 0      |

PMADBL: MIC-Amp B Lch and ADCB Lch Power Management

0: Power down (default)

1: Power up

PMADBR: MIC-Amp B Rch and ADCB Rch Power Management

0: Power down (default)

1: Power up

When the PMADBL or PMADBR bit is changed from “0” to “1”, the initialization cycle ( $1059/\text{fs}=24\text{ms}$  @44.1kHz, ADRSTB1-0 bits = “00”) starts. After initializing, digital data of the ADC is output.

PMMPB: MPWRB pin Power Management

0: Power down: Hi-Z (default)

1: Power up

MIXB: ADCB Output Data Select ([Table 27](#))

0: Normal operation (default)

1: (L+R)/2

Each block can be powered-down respectively by writing “0” in each bit of this address. When the PDN pin is “L”, all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When PMVCM, PMADAL, PMADAR, PMADBL, PMADBR, PMMPA, PMMPB, PMPLL and MCKO bits are “0”, all blocks are powered-down. The register values remain unchanged.

When the all ADC is powered-down, external clocks may not be present. When one of the ADC is powered-up, external clocks must always be present.

| Addr | Register Name              | D7     | D6      | D5      | D4      | D3 | D2 | D1     | D0     |
|------|----------------------------|--------|---------|---------|---------|----|----|--------|--------|
| 12H  | Mic Gain & Signal Select B | HPFADB | MGAINB2 | MGAINB1 | MGAINB0 | 0  | 0  | MDIFB2 | MDIFB1 |
|      | R/W                        | R/W    | R/W     | R/W     | R/W     | R  | R  | R/W    | R/W    |
|      | Default                    | 0      | 1       | 1       | 0       | 0  | 0  | 0      | 0      |

MDIFB1: ADCB Lch Input Type Select

0: Single-ended Input (LIN2 pin: Default)

1: Full-differential Input (LINB+/LINB- pins)

MDIFB2: ADCB Rch Input Type Select

0: Single-ended Input (RIN2 pin: Default)

1: Full-differential Input (RINB+/RINB- pins)

MGAINB2-0: MIC-Amp B Gain Control (Table 22)

Default: "110" (+30dB)

HPFADB: HPF1B Enable

0: Disable (default)

1: Enable

While using ADCB, HPFADB bit should be set to "1".

| Addr | Register Name      | D7 | D6 | D5 | D4 | D3    | D2    | D1    | D0    |
|------|--------------------|----|----|----|----|-------|-------|-------|-------|
| 13H  | Mic Gain Adjust B0 | 0  | 0  | 0  | 0  | MGBL3 | MGBL2 | MGBL1 | MGBL0 |
| 14H  | Mic Gain Adjust B1 | 0  | 0  | 0  | 0  | MGBR3 | MGBR2 | MGBR1 | MGBR0 |
|      | R/W                | R  | R  | R  | R  | R/W   | R/W   | R/W   | R/W   |
|      | Default            | 0  | 0  | 0  | 0  | 0     | 1     | 0     | 0     |

MGBL/R3-0: ADCB Lch/Rch MIC Gain Adjust (Table 26)

Default: "4H" (0dB)

| Addr | Register Name    | D7    | D6    | D5   | D4    | D3 | D2 | D1 | D0 |
|------|------------------|-------|-------|------|-------|----|----|----|----|
| 15H  | Filter Control B | HPFB1 | HPFB0 | LPFB | HPF2B | 0  | 0  | 0  | 0  |
|      | R/W              | R/W   | R/W   | R/W  | R/W   | R  | R  | R  | R  |
|      | Default          | 0     | 0     | 0    | 0     | 0  | 0  | 0  | 0  |

HPF2B: HPF2B Coefficient Setting Enable

0: Disable (default)

1: Enable

When HPF2BA bit is "1", the settings of FB1A13-0 and FB1B13-0 bits are enabled. When HPF2B bit is "0", the audio data passes the HPF2B block by is 0dB gain.

LPFB: LPFB Coefficient Setting Enable

0: Disable (default)

1: Enable

When LPFB bit is "1", the settings of FB2A13-0 and FB2B13-0 bits are enabled. When LPFB bit is "0", the audio data passes the LPFB block by is 0dB gain.

HPFB1-0: Cut-off Frequency Setting of HPF1B (Table 25)

Default: "00" ( $f_c=3.4\text{Hz}@f_s=44.1\text{kHz}$ )

| Addr | Register Name         | D7      | D6      | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|---------|---------|----|----|----|----|----|----|
| 16H  | Clock Output Select B | ADRSTB1 | ADRSTB0 | 0  | 0  | 0  | 0  | 0  | 0  |
|      | R/W                   | R/W     | R/W     | R  | R  | R  | R  | R  | R  |
|      | Default               | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  |

ADRSTB1-0: ADCB Initialization Cycle ([Table 16](#))

Default: "00" (1059/fs)

| Addr | Register Name              | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|------|----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 17H  | Lch Input Volume Control B | IVBL7 | IVBL6 | IVBL5 | IVBL4 | IVBL3 | IVBL2 | IVBL1 | IVBL0 |
| 18H  | Rch Input Volume Control B | IVBR7 | IVBR6 | IVBR5 | IVBR4 | IVBR3 | IVBR2 | IVBR1 | IVBR0 |
|      | R/W                        | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
|      | Default                    | 1     | 0     | 0     | 1     | 0     | 0     | 0     | 1     |

IVBL7-0, IVBR7-0: Input Digital Volume; 0.375dB step, 242 Level ([Table 39](#))

Default: "91H" (0dB)

| Addr | Register Name  | D7     | D6 | D5     | D4     | D3 | D2 | D1 | D0 |
|------|----------------|--------|----|--------|--------|----|----|----|----|
| 19H  | Timer Select B | IVOLBC | 0  | RFSTB1 | RFSTB0 | 0  | 0  | 0  | 0  |
|      | R/W            | R/W    | R  | R/W    | R/W    | R  | R  | R  | R  |
|      | Default        | 1      | 0  | 0      | 0      | 0  | 0  | 0  | 0  |

RFSTB1-0: ALCB First recovery Speed ([Table 36](#))

Default: "00" (0.0032dB)

IVOLBC: Input Digital Volume B Control Mode Select

0: Independent

1: Dependent (default)

When IVOLBC bit = "1", IVBL7-0 bits control both Lch and Rch volume levels, while register values of IVBL7-0 bits are not written to IVBR7-0 bits. When IVOLBC bit = "0", IVBL7-0 bits control Lch level and IVBR7-0 bits control Rch level, respectively.

| Addr | Register Name       | D7   | D6 | D5 | D4      | D3      | D2      | D1     | D0     |
|------|---------------------|------|----|----|---------|---------|---------|--------|--------|
| 1AH  | ALC Mode Control B0 | ALCB | 0  | 0  | RGAINB2 | RGAINB1 | RGAINB0 | LMTHB1 | LMTHB0 |
|      | R/W                 | R/W  | R  | R  | R/W     | R/W     | R/W     | R/W    | R/W    |
|      | Default             | 0    | 0  | 0  | 0       | 0       | 0       | 0      | 0      |

LMTHB1-0: ALCB Limiter Detection Level / Recovery Counter Reset Level ([Table 31](#))

Default: "00"

RGAINB2-0: ALCB Recovery Gain Step ([Table 34](#))

Default: "000" (0.00424dB)

ALCB: ALCB Enable ([Table 30](#))

0: ALCB Disable (default)

1: ALCB Enable

| Addr | Register Name       | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 1BH  | ALC Mode Control B1 | REFB7 | REFB6 | REFB5 | REFB4 | REFB3 | REFB2 | REFB1 | REFB0 |
|      | R/W                 | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
|      | Default             | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 1     |

REFB7-0: Reference Value at ALCB Recovery Operation; 0.375dB step, 242 Level (Table 35)

Default: "E1H" (+30.0dB)

| Addr | Register Name              | D7    | D6 | D5     | D4     | D3     | D2     | D1     | D0     |
|------|----------------------------|-------|----|--------|--------|--------|--------|--------|--------|
| 1CH  | L2 Ch Output Delay Control | DLY2L | 0  | DLY2L5 | DLY2L4 | DLY2L3 | DLY2L2 | DLY2L1 | DLY2L0 |
|      | R/W                        | R/W   | R  | R/W    | R/W    | R/W    | R/W    | R/W    | R/W    |
|      | Default                    | 0     | 0  | 0      | 0      | 0      | 0      | 0      | 0      |

DLY2L5-0: Programmable Output Data Delay (Table 24)

"00H": 1/64fs (default)

DLY2L: Programmable Output Data Delay Enable for L2 Channel

0: Disable (default)

1: Enable

When DLY2L bit is "1", the settings of DLY2L5-0 bits are enabled. When DLY2L bit is "0", the audio data of the L2 channel block is not delayed.

| Addr | Register Name              | D7    | D6 | D5     | D4     | D3     | D2     | D1     | D0     |
|------|----------------------------|-------|----|--------|--------|--------|--------|--------|--------|
| 1DH  | R2 Ch Output Delay Control | DLY2R | 0  | DLY2R5 | DLY2R4 | DLY2R3 | DLY2R2 | DLY2R1 | DLY2R0 |
|      | R/W                        | R/W   | R  | R/W    | R/W    | R/W    | R/W    | R/W    | R/W    |
|      | Default                    | 0     | 0  | 0      | 0      | 0      | 0      | 0      | 0      |

DLY2R5-0: Programmable Output Data Delay (Table 24)

"00H": 1/64fs (default)

DLY2R: Programmable Output Data Delay Enable for R2 Channel

0: Disable (default)

1: Enable

When DLY2R bit is "1", the settings of DLY2R5-0 bits are enabled. When DLY2R bit is "0", the audio data of the R2 channel block is not delayed.

| Addr    | Register Name        | D7   | D6    | D5     | D4     | D3     | D2     | D1    | D0    |
|---------|----------------------|--|-------|--------|--------|--------|--------|-------|-------|
| 20H     | HPFA2 Co-efficient 0 | FA1A7  | FA1A6 | FA1A5  | FA1A4  | FA1A3  | FA1A2  | FA1A1 | FA1A0 |
| 21H     | HPFA2 Co-efficient 1 | 0  | 0     | FA1A13 | FA1A12 | FA1A11 | FA1A10 | FA1A9 | FA1A8 |
| 22H     | HPFA2 Co-efficient 2 | FA1B7  | FA1B6 | FA1B5  | FA1B4  | FA1B3  | FA1B2  | FA1B1 | FA1B0 |
| 23H     | HPFA2 Co-efficient 3 | 0  | 0     | FA1B13 | FA1B12 | FA1B11 | FA1B10 | FA1B9 | FA1B8 |
| R/W     |                      | R/W  | R/W   | R/W    | R/W    | R/W    | R/W    | R/W   | R/W   |
| Default |                      | FA1A13-0 bits = "1FA9H", FA1B13-0 bits = "20ADH" |       |        |        |        |        |       |       |

FA1A13-0, FA1B13-B0: High Pass Filter (HPF2A) Coefficient (14bit x 2)

Default: FA1A13-0 bits = "1FA9H", FA1B13-0 bits = "20ADH" (fc=150Hz@fs=44.1kHz)

| Addr    | Register Name       | D7    | D6    | D5     | D4    | D3     | D2     | D1    | D0    |
|---------|---------------------|-------|-------|--------|-------|--------|--------|-------|-------|
| 24H     | LPFA Co-efficient 0 | FA2A7 | FA2A6 | FA2A5  | FA2A4 | FA2A3  | FA2A2  | FA2A1 | FA2A0 |
| 25H     | LPFA Co-efficient 1 | 0     | 0     | FA2A13 | FA12  | FA2A11 | FA2A10 | FA2A9 | FA2A8 |
| 26H     | LPFA Co-efficient 2 | FA2B7 | FA2B6 | FA2B5  | FA2B4 | FA2B3  | FA2B2  | FA2B1 | FA2B0 |
| 27H     | LPFA Co-efficient 3 | 0     | 0     | FA2B13 | FB12  | FA2B11 | FA2B10 | FA2B9 | FA2B8 |
| R/W     |                     | R/W   | R/W   | R/W    | R/W   | R/W    | R/W    | R/W   | R/W   |
| Default |                     | 0     | 0     | 0      | 0     | 0      | 0      | 0     | 0     |

FA2A13-0, FA2B13-B0: Low Pass Filter (LPFA) Coefficient (14bit x 2)

Default: "0000H"

| Addr    | Register Name        | D7   | D6    | D5     | D4     | D3     | D2     | D1    | D0    |
|---------|----------------------|--|-------|--------|--------|--------|--------|-------|-------|
| 30H     | HPFB2 Co-efficient 0 | FB1A7  | FB1A6 | FB1A5  | FB1A4  | FB1A3  | FB1A2  | FB1A1 | FB1A0 |
| 31H     | HPFB2 Co-efficient 1 | 0  | 0     | FB1A13 | FB1A12 | FB1A11 | FB1A10 | FB1A9 | FB1A8 |
| 32H     | HPFB2 Co-efficient 2 | FB1B7  | FB1B6 | FB1B5  | FB1B4  | FB1B3  | FB1B2  | FB1B1 | FB1B0 |
| 33H     | HPFB2 Co-efficient 3 | 0  | 0     | FB1B13 | FB1B12 | FB1B11 | FB1B10 | FB1B9 | FB1B8 |
| R/W     |                      | R/W  | R/W   | R/W    | R/W    | R/W    | R/W    | R/W   | R/W   |
| Default |                      | FB1A13-0 bits = "1FA9H", FB1B13-0 bits = "20ADH" |       |        |        |        |        |       |       |

FB1A13-0, FB1B13-B0: High Pass Filter (HPF2B) Coefficient (14bit x 2)

Default: FB1A13-0 bits = "1FA9H", FB1B13-0 bits = "20ADH" (fc=150Hz@fs=44.1kHz)

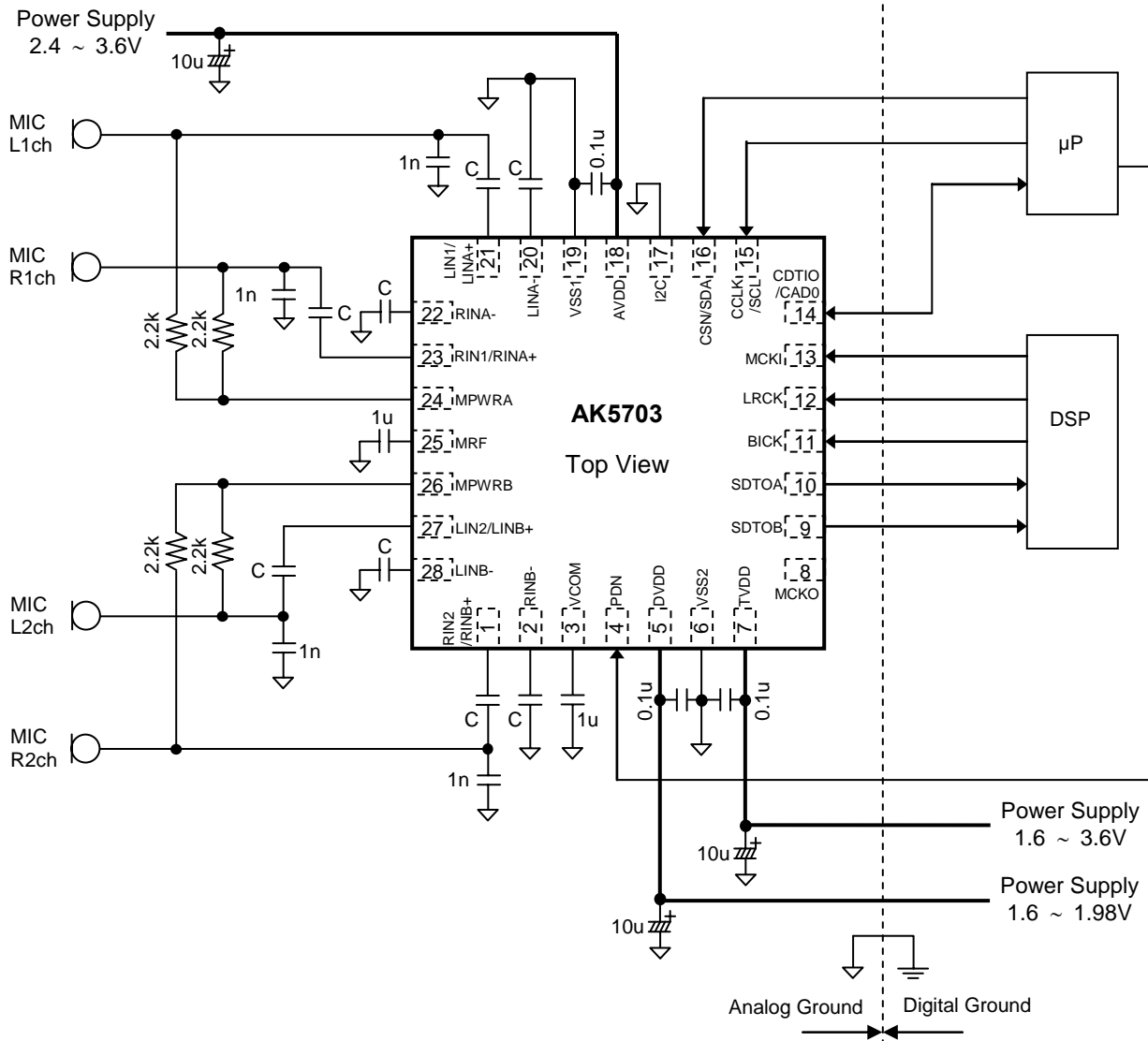
| Addr    | Register Name       | D7    | D6    | D5     | D4    | D3     | D2     | D1    | D0    |
|---------|---------------------|-------|-------|--------|-------|--------|--------|-------|-------|
| 34H     | LPFB Co-efficient 0 | FB2A7 | FB2A6 | FB2A5  | FB2A4 | FB2A3  | FB2A2  | FB2A1 | FB2A0 |
| 35H     | LPFB Co-efficient 1 | 0     | 0     | FB2A13 | FA12  | FB2A11 | FB2A10 | FB2A9 | FB2A8 |
| 36H     | LPFB Co-efficient 2 | FB2B7 | FB2B6 | FB2B5  | FB2B4 | FB2B3  | FB2B2  | FB2B1 | FB2B0 |
| 37H     | LPFB Co-efficient 3 | 0     | 0     | FB2B13 | FB12  | FB2B11 | FB2B10 | FB2B9 | FB2B8 |
| R/W     |                     | R/W   | R/W   | R/W    | R/W   | R/W    | R/W    | R/W   | R/W   |
| Default |                     | 0     | 0     | 0      | 0     | 0      | 0      | 0     | 0     |

FB2A13-0, FB2B13-B0: Low Pass Filter (LPFB) Coefficient (14bit x 2)

Default: "0000H"

**SYSTEM DESIGN**

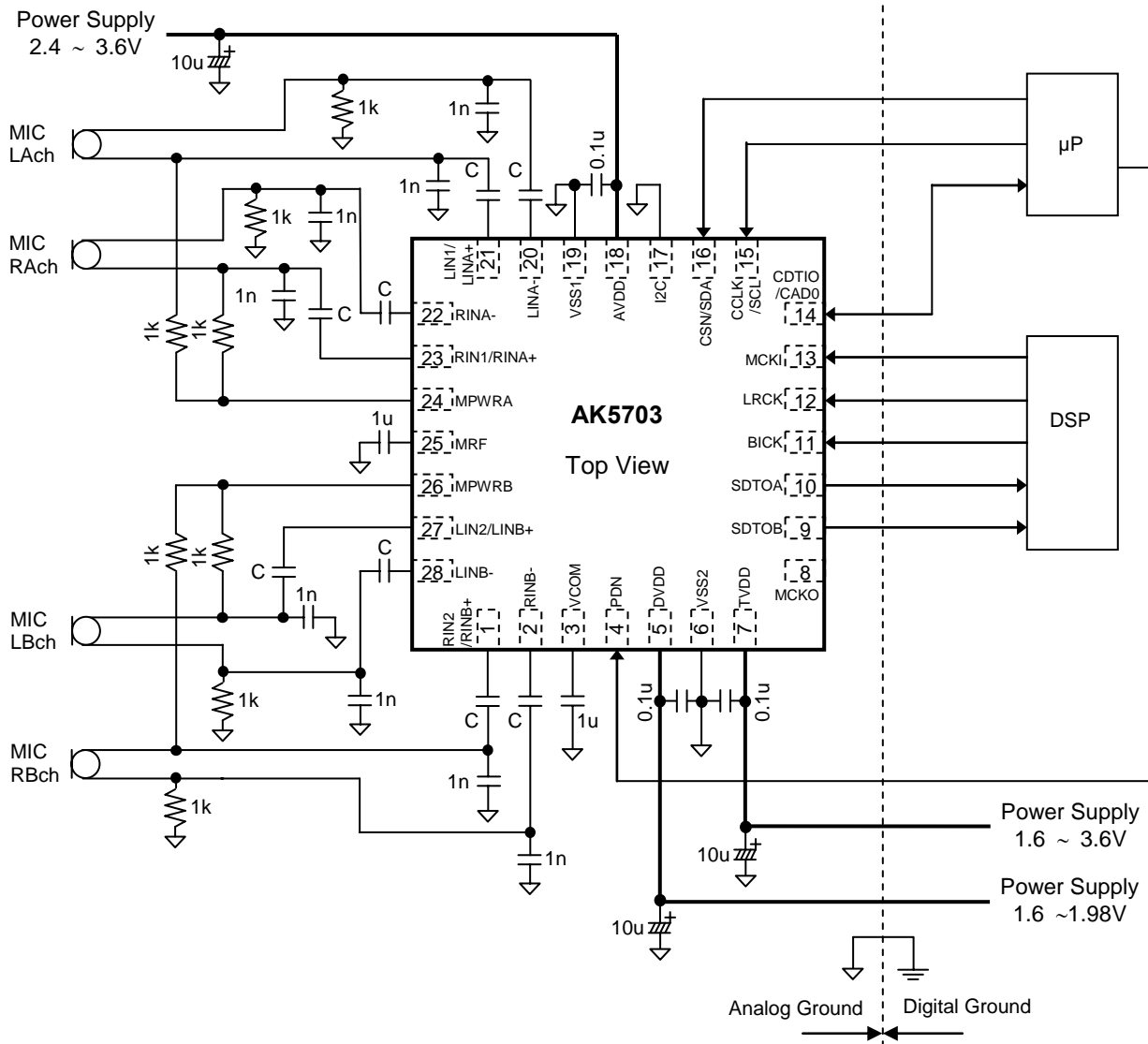
Figure 50 and Figure 51 show the system connection diagram. An evaluation board (AKD5703) is available for fast evaluation as well as suggestions for peripheral circuitry.



**Note:**

- VSS1 and VSS2 of the AK5703 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- Recommended AC coupling capacitors (C) of analog inputs are 0.1μF ~ 1μF. Negative input pins must be connected to VSS1 with same value capacitor in series.

Figure 50. System Connection Diagram (Single-ended Input)



Note:

- VSS1 and VSS2 of the AK5703 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- Recommended AC coupling capacitors (C) of analog inputs are 0.1μF ~ 1μF.

Figure 51. System Connection Diagram (Full-differential Input)

## 1. Grounding and Power Supply Decoupling

The AK5703 requires careful attention to power supply and grounding arrangements. AVDD is usually supplied from the system's analog supply, and DVDD and TVDD are supplied from the system's digital power supply. If AVDD, DVDD and TVDD are supplied separately, the power-up sequence is not critical. The PDN pin should be held "L" when power supplies are tuning on. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

### 1) Power-up

- The PDN pin should be held "L" when power supplies are turning on. The AK5703 can be reset by keeping the PDN pin "L" for 1 $\mu$ s or longer after all power supplies are applied and settled.

### 2) Power-down

- Each of power supplies can be powered OFF after the PDN pin is set to "L".

VSS1 and VSS2 of the AK5703 should be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

## 2. Voltage Reference

VCOM is a signal ground of this chip (typ. 0.5 x AVDD). A 1 $\mu$ F  $\pm$ 50% ceramic capacitor attached between the VCOM pin and VSS1 pin eliminates the effects of high frequency noise. It should be connected as close as possible to the VCOM pin. No load current is allowed to be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5703.

## 3. Analog Inputs

The analog inputs are single-ended or full-differential and input resistance is 100k $\Omega$  (typ). The input signal range scales with typ. 0.6 x AVDD Vpp (@ MGAINA/B2-0 bits = "000"), centered around the internal common voltage (typ. 0.5 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is  $f_c = 1/(2\pi RC)$ . The ADC output data format is 2's complement. The DC offset including the ADC's own DC offset is removed by the internal HPF ( $f_c=3.4\text{Hz}$ @ HPFA/B1-0 bits = "00",  $f_s=44.1\text{kHz}$ ). The AK5703 can accept input voltages from VSS1 to AVDD.

## CONTROL SEQUENCE

### ■ Clock Set up

When any circuits of the AK5703 are powered-up, the clocks must be supplied.

#### 1. PLL Master Mode

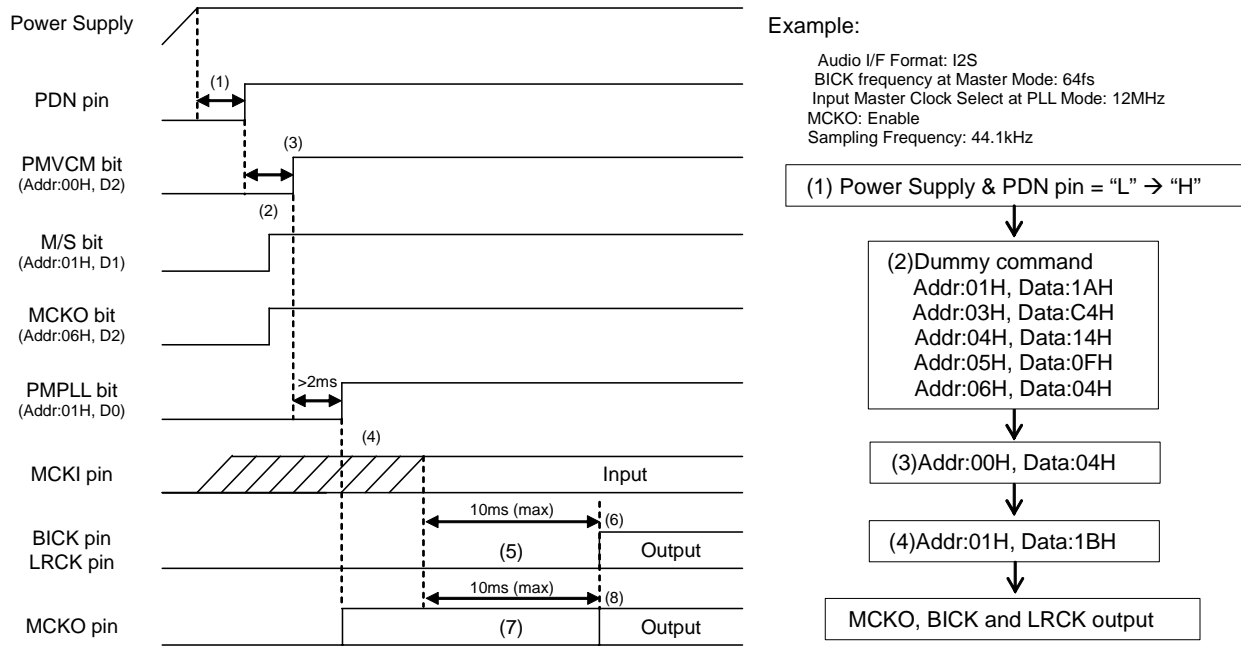


Figure 52. Clock Set Up Sequence (1)

#### < Example >

- (1) After Power Up, PDN pin "L" → "H".  
"L" time of 1μs or more is needed to reset the AK5703.
- (2) Dummy Command must be executed before control registers are set. M/S, PLL3-0, DIF1-0, FS3-0, PS1-0, BCKO and MCKO bits must be set during this period.  
In case of using MCKO output: MCKO bit = "1"  
In case of not using MCKO output: MCKO bit = "0"
- (3) Power Up VCOM: PMVCM bit = "0" → "1"  
VCOM must first be powered-up before operating other blocks. Rise-up time of the VCOM pin is 2ms (max) when the capacitance of an external capacitor is 1μF ±50%.
- (4) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source. PLL lock time is 10ms (max).
- (5) BICK pin and LRCK pin output "L" during this period.
- (6) The AK5703 starts outputting LRCK and BICK clocks after the PLL becomes stable. Then normal operation starts.
- (7) The invalid frequency is output from the MCKO pin during this period if MCKO bit = "1".
- (8) The normal clock is output from the MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (BICK pin)

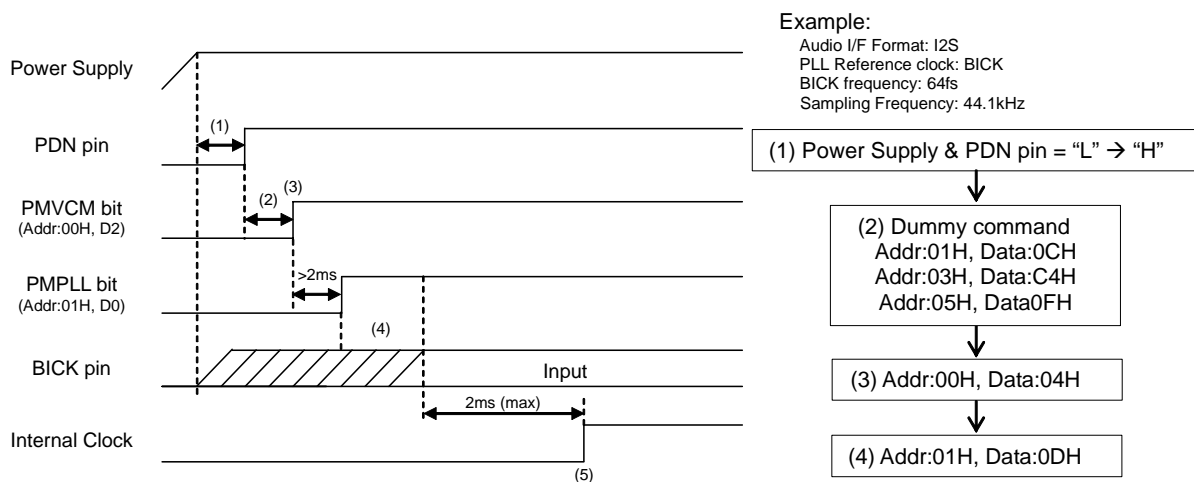
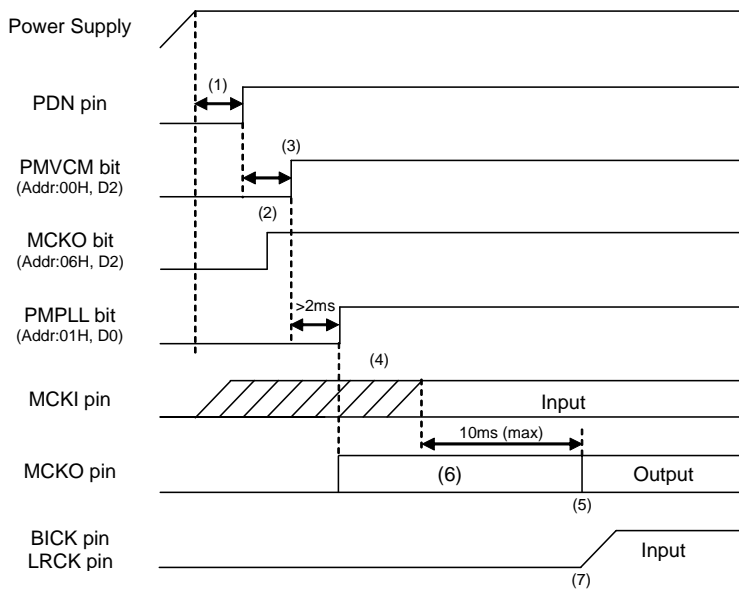


Figure 53. Clock Set Up Sequence (2)

<Example>

- (1) After Power Up: PDN pin "L" → "H"  
"L" time of 1μs or more is needed to reset the AK5703.
- (2) Dummy Command must be executed before control registers are set. PLL3-0, DIF1-0 and FS3-0 bits must be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"  
VCOM must first be powered-up before operating other blocks. Rise-up time of the VCOM pin is 2ms (max) when the capacitance of an external capacitor is 1μF ±50%.
- (4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied. PLL lock time is 2ms (max).
- (5) Normal operation starts after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)



Example:

Audio I/F Format: I2S  
 Input Master Clock Select at PLL Mode: 12MHz  
 MCKO: Enable  
 Sampling Frequency: 44.1kHz

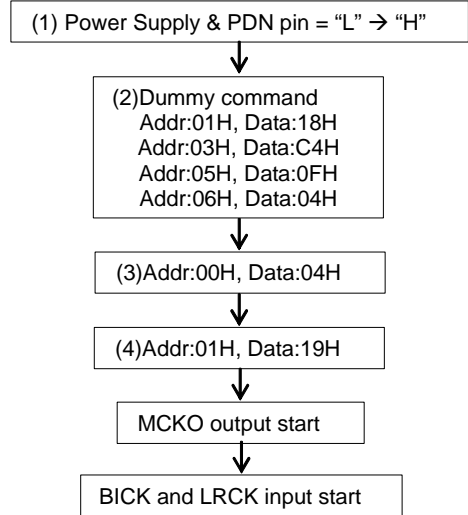


Figure 54. Clock Set Up Sequence (3)

<Example>

- (1) After Power up: PDN pin "L" → "H"  
 "L" time of 1μs or more is needed reset the AK5703.
- (2) After Dummy Command input, PLL3-0, DIF1-0, FS3-0, PS1-0 and MCKO bits must be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"  
 VCOM must first be powered-up before operating other blocks. Rise-up time of the VCOM pin is 2ms (max) when the capacitance of an external capacitor is 1μF ±50%.
- (4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied. PLL lock time is 10ms (max).
- (5) The normal clock is output from the MCKO pin after the PLL is locked.
- (6) The invalid frequency is output from the MCKO pin during this period.
- (7) BICK and LRCK clocks must be synchronized with MCKO clock.

4. EXT Slave Mode

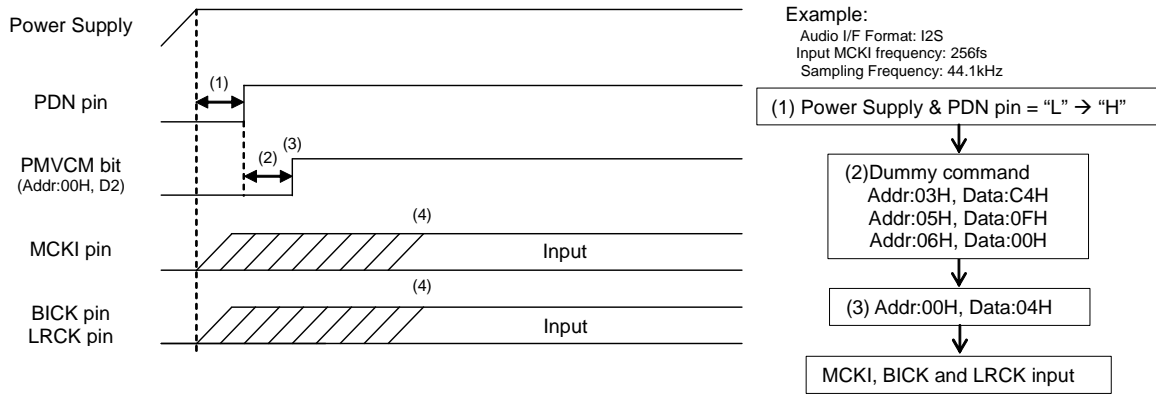


Figure 55. Clock Set Up Sequence (4)

<Example>

- (1) After power Up: PDN pin "L" → "H"  
 "L" time of 1μs or more is needed to reset the AK5703.
- (2) After Dummy Command input, DIF1-0, FS3-0 and CM1-0 bits must be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"  
 VCOM must first be powered-up before the other block operates. Rise-up time of the VCOM pin is 2ms (max) when the capacitance of an external capacitor is 1μF ±50%.
- (4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

5. EXT Master Mode

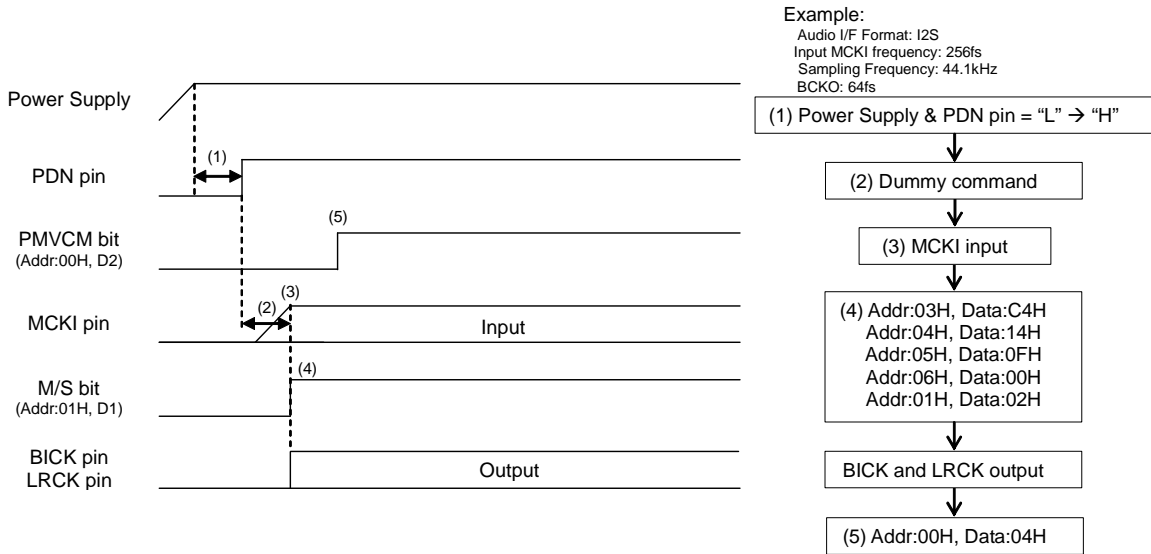


Figure 56. Clock Set Up Sequence (5)

<Example>

- (1) After power Up: PDN pin "L" → "H"  
 "L" time of 1μs or more is needed to reset the AK5703.
- (2) Dummy Command must be input during this period.
- (3) MCKI is supplied.
- (4) After DIF1-0, FS3-0, BCKO1-0 and CM1-0 bits are set. M/S bit should be set to "1".  
 Then LRCK and BICK are output.
- (5) Power Up VCOM: PMVCM bit = "0" → "1"  
 VCOM must first be powered-up before the other block operates. Rise-up time of the VCOM pin is 2ms (max) when the capacitance of an external capacitor is 1μF ±50%.

■ Microphone Input Recording (Stereo)

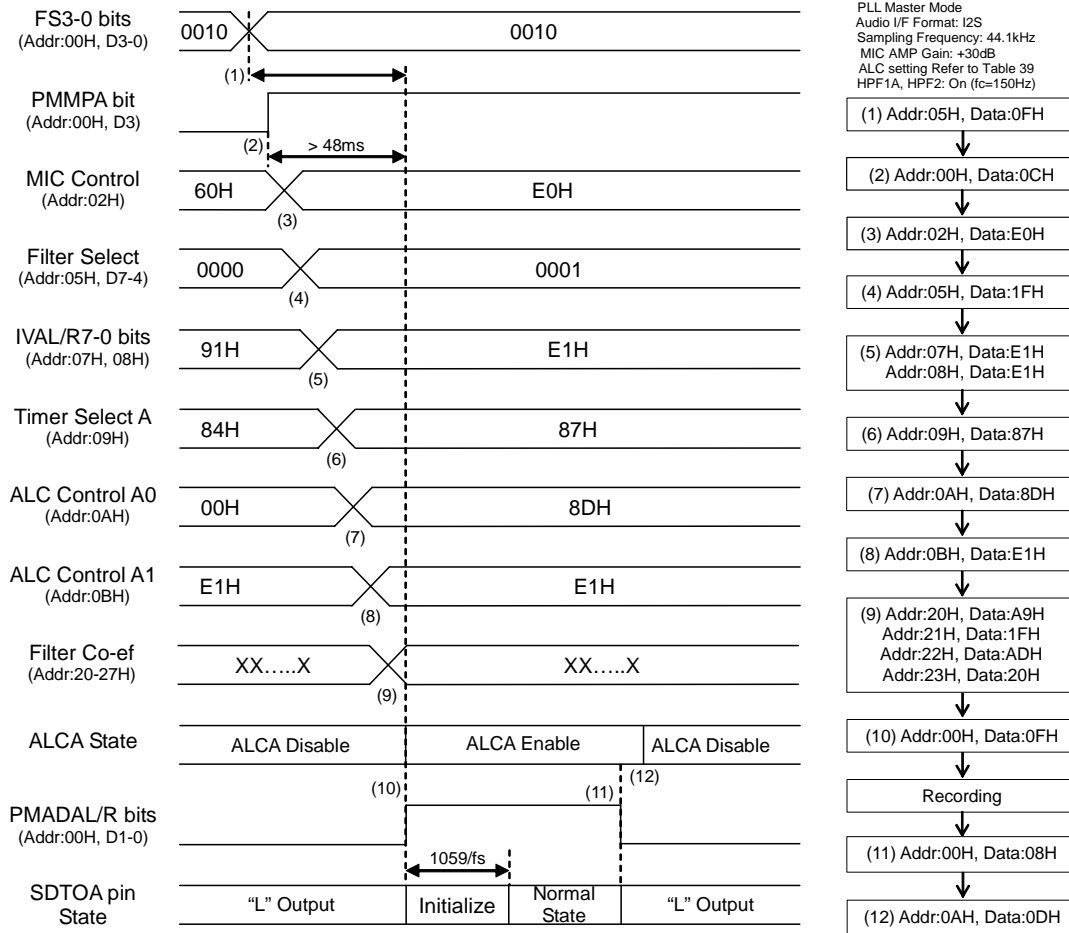


Figure 57. Microphone Input Recording Sequence (LIN1/RIN1 → ADCA → ALCA → Audio I/F → SDTOA)

<Example>

This sequence is an example of ALC setting at fs=44.1kHz. For changing the parameter of ALC, please refer to “Example of registers set-up sequence of ALC Operation”.

At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up the sampling frequency (FS3-0 bits). When the AK5703 is in PLL mode, ADC of (10) must be powered-up in consideration of PLL lock time after the sampling frequency is changed.
- (2) Power up Microphone Power Supply A: PMMPA bit = “1”  
Power-up time of Microphone Power is 48ms (max).
- (3) Set up HPF1A ON, Microphone Gain and Microphone Inputs (Addr = 02H)
- (4) Set up HPF2A and LPFA ON/OFF
- (5) Set up IVOL value of ALCA (Addr = 07H, 08H)
- (6) Set up the Timer of ALCA (Addr = 09H)
- (7) Set up the LMTHA1-0, RGAINA2-0, ALCEQN, ALCA bits (Addr = 0AH)
- (8) Set up IREF of ALCA (Addr = 0BH)
- (9) Set up Coefficient of HPF2A and LPFA (Addr: 20H ~ 27H)
- (10) Power up ADC: PMADAL = PMADAR bits = “0” → “1”  
The initialization cycle time of ADC is 1059/fs=24ms @ fs=44.1kHz, ADRSTA1-0 bits = “00”. The ADC outputs “0” data during the initialization cycle. After the ALC bit is set to “1”, the ALCA operation starts from IVOL value of (5).
- (11) Power down ADC: PMADAL = PMADAR bits = “1” → “0”
- (12) ALCA Disable: ALCA bit = “1” → “0”

■ Stop of Clock

1. PLL Master Mode

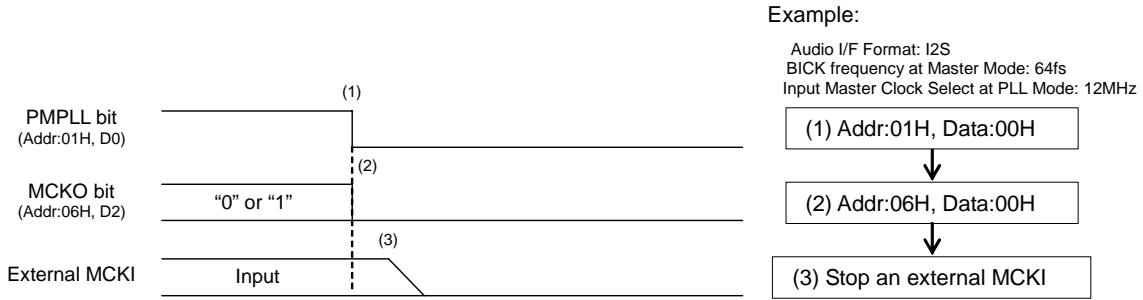


Figure 58. Clock Stopping Sequence (1)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
- (2) Stop MCKO output: MCKO bit = "1" → "0"
- (3) Stop the external master clock.

2. PLL Slave Mode (BICK pin)

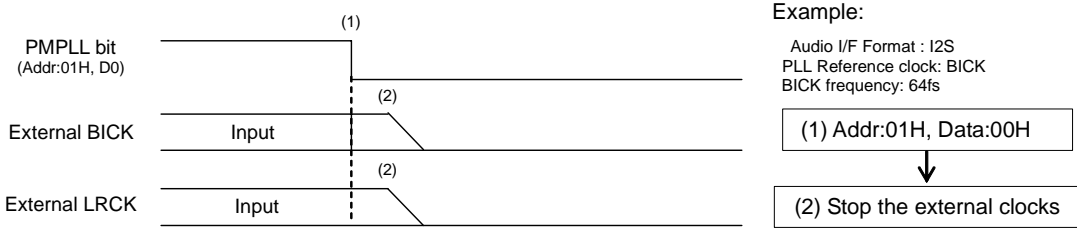


Figure 59. Clock Stopping Sequence (2)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
- (2) Stop the external BICK and LRCK clocks.

3. PLL Salve Mode (MCKI pin)

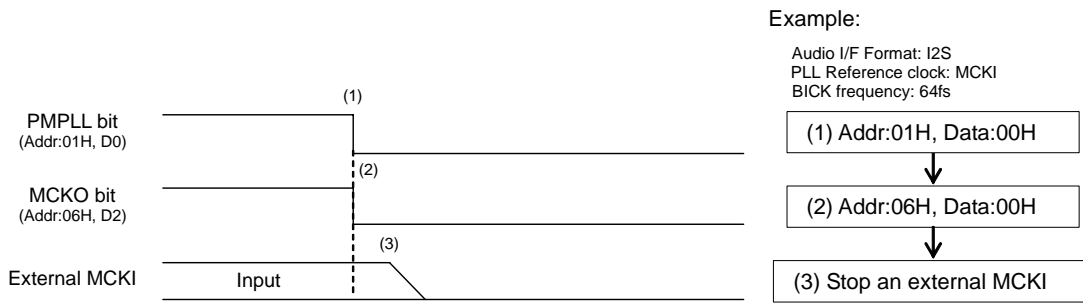


Figure 60. Clock Stopping Sequence (3)

<Example>

- (1) Power down PLL: PMPLL bit = “1” → “0”
- (2) Stop MCKO output: MCKO bit = “1” → “0”
- (3) Stop the external master clock.

4. EXT Slave Mode

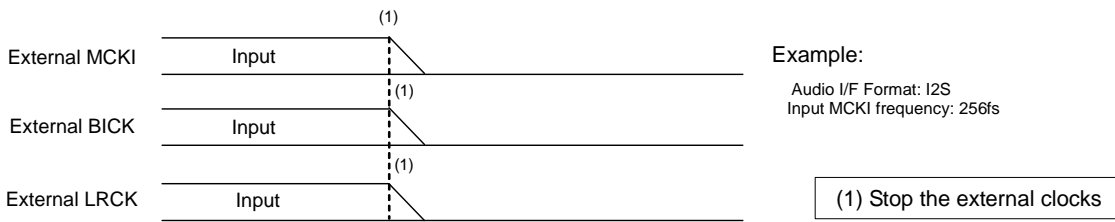


Figure 61. Clock Stopping Sequence (4)

<Example>

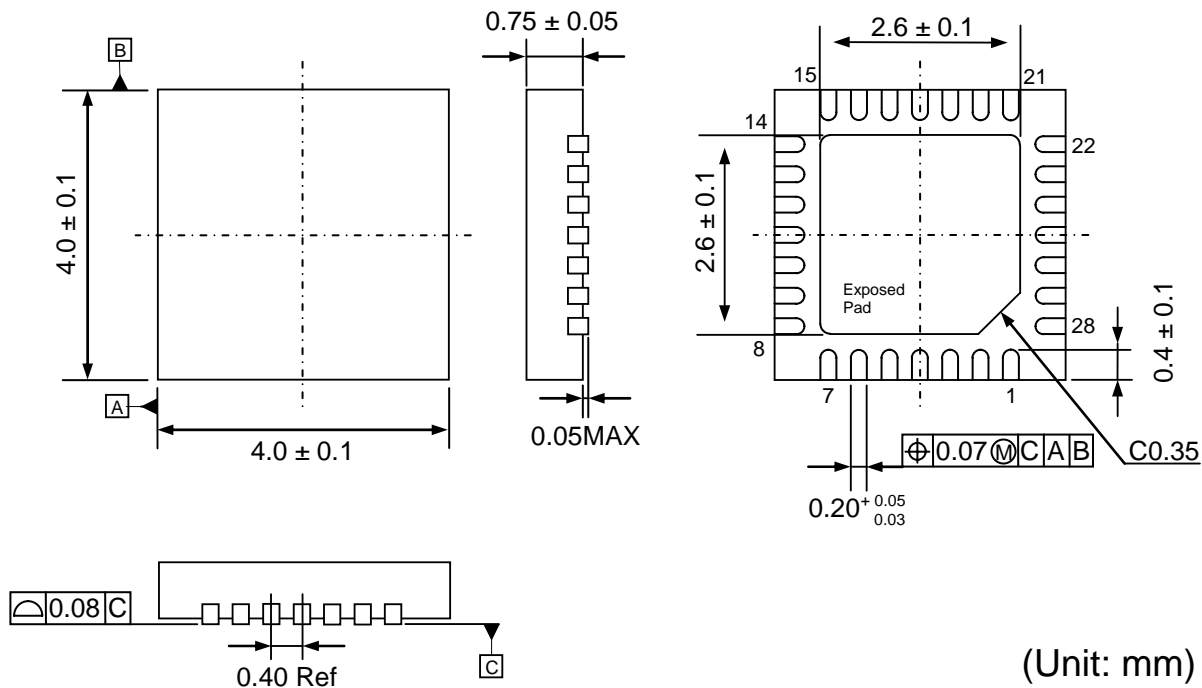
- (1) Stop the external MCKI, BICK and LRCK clocks.

■ Power Down

Power supply current can not be shut down by stopping clocks and setting PMVCM bit = “0”. Power supply current can be shut down (typ. 1μA) by stopping clocks and setting the PDN pin = “L”. When the PDN pin = “L”, all registers are initialized.

PACKAGE

28pin QFN



(Unit: mm)

Note: The exposed pad on the bottom surface of the package must be open or connected to the ground.

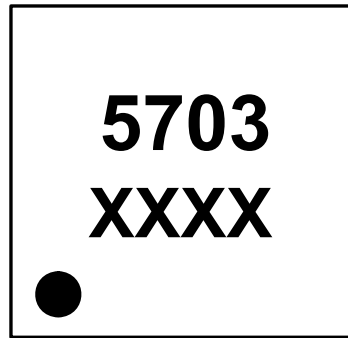
■ Material & Lead finish

Package molding compound: Epoxy Resin, Halogen (Br and Cl) free

Lead frame material: Cu Alloy

Lead frame surface treatment: Solder (Pb free) plate

**MARKING**



1

XXXX: Date code (4 digit)  
Pin #1 indication

|                         |
|-------------------------|
| <b>REVISION HISTORY</b> |
|-------------------------|



| Date (Y/M/D) | Revision | Reason        | Page/Line | Contents |
|--------------|----------|---------------|-----------|----------|
| 13/05/08     | 00       | First Edition |           |          |

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