



**THE DATASHEET OF
MC74HC86ADR2**



Quad 2-Input Exclusive OR Gate

High-Performance Silicon-Gate CMOS

MC74HC86A, MC74HCT86A

The MC74HC86A/MC74HCT86A is identical in pinout to the LS86. The MC74HC86A device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT86A inputs are compatible with Standard CMOS or TTL outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with JEDEC Standard No. 7 A Requirements
- Chip Complexity: 56 FETs or 14 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

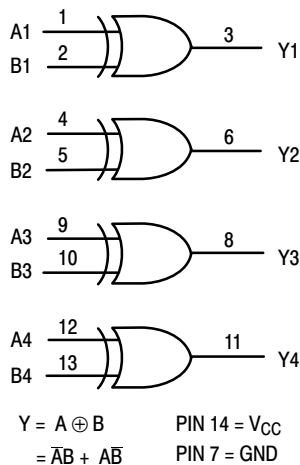


Figure 1. Logic Diagram

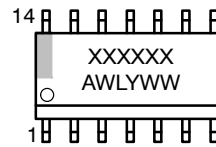


SOIC-14 NB
D SUFFIX
CASE 751A

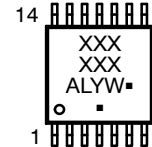


TSSOP-14
DT SUFFIX
CASE 948G

MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

- XXX = Specific Device Code
- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

MC74HC86A, MC74HCT86A

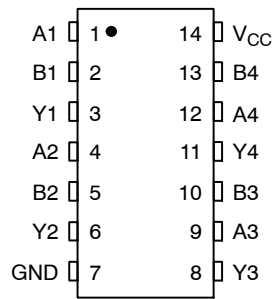


Figure 2. Pinout

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, Per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
I_{IK}	Input Clamp Current ($V_{IN} < 0$ or $V_{IN} > V_{CC}$)	± 20	mA
I_{OK}	Output Clamp Current ($V_{OUT} < 0$ or $V_{OUT} > V_{CC}$)	± 20	mA
T_{STG}	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	$^{\circ}\text{C}$
T_J	Junction Temperature Under Bias	+150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Note 1)	SOIC-14 QFN14 TSSOP-14	116 130 150 $^{\circ}\text{C}/\text{W}$
P_D	Power Dissipation in Still Air at 25 $^{\circ}\text{C}$	SOIC-14 QFN14 TSSOP-20	1077 962 833 mW
MSL	Moisture Sensitivity	Level 1	-
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in -
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	> 2000 N/A V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

MC74HC86A, MC74HCT86A

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
MC74HC				
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN} , V_{OUT}	DC Input, Output Voltage (Referenced to GND) (Note 3)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+125	°C
t_r , t_f	Input Rise or Fall Rate	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	1000 500 400	ns

MC74HCT

V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN} , V_{OUT}	DC Input, Output Voltage (Referenced to GND) (Note 3)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+125	°C
t_r , t_f	Input Rise or Fall Rate	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74HC86A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit	
				-55 to 25°C	≤ 85°C	≤ 125°C		
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{ V or } V_{CC} - 0.1\text{ V}$ $ I_{out} \leq 20\ \mu\text{A}$	2.0	1.5	1.5	1.5	V	
			3.0	2.1	2.1	2.1		
			4.5	3.15	3.15	3.15		
			6.0	4.2	4.2	4.2		
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{ V or } V_{CC} - 0.1\text{ V}$ $ I_{out} \leq 20\ \mu\text{A}$	2.0	0.5	0.5	0.5	V	
			3.0	0.9	0.9	0.9		
			4.5	1.35	1.35	1.35		
			6.0	1.8	1.8	1.8		
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}\text{ or } V_{IL}$ $ I_{out} \leq 20\ \mu\text{A}$	2.0	1.9	1.9	1.9	V	
			4.5	4.4	4.4	4.4		
			6.0	5.9	5.9	5.9		
		$V_{in} = V_{IH}\text{ or } V_{IL}$	$ I_{out} \leq 2.4\text{ mA}$	3.0	2.48	2.34		2.20
			$ I_{out} \leq 4.0\text{ mA}$	4.5	3.98	3.84		3.70
$ I_{out} \leq 5.2\text{ mA}$	6.0	5.48	5.34	5.20				
	V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}\text{ or } V_{IL}$ $ I_{out} \leq 20\ \mu\text{A}$	2.0	0.1	0.1	0.1	V
4.5				0.1	0.1	0.1		
6.0				0.1	0.1	0.1		
$V_{in} = V_{IH}\text{ or } V_{IL}$				$ I_{out} \leq 2.4\text{ mA}$	3.0	0.26	0.33	
	$ I_{out} \leq 4.0\text{ mA}$	4.5	0.26	0.33	0.40			
	$ I_{out} \leq 5.2\text{ mA}$	6.0	0.26	0.33	0.40			
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}\text{ or GND}$	6.0	±0.1	±1.0	±1.0	μA	
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}\text{ or GND}$ $I_{out} = 0\ \mu\text{A}$	6.0	1.0	10	40	μA	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74HC86A, MC74HCT86A

AC ELECTRICAL CHARACTERISTICS (MC74HC86A)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, (A or B) to Y (Figures 3 and 4)	2.0	100	125	150	ns
		3.0	80	90	110	
		4.5	20	25	31	
		6.0	17	21	26	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	

C _{in}	Maximum Input Capacitance	-	10	10	10	pF
C _{PD}	Power Dissipation Capacitance (Per Gate)*	Typical @ 25°C, V _{CC} = 5.0 V			pF	
		33				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

MC74HC86A, MC74HCT86A

DC ELECTRICAL CHARACTERISTICS (MC74HCT86A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5 to 5.5	2.0	2.0	2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5 to 5.5	0.8	0.8	0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	4.5	3.98	3.84	3.70	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	4.5	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	1.0	10	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74HCT86A)

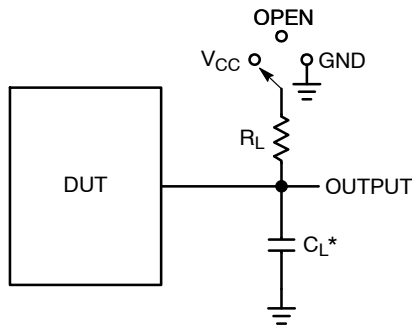
Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit	
			- 55 to 25°C	≤ 85°C	≤ 125°C		
t _{PLH} , t _{PHL}	Maximum Propagation Delay, (A or B) to Y (Figures 3 and 4)	t _{PLH} t _{PHL}	5.0 5.0	20 17	25 21	31 26	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)		5.0	15	19	22	ns
C _{in}	Maximum Input Capacitance		—	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Gate)*	Typical @ 25°C, V _{CC} = 5.0 V		pF
		33		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

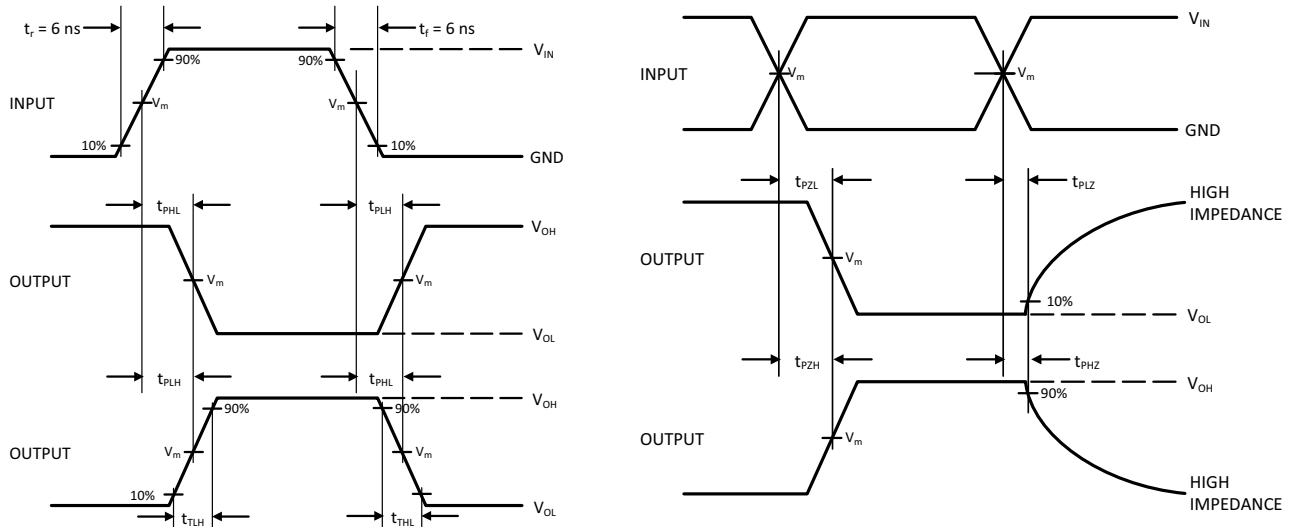
MC74HC86A, MC74HCT86A



*C_L Includes probe and jig capacitance

Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 3. Test Circuit



Device	V _{IN} , V	V _m , V
MC74HC86A	V _{CC}	50% x V _{CC}
MC74HCT86A	3 V	1.5 V

Figure 4. Switching Waveforms

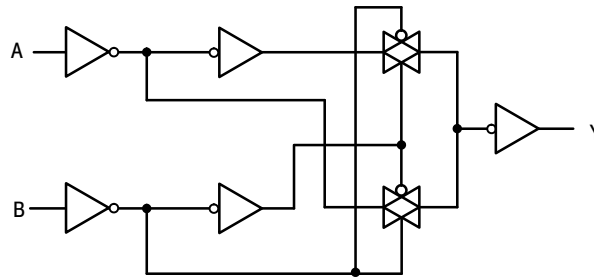


Figure 5. Expanded Logic Diagram
(1/4 of Device)

MC74HC86A, MC74HCT86A

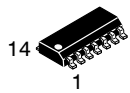
ORDERING INFORMATION

Device	Package	Marking	Shipping [†]
MC74HC86ADG	SOIC-14	HC86A	55 Units / Rail
MC74HC86ADG-Q*	SOIC-14	HC86A	55 Units / Rail
MC74HC86ADR2G	SOIC-14	HC86A	2500 / Tape & Reel
MC74HC86ADR2G-Q*	SOIC-14	HC86A	2500 / Tape & Reel
MC74HC86ADTR2G	TSSOP-14	HC 86A	2500 / Tape & Reel
MC74HC86ADTR2G-Q*	TSSOP-14	HC 86A	2500 / Tape & Reel
MC74HCT86ADR2G	SOIC-14	HCT86A	2500 / Tape & Reel
MC74HCT86ADTR2G	TSSOP-14	HCT 86A	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

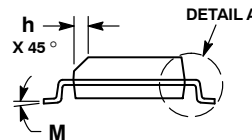
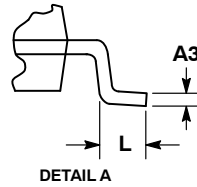
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
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 13. ANODE
 14. ANODE

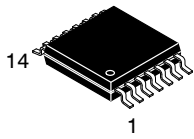
STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*

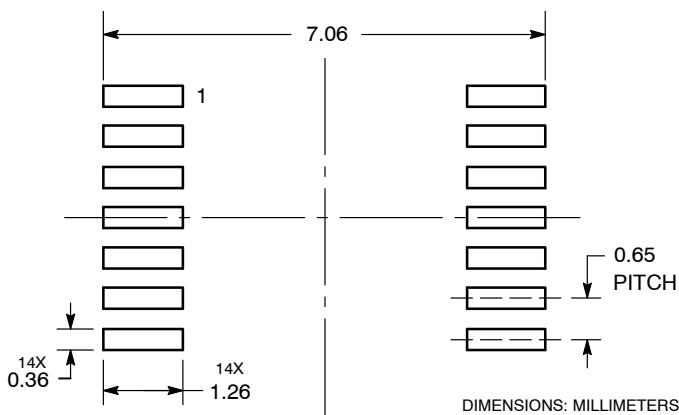


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



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