



**THE DATASHEET OF  
SN75976A1DLRG4**



# SN75976A, SN55976A 9-CHANNEL DIFFERENTIAL TRANSCIVER

SLLS218B – MAY 1995 – REVISED MAY 1997

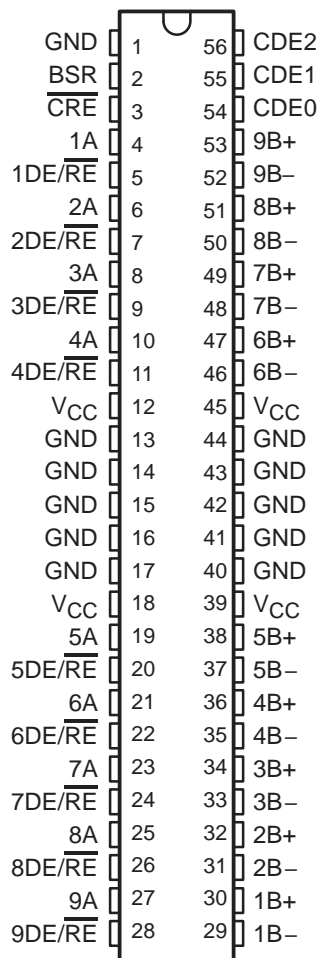
- Improved Speed and Package Replacement for the SN75LBC976
- Designed to Operate at up to 20 Million Data Transfers per Second (Fast-20 SCSI)
- Nine Differential Channels for the Data and Control Paths of the Small Computer Systems Interface (SCSI) and Intelligent Peripheral Interface (IPI)
- SN75976A Packaged in Shrink Small-Outline Package with 25-Mil Terminal Pitch (DL) and Thin Shrink Small-Outline Package with 20-Mil Terminal Pitch (DGG)
- SN55976A Packaged in a 56-Pin Ceramic Flat Pack (WD)
- Two Skew Limits Available
- ESD Protection on Bus Terminals Exceeds 12 kV
- Low Disabled Supply Current 8 mA Typ
- Thermal Shutdown Protection
- Positive- and Negative-Current Limiting
- Power-Up/Down Glitch Protection

## description

The SN75976A is an improved replacement for the industry's first 9-channel RS-485 transceiver — the SN75LBC976. The A version offers improved switching performance, a smaller package, and higher ESD protection. The SN75976A is offered in two versions. The '976A2 skew limits of 4 ns for the differential drivers and 5 ns for the differential receivers complies with the recommended skew budget of the Fast-20 SCSI standard for data transfer rates up to 20 million transfers per second. The '976A1 supports the Fast SCSI skew budget for 10 million transfers per second. The skew limit ensures that the propagation delay times, not only from channel-to-channel but from device-to-device, are closely matched for the tight skew budgets associated with high-speed parallel data buses.

The patented thermal enhancements made to the 56-pin shrink small-outline package (SSOP) of the SN75976 have been applied to the new, thin shrink, small-outline package (TSSOP). The TSSOP package offers even less board area requirements than the SSOP while reducing the package height to 1 mm. This provides more board area and allows component mounting to both sides of the printed circuit boards for low-profile, space-restricted applications such as small form-factor hard disk drives.

SN75976A DGG or DL  
SN55976A WD  
(TOP VIEW)



Terminals 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.



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## description (continued)

In addition to speed improvements, the '976A can withstand electrostatic discharges exceeding 12 kV using the human-body model, and 600 V using the machine model of MIL-PRF-38535, Method 3015.7 on the RS-485 I/O terminals. This is six times the industry standard and provides protection from the noise that can be coupled into external cables. The other terminals of the device can withstand discharges exceeding 4 kV and 400 V respectively.

Each of the nine channels of the '976A typically meet or exceed the requirements of EIA RS-485 (1983) and ISO 8482-1987/TIA TR30.2 referenced by American National Standard of Information (ANSI) Systems, X3.131-1994 (SCSI-2) standard, X2.277-1996 (Fast-20 Parallel Interface), and the Intelligent Peripheral Interface Physical Layer-ANSI X3.129-1986 standard.

The SN75976A is characterized for operation over an ambient air temperature range of 0°C to 70°C. The SN55976A is characterized for operation over an ambient air temperature range of –55°C to 125°C.

### AVAILABLE OPTIONS

| T <sub>A</sub> | Skew Limit (ns) |          | PACKAGE†                      |                             |                        |
|----------------|-----------------|----------|-------------------------------|-----------------------------|------------------------|
|                | Driver          | Receiver | TSSOP (DGG)                   | SSOP (DL)                   | CERAMIC FLAT PACK (WD) |
| 0°C to 70°C    | 8               | 9        | SN75976A1DGG<br>SN75976A1DGGR | SN75976A1DL<br>SN75976A1DLR | —                      |
|                | 4               | 5        | SN75976A2DGG<br>SN75976A2DGGR | SN75976A2DL<br>SN75976A2DLR | —                      |
| –55°C to 125°C | 8               | 9        | —                             | —                           | SN55976A1WD            |
|                | 4               | 5        | —                             | —                           | SN55976A2WD            |

† The R suffix indicates taped and reeled packages.



### Terminal Functions

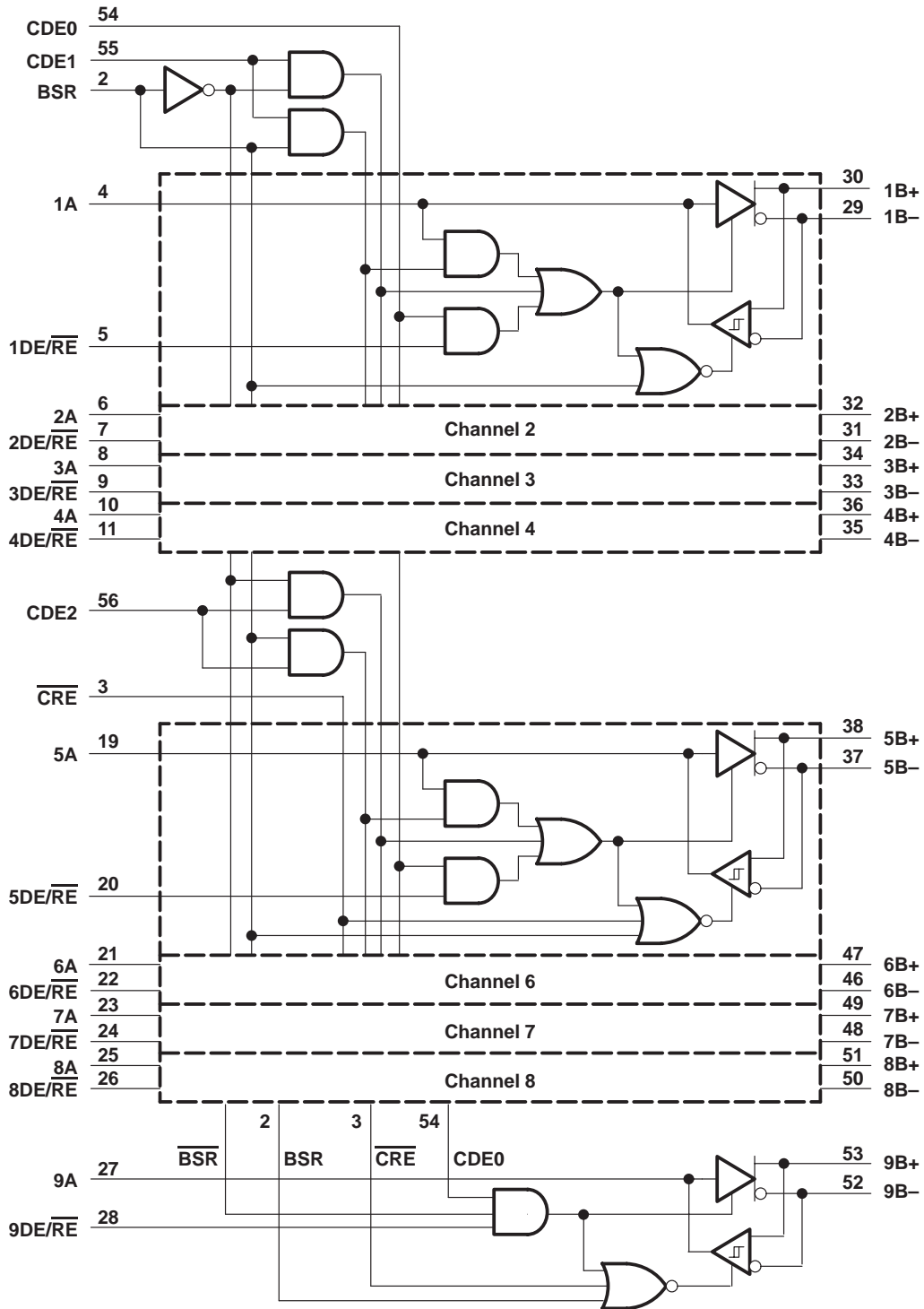
| TERMINAL NAME    | NO.   | Logic Level | I/O   | Termination | DESCRIPTION   |
|------------------|---|-------------|-------|-------------|---|
| 1A to 9A         | 4,6,8,10,<br>19,21,23,<br>25,27             | TTL         | I/O   | Pullup      | 1A to 9A carry data to and from the communication controller.   |
| 1B– to 9B–       | 29,31,33,<br>35,37,46,<br>48,50,52          | RS-485      | I/O   | Pulldown    | 1B– to 9B– are the inverted data signals of the balanced pair to/from the bus.  |
| 1B+ to 9B+       | 30,32,34,<br>36,38,47,<br>49,51,53          | RS-485      | I/O   | Pullup      | 1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus.   |
| BSR              | 2   | TTL         | Input | Pullup      | BSR is the bit significant response. BSR disables receivers 1 through 8 and enables wired-OR drivers when BSR and DE/RE and CDE1 or CDE2 are high. Channel 9 is placed in a high-impedance state with BSR high. |
| CDE0             | 54  | TTL         | Input | Pulldown    | CDE0 is the common driver enable 0. Its input signal enables all drivers when CDE0 and 1DE/RE – 9DE/RE are high.  |
| CDE1             | 55  | TTL         | Input | Pulldown    | CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when CDE1 is high and BSR is low.   |
| CDE2             | 56  | TTL         | Input | Pulldown    | CDE2 is the common driver enable 2. When CDE2 is high and BSR is low, drivers 5 to 8 are enabled.   |
| CRE              | 3   | TTL         | Input | Pullup      | CRE is the common receiver enable. When high, CRE disables receiver channels 5 to 9.  |
| 1DE/RE to 9DE/RE | 5,7,9,11,<br>20,22,24,<br>26,28             | TTL         | Input | Pullup      | 1DE/RE–9DE/RE are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when 1DE/RE–9DE/RE and CRE and BSR are low and CDE1 and CDE2 are low.               |
| GND              | 1,13,14,<br>15,16,17,<br>40,41,42,<br>43,44 | NA          | Power | NA          | GND is the circuit ground. All GND terminals except terminal 1 are physically tied to the die pad for improved thermal conductivity.†   |
| VCC              | 12,18,39,<br>45                             | NA          | Power | NA          | Supply voltage  |

† Terminal 1 must be connected to signal ground for proper operation.

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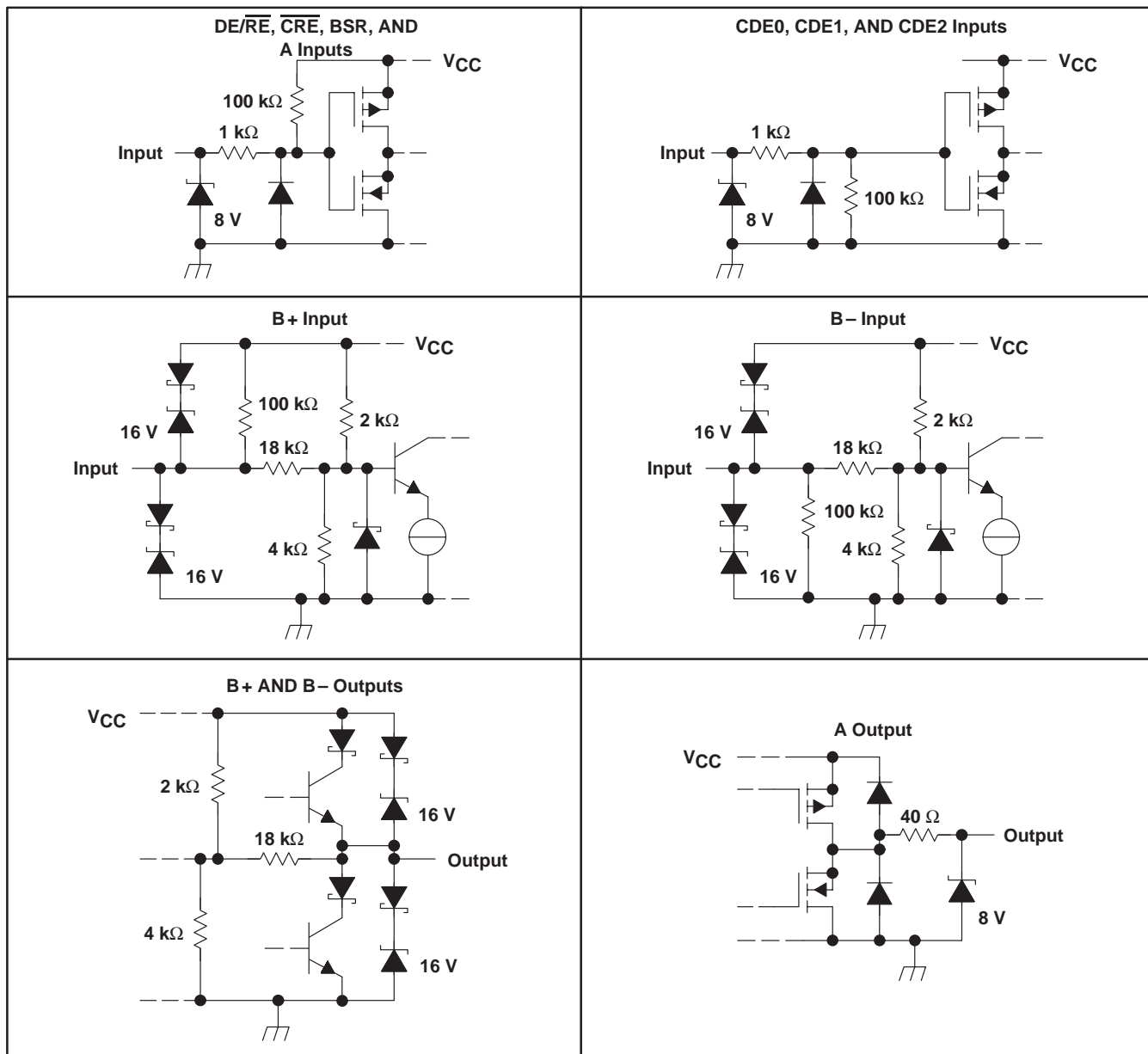
## logic diagram (positive logic)



# SN75976A, SN55976A 9-CHANNEL DIFFERENTIAL TRANSCIEVER

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## schematics of inputs and outputs



# SN75976A, SN55976A 9-CHANNEL DIFFERENTIAL TRANSCEIVER

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |       |                            |
|---|-------|----------------------------|
| Supply voltage range, $V_{CC}$ (see Note 1)                       | ..... | -0.3 V to 6 V              |
| Bus voltage range   | ..... | -10 V to 15 V              |
| Data I/O and control (A side) voltage range                       | ..... | -0.3 V to $V_{CC} + 0.5$ V |
| Electrostatic discharge: B side and GND, Class 3, A: (see Note 2) | ..... | 12 kV                      |
| B side and GND, Class 3, B: (see Note 2)                          | ..... | 400 V                      |
| All terminals, Class 3, A:  | ..... | 4 kV                       |
| All terminals, Class 3, B:  | ..... | 400 V                      |
| Continuous total power dissipation (see Note 3)                   | ..... | internally limited         |
| Storage temperature range, $T_{stg}$                              | ..... | -65°C to 150°C             |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds      | ..... | 260°C                      |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the GND terminals.  
 2. This absolute maximum rating is tested in accordance with MIL-PRF-38535, Method 3015.7.  
 3. The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ | OPERATING FACTOR‡<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 125^\circ\text{C}$<br>POWER RATING |
|---------|-----------------------------|---|--|---|
| DGG     | 2500 mW                     | 20 mW/°C  | 1600 mW                                  | —   |
| DL      | 2500 mW                     | 20 mW/°C  | 1600 mW                                  | —   |
| WD      | 1300 mW                     | 10.5 mW/°C  | 827 mW                                   | 250 mW                                    |

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## package thermal characteristics

|   |                                 | MIN | NOM  | MAX | UNIT |
|---|---------------------------------|-----|------|-----|------|
| Junction-to-ambient thermal resistance, $R_{\theta JA}$ | DGG, board-mounted, no air flow |     | 50   |     | °C/W |
|   | DL, board-mounted, no air flow  |     | 50   |     | °C/W |
| Junction-to-ambient thermal resistance, $R_{\theta JA}$ | WD                              |     | 95.4 |     | °C/W |
| Junction-to-case thermal resistance, $R_{\theta JC}$    | DGG                             |     | 27   |     | °C/W |
|   | DL                              |     | 12   |     | °C/W |
| Junction-to-case thermal resistance, $R_{\theta JC}$    | WD                              |     | 5.67 |     | °C/W |
| Thermal-shutdown junction temperature, $T_{JS}$         |                                 |     | 165  |     | °C   |



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## recommended operating conditions

|  |                  | MIN  | NOM | MAX  | UNIT |
|--|------------------|------|-----|------|------|
| Supply voltage, $V_{CC}$   |                  | 4.75 | 5   | 5.25 | V    |
| High-level input voltage, $V_{IH}$   | Except nB+, nB-† | 2    |     |      | V    |
| Low-level input voltage, $V_{IL}$  | Except nB+, nB-† |      |     | 0.8  | V    |
| Voltage at any bus terminal (separately or common-mode), $V_O$ , $V_I$ , or $V_{IC}$ | nB+ or nB -      |      |     | 12   | V    |
|  |                  |      |     | -7   | V    |
| High-level output current, $I_{OH}$  | Driver           |      |     | -60  | mA   |
|  | Receiver         |      |     | -8   | mA   |
| Low-level output current, $I_{OL}$   | Driver           |      |     | 60   | mA   |
|  | Receiver         |      |     | 8    | mA   |
| Operating case temperature, $T_C$  | SN75976A         | 0    |     | 125  | °C   |
| Operating free-air temperature, $T_A$  | SN75976A         | 0    |     | 70   | °C   |
|  | SN55976A         | -55  |     | 125  | °C   |

† n = 1 – 9



# SN75976A, SN55976A

## 9-CHANNEL DIFFERENTIAL TRANSCEIVER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS   | SN55976A |      | SN75976A                                |      | UNIT                                    |      |
|---|---|----------|------|---|------|---|------|
|   |   | MIN      | TYP† | MAX                                     | MIN  |   | TYP† |
| V <sub>ODH</sub> Driver differential high-level output voltage                    | S1 to A, V <sub>T</sub> = 5 V, See Figure 1                             | 0.7      |      |   | 1    | 1.8                                     | V    |
|   | S1 to B, V <sub>T</sub> = 5 V, T <sub>C</sub> ≥ 25°C, See Figure 1      |          |      |   | 1    | 1.4                                     | V    |
|   | S1 to B, V <sub>T</sub> = 5 V, See Figure 1                             | 0.7      |      |   | 0.8  |   | V    |
| V <sub>ODL</sub> Driver differential low-level output voltage                     | S1 to A, V <sub>T</sub> = 5 V, T <sub>C</sub> ≥ 25°C, See Figure 1      | 0.7      | -1.4 |   | -1   | -1.4                                    | V    |
|   | S1 to B, V <sub>T</sub> = 5 V, See Figure 1                             | 0.7      | -1.8 |   | -1   | -1.8                                    | V    |
|   | S1 to A, V <sub>T</sub> = 5 V, See Figure 1                             | -0.8     | -1.4 |   | -0.8 | -1.4                                    | V    |
| V <sub>OH</sub> High-level output voltage   | A side, I <sub>OH</sub> = -8 mA, V <sub>ID</sub> = 200 mV, See Figure 3 | 4        | 4.5  |   | 4    | 4.5                                     | V    |
|   | B side, V <sub>T</sub> = 5 V, See Figure 1                              |          | 3    |   | 3    |   | V    |
| V <sub>OL</sub> Low-level output voltage  | A side, I <sub>OH</sub> = 8 mA, V <sub>ID</sub> = -200 mV, See Figure 3 |          | 0.6  | 0.8                                     | 0.6  | 0.8                                     | V    |
|   | A side, V <sub>T</sub> = 5 V, See Figure 1                              |          | 1    |   | 1    |   | V    |
| V <sub>IT+</sub> Receiver positive-going differential input threshold voltage     | I <sub>OH</sub> = -8 mA, See Figure 3                                   |          |      | 0.2                                     |      | 0.2                                     | V    |
| V <sub>IT-</sub> Receiver negative-going differential input threshold voltage     | I <sub>OL</sub> = 8 mA, See Figure 3                                    |          |      | -0.2                                    |      | -0.2                                    | V    |
| V <sub>hys</sub> Receiver input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> ) | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C                            | 24       | 45   |   | 24   | 45                                      | mV   |
| I <sub>I</sub> Bus input current  | V <sub>IH</sub> = 12 V, V <sub>CC</sub> = 5 V, Other input at 0 V       |          | 0.4  | 1                                       | 0.4  | 1                                       | mA   |
|   | V <sub>IH</sub> = 12 V, V <sub>CC</sub> = 0, Other input at 0 V         |          | 0.5  | 1                                       | 0.5  | 1                                       | mA   |
|   | V <sub>IH</sub> = -7 V, V <sub>CC</sub> = 5 V, Other input at 0 V       |          | -0.4 | -0.8                                    | -0.4 | -0.8                                    | mA   |
|   | V <sub>IH</sub> = -7 V, V <sub>CC</sub> = 0, Other input at 0 V         |          | -0.3 | -0.8                                    | -0.3 | -0.8                                    | mA   |
| I <sub>IH</sub> High-level input current  | A, BSR, DE/RE, and CRE, V <sub>IH</sub> = 2 V                           |          |      | -100                                    |      | -100                                    | μA   |
|   | CDE0, CDE1, and CDE2, V <sub>IH</sub> = 2 V                             |          |      | 100                                     |      | 100                                     | μA   |
| I <sub>IL</sub> Low-level input current   | A, BSR, DE/RE, and CRE, V <sub>IL</sub> = 0.8 V                         |          |      | -100                                    |      | -100                                    | μA   |
|   | CDE1, CDE1, and CDE2, V <sub>IL</sub> = 0.8 V                           |          |      | 100                                     |      | 100                                     | μA   |
| I <sub>OS</sub> Short circuit output current                                      | nB+ or nB-  |          |      | ±260                                    |      | ±260                                    | mA   |
| I <sub>OZ</sub> High-impedance-state output current                               | A   |          |      | See I <sub>IH</sub> and I <sub>IL</sub> |      | See I <sub>IH</sub> and I <sub>IL</sub> |      |
|   | nB+ or nB-  |          |      | See I <sub>I</sub>                      |      | See I <sub>I</sub>                      |      |
| I <sub>CC</sub> Supply current  | Disabled  |          |      | 10                                      |      | 10                                      | mA   |
|   | All drivers enabled, no load  |          |      | 60                                      |      | 60                                      | mA   |
|   | All receivers enabled, no load  |          |      | 45                                      |      | 45                                      | mA   |
| C <sub>O</sub> Output capacitance   | nB+ or nB- to GND   |          | 18   |   | 18   | 25                                      | pF   |
| C <sub>pd</sub> Power dissipation capacitance (see Note 4)                        | Receiver  |          | 40   |   | 40   |   | pF   |
|   | Driver  |          | 100  |   | 100  |   | pF   |

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTE 4: C<sub>pd</sub> determines the no-load dynamic supply current consumption, I<sub>S</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f + I<sub>CC</sub>



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## driver switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER     |   | TEST CONDITIONS       | SN75976A                                       |      |      | UNIT |
|---------------|---|-----------------------|--|------|------|------|
|               |   |                       | MIN  | TYP† | MAX  |      |
| $t_{pd}$      | Propagation delay time, $t_{PHL}$ or $t_{PLH}$<br>(see Figures 1 and 2) | '976A1                |  | 2.5  | 13.5 | ns   |
|               |   |                       | $V_{CC} = 5\text{ V}, T_C = 25^\circ\text{C}$  | 3    | 11   | ns   |
|               |   |                       | $V_{CC} = 5\text{ V}, T_C = 100^\circ\text{C}$ | 5    | 13   | ns   |
|               |   | '976A2                |  | 4.5  | 11.5 | ns   |
|               |   |                       | $V_{CC} = 5\text{ V}, T_C = 25^\circ\text{C}$  | 5    | 9    | ns   |
|               |   |                       | $V_{CC} = 5\text{ V}, T_C = 100^\circ\text{C}$ | 7    | 11   | ns   |
| $t_{sk(lim)}$ | Skew limit, maximum $t_{pd}$ – minimum $t_{pd}$<br>(see Note 5)         | '976A1                |  | 8    | ns   |      |
|               |   | '976A2                |  | 4    | ns   |      |
| $t_{sk(p)}$   | Pulse skew, $ t_{PHL} - t_{PLH} $                                       |                       |  | 4    | ns   |      |
| $t_f$         | Fall time   | S1 to B, See Figure 2 |  | 4    | ns   |      |
| $t_r$         | Rise time   | See Figure 2          |  | 8    | ns   |      |
| $t_{en}$      | Enable time, control inputs to active output                            |                       |  | 50   | ns   |      |
| $t_{dis}$     | Disable time, control inputs to high-impedance output                   |                       |  | 100  | ns   |      |
| $t_{PHZ}$     | Propagation delay time, high-level to high-impedance output             | See Figures 5 and 6   |  | 17   | 100  | ns   |
| $t_{PLZ}$     | Propagation delay time, low-level to high-impedance output              |                       |  | 25   | 100  | ns   |
| $t_{PZH}$     | Propagation delay time, high-impedance to high-level output             |                       |  | 17   | 50   | ns   |
| $t_{PZL}$     | Propagation delay time, high-impedance to low-level output              |                       |  | 17   | 50   | ns   |

† All typical values are at  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ .

NOTE 5: This parameter is applicable at one  $V_{CC}$  and operating temperature within the recommended operating conditions and to any two devices.

## driver switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER     |   | TEST CONDITIONS       | SN55976A                                      |      |      | UNIT |
|---------------|---|-----------------------|---|------|------|------|
|               |   |                       | MIN   | TYP† | MAX  |      |
| $t_{pd}$      | Propagation delay time, $t_{PHL}$ or $t_{PLH}$<br>(see Figures 1 and 2) | '976A1                | $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ |      | 15   | ns   |
|               |   | '976A2                | $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ |      | 13.5 | ns   |
| $t_{sk(lim)}$ | Skew limit, maximum $t_{pd}$ – minimum $t_{pd}$<br>(see Note 5)         | '976A1                |   |      | 8    | ns   |
|               |   | '976A2                |   |      | 4    | ns   |
| $t_{sk(p)}$   | Pulse skew, $ t_{PHL} - t_{PLH} $                                       |                       |   | 4    | ns   |      |
| $t_f$         | Fall time   | S1 to B, See Figure 2 |   | 4    | ns   |      |
| $t_r$         | Rise time   | See Figure 2          |   | 8    | ns   |      |
| $t_{en}$      | Enable time, control inputs to active output                            |                       |   | 60   | ns   |      |
| $t_{dis}$     | Disable time, control inputs to high-impedance output                   |                       |   | 140  | ns   |      |
| $t_{PHZ}$     | Propagation delay time, high-level to high-impedance output             | See Figures 5 and 6   |   |      | 120  | ns   |
| $t_{PLZ}$     | Propagation delay time, low-level to high-impedance output              |                       |   |      | 120  | ns   |
| $t_{PZH}$     | Propagation delay time, high-impedance to high-level output             |                       |   |      | 60   | ns   |
| $t_{PZL}$     | Propagation delay time, high-impedance to low-level output              |                       |   |      | 60   | ns   |

† All typical values are at  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ .

NOTE 5: This parameter is applicable at one  $V_{CC}$  and operating temperature within the recommended operating conditions and to any two devices.



# SN75976A, SN55976A

## 9-CHANNEL DIFFERENTIAL TRANSCEIVER

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### receiver switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER            |   | TEST CONDITIONS     | SN75976A                                      |      |      | UNIT |
|----------------------|---|---------------------|---|------|------|------|
|                      |   |                     | MIN   | TYP† | MAX  |      |
| t <sub>pd</sub>      | Propagation delay time, t <sub>PHL</sub> or t <sub>PLH</sub><br>(see Figures 3 and 4) | '976A1              |   | 7.5  | 16.5 | ns   |
|                      |   | '976A2              |   | 8.5  | 14.5 | ns   |
|                      |   |                     | V <sub>CC</sub> = 5 V, T <sub>C</sub> = 25°C  | 8.6  | 13.6 | ns   |
|                      |   |                     | V <sub>CC</sub> = 5 V, T <sub>C</sub> = 100°C | 9    | 14   | ns   |
| t <sub>sk(lim)</sub> | Skew limit, maximum t <sub>pd</sub> – minimum t <sub>pd</sub><br>(see Note 5)         | '976A1              |   |      | 9    | ns   |
|                      |   | '976A2              |   |      | 5    | ns   |
| t <sub>sk(p)</sub>   | Pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>                                      |                     | 0.6   | 4    | ns   |      |
| t <sub>t</sub>       | Transition time (t <sub>r</sub> or t <sub>f</sub> )                                   | See Figure 4        |   | 2    | ns   |      |
| t <sub>en</sub>      | Enable time, control inputs to active output  |                     |   | 50   | ns   |      |
| t <sub>dis</sub>     | Disable time, control inputs to high-impedance output                                 |                     |   | 60   | ns   |      |
| t <sub>PHZ</sub>     | Propagation delay time, high-level to high-impedance output                           | See Figures 7 and 8 |   |      | 60   | ns   |
| t <sub>PLZ</sub>     | Propagation delay time, low-level to high-impedance output                            |                     |   |      | 50   | ns   |
| t <sub>PZH</sub>     | Propagation delay time, high-impedance to high-level output                           |                     |   |      | 50   | ns   |
| t <sub>PZL</sub>     | Propagation delay time, high-impedance to low-level output                            |                     |   |      | 50   | ns   |

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTE 5. This parameter is applicable at one V<sub>CC</sub> and operating temperature within the recommended operating conditions and to any two devices.

### receiver switching characteristics over recommended operating conditions (unless otherwise noted)

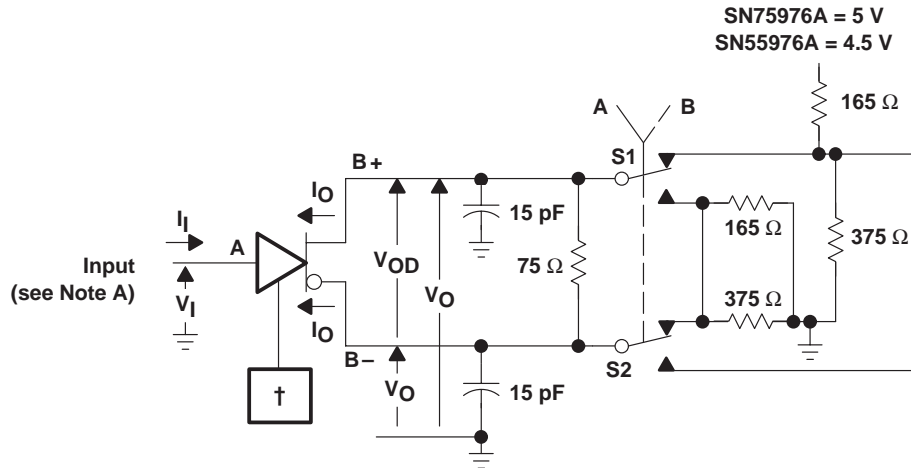
| PARAMETER            |   | TEST CONDITIONS     | SN55976A                                     |      |     | UNIT |
|----------------------|---|---------------------|--|------|-----|------|
|                      |   |                     | MIN  | TYP† | MAX |      |
| t <sub>pd</sub>      | Propagation delay time, t <sub>PHL</sub> or t <sub>PLH</sub><br>(see Figures 3 and 4) | '976A1              | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C |      | 19  | ns   |
|                      |   | '976A2              | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C |      | 16  | ns   |
| t <sub>sk(lim)</sub> | Skew limit, maximum t <sub>pd</sub> – minimum t <sub>pd</sub><br>(see Note 5)         | '976A1              |  |      | 9   | ns   |
|                      |   | '976A2              |  |      | 5   | ns   |
| t <sub>sk(p)</sub>   | Pulse skew,  t <sub>PHL</sub> – t <sub>PLH</sub>                                      |                     |  | 0.6  | 4   | ns   |
| t <sub>t</sub>       | Transition time (t <sub>r</sub> or t <sub>f</sub> )                                   | See Figure 4        |  | 2    | ns  |      |
| t <sub>en</sub>      | Enable time, control inputs to active output  |                     |  | 70   | ns  |      |
| t <sub>dis</sub>     | Disable time, control inputs to high-impedance output                                 |                     |  | 80   | ns  |      |
| t <sub>PHZ</sub>     | Propagation delay time, high-level to high-impedance output                           | See Figures 7 and 8 |  |      | 80  | ns   |
| t <sub>PLZ</sub>     | Propagation delay time, low-level to high-impedance output                            |                     |  |      | 70  | ns   |
| t <sub>PZH</sub>     | Propagation delay time, high-impedance to high-level output                           |                     |  |      | 70  | ns   |
| t <sub>PZL</sub>     | Propagation delay time, high-impedance to low-level output                            |                     |  |      | 70  | ns   |

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTE 5. This parameter is applicable at one V<sub>CC</sub> and operating temperature within the recommended operating conditions and to any two devices.



PARAMETER MEASUREMENT INFORMATION



† CDE0 and DE/RE are at 2 V, BSR is at 0.8 V and, for the SN75976A only, all others are open.  
‡ For the SN75976A only, all nine drivers are enabled, similarly loaded, and switching.

Figure 1. Driver Test Circuit, Currents, and Voltages†‡

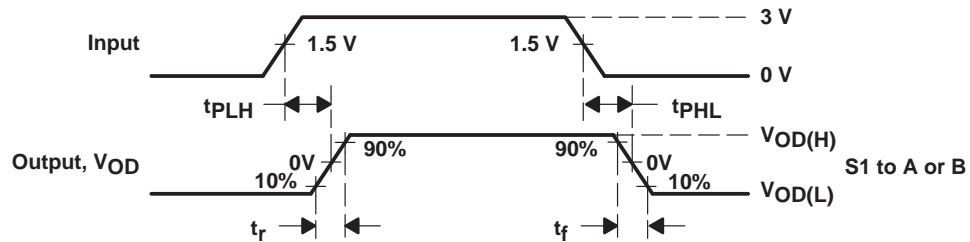
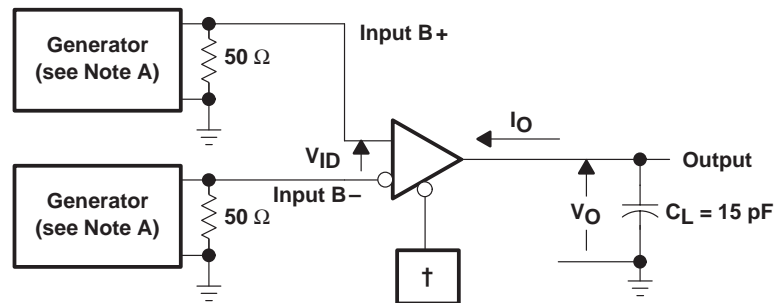


Figure 2. Driver Delay and Transition Time Test Waveforms



† CDE0, CDE1, CDE2, BSR, CRE, and DE/RE at 0.8 V  
‡ For the SN75976A only, all nine receivers are enabled and switching.

Figure 3. Receiver Propagation Delay and Transition Time Test Circuit†‡

- NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .  
B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.  
C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.  
D. All indicated voltages are  $\pm 10$  mV.

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## PARAMETER MEASUREMENT INFORMATION

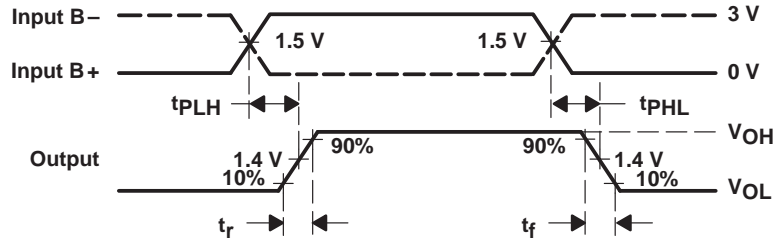
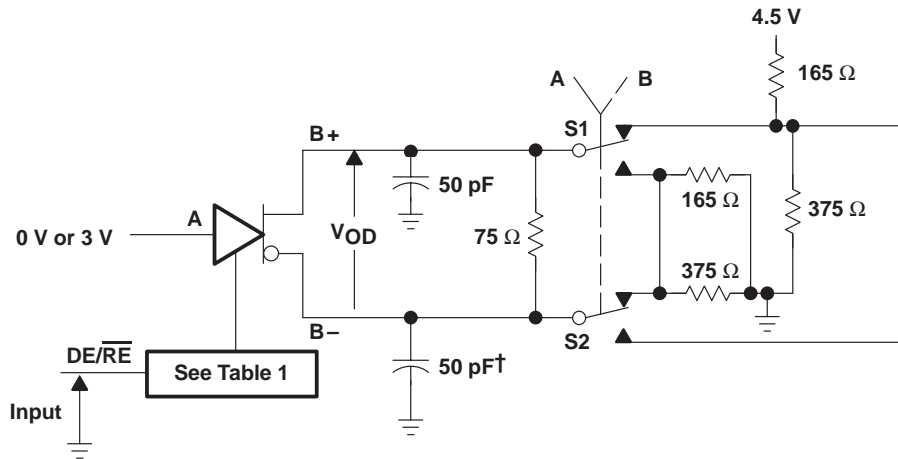


Figure 4. Receiver Delay and Transition Time Waveforms



† Includes probe and jig capacitance in two places.

Figure 5. Driver Enable and Disable Time Test Circuit

Table 1. Enabling For Driver Enable And Disable Time

| DRIVER | BSR | CDE0 | CDE1 | CDE2 | $\overline{\text{CRE}}$ |
|--------|-----|------|------|------|-------------------------|
| 1 – 8  | H   | H    | L    | L    | X                       |
| 9      | L   | H    | H    | H    | H                       |

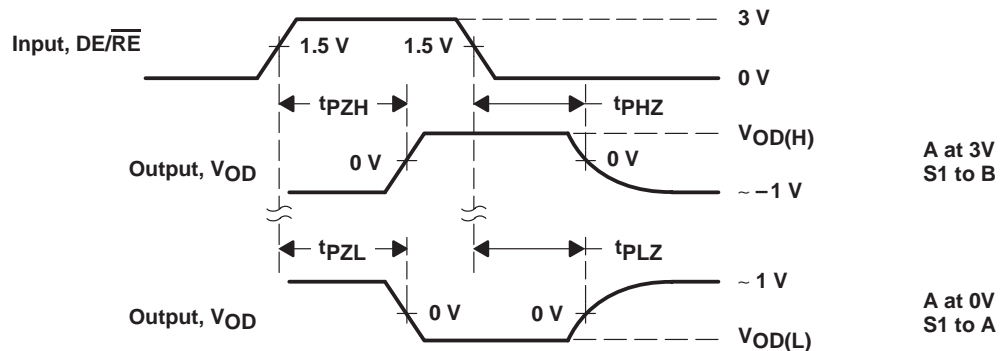
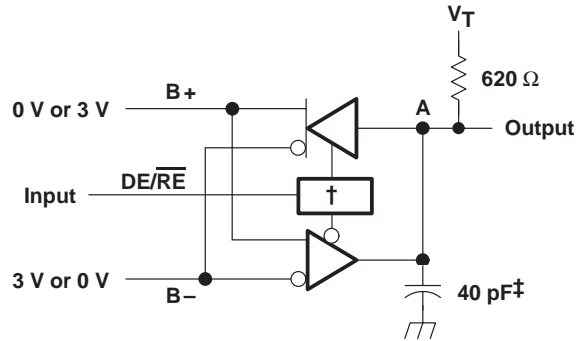


Figure 6. Driver Enable Time Waveforms

- NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $\text{PRR} \leq 1$  MHz, duty cycle = 50%,  $Z_0 = 50 \Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

PARAMETER MEASUREMENT INFORMATION



† CDE0 is high, CDE1, CDE2, BSR, and CRE are low and, for the SN75976A only, all others are open.

‡ Includes probe and jig capacitance.

Figure 7. Receiver Enable and Disable Time Test Circuit

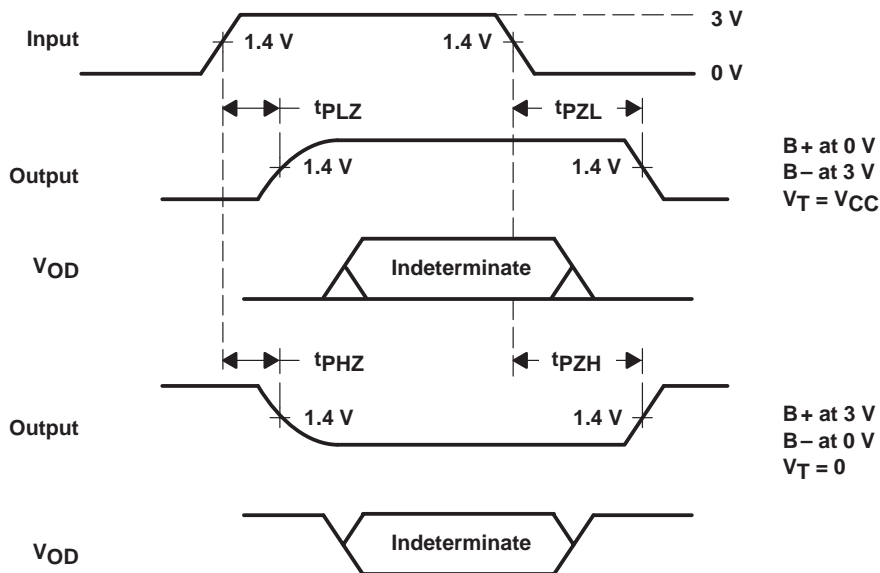


Figure 8. Receiver Enable and Disable Time Waveforms

- NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $PRR \leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

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## TYPICAL CHARACTERISTICS

**AVERAGE SUPPLY CURRENT  
vs  
FREQUENCY**

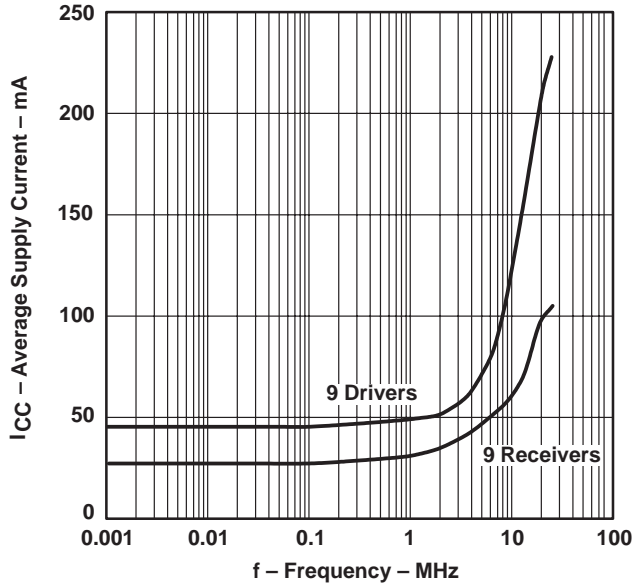


Figure 9

**LOGIC INPUT CURRENT  
vs  
INPUT VOLTAGE**

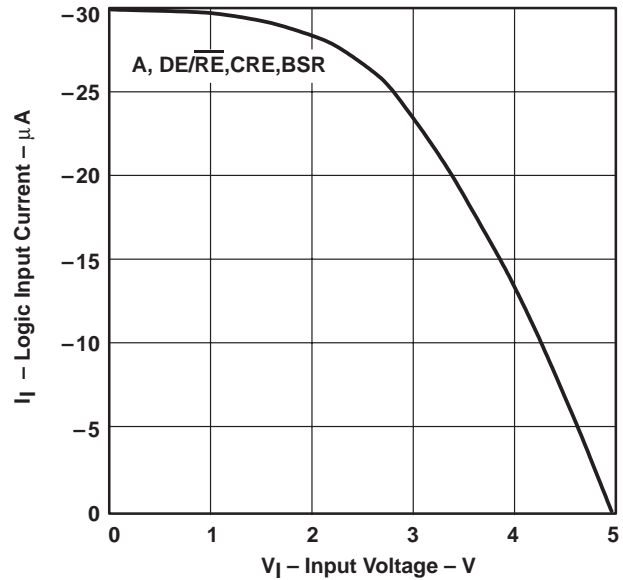


Figure 10

**BUS  
INPUT CURRENT  
vs  
INPUT VOLTAGE**

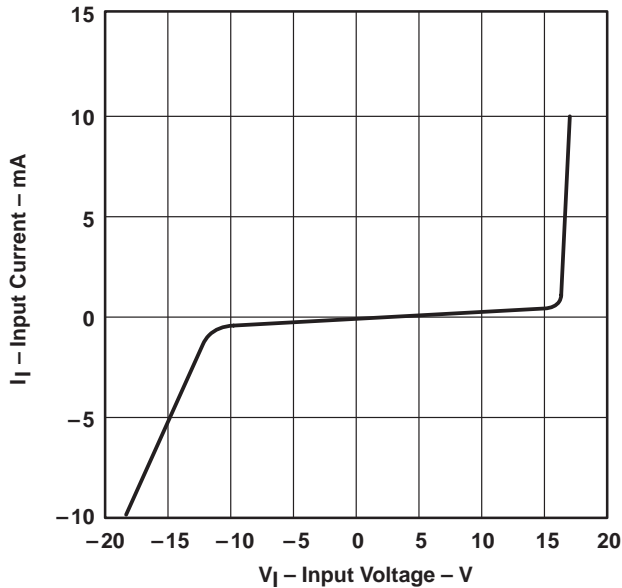


Figure 11

**DRIVER  
LOW-LEVEL OUTPUT VOLTAGE  
vs  
LOW-LEVEL OUTPUT CURRENT**

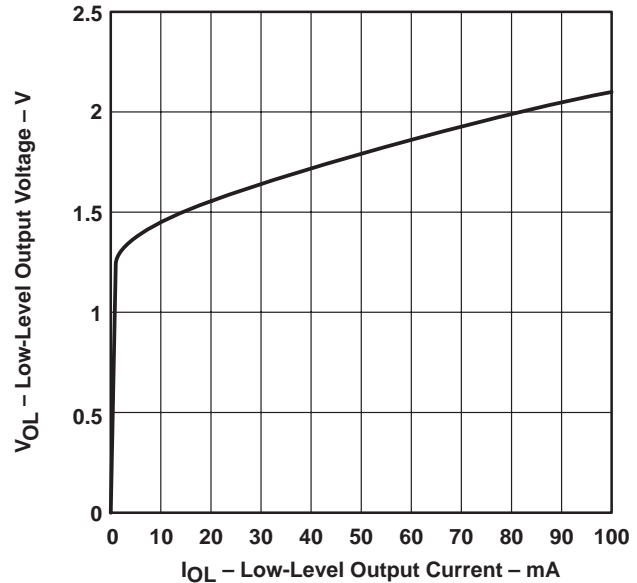
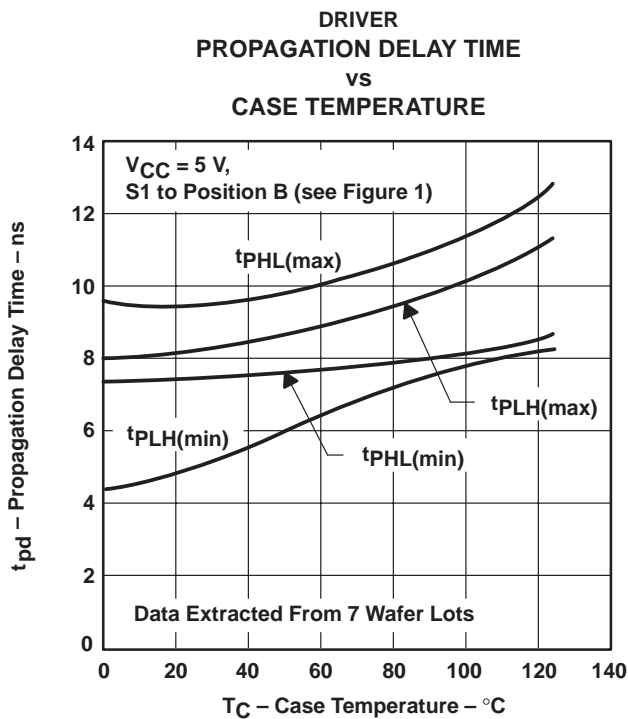
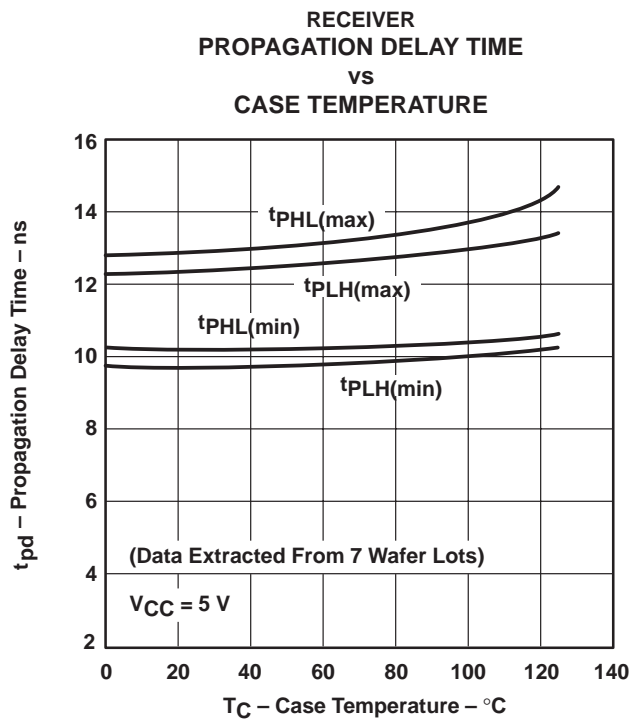
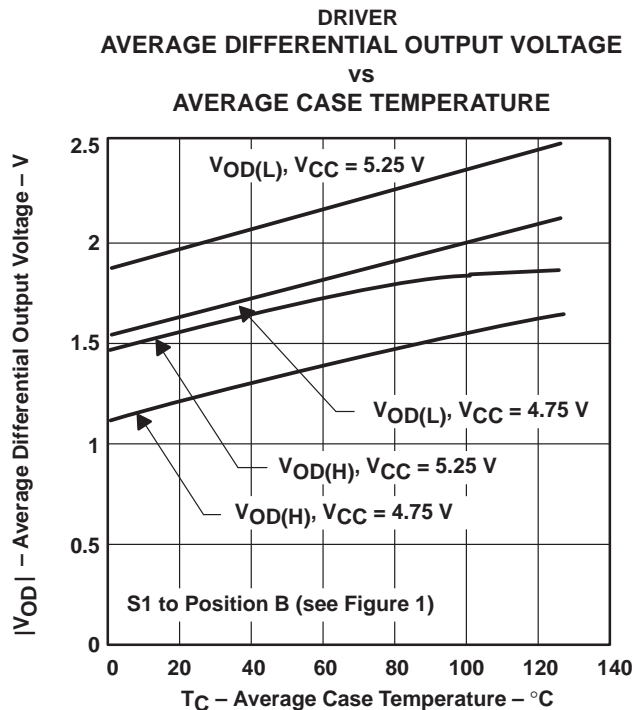
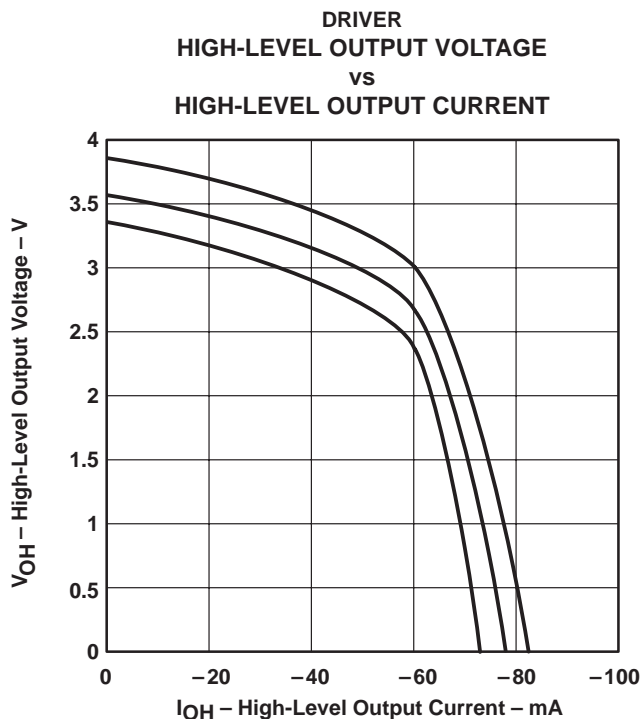


Figure 12

TYPICAL CHARACTERISTICS



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## TYPICAL CHARACTERISTICS

DRIVER  
OUTPUT CURRENT  
vs  
SUPPLY VOLTAGE

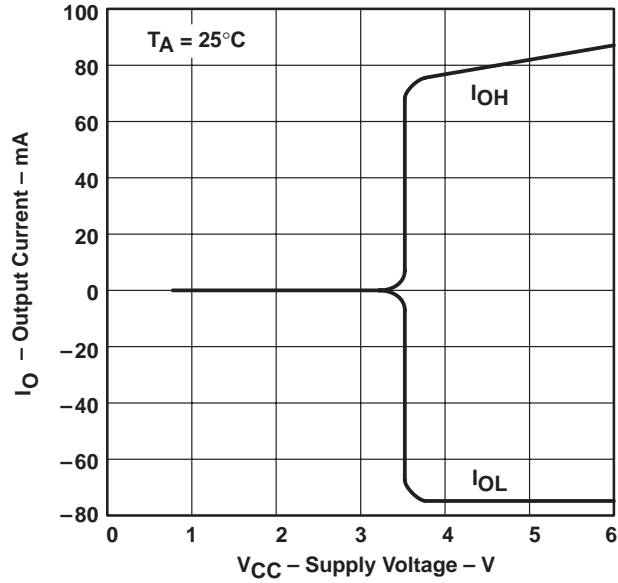


Figure 17

**APPLICATION INFORMATION**

**Table 2. Typical Signal and Terminal Assignments**

| SIGNAL                      | TERMINAL | SCSI DATA    | SCSI CONTROL | IPI DATA        | IPI CONTROL     |
|-----------------------------|----------|--------------|--------------|-----------------|-----------------|
| CDE0                        | 54       | DIFFSENSE    | DIFFSENSE    | V <sub>CC</sub> | V <sub>CC</sub> |
| CDE1                        | 55       | GND          | GND          | XMTA, XMTB      | GND             |
| CDE2                        | 56       | GND          | GND          | XMTA, XMTB      | SLAVE/MASTER    |
| BSR                         | 2        | GND          | GND          | GND, BSR        | GND             |
| $\overline{\text{CRE}}$     | 3        | GND          | GND          | GND             | V <sub>CC</sub> |
| 1A                          | 4        | DB0, DB8     | ATN          | AD7, BD7        | NOT USED        |
| 1DE/ $\overline{\text{RE}}$ | 5        | DBE0, DBE8   | INIT EN      | GND             | GND             |
| 2A                          | 6        | DB1, DB9     | BSY          | AD6, BD6        | NOT USED        |
| 2DE/ $\overline{\text{RE}}$ | 7        | DBE1, DBE9   | BSY EN       | GND             | GND             |
| 3A                          | 8        | DB2, DB10    | ACK          | AD5, BD5        | SYNC IN         |
| 3DE/ $\overline{\text{RE}}$ | 9        | DBE2, DBE10  | INIT EN      | GND             | GND             |
| 4A                          | 10       | DB3, DB11    | RST          | AD4, BD4        | SLAVE IN        |
| 4DE/ $\overline{\text{RE}}$ | 11       | DBE3, DBE11  | GND          | GND             | GND             |
| 5A                          | 19       | DB4, DB12    | MSG          | AD3, BD3        | NOT USED        |
| 5DE/ $\overline{\text{RE}}$ | 20       | DBE4, DBE12  | TARG EN      | GND             | GND             |
| 6A                          | 21       | DB5, DB13    | SEL          | AD2, BD2        | SYNC OUT        |
| 6DE/ $\overline{\text{RE}}$ | 22       | DBE5, DBE13  | SEL EN       | GND             | GND             |
| 7A                          | 23       | DB6, DB14    | C/D          | AD1, BD1        | MASTER OUT      |
| 7DE/ $\overline{\text{RE}}$ | 24       | DBE6, DBE14  | TARG EN      | GND             | GND             |
| 8A                          | 25       | DB7, DB15    | REQ          | AD0, BD0        | SELECT OUT      |
| 8DE/ $\overline{\text{RE}}$ | 26       | DBE7, DBE15  | TARG EN      | GND             | GND             |
| 9A                          | 27       | DBP0, DBP1   | I/O          | AP, BP          | ATTENTION IN    |
| 9DE/ $\overline{\text{RE}}$ | 28       | DBPE0, DBPE1 | TARG EN      | XMTA, XMTB      | V <sub>CC</sub> |

ABBREVIATIONS:

- DB<sub>n</sub> = data bit n, where n = (0,1, . . . ,15)
- DBE<sub>n</sub> = data bit n enable, where n = (0,1, . . . ,15)
- DBP0 = parity bit for data bits 0 through 7 or IPI bus A
- DBPE0 = parity bit enable for P0
- DBP1 = parity bit for data bits 8 through 15 or IPI bus B
- DBPE1 = parity bit enable for P1
- AD<sub>n</sub> or BD<sub>n</sub> = IPI Bus A – Bit n (AD<sub>n</sub>) or Bus B – Bit n (BD<sub>n</sub>), where n = (0,1, . . . ,7)
- AP or BP = IPI parity bit for bus A or bus B
- XMTA or XMTB = transmit enable for IPI bus A or B
- BSR = bit significant response
- INIT EN = common enable for SCSI initiator mode
- TARG EN = common enable for SCSI target mode

NOTE A: Signal inputs are shown as active high. When only active-low inputs are available, logic inversion is accomplished by reversing the B+ and B– connector terminal assignments.

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## APPLICATION INFORMATION

### Function Tables

RECEIVER



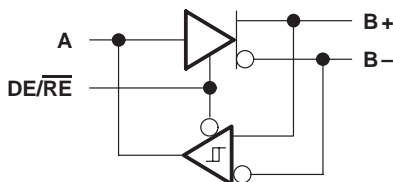
| INPUTS |     | OUTPUT<br>A |
|--------|-----|-------------|
| B+†    | B-† |             |
| L      | H   | L           |
| H      | L   | H           |

DRIVER



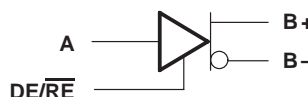
| INPUT<br>A | OUTPUTS |    |
|------------|---------|----|
|            | B+      | B- |
| L          | L       | H  |
| H          | H       | L  |

TRANSCIEVER



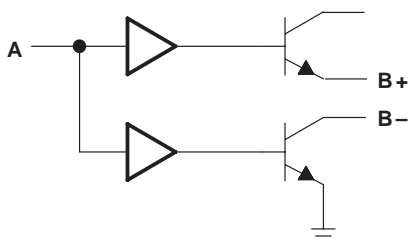
| DE/RE | INPUTS |     |     | OUTPUTS |    |    |
|-------|--------|-----|-----|---------|----|----|
|       | A      | B+† | B-† | A       | B+ | B- |
| L     | -      | L   | H   | L       | -  | -  |
| L     | -      | H   | L   | H       | -  | -  |
| H     | L      | -   | -   | -       | L  | H  |
| H     | H      | -   | -   | -       | H  | L  |

DRIVER WITH ENABLE



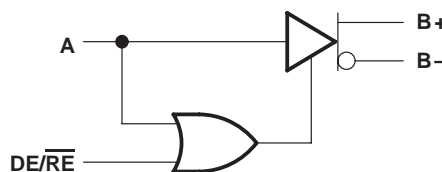
| DE/RE | A | OUTPUTS |    |
|-------|---|---------|----|
|       |   | B+      | B- |
| L     | L | Z       | Z  |
| L     | H | Z       | Z  |
| H     | L | L       | H  |
| H     | H | H       | L  |

WIRED-OR DRIVER



| INPUT<br>A | OUTPUTS |    |
|------------|---------|----|
|            | B+      | B- |
| L          | Z       | Z  |
| H          | H       | L  |

TWO-ENABLE INPUT DRIVER

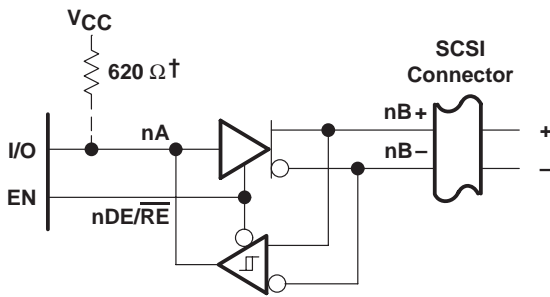


| DE/RE | A | OUTPUTS |    |
|-------|---|---------|----|
|       |   | B+      | B- |
| L     | L | Z       | Z  |
| L     | H | H       | L  |
| H     | L | L       | H  |
| H     | H | H       | L  |

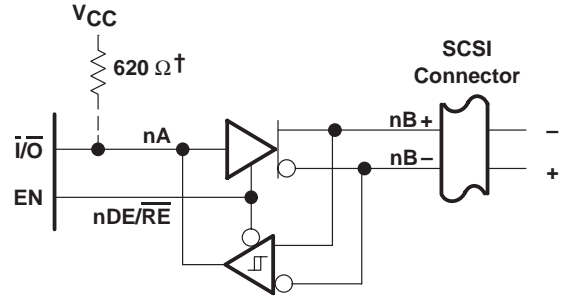
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

† An H in this column represents a voltage of 200 mV or higher than the other bus input. An L represents a voltage of 200 mV or lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

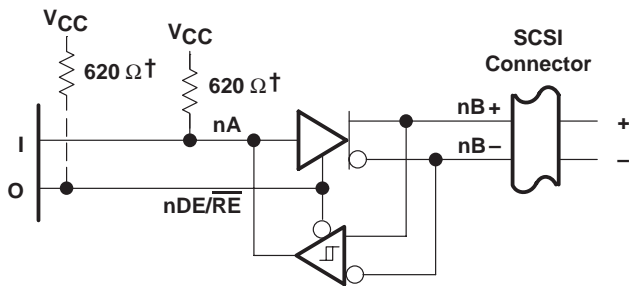
APPLICATION INFORMATION



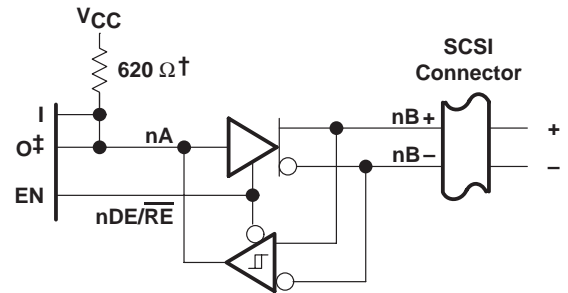
(a) ACTIVE-HIGH BIDIRECTIONAL I/O WITH SEPARATE ENABLE



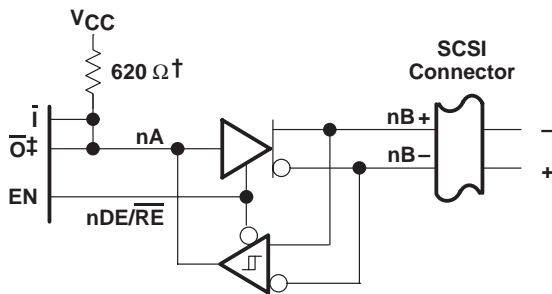
(b) ACTIVE-LOW BIDIRECTIONAL I/O WITH SEPARATE ENABLE



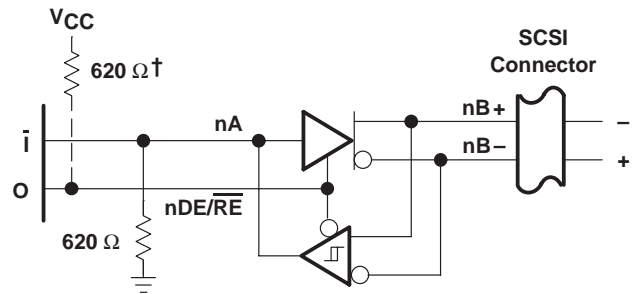
(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT



(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT, AND ENABLE



(e) SEPARATE ACTIVE-LOW INPUT AND OUTPUT AND ACTIVE-HIGH ENABLE



(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

† When 0 is open drain

‡ Must be open-drain or 3-state output

NOTE A: The BSR, CRE, A, and DE/RE inputs have internal pullup resistors. CDE0, CDE1, and CDE2 have internal pulldown resistors.

Figure 18. Typical SCSI Transceiver Connections

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## APPLICATION INFORMATION

### channel logic configurations with control input logic

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; the BSR, CDE0, CDE1, CDE2, and CRE bit values are shown below the diagrams. Channel 1 is at the top of the logic diagrams; channel 9 is at the bottom of the logic diagrams.

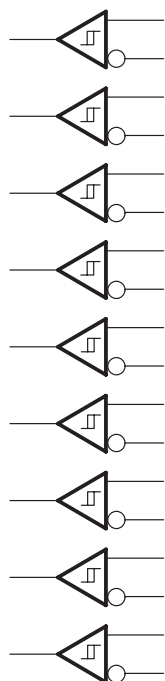


Figure 19. 00000

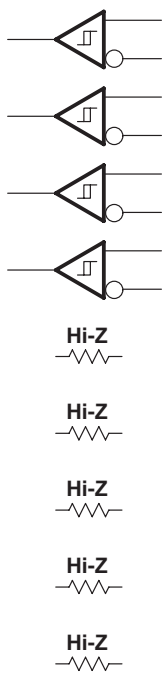


Figure 20. 00001

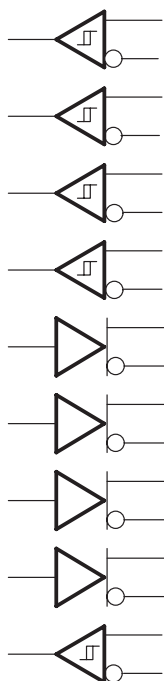


Figure 21. 00010

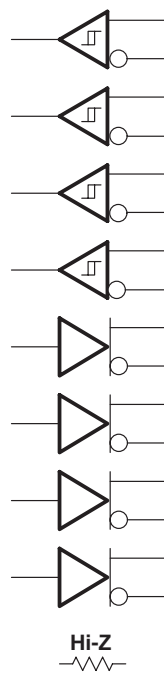


Figure 22. 00011

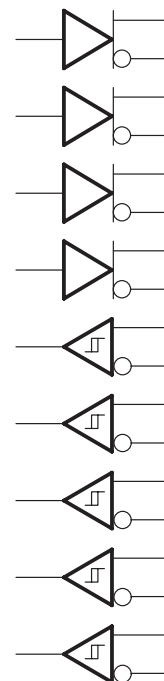


Figure 23. 00100

APPLICATION INFORMATION

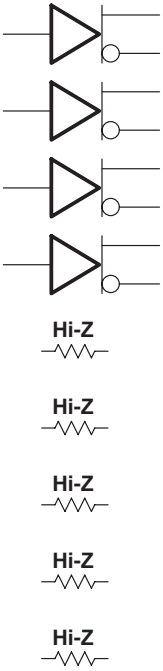


Figure 24. 00101

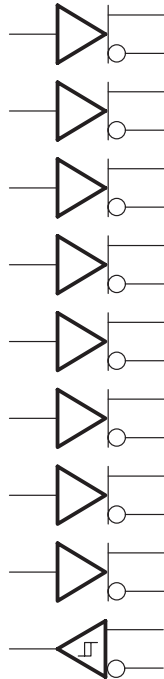


Figure 25. 00110

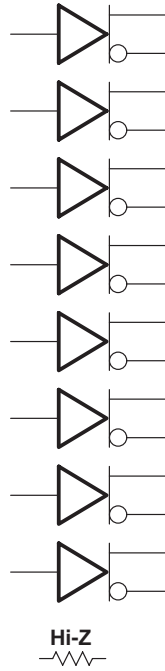


Figure 26. 00111

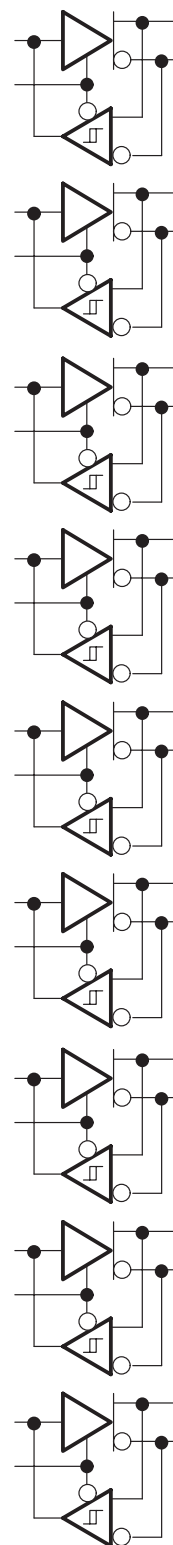


Figure 27. 01000

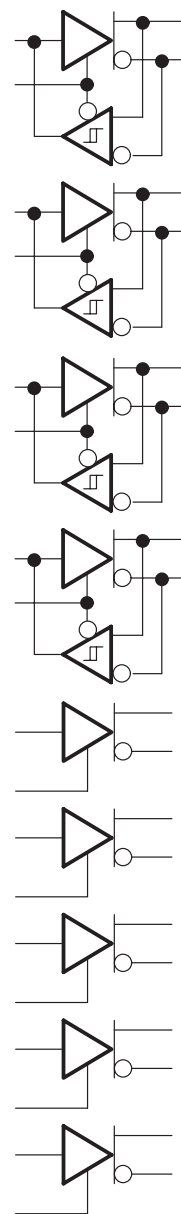


Figure 28. 01001

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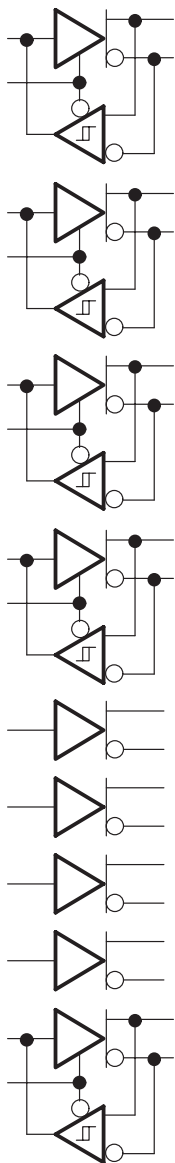


Figure 29. 01010

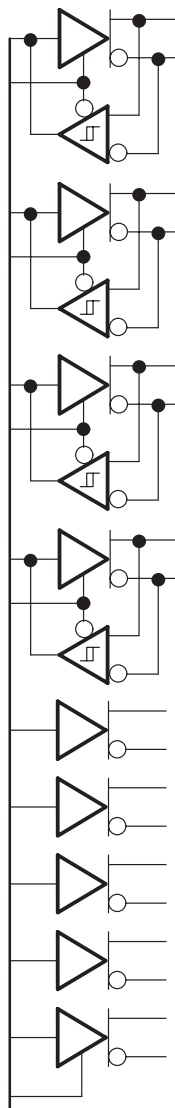


Figure 30. 01011

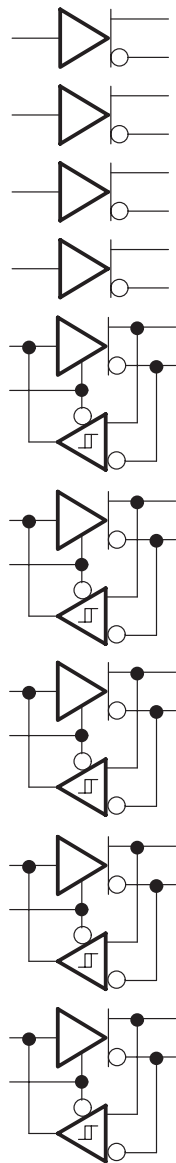


Figure 31. 01100

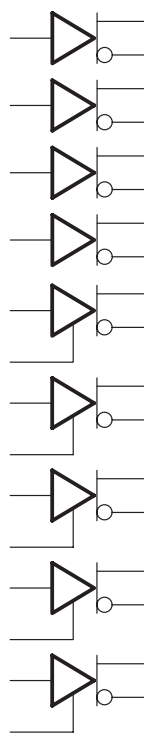


Figure 32. 01101

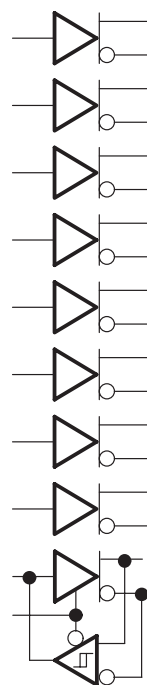


Figure 33. 01110

APPLICATION INFORMATION

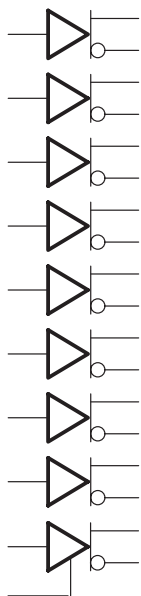


Figure 34. 01111



Figure 35. 10000 and 10001

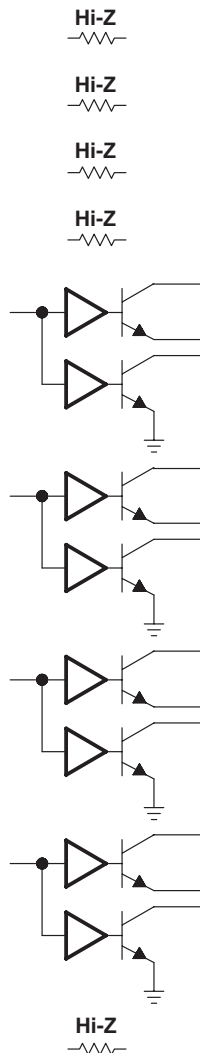


Figure 36. 10010 and 10011

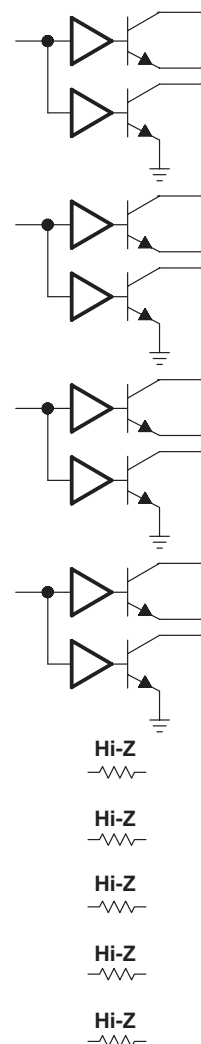


Figure 37. 10100 and 10101

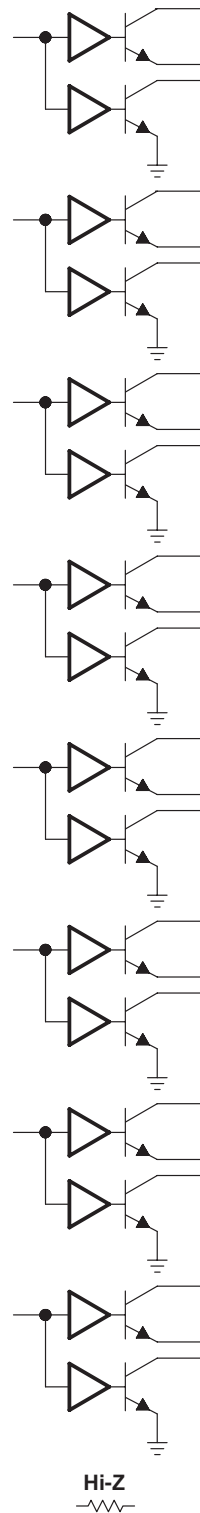


Figure 38. 10110 and 10111

# SN75976A, SN55976A 9-CHANNEL DIFFERENTIAL TRANSCIEVER

SLLS218B – MAY 1995 – REVISED MAY 1997

## APPLICATION INFORMATION

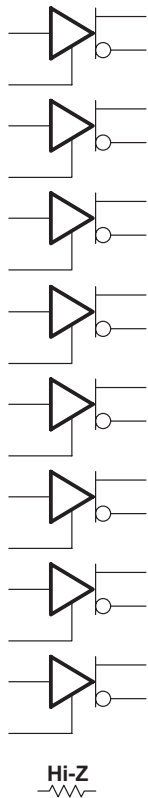


Figure 39. 11000 and 11001

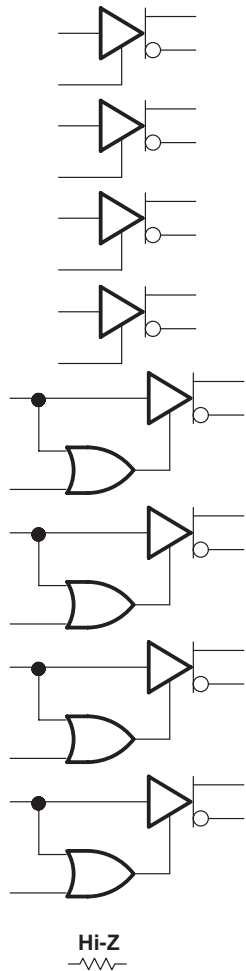


Figure 40. 11010 and 11011

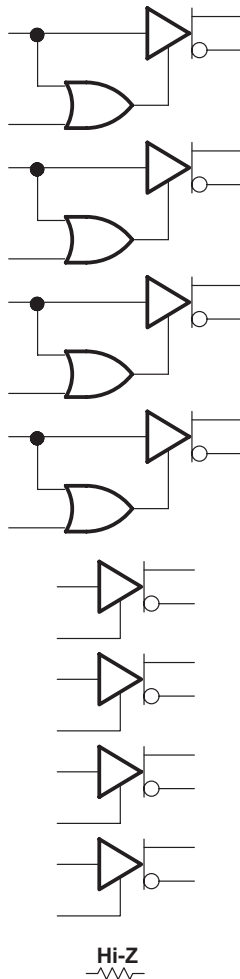


Figure 41. 11100 and 11101

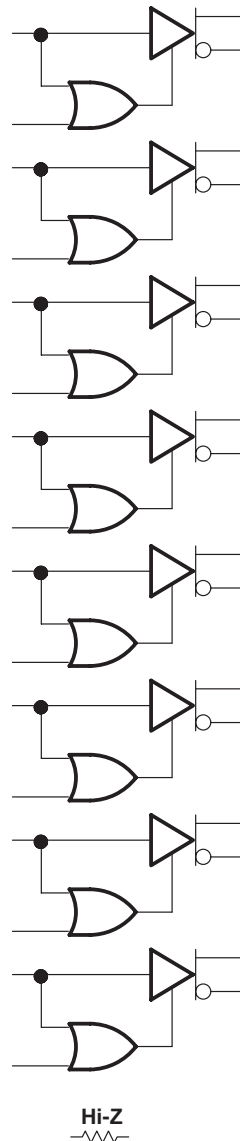


Figure 42. 11110 and 11111

# SN75976A, SN55976A 9-CHANNEL DIFFERENTIAL TRANSCIEVER

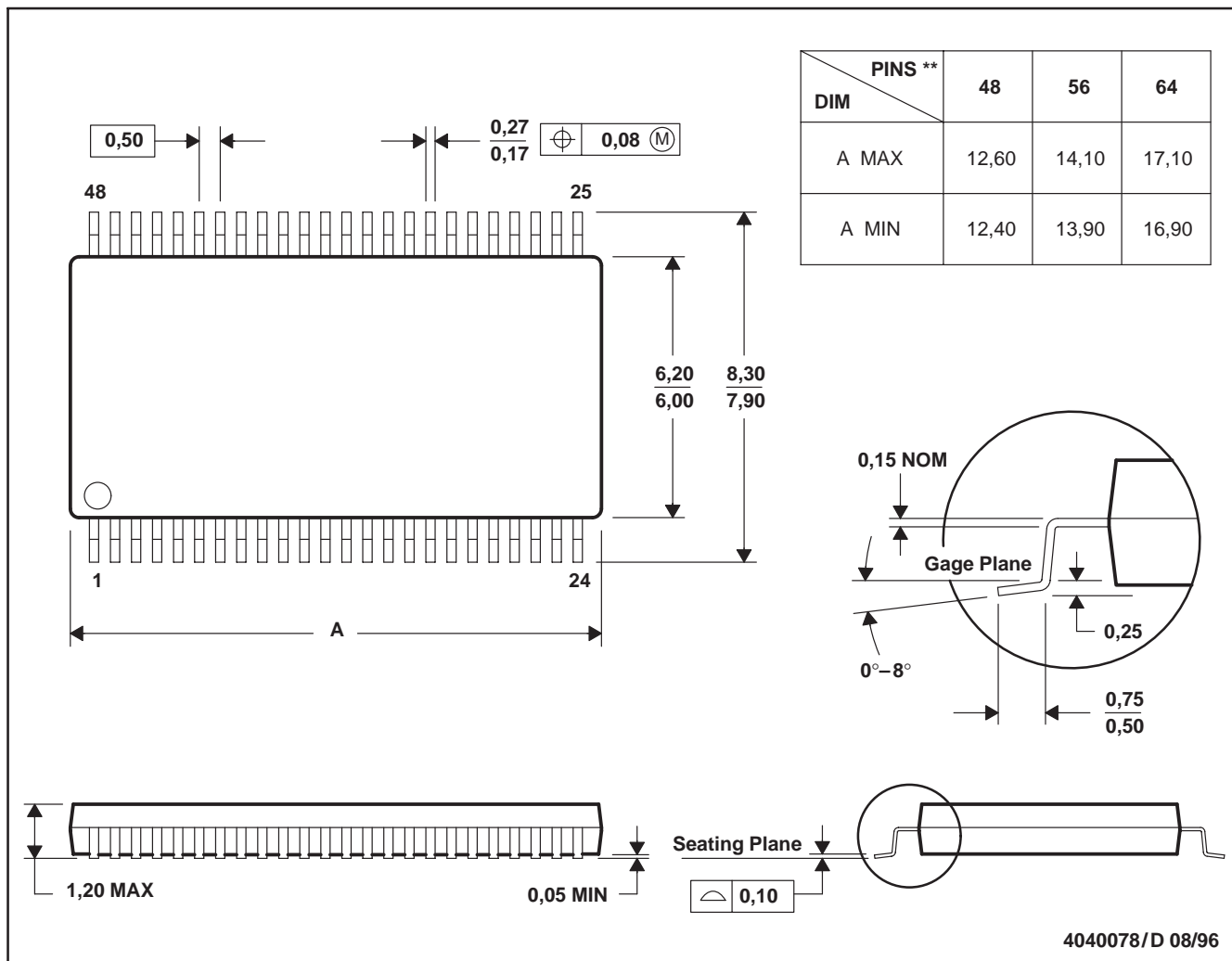
SLLS218B – MAY 1995 – REVISED MAY 1997

## MECHANICAL INFORMATION

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES: B. All linear dimensions are in millimeters.  
 C. This drawing is subject to change without notice.  
 D. Falls within JEDEC MO-153

# SN75976A, SN55976A 9-CHANNEL DIFFERENTIAL TRANSCEIVER

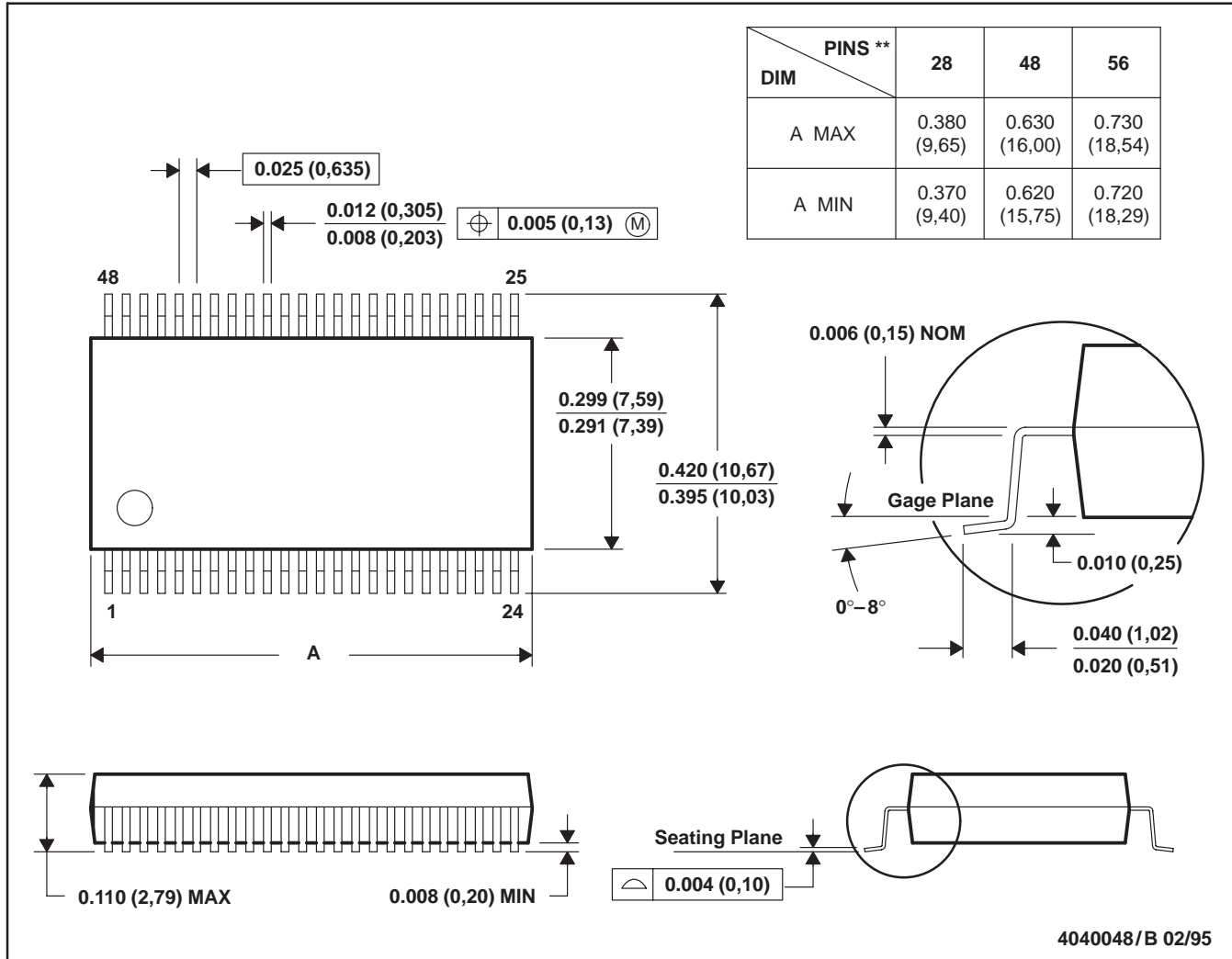
SLLS218B – MAY 1995 – REVISED MAY 1997

## MECHANICAL INFORMATION

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

# SN75976A, SN55976A 9-CHANNEL DIFFERENTIAL TRANSCEIVER

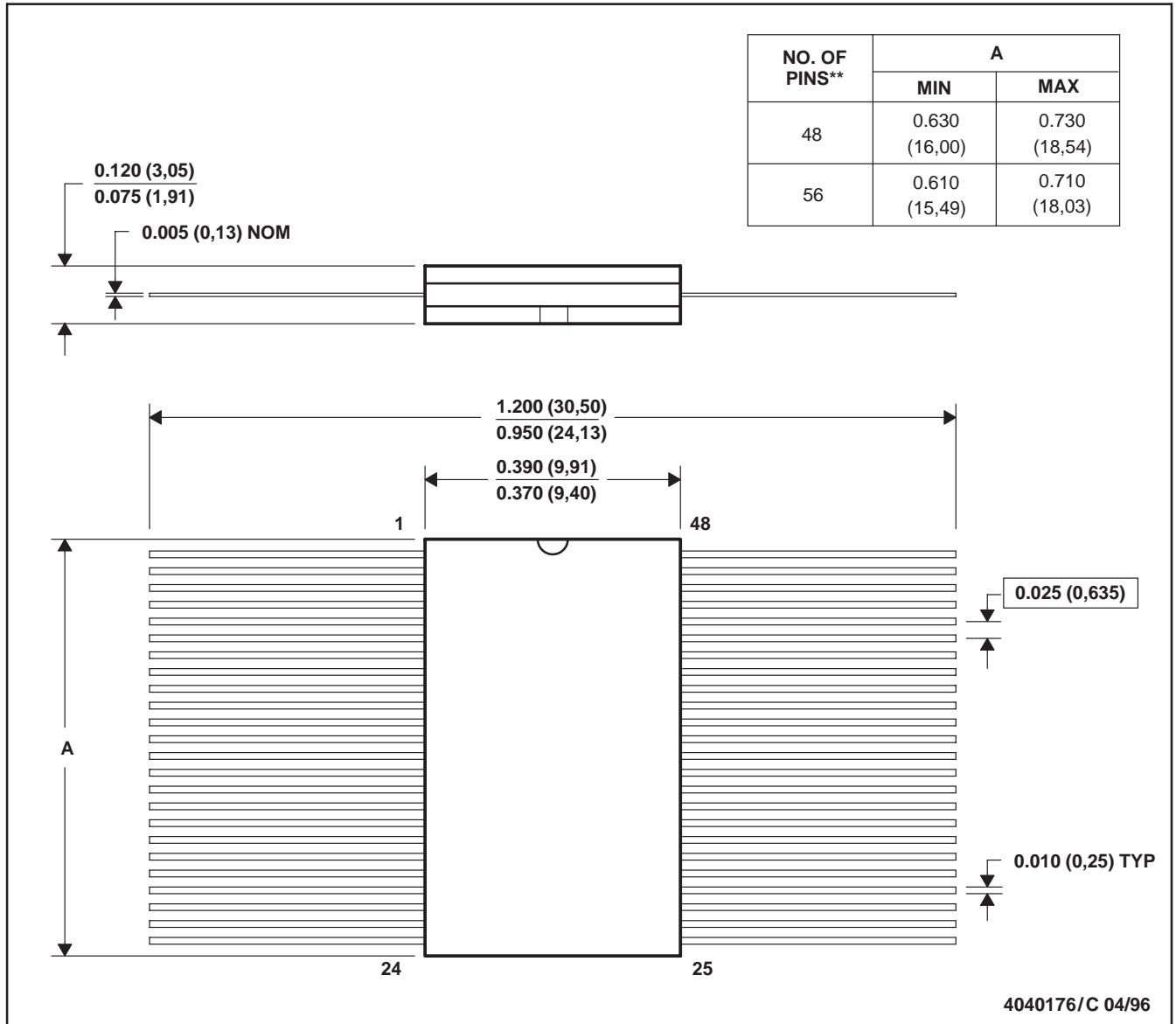
SLLS218B – MAY 1995 – REVISED MAY 1997

## MECHANICAL INFORMATION

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 PIN SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for pin identification only
  - Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA  
GDFP1-F56 and JEDEC MO-146AB

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)             | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| 5962-9689301QXA  | ACTIVE        | CFP          | WD              | 56   | 1           | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9689301QX<br>A<br>SNJ55976A1WD | <a href="#">Samples</a> |
| SN55976A1WD      | ACTIVE        | CFP          | WD              | 56   | 1           | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | SN55976A1WD                         | <a href="#">Samples</a> |
| SN75976A1DGG     | ACTIVE        | TSSOP        | DGG             | 56   | 35          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  |              | SN75976A1                           | <a href="#">Samples</a> |
| SN75976A1DL      | ACTIVE        | SSOP         | DL              | 56   | 20          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  |              | SN75976A1                           | <a href="#">Samples</a> |
| SN75976A1DLG4    | ACTIVE        | SSOP         | DL              | 56   | 20          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  |              | SN75976A1                           | <a href="#">Samples</a> |
| SN75976A1DLR     | ACTIVE        | SSOP         | DL              | 56   | 1000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  |              | SN75976A1                           | <a href="#">Samples</a> |
| SN75976A2DGG     | ACTIVE        | TSSOP        | DGG             | 56   | 35          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | SN75976A2                           | <a href="#">Samples</a> |
| SN75976A2DGGG4   | ACTIVE        | TSSOP        | DGG             | 56   | 35          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | SN75976A2                           | <a href="#">Samples</a> |
| SN75976A2DGGR    | ACTIVE        | TSSOP        | DGG             | 56   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  |              | SN75976A2                           | <a href="#">Samples</a> |
| SN75976A2DL      | ACTIVE        | SSOP         | DL              | 56   | 20          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  |              | SN75976A2                           | <a href="#">Samples</a> |
| SN75976A2DLR     | ACTIVE        | SSOP         | DL              | 56   | 1000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  |              | SN75976A2                           | <a href="#">Samples</a> |
| SNJ55976A1WD     | ACTIVE        | CFP          | WD              | 56   | 1           | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9689301QX<br>A<br>SNJ55976A1WD | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN55976A, SN75976A :**

- Catalog: [SN75976A](#)
- Enhanced Product: [SN75976A-EP](#), [SN75976A-EP](#)
- Military: [SN55976A](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75976A1DLR  | SSOP         | DL              | 56   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |
| SN75976A2DGGR | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| SN75976A2DLR  | SSOP         | DL              | 56   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**

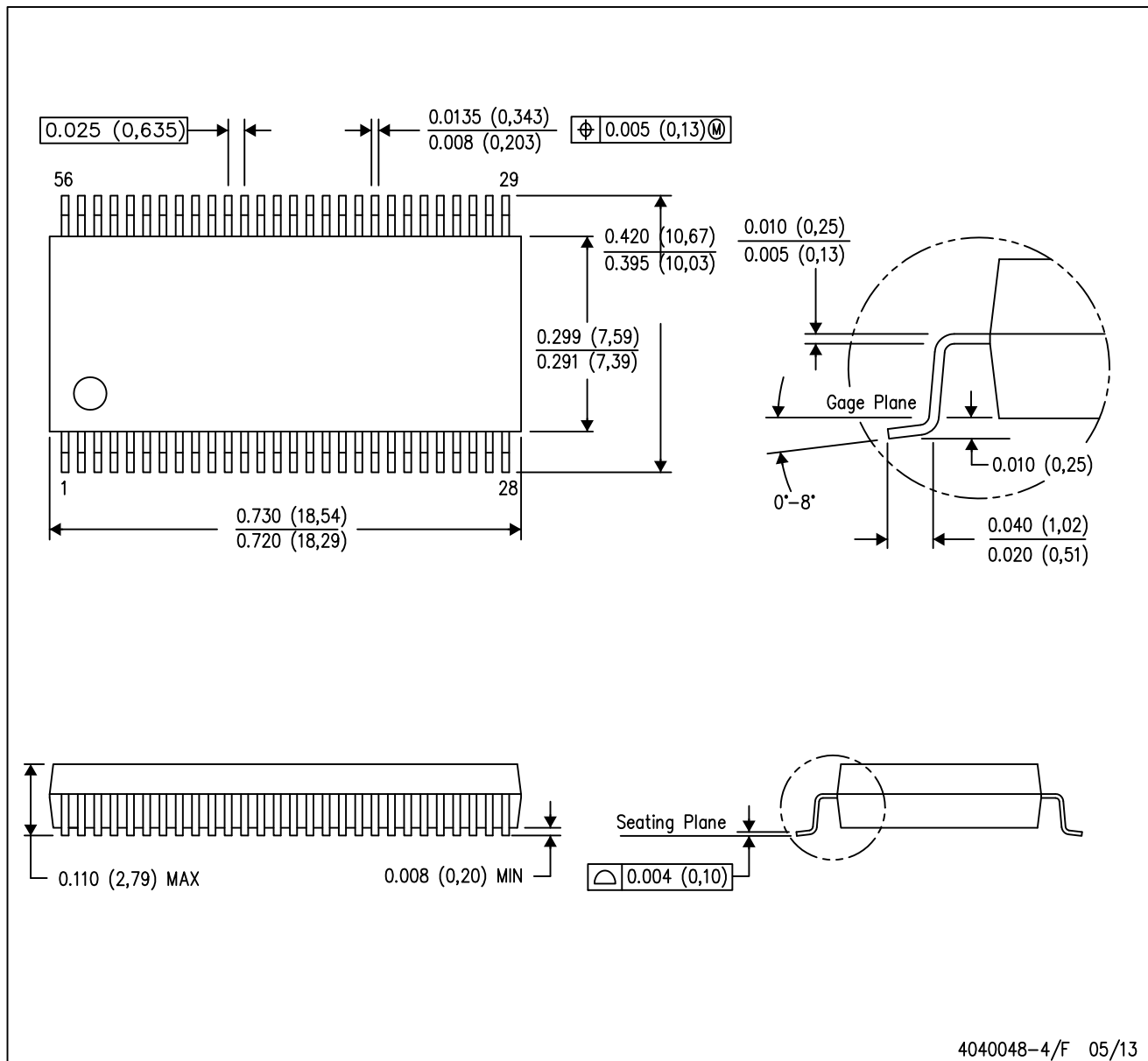

\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75976A1DLR  | SSOP         | DL              | 56   | 1000 | 367.0       | 367.0      | 55.0        |
| SN75976A2DGGR | TSSOP        | DGG             | 56   | 2000 | 367.0       | 367.0      | 45.0        |
| SN75976A2DLR  | SSOP         | DL              | 56   | 1000 | 367.0       | 367.0      | 55.0        |

# MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

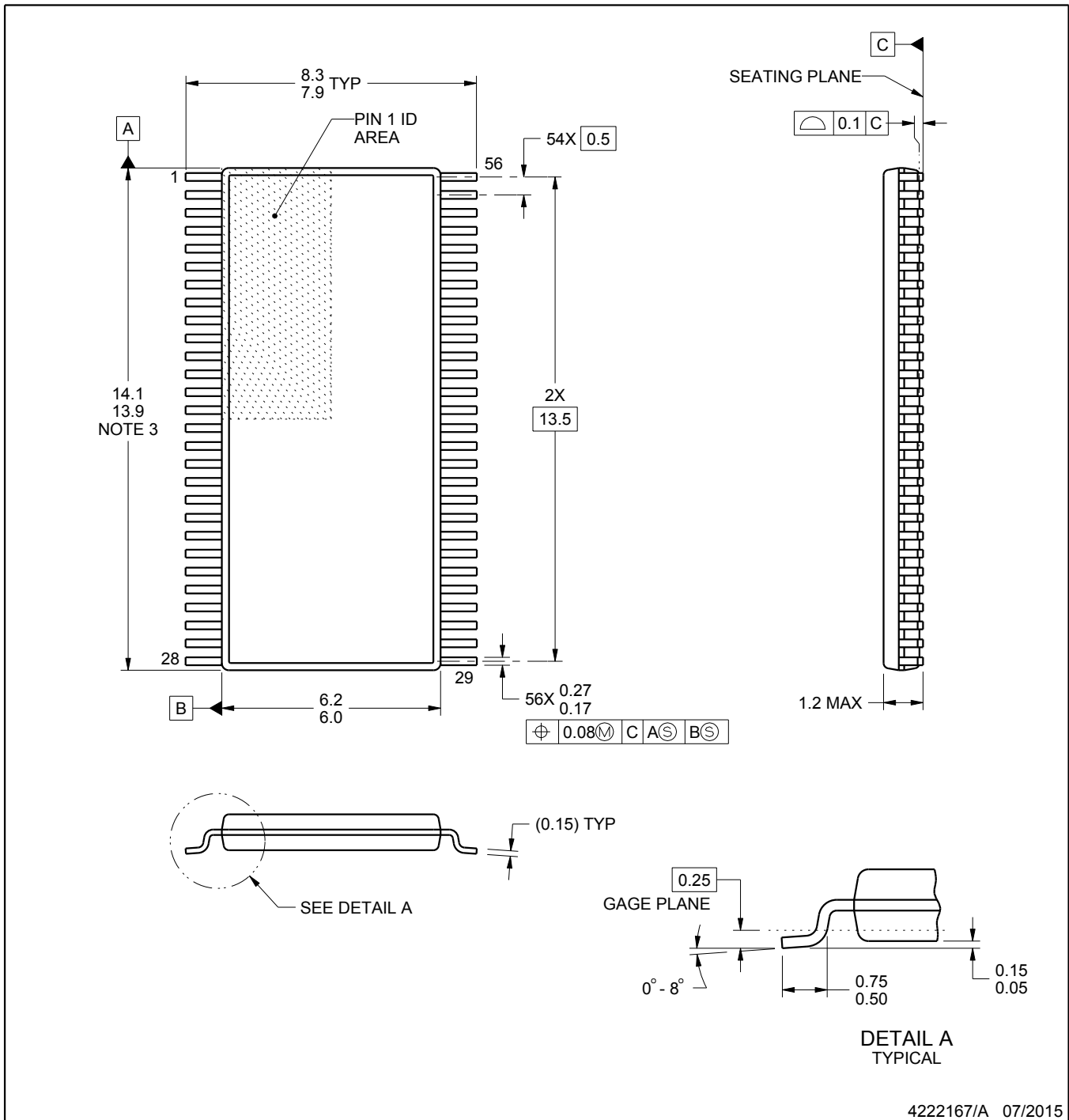
# DGG0056A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

### NOTES:

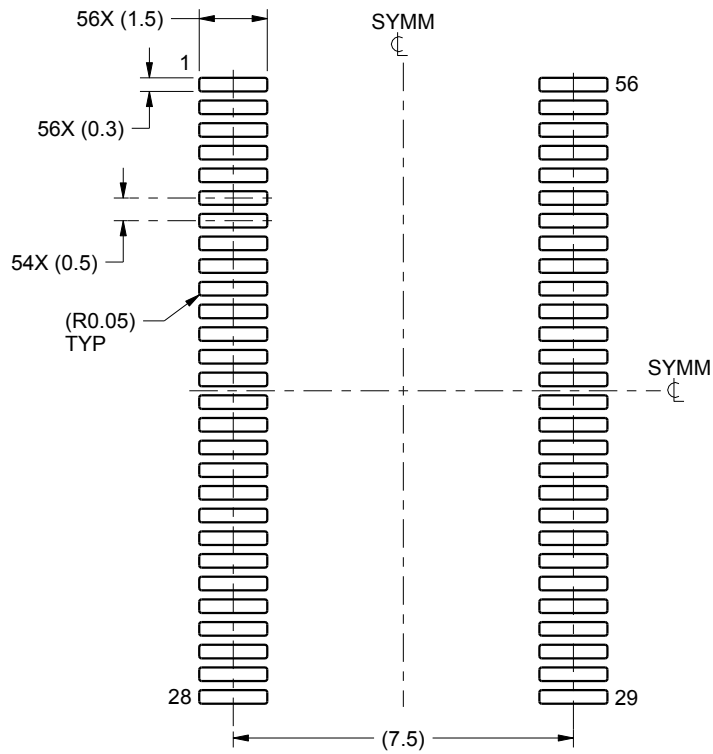
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

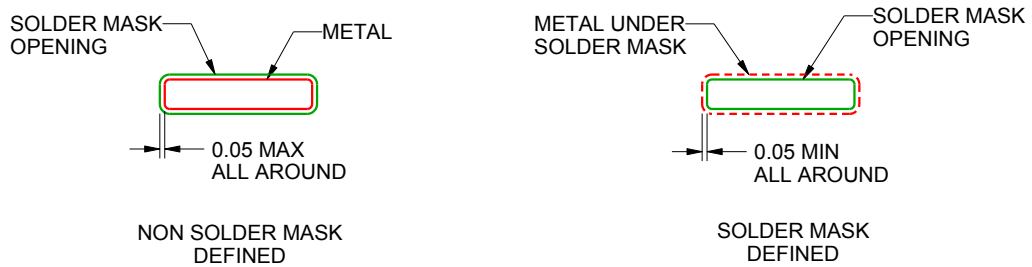
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

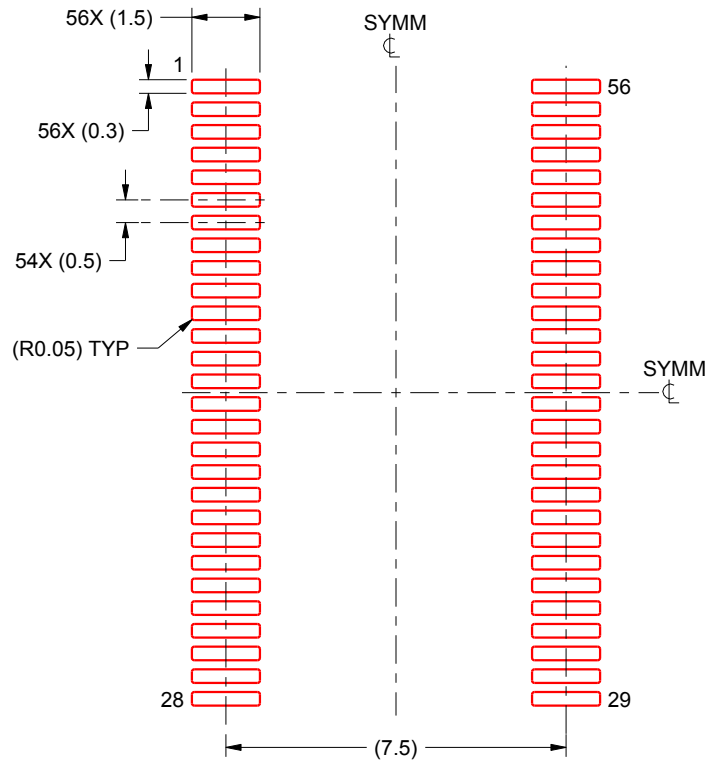
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

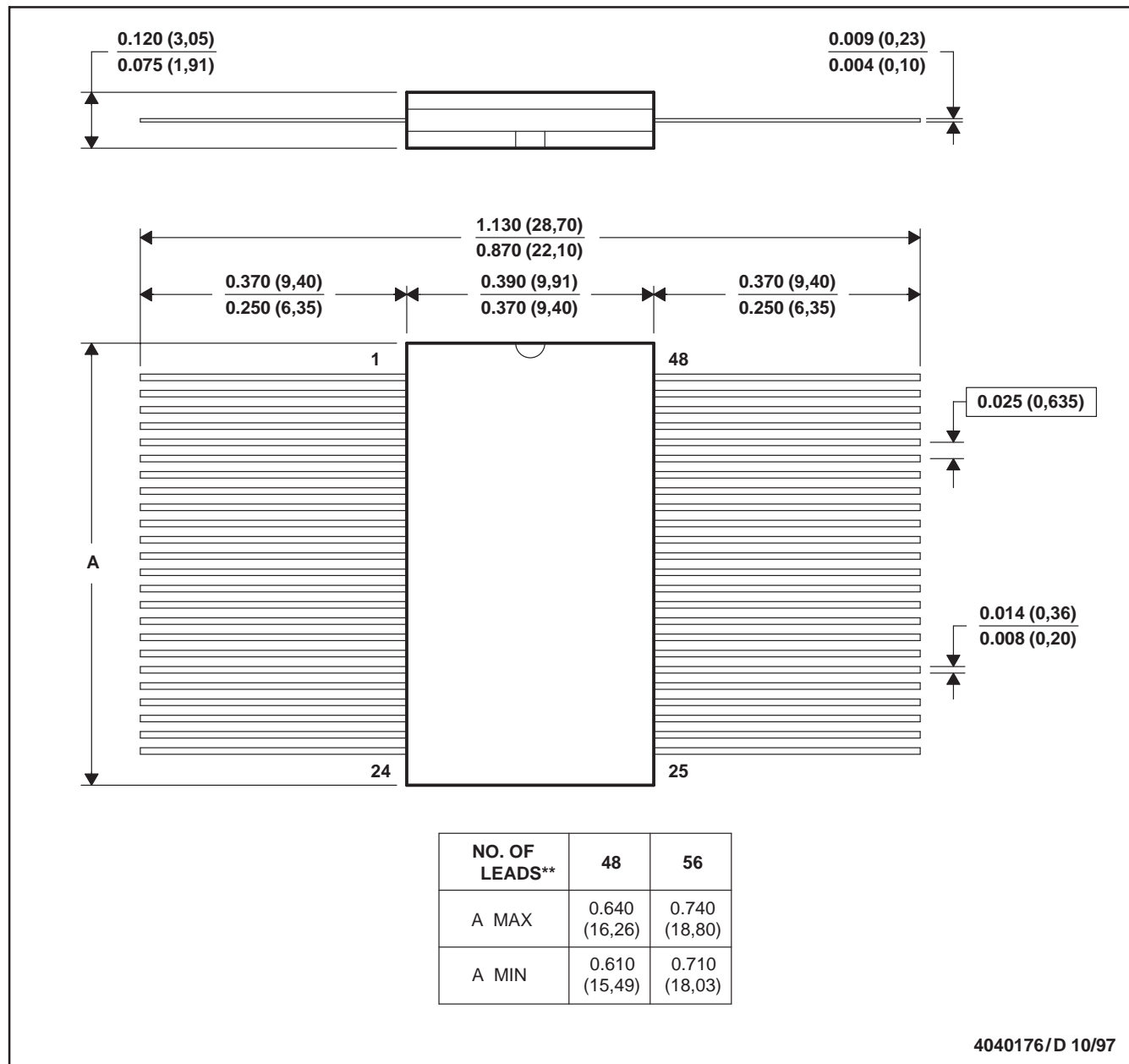
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

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