THE DATASHEET OF

UCC3882PWTR-1G4

AVERAGE CURRENT MODE SYNCHRONOUS CONTROLLER WITH 5-BIT DAC

Check for Samples: UCC3882/-1

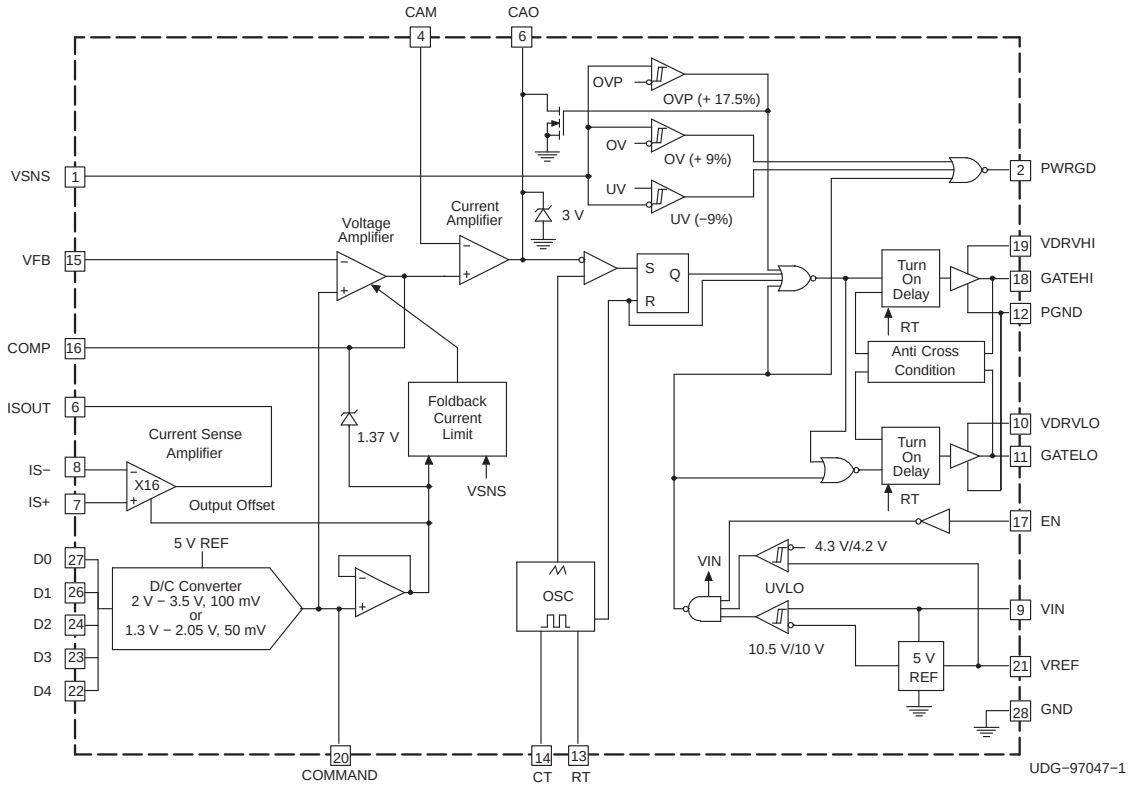
FEATURES

- **Combined DAC/Voltage Monitor and PWM With Synchronous Rectification Functions**
- **5-Bit Digital-to-Analog (DAC) Converter**
- **1% DAC/Reference Combined Accuracy**
- **Compatible with 5 V and 12 V Systems and 12 V-Only Systems**
- **Low Offset Current Sense Amplifier**
- **Programmable Oscillator Frequency Practical to 700 kHz**
- **Foldback Current Limiting**
- **Overvoltage and Undervoltage Fault Windows**
- **2-Ω Totem Pole Outputs with Programmable Dead Times to Eliminate Cross-Conduction**
- **Chip Disable Function**

DESCRIPTION

The UCC3882 combines high precision reference and voltage monitoring circuitry with average current mode PWM synchronous rectification controller circuitry to power high-end microprocessors with a minimum of external components. The UCC3882 converts 5 V or 12 V to an adjustable output ranging from 1.8VDC to 2.05VDC in 50 mV steps and 2.1VDC to 3.5VDC in 100 mV steps with 1% DC system accuracy.

BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The DAC output voltage is directly compatible with Intel's 5-bit VID code (Table 1) which covers 1.3 V to 2.05 V in 50 mV steps and 2.1 V to 3.5 V in 100 mV steps. The accuracy of the DAC/reference combination is better than 1%. Undervoltage lockout circuitry assures the correct logic states at the outputs during power up and power down. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its designed value by more than 9%. A second overvoltage comparator digitally forces GATEHI off and GATELO on when the system output voltage exceeds its designed value by more than 17.5%.

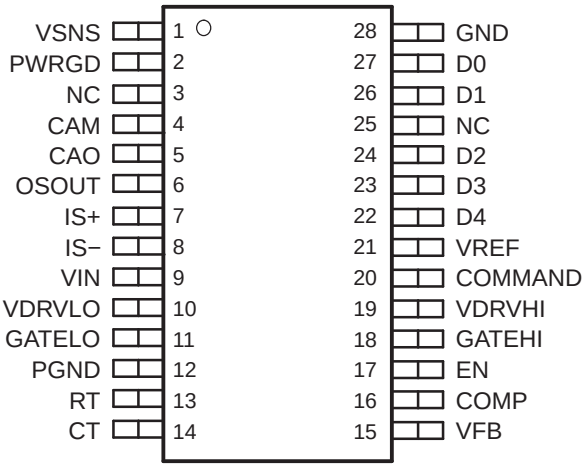
For all of the parts, grounding the EN pin disables the GATEHI and GATELO outputs, shutting down the power supply. For the 3882, programming a DAC output voltage below 1.8 V, or programming all of the VID pins high also disables the GATEHI and GATELO outputs. For the –1 option parts, the GATEHI and GATELO outputs are switching, and the power supply output voltage regulates at the programmed DAC output voltage for all VID codes.

The voltage and current amplifiers have 2.5 MHz gain-bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is externally programmed with RT and CT. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short-circuited, minimizing component stress and dissipation during abnormal conditions. The gate drivers are low impedance totem pole output stages capable of driving large external MOSFETs. Cross conduction is eliminated internally by programming the dead time between turn-off and turn on of the external high side and synchronous MOSFETs.

This device is available in a 28-pin wide body surface mount package. The UCC3882 is specified for operation from 0°C to 70°C.

CONNECTION DIAGRAM

N, DW or PW PACKAGES
(TOP VIEW)



NC − No internal connection

ABSOLUTE MAXIMUM RATINGS(1)

	UNIT
VDRVHI, GATEHI(2)	–0.3 V to 20 V
VDRVLO, GATELO	–0.3 V to 15 V
All other pins referenced to GND	–0.3 V to 5.3 V
VIN	15 V
Storage Temperature	–65°C to 150°C
Junction Temperatur	–55°C to 150°C.
Lead Temperature (Soldering, 10 sec.)	300°C

(1) Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.
(2) 20 V at no load. Derate to 18.5 V when used with capacitive loads of greater than 1000 pF in series with less than 20 Ω.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VIN = VDRVHI = VDRVLO = 12 V, VSNS = 3.5 V, $V_{D0} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = 0$ V, $R_T = 13$ k, $C_T = 1.8$ nF, EN = Open, 0°C < T_A < 70°C, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis		300	500	700	mV
SUPPLY CURRENT					
I_{IN}	EN = 0 V		7	12	mA
DAC/REFERENCE					
COMMAND Voltage Accuracy	10.8 V < VIN < 13.2 V, I_{REF} = 0 mA(1)	–1%		1%	
D0-D4 Voltage High	DX Pin Floating		5	5.2	V
D0-D4 Input Bias Current	DX Pin Tied to GND	–120	–70	–20	μA
OVP COMPARATOR					
Trip Point	% Over COMMAND Voltage(2)	10	17	25	μV
Hysteresis			20		mV
OV COMPARATOR					
Trip Point	% Over COMMAND Voltage(2)	5%	9%	12%	
Hysteresis			20		mV
PWRGD On Resistance				470	Ω
UV COMPARATOR					
Trip Point	% Over COMMAND Voltage(2)	–12%	–9%	–5%	
Hysteresis			20		mV
ENABLE PIN					
Pull Up Current	V_{EN} = 2.5 V	–80	–50	–20	μA

(1) This test measures the combined errors of the COMMAND voltage and the voltage amplifier offset voltage. Applies to all DAC codes from 1.8 V to 3.5 V.
(2) This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0–D4 pins.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, VIN = VDRVHI = VDRVLO = 12 V, VSNS = 3.5 V, $V_{D0} = V_{D1} = V_{D2} = V_{D3} = V_{D4}$ = 0 V, R_T = 13 k, C_T = 1.8 nF, EN = Open, 0°C < T_A < 70°C, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE ERROR AMPLIFIER					
Input Offset Voltage	V_{CM} = 3 V	–10	0	10	mV
Input Bias Current	V_{CM} = 3 V	–0.5		0.5	µA
Open Loop Gain	2.05 V < V_{COMP} < 3.05 V		90		dB
Power Supply Rejection Ratio	10.8 V < VIN < 15 V		85		dB
Output Sourcing Current	V_{VFB} = 2 V, $V_{COMMAND} = V_{COMP}$ = 2.5 V		–1.6	–0.8	mA
Output Sinking Current	V_{VFB} = 3 V, $V_{COMMAND} = V_{COMP}$ = 2.5 V		1		mA
CURRENT SENSE AMPLIFIER					
Gain		15	16	17	V/V
Common Mode Rejection Ratio	0 V < V_{CM} < 4.5 V		60		dB
Power Supply Rejection Ratio	10.8 V < VIN < 15 V		80		dB
Output Sourcing Current	$V_{IS–}$ = 2 V, $V_{ISOUT} = V_{IS+}$ = 2.5 V		–4	–3	mA
Output Sinking Current	$V_{IS–}$ = 3 V, $V_{ISOUT} = V_{IS+}$ = 2.5 V	3	4		Ma
CURRENT AMPLIFIER					
Input Offset Voltage	V_{CM} = 3 V		1		mV
Input Bias Current	V_{CM} = 3 V		–0.1		µA
Open Loop Gain	1 V < V_{CAO} < 2.5 V		90		dB
Output Voltage High			3		V
Power Supply Rejection Ratio	10.8 V < VIN < 15 V		80		dB
Output Sourcing Current	V_{CAM} = 2 V, $V_{CAO} = V_{COMP}$ = 2.5 V		–7		mA
Output Sinking Current	V_{CAM} = 3 V, $V_{CAO} = V_{COMP}$ = 2.5 V		17		Ma
OSCILLATOR					
Initial Accuracy	T_A = 25°C	324	360	396	kHz
	0°C < T_A < 70°C	300	360	420	kHz
Valley to Peak Voltage			1.67		V
Frequency Change With Voltage	10.8 V < VIN < 15 V		1%		
OUTPUT SECTION (GATEHI AND GATELO)					
Output Low Voltage	I_{GATE} = –100 mA		0.2		V
Output High Voltage	I_{GATE} = 100 mA		11.8		V
Rise Time	C_{GATE} = 3.3 nF, R_{SERIES} = 10 Ω		20	80	ns
Fall Time	C_{GATE} = 3.3 nF, R_{SERIES} = 10 Ω		15	80	ns
TURN ON DALAY					
GATEHI Turn Off to GATELO Turn On			150		ns
GATELO Turn Off to GATEHI Turn On			135		ns
FOLDBACK CURRENT LIMIT					
Clamp Level	$V_{COMMAND} = V_{SNS}$, $V_{FB} = V_{COMMAND}$ – 100mV (3)		1.37		V
	$V_{COMMAND}$ = 0, $V_{FB} = V_{COMMAND}$ – 100mV (3)		0.71		
System Short Circuit Current Limit	$V_{COMMAND}$ = 2.3 V, V_{FB} = 0 V (4)	14.4	17	22	A

(3) This voltage is measured with respect to the COMMAND voltage.
(4) The calculation of this parameter assumes an offchip sense resistor value of 0.005 Ω . This test encompasses all sources of error from the IC.

PIN DESCRIPTIONS

CAM: This pin is the inverting input to the current amplifier. The average load current feedback from the ISOUT pin is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO).

CAO: This pin is the current amplifier output. The current loop compensation network is connected between this pin and the CAM pin. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The voltage at this output ranges from below 0.5 V (forcing 0% duty cycle) to above 2.5 V forcing maximum duty cycle. A 3 V clamp circuit prevents the CAO voltage from rising excessively past the oscillator peak voltage, for excellent transient response.

COMP: This pin is the voltage error amplifier output voltage. The system voltage compensation network is applied between COMP and VFB. A 1.37 V clamp above COMMAND is used to force the power supply into current limit mode when the output is short circuited. See the Applications Section for programming current limit.

COMMAND: This pin is the output of the 5-bit digital-to-analog (DAC) converter and is the non-inverting input of the voltage error amplifier. The voltage on this pin sets the switching regulator output voltage. The COMMAND voltage is set by the DAC input pins D0-D4, according to Table 1. The COMMAND source impedance typically 1.2 kΩ and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01 μF, low ESR, low ESL capacitor for best circuit noise immunity.

CT: This pin is used with RT to program the internal PWM oscillator frequency. Use a high quality capacitor for best oscillator accuracy. See the Applications Section for programming the oscillator.a

D0-D4: These are the digital input control codes for the DAC (see Table 1). The DAC is comprised of two ranges set by D4 and with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected to GND; a bit is set high by floating it, or connecting it to a 5-V source. Each control pin is pulled up to approximately 5 V by an internal pull up. A voltage of 1.5 V will be interrpreted as a zero while the voltage above 3.5 V will be interpreted as a 1.

EN: This input is used to disable the GATEHI and GATELO outputs, resulting in disabling the power supply. Pulling EN to GND causes the GATEHI and GATELO outputs to be held low, while floating the pin or pulling it up to 5V ensures normal operation. EN is pulled up to 5V internally.

GATEHI: This output provides a low impedance totem pole driver to drive the high-side external MOSFET. A series resistor between this pin and the gate of the external MOSFET is recommended to prevent gate drive ringing and overshoot. Good layout techniques should be used to prevent GATEHI from ringing more than 0.3V below PGND. The VDRVHI pin provides the power for the GATEHI pin. GATEHI is disabled during UVLO and overvoltage conditions. For the 3882, GATEHI is also disabled when the COMMAND voltage is programmed between 1.3 V and 1.75 V, or where the D0–D4 pins are all logic high levels, indicating no processor present.

GATELO: This output provides a low impedance totem pole driver to drive the low-side synchronous external MOSFET. A series resistor between this pin and the gate of the external MOSFET is recommended to prevent gate drive ringing and overshoot. Good layout techniques should be used to prevent GATELO from ringing more than 0.3 V below PGND. The VDRVLO pin provides the power for GATELO. GATELO is disabled during UVLO conditions. For the 3882, GATELO is also disabled when the COMMAND voltage is programmed between 1.3 V and 1.75 V, or where the D0–D4 pins are all logic high levels, indicating no processor present.

GND: Ground reference for the device. All voltages, with the exception of the GATE voltages, are measured with respect to GND. Bypass capacitors on VIN, VREF, VSNS and COMMAND should be connected directly to the ground plane near GND.

IS–: This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+: This pin is the non-inverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT: This pin is the output of the current sense amplifier. The voltage on this pin is equal to the voltage across the sense resistor multiplied by 16 and biased up by the COMMAND voltage. This voltage is used for Average Current mode control and for current limiting.

PGND: This pin provides a dedicated ground for the output gate drivers. The GND and PGND pins should be connected externally using a short PC board trace or plane. Decouple VDRVHI and VDRVLO to PGND with low ESR capacitor of at least 0.1 μF.

PWRGD: This pin is an open drain output which is driven low to reset the microprocessor when VSNS rises above or falls below its nominal value by 9%. The on resistance of the open-drain switch will be no higher than 470 Ω. This output should be pulled up to a logic level voltage and should be programmed to sink 1 mA or less.

RT: This pin is used with CT to program the internal PWM oscillator frequency. It is also used to program the delay times between the external MOSFET turn on and turn off periods, which eliminates cross conduction in those MOSFETs. See the Applications Section for programming the oscillator and for controlling cross conduction.

VDRVHI: This pin supplies power to the high side output driver, GATEHI. Connect VDRVHI to an 18V or lower source for power supplies converting 12VDC to lower voltages, and to a 12V source for systems for power supplies converting 5VDC. This pin should be bypassed directly to PGND using a low ESR capacitor.

VDRVLO: This pin supplies power to the low side output driver, GATELO. VDRVLO is typically connected to a 12V source, but may be connected to a 5V source for driving logic level MOSFETs. This pin should be bypassed directly to PGND using a low ESR capacitor.

VIN: This pin supplies power to the chip. Connect VIN to a stable voltage source that is at least 10.8V above GND. The GATEHI, GATELO and PWRGD outputs will be held low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to GND.

VFB: This pin is the inverting input to the error amplifier. This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF: This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A Converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01 μF.

VSNS: This pin is connected to the system output voltage through a low pass R-C filter. When the voltage on VSNS rises above or falls below the COMMAND voltage by 9%, the PWRGD output is driven low to reset the microprocessor. When the voltage on VSNS rises above the COMMAND voltage by 17.5%, the OVP comparator disables the GATEHI output and enables the GATELO output, forcing 0% duty cycle on the power supply. This pin is also used by the foldback current limiting circuitry to indicate when the output voltage has been short circuited. VSNS should be decoupled very closely to the IC with a capacitor to GND. The OV and UV comparators' hysteresis is typically 20mV, requiring good layout and filtering techniques to insure that noise and ground-bounce do not inadvertently trip the OV and UV comparators. It is recommended that an R-C filter set to approximately Fs/10 be used to filter noise from the system output, where Fs is the oscillator frequency.

DAC INFORMATION

The 5-bit Digital-to-Analog Converter (DAC) is programmed according to Table 1.The COMMAND voltage is always active as long as the UCC3882 VIN pin is above the undervoltage lockout voltage. For the 3882, the output gate drives GATEHI and GATELO are disabled at certain DAC codes, as shown in Table 1. Disabling the gate drives disables the power supply. For the 3882 -1, the GATEHI and GATELO drives are enabled for all DAC codes. For a given code, the power supply output regulates at the corresponding COMMAND voltage.

Table 1. Programming the Command Voltage for the UCC3882

Digital Command					Command Voltage	GATEHI/GATELO Status	Digital Command					Command Voltage	GATEHI/GATELO Status
D4	D3	D2	D1	D0			D4	D3	D2	D1	D0		
0	1	1	1	1	1.300	Note 1 ?	1	1	1	1	1	2.000	Note 1 ?
0	1	1	1	0	1.350	Note 1 ?	1	1	1	1	0	2.100	Enabled
0	1	1	0	1	1.400	Note 1 ?	1	1	1	0	1	2.200	Enabled
0	1	1	0	0	1.450	Note 1 ?	1	1	1	0	0	2.300	Enabled
0	1	0	1	1	1.500	Note 1 ?	1	1	0	1	1	2.400	Enabled
0	1	0	1	0	1.550	Note 1 ?	1	1	0	1	0	2.500	Enabled
0	1	0	0	1	1.600	Note 1 ?	1	1	0	0	1	2.600	Enabled
0	1	0	0	0	1.650	Note 1 ?	1	1	0	0	0	2.700	Enabled
0	0	1	1	1	1.700	Note 1 ?	1	0	1	1	1	2.800	Enabled
0	0	1	1	0	1.750	Note 1 ?	1	0	1	1	0	2.900	Enabled
0	0	1	0	1	1.800	Enabled	1	0	1	0	1	3.000	Enabled
0	0	1	0	0	1.850	Enabled	1	0	1	0	0	3.100	Enabled
0	0	0	1	1	1.900	Enabled	1	0	0	1	1	3.200	Enabled
0	0	0	1	0	1.950	Enabled	1	0	0	1	0	3.300	Enabled
0	0	0	0	1	2.000	Enabled	1	0	0	0	1	3.400	Enabled
0	0	0	0	0	2.050	Enabled	1	0	0	0	0	3.500	Enabled

APPLICATION INFORMATION

This IC is intended to be used in a high performance power supply to power the Pentium® II or a similar processor. Figure 1 shows a typical power supply application circuit which converts +5V to lower voltages required by the Pentium®II Processor.

Synchronous Switching Delay Time

Figure 2 shows that the fundamental difference between a Buck and a Synchronous Buck regulator is the use of a MOSFET rather than a Schottky diode as the low side or free-wheeling switch.

In order to maintain safe and efficient operation of a Synchronous Buck regulator, both MOSFETs, Q1 and Q2, should never be turned on at the same time. Having both MOSFETs on at the same time results in cross conduction, which can result in excessively high power dissipation in one or both MOSFETs. The UCC3882 has a built in delay between the turn OFF of one MOSFET and the turn ON of the other MOSFET. This delay is a controlled delay between the GATEHI and GATELO drive outputs and is programmable by the selection of the resistor R_T. Controlling the delay between the gate drive outputs is only part of the solution. The power supply designer must also understand intrinsic delays involving MOSFET turn on, turn off, rise and fall times in order to insure that there is no cross conduction.

It is recommended that a value between 10 kΩ and 15 kΩ be used for R_T, which minimizes the delay and can result in the highest efficiency operation. A higher value of R_T will result in a larger delay between the MOSFET Gate transitions. R_T should be between 10 kΩ minimum and 50 kΩ maximum.

Programming the Oscillator

The first step in programming the oscillator is choosing the value of R_T as described above. The second step is to program the frequency according to the curves shown in Figure 3, by choosing the appropriate capacitor value.ransitions. R_T should be between 10 kΩ minimum and 50 kΩ maximum.

For convenience, values are shown in Table 1 for nominal frequencies from 100 kHz to 700 kHz using standards resistors and capacitor values.

Table 2. Programming Standard Frequencies

FREQUENCY (kHz)	R_T (kΩ)	C_T (pF)
100	14.7	5600
200	11.0	3900
300	10.5	2700
400	11.3	1800
500	12.7	1200
600	10.7	1200
700	11.0	1000

An excessively long delay time between gate drive signals, or a delay time that is too small, will result in a inefficient power supply design. The third step in programming the oscillator is to observe the actual circuit waveforms to insure that the delay is optimal. The designer should vary R_T and C_T accordingly to adjust the delay time and to program the proper oscillator frequency.

Using an External Schottky Diode in Parallel With the Low Side MOSFET

The purpose of using a synchronous buck regulator is to substitute a low voltage drop MOSFET in place of a Schottky diode as the low side switch. An external Schottky diode may still be required however, in order to reduce the losses due to the reverse recovery of the low-side MOSFET body diode. Figure 4 illustrates the effects on power losses due to the non-ideal nature of a typical MOSFET body diode. IRM is the peak recovery current of the body diode of Q2 and I_{LOUT} is the current of the output inductor. Using a parallel Schottky diode can reduce these losses and increase circuit efficiency. The size of the diode should be increased as a function of load current, input voltage, and operating frequency. The diode should be as close to the lower MOSFET, Q2, as possible, to reduce stray inductance.

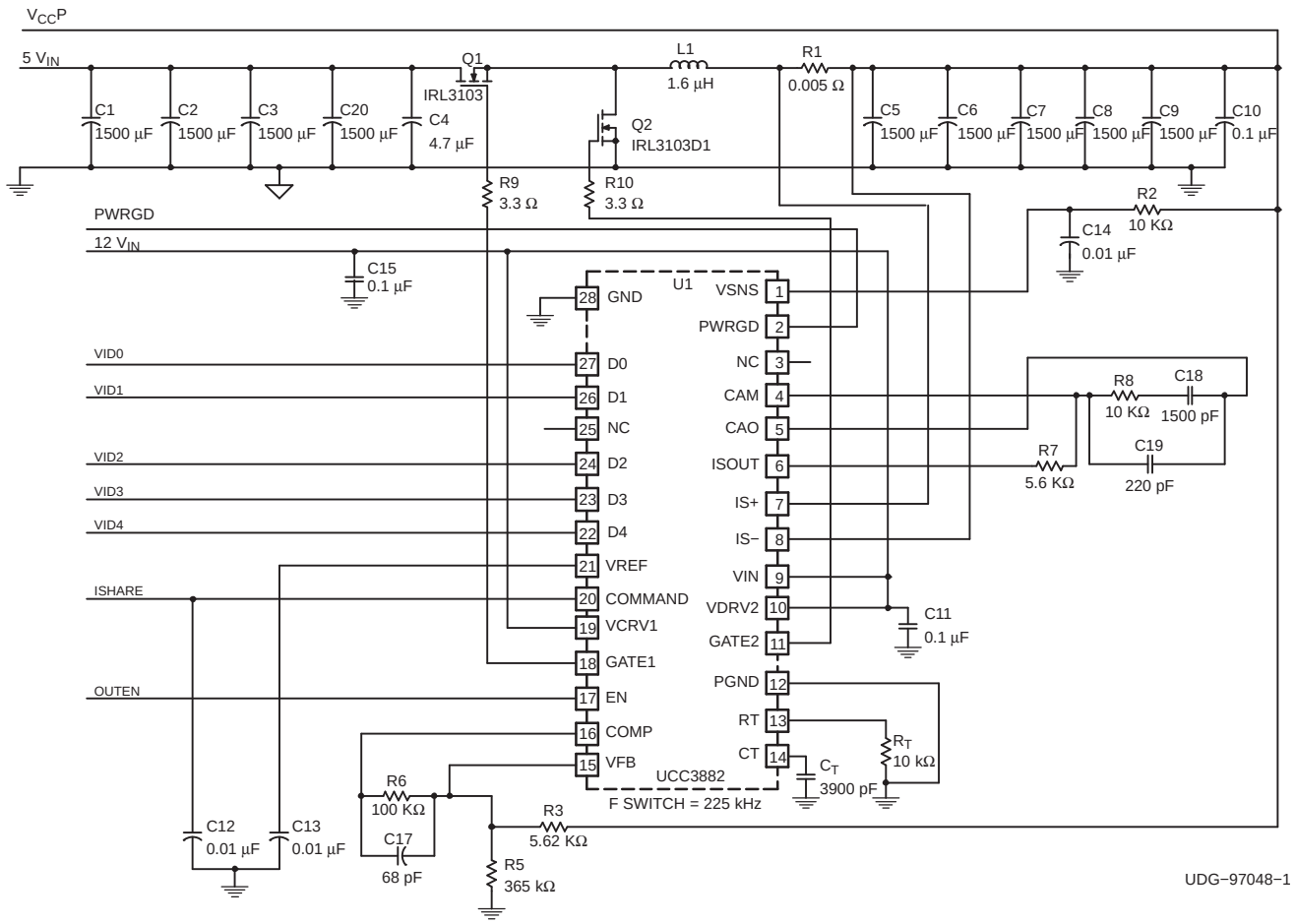


Figure 1. Application Circuit – Pentium® II Power Supply

Choosing R_{SENSE} to Set the Current Limit

R_{SENSE} is chosen to limit the maximum (short circuit) current of the power supply. The short circuit current equation for the UCC3882 is:

$$ISC = \frac{1.37\ V}{RSENSE \times 16} \quad (1)$$

and therefore, the value of the sense resistor, for a chosen short circuit current is:

$$RSENSE = \frac{1.37\ V}{ISC \times 16} \quad (2)$$

The short circuit current limit does vary slightly as a function of the switching regulator's output inductor value and operating frequency because a high value of ripple current will reduce the average short circuit current limit. Figure 5 shows the variation in Isc given common values for the UCC3882. The UCC3882 is nominally configured so that a 0.005 mΩ resistor will set the current limit to approximately 17A.

The UCC3882 incorporates short circuit current foldback, as shown in Figure 6. When the output of the power supply is short circuited, the output voltage falls. When the output voltage reaches 1/2 of its nominal voltage (COMMAND/ 2) then the output current is reduced. This feature reduces the amount of current in the MOSFETs and capacitors, and insures high reliability.

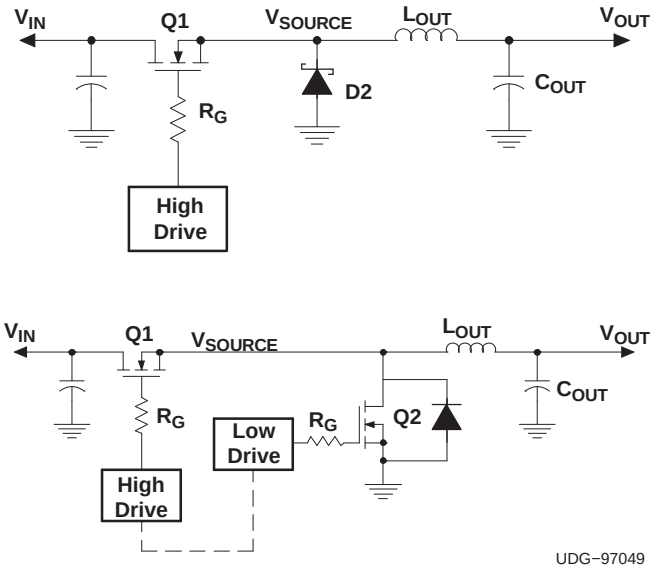


Figure 2. Buck vs Synchronous Buck Regulator

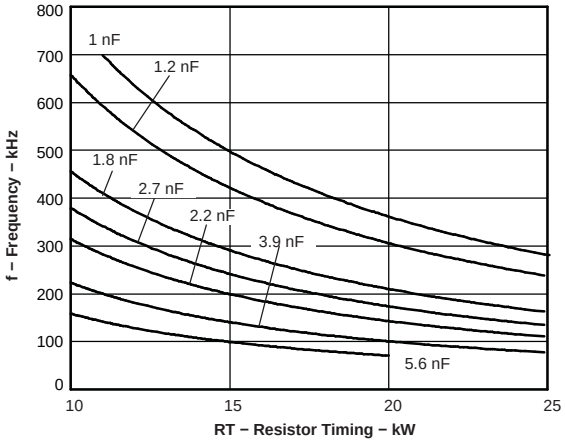


Figure 3. Programming UCC3882 Oscillator Frequency

Choosing VDRVLO, VDRVHI and VIN,

The UCC3882 requires a nominal 12V input supplied at VIN. VDRVLO and VDRVHI can be set to any voltage less than 18.5V, and may be set individually. A power supply deriving its power from +5V should use +12V at the VDRVHI pin, but may use either +5V or +12V depending on the drive requirements of the synchronous low-side MOSFET. A power supply deriving its power from +12V should use +18V at VDRVHI in order to provide adequate voltage (6 V) gate drive to the high-side MOSFET. VIN must be less than +15V.

Input Capacitors

The input capacitors are chosen primarily based on their switching frequency RMS current handling capability and their voltage rating. The input capacitors must handle virtually all of the RMS current at the switching frequency, even if the circuit does not have an input inductor. The switching current in the input capacitors appears as shown in Figure 7.

Aluminum or tantalum capacitors can be used. The amount of RMS current in an Electrolytic capacitor has a strong impact on the reliability and lifetime of the capacitor. Other factors which affect the life of an input capacitor are internal heat rise, external airflow, the amount of time that the circuit operates at maximum current and the operating voltage. The curves in Figure 8 show the RMS current handled by the total input capacitance in typical VRM circuits powered from 5 V or from 12 V.

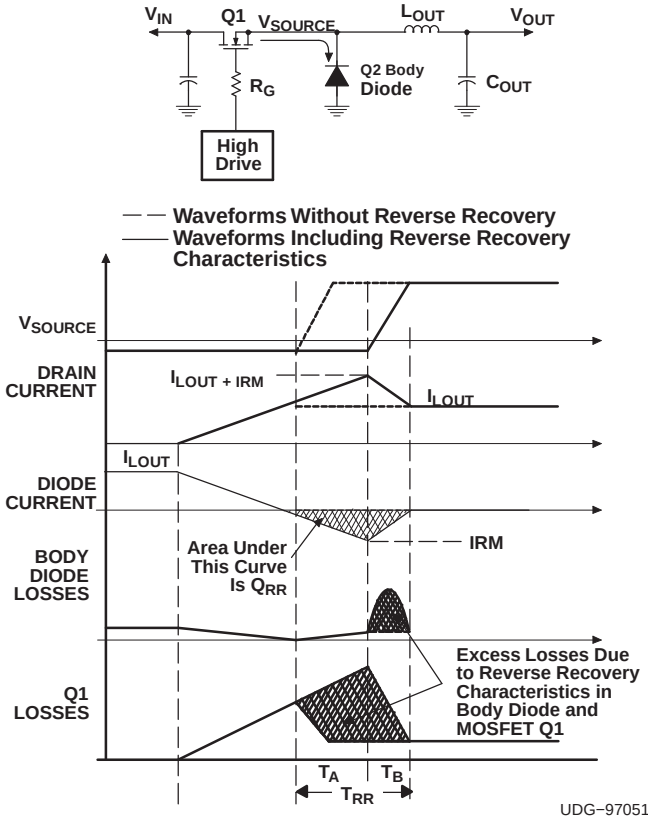


Figure 4. Effects of Reverse Recovery in a Synchronous Rectifier

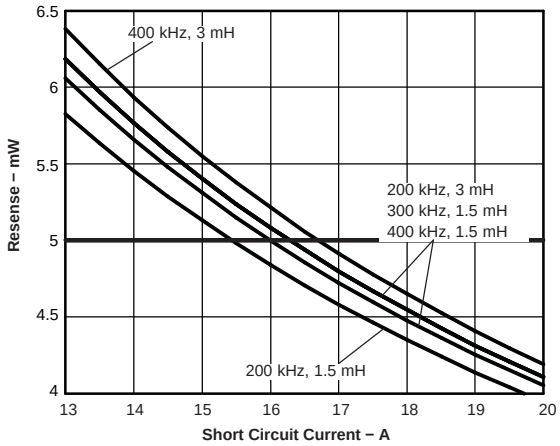


Figure 5. Short Circuit Current Limit vs R_{SENSE} for Various Frequency and Inductor Values

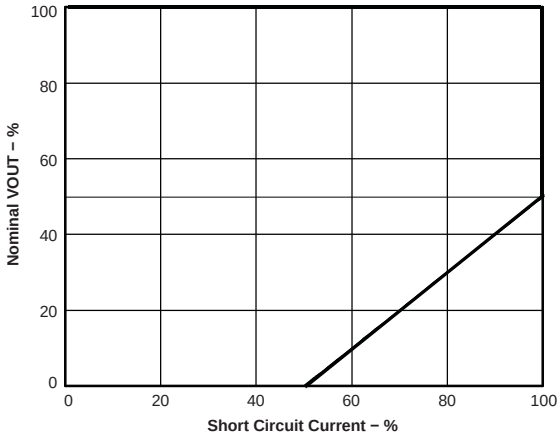


Figure 6. Short circuit Foldback Reduces Stress on Circuit Components by Reducing Short Circuit Current

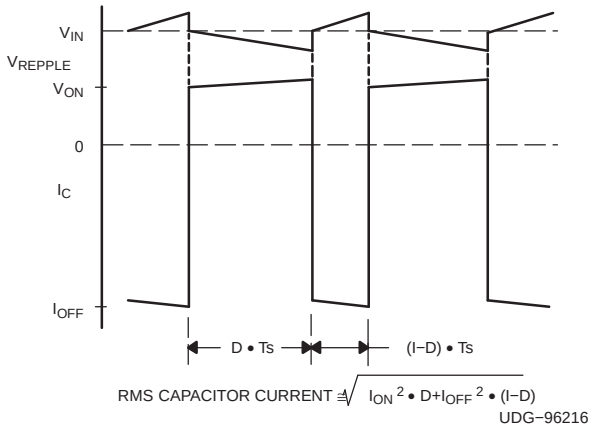


Figure 7. Input Capacitors Current Waveform

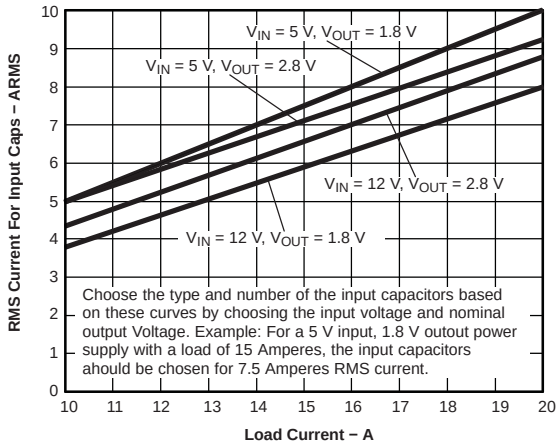


Figure 8. Load Current vs RMS Current for Input Capacitors – Pentium® II Family

Demonstration Kit Design and Performance

A demonstration circuit was built based on the UCC3882 and utilizing an Intel VRM 8.1 form factor connector. The schematic is shown in Figure 9 and the list of materials in Table 3. The circuit is configured for the following operating parameters:

- Switching Frequency = 225 kHz
- Rated Output Current = 15 A
- Short Circuit Current = 17 A Nominal
- Output Voltage: 1.8 V to 2.8 V Configured by VID Code.
- Airflow: 100 LFM
- Temperature: 0°C to 60°C
- Regulation: Per Intel VRM 8.1 DC-DC Converter Design Guidelines

Figure 17–Figure 19 show the performance of the circuit.

Table 3. List of Materials

REF	DESCRIPTION	PACKAGE
U1	Unitrode UCC3882 DAC/PWM	SOIC-28 WIDE
C01	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
C02	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
C03	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
C04	Sprague/Vishay 595D475X0016A2B, 4.7 μF 16 V Tantalum	SPRAGUE Size A,
C05	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
C06	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
C07	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
C08	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
C09	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
C10	0.10 μF Ceramic	1206 SMD
C11	0.10 μF Ceramic	1206 SMD
C12	0.01 μF Ceramic	0603 SMD
C13	0.01 μF Ceramic	0603 SMD
C14	0.01 μF Ceramic	0603 SMD
C15	0.10 μF Ceramic	1206 SMD
C17	68 pF NPO Ceramic	0603 SMD
C18	1000 pF Ceramic	0603 SMD
C19	220 pF NPO Ceramic	0603 SMD
C20	Sanyo 6MV1500GX, 1500 μF, 6.3 V, Aluminum Electrolytic	10x20mm Radial Can
CT	3900pF Ceramic	0603 SMD
J1	AMP 532956-7 40 Pin Connector	40 Pin
L1	Toroid T51-52C, 5 Turns #16AWG, 1.6 μH	Toroid
Q1	International Rectifier IRL3103, 30 V, 56 A	TO-220AB, layed down
Q2	International Rectifier IRL3103D1, 30 V, 56 A	TO-220AB, layed down
R01	5 mΩ, PCB Resistor	Copper Trace
R02	10 kΩ, 5%, 1/16 Watt	0603 SMD
R03	5.62 kΩ, 1%, 1/16 Watt	0603 SMD
R05	365 kΩ, 1%, 1/16 Watt	0603 SMD
R06	100 kΩ, 5%, 1/16 Watt	0603 SMD
R07	5.6 kΩ, 5%, 1/16 Watt	0603 SMD
R08	10 kΩ, 5%, 1/16 Watt	0603 SMD
R09	3.3 Ω, 5%, 1/16 Watt	0603 SMD
R10	3.3 Ω, 5%, 1/16 Watt	0603 SMD

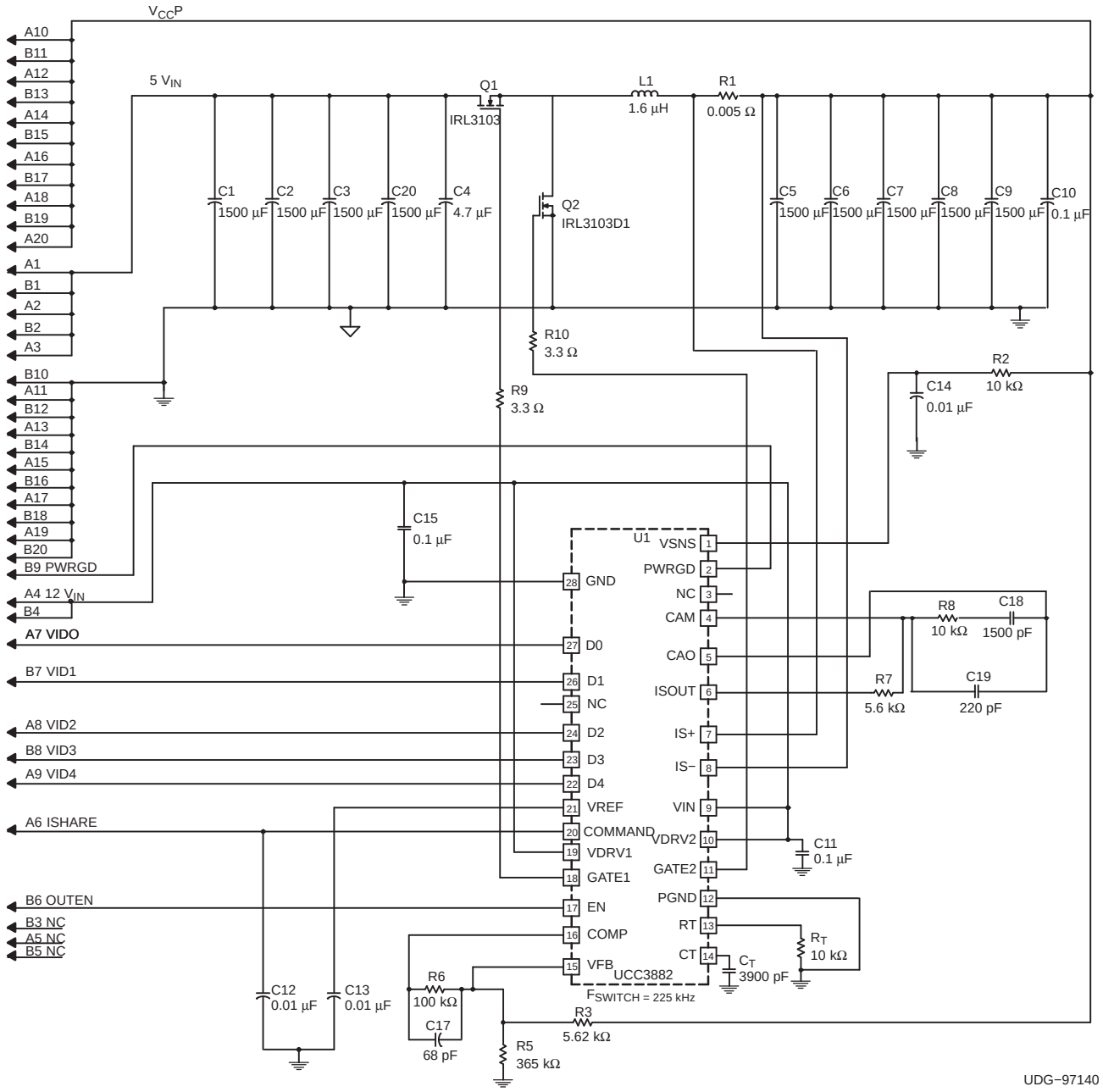


Figure 9. Reference Design – UCC3882 5-Bit Synchronous Wectifier PWM Controller for the Intel Pentium®II Processor

Figure 10. Demo Board

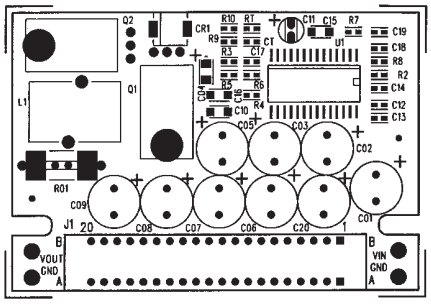


Figure 11. COMP Silkscreen

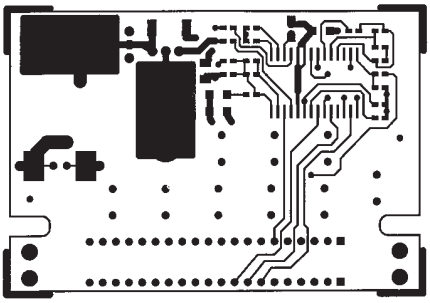


Figure 12. COMP Side

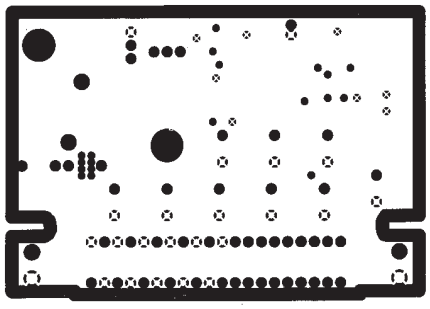


Figure 13. GND Layer

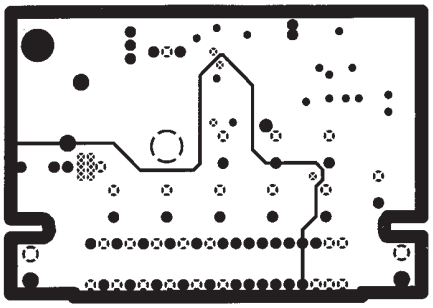


Figure 14. PWR Layer

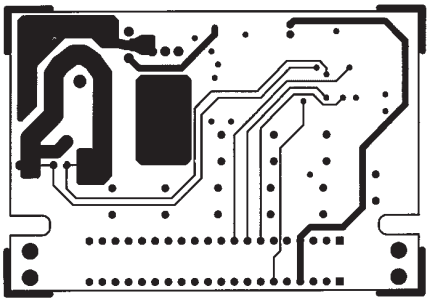
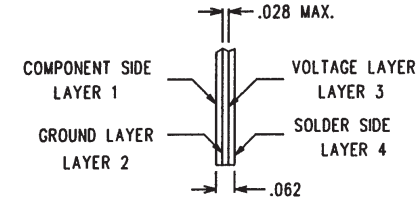
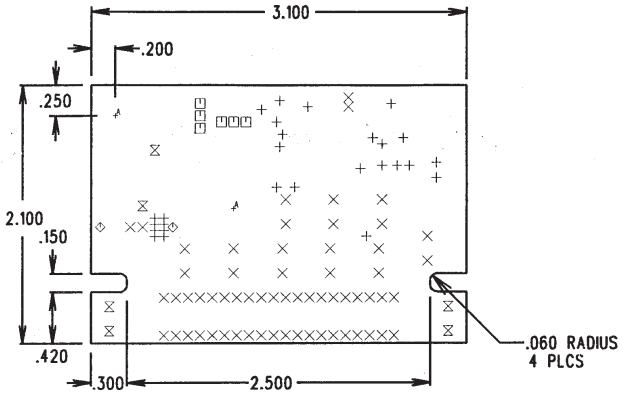


Figure 15. Solder Side



1 OZ. CU. INNER LAYERS, 1 OZ. CU. OUTER LAYERS



DRILL DRAWING
UCC3882 BOARD

NOTES:

1. MAT'L: .062 THK. FR4 COPPERCLAD LAMINATE
2. ALL HOLES TO BE PLATED THRU WITH A MINIMUM WALL THICKNESS OF .001 AND A SOLDER COATING OF .0003.
3. BOARDS TO BE SOLDERMASKED BOTH SIDES LPI OBC.
4. BOARDS TO BE SILKSCREENED ON BOTH SIDES WITH PERMANENT, WHITE EPOXY (CHEMICAL AND SCRATCH RESISTANT).
5. BOARDS SHALL BE MADE FROM UNDERWRITER LABORATORY RECOGNIZED MATERIAL AND THE FINISHED BOARD MUST CARRY THE VENDER'S U.L. LOGO.
6. ALL DRAWINGS AND FILMS VIEWED FROM COMPONENT SIDE.

DRILL CHART			
SYMBOL	SIZE	QTY	PLATED TYPE
+	.016	27	PLATED
×	.037	62	PLATED
□	.045	6	PLATED
◇	.050	2	PLATED
⧖	.070	6	PLATED
A	.156	2	PLATED

Figure 16. Drill Drawing

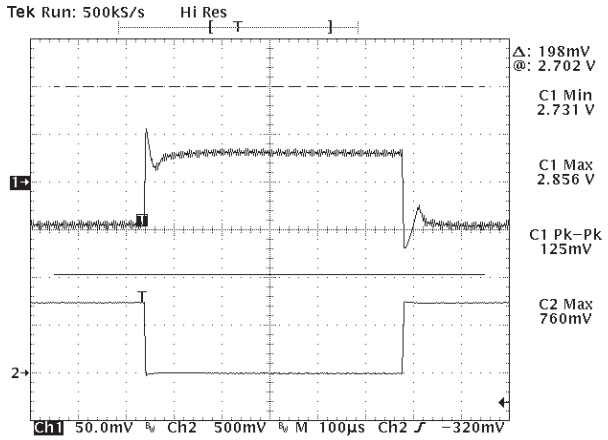


Figure 17. Transient Response to 15.2A Step Load Channel 2 Scale is 50 mV/A

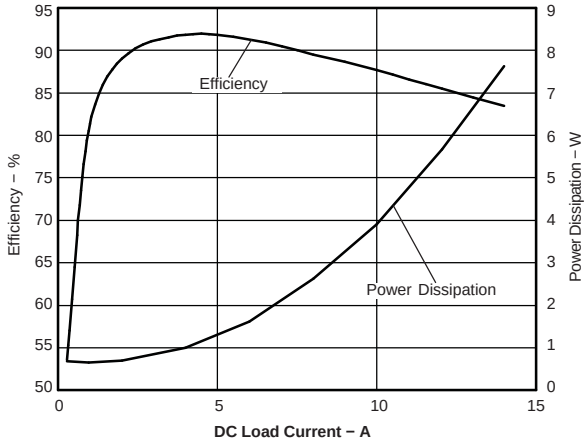


Figure 18. UCC3882 Demo Kit Efficiency

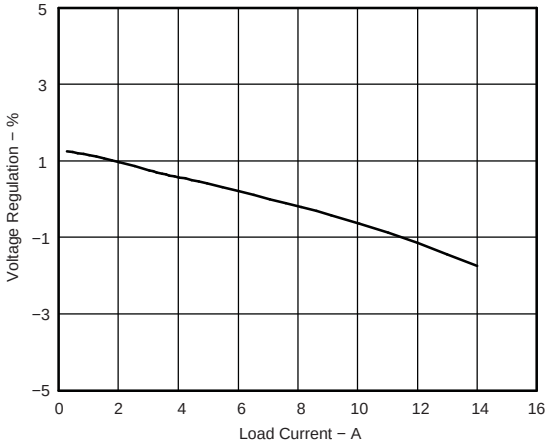


Figure 19. Load Regulation

REVISION HISTORY

Changes from Revision B (September 2008) to Revision C	Page
• Added A voltage of 1.5 V will be interrpreted as a zero while the voltage above 3.5 V will be interrpreted as a 1.	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC3882DW-1	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC3882DW-1G4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC3882PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC3882PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC3882PWTR-1	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
UCC3882PWTR-1G4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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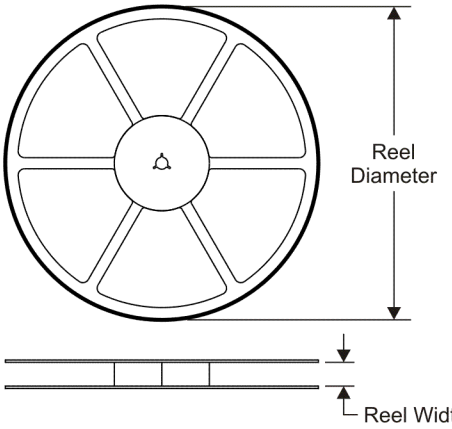
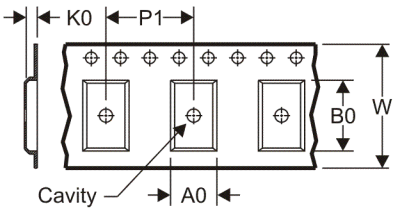
TAPE AND REEL INFORMATION

REEL DIMENSIONS

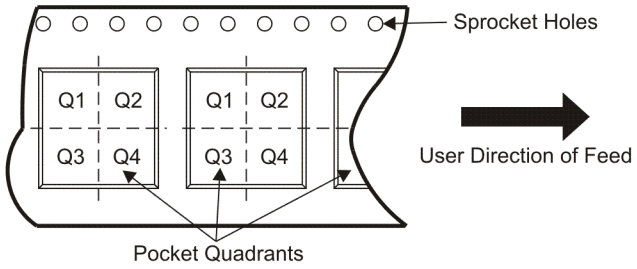


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

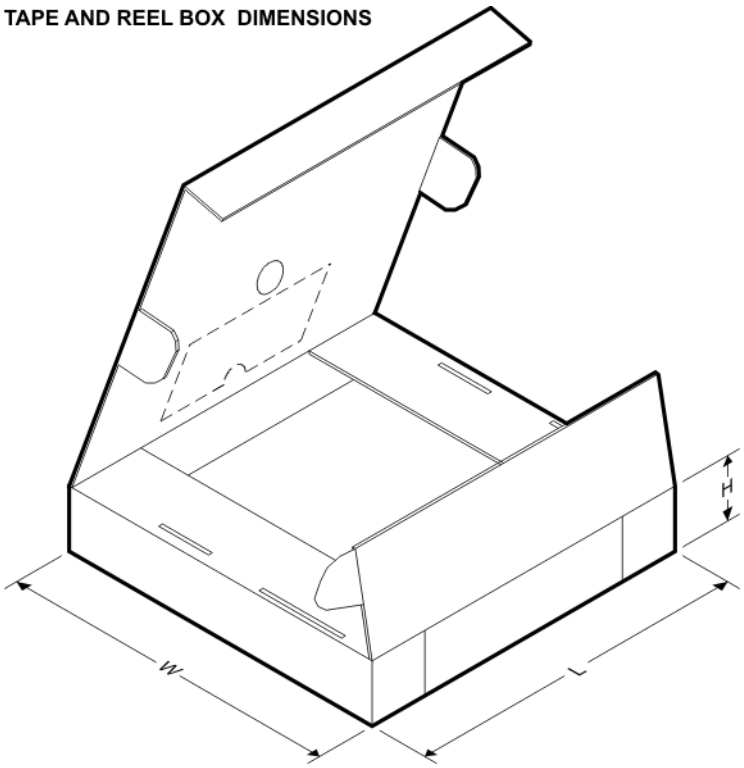
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC3882PWTR-1	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC3882PWTR-1	TSSOP	PW	28	2000	346.0	346.0	33.0

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