# THE DATASHEET OF

# TMS320DM8168CCYG2

www.win-source.net 0086-755-83957316

# TMS320DM816x DaVinci™ Digital Media Processors

## 1 Device Overview

### 1.1 Features

- High-Performance DaVinci Digital Media Processors
  - ARM® Cortex™-A8 RISC Processor
    - Up to 1.20 GHz
  - C674x™ VLIW DSP
    - Up to 1 GHz
    - Up to 8000 MIPS and 6000 MFLOPS
    - Fully Software-Compatible with C67x+ and C64x+™
- ARM Cortex-A8 Core
  - ARMv7 Architecture
    - In-Order, Dual-Issue, Superscalar Processor Core
    - NEON™ Multimedia Architecture
  - Supports Integer and Floating Point (VFPv3-IEEE754 Compliant)
    - Jazelle® RCT Execution Environment
- ARM Cortex-A8 Memory Architecture
  - 32-KB Instruction and Data Caches
  - 256-KB L2 Cache
  - 64-KB RAM, 48-KB of Boot ROM
- TMS320C674x Floating-Point VLIW DSP
  - 64 General-Purpose Registers (32-Bit)
  - Six ALU (32-Bit and 40-Bit) Functional Units
    - Supports 32-Bit Integer, SP (IEEE Single Precision, 32-Bit) and DP (IEEE Double Precision, 64-Bit) Floating Point
    - Supports up to Four SP Adds Per Clock and Four DP Adds Every Two Clocks
    - Supports up to Two Floating-Point (SP or DP) Approximate Reciprocal or Square Root Operations Per Cycle
  - Two Multiply Functional Units
    - Mixed-Precision IEEE Floating-Point Multiply Supported up to:
      - 2 SP x SP → SP Per Clock
      - 2 SP x SP → DP Every Two Clocks
      - 2 SP x DP → DP Every Three Clocks
      - 2 DP x DP → DP Every Four Clocks
    - Fixed-Point Multiply Supports Two 32 x 32 Multiplies, Four 16 x 16-Bit Multiplies Including Complex Multiplies, or Eight 8 x 8-Bit Multiplies per Clock Cycle
- C674x Two-Level Memory Architecture
  - 32-KB L1P and L1D RAM and Cache
  - 256-KB L2 Unified Mapped RAM and Caches
- System Memory Management Unit (System MMU)
  - Maps C674x DSP and EMDA TCB Memory Accesses to System Addresses
- 512KB of On-Chip Memory Controller (OCMC) RAM
- Media Controller
  - Manages HDVPSS and HDVICP2 Modules
- Up to Three Programmable High-Definition Video Image Coprocessing (HDVICP2) Engines
  - Encode, Decode, Transcode Operations
  - H.264, MPEG-2, VC-1, MPEG-4 SP and ASP
- SGX530 3D Graphics Engine (Available Only on the DM8168 Device)
  - Delivers up to 30 MTriangles per Second
  - Universal Scalable Shader Engine
  - Direct3D® Mobile, OpenGL® ES 1.1 and 2.0, OpenVG™ 1.1, OpenMax™ API Support
  - Advanced Geometry DMA Driven Operation
  - Programmable HQ Image Anti-Aliasing
- Endianness
  - ARM, DSP Instructions and Data – Little Endian
- HD Video Processing Subsystem (HDVPSS)
  - Two 165-MHz HD Video Capture Channels
    - One 16-Bit or 24-Bit and One 16-Bit Channel
    - Each Channel Splittable Into Dual 8-Bit Capture Channels
  - Two 165-MHz HD Video Display Channels
    - One 16-Bit, 24-Bit, 30-Bit Channel and One 16-Bit Channel
  - Simultaneous SD and HD Analog Output
  - Digital HDMI 1.3 Transmitter with PHY with HDCP up to 165-MHz Pixel Clock
  - Three Graphics Layers
- Dual 32-Bit DDR2 and DDR3 SDRAM Interfaces
  - Supports up to DDR2-800 and DDR3-1600
  - Up to Eight x8 Devices Total
  - 2GB of Total Address Space
  - Dynamic Memory Manager (DMM)
    - Programmable Multi-Zone Memory Mapping and Interleaving
    - Enables Efficient 2D Block Accesses
    - Supports Tiled Objects in 0°, 90°, 180°, or 270° Orientation and Mirroring
    - Optimizes Interlaced Accesses
- One PCI Express® (PCIe) 2.0 Port with Integrated PHY

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

  - Single Port with 1 or 2 Lanes at 5.0 GT per Second
  - Configurable as Root Complex or Endpoint
- Serial ATA (SATA) 3.0 Gbps Controller with Integrated PHYs
  - Direct Interface for Two Hard Disk Drives
  - Hardware-Assisted Native Command Queuing (NCQ) from up to 32 Entries
  - Supports Port Multiplier and Command-Based Switching
- Two 10 Mbps, 100 Mbps, and 1000 Mbps Ethernet MACs (EMAC)
  - IEEE 802.3 Compliant (3.3-V I/O Only)
  - MII and GMII Media Independent Interfaces
  - Management Data I/O (MDIO) Module
- Dual USB 2.0 Ports with Integrated PHYs
  - USB 2.0 High-Speed and Full-Speed Client
  - USB 2.0 High-Speed, Full-Speed, and Low-Speed Host
  - Supports Endpoints 0-15
- General-Purpose Memory Controller (GPMC)
  - 8-Bit and 16-Bit Multiplexed Address and Data Bus
  - Up to 6 Chip Selects with up to 256-MB Address Space per Chip Select Pin
  - Glueless Interface to NOR Flash, NAND Flash (with BCH and Hamming Error Code Detection), SRAM and Pseudo-SRAM
  - Error Locator Module (ELM) Outside of GPMC to Provide up to 16-Bit and 512-Byte Hardware ECC for NAND
  - Flexible Asynchronous Protocol Control for Interface to FPGA, CPLD, ASICs
- Enhanced Direct-Memory-Access (EDMA) Controller
  - Four Transfer Controllers
  - 64 Independent DMA Channels and 8 Quick DMA (QDMA) Channels
- Seven 32-Bit General-Purpose Timers
- One System Watchdog Timer
- Three Configurable UART, IrDA, and CIR Modules
  - UART0 with Modem Control Signals
  - Supports up to 3.6864 Mbps UART
  - SIR, MIR, FIR (4.0 MBAUD), and CIR
- One 40-MHz Serial Peripheral Interface (SPI) with Four Chip Selects
- SD and SDIO Serial Interface (1-Bit and 4-Bit)
- Dual Inter-Integrated Circuit ( $I^2C$ bus®) Ports
- Three Multichannel Audio Serial Ports (McASPs)
  - One Six-Serializer Transmit and Receive Port
  - Two Dual-Serializer Transmit and Receive Ports
  - DIT-Capable For SDIF and PDIF (All Ports)
- Multichannel Buffered Serial Port (McBSP)
  - Transmit and Receive Clocks up to 48 MHz
  - Two Clock Zones and Two Serial Data Pins
  - Supports TDM, I2S, and Similar Formats
- Real-Time Clock (RTC)
  - One-Time or Periodic Interrupt Generation
- Up to 64 General-Purpose I/O (GPIO) Pins
- On-Chip ARM ROM Bootloader (RBL)
- Power, Reset, and Clock Management
  - SmartReflex™ Technology (Level 2)
  - Seven Independent Core Power Domains
  - Clock Enable and Disable Control For Subsystems and Peripherals
- IEEE 1149.1 (JTAG) and IEEE 1149.7 (cJTAG) Compatible
- Via Channel™ Technology Enables use of 0.8-mm Design Rules
- 40-nm CMOS Technology
- 3.3-V Single-Ended LVCMOS I/Os (Except for DDR3 at 1.5 V, DDR2 at 1.8 V, and DEV_CLKIN at 1.8 V)


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## 1.2 Applications

- Video Encode, Decode, Transcode, and Transrate
- Video Security
- Video Conferencing
- Video Infrastructure
- Media Server
- Digital Signage

## 1.3 Description

The DM816x DaVinci video processors are a highly integrated, programmable platform that leverages TI's DaVinci technology to meet the processing needs of the following applications: video encode, decode, transcode, and transrate; video security; video conferencing; video infrastructure; media server; and digital signage.

The device enables original-equipment manufacturers (OEMs) and original-design manufacturers (ODMs) to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance through the maximum flexibility of a fully integrated mixed processor solution. The device combines programmable video and audio processing with a highly integrated peripheral set.

Key to the device are up to three high-definition video and imaging coprocessors (HDVICP2). Each coprocessor can perform a single 1080p60 H.264 encode or decode or multiple lower resolution or frame rate encodes and decodes. Multichannel HD-to-HD or HD-to-SD transcoding and multicoding are also possible. With the ability to simultaneously process 1080p60 streams, the TMS320DM816x device is a powerful solution for today's demanding HD video application requirements.

Programmability is provided by an ARM Cortex-A8 RISC CPU with NEON extension, TI C674x VLIW floating-point DSP core, and high-definition video and imaging coprocessors. The ARM processor lets developers keep control functions separate from audio and video algorithms programmed on the DSP and coprocessors, thus reducing the complexity of the system software. The ARM Cortex-A8 32-bit RISC processor with NEON floating-point extension includes: 32KB of instruction cache; 32KB of data cache; 256KB of L2 cache; 48KB of public ROM, and 64KB of RAM.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each peripheral, see the related sections in this document and the associated peripheral reference guides. The peripheral set includes: HD video processing subsystem (HDVPSS), which provides output of simultaneous HD and SD analog video and dual HD video inputs; up to two Gigabit Ethernet MACs (10 Mbps,100, Mbps, 1000 Mbps) with GMII and MDIO interface; two USB ports with integrated 2.0 PHY; PCIe port x2 lanes GEN2 compliant interface, which allows the device to act as a PCIe root complex or device endpoint; one 6-channel McASP audio serial port (with DIT mode); two dual-channel McASP audio serial ports (with DIT mode); one McBSP multichannel buffered serial port; three UARTs with IrDA and CIR support; SPI serial interface; SD and SDIO serial interface; two $I^2C$ master and slave interfaces; up to 64 GPIO pins; seven 32-bit timers; system watchdog timer; dual DDR2 and DDR3 SDRAM interface; flexible 8-bit and 16-bit asynchronous memory interface; and up to two SATA interfaces for external storage on two disk drives or more with the use of a port multiplier.

The device also includes an SGX530 3D graphics engine (available only on the TMS320DM8168 device) to enable sophisticated GUIs and compelling user interfaces and interactions. Additionally, the device has a complete set of development tools for both the ARM and DSP, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Microsoft® Windows® debugger interface for visibility into source code execution.

The C674x DSP core is the high-performance floating-point DSP generation in the TMS320C6000™ DSP platform. The C674x floating-point DSP processor uses 32KB of L1 program memory and 32KB of L1 data memory. Up to 32KB of L1P can be configured as program cache. The remaining is noncacheable no-wait-state program memory. Up to 32KB of L1D can be configured as data cache. The remaining is noncacheable no-wait-state data memory. The DSP has 256KB of L2 RAM, which can be defined as SRAM, L2 cache, or a combination of both. All C674x L3 and off-chip memory accesses are routed through a system MMU.

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The device package has been specially engineered with Via Channel technology. This technology allows use of 0.8-mm pitch PCB feature sizes in this 0.65-mm pitch package, and substantially reduces PCB costs. Via Channel technology also allows PCB routing in only two signal layers due to the increased layer efficiency of the Via Channel BGA technology.

**Device Information**

| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| TMS320DM8168CYG | FCBGA (1031) | 25.0 mm x 25.0 mm |
| TMS320DM8167CYG | FCBGA (1031) | 25.0 mm x 25.0 mm |
| TMS320DM8165CYG | FCBGA (1031) | 25.0 mm x 25.0 mm |


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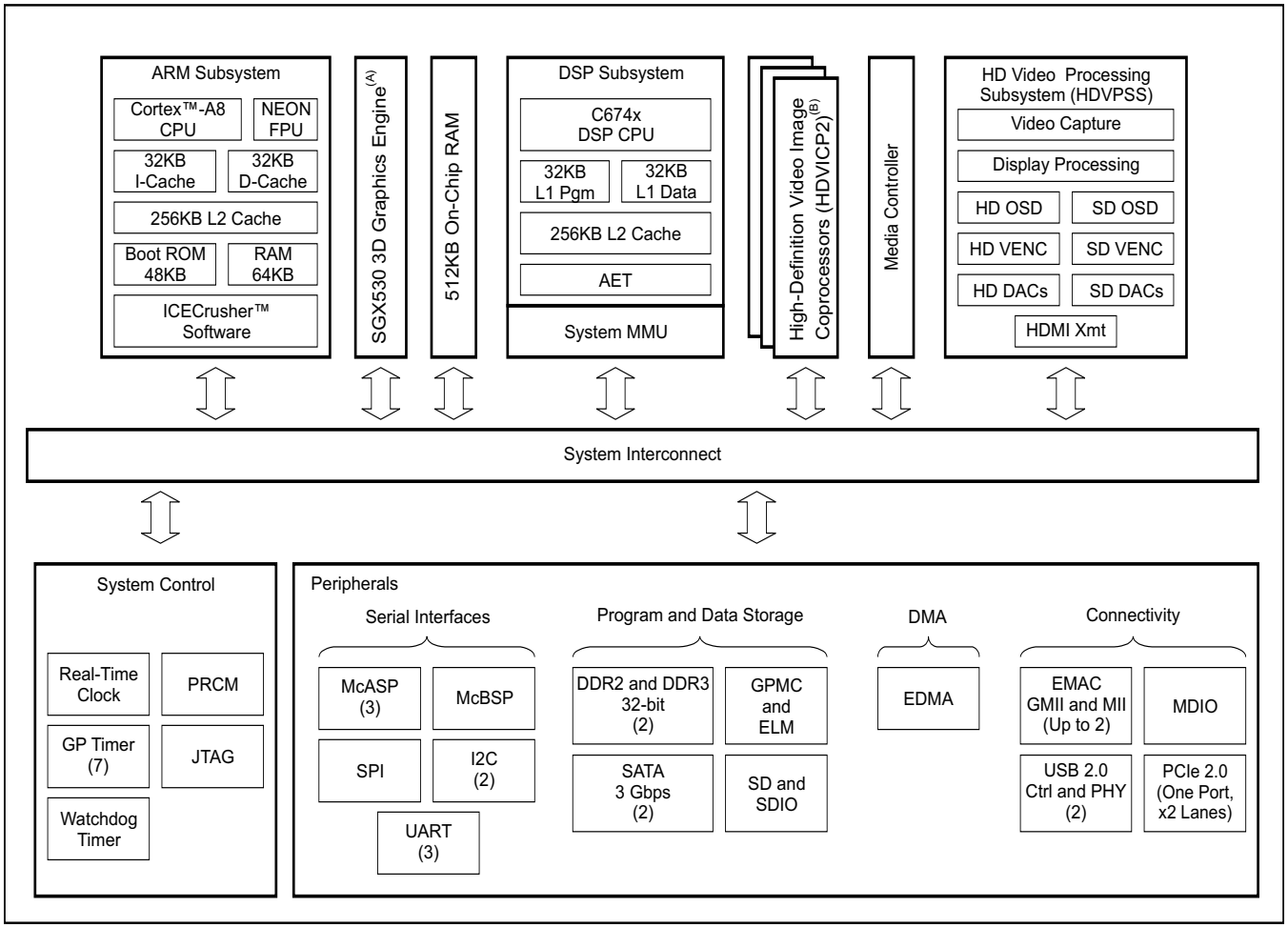
## 1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.




A. SGX530 is available only on the TMS320DM8168 devices.
B. Three HD video image coprocessors (HDVICP2) are available on the TMS320DM8168 and TMS320DM8167 devices; two (HDVICP2-0 and HDVICP2-1) are available on the TMS320DM8165 devices.

**Figure 1-1. TMS320DM816x Device Functional Block Diagram**

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from February 1, 2014 to March 17, 2015 (from E Revision (February 2014) to F Revision) | Page |
|---|---|
| • Updated entire document to adhere to Superior Data Manual Standards | 1 |
| • Updated/Changed title from "*...Video Processors...*" to "*...Digital Media Processors...*" | 1 |
| • Updated/Changed ARM® Cortex™-A8 RISC Processor in Features from "*Up to 1.35 GHz*" to "*Up to 1.20 GHz*" | 1 |
| • Updated/Changed C674x™ VLIW DSP in Features from "*Up to 1.25 GHz*" to "*Up to 1 GHz*" | 1 |
| • Updated/Changed C674x™ VLIW DSP in Features from "*Up to 9000 MIPS and 6750 MFLOPS*" to "*Up to 8000 MIPS and 6000 MFLOPS*" | 1 |
| • Updated/Changed CPU Frequency row | 10 |
| • Removed Cycle Time row | 10 |
| • Updated/Changed Handling Ratings to ESD Ratings | 116 |
| • Updated/Changed CVDD Initial Startup NOM from "1.00 or 1.10" to "1.00 or **1.05**" | 117 |
| • Updated/Changed CVDD CYG & CYG2 NOM from "0.85-1.10" top "**0.85-1.05**" | 117 |
| • Added footnote to CVDD CYG & CYG2 NOM value | 117 |
| • Updated footnote from "1.10V nominal (for CYG..." to "**1.05** nominal (for CYG..." | 118 |
| • Removed FSYSCLK row | 118 |
| • Removed "*AVS Variable Core voltage = 0.8 V*" from $I_{CDO}$ and $I_{DDD}$ | 120 |
| • Updated/Changed the System Clocking Overview Figure from "*432 MHz*" to "*audio reference clock*" | 149 |
| • Updated/Changed body of text in PLL Programming Limits | 154 |
| • Completely updated PLL Clock Frequencies table | 155 |
| • Completely updated SYSCLK Frequencies table | 156 |
| • Completely updated SYSCLK Frequencies table | 157 |
| • Updated/Changed $t_{su(CMDV-CLKH)}$ and $t_{h(CLKH-DATV)}$ MIN from "6.0" to "**4.1**" | 293 |
| • Updated/Changed $t_{h(CLKH-CMDIV)}$ and $t_{h(CLKH-DATV)}$ MIN from "19.2" to "**1.9**" | 293 |
| • Added footnote to $t_{d(CLKL-CMD)}$ and $t_{d(CLKL-DAT)}$ MIN values | 294 |
| • Updated/Changed the blank example from "*1.0-GHz ARM, 800-MHz DSP*" to "*930-MHz ARM, 750-MHz DSP*" | 321 |
| • Updated DEVICE SPEED RANGE in Figure 10-1 | 321 |
| • Completely updated Table 10-1 | 321 |

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# 3 Device Comparison

There are variations in the availability of some functions of the TMS320DM816x devices. A comparison of the devices, highlighting the differences, is shown in Table 3-1. For more detailed information on the significant device features, see Section 3.1, *Device Characteristics*.

**Table 3-1. Device Comparison**

| FEATURES | DEVICES | | |
|---|---|---|---|
| | TMS320DM8168 | TMS320DM8167 | TMS320DM8165 |
| HDVICP2 | 3 | 3 | 2 |
| SGX530 | Y | N | N |


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## 3.1 Device Characteristics

Table 3-2 provides an overview of the significant features of the TMS320DM816x devices, including the capacity of on-chip RAM, peripherals, and the package type with pin count.

**Table 3-2. Characteristics of the Processor**

| HARDWARE FEATURES | | DM8168, DM6187, and DM6185 |
|---|---|---|
| Peripherals<br>Not all peripherals pins are available at the same time (for more detail, see Section 6, *Device Configurations*). | HD Video Processing Subsystem (HDVPSS) | 1 16-bit and 24-bit HD Capture Channel ***or***<br>2 8-bit SD Capture Channels<br>***and***<br>1 16-bit HD Capture Channel ***or***<br>2 8-bit SD Capture Channels<br>***and***<br>1 16-bit, 24-bit, and 32-bit HD Display Channel<br>***and***<br>1 16-bit HD Display Channel<br>***and***<br>3 HD and 4 SD Video DACs<br>***and***<br>1 HDMI 1.3 Transmitter |
| | DDR2 and DDR3 Memory Controller | 2 (32-bit Bus Widths) |
| | GPMC and ELM | Asynchronous (8-bit and 16-bit bus width) RAM, NOR, NAND |
| | EDMA | 64 Independent Channels<br>8 QDMA Channels |
| | 10 Mbps, 100 Mbps, and 1000 Mbps Ethernet MAC with Management Data Input and Output (MDIO) | 2 (with MII and GMII Interface) |
| | USB 2.0 | 2 (Supports High-Speed and Full-Speed as a Device and High-Speed, Full-Speed, and Low-Speed as a Host) |
| | PCI Express 2.0 | 1 Port (2 5.0GT per second lanes) |
| | Timers | 7 (32-bit General Purpose)<br>***and***<br>1 (Watchdog) |
| | UART | 3 (with SIR, MIR, CIR support and RTS and CTS flow control)<br>(UART0 Supports Modem Interface) |
| | SPI | 1 (Supports 4 slave devices) |
| | SD and SDIO | 1 (1-bit or 4-bit) |
| | I2C | 2 (Master or Slave) |
| | McASP | 3 (1 Six-Serializer and 2 Dual Serializers, Each with Transmit and Receive and DIT Capability) |
| | McBSP | 1 (2 Data Pins, Transmit and Receive) |
| | Serial ATA (SATA) | Supports 2 Interfaces |
| | RTC | 1 |
| | GPIO | Up to 64 pins |
| On-Chip Memory | Organization | **ARM**<br>32KB I-cache<br>32KB D-cache<br>256KB L2 Cache<br>64KB RAM<br>48KB Boot ROM |
| | | **DSP**<br>32KB L1 Program (L1P) and Cache (up to 32KB)<br>32KB L1 Data (L1D) and Cache (up to 32KB)<br>256KB Unified Mapped RAM and Cache (L2) |
| | | **MEDIA CONTROLLER**<br>32KB Shared L1 Cache<br>256KB L2 RAM |

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**Table 3-2. Characteristics of the Processor (continued)**

| HARDWARE FEATURES | | | DM8168, DM6187, and DM6185 |
|---|---|---|---|
| | | | **ADDITIONAL SHARED MEMORY**<br>512KB On-chip RAM |
| CPU ID + CPU Rev ID | Control Status Register (CSR.[31:16]) | | 0x1003 |
| C674x Megamodule Revision | Revision ID Register (MM_REVID[15:0]) | | 0x0000 |
| JTAG BSDL_ID | JTAGID Register | | 0x2B81 E02F |
| CPU Frequency(1) | MHz | Blank | ARM Cortex-A8: 930 MHz |
| | | | DSP: 750 MHz |
| | | 2 | ARM Cortex-A8: 1100 MHz |
| | | | DSP: 930 MHz |
| | | 4 | ARM Cortex-A8: 1200 MHz |
| | | | DSP: 1000 MHz |
| Voltage | Core Logic (V) | | 1.0 V with Required AVS Capability |
| | USB Logic (V) | | 0.9 V |
| | RAM (V) | | 1.0 V |
| | IO (V) | | 1.5 V, 1.8 V, 3.3 V |
| Package | 25 x 25 mm | | 1031-Pin BGA (CYG) |
| Process Technology | µm | | 0.04 µm |
| Product Status(2) | Product Preview (PP),<br>Advance Information (AI),<br>or Production Data (PD) | | PD |

(1) For more information on the available device speed ranges for each part number, see Table 10-1.
(2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## 3.2 ARM Subsystem

The ARM subsystem is designed to give the ARM Cortex-A8 master control of the device. In general, the ARM Cortex-A8 is responsible for configuration and control of the various subsystem, peripherals, and external memories.

The ARM subsystem includes the following features:

- ARM Cortex-A8 RISC processor:
  - ARMv7 ISA plus Thumb®-2, Jazelle-X, and media extensions
  - NEON floating-point unit
  - Enhanced memory management unit (MMU)
  - Little Endian
  - 32KB L1 instruction cache
  - 32KB L1 data cache
  - 256KB L2 cache
- Foresight embedded trace module (ETM)
- ARM Cortex-A8 interrupt controller (AINTC)
- 64KB internal RAM
- 48KB internal public ROM.


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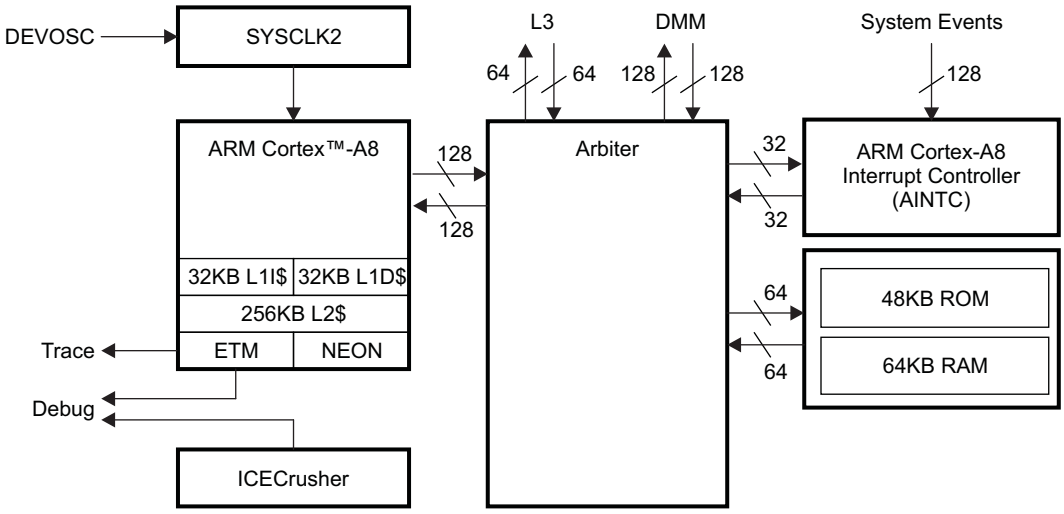


**Figure 3-1. ARM Cortex-A8 Subsystem Block Diagram**

### 3.2.1 ARM Cortex-A8 RISC Processor

The ARM Cortex-A8 subsystem integrates the ARM Cortex-A8 processor. The ARM Cortex-A8 processor is a member of ARM Cortex family of general-purpose processors. This processor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM Cortex-A8 processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM Cortex-A8 processor has a Harvard architecture and provides a complete high-performance subsystem, including:

- ARM Cortex-A8 integer core
- Superscalar ARMv7 instruction set
- Thumb-2 instruction set
- Jazelle RCT acceleration
- CP14 debug coprocessor
- CP15 system control coprocessor
- NEON 64-bit and 128-bit hybrid SIMD engine for multimedia
- Enhanced memory management unit (MMU)
- Separate level-1 instruction and data caches
- Integrated level-2 cache
- 128-bit interconnect to system memories and peripherals
- Embedded trace module (ETM).

### 3.2.2 Embedded Trace Module (ETM)

To support real-time trace, the ARM Cortex-A8 processor provides an interface to enable connection of an embedded trace module (ETM). The ETM consists of two parts:

- The Trace port provides real-time trace capability for the ARM Cortex-A8.
- Triggering facilities provide trigger resources, which include address and data comparators, counter, and sequencers.

The ARM Cortex-A8 trace port is connected to the system-level embedded trace buffer (ETB). The ETB has a 32KB buffer memory. ETB enabled debug tools are required to read and interpret the captured trace data.

For more details on the ETB, see Section 9.4.2.

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### 3.2.3 ARM Cortex-A8 Interrupt Controller (AINTC)

The ARM Cortex-A8 subsystem contains an interrupt controller (AINTC) that prioritizes all service requests from the system peripherals and generates either IRQ or FIQ to the ARM Cortex-A8 processor. For more details on the AINTC, see Section 8.4.

### 3.2.4 System Interconnect

The ARM Cortex-A8 processor in connected through the arbiter to both an L3 interconnect port and a DMM port. The DMM port is 128-bits wide and provides the ARM Cortex-A8 direct access to the DDR memories, while the L3 interconnect port is 64-bits wide and provides access to the remaining device modules.


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## 3.3 DSP Subsystem

The DSP Subsystem includes the following features:

- C674x DSP CPU
- 32KB L1 Program (L1P) and Cache (up to 32KB) with Error Detection Code (EDC)
- 32KB L1 Data (L1D) and Cache (up to 32KB)
- 256KB L2 Unified Mapped RAM and Cache with Error Correction Code (ECC)
- Direct Connection to the HDVICP2 Host SL2 Port for HDVICP2-0 and HDVICP2-1
- Little endian

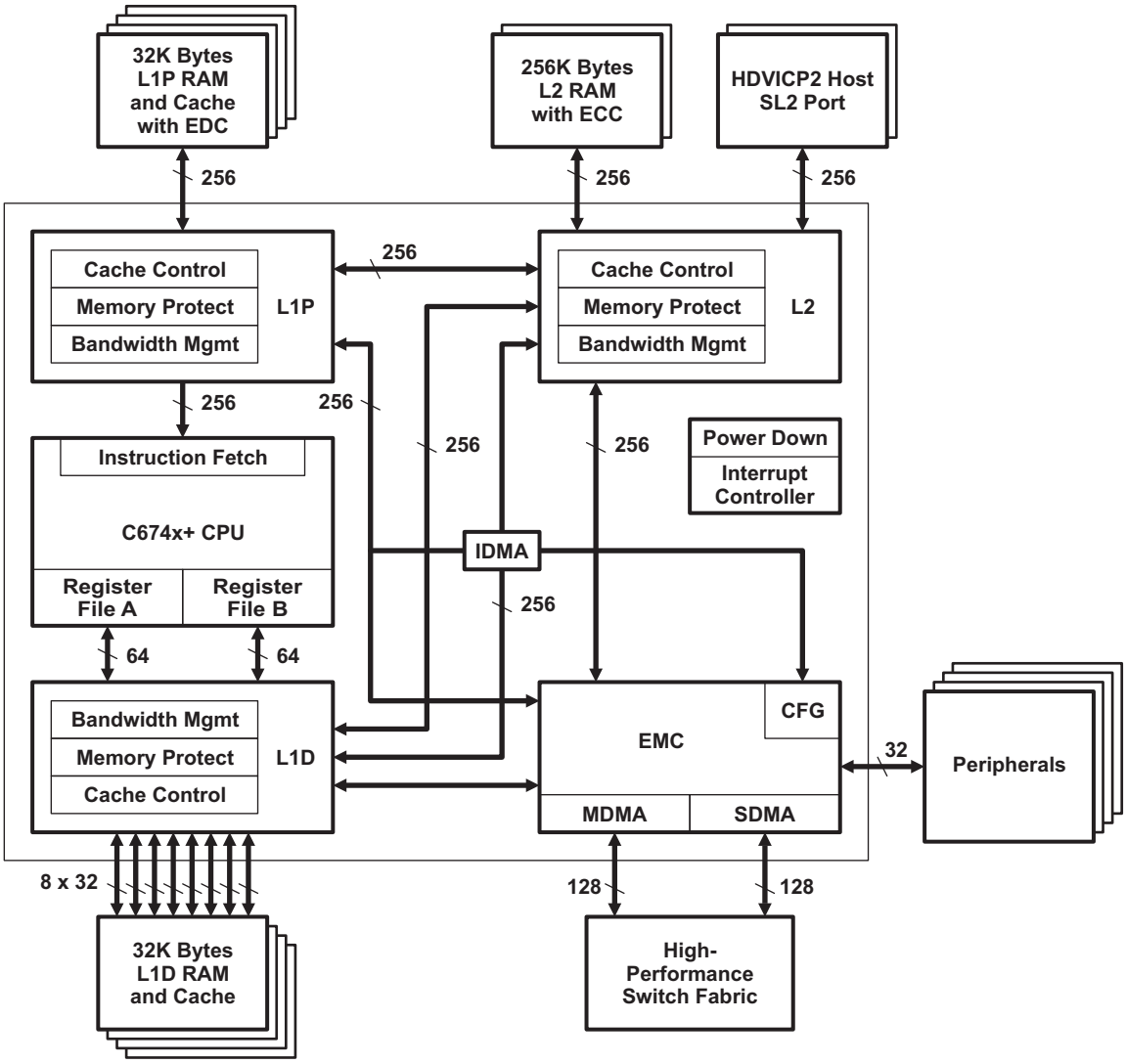


**Figure 3-2. C674x Megamodule Block Diagram**

### 3.3.1 C674x DSP CPU Description

The C674x central processing unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 3-3. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C674x CPU combines the performance of the C64x+ core with the floating-point capabilities of the C67x+ core.

Each C674x .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add and subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add and subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes for 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add and subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C674x core enhances the .S unit in several ways. On the previous cores, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C674x core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit and 16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C674x compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C674x CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.


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- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C674x CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C674x DSP CPU and Instruction Set User's Guide* (literature number SPRUFE8)
- *TMS320C674x DSP Megamodule Reference Guide* (literature number SPRUFK5)

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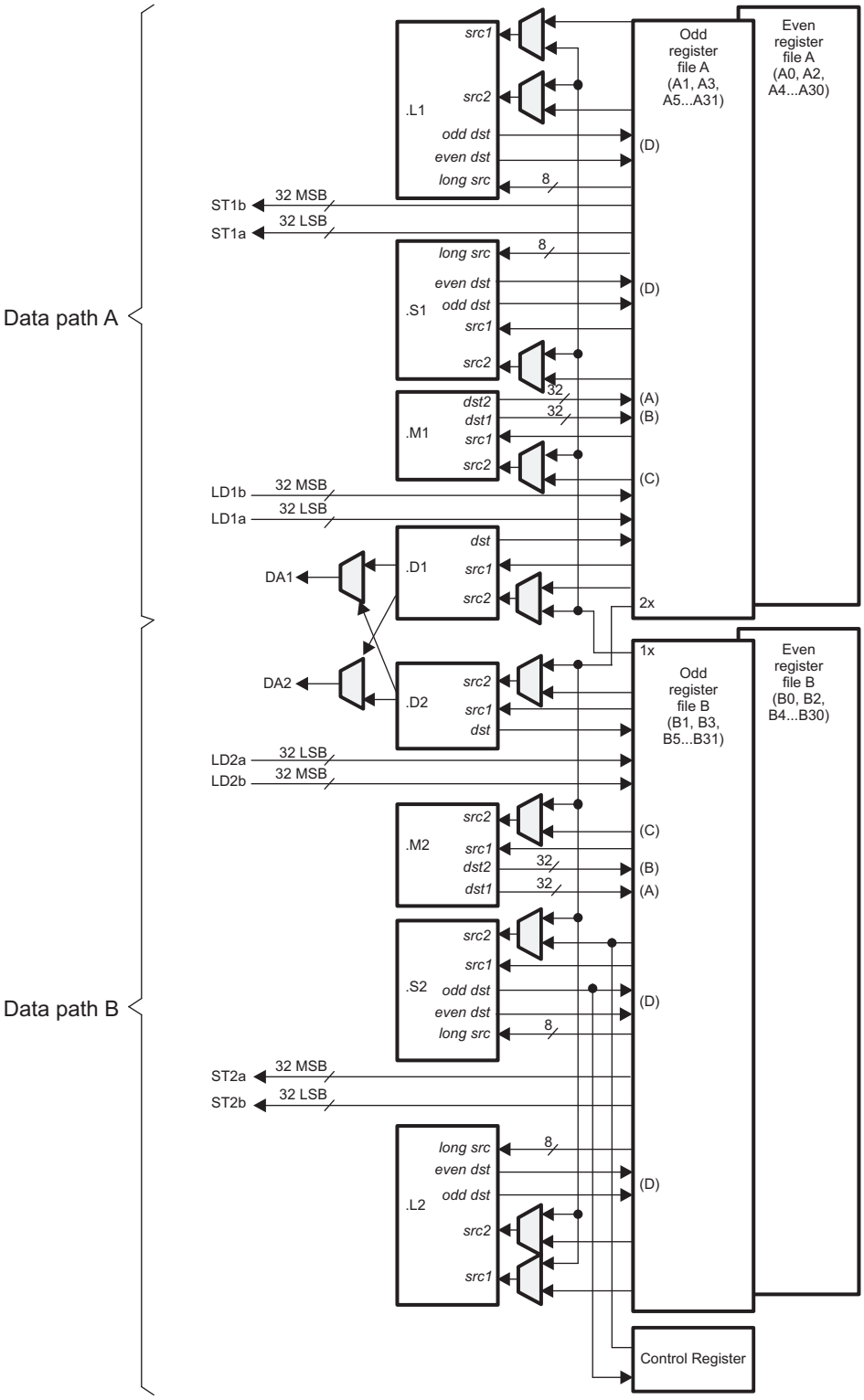


A. .M unit, *dst2* is 32 MSB.
B On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and even *dst* connects to even register files

**Figure 3-3. TMS320C674x CPU (DSP Core) Data Paths**


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### 3.3.2 System Memory Management Unit (System MMU)

All C674x DSP accesses through the MDMA port are directed through the system memory management unit (System MMU) module where they are remapped to physical system addresses. This protects the ARM Cortex-A8 memory regions from accidental corruption by C674x code and allows for direct allocation of buffers in user space without the need for translation between ARM and DSP applications.

In addition, accesses by the EDMA TC0 may optionally be routed through the System MMU. This allows EDMA Channel 0 to be used by the DSP to perform transfers using only the known virtual addresses of the associated buffers. The MMU_CFG register in the Control Module is used to enable and disable use of the DSP EDMA MMU by the EDMA TC.

For details on the System MMU features and registers, see the System MMU chapter of the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

#### 3.3.2.1 System MMU Registers

Table 3-3 lists the System MMU registers.

**Table 3-3. System MMU Registers Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4801 0000h | MMU_REVISION | Revision |
| 0x4801 0010h | MMU_SYSCONFIG | Configuration |
| 0x4801 0014h | MMU_SYSSTATUS | Status |
| 0x4801 0018h | MMU_IRQSTATUS | IRQ Status |
| 0x4801 001Ch | MMU_IRQENABLE | IRQ Enable |
| 0x4801 0040h | MMU_WALKING_ST | Table Walking Logic |
| 0x4801 0044h | MMU_CNTL | Control |
| 0x4801 0048h | MMU_FAULT_AD | Fault Address |
| 0x4801 004Ch | MMU_TTB | Translation Table Base Address |
| 0x4801 0050h | MMU_LOCK | Lock |
| 0x4801 0054h | MMU_LD_TLB | Load |
| 0x4801 0058h | MMU_CAM | CAM |
| 0x4801 005Ch | MMU_RAM | RAM |
| 0x4801 0060h | MMU_GFLUSH | Global Flush |
| 0x4801 0064h | MMU_FLUSH_ENTRY | Flush Entry |
| 0x4801 0068h | MMU_READ_CAM | Read CAM |
| 0x4801 006Ch | MMU_READ_RAM | Read RAM |
| 0x4801 0070h | MMU_EMU_FAULT_AD | EMU Fault Address |
| 0x4801 0080h | MMU_FAULT_PC | Fault Program Counter |

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## 3.4 Media Controller

The Media Controller has the responsibility of managing the HDVPSS and HDVICP2 modules.

## 3.5 High-Definition Video Image Coprocessor 2 (HDVICP2)

The HDVICP2 is a video encoder and decoder hardware accelerator supporting a range of encode and decode operations at up to 1080p60 for most major video codec standards. Transcode operations are also supported. The main video codec standards supported in hardware are MPEG1, MPEG2 and MPEG4 ASP and SP, H.264 BL, MP, and HP, VC-1 SP, MP, and AP, RV9 and RV10, AVS-1.0, and ON2 VP6.2 and VP7. The HDVICP2 hardware accelerator is composed of the following elements:

- Motion estimation acceleration engine
- Loop filter acceleration engine
- Two RISC processors and associated memory used for algorithmic decision making and control
- Intra-prediction estimation engine
- Calculation engine
- Motion compensation engine
- Entropy coder and decoder
- Video DMA
- Synchronization boxes
- Shared L2 controller
- Local interconnect.

## 3.6 Inter-Processor Communication

This device is a multi-core device that requires software to efficiently manage and communicate between the cores. The following are the main features that need to be implemented by such software:

1. Device management of the slave processors from the host processor.
2. Inter-processor communication between the cores for transfer and exchange of information between them.

On this device, the host processor is usually the ARM Cortex-A8. This processor is responsible for bootloading the slave processors (C674x). Bootloading includes power management of the slaves (powerup and powerdown and other power management), reset control (reset and release of the slave processor) and setting the entry point of the slave executable into the appropriate register. This device has a power-on reset (POR) and warm reset. For the POR reset, the ARM Cortex-A8 is taken out of reset and it boots from its boot ROM. Once booted, the ARM Cortex-A8 bootloads the C674x processor.

For implementing efficient inter-processor communication between the multiple cores on the device, the following hardware features are provided:

- Mailbox interrupts
- Hardware spinlocks

Mailboxes provide a mechanism for one processor to write a value to a register and send an interrupt to another processor. Spinlocks facilitate access to shared resources in the system.

### *3.6.1 Mailbox Module*

The device Mailbox module facilitates communication between the ARM Cortex-A8, C674x DSP, and the Media Controller. It consists of twelve mailboxes, each supporting communication between two of the above processors. The sender sends information to the receiver by writing a message to the mailbox registers. Interrupt signaling is used to notify the receiver that a message has been queued or to notify the sender about an overflow situation.

The Mailbox module supports the following features (see Figure 3-4):

- 12 mailboxes


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- Four-message FIFO depth for each message queue
- 32-bit message width
- Message reception and queue-not-full notification using interrupts
- Four interrupts (one to ARM Cortex-A8, one to C674x, two to Media Controller).

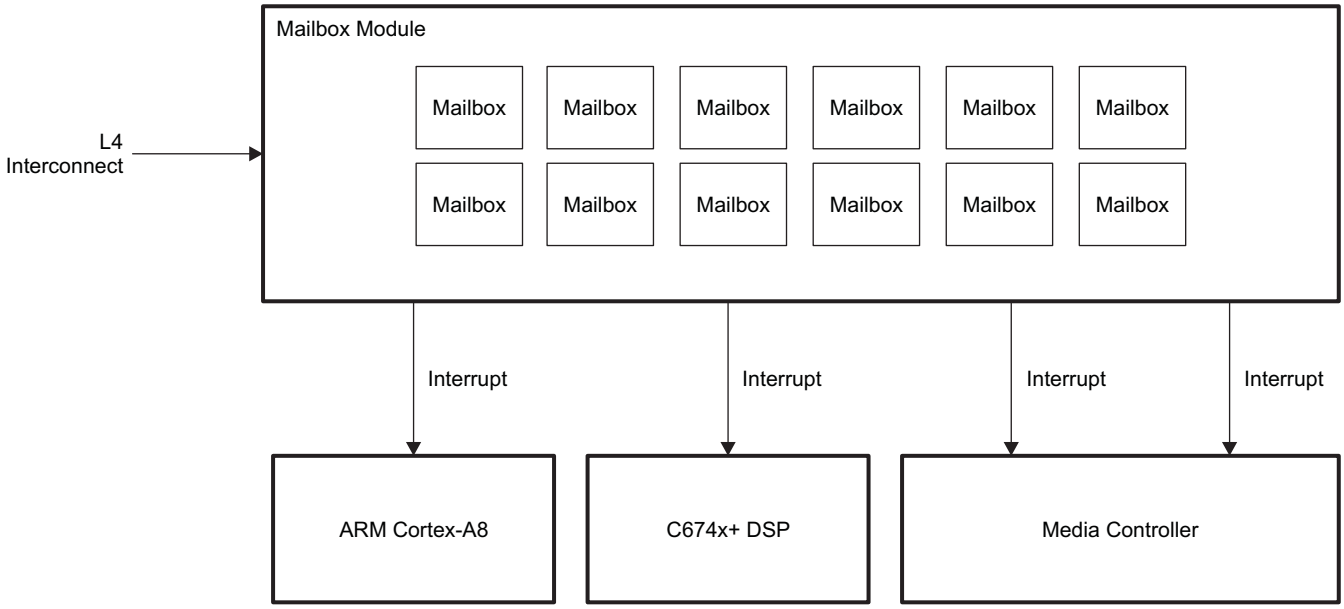


**Figure 3-4. Mailbox Module Block Diagram**

### 3.6.1.1 Mailbox Registers

Table 3-4 lists the Mailboxes available on this device. The register set below is applicable to these mailboxes. Table 3-5 lists the Mailbox registers.

**Table 3-4. Mailboxes**

| MAILBOX TYPE | USER NUMBER (u) | MAILBOX NUMBER (m) | MESSAGES PER MAILBOX |
|---|---|---|---|
| System Mailbox | 0 to 3 | 0 to 11 | 4 |
| HDVICP2-0 Mailbox | 0 to 3 | 0 to 5 | 4 |
| HDVICP2-1Mailbox | 0 to 3 | 0 to 5 | 4 |
| HDVICP2-2 Mailbox | 0 to 3 | 0 to 5 | 4 |

**Table 3-5. Mailbox Registers Summary(1)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x480C 8000 | MAILBOX_REVISION | Mailbox Revision |
| 0x480C 8010 | MAILBOX_SYSCONFIG | Mailbox System Configuration |
| 0x480C 8040 + (0x4 * m) | MAILBOX_MESSAGE_m | Mailbox Message |
| 0x480C 8080 + (0x4 * m) | MAILBOX_FIFOSTATUS_m | Mailbox FIFO Status |
| 0x480C 80C0 + (0x4 * m) | MAILBOX_MSGSTATUS_m | Mailbox Message Status |
| 0x480C 8100 + (0x10 * u) | MAILBOX_IRQSTATUS_RAW_u | Mailbox IRQ RAW Status |
| 0x480C 8104 + (0x10 * u) | MAILBOX_IRQSTATUS_CLR_u | Mailbox IRQ Clear Status |
| 0x480C 8108 + (0x10 * u) | MAILBOX_IRQENABLE_SET_u | Mailbox IRQ Enable Set |
| 0x480C 810C + (0x10 * u) | MAILBOX_IRQENABLE_CLR_u | Mailbox IRQ Enable Clear |
| 0x480C 8140 | - | Reserved |

(1) For the range of m and u, see Table 3-4.

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### 3.6.2 Spinlock Module

The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device:

- ARM Cortex-A8 processor
- C674x DSP
- Media Controller processors.

The Spinlock module implements 64 spinlocks (or hardware semaphores) that provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need for a read-modify-write bus transfer of which the programmable cores are not capable.

#### 3.6.2.1 Spinlock Registers

**Table 3-6. Spinlock Registers Summary(1)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x480C A000 | SPINLOCK_REV | Revision |
| 0x480C A010h | SPINLOCK_SYSCFG | System Configuration |
| 0x480C A014h | SPINLOCK_SYSSTAT | System Status |
| 0x480C A800 + (0x4*i) | SPINLOCK_LOCK_REG_i | Lock |

(1) i = 0 to 63

## 3.7 Power, Reset and Clock Management (PRCM) Module

The PRCM module is the centralized management module for the power, reset, and clock control signals of the device. It interfaces with all the components on the device for power, clock, and reset management through power-control signals. It integrates enhanced features to allow the device to adapt energy consumption dynamically, according to changing application and performance requirements. The innovative hardware architecture allows a substantial reduction in leakage current.

The PRCM module is composed of two main entities:

- Power reset manager (PRM): Handles the power, reset, wake-up management, and system clock source control (oscillator)
- Clock manager (CM): Handles the clock generation, distribution, and management.

Table 3-7 lists the physical addresses of the PRM and CM modules. Table 3-8 through Table 3-25 provide register mapping summaries of the PRM and CM registers.

For more details on the PRCM, see Section 8 of this data sheet, *Power, Reset, Clocking and Interrupts*, and the PRCM chapter of the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

**Table 3-7. PRCM Register Address Summary**

| ADDRESS OFFSET | MODULE NAME | SIZE | SEE |
|---|---|---|---|
| 0x0000 | PRM_DEVICE | 256 Bytes | Table 3-8 |
| 0x0100 | CM_DEVICE | 256 Bytes | Table 3-9 |
| 0x0300 | CM_DPLL | 256 Bytes | Table 3-11 |
| 0x0400 | CM_ACTIVE | 256 Bytes | Table 3-12 |
| 0x0500 | CM_DEFAULT | 256 Bytes | Table 3-13 |
| 0x0600 | CM_IVAHD0 | 256 Bytes | Table 3-14 |
| 0x0700 | CM_IVAHD1 | 256 Bytes | Table 3-15 |
| 0x0800 | CM_IVAHD2 | 256 Bytes | Table 3-16 |
| 0x0900 | CM_SGX | 256 Bytes | Table 3-17 |
| 0x0A00 | PRM_ACTIVE | 256 Bytes | Table 3-18 |


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**Table 3-7. PRCM Register Address Summary (continued)**

| ADDRESS OFFSET | MODULE NAME | SIZE | SEE |
|---|---|---|---|
| 0x0B00 | PRM_DEFAULT | 256 Bytes | Table 3-19 |
| 0x0C00 | PRM_IVAHD0 | 256 Bytes | Table 3-20 |
| 0x0D00 | PRM_IVAHD1 | 256 Bytes | Table 3-21 |
| 0x0E00 | PRM_IVAHD2 | 256 Bytes | Table 3-22 |
| 0x0F00 | PRM_SGX | 256 Bytes | Table 3-23 |
| 0x1400 | CM_ALWON | 1 KBytes | Table 3-24 |
| 0x1800 | PRM_ALWON | 1 KBytes | Table 3-25 |

**Table 3-8. PRM_DEVICE Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 00A0 | PRM_RSTCTRL | Global software cold and warm reset control |
| 0x4818 00A4 | PRM_RSTTIME | Reset duration control |
| 0x4818 00A8 | PRM_RSTST | Global reset sources log |

**Table 3-9. CM_DEVICE Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0100 | CM_CLKOUT_CTRL | SYS_CCCLKOUT output control |

**Table 3-10. OCP_SOCKET_PRM Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0200 | REVISION_PRM | PRCM IP revision code |

**Table 3-11. CM_DPLL Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0300 | CM_SYSCLK1_CLKSEL | SYSCLK1 clock divider value select |
| 0x4818 0304 | CM_SYSCLK2_CLKSEL | SYSCLK2 clock divider value select |
| 0x4818 0308 | CM_SYSCLK3_CLKSEL | SYSCLK3 clock divider value select |
| 0x4818 030C | CM_SYSCLK4_CLKSEL | SYSCLK4 clock divider value select |
| 0x4818 0310 | CM_SYSCLK5_CLKSEL | SYSCLK5 clock divider value select |
| 0x4818 0314 | CM_SYSCLK6_CLKSEL | SYSCLK6 clock divider value select |
| 0x4818 0318 | CM_SYSCLK7_CLKSEL | SYSCLK7 clock divider value select |
| 0x4818 0324 | CM_SYSCLK10_CLKSEL | SYSCLK10 clock divider value select |
| 0x4818 032C | CM_SYSCLK11_CLKSEL | SYSCLK11 clock divider value select |
| 0x4818 0334 | CM_SYSCLK13_CLKSEL | SYSCLK13 clock divider value select |
| 0x4818 0338 | CM_SYSCLK15_CLKSEL | SYSCLK15 clock divider value select |
| 0x4818 0340 | CM_VPB3_CLKSEL | Video PLL B3 clock divider value select |
| 0x4818 0344 | CM_VPC1_CLKSEL | Video PLL C1 clock divider value select |
| 0x4818 0348 | CM_VPD1_CLKSEL | Video PLL D1 clock divider value select |
| 0x4818 034C | CM_SYSCLK19_CLKSEL | SYSCLK19 clock divider value select |
| 0x4818 0350 | CM_SYSCLK20_CLKSEL | SYSCLK20 clock divider value select |
| 0x4818 0354 | CM_SYSCLK21_CLKSEL | SYSCLK21 clock divider value select |
| 0x4818 0358 | CM_SYSCLK22_CLKSEL | SYSCLK22 clock divider value select |
| 0x4818 035C | CM_APA_CLKSEL | Audio PLL A clock divider value select |
| 0x4818 0370 | CM_SYSCLK14_CLKSEL | SYSCLK14 clock mux select line |
| 0x4818 0374 | CM_SYSCLK16_CLKSEL | SYSCLK16 clock mux select line |
| 0x4818 0378 | CM_SYSCLK18_CLKSEL | SYSCLK18 clock mux select line |

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**Table 3-11. CM_DPLL Register Summary (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 037C | CM_AUDIOCLK_MCASP0_CLKSEL | McASP0 audio clock mux select line |
| 0x4818 0380 | CM_AUDIOCLK_MCASP1_CLKSEL | McASP1 audio clock mux select line |
| 0x4818 0384 | CM_AUDIOCLK_MCASP2_CLKSEL | McASP2 audio clock mux select line |
| 0x4818 0388 | CM_AUDIOCLK_MCBSP_CLKSEL | McBSP audio clock mux select line |
| 0x4818 0390 | CM_TIMER1_CLKSEL | Timer1 clock mux select line |
| 0x4818 0394 | CM_TIMER2_CLKSEL | Timer2 clock mux select line |
| 0x4818 0398 | CM_TIMER3_CLKSEL | Timer3 clock mux select line |
| 0x4818 039C | CM_TIMER4_CLKSEL | Timer4 clock mux select line |
| 0x4818 03A0 | CM_TIMER5_CLKSEL | Timer5 clock mux select line |
| 0x4818 03A4 | CM_TIMER6_CLKSEL | Timer6 clock mux select line |
| 0x4818 03A8 | CM_TIMER7_CLKSEL | Timer7 clock mux select line |
| 0x4818 03B0 | CM_SYSCLK23_CLKSEL | SYSCLK23 clock divider value select |
| 0x4818 03B4 | CM_SYSCLK24_CLKSEL | SYSCLK24 clock divider value select |

**Table 3-12. CM_ACTIVE Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0400 | CM_GEM_CLKSTCTRL | DSP clock domain power state transition |
| 0x4818 0404 | CM_HDDSS_CLKSTCTRL | HDVPSS clock domain power state transition |
| 0x4818 0408 | CM_HDMI_CLKSTCTRL | HDMI clock domain power state transition |
| 0x4818 0420 | CM_ACTIVE_GEM_CLKCTRL | DSP clock management control |
| 0x4818 0424 | CM_ACTIVE_HDDSS_CLKCTRL | HDVPSS clock management control |
| 0x4818 0428 | CM_ACTIVE_HDMI_CLKCTRL | HDMI clock management control |

**Table 3-13. CM_DEFAULT Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0504 | CM_DEFAULT_L3_MED_CLKSTCTRL | L3 clock domain power state transition |
| 0x4818 0508 | CM_DEFAULT_L3_FAST_CLKSTCTRL | L3 clock domain power state transition |
| 0x4818 0510 | CM_DEFAULT_PCI_CLKSTCTRL | PCI clock domain power state transition |
| 0x4818 0514 | CM_DEFAULT_L3_SLOW_CLKSTCTRL | L3 clock domain power state transition |
| 0x4818 0520 | CM_DEFAULT_EMIF_0_CLKCTRL | EMIF0 clock management control |
| 0x4818 0524 | CM_DEFAULT_EMIF_1_CLKCTRL | EMIF1 clock management control |
| 0x4818 0528 | CM_DEFAULT_DMM_CLKCTRL | DMM clock management control |
| 0x4818 052C | CM_DEFAULT_FW_CLKCTRL | EMIF FW clock management control |
| 0x4818 0558 | CM_DEFAULT_USB_CLKCTRL | USB clock management control |
| 0x4818 0560 | CM_DEFAULT_SATA_CLKCTRL | SATA clock management control |
| 0x4818 0578 | CM_DEFAULT_PCI_CLKCTRL | PCI clock management control |

**Table 3-14. CM_IVAHD0 Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0600 | CM_IVAHD0_CLKSTCTRL | HDVICP2-0 clock domain power state transition |
| 0x4818 0620 | CM_IVAHD0_IVAHD_CLKCTRL | HDVICP2-0 clock management control |
| 0x4818 0624 | CM_IVAHD0_SL2_CLKCTRL | HDVICP2-0 SL2 clock management control |


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**Table 3-15. CM_IVAHD1 Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0700 | CM_IVAHD1_CLKSTCTRL | HDVICP2-1 clock domain power state transition |
| 0x4818 0720 | CM_IVAHD1_IVAHD_CLKCTRL | HDVICP2-1 clock management control |
| 0x4818 0724 | CM_IVAHD1_SL2_CLKCTRL | HDVICP2-1 SL2 clock management control |

**Table 3-16. CM_IVAHD2 Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0800 | CM_IVAHD2_CLKSTCTRL | HDVICP2-2 clock domain power state transition |
| 0x4818 0820 | CM_IVAHD2_IVAHD_CLKCTRL | HDVICP2-2 clock management control |
| 0x4818 0824 | CM_IVAHD2_SL2_CLKCTRL | HDVICP2-2 SL2 clock management control |

**Table 3-17. CM_SGX Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0900 | CM_SGX_CLKSTCTRL | SGX530 clock domain power state transition |
| 0x4818 0920 | CM_SGX_SGX_CLKCTRL | SGX530 clock management control |

**Table 3-18. PRM_ACTIVE Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0A00 | PM_ACTIVE_PWRSTCTRL | Active power state control |
| 0x4818 0A04 | PM_ACTIVE_PWRSTST | Active power domain state status |
| 0x4818 0A10 | RM_ACTIVE_RSTCTRL | Active domain reset control release |
| 0x4818 0A14 | RM_ACTIVE_RSTST | Active domain reset source log |

**Table 3-19. PRM_DEFAULT Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0B00 | PM_DEFAULT_PWRSTCTRL | Default power state |
| 0x4818 0B04 | PM_DEFAULT_PWRSTST | Default power domain state 0 status |
| 0x4818 0B10 | RM_DEFAULT_RSTCTRL | Default subsystem reset control release |
| 0x4818 0B14 | RM_DEFAULT_RSTST | Default domain reset source log |

**Table 3-20. PRM_IVAHD0 Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0C00 | PM_IVAHD0_PWRSTCTRL | HDVICP2-0 power state control |
| 0x4818 0C04 | PM_IVAHD0_PWRSTST | HDVICP2-0 power domain state status |
| 0x4818 0C10 | RM_IVAHD0_RSTCTRL | HDVICP2-0 subsystem reset control release |
| 0x4818 0C14 | RM_IVAHD0_RSTST | HDVICP2-0 domain reset source log |

**Table 3-21. PRM_IVAHD1 Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0D00 | PM_IVAHD1_PWRSTCTRL | HDVICP2-1 power state control |
| 0x4818 0D04 | PM_IVAHD1_PWRSTST | HDVICP2-1 power domain state status |
| 0x4818 0D10 | RM_IVAHD1_RSTCTRL | HDVICP2-1 subsystem reset control release |
| 0x4818 0D14 | RM_IVAHD1_RSTST | HDVICP2-1 domain reset source log |

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### Table 3-22. PRM_IVAHD2 Register Summary

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0E00 | PM_IVAHD2_PWRSTCTRL | HDVICP2-2 power state control |
| 0x4818 0E04 | PM_IVAHD2_PWRSTST | HDVICP2-2 power domain state status |
| 0x4818 0E10 | RM_IVAHD2_RSTCTRL | HDVICP2-2 subsystem reset control release |
| 0x4818 0E14 | RM_IVAHD2_RSTST | HDVICP2-2 domain reset source log |

### Table 3-23. PRM_SGX Register Summary

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 0F00 | PM_SGX_PWRSTCTRL | SGX530 power state control |
| 0x4818 0F04 | RM_SGX_RSTCTRL | SGX530 domain reset control release |
| 0x4818 0F10 | PM_SGX_PWRSTST | SGX530 power domain state status |
| 0x4818 0F14 | RM_SGX_RSTST | SGX530 domain reset source log |

### Table 3-24. CM_ALWON Register Summary

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 1400 | CM_ALWON_L3_SLOW_CLKSTCTRL | L3 clock domain power state transition |
| 0x4818 1404 | CM_ETHERNET_CLKSTCTRL | EMAC clock domain power state transition |
| 0x4818 1408 | CM_ALWON_L3_MED_CLKSTCTRL | L3 clock domain power state transition |
| 0x4818 140C | CM_MMU_CLKSTCTRL | MMU clock domain power state transition |
| 0x4818 1410 | CM_MMUCFG_CLKSTCTRL | MMU CFG clock domain power state transition |
| 0x4818 1414 | CM_ALWON_OCMC_0_CLKSTCTRL | OCMC 0 clock domain power state transition |
| 0x4818 1418 | CM_ALWON_OCMC_1_CLKSTCTRL | OCMC 1 clock domain power state transition |
| 0x4818 141C | CM_ALWON_MPU_CLKSTCTRL | Processor clock domain power state transition |
| 0x4818 1420 | CM_ALWON_SYSCLK4_CLKSTCTRL | SYSCLK4 clock domain power state transition |
| 0x4818 1424 | CM_ALWON_SYSCLK5_CLKSTCTRL | SYSCLK5 clock domain power state transition |
| 0x4818 1428 | CM_ALWON_SYSCLK6_CLKSTCTRL | SYSCLK6 clock domain power state transition |
| 0x4818 142C | CM_ALWON_RTC_CLKSTCTRL | RTC clock domain power state transition |
| 0x4818 1430 | CM_ALWON_L3_FAST_CLKSTCTRL | L3 clock domain power state transition |
| 0x4818 1540 | CM_ALWON_MCASP0_CLKCTRL | McASP 0 clock management control |
| 0x4818 1544 | CM_ALWON_MCASP1_CLKCTRL | McASP 1 clock management control |
| 0x4818 1548 | CM_ALWON_MCASP2_CLKCTRL | McASP 2 clock management control |
| 0x4818 154C | CM_ALWON_MCBSP_CLKCTRL | McBSP clock management control |
| 0x4818 1550 | CM_ALWON_UART_0_CLKCTRL | UART 0 clock management control |
| 0x4818 1554 | CM_ALWON_UART_1_CLKCTRL | UART 1 clock management control |
| 0x4818 1558 | CM_ALWON_UART_2_CLKCTRL | UART 2 clock management control |
| 0x4818 155C | CM_ALWON_GPIO_0_CLKCTRL | GPIO 0 clock management control |
| 0x4818 1560 | CM_ALWON_GPIO_1_CLKCTRL | GPIO 1 clock management control |
| 0x4818 1564 | CM_ALWON_I2C_0_CLKCTRL | I2C 0 clock management control |
| 0x4818 1568 | CM_ALWON_I2C_1_CLKCTRL | I2C 1 clock management control |
| 0x4818 1570 | CM_ALWON_TIMER_1_CLKCTRL | Timer1 clock management control |
| 0x4818 1574 | CM_ALWON_TIMER_2_CLKCTRL | Timer2 clock management control |
| 0x4818 1578 | CM_ALWON_TIMER_3_CLKCTRL | Timer3 clock management control |
| 0x4818 157C | CM_ALWON_TIMER_4_CLKCTRL | Timer4 clock management control |
| 0x4818 1580 | CM_ALWON_TIMER_5_CLKCTRL | Timer5 clock management control |
| 0x4818 1584 | CM_ALWON_TIMER_6_CLKCTRL | Timer6 clock management control |
| 0x4818 1588 | CM_ALWON_TIMER_7_CLKCTRL | Timer7 clock management control |
| 0x4818 158C | CM_ALWON_WDTIMER_CLKCTRL | WDTIMER clock management control |
| 0x4818 1590 | CM_ALWON_SPI_CLKCTRL | SPI clock management control |


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**Table 3-24. CM_ALWON Register Summary (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 1594 | CM_ALWON_MAILBOX_CLKCTRL | MAILBOX clock management control |
| 0x4818 1598 | CM_ALWON_SPINBOX_CLKCTRL | SPINBOX clock management control |
| 0x4818 159C | CM_ALWON_MMUDATA_CLKCTRL | MMU DATA clock management control |
| 0x4818 15A8 | CM_ALWON_MMUCFG_CLKCTRL | MMU CFG clock management control |
| 0x4818 15B0 | CM_ALWON_SDIO_CLKCTRL | SDIO clock management control |
| 0x4818 15B4 | CM_ALWON_OCMC_0_CLKCTRL | OCMC 0 clock management control |
| 0x4818 15B8 | CM_ALWON_OCMC_1_CLKCTRL | OCMC 1 clock management control |
| 0x4818 15C4 | CM_ALWON_CONTROL_CLKCTRL | Control clock management control |
| 0x4818 15D0 | CM_ALWON_GPMC_CLKCTRL | GPMC clock management control |
| 0x4818 15D4 | CM_ALWON_ETHERNET_0_CLKCTRL | Ethernet 0 clock management control |
| 0x4818 15D8 | CM_ALWON_ETHERNET_1_CLKCTRL | Ethernet 1 clock management control |
| 0x4818 15DC | CM_ALWON_MPU_CLKCTRL | Processor clock management control |
| 0x4818 15E0 | CM_ALWON_DEBUGSS_CLKCTRL | Debug clock management control |
| 0x4818 15E4 | CM_ALWON_L3_CLKCTRL | L3 clock management control |
| 0x4818 15E8 | CM_ALWON_L4HS_CLKCTRL | L4 high-speed clock management control |
| 0x4818 15EC | CM_ALWON_L4LS_CLKCTRL | L4 standard-speed clock management control |
| 0x4818 15F0 | CM_ALWON_RTC_CLKCTRL | RTC clock management control |
| 0x4818 15F4 | CM_ALWON_TPCC_CLKCTRL | TPCC clock management control |
| 0x4818 15F8 | CM_ALWON_TPTC0_CLKCTRL | TPTC0 clock management control |
| 0x4818 15FC | CM_ALWON_TPTC1_CLKCTRL | TPTC1 clock management control |
| 0x4818 1600 | CM_ALWON_TPTC2_CLKCTRL | TPTC2 clock management control |
| 0x4818 1604 | CM_ALWON_TPTC3_CLKCTRL | TPTC3 clock management control |
| 0x4818 1608 | CM_ALWON_SR_0_CLKCTRL | SmartReflex 0 clock management control |
| 0x4818 160C | CM_ALWON_SR_1_CLKCTRL | SmartReflex 1 clock management control |
| 0x4818 1628 | CM_ALWON_CUST_EFUSE_CLKCTRL | Customer e-Fuse clock management control |

**Table 3-25. PRM_ALWON Register Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4818 1810 | RM_ALWON_RSTCTRL | ALWAYS ON domain resets control |
| 0x4818 1814 | RM_ALWON_RSTST | ALWAYS ON reset sources |

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## 3.8 SGX530 (DM8168 only)

The SGX530 is a vector and 3D graphics accelerator for vector and 3-dimensional (3D) graphics applications. The SGX530 graphics accelerator efficiently processes a number of various multimedia data types concurrently:

- Pixel data
- Vertex data
- Video data.

This is achieved using a multi-threaded architecture using two levels of scheduling and data partitioning enabling zero overhead task switching.

The SGX530 has the following major features:

- Vector graphics and 3D graphics.
- Tile-based architecture.
- Universal Scalable Shader Engine (USSE) - multi-threaded engine incorporating pixel and vertex shader functionality.
- Advanced shader feature set - in excess of Microsoft VS3.0, PS3.0, and OpenGL 2.0.
- Industry standard API support - OpenGL ES 1.1 and 2.0, OpenVG v1.1.
- Fine-grained task switching, load balancing, and power management.
- Advanced geometry direct memory access (DMA) driven operation for minimum CPU interaction.
- Programmable high-quality image anti-aliasing.
- PowerVR® SGX core MMU for address translation from the core virtual address to the external physical address (up to 4GB address range).
- Fully-virtualized memory addressing for OS operation in a unified memory architecture.
- Advanced and standard 2D operations [for example, vector graphics, block level transfers (BLTs), raster operations (ROPs)].


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## 3.9 Memory Map Summary

The device has multiple on-chip memories associated with its processors and various subsystems. To help simplify software development a unified memory map is used where possible to maintain a consistent view of device resources across all bus masters.

The device system memory mapping is broken into four 1-GB quadrants for target address spaces allocation. The four quadrants are labeled Q0, Q1, Q2 and Q3 for a total of 4-GB 32-bit address space. (HDVPSS includes a thirty-third address bit for an additional 4GB of address range; this is for virtual addressing and not physical memory addressing.) Inside each quadrant, system targets are mapped on 4-MB boundary (except EDMA targets which are decreased to 1-MB regions).

### *3.9.1 L3 Memory Map*

The L3 high-performance interconnect is based on a Network-on-Chip (NoC) interconnect infrastructure. The NoC uses an internal packet-based protocol for forward (read command, write command with data payload) and backward (read response with data payload, write response) transactions. All exposed interfaces of this NoC interconnect, both for targets and initiators, comply with the OCPIP2.2 reference standard.

Table 3-26 shows the general device level-3 (L3) memory map. The table represents the physical addresses used by the L3 infrastructure. Some processors within the device (such as Cortex™-A8 ARM, C674x DSP) may re-map these targets to different virtual addresses through an internal or external MMU. Processors without MMUs and other bus masters use these physical addresses to access L3 regions. Note that not all masters have access to all L3 regions, but only those with defined connectivity, as shown in Table 7-1. For a list of the specific peripherals attached to each of the Level-4 (L4) peripheral ports see Section 7.2. The L3 interconnect returns an address-hole error if any initiator attempts to access a target to which it has no connection.

**Table 3-26. L3 Memory Map**

| QUAD | BLOCK NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|---|
| Q0 | GPMC | 0x0100 0000 | 0x1FFF FFFF | 496MB | GPMC(1) |
| Q0 | PCIe Gen2 | 0x2000 0000 | 0x2FFF FFFF | 256MB | PCIe Gen2 Targets |
| Q0 | Reserved | 0x3000 0000 | 0x3FFF FFFF | 256MB | Reserved |
| Q1 | Reserved | 0x4000 0000 | 0x402F FFFF | 3MB | Reserved |
| Q1 | L3 OCMC0 | 0x4030 0000 | 0x4033 FFFF | 256KB | OCMC SRAM |
| Q1 | Reserved | 0x4034 0000 | 0x403F FFFF | 768KB | Reserved (OCMC RAM0) |
| Q1 | L3 OCMC1 | 0x4040 0000 | 0x4043 FFFF | 256KB | OCMC SRAM |
| Q1 | Reserved | 0x4044 0000 | 0x404F FFFF | 768KB | Reserved (OCMC RAM1) |
| Q1 | Reserved | 0x4050 0000 | 0x407F FFFF | 3MB | Reserved |
| Q1 | C674x | 0x4080 0000 | 0x4083 FFFF | 256KB | C674x UMAP0 (L2 RAM) |
| Q1 | Reserved | 0x4084 0000 | 0x40DF FFFF | 5888KB | Reserved |
| Q1 | C674x | 0x40E0 0000 | 0x40E0 7FFF | 32KB | C674x L1P Cache and RAM |
| Q1 | Reserved | 0x40E0 8000 | 0x40EF FFFF | 992KB | Reserved |
| Q1 | C674x | 0x40F0 0000 | 0x40F0 7FFF | 32KB | C674x L1D Cache and RAM |
| Q1 | Reserved | 0x40F0 8000 | 0x40FF FFFF | 992KB | Reserved |
| Q1 | Reserved | 0x4100 0000 | 0x41FF FFFF | 16MB | Reserved |
| Q1 | Reserved | 0x4200 0000 | 0x43FF FFFF | 32MB | Reserved |
| Q1 | L3 CFG Regs | 0x4400 0000 | 0x44BF FFFF | 12MB | L3 configuration registers |
| Q1 | Reserved | 0x44C0 0000 | 0x45FF FFFF | 20MB | Reserved |

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**Table 3-26. L3 Memory Map (continued)**

| QUAD | BLOCK NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|---|
| Q1 | McASP0 | 0x4600 0000 | 0x463F FFFF | 4MB | McASP0 DAT Port Access(2) |
| Q1 | McASP1 | 0x4640 0000 | 0x467F FFFF | 4MB | McASP1 DAT Port Access(2) |
| Q1 | McASP2 | 0x4680 0000 | 0x46BF FFFF | 4MB | McASP2 DAT Port Access(2) |
| Q1 | HDMI 1.3 Tx | 0x46C0 0000 | 0x46FF FFFF | 4MB | HDMI 1.3 Tx |
| Q1 | McBSP | 0x4700 0000 | 0x473F FFFF | 4MB | McBSP |
| Q1 | USB2.0 | 0x4740 0000 | 0x477F FFFF | 4MB | USB2.0 Registers and CPPI |
| Q1 | Reserved | 0x4780 0000 | 0x47BF FFFF | 4MB | Reserved |
| Q1 | Reserved | 0x47C0 0000 | 0x47FF FFFF | 4MB | Reserved |
| Q1 | L4 Standard domain | 0x4800 0000 | 0x48FF FFFF | 16MB | Standard Peripheral domain (see Table 3-27) |
| Q1 | EDMA TPCC | 0x4900 0000 | 0x490F FFFF | 1MB | EDMA TPCC Registers |
| Q1 | Reserved | 0x4910 0000 | 0x497F FFFF | 7MB | Reserved |
| Q1 | EDMA TPTC0 | 0x4980 0000 | 0x498F FFFF | 1MB | EDMA TPTC0 Registers |
| Q1 | EDMA TPTC1 | 0x4990 0000 | 0x499F FFFF | 1MB | EDMA TPTC1 Registers |
| Q1 | EDMA TPTC2 | 0x49A0 0000 | 0x49AF FFFF | 1MB | EDMA TPTC2 Registers |
| Q1 | EDMA TPTC3 | 0x49B0 0000 | 0x49BF FFFF | 1MB | EDMA TPTC3 Registers |
| Q1 | Reserved | 0x49C0 0000 | 0x49FF FFFF | 4MB | Reserved |
| Q1 | L4 High-Speed Domain | 0x4A00 0000 | 0x4AFF FFFF | 16MB | High-Speed Peripheral domain (see Table 3-28) |
| Q1 | Instrumentation | 0x4B00 0000 | 0x4BFF FFFF | 16MB | EMU Subsystem region |
| Q1 | DDR EMIF0 registers(3) | 0x4C00 0000 | 0x4CFF FFFF | 16MB | Configuration registers |
| Q1 | DDR EMIF1 registers(3) | 0x4D00 0000 | 0x4DFF FFFF | 16MB | Configuration registers |
| Q1 | DDR DMM Registers(3) | 0x4E00 0000 | 0x4FFF FFFF | 32MB | Configuration registers |
| Q1 | GPMC Registers | 0x5000 0000 | 0x50FF FFFF | 16MB | Configuration registers |
| Q1 | PCIe Gen2 Registers | 0x5100 0000 | 0x51FF FFFF | 16MB | Configuration registers |
| Q1 | Reserved | 0x5200 0000 | 0x52FF FFFF | 16MB | Reserved |
| Q1 | HDVICP2-2 Config | 0x5300 0000 | 0x53FF FFFF | 16MB | HDVICP2-2 Host Port |
| Q1 | HDVICP2-2 SL2 | 0x5400 0000 | 0x54FF FFFF | 16MB | HDVICP2-2 SL2 Port |
| Q1 | Reserved | 0x5500 0000 | 0x55FF FFFF | 16MB | Reserved |
| Q1 | SGX530 (DM8168 only) | 0x5600 0000 | 0x56FF FFFF | 16MB | SGX530 Slave Port |
| Q1 | Reserved (DM8167 and DM8165 only) | 0x5600 0000 | 0x56FF FFFF | 16MB | Reserved |
| Q1 | Reserved | 0x5700 0000 | 0x57FF FFFF | 16MB | Reserved |
| Q1 | HDVICP2-0 Config | 0x5800 0000 | 0x58FF FFFF | 16MB | HDVICP2-0 Host Port |
| Q1 | HDVICP2-0 SL2 | 0x5900 0000 | 0x59FF FFFF | 16MB | HDVICP2-0 SL2 Port |
| Q1 | HDVICP2-1 Config | 0x5A00 0000 | 0x5AFF FFFF | 16MB | HDVICP2-1 Host Port |
| Q1 | HDVICP2-1 SL2 | 0x5B00 0000 | 0x5BFF FFFF | 16MB | HDVICP2-1 SL2 Port |
| Q1 | Reserved | 0x5C00 0000 | 0x5DFF FFFF | 32MB | Reserved |
| Q1 | Reserved | 0x5E00 0000 | 0x5FFF FFFF | 32MB | Reserved |
| Q1 | Tiler | 0x6000 0000 | 0x7FFF FFFF | 512MB | Virtual Tiled Address Space |


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**Table 3-26. L3 Memory Map (continued)**

| QUAD | BLOCK NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|---|
| Q2 | DDR EMIF0 and EMIF1 SDRAM(4) | 0x8000 0000 | 0xBFFF FFFF | 1GB | DDR |
| Q3 | DDR EMIF0 and EMIF1 SDRAM(4) | 0xC000 0000 | 0xFFFF FFFF | 1GB | DDR |
| Q4-7 | DDR DMM | 0x1 0000 0000 | 0x1 FFFF FFFF | 4GB | DDR DMM Tiler Extended address map – Virtual Views (HDVPSS only) |

(1) The first section of GPMC memory (0x0 - 0x00FF_FFFF) is reserved for BOOTROM. Accessible memory starts at location 0x0100_0000.

(2) For more information about McASP registers accessed through the DAT port, see Table 9-78.

(3) These accesses occur through the DDR DMM Tiler Ports. The DMM will split address ranges internally to address DDR EMIF and DDR DMM control registers.

(4) DDR EMIF0 and DDR EMIF1 addresses may be contiguous or bank interleaved depending on configuration of the DDR DMM; for more details, see the DDR DMM documentation.

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### 3.9.2 L4 Memory Map

#### 3.9.2.1 L4 Standard Peripheral

The L4 standard peripheral bus accesses standard peripherals and IP configuration registers. The memory map is shown in Table 3-27.

**Table 3-27. L4 Standard Peripheral Memory Map**

| DEVICE NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| L4 Standard Configuration | 0x4800 0000 | 0x4800 07FF | 2KB | Address and Protection (AP) |
| | 0x4800 0800 | 0x4800 0FFF | 2KB | Link Agent (LA) |
| | 0x4800 1000 | 0x4800 13FF | 1KB | Initiator Port (IP0) |
| | 0x4800 1400 | 0x4800 17FF | 1KB | Initiator Port (IP1) |
| | 0x4800 1800 | 0x4800 1FFF | 2KB | Reserved (IP2 – IP3) |
| Reserved | 0x4800 2000 | 0x4800 7FFF | 24KB | Reserved |
| e-Fuse Controller | 0x4800 8000 | 0x4800 8FFF | 4KB | Peripheral Registers |
| | 0x4800 9000 | 0x4800 9FFF | 4KB | Support Registers |
| Reserved | 0x4800 A000 | 0x4800 FFFF | 24KB | Reserved |
| System MMU | 0x4801 0000 | 0x4801 0FFF | 4KB | Peripheral Registers |
| | 0x4801 1000 | 0x4801 1FFF | 4KB | Support Registers |
| Reserved | 0x4801 2000 | 0x4801 FFFF | 56KB | Reserved |
| UART0 | 0x4802 0000 | 0x4802 0FFF | 4KB | Peripheral Registers |
| | 0x4802 1000 | 0x4802 1FFF | 4KB | Support Registers |
| UART1 | 0x4802 2000 | 0x4802 2FFF | 4KB | Peripheral Registers |
| | 0x4802 3000 | 0x4802 3FFF | 4KB | Support Registers |
| UART2 | 0x4802 4000 | 0x4802 4FFF | 4KB | Peripheral Registers |
| | 0x4802 5000 | 0x4802 5FFF | 4KB | Support Registers |
| Reserved | 0x4802 6000 | 0x4802 7FFF | 8KB | Reserved |
| I2C0 | 0x4802 8000 | 0x4802 8FFF | 4KB | Peripheral Registers |
| | 0x4802 9000 | 0x4802 9FFF | 4KB | Support Registers |
| I2C1 | 0x4802 A000 | 0x4802 AFFF | 4KB | Peripheral Registers |
| | 0x4802 B000 | 0x4802 BFFF | 4KB | Support Registers |
| Reserved | 0x4802 C000 | 0x4802 DFFF | 8KB | Reserved |
| TIMER1 | 0x4802 E000 | 0x4802 EFFF | 4KB | Peripheral Registers |
| | 0x4802 F000 | 0x4802 FFFF | 4KB | Support Registers |
| SPIOCP | 0x4803 0000 | 0x4803 0FFF | 4KB | Peripheral Registers |
| | 0x4803 1000 | 0x4803 1FFF | 4KB | Support Registers |
| GPIO0 | 0x4803 2000 | 0x4803 2FFF | 4KB | Peripheral Registers |
| | 0x4803 3000 | 0x4803 3FFF | 4KB | Support Registers |
| Reserved | 0x4803 4000 | 0x4803 7FFF | 16KB | Reserved |
| McASP0 CFG | 0x4803 8000 | 0x4803 9FFF | 8KB | Peripheral Registers |
| | 0x4803 A000 | 0x4803 AFFF | 4KB | Support Registers |
| Reserved | 0x4803 B000 | 0x4803 BFFF | 4KB | Reserved |
| McASP1 CFG | 0x4803 C000 | 0x4803 DFFF | 8KB | Peripheral Registers |
| | 0x4803 E000 | 0x4803 EFFF | 4KB | Support Registers |
| Reserved | 0x4803 F000 | 0x4803 FFFF | 4KB | Reserved |
| TIMER2 | 0x4804 0000 | 0x4804 0FFF | 4KB | Peripheral Registers |
| | 0x4804 1000 | 0x4804 1FFF | 4KB | Support Registers |
| TIMER3 | 0x4804 2000 | 0x4804 2FFF | 4KB | Peripheral Registers |
| | 0x4804 3000 | 0x4804 3FFF | 4KB | Support Registers |


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**Table 3-27. L4 Standard Peripheral Memory Map (continued)**

| DEVICE NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| TIMER4 | 0x4804 4000 | 0x4804 4FFF | 4KB | Peripheral Registers |
| | 0x4804 5000 | 0x4804 5FFF | 4KB | Support Registers |
| TIMER5 | 0x4804 6000 | 0x4804 6FFF | 4KB | Peripheral Registers |
| | 0x4804 7000 | 0x4804 7FFF | 4KB | Support Registers |
| TIMER6 | 0x4804 8000 | 0x4804 8FFF | 4KB | Peripheral Registers |
| | 0x4804 9000 | 0x4804 9FFF | 4KB | Support Registers |
| TIMER7 | 0x4804 A000 | 0x4804 AFFF | 4KB | Peripheral Registers |
| | 0x4804 B000 | 0x4804 BFFF | 4KB | Support Registers |
| GPIO1 | 0x4804 C000 | 0x4804 CFFF | 4KB | Peripheral Registers |
| | 0x4804 D000 | 0x4804 DFFF | 4KB | Support Registers |
| Reserved | 0x4804 E000 | 0x4804 FFFF | 8KB | Reserved |
| McASP2 CFG | 0x4805 0000 | 0x4805 1FFF | 8KB | Peripheral Registers |
| | 0x4805 2000 | 0x4805 2FFF | 4KB | Support Registers |
| Reserved | 0x4805 3000 | 0x4805 FFFF | 52KB | Reserved |
| SD and SDIO | 0x4806 0000 | 0x4806 FFFF | 64KB | Registers |
| | 0x4807 0000 | 0x4807 0FFF | 4KB | Support Registers |
| Reserved | 0x4807 1000 | 0x4807 FFFF | 60KB | Reserved |
| ELM | 0x4808 0000 | 0x4808 FFFF | 64KB | Error Location Module |
| | 0x4809 0000 | 0x4809 0FFF | 4KB | Support Registers |
| Reserved | 0x4809 1000 | 0x480B FFFF | 188KB | Reserved |
| RTC | 0x480C 0000 | 0x480C 0FFF | 4KB | Peripheral Registers |
| | 0x480C 1000 | 0x480C 1FFF | 4KB | Support Registers |
| WDT1 | 0x480C 2000 | 0x480C 2FFF | 4KB | Peripheral Registers |
| | 0x480C 3000 | 0x480C 3FFF | 4KB | Support Registers |
| Reserved | 0x480C 4000 | 0x480C 7FFF | 16KB | Reserved |
| Mailbox | 0x480C 8000 | 0x480C 8FFF | 4KB | Peripheral Registers |
| | 0x480C 9000 | 0x480C 9FFF | 4KB | Support Registers |
| Spinlock | 0x480C A000 | 0x480C AFFF | 4KB | Peripheral Registers |
| | 0x480C B000 | 0x480C BFFF | 4KB | Support Registers |
| Reserved | 0x480C C000 | 0x480F FFFF | 208KB | Reserved |
| HDVPSS | 0x4810 0000 | 0x4811 FFFF | 128KB | Peripheral Registers |
| | 0x4812 0000 | 0x4812 0FFF | 4KB | Support Registers |
| Reserved | 0x4812 1000 | 0x4812 1FFF | 4KB | Reserved |
| HDMI 1.3 Tx | 0x4812 2000 | 0x4812 2FFF | 4KB | Peripheral Registers |
| | 0x4812 3000 | 0x4812 3FFF | 4KB | Support Registers |
| Reserved | 0x4812 4000 | 0x4813 FFFF | 112KB | Reserved |
| Control Module | 0x4814 0000 | 0x4815 FFFF | 128KB | Peripheral Registers |
| | 0x4816 0000 | 0x4816 0FFF | 4KB | Support Registers |
| Reserved | 0x4816 1000 | 0x4817 FFFF | 124KB | Reserved |
| PRCM | 0x4818 0000 | 0x4818 2FFF | 12KB | Peripheral Registers |
| | 0x4818 3000 | 0x4818 3FFF | 4KB | Support Registers |
| Reserved | 0x4818 4000 | 0x4818 7FFF | 16KB | Reserved |
| SmartReflex0 | 0x4818 8000 | 0x4818 8FFF | 4KB | Peripheral Registers |
| | 0x4818 9000 | 0x4818 9FFF | 4KB | Support Registers |
| SmartReflex1 | 0x4818 A000 | 0x4818 AFFF | 4KB | Peripheral Registers |
| | 0x4818 B000 | 0x4818 BFFF | 4KB | Support Registers |

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**Table 3-27. L4 Standard Peripheral Memory Map (continued)**

| DEVICE NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| OCP Watchpoint | 0x4818 C000 | 0x4818 CFFF | 4KB | Peripheral Registers |
| | 0x4818 D000 | 0x4818 DFFF | 4KB | Support Registers |
| Reserved | 0x4818 E000 | 0x4818 EFFF | 4KB | Reserved |
| | 0x4818 F000 | 0x4818 FFFF | 4KB | Reserved |
| Reserved | 0x4819 0000 | 0x4819 0FFF | 4KB | Reserved |
| | 0x4819 1000 | 0x4819 1FFF | 4KB | Reserved |
| Reserved | 0x4819 2000 | 0x4819 2FFF | 4KB | Reserved |
| | 0x4819 3000 | 0x4819 3FFF | 4KB | Reserved |
| Reserved | 0x4819 4000 | 0x4819 4FFF | 4KB | Reserved |
| | 0x4819 5000 | 0x4819 5FFF | 4KB | Reserved |
| Reserved | 0x4819 6000 | 0x4819 6FFF | 4KB | Reserved |
| | 0x4819 7000 | 0x4819 7FFF | 4KB | Reserved |
| DDR0 Phy Ctrl Regs | 0x4819 8000 | 0x4819 8FFF | 4KB | Peripheral Registers |
| | 0x4819 9000 | 0x4819 9FFF | 4KB | Support Registers |
| DDR1 Phy Ctrl Regs | 0x4819 A000 | 0x4819 AFFF | 4KB | Peripheral Registers |
| | 0x4819 B000 | 0x4819 BFFF | 4KB | Support Registers |
| Reserved | 0x4819 C000 | 0x481F FFFF | 400KB | Reserved |
| Interrupt controller(1) | 0x4820 0000 | 0x4820 0FFF | 4KB | Cortex™-A8 Accessible Only |
| Reserved(1) | 0x4820 1000 | 0x4823 FFFF | 252KB | Cortex™-A8 Accessible Only |
| MPUSS config register(1) | 0x4824 0000 | 0x4824 0FFF | 4KB | Cortex™-A8 Accessible Only |
| Reserved(1) | 0x4824 1000 | 0x4827 FFFF | 252KB | Cortex™-A8 Accessible Only |
| Reserved(1) | 0x4828 1000 | 0x482F FFFF | 508KB | Cortex™-A8 Accessible Only |
| Reserved | 0x4830 0000 | 0x48FF FFFF | 13MB | Reserved |

(1) These regions are decoded internally by the Cortex™-A8 Subsystem and are not physically part of the L4 standard. They are included here only for reference when considering the Cortex™-A8 memory map. For masters other than the Cortex™-A8, these regions are reserved.


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### 3.9.2.2 L4 High-Speed Peripheral

The L4 high-speed peripheral bus accesses the IP configuration registers of high-speed peripherals in L3. The memory map is shown in Table 3-28.

**Table 3-28. L4 High-Speed Peripheral Memory Map**

| DEVICE NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| L4 High Speed configuration | 0x4A00 0000 | 0x4A00 07FF | 2KB | Address and Protection (AP) |
| | 0x4A00 0800 | 0x4A00 0FFF | 2KB | Link Agent (LA) |
| | 0x4A00 1000 | 0x4A00 13FF | 1KB | Initiator Port (IP0) |
| | 0x4A00 1400 | 0x4A00 17FF | 1KB | Initiator Port (IP1) |
| | 0x4A00 1800 | 0x4A00 1FFF | 2KB | Reserved (IP2 – IP3) |
| Reserved | 0x4A00 2000 | 0x4A07 FFFF | 504KB | Reserved |
| Reserved | 0x4A08 0000 | 0x4A0A 0FFF | 132KB | Reserved |
| Reserved | 0x4A0A 1000 | 0x4A0F FFFF | 380KB | Reserved |
| EMAC0 | 0x4A10 0000 | 0x4A10 3FFF | 16KB | Peripheral Registers |
| | 0x4A10 4000 | 0x4A10 4FFF | 4KB | Support Registers |
| Reserved | 0x4A10 5000 | 0x4A11 FFFF | 108KB | Reserved |
| EMAC1 | 0x4A12 0000 | 0x4A12 3FFF | 16KB | Peripheral Registers |
| | 0x4A12 4000 | 0x4A12 4FFF | 4KB | Support Registers |
| Reserved | 0x4A12 5000 | 0x4A13 FFFF | 108KB | Reserved |
| SATA | 0x4A14 0000 | 0x4A14 FFFF | 64KB | Peripheral Registers |
| | 0x4A15 0000 | 0x4A15 0FFF | 4KB | Support Registers |
| Reserved | 0x4A15 1000 | 0x4A17 FFFF | 188KB | Reserved |
| Reserved | 0x4A18 0000 | 0x4A19 FFFF | 128KB | Reserved |
| | 0x4A1A 0000 | 0x4A1A 0FFF | 4KB | Reserved |
| Reserved | 0x4A1A 1000 | 0x4AFF FFFF | 14716KB | Reserved |

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### 3.9.3 TILER Extended Addressing Map

The Tiling and Isometric Lightweight Engines for Rotation (TILER) ports are mainly used for optimized 2-D block accesses. The TILER also supports rotation of the image buffer at 0º, 90º, 180º, and 270º, with vertical and horizontal mirroring.

The TILER includes an additional 4-GB addressing range to access the frame buffer in these rotated and mirrored views. This range requires a thirty-third bit of address and is only accessible to peripherals that require access to the multiple views. On the device, this is limited to the HD Video Processing Subsystem (HDVPSS). (Other peripherals, based on ConnID, may access any one single view through the 512-MB TILER window region located in the base 4-GB range.)

The HDVPSS may use the virtual address space of 4GB (0x1:0000:0000 – 0x1:FFFF:FFFF) since various VPDMA clients of the HDVPSS may need to simultaneously access multiple 2-D images with different orientations of the image buffers.

The top 4-GB address space is divided into eight sections of 512MB each. These eight sections correspond to the eight different orientations as shown in Table 3-29.

**Table 3-29. TILER Extended Address Memory Map**

| BLOCK NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| Tiler View 0 | 0x1 0000 0000 | 0x1 1FFF FFFF | 512MB | Natural 0° View |
| Tiler View 1 | 0x1 2000 0000 | 0x1 3FFF FFFF | 512MB | 0° with Vertical Mirror View |
| Tiler View 2 | 0x1 4000 0000 | 0x1 5FFF FFFF | 512MB | 0° with Horizontal Mirror View |
| Tiler View 3 | 0x1 6000 0000 | 0x1 7FFF FFFF | 512MB | 180° View |
| Tiler View 4 | 0x1 8000 0000 | 0x1 9FFF FFFF | 512MB | 90° with Vertical Mirror View |
| Tiler View 5 | 0x1 A000 0000 | 0x1 BFFF FFFF | 512MB | 270° View |
| Tiler View 6 | 0x1 C000 0000 | 0x1 DFFF FFFF | 512MB | 90° View |
| Tiler View 7 | 0x1 E000 0000 | 0x1 FFFF FFFF | 512MB | 90° with Horizontal Mirror View |


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### 3.9.4 Cortex™-A8 Memory Map

The Cortex™-A8 includes an memory management unit (MMU) to translate virtual addresses to physical addresses which are then decoded within the Host ARM Subsystem. The subsystem includes its own ROM and RAM, as well as configuration registers for its interrupt controller. These addresses are hard-coded within the subsystem. In addition, the upper 2GB of address space is routed to a special port (Master 0) intended for low-latency access to DDR memory. All other physical addresses are routed to the L3 port (Master 1) where they are decoded by the device infrastructure. The Cortex™-A8 memory map is shown in Table 3-30.

**Table 3-30. Cortex™-A8 Memory Map**

| REGION NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| Boot Space | 0x0000 0000 | 0x000F FFFF | 1MB | Boot Space |
| L3 Target Space | 0x0000 0000 | 0x1FFF FFFF | 512MB | GPMC |
| | 0x2000 0000 | 0x2FFF FFFF | 256MB | PCIe Gen2 Targets |
| | 0x3000 0000 | 0x3FFF FFFF | 256MB | Reserved |
| ROM internal(1) | 0x4000 0000 | 0x4001 FFFF | 128KB | Reserved |
| | 0x4002 0000 | 0x4002 BFFF | 48KB | Public |
| | 0x4002 C000 | 0x400F FFFF | 848KB | Reserved |
| Reserved(1) | 0x4010 0000 | 0x401F FFFF | 1MB | Reserved |
| Reserved(1) | 0x4020 0000 | 0x402E FFFF | 960KB | Reserved |
| Reserved | 0x402F 0000 | 0x402F FFFF | 64KB | Reserved |
| L3 Target Space | 0x4030 0000 | 0x4033 FFFF | 256KB | OCMC SRAM |
| | 0x4034 0000 | 0x403F FFFF | 768KB | Reserved |
| | 0x4040 0000 | 0x4043 FFFF | 256KB | OCMC SRAM |
| | 0x4044 0000 | 0x404F FFFF | 768KB | Reserved |
| | 0x4050 0000 | 0x407F FFFF | 3MB | Reserved |
| | 0x4080 0000 | 0x4083 FFFF | 256KB | C674x UMAP0 (L2 RAM) |
| | 0x4084 0000 | 0x40DF FFFF | 5888KB | Reserved |
| | 0x40E0 0000 | 0x40E0 7FFF | 32KB | C674x L1P Cache and RAM |
| | 0x40E0 8000 | 0x40EF FFFF | 992KB | Reserved |
| | 0x40F0 0000 | 0x40F0 7FFF | 32KB | C674x L1D Cache and RAM |
| | 0x40F0 8000 | 0x40FF FFFF | 992KB | Reserved |
| | 0x4100 0000 | 0x41FF FFFF | 16MB | Reserved |
| | 0x4200 0000 | 0x43FF FFFF | 32MB | Reserved |
| | 0x4400 0000 | 0x44BF FFFF | 12MB | L3 configuration registers |
| | 0x44C0 0000 | 0x45FF FFFF | 20MB | Reserved |
| | 0x4600 0000 | 0x463F FFFF | 4MB | McASP0 |
| | 0x4640 0000 | 0x467F FFFF | 4MB | McASP1 |
| | 0x4680 0000 | 0x46BF FFFF | 4MB | McASP2 |
| | 0x46C0 0000 | 0x46FF FFFF | 4MB | HDMI 1.3 Tx |
| | 0x4700 0000 | 0x473F FFFF | 4MB | McBSP |
| | 0x4740 0000 | 0x477F FFFF | 4MB | USB2.0 Registers and CPPI |
| | 0x4780 0000 | 0x47BF FFFF | 4MB | Reserved |
| | 0x47C0 0000 | 0x47FF FFFF | 4MB | Reserved |
| | 0x4800 0000 | 0x481F FFFF | 2MB | Standard Peripheral domain (see Table 3-27) |
| ARM Subsystem INTC(1) | 0x4820 0000 | 0x4820 0FFF | 4KB | Cortex™-A8 Interrupt Controller |
| Reserved(1) | 0x4820 1000 | 0x4823 FFFF | 252KB | Reserved |
| Reserved(1) | 0x4824 1000 | 0x4827 FFFF | 252KB | Reserved |

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**Table 3-30. Cortex™-A8 Memory Map (continued)**

| REGION NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| L3 Target Space | 0x4830 0000 | 0x48FF FFFF | 13MB | Standard Peripheral domain (see Table 3-27) |
| | 0x4900 0000 | 0x490F FFFF | 1MB | EDMA TPCC Registers |
| | 0x4910 0000 | 0x497F FFFF | 7MB | Reserved |
| | 0x4980 0000 | 0x498F FFFF | 1MB | EDMA TPTC0 Registers |
| | 0x4990 0000 | 0x499F FFFF | 1MB | EDMA TPTC1 Registers |
| | 0x49A0 0000 | 0x49AF FFFF | 1MB | EDMA TPTC2 Registers |
| | 0x49B0 0000 | 0x49BF FFFF | 1MB | EDMA TPTC3 Registers |
| | 0x49C0 0000 | 0x49FF FFFF | 4MB | Reserved |
| | 0x4A00 0000 | 0x4AFF FFFF | 16MB | High Speed Peripheral domain (see Table 3-28) |
| | 0x4B00 0000 | 0x4BFF FFFF | 16MB | EMU Subsystem region |
| | 0x4C00 0000 | 0x4CFF FFFF | 16MB | DDR EMIF0(2) Configuration registers |
| | 0x4D00 0000 | 0x4DFF FFFF | 16MB | DDR EMIF1(2) Configuration registers |
| | 0x4E00 0000 | 0x4FFF FFFF | 32MB | DDR DMM(2) Configuration registers |
| | 0x5000 0000 | 0x50FF FFFF | 16MB | GPMC Configuration registers |
| | 0x5100 0000 | 0x51FF FFFF | 16MB | PCIE Configuration registers |
| | 0x5200 0000 | 0x52FF FFFF | 16MB | Reserved |
| | 0x5300 0000 | 0x53FF FFFF | 16MB | HDVICP2-2 Host Port |
| | 0x5400 0000 | 0x54FF FFFF | 16MB | HDVICP2-2 SL2 Port |
| | 0x5500 0000 | 0x55FF FFFF | 16MB | Reserved |
| | 0x5600 0000 | 0x56FF FFFF | 16MB | SGX530 Slave Port (DM8168 only) |
| | 0x5600 0000 | 0x56FF FFFF | 16MB | Reserved (DM8167 and DM8165 only) |
| | 0x5700 0000 | 0x57FF FFFF | 16MB | Reserved |
| | 0x5800 0000 | 0x58FF FFFF | 16MB | HDVICP2-0 Host Port |
| | 0x5900 0000 | 0x59FF FFFF | 16MB | HDVICP2-0 SL2 Port |
| | 0x5A00 0000 | 0x5AFF FFFF | 16MB | HDVICP2-1 Host Port |
| | 0x5B00 0000 | 0x5BFF FFFF | 16MB | HDVICP2-1 SL2 Port |
| | 0x5C00 0000 | 0x5FFF FFFF | 64MB | Reserved |
| | 0x6000 0000 | 0x7FFF FFFF | 512MB | TILER Window |
| DDR EMIF0 and EMIF1 SDRAM(3)(4) | 0x8000 0000 | 0xBFFF FFFF | 1GB | DDR |
| DDR EMIF0 and EMIF1 SDRAM(3)(4) | 0xC000 0000 | 0xFFFF FFFF | 1GB | DDR |

(1) These addresses are decoded within the Cortex™-A8 subsystem.

(2) These accesses occur through the DDR DMM TILER ports. The DDR DMM splits address ranges internally to address DDR EMIF and DDR DMM control registers based on DDR DMM tie-offs.

(3) These addresses are routed to the Master 0 port for direct connection to the DDR DMM ELLA port.

(4) DDR EMIF0 and DDR EMIF1 addresses may be contiguous or bank interleaved, depending on configuration of the DDR DMM.


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### 3.9.5 C674x Memory Map

Because the C674x DSP has specific hardwired address decoding built in, the C674x memory map is slightly different than that of the Cortex™-A8. The C674x has a separate CFG bus which is used to access L4 peripherals and its UMAP1 bus has a direct connection into HDVICP2 SL2 (HDVICP2-0 and HDVICP2-1 only) memories. All C674x MDMA port accesses are routed through the System MMU for address translation.

**Table 3-31. C674x Memory Map**

| REGION NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| Reserved(1) | 0x0000 0000 | 0x003F FFFF | 4MB | Reserved |
| UMAP1(1) | 0x0040 0000 | 0x0043 FFFF | 256KB | C674x UMAP1 (HDVICP2-0 SL2) |
| Reserved (UMAP1)(1) | 0x0044 0000 | 0x004F FFFF | 768KB | Reserved |
| UMAP1(1) | 0x0050 0000 | 0x0053 FFFF | 256KB | C674x UMAP1 (HDVICP2-1 SL2) |
| Reserved (UMAP1)(1) | 0x0054 0000 | 0x005F FFFF | 768KB | Reserved |
| Reserved(1) | 0x0060 0000 | 0x007F FFFF | 2MB | Reserved |
| L2 SRAM(1) | 0x0080 0000 | 0x0083 FFFF | 256KB | C674x UMAP0 (L2 RAM) |
| Reserved(1) | 0x0084 0000 | 0x00DF FFFF | 5888KB | Reserved |
| L1P SRAM(1) | 0x00E0 0000 | 0x00E0 7FFF | 32KB | C674x L1P Cache and RAM |
| Reserved(1) | 0x00E0 8000 | 0x00EF FFFF | 992KB | Reserved |
| L1D SRAM(1) | 0x00F0 0000 | 0x00F0 7FFF | 32KB | C674x L1D Cache and RAM |
| Reserved(1) | 0x00F0 8000 | 0x017F FFFF | 9184KB | Reserved |
| Internal CFG(2)(3) | 0x0180 0000 | 0x01BF FFFF | 4MB | C674x Internal CFG registers |
| Reserved(3) | 0x01C0 0000 | 0x07FF FFFF | 100MB | Reserved |
| L4 Standard Domain(3) | 0x0800 0000 | 0x08FF FFFF | 16MB | Peripheral Domain (see Table 3-27) |
| EDMA TPCC(3) | 0x0900 0000 | 0x090F FFFF | 1MB | EDMA TPCC Registers |
| Reserved(3) | 0x0910 0000 | 0x097F FFFF | 7MB | Reserved |
| EDMA TPTC0(3) | 0x0980 0000 | 0x098F FFFF | 1MB | EDMA TPTC0 Registers |
| EDMA TPTC1(3) | 0x0990 0000 | 0x099F FFFF | 1MB | EDMA TPTC1 Registers |
| EDMA TPTC2(3) | 0x09A0 0000 | 0x09AF FFFF | 1MB | EDMA TPTC2 Registers |
| EDMA TPTC3(3) | 0x09B0 0000 | 0x09BF FFFF | 1MB | EDMA TPTC3 Registers |
| Reserved(3) | 0x09C0 0000 | 0x09FF FFFF | 4MB | Reserved |
| L4 High-Speed Domain(3) | 0x0A00 0000 | 0x0AFF FFFF | 16MB | Peripheral Domain (see Table 3-28) |
| Reserved(3) | 0x0B00 0000 | 0x0FFF FFFF | 80MB | Reserved |
| C674x L1 and L2(4) | 0x1000 0000 | 0x10FF FFFF | 16MB | C674x Internal Global Address |
| MDMA L3(5) | 0x1100 0000 | 0xFFFF FFFF | 3824MB | System MMU Mapped L3 Regions |

(1) Addresses 0x0000 0000 to 0x017F FFFF are internal to the C674x device.
(2) Addresses 0x0180 0000 to 0x01BF FFFF are reserved for C674x internal CFG registers.
(3) Addresses 0x01C0 0000 to 0x0FFF FFFF are mapped to the C674x CFG bus.
(4) Addresses 0x1000 0000 to 0x10FF FFFF are mapped to C674x internal addresses 0x0000 0000 to 0x00FF FFFF.
(5) These accesses are routed through the System MMU where the page tables translate to the physical L3 addresses shown in Table 3-26.

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# 4 Terminal Configuration and Functions

## 4.1 Pin Assignments

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. For more information on pin muxing, see Section 6.5, *Pin Multiplexing Control*.

### *4.1.1 Pin Map (Bottom View)*

Figure 4-1 through Figure 4-19 show the bottom view of the package pin assignments in 15 sections (A, B, C, D, E, F, G, H, I, J, K, L, M, N, and O).

**NOTE**

Pin map sections D, E, K, and L show the different pin names for silicon revision 1.x devices and silicon revision 2.x devices.


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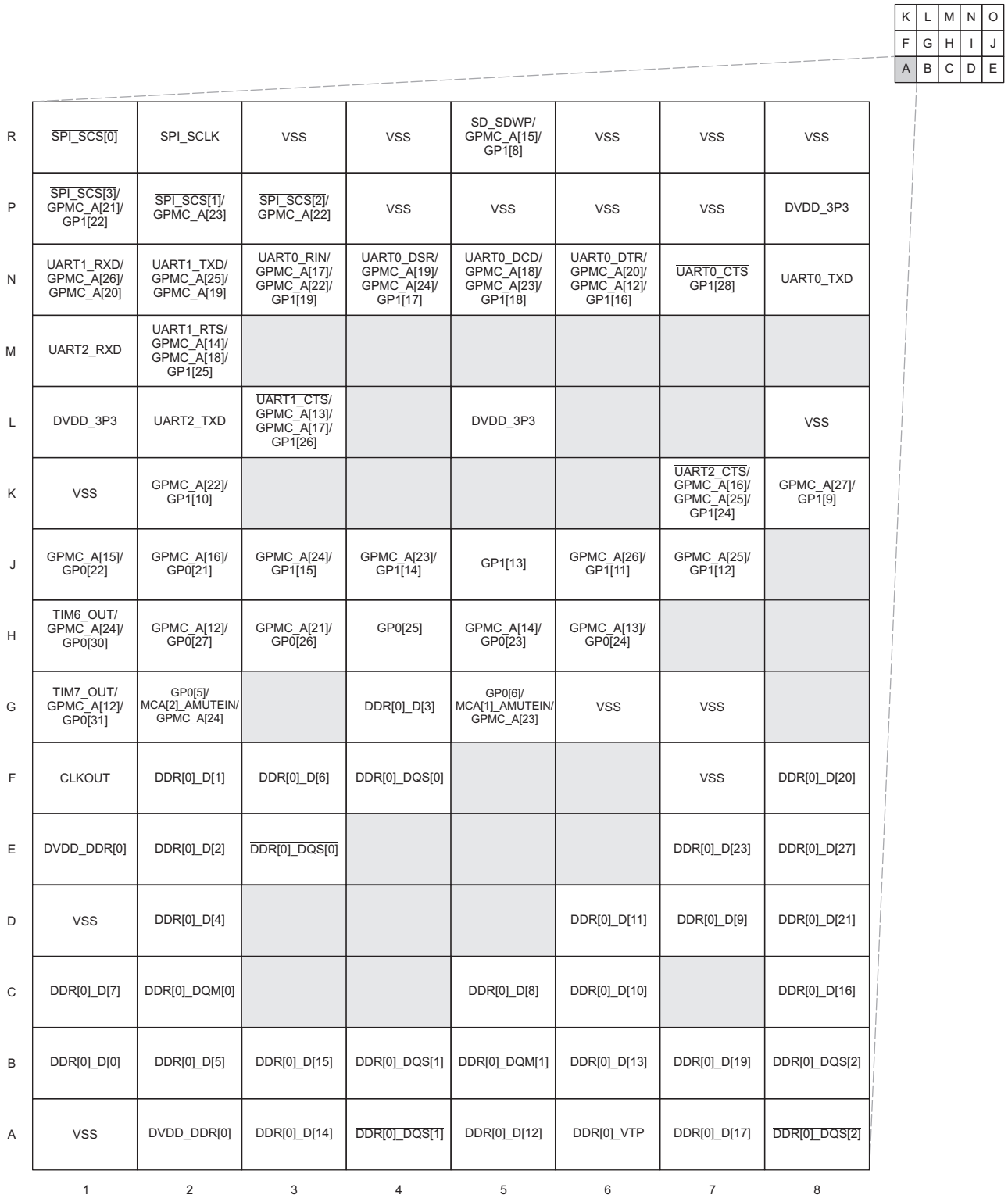
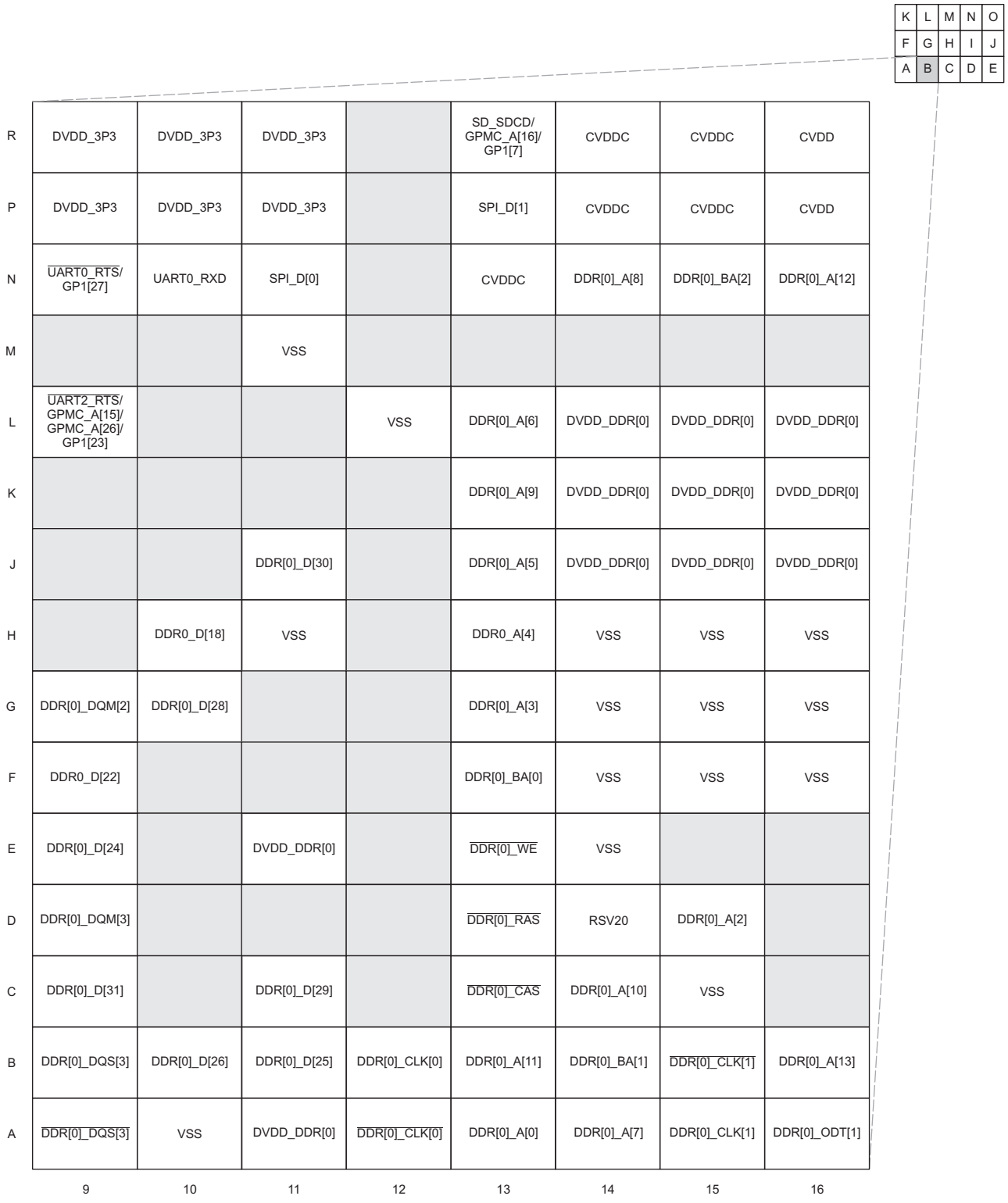


| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| R | SPI_SCS[0] | SPI_SCLK | VSS | VSS | SD_SDWP/ GPMC_A[15]/ GP1[8] | VSS | VSS | VSS |
| P | SPI_SCS[3]/ GPMC_A[21]/ GP1[22] | SPI_SCS[1]/ GPMC_A[23] | SPI_SCS[2]/ GPMC_A[22] | VSS | VSS | VSS | VSS | DVDD_3P3 |
| N | UART1_RXD/ GPMC_A[26]/ GPMC_A[20] | UART1_TXD/ GPMC_A[25]/ GPMC_A[19] | UART0_RIN/ GPMC_A[17]/ GPMC_A[22]/ GP1[19] | UART0_DSR/ GPMC_A[19]/ GPMC_A[24]/ GP1[17] | UART0_DCD/ GPMC_A[18]/ GPMC_A[23]/ GP1[18] | UART0_DTR/ GPMC_A[20]/ GPMC_A[12]/ GP1[16] | UART0_CTS GP1[28] | UART0_TXD |
| M | UART2_RXD | UART1_RTS/ GPMC_A[14]/ GPMC_A[18]/ GP1[25] | | | | | | |
| L | DVDD_3P3 | UART2_TXD | UART1_CTS/ GPMC_A[13]/ GPMC_A[17]/ GP1[26] | | DVDD_3P3 | | | VSS |
| K | VSS | GPMC_A[22]/ GP1[10] | | | | | UART2_CTS/ GPMC_A[16]/ GPMC_A[25]/ GP1[24] | GPMC_A[27]/ GP1[9] |
| J | GPMC_A[15]/ GP0[22] | GPMC_A[16]/ GP0[21] | GPMC_A[24]/ GP1[15] | GPMC_A[23]/ GP1[14] | GP1[13] | GPMC_A[26]/ GP1[11] | GPMC_A[25]/ GP1[12] | |
| H | TIM6_OUT/ GPMC_A[24]/ GP0[30] | GPMC_A[12]/ GP0[27] | GPMC_A[21]/ GP0[26] | GP0[25] | GPMC_A[14]/ GP0[23] | GPMC_A[13]/ GP0[24] | | |
| G | TIM7_OUT/ GPMC_A[12]/ GP0[31] | GP0[5]/ MCA[2]_AMUTEIN/ GPMC_A[24] | | DDR[0]_D[3] | GP0[6]/ MCA[1]_AMUTEIN/ GPMC_A[23] | VSS | VSS | |
| F | CLKOUT | DDR[0]_D[1] | DDR[0]_D[6] | DDR[0]_DQS[0] | | | VSS | DDR[0]_D[20] |
| E | DVDD_DDR[0] | DDR[0]_D[2] | DDR[0]_DQS[0] | | | | DDR[0]_D[23] | DDR[0]_D[27] |
| D | VSS | DDR[0]_D[4] | | | | DDR[0]_D[11] | DDR[0]_D[9] | DDR[0]_D[21] |
| C | DDR[0]_D[7] | DDR[0]_DQM[0] | | | DDR[0]_D[8] | DDR[0]_D[10] | | DDR[0]_D[16] |
| B | DDR[0]_D[0] | DDR[0]_D[5] | DDR[0]_D[15] | DDR[0]_DQS[1] | DDR[0]_DQM[1] | DDR[0]_D[13] | DDR[0]_D[19] | DDR[0]_DQS[2] |
| A | VSS | DVDD_DDR[0] | DDR[0]_D[14] | DDR[0]_DQS[1] | DDR[0]_D[12] | DDR[0]_VTP | DDR[0]_D[17] | DDR[0]_DQS[2] |

**Figure 4-1. Pin Map [Section A]**



| | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|
| R | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 | | SD_SDCD/ GPMC_A[16]/ GP1[7] | CVDDC | CVDDC | CVDD |
| P | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 | | SPI_D[1] | CVDDC | CVDDC | CVDD |
| N | UART0_RTS/ GP1[27] | UART0_RXD | SPI_D[0] | | CVDDC | DDR[0]_A[8] | DDR[0]_BA[2] | DDR[0]_A[12] |
| M | | | VSS | | | | | |
| L | UART2_RTS/ GPMC_A[15]/ GPMC_A[26]/ GP1[23] | | | VSS | DDR[0]_A[6] | DVDD_DDR[0] | DVDD_DDR[0] | DVDD_DDR[0] |
| K | | | | | DDR[0]_A[9] | DVDD_DDR[0] | DVDD_DDR[0] | DVDD_DDR[0] |
| J | | | DDR[0]_D[30] | | DDR[0]_A[5] | DVDD_DDR[0] | DVDD_DDR[0] | DVDD_DDR[0] |
| H | | DDR0_D[18] | VSS | | DDR0_A[4] | VSS | VSS | VSS |
| G | DDR[0]_DQM[2] | DDR[0]_D[28] | | | DDR[0]_A[3] | VSS | VSS | VSS |
| F | DDR0_D[22] | | | | DDR[0]_BA[0] | VSS | VSS | VSS |
| E | DDR[0]_D[24] | | DVDD_DDR[0] | | DDR[0]_WE | VSS | | |
| D | DDR[0]_DQM[3] | | | | DDR[0]_RAS | RSV20 | DDR[0]_A[2] | |
| C | DDR[0]_D[31] | | DDR[0]_D[29] | | DDR[0]_CAS | DDR[0]_A[10] | VSS | |
| B | DDR[0]_DQS[3] | DDR[0]_D[26] | DDR[0]_D[25] | DDR[0]_CLK[0] | DDR[0]_A[11] | DDR[0]_BA[1] | DDR[0]_CLK[1] | DDR[0]_A[13] |
| A | DDR[0]_DQS[3] | VSS | DVDD_DDR[0] | DDR[0]_CLK[0] | DDR[0]_A[0] | DDR[0]_A[7] | DDR[0]_CLK[1] | DDR[0]_ODT[1] |

**Figure 4-2. Pin Map [Section B]**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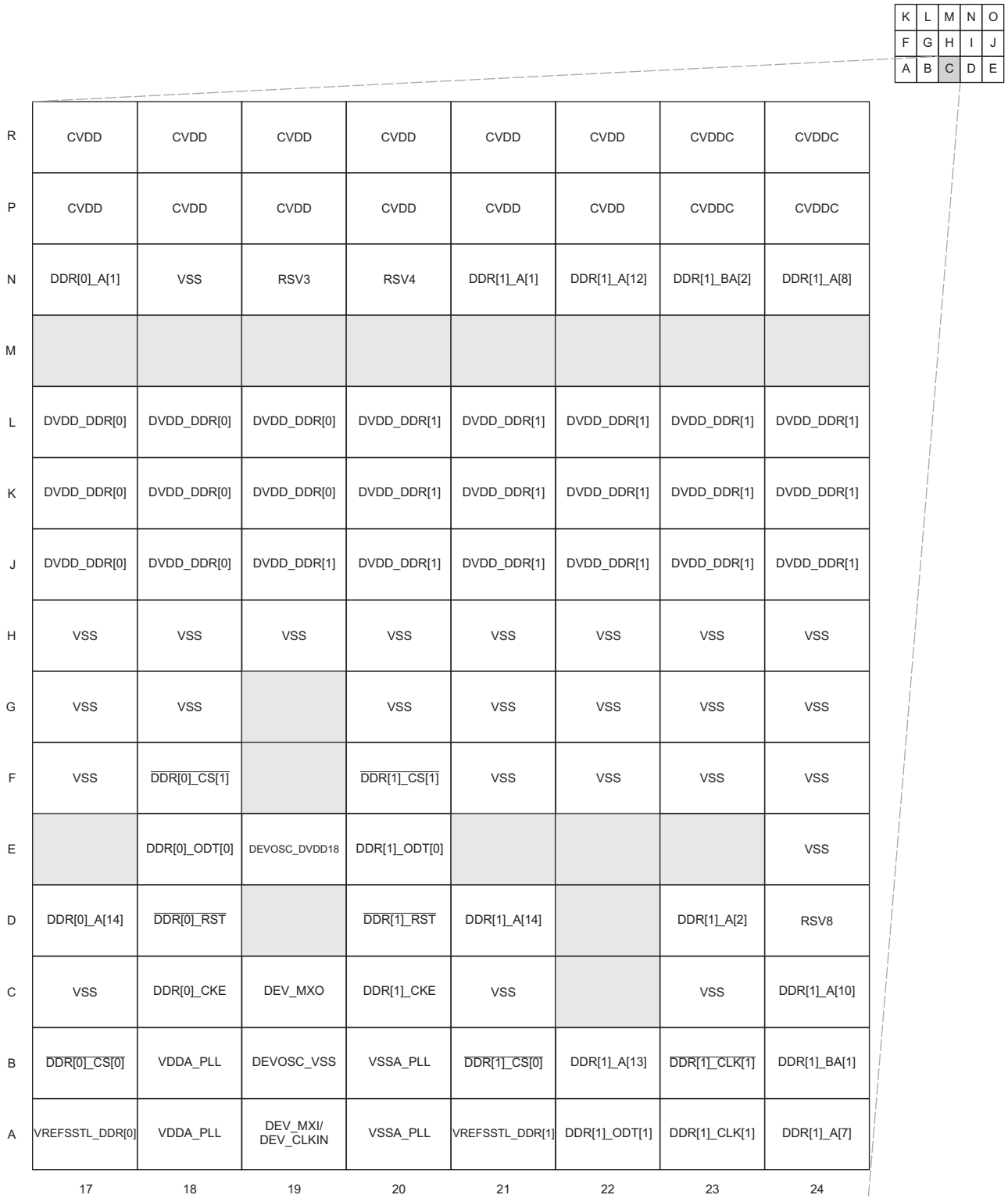


**Figure 4-3. Pin Map [Section C]**

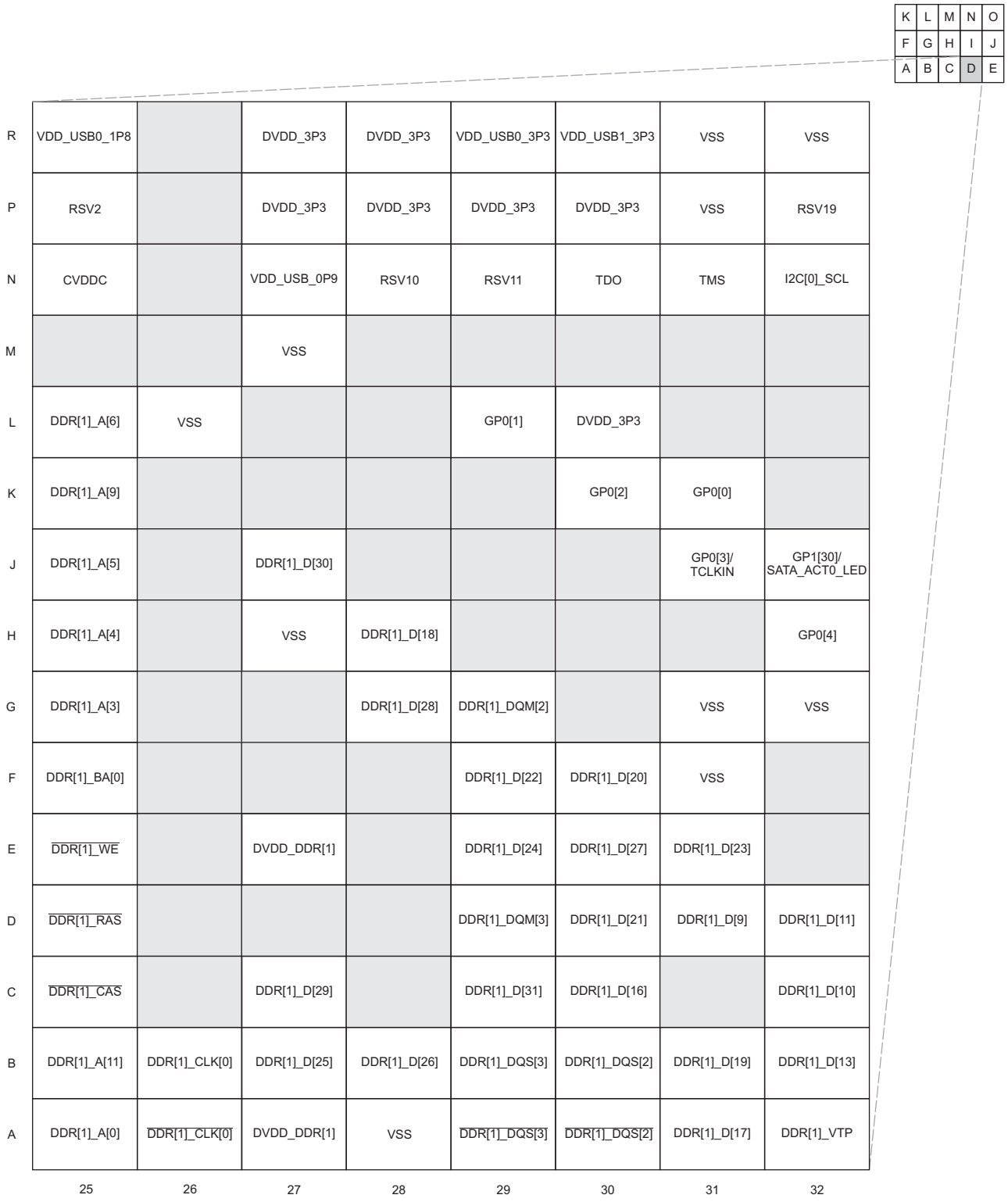


**Figure 4-4. Pin Map [Section D] - Silicon Revision 1.x**


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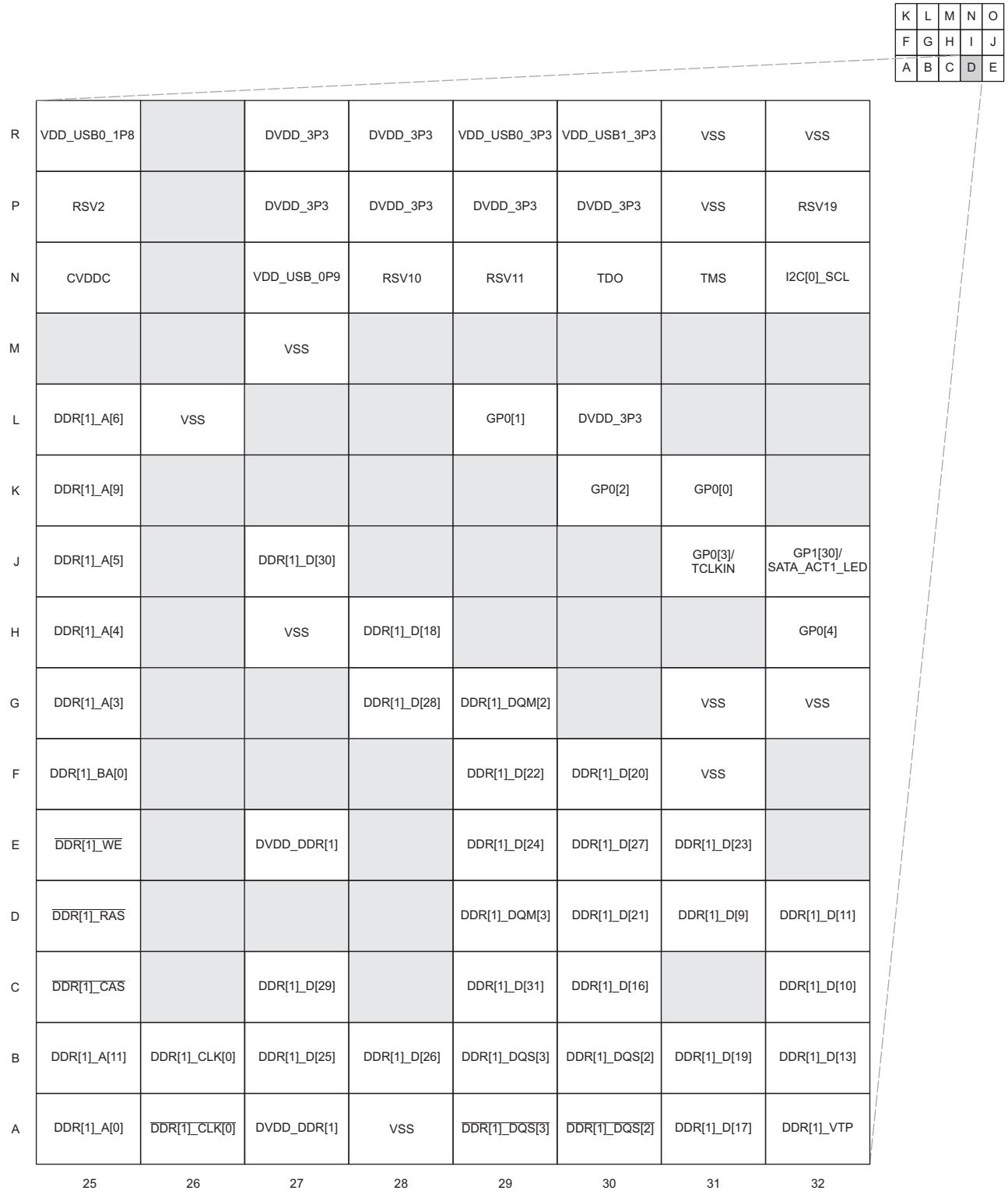


**Figure 4-5. Pin Map [Section D] - Silicon Revision 2.x**

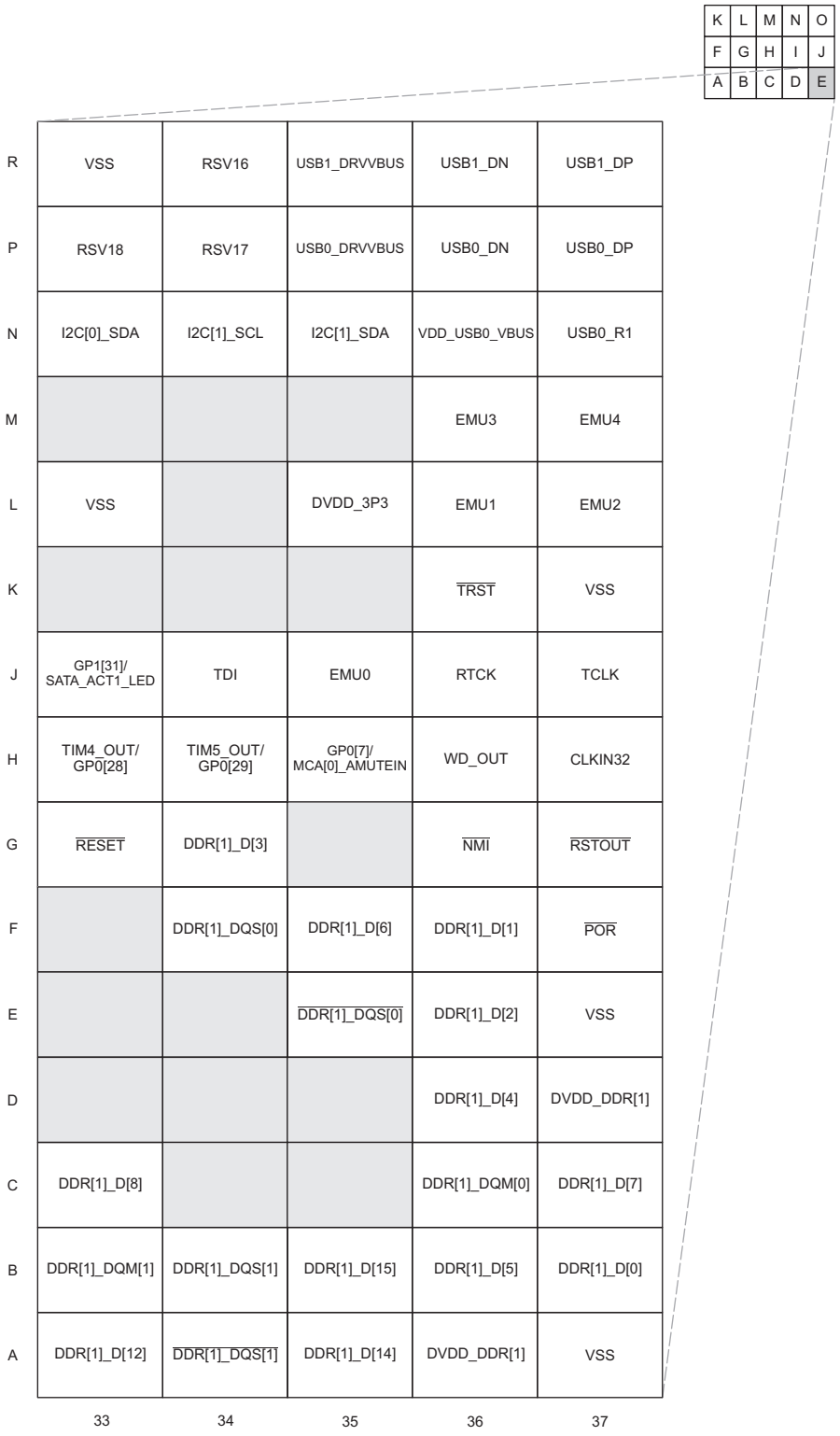


**Figure 4-6. Pin Map [Section E] - Silicon Revision 1.x**


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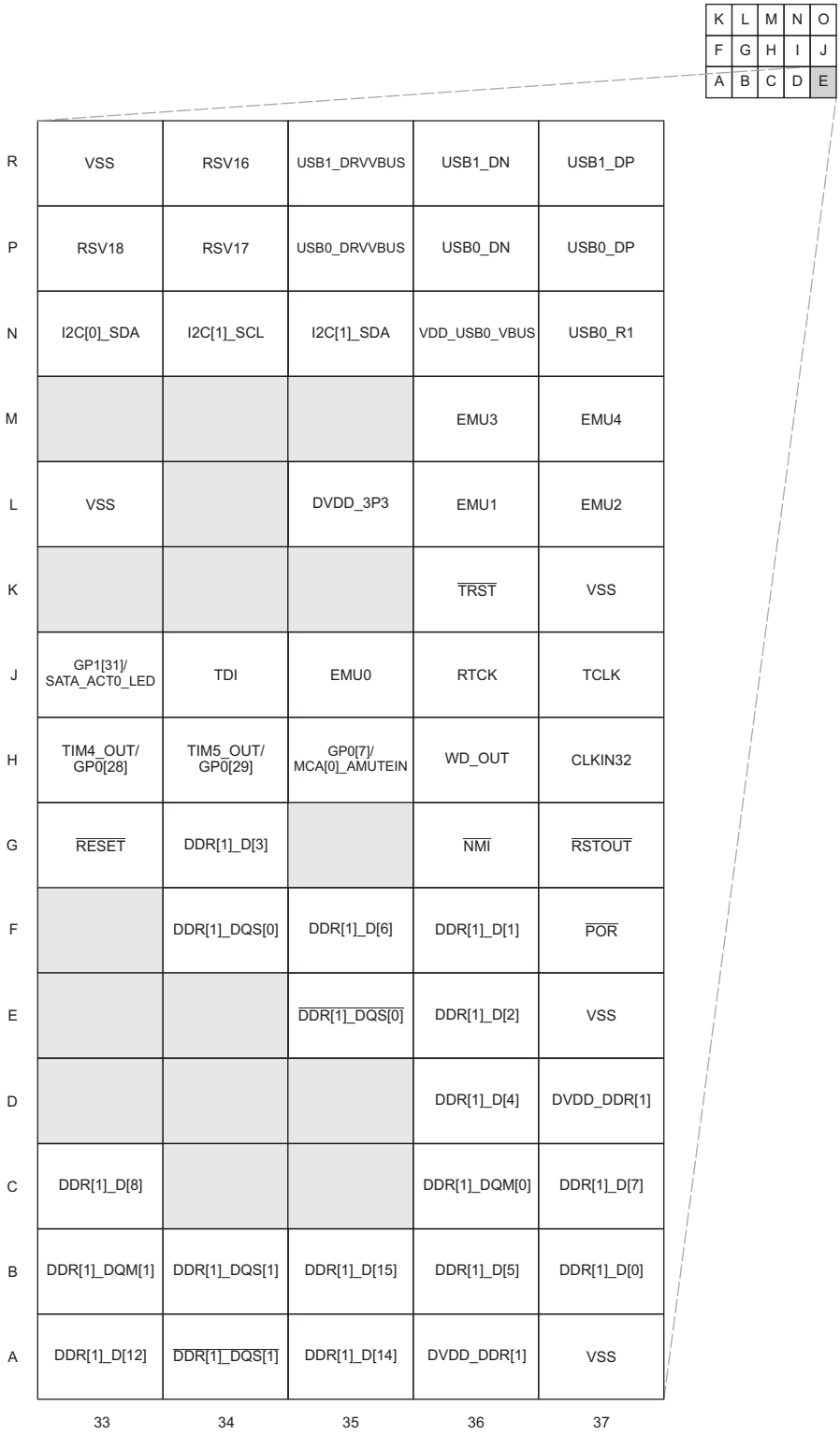
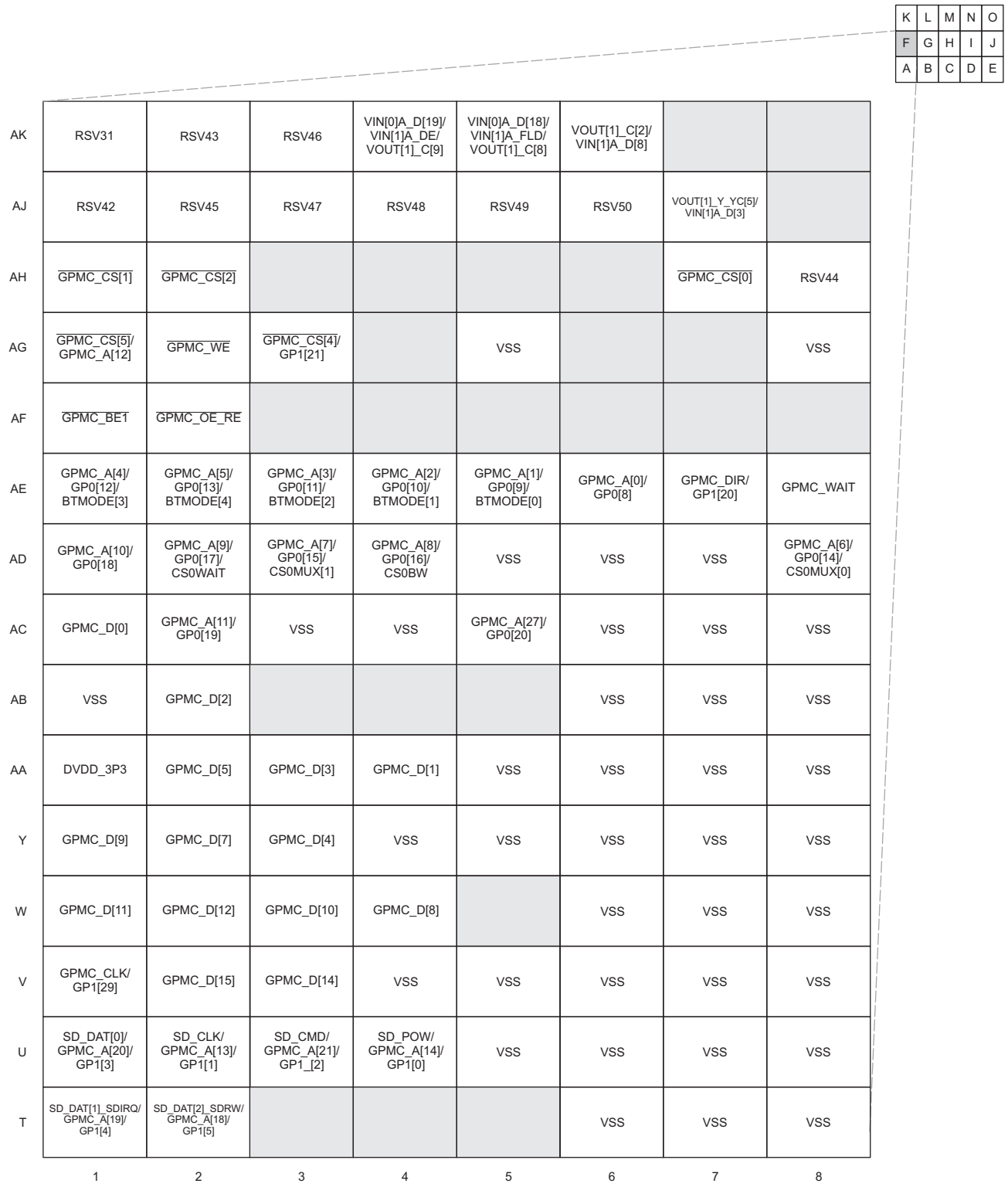



**Figure 4-7. Pin Map [Section E] - Silicon Revision 2.x**




| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| AK | RSV31 | RSV43 | RSV46 | VIN[0]A_D[19]/ VIN[1]A_DE/ VOUT[1]_C[9] | VIN[0]A_D[18]/ VIN[1]A_FLD/ VOUT[1]_C[8] | VOUT[1]_C[2]/ VIN[1]A_D[8] | | |
| AJ | RSV42 | RSV45 | RSV47 | RSV48 | RSV49 | RSV50 | VOUT[1]_Y_YC[5]/ VIN[1]A_D[3] | |
| AH | GPMC_CS[1] | GPMC_CS[2] | | | | | GPMC_CS[0] | RSV44 |
| AG | GPMC_CS[5]/ GPMC_A[12] | GPMC_WE | GPMC_CS[4]/ GP1[21] | | VSS | | | VSS |
| AF | GPMC_BE1 | GPMC_OE_RE | | | | | | |
| AE | GPMC_A[4]/ GP0[12]/ BTMODE[3] | GPMC_A[5]/ GP0[13]/ BTMODE[4] | GPMC_A[3]/ GP0[11]/ BTMODE[2] | GPMC_A[2]/ GP0[10]/ BTMODE[1] | GPMC_A[1]/ GP0[9]/ BTMODE[0] | GPMC_A[0]/ GP0[8] | GPMC_DIR/ GP1[20] | GPMC_WAIT |
| AD | GPMC_A[10]/ GP0[18] | GPMC_A[9]/ GP0[17]/ CS0WAIT | GPMC_A[7]/ GP0[15]/ CS0MUX[1] | GPMC_A[8]/ GP0[16]/ CS0BW | VSS | VSS | VSS | GPMC_A[6]/ GP0[14]/ CS0MUX[0] |
| AC | GPMC_D[0] | GPMC_A[11]/ GP0[19] | VSS | VSS | GPMC_A[27]/ GP0[20] | VSS | VSS | VSS |
| AB | VSS | GPMC_D[2] | | | | VSS | VSS | VSS |
| AA | DVDD_3P3 | GPMC_D[5] | GPMC_D[3] | GPMC_D[1] | VSS | VSS | VSS | VSS |
| Y | GPMC_D[9] | GPMC_D[7] | GPMC_D[4] | VSS | VSS | VSS | VSS | VSS |
| W | GPMC_D[11] | GPMC_D[12] | GPMC_D[10] | GPMC_D[8] | | VSS | VSS | VSS |
| V | GPMC_CLK/ GP1[29] | GPMC_D[15] | GPMC_D[14] | VSS | VSS | VSS | VSS | VSS |
| U | SD_DAT[0]/ GPMC_A[20]/ GP1[3] | SD_CLK/ GPMC_A[13]/ GP1[1] | SD_CMD/ GPMC_A[21]/ GP1_[2] | SD_POW/ GPMC_A[14]/ GP1[0] | VSS | VSS | VSS | VSS |
| T | SD_DAT[1]_SDIRQ/ GPMC_A[19]/ GP1[4] | SD_DAT[2]_SDRW/ GPMC_A[18]/ GP1[5] | | | | VSS | VSS | VSS |

**Figure 4-8. Pin Map [Section F]**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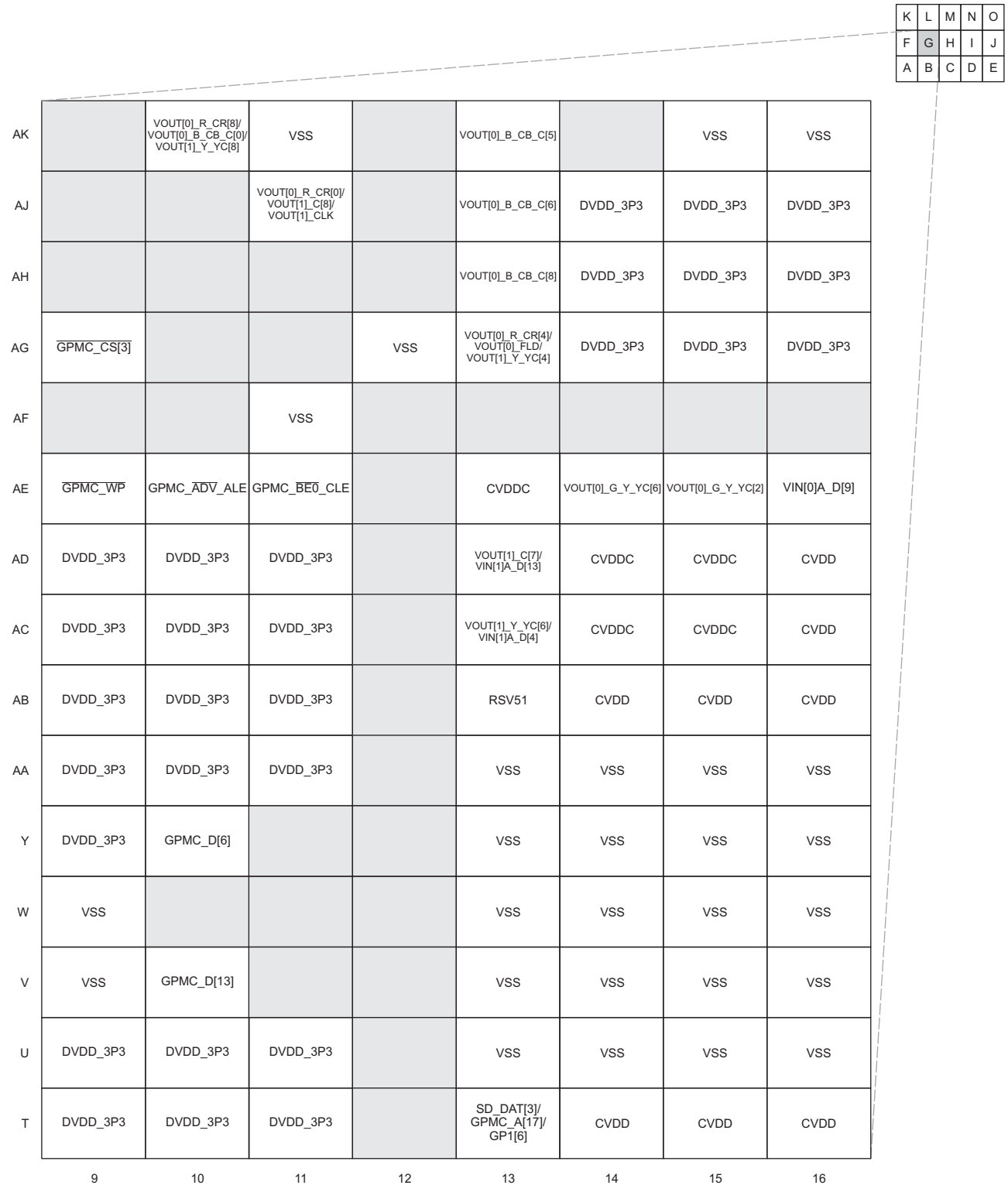
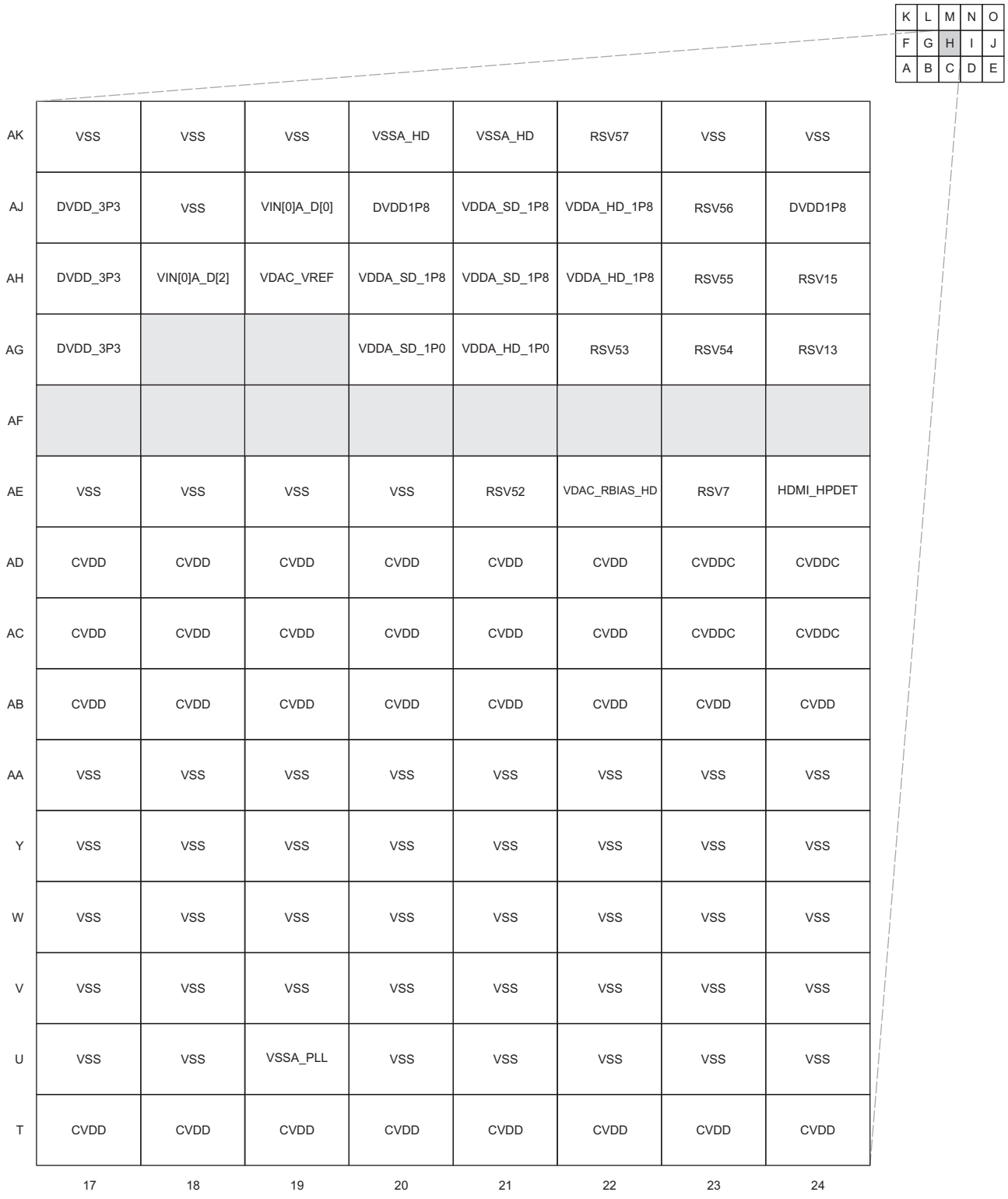


| | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|
| AK | | VOUT[0]_R_CR[8]/ VOUT[0]_B_CB_C[0]/ VOUT[1]_Y_YC[8] | VSS | | VOUT[0]_B_CB_C[5] | | VSS | VSS |
| AJ | | | VOUT[0]_R_CR[0]/ VOUT[1]_C[8]/ VOUT[1]_CLK | | VOUT[0]_B_CB_C[6] | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 |
| AH | | | | | VOUT[0]_B_CB_C[8] | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 |
| AG | $\overline{\text{GPMC_CS[3]}}$ | | | VSS | VOUT[0]_R_CR[4]/ VOUT[0]_FLD/ VOUT[1]_Y_YC[4] | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 |
| AF | | | VSS | | | | | |
| AE | $\overline{\text{GPMC_WP}}$ | GPMC_$\overline{\text{ADV}}$_ALE | GPMC_$\overline{\text{BE0}}$_CLE | | CVDDC | VOUT[0]_G_Y_YC[6] | VOUT[0]_G_Y_YC[2] | VIN[0]A_D[9] |
| AD | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 | | VOUT[1]_C[7]/ VIN[1]A_D[13] | CVDDC | CVDDC | CVDD |
| AC | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 | | VOUT[1]_Y_YC[6]/ VIN[1]A_D[4] | CVDDC | CVDDC | CVDD |
| AB | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 | | RSV51 | CVDD | CVDD | CVDD |
| AA | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 | | VSS | VSS | VSS | VSS |
| Y | DVDD_3P3 | GPMC_D[6] | | | VSS | VSS | VSS | VSS |
| W | VSS | | | | VSS | VSS | VSS | VSS |
| V | VSS | GPMC_D[13] | | | VSS | VSS | VSS | VSS |
| U | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 | | VSS | VSS | VSS | VSS |
| T | DVDD_3P3 | DVDD_3P3 | DVDD_3P3 | | SD_DAT[3]/ GPMC_A[17]/ GP1[6] | CVDD | CVDD | CVDD |

**Figure 4-9. Pin Map [Section G]**




| | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|
| AK | VSS | VSS | VSS | VSSA_HD | VSSA_HD | RSV57 | VSS | VSS |
| AJ | DVDD_3P3 | VSS | VIN[0]A_D[0] | DVDD1P8 | VDDA_SD_1P8 | VDDA_HD_1P8 | RSV56 | DVDD1P8 |
| AH | DVDD_3P3 | VIN[0]A_D[2] | VDAC_VREF | VDDA_SD_1P8 | VDDA_SD_1P8 | VDDA_HD_1P8 | RSV55 | RSV15 |
| AG | DVDD_3P3 | | | VDDA_SD_1P0 | VDDA_HD_1P0 | RSV53 | RSV54 | RSV13 |
| AF | | | | | | | | |
| AE | VSS | VSS | VSS | VSS | RSV52 | VDAC_RBIAS_HD | RSV7 | HDMI_HPDET |
| AD | CVDD | CVDD | CVDD | CVDD | CVDD | CVDD | CVDDC | CVDDC |
| AC | CVDD | CVDD | CVDD | CVDD | CVDD | CVDD | CVDDC | CVDDC |
| AB | CVDD | CVDD | CVDD | CVDD | CVDD | CVDD | CVDD | CVDD |
| AA | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| Y | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| W | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| V | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| U | VSS | VSS | VSSA_PLL | VSS | VSS | VSS | VSS | VSS |
| T | CVDD | CVDD | CVDD | CVDD | CVDD | CVDD | CVDD | CVDD |

**Figure 4-10. Pin Map [Section H]**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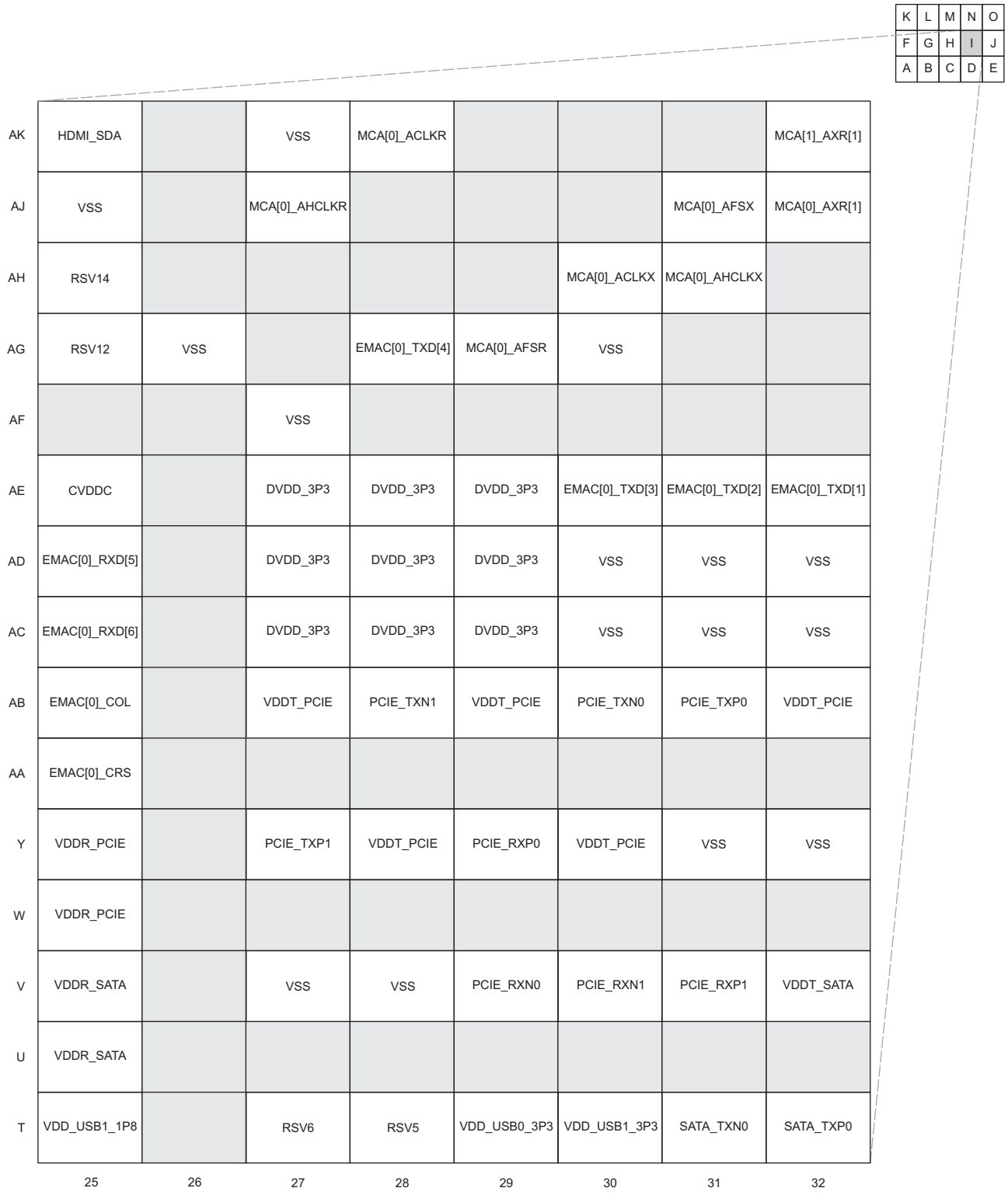


**Figure 4-11. Pin Map [Section I]**

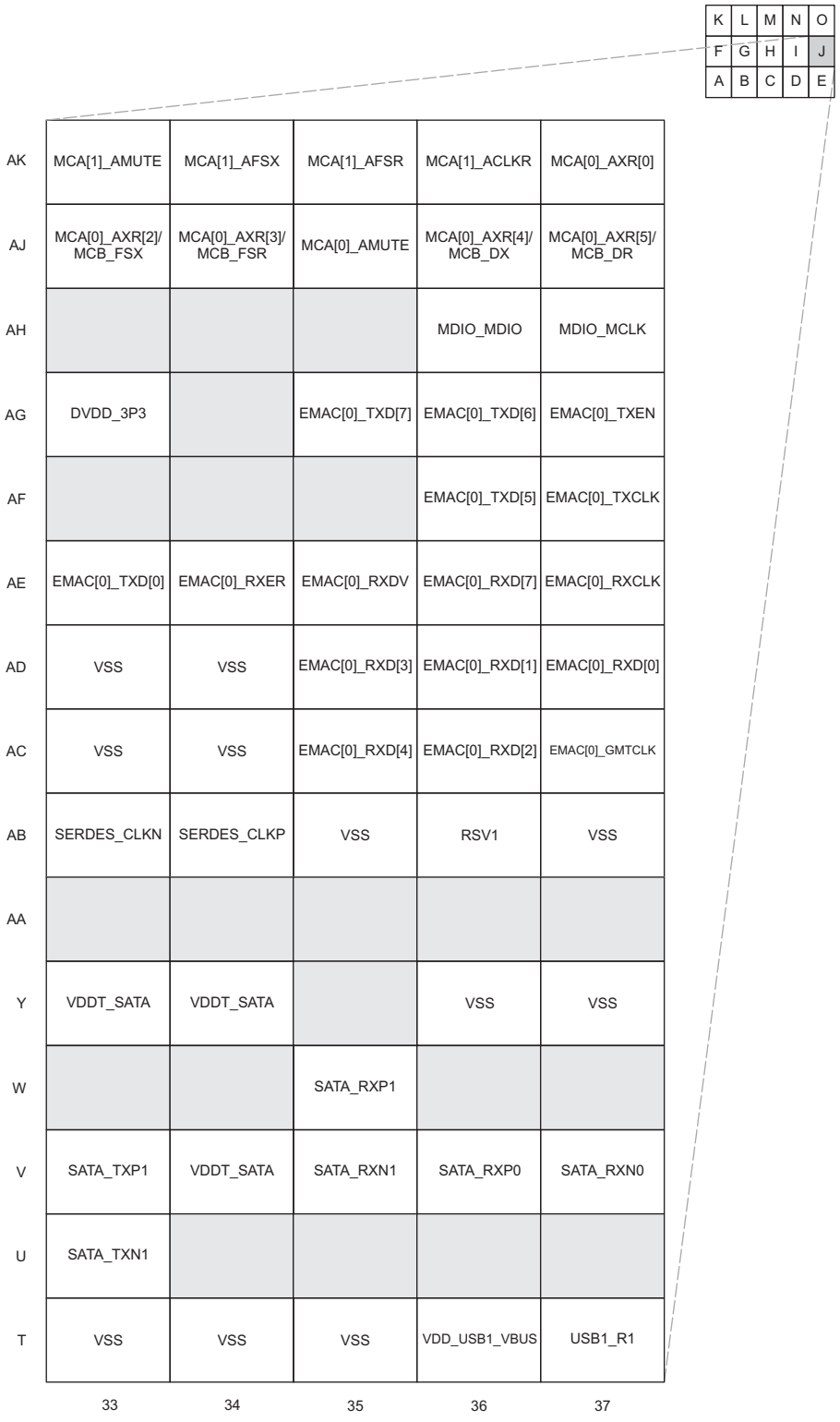


**Figure 4-12. Pin Map [Section J]**


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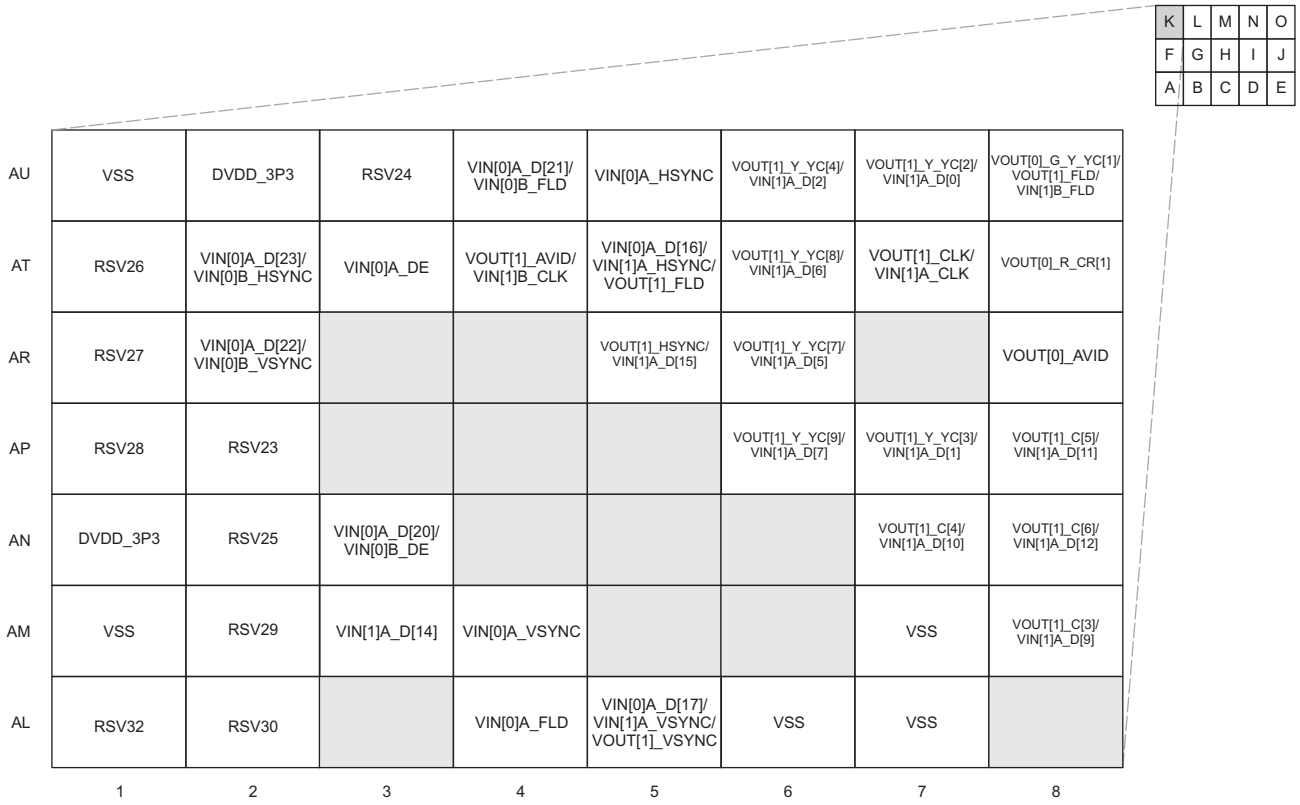
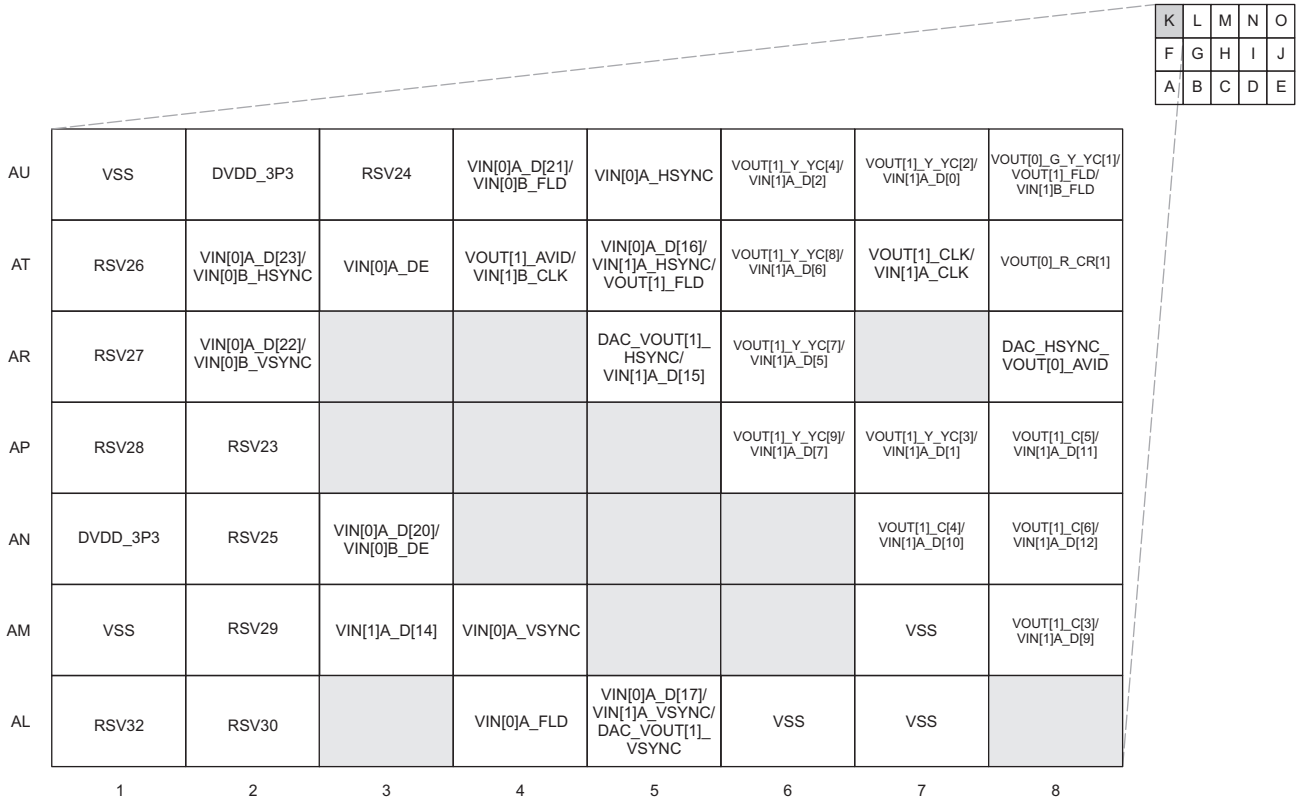


| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| AU | VSS | DVDD_3P3 | RSV24 | VIN[0]A_D[21]/ VIN[0]B_FLD | VIN[0]A_HSYNC | VOUT[1]_Y_YC[4]/ VIN[1]A_D[2] | VOUT[1]_Y_YC[2]/ VIN[1]A_D[0] | VOUT[0]_G_Y_YC[1]/ VOUT[1]_FLD/ VIN[1]B_FLD |
| AT | RSV26 | VIN[0]A_D[23]/ VIN[0]B_HSYNC | VIN[0]A_DE | VOUT[1]_AVID/ VIN[1]B_CLK | VIN[0]A_D[16]/ VIN[1]A_HSYNC/ VOUT[1]_FLD | VOUT[1]_Y_YC[8]/ VIN[1]A_D[6] | VOUT[1]_CLK/ VIN[1]A_CLK | VOUT[0]_R_CR[1] |
| AR | RSV27 | VIN[0]A_D[22]/ VIN[0]B_VSYNC | | | VOUT[1]_HSYNC/ VIN[1]A_D[15] | VOUT[1]_Y_YC[7]/ VIN[1]A_D[5] | | VOUT[0]_AVID |
| AP | RSV28 | RSV23 | | | | VOUT[1]_Y_YC[9]/ VIN[1]A_D[7] | VOUT[1]_Y_YC[3]/ VIN[1]A_D[1] | VOUT[1]_C[5]/ VIN[1]A_D[11] |
| AN | DVDD_3P3 | RSV25 | VIN[0]A_D[20]/ VIN[0]B_DE | | | | VOUT[1]_C[4]/ VIN[1]A_D[10] | VOUT[1]_C[6]/ VIN[1]A_D[12] |
| AM | VSS | RSV29 | VIN[1]A_D[14] | VIN[0]A_VSYNC | | | VSS | VOUT[1]_C[3]/ VIN[1]A_D[9] |
| AL | RSV32 | RSV30 | | VIN[0]A_FLD | VIN[0]A_D[17]/ VIN[1]A_VSYNC/ VOUT[1]_VSYNC | VSS | VSS | |

**Figure 4-13. Pin Map [Section K] - Silicon Revision 1.x**



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| AU | VSS | DVDD_3P3 | RSV24 | VIN[0]A_D[21]/ VIN[0]B_FLD | VIN[0]A_HSYNC | VOUT[1]_Y_YC[4]/ VIN[1]A_D[2] | VOUT[1]_Y_YC[2]/ VIN[1]A_D[0] | VOUT[0]_G_Y_YC[1]/ VOUT[1]_FLD/ VIN[1]B_FLD |
| AT | RSV26 | VIN[0]A_D[23]/ VIN[0]B_HSYNC | VIN[0]A_DE | VOUT[1]_AVID/ VIN[1]B_CLK | VIN[0]A_D[16]/ VIN[1]A_HSYNC/ VOUT[1]_FLD | VOUT[1]_Y_YC[8]/ VIN[1]A_D[6] | VOUT[1]_CLK/ VIN[1]A_CLK | VOUT[0]_R_CR[1] |
| AR | RSV27 | VIN[0]A_D[22]/ VIN[0]B_VSYNC | | | DAC_VOUT[1]_ HSYNC/ VIN[1]A_D[15] | VOUT[1]_Y_YC[7]/ VIN[1]A_D[5] | | DAC_HSYNC_ VOUT[0]_AVID |
| AP | RSV28 | RSV23 | | | | VOUT[1]_Y_YC[9]/ VIN[1]A_D[7] | VOUT[1]_Y_YC[3]/ VIN[1]A_D[1] | VOUT[1]_C[5]/ VIN[1]A_D[11] |
| AN | DVDD_3P3 | RSV25 | VIN[0]A_D[20]/ VIN[0]B_DE | | | | VOUT[1]_C[4]/ VIN[1]A_D[10] | VOUT[1]_C[6]/ VIN[1]A_D[12] |
| AM | VSS | RSV29 | VIN[1]A_D[14] | VIN[0]A_VSYNC | | | VSS | VOUT[1]_C[3]/ VIN[1]A_D[9] |
| AL | RSV32 | RSV30 | | VIN[0]A_FLD | VIN[0]A_D[17]/ VIN[1]A_VSYNC/ DAC_VOUT[1]_ VSYNC | VSS | VSS | |

**Figure 4-14. Pin Map [Section K] - Silicon Revision 2.x**

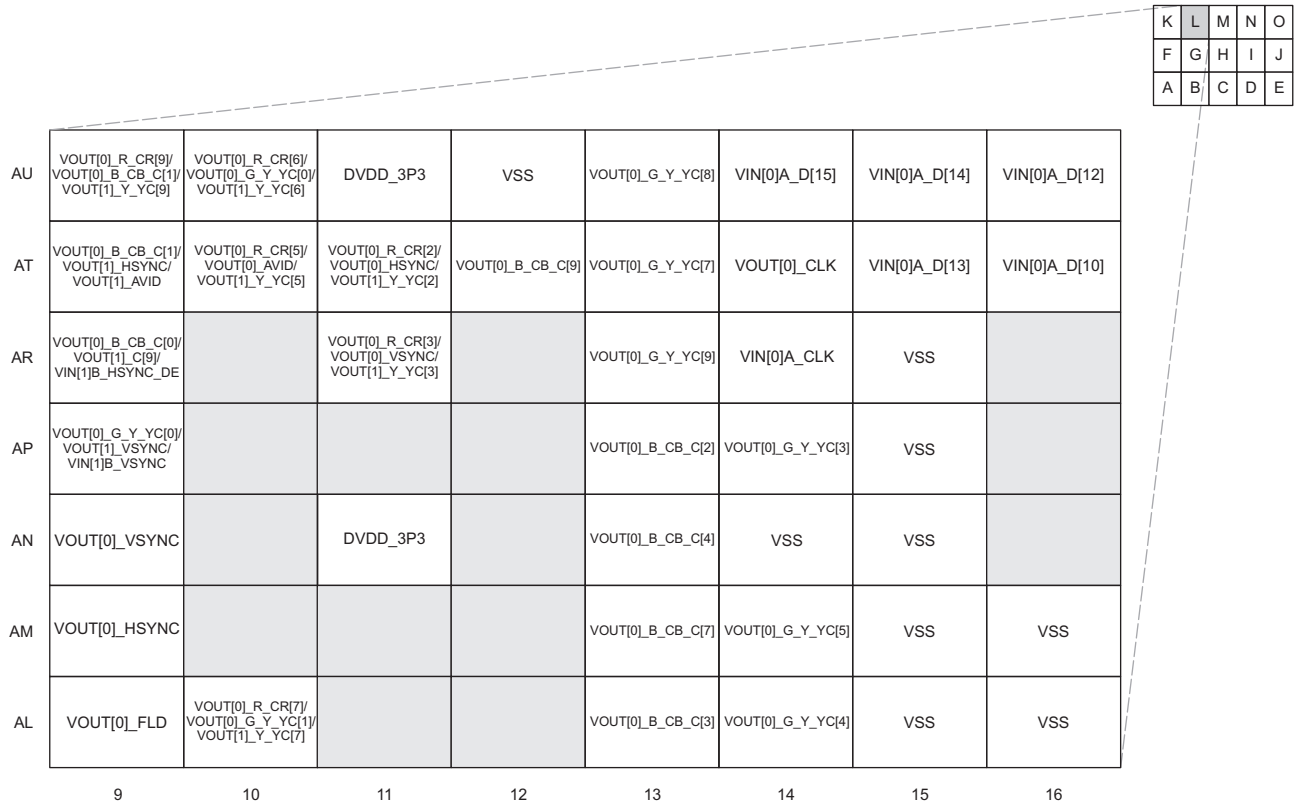



**Figure 4-15. Pin Map [Section L] - Silicon Revision 1.x**

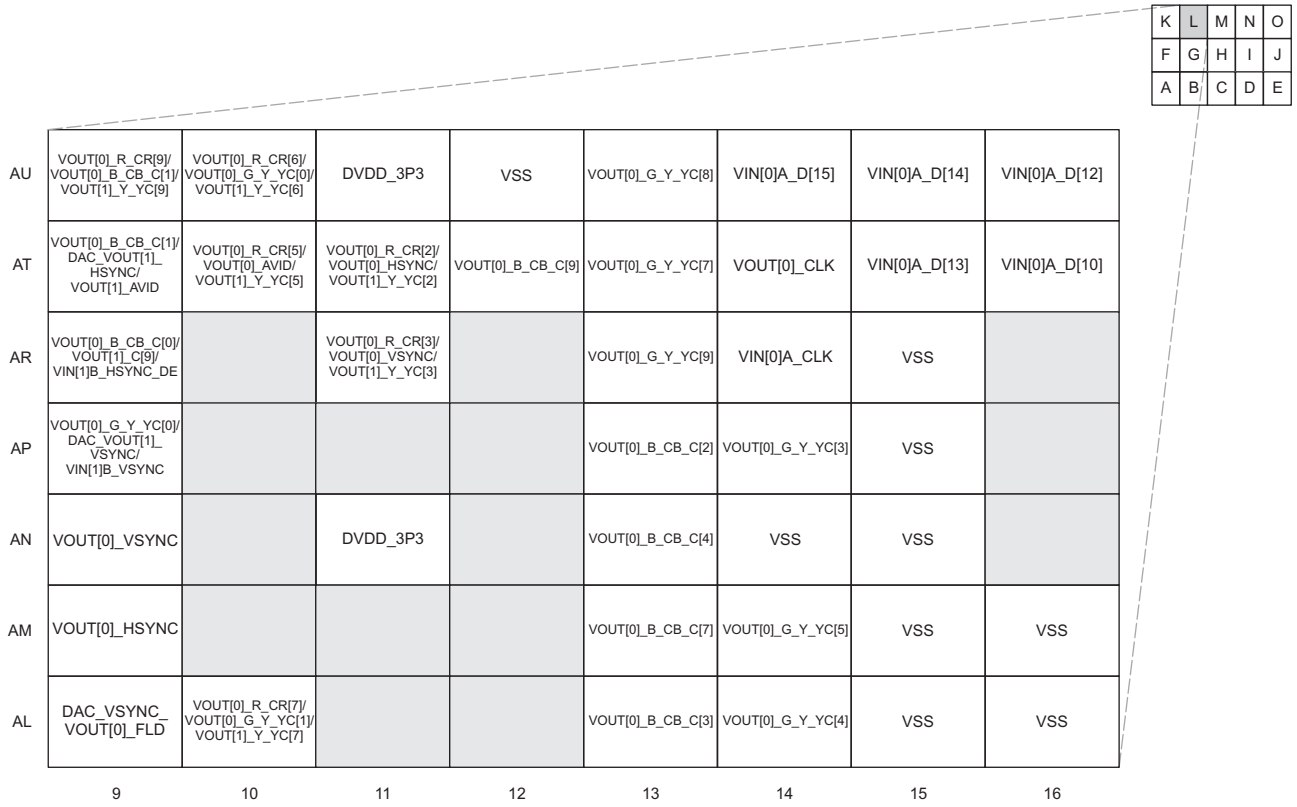



**Figure 4-16. Pin Map [Section L] - Silicon Revision 2.x**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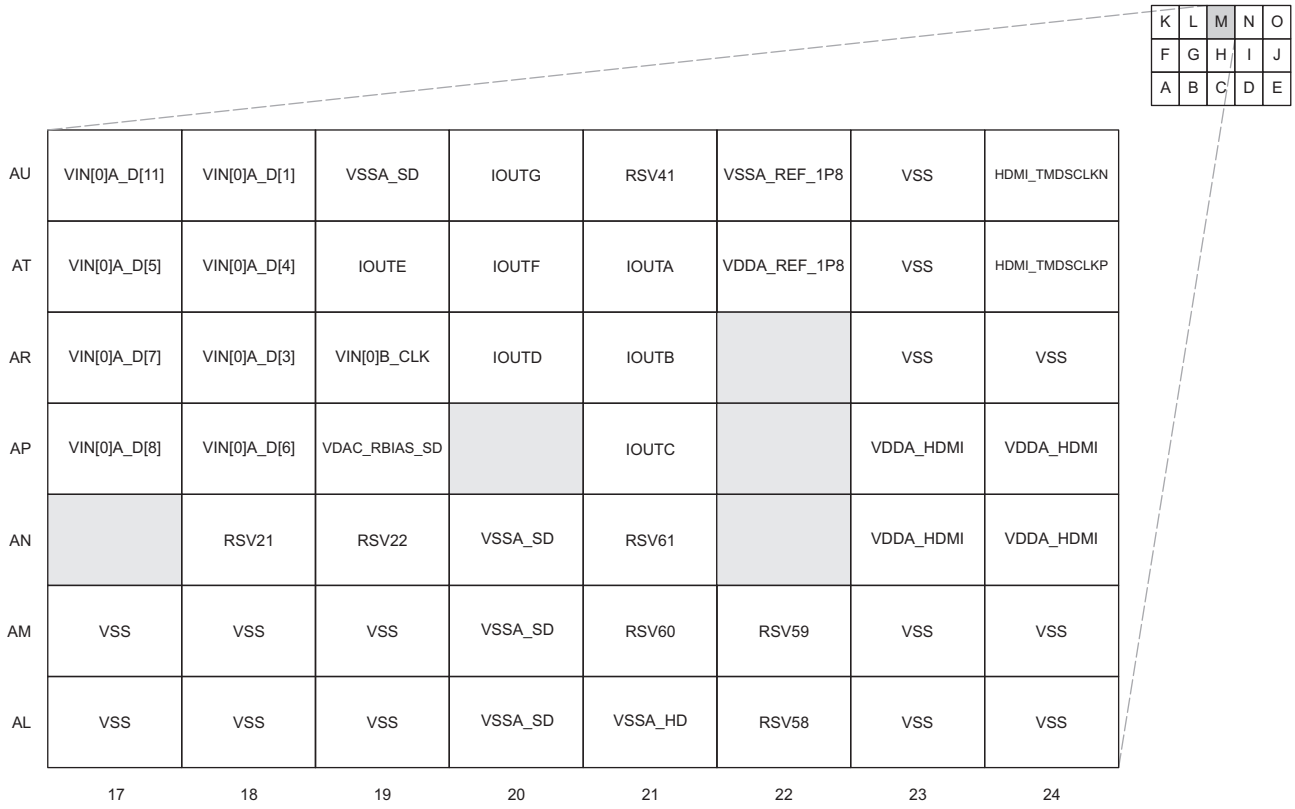


**Figure 4-17. Pin Map [Section M]**

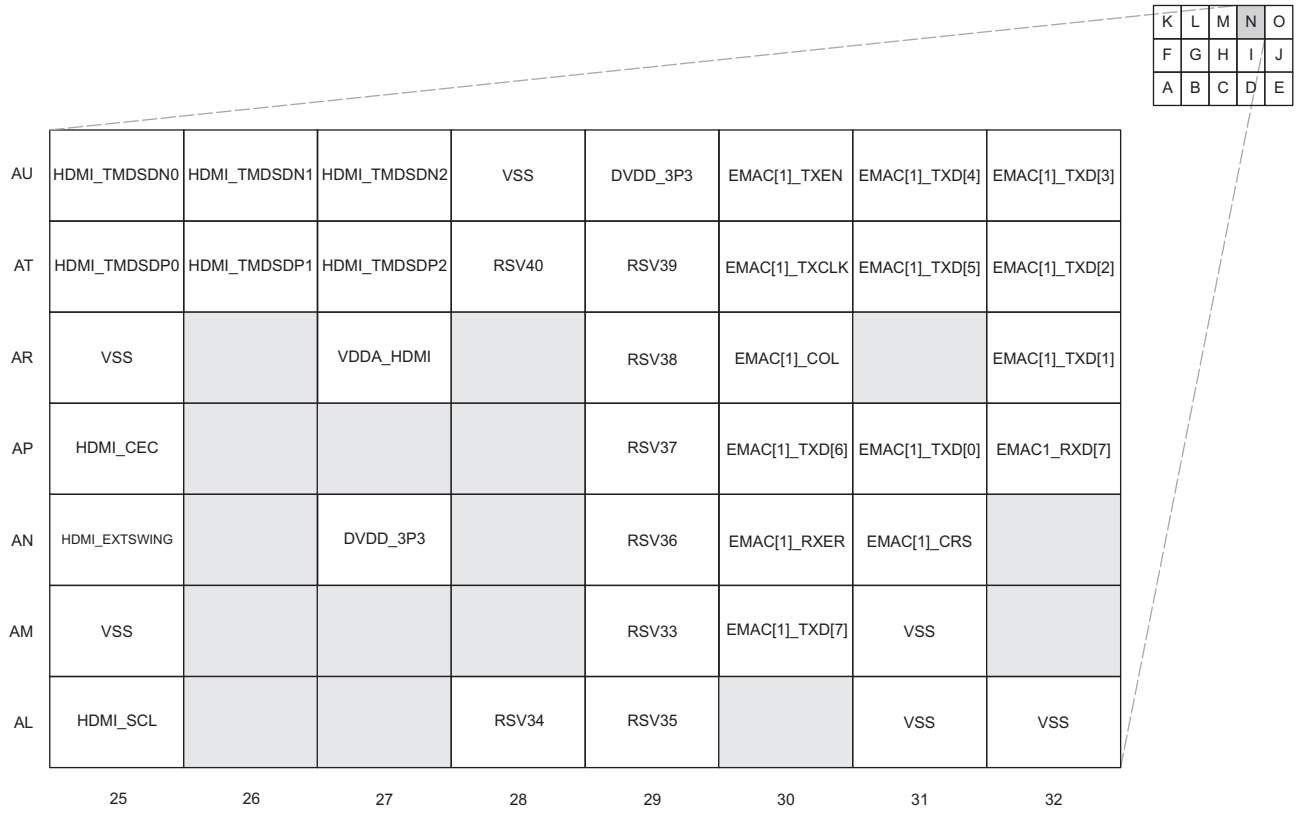


**Figure 4-18. Pin Map [Section N]**


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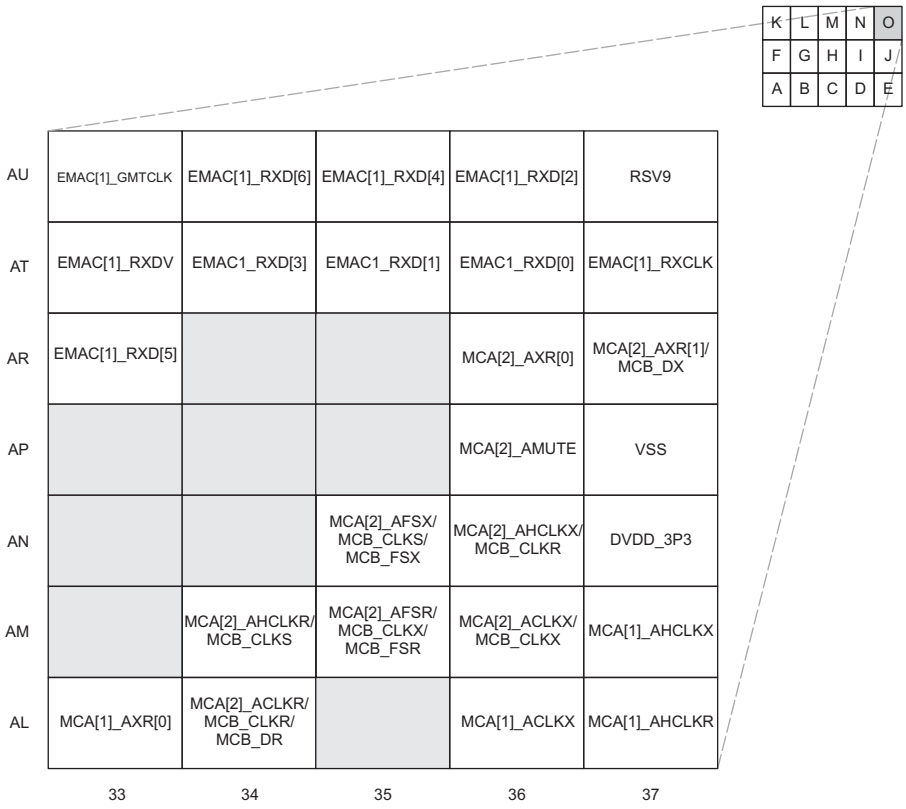


**Figure 4-19. Pin Map [Section O]**

## 4.2 Terminal Functions

The terminal functions tables identify the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors, and a functional pin description. Bolded pin names denote the muxed pin function being described in each table. For more detailed information on device configurations, peripheral selection, multiplexed pin, and shared pin see Section 6, *Device Configurations*.

### 4.2.1 Boot Configuration

**Table 4-1. Boot Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **BOOT** | | | | | |
| Boot Mode inputs. Select the peripheral over which the Host ARM Cortex™-A8 will boot. | | | | | |
| GPMC_A[5]/GPO[13]/ **BTMODE[4]** | AE2 | I | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, GP0 PINCTRL226 | Boot Mode Selection pins. For boot mode information, see Table 6-6. |
| GPMC_A[4]/GPO[12]/ **BTMODE[3]** | AE1 | | | GPMC, GP0 PINCTRL225 | |
| GPMC_A[3]/GPO[11]/ **BTMODE[2]** | AE3 | | | GPMC, GP0 PINCTRL224 | |
| GPMC_A[2]/GPO[10]/ **BTMODE[1]** | AE4 | | | GPMC, GP0 PINCTRL223 | |
| GPMC_A[1]/GPO[9]/ **BTMODE[0]** | AE5 | | | GPMC, GP0 PINCTRL222 | |
| **DEVICE CONTROL** | | | | | |
| GPMC_A[8]/GPO[16]/ **CS0BW** | AD4 | I | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, GP0 PINCTRL229 | GPMC CS0 default Data Bus Width input<br>0 = 8-bit data bus<br>1 = 16-bit data bus<br>The CS0BW pin is also used by the ROM bootloader to set up the size of BAR ranges in PCIe boot mode.(4) |
| GPMC_A[7]/GPO[15]/ **CS0MUX[1]** | AD3 | I | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, GP0 PINCTRL228 | GPMC CS0 default Address/Data multiplexing mode input<br>00 = Not multiplexed<br>01 = A/A/D muxed<br>10 = A/D muxed<br>11 = Reserved<br>The CS0MUX[1:0] pins are also used by the ROM bootloader to set up the size of BAR ranges in PCIe boot mode.(4) |
| GPMC_A[6]/GPO[14]/ **CS0MUX[0]** | AD8 | | | GPMC, GP0 PINCTRL227 | |
| GPMC_A[9]/GPO[17]/ **CS0WAIT** | AD2 | I | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, GP0 PINCTRL230 | GPMC CS0 default GPMC_Wait enable input<br>0 = Wait disabled<br>1 = Wait enabled<br>The CS0WAIT pin is also used by the ROM bootloader to set up the size of BAR ranges in PCIe boot mode.(4) |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.
(4) For details on the BAR ranges setup, see the ROM Code Memory and Peripheral Booting chapter of the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).


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### 4.2.2 DDR2 and DDR3 Memory Controller Signals

**Table 4-2. DDR2 and DDR3 Memory Controller 0 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) | DESCRIPTION |
|---|---|---|---|---|
| DDR[0]_CLK[0] | B12 | O | DVDD_DDR[0] | DDR[0] Clock 0 |
| $\overline{\text{DDR[0]_CLK[0]}}$ | A12 | O | DVDD_DDR[0] | DDR[0] Negative Clock 0 |
| DDR[0]_CLK[1] | A15 | O | DVDD_DDR[0] | DDR[0] Clock 1 |
| $\overline{\text{DDR[0]_CLK[1]}}$ | B15 | O | DVDD_DDR[0] | DDR[0] Negative Clock 1 |
| DDR[0]_CKE | C18 | O | DVDD_DDR[0] | DDR[0] Clock Enable |
| $\overline{\text{DDR[0]_WE}}$ | E13 | O | DVDD_DDR[0] | DDR[0] Write Enable |
| $\overline{\text{DDR[0]_CS[0]}}$ | B17 | O | DVDD_DDR[0] | DDR[0] Chip Select 0 |
| $\overline{\text{DDR[0]_CS[1]}}$ | F18 | O | DVDD_DDR[0] | DDR[0] Chip Select 1 |
| $\overline{\text{DDR[0]_RAS}}$ | D13 | O | DVDD_DDR[0] | DDR[0] Row Address Strobe output |
| $\overline{\text{DDR[0]_CAS}}$ | C13 | O | DVDD_DDR[0] | DDR[0] Column Address Strobe output |
| DDR[0]_DQM[3] | D9 | O | DVDD_DDR[0] | DDR[0] Data Mask outputs<br>DDR[0]_DQM[3]: For upper byte data bus DDR[0]_D[31:24]<br>DDR[0]_DQM[2]: For DDR[0]_D[23:16]<br>DDR[0]_DQM[1]: For DDR[0]_D[15:8]<br>DDR[0]_DQM[0]: For lower byte data bus DDR[0]_D[7:0] |
| DDR[0]_DQM[2] | G9 | O | DVDD_DDR[0] | |
| DDR[0]_DQM[1] | B5 | O | DVDD_DDR[0] | |
| DDR[0]_DQM[0] | C2 | O | DVDD_DDR[0] | |
| DDR[0]_DQS[3] | B9 | IO | DVDD_DDR[0] | Data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR[0] memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>DDR[0]_DQS[3]: For upper byte data bus DDR[0]_D[31:24]<br>DDR[0]_DQS[2]: For DDR[0]_D[23:16]<br>DDR[0]_DQS[1]: For DDR[0]_D[15:8]<br>DDR[0]_DQS[0]: For lower byte data bus DDR[0]_D[7:0] |
| DDR[0]_DQS[2] | B8 | IO | DVDD_DDR[0] | |
| DDR[0]_DQS[1] | B4 | IO | DVDD_DDR[0] | |
| DDR[0]_DQS[0] | F4 | IO | DVDD_DDR[0] | |
| $\overline{\text{DDR[0]_DQS[3]}}$ | A9 | IO | DVDD_DDR[0] | Complementary data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR[0] memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>$\overline{\text{DDR[0]_DQS[3]}}$: For upper byte data bus DDR[0]_D[31:24]<br>$\overline{\text{DDR[0]_DQS[2]}}$: For DDR[0]_D[23:16]<br>$\overline{\text{DDR[0]_DQS[1]}}$: For DDR[0]_D[15:8]<br>DDR[0]_DQS[0]: For lower byte data bus DDR[0]_D[7:0] |
| $\overline{\text{DDR[0]_DQS[2]}}$ | A8 | IO | DVDD_DDR[0] | |
| $\overline{\text{DDR[0]_DQS[1]}}$ | A4 | IO | DVDD_DDR[0] | |
| $\overline{\text{DDR[0]_DQS[0]}}$ | E3 | IO | DVDD_DDR[0] | |
| DDR[0]_ODT[0] | E18 | O | DVDD_DDR[0] | DDR[0] On-Die Termination for Chip Select 0. |
| DDR[0]_ODT[1] | A16 | O | DVDD_DDR[0] | DDR[0] On-Die Termination for Chip Select 1. |
| $\overline{\text{DDR[0]_RST}}$ | D18 | O | DVDD_DDR[0] | DDR[0] Reset output |
| DDR[0]_BA[2] | N15 | O | DVDD_DDR[0] | DDR[0] Bank Address outputs |
| DDR[0]_BA[1] | B14 | O | DVDD_DDR[0] | |
| DDR[0]_BA[0] | F13 | O | DVDD_DDR[0] | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating IO supply voltage for each signal.

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**Table 4-2. DDR2 and DDR3 Memory Controller 0 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) | DESCRIPTION |
|---|---|---|---|---|
| DDR[0]_A[14] | D17 | O | DVDD_DDR[0] | DDR[0] Address Bus |
| DDR[0]_A[13] | B16 | O | DVDD_DDR[0] | |
| DDR[0]_A[12] | N16 | O | DVDD_DDR[0] | |
| DDR[0]_A[11] | B13 | O | DVDD_DDR[0] | |
| DDR[0]_A[10] | C14 | O | DVDD_DDR[0] | |
| DDR[0]_A[9] | K13 | O | DVDD_DDR[0] | |
| DDR[0]_A[8] | N14 | O | DVDD_DDR[0] | |
| DDR[0]_A[7] | A14 | O | DVDD_DDR[0] | |
| DDR[0]_A[6] | L13 | O | DVDD_DDR[0] | |
| DDR[0]_A[5] | J13 | O | DVDD_DDR[0] | |
| DDR[0]_A[4] | H13 | O | DVDD_DDR[0] | |
| DDR[0]_A[3] | G13 | O | DVDD_DDR[0] | |
| DDR[0]_A[2] | D15 | O | DVDD_DDR[0] | |
| DDR[0]_A[1] | N17 | O | DVDD_DDR[0] | |
| DDR[0]_A[0] | A13 | O | DVDD_DDR[0] | |
| DDR[0]_D[31] | C9 | IO | DVDD_DDR[0] | DDR[0] Data Bus |
| DDR[0]_D[30] | J11 | IO | DVDD_DDR[0] | |
| DDR[0]_D[29] | C11 | IO | DVDD_DDR[0] | |
| DDR[0]_D[28] | G10 | IO | DVDD_DDR[0] | |
| DDR[0]_D[27] | E8 | IO | DVDD_DDR[0] | |
| DDR[0]_D[26] | B10 | IO | DVDD_DDR[0] | |
| DDR[0]_D[25] | B11 | IO | DVDD_DDR[0] | |
| DDR[0]_D[24] | E9 | IO | DVDD_DDR[0] | |
| DDR[0]_D[23] | E7 | IO | DVDD_DDR[0] | |
| DDR[0]_D[22] | F9 | IO | DVDD_DDR[0] | |
| DDR[0]_D[21] | D8 | IO | DVDD_DDR[0] | |
| DDR[0]_D[20] | F8 | IO | DVDD_DDR[0] | |
| DDR[0]_D[19] | B7 | IO | DVDD_DDR[0] | |
| DDR[0]_D[18] | H10 | IO | DVDD_DDR[0] | |
| DDR[0]_D[17] | A7 | IO | DVDD_DDR[0] | |
| DDR[0]_D[16] | C8 | IO | DVDD_DDR[0] | |


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**Table 4-2. DDR2 and DDR3 Memory Controller 0 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) | DESCRIPTION |
|---|---|---|---|---|
| DDR[0]_D[15] | B3 | IO | DVDD_DDR[0] | DDR[0] Data Bus |
| DDR[0]_D[14] | A3 | IO | DVDD_DDR[0] | |
| DDR[0]_D[13] | B6 | IO | DVDD_DDR[0] | |
| DDR[0]_D[12] | A5 | IO | DVDD_DDR[0] | |
| DDR[0]_D[11] | D6 | IO | DVDD_DDR[0] | |
| DDR[0]_D[10] | C6 | IO | DVDD_DDR[0] | |
| DDR[0]_D[9] | D7 | IO | DVDD_DDR[0] | |
| DDR[0]_D[8] | C5 | IO | DVDD_DDR[0] | |
| DDR[0]_D[7] | C1 | IO | DVDD_DDR[0] | |
| DDR[0]_D[6] | F3 | IO | DVDD_DDR[0] | |
| DDR[0]_D[5] | B2 | IO | DVDD_DDR[0] | |
| DDR[0]_D[4] | D2 | IO | DVDD_DDR[0] | |
| DDR[0]_D[3] | G4 | IO | DVDD_DDR[0] | |
| DDR[0]_D[2] | E2 | IO | DVDD_DDR[0] | |
| DDR[0]_D[1] | F2 | IO | DVDD_DDR[0] | |
| DDR[0]_D[0] | B1 | IO | DVDD_DDR[0] | |
| DDR[0]_VTP | A6 | I | DVDD_DDR[0] | DDR VTP Compensation Resistor Connection |

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## Table 4-3. DDR2 and DDR3 Memory Controller 1 Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) | DESCRIPTION |
|---|---|---|---|---|
| DDR[1]_CLK[0] | B26 | O | DVDD_DDR[1] | DDR[1] Clock 0 |
| DDR[1]_CLK[0] | A26 | O | DVDD_DDR[1] | DDR[1] Negative Clock 0 |
| DDR[1]_CLK[1] | A23 | O | DVDD_DDR[1] | DDR[1] Clock 1 |
| DDR[1]_CLK[1] | B23 | O | DVDD_DDR[1] | DDR[1] Negative Clock 1 |
| DDR[1]_CKE | C20 | O | DVDD_DDR[1] | DDR[1] Clock Enable |
| DDR[1]_WE | E25 | O | DVDD_DDR[1] | DDR[1] Write Enable |
| DDR[1]_CS[0] | B21 | O | DVDD_DDR[1] | DDR[1] Chip Select 0 |
| DDR[1]_CS[1] | F20 | O | DVDD_DDR[1] | DDR[1] Chip Select 1 |
| DDR[1]_RAS | D25 | O | DVDD_DDR[1] | DDR[1] Row Address Strobe output |
| DDR[1]_CAS | C25 | O | DVDD_DDR[1] | DDR[1] Column Address Strobe output |
| DDR[1]_DQM[3] | D29 | O | DVDD_DDR[1] | DDR[1] Data Mask outputs<br>DDR[1]_DQM[3]: For upper byte data bus DDR[1]_D[31:24]<br>DDR[1]_DQM[2]: For DDR[1]_D[23:16]<br>DDR[1]_DQM[1]: For DDR[1]_D[15:8]<br>DDR[1]_DQM[0]: For lower byte data bus DDR[1]_D[7:0] |
| DDR[1]_DQM[2] | G29 | O | DVDD_DDR[1] | |
| DDR[1]_DQM[1] | B33 | O | DVDD_DDR[1] | |
| DDR[1]_DQM[0] | C36 | O | DVDD_DDR[1] | |
| DDR[1]_DQS[3] | B29 | O | DVDD_DDR[1] | Data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR[1] memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>DDR[1]_DQS[3]: For upper byte data bus DDR[1]_D[31:24]<br>DDR[1]_DQS[2]: For DDR[1]_D[23:16]<br>DDR[1]_DQS[1]: For DDR[1]_D[15:8]<br>DDR[1]_DQS[0]: For lower byte data bus DDR[1]_D[7:0] |
| DDR[1]_DQS[2] | B30 | IO | DVDD_DDR[1] | |
| DDR[1]_DQS[1] | B34 | IO | DVDD_DDR[1] | |
| DDR[1]_DQS[0] | F34 | IO | DVDD_DDR[1] | |
| DDR[1]_DQS[3] | A29 | IO | DVDD_DDR[1] | Complementary data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR[1] memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>DDR[1]_DQS[3]: For upper byte data bus DDR[1]_D[31:24]<br>DDR[1]_DQS[2]: For DDR[1]_D[23:16]<br>DDR[1]_DQS[1]: For DDR[1]_D[15:8]<br>DDR[1]_DQS[0]: For lower byte data bus DDR[1]_D[7:0] |
| DDR[1]_DQS[2] | A30 | IO | DVDD_DDR[1] | |
| DDR[1]_DQS[1] | A34 | IO | DVDD_DDR[1] | |
| DDR[1]_DQS[0] | E35 | IO | DVDD_DDR[1] | |
| DDR[1]_ODT[0] | E20 | O | DVDD_DDR[1] | DDR[1] On-Die Termination for Chip Select 0. |
| DDR[1]_ODT[1] | A22 | O | DVDD_DDR[1] | DDR[1] On-Die Termination for Chip Select 1. |
| DDR[1]_RST | D20 | O | DVDD_DDR[1] | DDR[1] Reset output |
| DDR[1]_BA[2] | N23 | O | DVDD_DDR[1] | DDR[1] Bank Address outputs |
| DDR[1]_BA[1] | B24 | O | DVDD_DDR[1] | |
| DDR[1]_BA[0] | F25 | O | DVDD_DDR[1] | |
| DDR[1]_A[14] | D21 | O | DVDD_DDR[1] | DDR[1] Address Bus |
| DDR[1]_A[13] | B22 | O | DVDD_DDR[1] | |
| DDR[1]_A[12] | N22 | O | DVDD_DDR[1] | |
| DDR[1]_A[11] | B25 | O | DVDD_DDR[1] | |
| DDR[1]_A[10] | C24 | O | DVDD_DDR[1] | |
| DDR[1]_A[9] | K25 | O | DVDD_DDR[1] | |
| DDR[1]_A[8] | N24 | O | DVDD_DDR[1] | |
| DDR[1]_A[7] | A24 | O | DVDD_DDR[1] | |
| DDR[1]_A[6] | L25 | O | DVDD_DDR[1] | |
| DDR[1]_A[5] | J25 | O | DVDD_DDR[1] | |
| DDR[1]_A[4] | H25 | O | DVDD_DDR[1] | |
| DDR[1]_A[3] | G25 | O | DVDD_DDR[1] | |
| DDR[1]_A[2] | D23 | O | DVDD_DDR[1] | |
| DDR[1]_A[1] | N21 | O | DVDD_DDR[1] | |
| DDR[1]_A[0] | A25 | O | DVDD_DDR[1] | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating IO supply voltage for each signal.


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**Table 4-3. DDR2 and DDR3 Memory Controller 1 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] | DESCRIPTION |
|---|---|---|---|---|
| DDR[1]_D[31] | C29 | IO | DVDD_DDR[1] | DDR[1] Data Bus |
| DDR[1]_D[30] | J27 | IO | DVDD_DDR[1] | |
| DDR[1]_D[29] | C27 | IO | DVDD_DDR[1] | |
| DDR[1]_D[28] | G28 | IO | DVDD_DDR[1] | |
| DDR[1]_D[27] | E30 | IO | DVDD_DDR[1] | |
| DDR[1]_D[26] | B28 | IO | DVDD_DDR[1] | |
| DDR[1]_D[25] | B27 | IO | DVDD_DDR[1] | |
| DDR[1]_D[24] | E29 | IO | DVDD_DDR[1] | |
| DDR[1]_D[23] | E31 | IO | DVDD_DDR[1] | |
| DDR[1]_D[22] | F29 | IO | DVDD_DDR[1] | |
| DDR[1]_D[21] | D30 | IO | DVDD_DDR[1] | |
| DDR[1]_D[20] | F30 | IO | DVDD_DDR[1] | |
| DDR[1]_D[19] | B31 | IO | DVDD_DDR[1] | |
| DDR[1]_D[18] | H28 | IO | DVDD_DDR[1] | |
| DDR[1]_D[17] | A31 | IO | DVDD_DDR[1] | |
| DDR[1]_D[16] | C30 | IO | DVDD_DDR[1] | |
| DDR[1]_D[15] | B35 | IO | DVDD_DDR[1] | DDR[1] Data Bus |
| DDR[1]_D[14] | A35 | IO | DVDD_DDR[1] | |
| DDR[1]_D[13] | B32 | IO | DVDD_DDR[1] | |
| DDR[1]_D[12] | A33 | IO | DVDD_DDR[1] | |
| DDR[1]_D[11] | D32 | IO | DVDD_DDR[1] | |
| DDR[1]_D[10] | C32 | IO | DVDD_DDR[1] | |
| DDR[1]_D[9] | D31 | IO | DVDD_DDR[1] | |
| DDR[1]_D[8] | C33 | IO | DVDD_DDR[1] | |
| DDR[1]_D[7] | C37 | IO | DVDD_DDR[1] | |
| DDR[1]_D[6] | F35 | IO | DVDD_DDR[1] | |
| DDR[1]_D[5] | B36 | IO | DVDD_DDR[1] | |
| DDR[1]_D[4] | D36 | IO | DVDD_DDR[1] | |
| DDR[1]_D[3] | G34 | IO | DVDD_DDR[1] | |
| DDR[1]_D[2] | E36 | IO | DVDD_DDR[1] | |
| DDR[1]_D[1] | F36 | IO | DVDD_DDR[1] | |
| DDR[1]_D[0] | B37 | IO | DVDD_DDR[1] | |
| DDR[1]_VTP | A32 | I | DVDD_DDR[1] | DDR VTP Compensation Resistor Connection |

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### 4.2.3 Ethernet Media Access Controller (EMAC) Signals

**Table 4-4. EMAC Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| MDIO_MCLK | AH37 | O | PULL: IPU / IPU<br>DRIVE: H / H<br>DVDD_3P3 | -<br>PINCTRL275 | Management Data Serial Clock output |
| MDIO_MDIO | AH36 | IO | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL276 | Management Data IO |
| **EMAC0** | | | | | |
| EMAC[0]_COL | AB25 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL251 | [G]MII Collision Detect (Sense) input |
| EMAC[0]_CRS | AA25 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL252 | [G]MII Carrier Sense input |
| EMAC[0]_GMTCLK | AC37 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL253 | GMII Source Asynchronous Transmit Clock |
| EMAC[0]_RXCLK | AE37 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL254 | [G]MII Receive Clock |
| EMAC[0]_RXD[7] | AE36 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL262 | [G]MII Receive Data [7:0]. For 1000 EMAC GMII operation, EMAC[0]_RXD[7:0] are used. For 10/100 EMAC MII operation, *only* EMAC[0]_RXD[3:0] are used. |
| EMAC[0]_RXD[6] | AC25 | | | -<br>PINCTRL261 | |
| EMAC[0]_RXD[5] | AD25 | | | -<br>PINCTRL260 | |
| EMAC[0]_RXD[4] | AC35 | | | -<br>PINCTRL259 | |
| EMAC[0]_RXD[3] | AD35 | | | -<br>PINCTRL258 | |
| EMAC[0]_RXD[2] | AC36 | | | -<br>PINCTRL257 | |
| EMAC[0]_RXD[1] | AD36 | | | -<br>PINCTRL256 | |
| EMAC[0]_RXD[0] | AD37 | | | -<br>PINCTRL255 | |
| EMAC[0]_RXDV | AE35 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL263 | [G]MII Receive Data Valid input |
| EMAC[0]_RXER | AE34 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL264 | [G]MII Receive Data Error input |
| EMAC[0]_TXCLK | AF37 | I | PULL: IPD / DIS<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL265 | [G]MII Transmit Clock input |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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**Table 4-4. EMAC Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMAC[0]_TXD[7] | AG35 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | - PINCTRL273 | [G]MII Transmit Data [7:0]. For 1000 EMAC GMII operation, EMAC[0]_TXD[7:0] are used. For 10/100 EMAC MII operation, *only* EMAC[0]_TXD[3:0] are used. |
| EMAC[0]_TXD[6] | AG36 | | | - PINCTRL272 | |
| EMAC[0]_TXD[5] | AF36 | | | - PINCTRL271 | |
| EMAC[0]_TXD[4] | AG28 | | | - PINCTRL270 | |
| EMAC[0]_TXD[3] | AE30 | | | - PINCTRL269 | |
| EMAC[0]_TXD[2] | AE31 | | | - PINCTRL268 | |
| EMAC[0]_TXD[1] | AE32 | | | - PINCTRL267 | |
| EMAC[0]_TXD[0] | AE33 | | | - PINCTRL266 | |
| EMAC[0]_TXEN | AG37 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | - PINCTRL274 | [G]MII Transmit Data Enable output |
| **EMAC1** | | | | | |
| EMAC[1]_COL | AR30 | I | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | - PINCTRL72 | [G]MII Collision Detect (Sense) input |
| EMAC[1]_CRS | AN31 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | - PINCTRL73 | [G]MII Carrier Sense input |
| EMAC[1]_GMTCLK | AU33 | O | PULL: IPD / DIS<br>DRIVE: Z / Z<br>DVDD_3P3 | - PINCTRL61 | GMII Source Asynchronous Transmit Clock |
| EMAC[1]_RXCLK | AT37 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | - PINCTRL51 | [G]MII Receive Clock |
| EMAC[1]_RXD[7] | AP32 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | - PINCTRL59 | [G]MII Receive Data [7:0]. For 1000 EMAC GMII operation, EMAC[1]_RXD[7:0] are used. For 10/100 EMAC MII operation, *only* EMAC[1]_RXD[3:0] are used. |
| EMAC[1]_RXD[6] | AU34 | | | - PINCTRL58 | |
| EMAC[1]_RXD[5] | AR33 | | | - PINCTRL57 | |
| EMAC[1]_RXD[4] | AU35 | | | - PINCTRL56 | |
| EMAC[1]_RXD[3] | AT34 | | | - PINCTRL55 | |
| EMAC[1]_RXD[2] | AU36 | | | - PINCTRL54 | |
| EMAC[1]_RXD[1] | AT35 | | | - PINCTRL53 | |
| EMAC[1]_RXD[0] | AT36 | | | - PINCTRL52 | |
| EMAC[1]_RXDV | AT33 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | - PINCTRL60 | [G]MII Receive Data Valid input |
| EMAC[1]_RXER | AN30 | I | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | - PINCTRL74 | [G]MII Receive Data Error input |

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**Table 4-4. EMAC Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMAC[1]_TXCLK | AT30 | I | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL71 | [G]MII Transmit Clock input |
| EMAC[1]_TXD[7] | AM30 | O | PULL: IPD / DIS<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL69 | [G]MII Transmit Data [7:0]. For 1000 EMAC GMII operation, EMAC[1]_TXD[7:0] are used. For 10/100 EMAC MII operation, *only* EMAC[1]_TXD[3:0] are used. |
| EMAC[1]_TXD[6] | AP30 | | | -<br>PINCTRL68 | |
| EMAC[1]_TXD[5] | AT31 | | | -<br>PINCTRL67 | |
| EMAC[1]_TXD[4] | AU31 | | | -<br>PINCTRL66 | |
| EMAC[1]_TXD[3] | AU32 | | | -<br>PINCTRL65 | |
| EMAC[1]_TXD[2] | AT32 | | | -<br>PINCTRL64 | |
| EMAC[1]_TXD[1] | AR32 | | | -<br>PINCTRL63 | |
| EMAC[1]_TXD[0] | AP31 | | | -<br>PINCTRL62 | |
| EMAC[1]_TXEN | AU30 | O | PULL: IPD / DIS<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL70 | [G]MII Transmit Data Enable output |


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### 4.2.4 General-Purpose Input/Output (GPIO) Signals

**Table 4-5. GPIO Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPIO0** | | | | | |
| **Note:** General-Purpose Input/Output (IO) pins can also serve as external interrupt inputs. | | | | | |
| TIM7_OUT/ GPMC_A[12]/ **GP0[31]** | G1 | IO | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | TIM7, GPMC PINCTRL206 | General-Purpose Input/Output (IO) 0 [GP0] pin 31. |
| TIM6_OUT/ GPMC_A[24]/ **GP0[30]** | H1 | IO | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | TIM6, GPMC PINCTRL205 | General-Purpose Input/Output (IO) 0 [GP0] pin 30. |
| TIM5_OUT/ **GP0[29]** | H34 | IO | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | TIM5 PINCTRL204 | General-Purpose Input/Output (IO) 0 [GP0] pin 29. |
| TIM4_OUT/ **GP0[28]** | H33 | IO | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | TIM4 PINCTRL203 | General-Purpose Input/Output (IO) 0 [GP0] pin 28. |
| GPMC_A[12]/ **GP0[27]** | H2 | IO | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GPMC PINCTRL202 | General-Purpose Input/Output (IO) 0 [GP0] pin 27. |
| GPMC_A[21]/ **GP0[26]** | H3 | IO | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GPMC PINCTRL201 | General-Purpose Input/Output (IO) 0 [GP0] pin 26. |
| **GP0[25]** | H4 | IO | PULL: IPU / DIS DRIVE: H / L DVDD_3P3 | - PINCTRL200 | General-Purpose Input/Output (IO) 0 [GP0] pin 25. |
| GPMC_A[13]/ **GP0[24]** | H6 | IO | PULL: IPU / IPD DRIVE: H / L DVDD_3P3 | GPMC PINCTRL199 | General-Purpose Input/Output (IO) 0 [GP0] pin 24. |
| GPMC_A[14]/ **GP0[23]** | H5 | IO | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | GPMC PINCTRL198 | General-Purpose Input/Output (IO) 0 [GP0] pin 23. |
| GPMC_A[15]/ **GP0[22]** | J1 | IO | PULL: IPU / DIS DRIVE: H / L DVDD_3P3 | GPMC PINCTRL197 | General-Purpose Input/Output (IO) 0 [GP0] pin 22. |
| GPMC_A[16]/ **GP0[21]** | J2 | IO | PULL: DIS / IPD DRIVE: Z / Z DVDD_3P3 | GPMC PINCTRL196 | General-Purpose Input/Output (IO) 0 [GP0] pin 21. |
| GPMC_A[27]/ **GP0[20]** | AC5 | IO | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GPMC PINCTRL233 | General-Purpose Input/Output (IO) 0 [GP0] pin 20. |
| GPMC_A[11]/ **GP0[19]** | AC2 | IO | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GPMC PINCTRL232 | General-Purpose Input/Output (IO) 0 [GP0] pin 19. |
| GPMC_A[10]/ **GP0[18]** | AD1 | IO | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GPMC PINCTRL231 | General-Purpose Input/Output (IO) 0 [GP0] pin 18. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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**Table 4-5. GPIO Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| GPMC_A[9]/ **GP0[17]**/ CS0WAIT | AD2 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL230 | General-Purpose Input/Output (IO) 0 [GP0] pin 17. |
| GPMC_A[8]/ **GP0[16]**/ CS0BW | AD4 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL229 | General-Purpose Input/Output (IO) 0 [GP0] pin 16. |
| GPMC_A[7]/ **GP0[15]**/ CS0MUX[1] | AD3 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL228 | General-Purpose Input/Output (IO) 0 [GP0] pin 15. |
| GPMC_A[6]/ **GP0[14]**/ CS0MUX[0] | AD8 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL227 | General-Purpose Input/Output (IO) 0 [GP0] pin 14. |
| GPMC_A[5]/ **GP0[13]**/ BTMODE[4] | AE2 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL226 | General-Purpose Input/Output (IO) 0 [GP0] pin 13. |
| GPMC_A[4]/ **GP0[12]**/ BTMODE[3] | AE1 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL225 | General-Purpose Input/Output (IO) 0 [GP0] pin 12. |
| GPMC_A[3]/ **GP0[11]**/ BTMODE[2] | AE3 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL224 | General-Purpose Input/Output (IO) 0 [GP0] pin 11. |
| GPMC_A[2]/ **GP0[10]**/ BTMODE[1] | AE4 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL223 | General-Purpose Input/Output (IO) 0 [GP0] pin 10. |
| GPMC_A[1]/ **GP0[9]**/ BTMODE[0] | AE5 | IO | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, BOOT PINCTRL222 | General-Purpose Input/Output (IO) 0 [GP0] pin 9. |
| GPMC_A[0]/ **GP0[8]** | AE6 | IO | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GPMC PINCTRL221 | General-Purpose Input/Output (IO) 0 [GP0] pin 8. |
| **GP0[7]**/ MCA[0]_AMUTEIN | H35 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[0] PINCTRL298 | General-Purpose Input/Output (IO) 0 [GP0] pin 7. |
| **GP0[6]**/ MCA[1]_AMUTEIN/ GPMC_A[23] | G5 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[1], GPMC PINCTRL297 | General-Purpose Input/Output (IO) 0 [GP0] pin 6. |
| **GP0[5]**/ MCA[2]_AMUTEIN/ GPMC_A[24] | G2 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2], GPMC PINCTRL296 | General-Purpose Input/Output (IO) 0 [GP0] pin 5. |
| **GP0[4]** | H32 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL295 | General-Purpose Input/Output (IO) 0 [GP0] pin 4. |
| **GP0[3]**/ TCLKIN | J31 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | Timer CLKIN PINCTRL294 | General-Purpose Input/Output (IO) 0 [GP0] pin 3. |
| GP0[2] | K30 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL293 | General-Purpose Input/Output (IO) 0 [GP0] pin 2. |
| GP0[1] | L29 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL292 | General-Purpose Input/Output (IO) 0 [GP0] pin 1. |
| GP0[0] | K31 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL291 | General-Purpose Input/Output (IO) 0 [GP0] pin 0. |


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**Table 4-5. GPIO Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPIO1** | | | | | |
| **Note:** General-Purpose Input/Output (IO) pins can also serve as external interrupt inputs. | | | | | |
| **GP1[31]**/ SATA_ACT1_LED (silicon revision 1.x) SATA_ACT0_LED (silicon revision 2.x) | J33 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SATA PINCTRL300 | General-Purpose Input/Output (IO) 1 [GP1] pin 31. |
| **GP1[30]**/ SATA_ACT0_LED (silicon revision 1.x) SATA_ACT1_LED (silicon revision 2.x) | J32 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SATA PINCTRL299 | General-Purpose Input/Output (IO) 1 [GP1] pin 30. |
| GPMC_CLK/ **GP1[29]** | V1 | IO | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | GPMC PINCTRL250 | General-Purpose Input/Output (IO) 1 [GP1] pin 29. |
| $\overline{\text{UART0_CTS}}$/ **GP1[28]** | N7 | IO | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0 PINCTRL176 | General-Purpose Input/Output (IO) 1 [GP1] pin 28. |
| $\overline{\text{UART0_RTS}}$/ **GP1[27]** | N9 | IO | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART0 PINCTRL175 | General-Purpose Input/Output (IO) 1 [GP1] pin 27. |
| $\overline{\text{UART1_CTS}}$/ GPMC_A[13]/ GPMC_A[17]/ **GP1[26]** | L3 | IO | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART1, GPMC PINCTRL184 | General-Purpose Input/Output (IO) 1 [GP1] pin 26. |
| $\overline{\text{UART1_RTS}}$/ GPMC_A[14]/ GPMC_A[18]/ **GP1[25]** | M2 | IO | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART1, GPMC PINCTRL183 | General-Purpose Input/Output (IO) 1 [GP1] pin 25. |
| $\overline{\text{UART2_CTS}}$/ GPMC_A[16]/ GPMC_A[25]/ **GP1[24]** | K7 | IO | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART2, GPMC PINCTRL188 | General-Purpose Input/Output (IO) 1 [GP1] pin 24. |
| $\overline{\text{UART2_RTS}}$/ GPMC_A[15]/ GPMC_A[26]/ **GP1[23]** | L9 | IO | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART2, GPMC PINCTRL187 | General-Purpose Input/Output (IO) 1 [GP1] pin 23. |
| $\overline{\text{SPI_SCS[3]}}$/ **GPMC_A[21]**/ GP1[22] | P1 | IO | PULL: DIS / IPU DRIVE: Z / Z DVDD_3P3 | SPI, GPMC PINCTRL170 | General-Purpose Input/Output (IO) 1 [GP1] pin 22. |
| $\overline{\text{GPMC_CS[4]}}$/ **GP1[21]** | AG3 | IO | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | GPMC PINCTRL211 | General-Purpose Input/Output (IO) 1 [GP1] pin 21. |
| GPMC_DIR/ **GP1[20]** | AE7 | IO | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GPMC PINCTRL218 | General-Purpose Input/Output (IO) 1 [GP1] pin 20. |
| UART0_RIN/ GPMC_A[17]/ GPMC_A[22]/ **GP1[19]** | N3 | IO | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC PINCTRL180 | General-Purpose Input/Output (IO) 1 [GP1] pin 19. |
| $\overline{\text{UART0_DCD}}$/ GPMC_A[18]/ GPMC_A[23]/ **GP1[18]** | N5 | IO | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC PINCTRL179 | General-Purpose Input/Output (IO) 1 [GP1] pin 18. |
| $\overline{\text{UART0_DSR}}$/ GPMC_A[19]/ GPMC_A[24]/ **GP1[17]** | N4 | IO | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC PINCTRL178 | General-Purpose Input/Output (IO) 1 [GP1] pin 17. |

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**Table 4-5. GPIO Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| UART0_DTR/ GPMC_A[20]/ GPMC_A[12]/ **GP1[16]** | N6 | IO | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART0, GPMC PINCTRL177 | General-Purpose Input/Output (IO) 1 [GP1] pin 16. |
| **GPMC_A[24]**/ **GP1[15]** | J3 | IO | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GPMC PINCTRL195 | General-Purpose Input/Output (IO) 1 [GP1] pin 15. |
| GPMC_A[23]/ **GP1[14]** | J4 | IO | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GPMC PINCTRL194 | General-Purpose Input/Output (IO) 1 [GP1] pin 14. |
| **GP1[13]** | J5 | IO | PULL: IPU / DIS DRIVE: H / L DVDD_3P3 | - PINCTRL193 | General-Purpose Input/Output (IO) 1 [GP1] pin 13. |
| GPMC_A[25]/ **GP1[12]** | J7 | IO | PULL: IPU / IPD DRIVE: H / L DVDD_3P3 | GPMC PINCTRL192 | General-Purpose Input/Output (IO) 1 [GP1] pin 12. |
| GPMC_A[26]/ **GP1[11]** | J6 | IO | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | GPMC PINCTRL191 | General-Purpose Input/Output (IO) 1 [GP1] pin 11. |
| GPMC_A[22]/ **GP1[10]** | K2 | IO | PULL: IPU / DIS DRIVE: H / L DVDD_3P3 | GPMC PINCTRL190 | General-Purpose Input/Output (IO) 1 [GP1] pin 10. |
| GPMC_A[27]/ **GP1[9]** | K8 | IO | PULL: DIS / IPD DRIVE: Z / Z DVDD_3P3 | GPMC PINCTRL189 | General-Purpose Input/Output (IO) 1 [GP1] pin 9. |
| SD_SDWP/ GPMC_A[15]/ **GP1[8]** | R5 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GPMC PINCTRL165 | General-Purpose Input/Output (IO) 1 [GP1] pin 8. |
| SD_SDCD/ GPMC_A[16]/ **GP1[7]** | R13 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GPMC PINCTRL164 | General-Purpose Input/Output (IO) 1 [GP1] pin 7. |
| SD_DAT[3]/ GPMC_A[17]/ **GP1[6]** | T13 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GPMC PINCTRL163 | General-Purpose Input/Output (IO) 1 [GP1] pin 6. |
| SD_DAT[2]_SDRW/ GPMC_A[18]/ **GP1[5]** | T2 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GPMC PINCTRL162 | General-Purpose Input/Output (IO) 1 [GP1] pin 5. |
| SD_DAT[1]_SDIRQ/ GPMC_A[19]/ **GP1[4]** | T1 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GPMC PINCTRL161 | General-Purpose Input/Output (IO) 1 [GP1] pin 4. |
| SD_DAT[0]/ GPMC_A[20]/ **GP1[3]** | U1 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GPMC PINCTRL160 | General-Purpose Input/Output (IO) 1 [GP1] pin 3. |
| SD_CMD/ GPMC_A[21]/ **GP1[2]** | U3 | IO | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | SD, GPMC PINCTRL159 | General-Purpose Input/Output (IO) 1 [GP1] pin 2. |
| SD_CLK/ GPMC_A[13]/ **GP1[1]** | U2 | IO | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | SD, GPMC PINCTRL158 | General-Purpose Input/Output (IO) 1 [GP1] pin 1. |
| SD_POW/ GPMC_A[14]/ **GP1[0]** | U4 | IO | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | SD, GPMC PINCTRL157 | General-Purpose Input/Output (IO) 1 [GP1] pin 0. |


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### 4.2.5 General-Purpose Memory Controller (GPMC) Signals

**Table 4-6. GPMC Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPMC_CLK**/ GP1[29] | V1 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | GP1 | GPMC Clock output |
| **GPMC_CS[5]** / GPMC_A[12] | AG1 | O | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | GPMC PINCTRL212 | GPMC Chip Select 5 |
| **GPMC_CS[4]** / GP1[21] | AG3 | O | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | GP1 PINCTRL211 | GPMC Chip Select 4 |
| GPMC_CS[3] | AG9 | O | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | - PINCTRL210 | GPMC Chip Select 3 |
| GPMC_CS[2] | AH2 | O | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | - PINCTRL209 | GPMC Chip Select 2 |
| GPMC_CS[1] | AH1 | O | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | - PINCTRL208 | GPMC Chip Select 1 |
| GPMC_CS[0] | AH7 | O | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | - PINCTRL207 | GPMC Chip Select 0 |
| GPMC_WE | AG2 | O | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | - PINCTRL213 | GPMC Write Enable output |
| GPMC_OE_RE | AF2 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | - PINCTRL214 | GPMC Output Enable output |
| GPMC_BE1 | AF1 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | - PINCTRL216 | GPMC Upper Byte Enable output |
| GPMC_BE0_CLE | AE11 | O | PULL: IPU / DIS DRIVE: H / L DVDD_3P3 | - PINCTRL215 | GPMC Lower Byte Enable output or Command Latch Enable output |
| GPMC_ADV_ALE | AE10 | O | PULL: IPU / DIS DRIVE: H / L DVDD_3P3 | - PINCTRL217 | GPMC Address Valid output or Address Latch Enable output |
| **GPMC_DIR**/ GP1[20] | AE7 | O | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GP1 PINCTRL218 | GPMC Direction Control for External Transceivers |
| GPMC_WP | AE9 | O | PULL: IPU / IPD DRIVE: H / L DVDD_3P3 | - PINCTRL219 | GPMC Write Protect output |
| GPMC_WAIT | AE8 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL220 | GPMC Wait input |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during POR reset
B is the state of the internal pull resistor after POR and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during POR reset
B is the driving state of the pin after POR and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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**Table 4-6. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPMC_A[27]**/ GP0[20] | AC5 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GP0 PINCTRL233 | GPMC Address 27 |
| **GPMC_A[27]**/ GP1[9] | K8 | O | PULL: DIS / IPD DRIVE: Z / Z DVDD_3P3 | GP1 PINCTRL189 | |
| UART1_RXD/ **GPMC_A[26]**/ GPMC_A[20] | N1 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | UART1, GPMC PINCTRL181 | GPMC Address 26 |
| $\overline{\text{UART2_RTS}}$/ GPMC_A[15]/ **GPMC_A[26]**/ GP1[23] | L9 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART2, GPMC, GP1 PINCTRL187 | |
| **GPMC_A[26]**/ GP1[11] | J6 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | GP1 PINCTRL191 | |
| UART1_TXD/ **GPMC_A[25]**/ GPMC_A[19] | N2 | O | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | UART1, GPMC PINCTRL182 | GPMC Address 25 |
| $\overline{\text{UART2_CTS}}$/ GPMC_A[16]/ **GPMC_A[25]**/ GP1[24] | K7 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART2, GPMC, GP1 PINCTRL188 | |
| **GPMC_A[25]**/ GP1[12] | J7 | O | PULL: IPU / IPD DRIVE: H / L DVDD_3P3 | GP1 PINCTRL192 | |
| GP0[5]/ MCA[2]_AMUTEIN/ **GPMC_A[24]** | G2 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GP0, MCA[2] PINCTRL296 | GPMC Address 24 |
| **GPMC_A[24]**/ GP1[15] | J3 | O | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GP1 PINCTRL195 | |
| TIM6_OUT/ **GPMC_A[24]**/ GP0[30] | H1 | O | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | TIM6, GP0 PINCTRL205 | |
| $\overline{\text{UART0_DSR}}$/ GPMC_A[19]/ **GPMC_A[24]**/ GP1[17] | N4 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC, GP1 PINCTRL178 | |
| GP0[6]/ MCA[1]_AMUTEIN/ **GPMC_A[23]** | G5 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GP0, MCA[1] PINCTRL297 | GPMC Address 23 |
| $\overline{\text{SPI_SCS[1]}}$/ **GPMC_A[23]** | P2 | O | PULL: DIS / IPU DRIVE: Z / Z DVDD_3P3 | SPI PINCTRL168 | |
| $\overline{\text{UART0_DCD}}$/ GPMC_A[18]/ **GPMC_A[23]**/ GP1[18] | N5 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC, GP1 PINCTRL179 | |
| **GPMC_A[23]**/ GP1[14] | J4 | O | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GP1 PINCTRL194 | |


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**Table 4-6. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SPI_SCS[2]/ **GPMC_A[22]** | P3 | O | PULL: DIS / IPU DRIVE: Z / Z DVDD_3P3 | SPI PINCTRL169 | GPMC Address 22 |
| **GPMC_A[22]**/ GP1[10] | K2 | O | PULL: IPU / DIS DRIVE: H / L DVDD_3P3 | GP1 PINCTRL190 | |
| UART0_RIN/ GPMC_A[17]/ **GPMC_A[22]**/ GP1[19] | N3 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC, GP1 PINCTRL180 | |
| SPI_SCS[3]/ **GPMC_A[21]**/ GP1[22] | P1 | O | PULL: DIS / IPU DRIVE: Z / Z DVDD_3P3 | SPI, GP1 PINCTRL170 | GPMC Address 21 |
| SD_CMD/ **GPMC_A[21]**/ GP1[2] | U3 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | SD, GP1 PINCTRL159 | |
| **GPMC_A[21]**/ GP0[26] | H3 | O | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GP0 PINCTRL201 | |
| SD_DAT[0]/ **GPMC_A[20]**/ GP1[3] | U1 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GP1 PINCTRL160 | GPMC Address 20 |
| UART0_DTR/ **GPMC_A[20]**/ GPMC_A[12]/ GP1[16] | N6 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART0, GPMC, GP1 PINCTRL177 | |
| UART1_RXD/ GPMC_A[26]/ **GPMC_A[20]** | N1 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | UART12, GPMC PINCTRL181 | |
| UART0_DSR/ **GPMC_A[19]**/ GPMC_A[24]/ GP1[17] | N4 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC, GP1 PINCTRL178 | GPMC Address 19 |
| SD_DAT[1]_SDIRQ/ **GPMC_A[19]**/ GP1[4] | T1 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GP1 PINCTRL161 | |
| UART1_TXD/ GPMC_A[25]/ **GPMC_A[19]** | N2 | O | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | UART1, GPMC PINCTRL182 | |
| SD_DAT[2]_SDRW/ **GPMC_A[18]**/ GP1[5] | T2 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GP1 PINCTRL162 | GPMC Address 18 |
| UART0_DCD/ **GPMC_A[18]**/ GPMC_A[23]/ GP1[18] | N5 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC, GP1 PINCTRL179 | |
| UART1_RTS/ GPMC_A[14]/ **GPMC_A[18]**/ GP1[25] | M2 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART1, GPMC, GP1 PINCTRL183 | |

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**Table 4-6. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SD_DAT[3]/ **GPMC_A[17]**/ GP1[6] | T13 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GP1 PINCTRL163 | GPMC Address 17 |
| UART0_RIN/ **GPMC_A[17]**/ GPMC_A[22]/ GP1[19] | N3 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART0, GPMC, GP1 PINCTRL180 | |
| $\overline{\text{UART1_CTS}}$/ GPMC_A[13]/ **GPMC_A[17]**/ GP1[26] | L3 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART1, GPMC, GP1 PINCTRL184 | |
| SD_SDCD/ **GPMC_A[16]**/ GP1[7] | R13 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GP1 PINCTRL164 | GPMC Address 16 |
| $\overline{\text{UART2_CTS}}$/ **GPMC_A[16]**/ GPMC_A[25]/ GP1[24] | K7 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART2, GPMC, GP1 PINCTRL188 | |
| **GPMC_A[16]**/ GP0[21] | J2 | O | PULL: DIS / IPD DRIVE: Z / Z DVDD_3P3 | GPMC, GP0 PINCTRL196 | |
| SD_SDWP/ **GPMC_A[15]**/ GP1[8] | R5 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | SD, GP1 PINCTRL165 | GPMC Address 15 |
| $\overline{\text{UART2_RTS}}$/ **GPMC_A[15]**/ GPMC_A[26]/ GP1[23] | L9 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART2, GPMC, GP1 PINCTRL187 | |
| **GPMC_A[15]**/ GP0[22] | J1 | O | PULL: IPU / DIS DRIVE: H / L DVDD_3P3 | GP0 PINCTRL197 | |
| SD_POW/ **GPMC_A[14]**/ GP1[0] | U4 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | SD, GPMC, GP1 PINCTRL157 | GPMC Address 14 |
| $\overline{\text{UART1_RTS}}$/ **GPMC_A[14]**/ GPMC_A[18]/ GP1[25] | M2 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART1, GPMC, GP1 PINCTRL183 | |
| **GPMC_A[14]**/ GP0[23] | H5 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | GP0 PINCTRL198 | |
| SD_CLK/ **GPMC_A[13]** / GP1[1] | U2 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | SD, GP1 PINCTRL158 | GPMC Address 13 |
| $\overline{\text{UART1_CTS}}$/ **GPMC_A[13]**/ GPMC_A[17]/ GP1[26] | L3 | O | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | UART1, GPMC, GP1 PINCTRL184 | |
| **GPMC_A[13]**/ GP0[24] | H6 | O | PULL: IPU / IPD DRIVE: H / L DVDD_3P3 | GP0 PINCTRL199 | |


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**Table 4-6. GPMC Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| UART0_DTR/ GPMC_A[20]/ **GPMC_A[12]**/ GP1[16] | N6 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | UART0, GPMC, GP1 PINCTRL177 | GPMC Address 12 |
| **GPMC_A[12]**/ GP0[27] | H2 | O | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GP0 PINCTRL202 | |
| TIM7_OUT/ **GPMC_A[12]**/ GP0[31] | G1 | O | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | TIM7, GP0 PINCTRL206 | |
| GPMC_CS[5]/ **GPMC_A[12]** | AG1 | O | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | GPMC PINCTRL212 | |
| **GPMC_A[11]**/ GP0[19] | AC2 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GP0 PINCTRL232 | GPMC Address 11 |
| **GPMC_A[10]**/ GP0[18] | AD1 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GP0 PINCTRL231 | GPMC Address 10 |
| **GPMC_A[9]**/ GP0[17]/ CS0WAIT | AD2 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL230 | GPMC Address 9 |
| **GPMC_A[8]**/ GP0[16]/ CS0BW | AD4 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL229 | GPMC Address 8 |
| **GPMC_A[7]**/ GP0[15]/ CS0MUX[1] | AD3 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL228 | GPMC Address 7 |
| **GPMC_A[6]**/ GP0[14]/ CS0MUX[0] | AD8 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL227 | GPMC Address 6 |
| **GPMC_A[5]**/ GP0[13]/ BTMODE[4] | AE2 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL226 | GPMC Address 5 |
| **GPMC_A[4]**/ GP0[12]/ BTMODE[3] | AE1 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL225 | GPMC Address 4 |
| **GPMC_A[3]**/ GP0[11]/ BTMODE[2] | AE3 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL224 | GPMC Address 3 |
| **GPMC_A[2]**/ GP0[10]/ BTMODE[1] | AE4 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL223 | GPMC Address 2 |
| **GPMC_A[1]**/ GP0[9]/ BTMODE[0] | AE5 | O | PULL: IPU / DIS DRIVE: Z / Z DVDD_3P3 | GP0, BOOT PINCTRL222 | GPMC Address 1 |
| **GPMC_A[0]**/ GP0[8] | AE6 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GP0 PINCTRL221 | GPMC Address 0 |

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**Table 4-6. GPMC Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| GPMC_D[15] | V2 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL249 | GPMC Data IOs. Only D[7:0] are used for 8-bit interfaces |
| GPMC_D[14] | V3 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL248 | |
| GPMC_D[13] | V10 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL247 | |
| GPMC_D[12] | W2 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL246 | |
| GPMC_D[11] | W1 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL245 | |
| GPMC_D[10] | W3 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL244 | |
| GPMC_D[9] | Y1 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL243 | |
| GPMC_D[8] | W4 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL242 | |
| GPMC_D[7] | Y2 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL241 | |
| GPMC_D[6] | Y10 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL240 | |
| GPMC_D[5] | AA2 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL239 | |
| GPMC_D[4] | Y3 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL238 | |
| GPMC_D[3] | AA3 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL237 | |
| GPMC_D[2] | AB2 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL236 | |
| GPMC_D[1] | AA4 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL235 | |
| GPMC_D[0] | AC1 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL234 | |


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### 4.2.6 High-Definition Multimedia Interface (HDMI) Signals

**Table 4-7. HDMI Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| HDMI_TMDSCLKP | AT24 | O | - VDDA_HDMI | - | HDMI Clock Output. When the HDMI PHY is powered down, these pins should be left unconnected. |
| HDMI_TMDSCLKN | AU24 | O | - VDDA_HDMI | - | |
| HDMI_TMDSDN2 | AU27 | O | - VDDA_HDMI | - | HDMI Data 2 output. When the HDMI PHY is powered down, these pins should be left unconnected. |
| HDMI_TMDSDP2 | AT27 | O | - VDDA_HDMI | - | |
| HDMI_TMDSDN1 | AU26 | O | - VDDA_HDMI | - | HDMI Data 1 output. When the HDMI PHY is powered down, these pins should be left unconnected. |
| HDMI_TMDSDP1 | AT26 | O | - VDDA_HDMI | - | |
| HDMI_TMDSDN0 | AU25 | O | - VDDA_HDMI | - | HDMI Data 0 output. When the HDMI PHY is powered down, these pins should be left unconnected. |
| HDMI_TMDSDP0 | AT25 | O | - VDDA_HDMI | - | |
| HDMI_SCL | AL25 | O | PULL: DIS / DIS DRIVE: Z / Z DVDD_3P3 | - PINCTRL301 | HDMI I2C Serial Clock Output |
| HDMI_SDA | AK25 | IO | PULL: DIS / DIS DRIVE: Z / Z DVDD_3P3 | - PINCTRL302 | HDMI I2C Serial Data IO |
| HDMI_CEC | AP25 | IO | PULL: IPU / IPU DRIVE: H / H DVDD_3P3 | - PINCTRL303 | HDMI Consumer Electronics Control IO |
| HDMI_HPDET | AE24 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL304 | HDMI Hot Plug Detect Input. Signals the connection / removal of an HDMI cable at the connector. |
| HDMI_EXTSWING | AN25 | A | - | - | HDMI Voltage Reference. When HDMI is used, this pin must be connected via an external 6.8K-Ω (±1% tolerance) resistor to $V_{SS}$. When the HDMI PHY is powered down, this pin should be left unconnected. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

### 4.2.7 Inter-Integrated Circuit (I2C) Signals

**Table 4-8. I2C Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **I2C0** | | | | | |
| I2C[0]_SCL | N32 | IO | PULL: DIS / DIS DRIVE: Z / Z DVDD_3P3 | - PINCTRL287 | I2C0 Clock IO |
| I2C[0]_SDA | N33 | IO | PULL: DIS / DIS DRIVE: Z / Z DVDD_3P3 | - PINCTRL288 | I2C0 Data IO |
| **I2C1** | | | | | |
| I2C[1]_SCL | N34 | IO | PULL: DIS / DIS DRIVE: Z / Z DVDD_3P3 | - PINCTRL289 | I2C1 Clock IO |
| I2C[1]_SDA | N35 | IO | PULL: DIS / DIS DRIVE: Z / Z DVDD_3P3 | - PINCTRL290 | I2C1 Data IO |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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### 4.2.8 Multichannel Audio Serial Port Signals

**Table 4-9. McASP0 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| MCA[0]_ACLKR | AK28 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL126 | McASP0 Receive Bit Clock IO |
| MCA[0]_AHCLKR | AJ27 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL127 | McASP0 Receive High-Frequency Master Clock IO |
| MCA[0]_AFSR | AG29 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL128 | McASP0 Receive Frame Sync IO |
| GP0[7]/<br>**MCA[0]_AMUTEIN** | H35 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | GP0<br>PINCTRL298 | McASP0 Mute Input |
| MCA[0]_ACLKX | AH30 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL129 | McASP0 Transmit Bit Clock IO |
| MCA[0]_AHCLKX | AH31 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL130 | McASP0 Transmit High-Frequency Master Clock IO |
| MCA[0]_AFSX | AJ31 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL131 | McASP0 Transmit Frame Sync IO |
| MCA[0]_AMUTE | AJ35 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL132 | McASP0 Mute Output |
| **MCA[0]_AXR[5]**/<br>MCB_DR | AJ37 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | MCB<br>PINCTRL138 | McASP0 Transmit/Receive Data IOs |
| **MCA[0]_AXR[4]**/<br>MCB_DX | AJ36 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | MCB<br>PINCTRL137 | |
| **MCA[0]_AXR[3]**/<br>MCB_FSR | AJ34 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | MCB<br>PINCTRL136 | |
| **MCA[0]_AXR[2]**/<br>MCB_FSX | AJ33 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | MCB<br>PINCTRL135 | |
| MCA[0]_AXR[1] | AJ32 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL134 | |
| MCA[0]_AXR[0] | AK37 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL133 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

**Table 4-10. McASP1 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| MCA[1]_ACLKR | AK36 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL139 | McASP1 Receive Bit Clock IO |
| MCA[1]_AHCLKR | AL37 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL140 | McASP1 Receive High-Frequency Master Clock IO |
| MCA[1]_AFSR | AK35 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL141 | McASP1 Receive Frame Sync IO |
| GP0[6]/<br>**MCA[1]_AMUTEIN**/<br>GPMC_A[23] | G5 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | GP0, GPMC<br>PINCTRL297 | McASP1 Mute Input |
| MCA[1]_ACLKX | AL36 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL142 | McASP1 Transmit Bit Clock IO |
| MCA[1]_AHCLKX | AM37 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL143 | McASP1 Transmit High-Frequency Master Clock IO |
| MCA[1]_AFSX | AK34 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL144 | McASP1 Transmit Frame Sync IO |
| MCA[1]_AMUTE | AK33 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL145 | McASP1 Mute Output |
| MCA[1]_AXR[1] | AK32 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL147 | McASP1 Transmit/Receive Data IOs |
| MCA[1]_AXR[0] | AL33 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL146 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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**Table 4-11. McASP2 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **MCA[2]_ACLKR**/ MCB_CLKR/ MCB_DR | AL34 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCB PINCTRL148 | McASP2 Receive Bit Clock IO |
| **MCA[2]_AHCLKR**/ MCB_CLKS | AM34 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCB PINCTRL149 | McASP2 Receive High-Frequency Master Clock IO |
| **MCA[2]_AFSR**/ MCB_CLKX/ MCB_FSR | AM35 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCB PINCTRL150 | McASP2 Receive Frame Sync IO |
| GP0[5]/ **MCA[2]_AMUTEIN**/ GPMC_A[24] | G2 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GP0, GPMC PINCTRL296 | McASP2 Mute Input |
| **MCA[2]_ACLKX**/ MCB_CLKX | AM36 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCB PINCTRL151 | McASP2 Transmit Bit Clock IO |
| **MCA[2]_AHCLKX**/ MCB_CLKR | AN36 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCB PINCTRL152 | McASP2 Transmit High-Frequency Master Clock IO |
| **MCA[2]_AFSX**/ MCB_CLKS/ MCB_FSX | AN35 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCB PINCTRL153 | McASP2 Transmit Frame Sync IO |
| MCA[2]_AMUTE | AP36 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL154 | McASP2 Mute Output |
| **MCA[2]_AXR[1]**/ MCB_DX | AR37 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCB PINCTRL156 | McASP2 Transmit/Receive Data IOs |
| MCA[2]_AXR[0] | AR36 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL155 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

### 4.2.9 Multichannel Buffered Serial Port Signals

**Table 4-12. McBSP Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| MCA[2]_ACLKR/ **MCB_CLKR**/ MCB_DR | AL34 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2], MCB PINCTRL148 | McBSP Receive Clock IO |
| MCA[2]_AHCLKX/ **MCB_CLKR** | AN36 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2] PINCTRL152 | |
| MCA[0]_AXR[3]/ **MCB_FSR** | AJ34 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[0] PINCTRL136 | McBSP Receive Frame Sync IO |
| MCA[2]_AFSR/ MCB_CLKX/ **MCB_FSR** | AM35 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2], MCB PINCTRL150 | |
| MCA[0]_AXR[5]/ **MCB_DR** | AJ37 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[0] PINCTRL138 | McBSP Receive Data Input |
| MCA[2]_ACLKR/ MCB_CLKR/ **MCB_DR** | AL34 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2], MCB PINCTRL148 | |
| MCA[2]_AFSR/ **MCB_CLKX**/ MCB_FSR | AM35 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2], MCB PINCTRL150 | McBSP Transmit Clock IO |
| MCA[2]_ACLKX/ **MCB_CLKX** | AM36 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2] PINCTRL151 | |
| MCA[0]_AXR[2]/ **MCB_FSX** | AJ33 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[0] PINCTRL135 | McBSP Transmit Frame Sync IO |
| MCA[2]_AFSX/ MCB_CLKS/ **MCB_FSX** | AN35 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2], MCB PINCTRL153 | |
| MCA[0]_AXR[4]/ **MCB_DX** | AJ36 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[0] PINCTRL137 | McBSP Transmit Data Output |
| MCA[2]_AXR[1]/ **MCB_DX** | AR37 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2] PINCTRL156 | |
| MCA[2]_AHCLKR/ **MCB_CLKS** | AM34 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2] PINCTRL149 | McBSP Source Clock Input |
| MCA[2]_AFSX/ **MCB_CLKS**/ MCB_FSX | AN35 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | MCA[2], MCB PINCTRL153 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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### 4.2.10 Oscillator/Phase-Locked Loop (PLL) Signals

**Table 4-13. Oscillator/PLL and Clock Generator Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **CLOCK GENERATOR** | | | | | |
| CLKOUT | F1 | O | PULL: IPU / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL320 | Device Clock output. Can be used as a system clock for other devices |
| **OSCILLATOR/PLL** | | | | | |
| DEV_MXI/<br>DEV_CLKIN | A19 | I | DIS<br>DEV_DVDD18 | - | Device Crystal input. Crystal connection to internal oscillator for system clock. Functions as CLKINDEV clock input when an ***external*** oscillator is used. |
| DEV_MXO | C19 | O | DIS<br>DEV_DVDD18 | - | Device Crystal output. Crystal connection to internal oscillator for system clock. When device oscillator is BYPASSED, leave this pin unconnected. |
| DEVOSC_DVDD18 | E19 | S | - | - | 1.8 V Power Supply for Device (DEV) Oscillator. If the internal oscillator is bypassed, DEVOSC_DVDD18 should still be connected to the 1.8-V power supply. |
| DEVOSC_VSS | B19 | GND | - | - | Supply Ground for DEV Oscillator. If the internal oscillator is bypassed, DEVOSC_VSS should be connected to ground (VSS). |
| CLKIN32 | H37 | I | PULL: IPU / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL321 | RTC Clock input. Optional 32.768 kHz clock for RTC reference. If this pin is not used, it should be held low. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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### 4.2.11 Peripheral Component Interconnect Express (PCIe) Signals

**Table 4-14. PCIe Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) | DESCRIPTION |
|---|---|---|---|---|
| PCIE_TXP0 | AB31 | O | VDDR_PCIE | PCIE Transmit Data Lane 0. When the PCIe SERDES are powered down, or if this lane is not used, these pins should be left unconnected. |
| PCIE_TXN0 | AB30 | O | | |
| PCIE_RXP0 | Y29 | I | VDDR_PCIE | PCIE Receive Data Lane 0. When the PCIe SERDES are powered down, or if this lane is not used, these pins should be left unconnected. |
| PCIE_RXN0 | V29 | I | | |
| PCIE_TXP1 | Y27 | O | VDDR_PCIE | PCIE Transmit Data Lane 1. When the PCIe SERDES are powered down, or if this lane is not used, these pins should be left unconnected. |
| PCIE_TXN1 | AB28 | O | | |
| PCIE_RXP1 | V31 | I | VDDR_PCIE | PCIE Receive Data Lane 1. When the PCIe SERDES are powered down, or if this lane is not used, these pins should be left unconnected. |
| PCIE_RXN1 | V30 | I | | |
| SERDES_CLKP | AB34 | I | VDD_LJCB | PCIE Serdes Reference Clock Inputs. Shared between PCI Express and Serial ATA. When neither PCI Express nor Serial ATA are used, these pins should be left unconnected. |
| SERDES_CLKN | AB33 | I | VDD_LJCB | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating IO supply voltage for each signal.


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### 4.2.12 Reset, Interrupts, and JTAG Interface Signals

**Table 4-15. RESET, Interrupts, and JTAG Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **RESET** | | | | | |
| $\overline{\text{RESET}}$ | G33 | I | PULL: IPD / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL316 | Device Reset input |
| $\overline{\text{POR}}$ | F37 | I | IPU<br>DVDD_3P3 | - | Power-On Reset input |
| $\overline{\text{RSTOUT}}$ | G37 | O | PULL: DIS / DIS<br>DVDD_3P3 | -<br>PINCTRL318 | Reset output<br>For more detailed information on $\overline{\text{RSTOUT}}$ pin behavior, see Section 8.2.13 |
| **INTERRUPTS** | | | | | |
| $\overline{\text{NMI}}$ | G36 | I | PULL: IPD / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL317 | External active low maskable interrupt |
| GP0[31:3] | see Table 4-5 | IO | see **NOTE** | - | Interrupt-capable general-purpose IOs<br>**NOTE:** All pins are multiplexed with other pin functions. For muxing and internal pullup, pulldown, or disable details, see Table 4-5, *GPIO Terminal Functions*. |
| GP1[31:0] | see Table 4-5 | IO | see **NOTE** | - | Interrupt-capable general-purpose IOs<br>**NOTE:** All pins are multiplexed with other pin functions. For muxing and internal pullup, pulldown, or disable details, see Table 4-5, *GPIO Terminal Functions*. |
| **JTAG** | | | | | |
| TCLK | J37 | I | PULL: IPU / IPU<br>DRIVE: H / H<br>DVDD_3P3 | -<br>PINCTRL305 | JTAG test clock input |
| RTCK | J36 | O | PULL: IPD / DIS<br>DRIVE: L / H<br>DVDD_3P3 | -<br>PINCTRL306 | JTAG return clock output |
| TDI | J34 | I | PULL: IPU / IPU<br>DRIVE: H / H<br>DVDD_3P3 | -<br>PINCTRL307 | JTAG test data input |
| TDO | N30 | O | PULL: IPD / DIS<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL308 | JTAG test port data output |
| TMS | N31 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL309 | JTAG test port mode select input. For proper operation, ***do not*** oppose the IPU on this pin. |
| $\overline{\text{TRST}}$ | K36 | I | PULL: IPD / IPD<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL310 | JTAG test port reset input |
| EMU4 | M37 | IO | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL315 | Emulator pin 4 |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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**Table 4-15. RESET, Interrupts, and JTAG Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMU3 | M36 | IO | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL314 | Emulator pin 3 |
| EMU2 | L37 | IO | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL313 | Emulator pin 2 |
| EMU1 | L36 | IO | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL312 | Emulator pin 1 |
| EMU0 | J35 | IO | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL311 | Emulator pin 0 |


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### 4.2.13 Secure Digital/Secure Digital Input Output (SD/SDIO) Signals

**Table 4-16. SD/SDIO Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **SD_CLK**/ GPMC_A[13]/ GP1[1] | U2 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | GPMC, GP1 PINCTRL158 | SD Clock output |
| **SD_CMD**/ GPMC_A[21]/ GP1_[2] | U3 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | GPMC, GP1 PINCTRL159 | SD Command output |
| **SD_DAT[0]**/ GPMC_A[20]/ GP1[3] | U1 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GPMC, GP1 PINCTRL160 | SD Data0 IO. Functions as data bit 0 for 4-bit SD mode and single data bit for 1-bit SD mode. |
| **SD_DAT[1]_SDIRQ**/ GPMC_A[19]/ GP1[4] | T1 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GMPC, GP1 PINCTRL161 | SD Data1 IO. Functions as data bit 1 for 4-bit SD mode and as an IRQ input for 1-bit SD mode |
| **SD_DAT[2]_SDRW**/ GPMC_A[18]/ GP1[5] | T2 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GPMC, GP1 PINCTRL162 | SD Data2 IO. Functions as data bit 2 for 4-bit SD mode and as a Read Wait input for 1-bit SD mode. |
| **SD_DAT[3]**/ GPMC_A[17]/ GP1[6] | T13 | IO | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GPMC, GP1 PINCTRL163 | SD Data3 IO. Functions as data bit 3 for 4-bit SD mode. |
| **SD_POW**/ GPMC_A[14]/ GP1[0] | U4 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | GPMC, GP1 PINCTRL157 | SD Card Power Enable output |
| **SD_SDCD**/ GPMC_A[16]/ GP1[7] | R13 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GPMC, GP1 PINCTRL164 | SD Card Detect input |
| **SD_SDWP**/ GPMC_A[15]/ GP1[8] | R5 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GMC, GP1 PINCTRL165 | SD Card Write Protect input |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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### 4.2.14 Serial ATA Signals

**NOTE**

Serial ATA pins J32 and J33 have a different naming convention and functionality for silicon revision 1.x devices and silicon revision 2.x devices. These pins are listed separately in Table 4-18.

**Table 4-17. Serial ATA Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SATA_TXN0 | T31 | O | - VDDR_SATA | - | Serial ATA Data Transmit for disk 0. When the SATA SERDES are powered down, these pins should be left unconnected. |
| SATA_TXP0 | T32 | O | - VDDR_SATA | - | |
| SATA_TXN1 | U33 | O | - VDDR_SATA | - | Serial ATA Data Transmit for disk 1. When the SATA SERDES are powered down, these pins should be left unconnected. |
| SATA_TXP1 | V33 | O | - VDDR_SATA | - | |
| SATA_RXN0 | V37 | I | - VDDR_SATA | - | Serial ATA Data Receive for disk 0. When the SATA SERDES are powered down, these pins should be left unconnected. |
| SATA_RXP0 | V36 | I | - VDDR_SATA | - | |
| SATA_RXN1 | V35 | I | - VDDR_SATA | - | Serial ATA Data Receive for disk 1. When the SATA SERDES are powered down, these pins should be left unconnected. |
| SATA_RXP1 | W35 | I | - VDDR_SATA | - | |
| SERDES_CLKP | AB34 | I | - VDD_LJCB | - | PCIE Serdes Reference Clock Input. Shared between PCI Express and Serial ATA. |
| SERDES_CLKN | AB33 | I | - VDD_LJCB | - | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

**Table 4-18. Serial ATA [Pins J32, J33] Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Silicon Revision 1.x** | | | | | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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**Table 4-18. Serial ATA [Pins J32, J33] Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| GP1[30]/ **SATA_ACT0_LED** | J32 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GP1 PINCTRL299 | Serial ATA disk 0 Activity LED output |
| GP1[31]/ **SATA_ACT1_LED** | J33 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GP1 PINCTRL300 | Serial ATA disk 1 Activity LED output |
| **Silicon Revision 2.x** | | | | | |
| GP1[30]/ **SATA_ACT1_LED** | J32 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GP1 PINCTRL299 | Serial ATA disk 1 Activity LED output |
| GP1[31]/ **SATA_ACT0_LED** | J33 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GP1 PINCTRL300 | Serial ATA disk 0 Activity LED output |

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### 4.2.15 Serial Peripheral Digital Interconnect Format (SPI) Signals

**Table 4-19. SPI Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SPI_SCLK | R2 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL166 | SPI Clock IO |
| **$\overline{\text{SPI_SCS[3]}}$** /<br>GPMC_A[21]/<br>GP1[22] | P1 | IO | PULL: DIS / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | GPMC, GP1<br>PINCTRL170 | SPI Chip Select IO |
| **$\overline{\text{SPI_SCS[2]}}$** /<br>GPMC_A[22] | P3 | IO | PULL: DIS / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | GPMC<br>PINCTRL169 | |
| **$\overline{\text{SPI_SCS[1]}}$** /<br>GPMC_A[23] | P2 | IO | PULL: DIS / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | GPMC<br>PINCTRL168 | |
| $\overline{\text{SPI_SCS[0]}}$ | R1 | IO | PULL: DIS / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL167 | |
| SPI_D[1] | P13 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL172 | SPI Data IO. Can be configured as either MISO or MOSI |
| SPI_D[0] | N11 | IO | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL171 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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### 4.2.16 Timer Signals

**Table 4-20. Timer Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **General-Purpose Timers7-1 and Watchdog Timer** | | | | | |
| GP0[3]/ **TCLKIN** | J31 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GP0 PINCTRL294 | Timer external clock input |
| **Timer7** | | | | | |
| **TIM7_OUT**/ GPMC_A[12]/ GP0[31] | G1 | IO | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | GPMC, GP0 PINCTRL206 | Timer7 capture event input or PWM output |
| **Timer6** | | | | | |
| **TIM6_OUT**/ GPMC_A[24]/ GP0[30] | H1 | IO | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | GPMC, GP0 PINCTRL205 | Timer6 capture event input or PWM output |
| **Timer5** | | | | | |
| **TIM5_OUT**/ GP0[29] | H34 | IO | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | GP0 PINCTRL204 | Timer5 capture event input or PWM output |
| **Timer4** | | | | | |
| **TIM4_OUT**/ GP0[28] | H33 | IO | PULL: IPD / IPD DRIVE: L / L DVDD_3P3 | GP0 PINCTRL203 | Timer4 capture event input or PWM output |
| **Timer3-1** | | | | | |
| There are no external pins on these timers for this device. | | | | | |
| **Watchdog Timer** | | | | | |
| WD_OUT | H36 | O | PULL: IPU / IPU DRIVE: H / L DVDD_3P3 | - PINCTRL319 | Watchdog timer event output |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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### 4.2.17 Universal Asynchronous Receiver/Transmitter (UART) Signals

**Table 4-21. UART0 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| UART0_RXD | N10 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL173 | UART0 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| UART0_TXD | N8 | O | PULL: IPD / DIS<br>DRIVE: L / H<br>DVDD_3P3 | -<br>PINCTRL174 | UART0 Transmit Data Output. Functions as transmit output in CIR and IrDA modes. |
| **$\overline{\text{UART0_RTS}}$** /<br>GP1[27] | N9 | O | PULL: IPU / DIS<br>DRIVE: H / H<br>DVDD_3P3 | GP1<br>PINCTRL175 | UART0 Request to Send Output. Indicates module is ready to receive data. Functions as SD output in IrDA mode. |
| **$\overline{\text{UART0_CTS}}$** /<br>GP1[28] | N7 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | GP1<br>PINCTRL176 | UART0 Clear to Send Input. Has no function in IrDA and CIR modes. |
| **$\overline{\text{UART0_DTR}}$** /<br>GPMC_A[20]/<br>GPMC_A[12]/<br>GP1[16] | N6 | O | PULL: IPU / DIS<br>DRIVE: H / H<br>DVDD_3P3 | GPMC, GP1<br>PINCTRL177 | UART0 Data Terminal Ready Output |
| **$\overline{\text{UART0_DSR}}$** /<br>GPMC_A[19]/<br>GPMC_A[24]/<br>GP1[17] | N4 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | GPMC, GP1<br>PINCTRL178 | UART0 Data Set Ready Input |
| **$\overline{\text{UART0_DCD}}$** /<br>GPMC_A[18]/<br>GPMC_A[23]/<br>GP1[18] | N5 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | GPMC, GP1<br>PINCTRL179 | UART0 Data Carrier Detect Input |
| **UART0_RIN**/<br>GPMC_A[17]/<br>GPMC_A[22]/<br>GP1[19] | N3 | I | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | GPMC, GP1<br>PINCTRL180 | UART0 Ring Indicator Input |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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**Table 4-22. UART1 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **UART1_RXD**/ GPMC_A[26]/ GPMC_A[20] | N1 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | GPMC PINCTRL181 | UART1 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| **UART1_TXD**/ GPMC_A[25]/ GPMC_A[19] | N2 | O | PULL: IPD / DIS DRIVE: L / H DVDD_3P3 | GPMC PINCTRL182 | UART1 Transmit Data Output. Functions as transmit output in CIR and IrDA modes. |
| **$\overline{\text{UART1_RTS}}$** / GPMC_A[14]/ GPMC_A[18]/ GP1[25] | M2 | O | PULL: IPU / DIS DRIVE: H / H DVDD_3P3 | GPMC, GP1 PINCTRL183 | UART1 Request to Send Output. Indicates module is ready to receive data. Functions as SD output in IrDA mode. |
| **$\overline{\text{UART1_CTS}}$** / GPMC_A[13]/ GPMC_A[17]/ GP1[26] | L3 | IO | PULL: IPU / IPU DRIVE: Z / Z DVDD_3P3 | GPMC, GP1 PINCTRL184 | UART1 Clear to Send Input. Has no function in IrDA and CIR modes. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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**Table 4-23. UART2 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| UART2_RXD | M1 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL185 | UART2 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| UART2_TXD | L2 | O | PULL: IPD / IPD<br>DRIVE: L / H<br>DVDD_3P3 | -<br>PINCTRL186 | UART2 Transmit Data Output. Functions as transmit output in CIR and IrDA modes. |
| **$\overline{\text{UART2_RTS}}$** /<br>GPMC_A[15]/<br>GPMC_A[26]/<br>GP1[23] | L9 | O | PULL: IPU / DIS<br>DRIVE: H / H<br>DVDD_3P3 | GPMC, GP1<br>PINCTRL187 | UART2 Request to Send Output. Indicates module is ready to receive data. Functions as SD output in IrDA mode. |
| **$\overline{\text{UART2_CTS}}$** /<br>GPMC_A[16]/<br>GPMC_A[25]/<br>GP1[24] | K7 | IO | PULL: IPU / IPU<br>DRIVE: Z / Z<br>DVDD_3P3 | GPMC, GP1<br>PINCTRL188 | UART2 Clear to Send Input. Has no function in IrDA and CIR modes. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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### 4.2.18 Universal Serial Bus (USB) Signals

**Table 4-24. USB Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **USB0** | | | | | |
| USB0_DP | P37 | A IO | - | - | USB0 bidirectional Data Differential signal pair [positive/negative].<br>When the USB0 PHY is powered down, these pins should be left unconnected. |
| USB0_DN | P36 | A IO | - | - | |
| USB0_R1 | N37 | A O | - | - | USB0 current reference output. When the USB0 peripheral is used, this pin must be connected via a 44.2-Ω ±1% resistor to VSS.<br>When the USB0 PHY is powered down, this pin should be left unconnected. |
| USB0_DRVVBUS | P35 | O | PULL: IPD / IPD<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL322 | When this pin is used as USB0_DRVVBUS and the USB0 Controller is operating as a Host, this signal is used by the USB0 Controller to enable the external VBUS charge pump.<br>When the USB0 PHY is powered down, this pin should be left unconnected. |
| VDD_USB0_VBUS | N36 | I | - | - | USB0 VBUS input (5 V).<br>The voltage level on this pin is sampled to determine session status.<br>When the USB0 PHY is powered down, this pin should be left unconnected. |
| **USB1** | | | | | |
| USB1_DP | R37 | A IO | - | - | USB1 bidirectional Data Differential signal pair [positive/negative].<br>When the USB1 PHY is powered down, these pins should be left unconnected. |
| USB1_DN | R36 | A IO | - | - | |
| USB1_R1 | T37 | A O | - | - | USB1 current reference output. When the USB1 peripheral is used, this pin must be connected via a 44.2-Ω ±1% resistor to VSS.<br>When the USB1 PHY is powered down, this pin should be left unconnected. |
| USB1_DRVVBUS | R35 | O | PULL: IPD / IPD<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL323 | When this pin is used as USB1_DRVVBUS and the USB1 Controller is operating as a Host, this signal is used by the USB1 Controller to enable the external VBUS charge pump.<br>When the USB1 PHY is powered down, this pin should be left unconnected. |
| VDD_USB1_VBUS | T36 | I | - | - | USB1 VBUS input (5 V).<br>The voltage level on this pin is sampled to determine session status.<br>When the USB1 PHY is powered down, this pin should be left unconnected. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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### 4.2.19 Video Input Signals

**Table 4-25. Video Input 0 Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_CLK | AR14 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL83 | Video Input 0 Port A Clock input. Input clock for 8-bit, 16-bit, or 24-bit Port A video capture. |
| VIN[0]B_CLK | AR19 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL84 | Video Input 0 Port B Clock input. Input clock for 8-bit Port B video capture. This signal is not used in 16-bit and 24-bit capture modes. |
| **VIN[0]A_D[23]**/<br>VIN[0]B_HSYNC | AT2 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[0]B<br>PINCTRL15 | Video Input 0 Port A Data inputs. For 16-bit capture, D[7:0] are Cb/Cr and [15:8] are Y Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs and D[15:8] are Port B YCbCr data inputs. For RGB capture, D[23:16] are R, D[15:8] are G, and D[7:0] are B data inputs. |
| **VIN[0]A_D[22]**/<br>VIN[0]B_VSYNC | AR2 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[0]B<br>PINCTRL14 | |
| **VIN[0]A_D[21]**/<br>VIN[0]B_FLD | AU4 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[0]B<br>PINCTRL13 | |
| **VIN[0]A_D[20]**/<br>VIN[0]B_DE | AN3 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[0]B<br>PINCTRL12 | |
| **VIN[0]A_D[19]**/<br>VIN[1]A_DE[0]/<br>VOUT[1]_C[9] | AK4 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[1]A,<br>VOUT[1]<br>PINCTRL25 | |
| **VIN[0]A_D[18]**/<br>VIN[1]A_FLD/<br>VOUT[1]_C[8] | AK5 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[1]A,<br>VOUT[1]<br>PINCTRL24 | |
| **VIN[0]A_D[17]**/<br>VIN[1]A_VSYNC/<br>VOUT[1]_VSYNC<br>(silicon revision 1.x)<br>DAC_VOUT[1]_VSYNC<br>(silicon revision 2.x) | AL5 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[1]A,<br>VOUT[1]<br>PINCTRL23 | |
| **VIN[0]A_D[16]**/<br>VIN[1]A_HSYNC/<br>VOUT[1]_FLD | AT5 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[1]A,<br>VOUT[1]<br>PINCTRL22 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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**Table 4-25. Video Input 0 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_D[15] | AU14 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL100 | Video Input 0 Port A Data inputs. For 16-bit capture, D[7:0] are Cb/Cr and [15:8] are Y Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs and D[15:8] are Port B YCbCr data inputs. For RGB capture, D[23:16] are R, D[15:8] are G, and D[7:0] are B data inputs. |
| VIN[0]A_D[14] | AU15 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL99 | |
| VIN[0]A_D[13] | AT15 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL98 | |
| VIN[0]A_D[12] | AU16 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL97 | |
| VIN[0]A_D[11] | AU17 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL96 | |
| VIN[0]A_D[10] | AT16 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL95 | |
| VIN[0]A_D[9] | AE16 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL94 | |
| VIN[0]A_D[8] | AP17 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL93 | |
| VIN[0]A_D[7] | AR17 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL92 | |
| VIN[0]A_D[6] | AP18 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL91 | |
| VIN[0]A_D[5] | AT17 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL90 | |
| VIN[0]A_D[4] | AT18 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL89 | |
| VIN[0]A_D[3] | AR18 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL88 | |
| VIN[0]A_D[2] | AH18 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL87 | |
| VIN[0]A_D[1] | AU18 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL86 | |
| VIN[0]A_D[0] | AJ19 | I | IPD<br>DVDD_3P3 | -<br>PINCTRL85 | |
| VIN[0]A_D[23]/<br>**VIN[0]B_HSYNC** | AT2 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VIN[0]A<br>PINCTRL15 | Video Input 0 Port B Horizontal Sync input. Discrete horizontal synchronization signal for Port B 8-bit YCbCr capture without embedded syncs ("BT.601" modes). Not used in RGB or 16-bit YCbCr capture modes |
| **VIN[0]A_HSYNC** | AU5 | I | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL32 | Video Input 0 Port A Horizontal Sync input. Discrete horizontal synchronization signal for Port A RGB capture mode or YCbCr capture without embedded syncs ("BT.601" modes). |

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**Table 4-25. Video Input 0 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_D[22]/ **VIN[0]B_VSYNC** | AR2 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A PINCTRL14 | Video Input 0 Port B Vertical Sync input. Discrete vertical synchronization signal for Port B 8-bit YCbCr capture without embedded syncs ("BT.601" modes). Not used in RGB or 16-bit YCbCr capture modes. |
| **VIN[0]A_VSYNC** | AM4 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL33 | Video Input 0 Port A Vertical Sync input. Discrete vertical synchronization signal for Port A RGB capture mode or YCbCr capture without embedded syncs ("BT.601" modes). |
| VIN[0]A_D[21]/ **VIN[0]B_FLD** | AU4 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A PINCTRL13 | Video Input 0 Port B Field ID input. Discrete field identification signal for Port B 8-bit YCbCr capture without embedded syncs ("BT.601" modes). Not used in RGB or 16-bit YCbCr capture modes |
| **VIN[0]A_FLD** | AL4 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL34 | Video Input 0 Port A Field ID input. Discrete field identification signal for Port A RGB capture mode or YCbCr capture without embedded syncs ("BT.601" modes). |
| VIN[0]A_D[20]/ **VIN[0]B_DE** | AN3 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A PINCTRL12 | Video Input 0 Port B Data Enable input. Discrete data valid signal for Port B RGB capture mode or YCbCr capture without embedded syncs ("BT.601" modes). |
| **VIN[0]A_DE** | AT3 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL35 | Video Input 0 Port A Data Enable input. Discrete data valid signal for Port A RGB capture mode or YCbCr capture without embedded syncs ("BT.601" modes). |


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**Table 4-26. Video Input 1 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_CLK/ **VIN[1]A_CLK** | AT7 | I | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL46 | Video Input 1 Port A Clock input. Input clock for 8-bit or 16-bit Port A video capture. Input data is sampled on the CLK0 edge. |
| VOUT[1]_AVID/ **VIN[1]B_CLK** | AT4 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL31 | Video Input 1 Port B Clock input. Input clock for 8-bit Port B video capture. Input data is sampled on the CLK1 edge. This signal is not used in 16-bit capture modes. |
| VOUT[1]_HSYNC (silicon revision 1.x) DAC_VOUT[1]_HSYNC (silicon revision 2.x)/ **VIN[1]A_D[15]** | AR5 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL21 | Video Input 1 Port A Data inputs. For 16-bit capture, D[7:0] are Cb/Cr and [15:8] are Y Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs and D[15:8] are Port B YCbCr data inputs. For VIN[1], only D[15:0] are available. |
| **VIN[1]A_D[14]** | AM3 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL11 | |
| VOUT[1]_C[7]/ **VIN[1]A_D[13]** | AD13 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL10 | |
| VOUT[1]_C[6] **VIN[1]A_D[12]** | AN8 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL9 | |
| VOUT[1]_C[5]/ **VIN[1]A_D[11]** | AP8 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL8 | |
| VOUT[1]_C[4]/ **VIN[1]A_D[10]** | AN7 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL7 | |
| VOUT[1]_C[3]/ **VIN[1]A_D[9]** | AM8 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL6 | |
| VOUT[1]_C[2]/ **VIN[1]A_D[8]** | AK6 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL20 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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**Table 4-26. Video Input 1 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_Y_YC[9]/ **VIN[1]A_D[7]** | AP6 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL19 | Video Input 1 Port A Data inputs. For 16-bit capture, D[7:0] are Cb/Cr and [15:8] are Y Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs and D[15:8] are Port B YCbCr data inputs. For VIN[1], only D[15:0] are available. |
| VOUT[1]_Y_YC[8]/ **VIN[1]A_D[6]** | AT6 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL18 | |
| VOUT[1]_Y_YC[7]/ **VIN[1]A_D[5]** | AR6 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL17 | |
| VOUT[1]_Y_YC[6]/ **VIN[1]A_D[4]** | AC13 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL16 | |
| VOUT[1]_Y_YC[5]/ **VIN[1]A_D[3]** | AJ7 | I | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL50 | |
| VOUT[1]_Y_YC[4]/ **VIN[1]A_D[2]** | AU6 | I | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL49 | |
| VOUT[1]_Y_YC[3]/ **VIN[1]A_D[1]** | AP7 | I | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL48 | |
| VOUT[1]_Y_YC[2]/ **VIN[1]A_D[0]** | AU7 | I | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL47 | |
| VOUT[0]_B_CB_C[0]/ VOUT[1]_C[9]/ **VIN[1]B_HSYNC_DE** | AR9 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL27 | Video Input 1 Port B Horizontal Sync or Data Valid signal input. Discrete horizontal synchronization signal for Port B 8-bit YCbCr capture without embedded syncs ("BT.601" modes). Not used in 16-bit YCbCr capture mode. |
| VIN[0]A_D[16]/ **VIN[1]A_HSYNC/** VOUT[1]_FLD | AT5 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VOUT[1] PINCTRL22 | Video Input 1 Port A Horizontal Sync input. Discrete horizontal synchronization signal for Port A YCbCr capture modes without embedded syncs ("BT.601" modes). |
| VOUT[0]_G_Y_YC[0]/ VOUT[1]_VSYNC (silicon revision 1.x) DAC_VOUT[1]_VSYNC (silicon revision 2.x)/ **VIN[1]B_VSYNC** | AP9 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL29 | Video Input 1 Port B Vertical Sync input. Discrete vertical synchronization signal for Port B 8-bit YCbCr capture without embedded syncs ("BT.601" modes). Not used in 16-bit YCbCr capture mode. |
| VIN[0]A_D[17]/ **VIN[1]A_VSYNC/** VOUT[1]_VSYNC (silicon revision 1.x) DAC_VOUT[1]_VSYNC (silicon revision 2.x) | AL5 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VOUT[1] PINCTRL23 | Video Input 1 Port A Vertical Sync input. Discrete vertical synchronization signal for Port A YCbCr capture modes without embedded syncs ("BT.601" modes). |
| VIN[0]A_D[19]/ **VIN[1]A_DE/** VOUT[1]_C[9] | AK4 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VOUT[1] PINCTRL25 | Video Input 1 Port A Data Enable input. Discrete data valid signal for Port A YCbCr capture modes without embedded syncs ("BT.601" modes). |
| VIN[0]A_D[18]/ **VIN[1]A_FLD/** VOUT[1]_C[8] | AK5 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VOUT[1] PINCTRL24 | Video Input 1Port A Field ID input. Discrete field identification signal for Port A YCbCr capture modes without embedded syncs ("BT.601" modes). |
| VOUT[0]_G_Y_YC[1]/ VOUT[1]_FLD/ **VIN[1]B_FLD** | AU8 | I | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL30 | Video Input 1 Port B Field ID input. Discrete field identification signal for Port B 8-bit YCbCr capture without embedded syncs ("BT.601" modes). Not used in 16-bit YCbCr capture mode. |


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### 4.2.20 Digital Video Output Signals

**NOTE**

Video output 0 pins AR8 and AL9 and video output 1 pins AT9, AR5, AP9, and AL5 have a different naming convention and functionality for silicon revision 1.x devices and silicon revision 2.x devices. These pins are listed separately in Table 4-28 and Table 4-30.

**Table 4-27. Video Output 0 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_CLK | AT14 | O | PULL: IPD / DIS<br>DRIVE: L / H<br>DVDD_3P3 | -<br>PINCTRL101 | Video Output 0 Clock output. |
| VOUT[0]_G_Y_YC[9] | AR13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL109 | Video Output 0 Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. |
| VOUT[0]_G_Y_YC[8] | AU13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL108 | |
| VOUT[0]_G_Y_YC[7] | AT13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL107 | |
| VOUT[0]_G_Y_YC[6] | AE14 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL106 | |
| VOUT[0]_G_Y_YC[5] | AM14 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL105 | |
| VOUT[0]_G_Y_YC[4] | AL14 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL104 | |
| VOUT[0]_G_Y_YC[3] | AP14 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL103 | |
| VOUT[0]_G_Y_YC[2] | AE15 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL102 | |
| **VOUT[0]_G_Y_YC[1]**/<br>VOUT[1]_FLD/<br>VIN[1]B_FLD | AU8 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VOUT,[1]<br>VIN[1]B<br>PINCTRL30 | Video Output 0 Data. These signals represent the 2 LSBs of G/Y/YC video data for 10-bit, 20-bit and 30-bit video modes (VOUT0 only). For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. These signals are not used in 8/16/24-bit modes |
| **VOUT[0]_G_Y_YC[0]**/<br>VOUT[1]_VSYNC<br>(silicon revision 1.x)<br>DAC_VOUT[1]_VSYNC<br>(silicon revision 2.x)/<br>VIN[1]B_VSYNC | AP9 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VOUT[1],<br>VIN[1]B<br>PINCTRL29 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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**Table 4-27. Video Output 0 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_B_CB_C[9] | AT12 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL117 | Video Output 0 Data. These signals represent the 8 MSBs of B/CB/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused |
| VOUT[0]_B_CB_C[8] | AH13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL116 | |
| VOUT[0]_B_CB_C[7] | AM13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL115 | |
| VOUT[0]_B_CB_C[6] | AJ13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL114 | |
| VOUT[0]_B_CB_C[5] | AK13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL113 | |
| VOUT[0]_B_CB_C[4] | AN13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL112 | |
| VOUT[0]_B_CB_C[3] | AL13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL111 | |
| VOUT[0]_B_CB_C[2] | AP13 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | -<br>PINCTRL110 | |
| **VOUT[0]_B_CB_C[1]**/<br>VOUT[1]_HSYNC<br>(silicon revision 1.x)<br>DAC_VOUT[1]_HSYNC<br>(silicon revision 2.x)/<br>VOUT[1]_AVID | AT9 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VOUT[1]<br>PINCTRL28 | Video Output 0 Data. These signals represent the 2 LSBs of B/CB/C video data for 20-bit and 30-bit video modes (VOUT[0] only). For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused. These signals are not used in 16/24-bit modes. |
| VOUT[0]_R_CR[9]/<br>**VOUT[0]_B_CB_C[1]**/<br>VOUT[1]_Y_YC[9] | AU9 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | VOUT[0],<br>VOUT[1]<br>PINCTRL125 | |
| **VOUT[0]_B_CB_C[0]**/<br>VOUT[1]_C[9]/<br>VIN[1]B_HSYNC_DE | AR9 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | VOUT[1],<br>VIN[1]B<br>PINCTRL27 | |
| VOUT[0]_R_CR[8]/<br>**VOUT[0]_B_CB_C[0]**/<br>VOUT[1]_Y_YC[8] | AK10 | O | PULL: IPD / DIS<br>DRIVE: L / L<br>DVDD_3P3 | VOUT[0],<br>VOUT[1]<br>PINCTRL124 | |


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**Table 4-27. Video Output 0 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **VOUT[0]_R_CR[9]**/ VOUT[0]_B_CB_C[1]/ VOUT[1]_Y_YC[9] | AU9 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL125 | Video Output 0 Data. These signals represent the 8 MSBs of R/CR video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused. |
| **VOUT[0]_R_CR[8]**/ VOUT[0]_B_CB_C[0]/ VOUT[1]_Y_YC[8] | AK10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL124 | |
| **VOUT[0]_R_CR[7]**/ VOUT[0]_G_Y_YC[1]/ VOUT[1]_Y_YC[7] | AL10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL123 | |
| **VOUT[0]_R_CR[6]**/ VOUT[0]_G_Y_YC[0]/ VOUT[1]_Y_YC[6] | AU10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL122 | |
| **VOUT[0]_R_CR[5]**/ VOUT[0]_AVID/ VOUT[1]_Y_YC[5] | AT10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL121 | |
| **VOUT[0]_R_CR[4]**/ VOUT[0]_FLD/ VOUT[1]_Y_YC[4] | AG13 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL120 | |
| **VOUT[0]_R_CR[3]**/ VOUT[0]_VSYNC/ VOUT[1]_Y_YC[3] | AR11 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL119 | |
| **VOUT[0]_R_CR[2]**/ VOUT[0]_HSYNC/ VOUT[1]_Y_YC[2] | AT11 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL118 | |
| **VOUT[0]_R_CR[1]** | AT8 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL40 | Video Output 0 Data. These signals represent the 2 LSBs of R/CR video data for 30-bit video modes (VOUT[0] only). For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused. These signals are not used in 24-bit mode. |
| **VOUT[0]_R_CR[0]/** VOUT[1]_C[8]/ VOUT[1]_CLK | AJ11 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[1] PINCTRL26 | |
| **VOUT[0]_VSYNC** | AN9 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL37 | Video Output 0 Vertical Sync output. This is the discrete vertical synchronization output. This signal is not used for embedded sync modes. |
| VOUT[0]_R_CR[3]/ **VOUT[0]_VSYNC**/ VOUT[1]_Y_YC[3] | AR11 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL119 | |
| **VOUT[0]_HSYNC** | AM9 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | - PINCTRL36 | Video Output 0 Horizontal Sync output. This is the discrete horizontal synchronization output. This signal is not used for embedded sync modes. |
| VOUT[0]_R_CR[2]/ **VOUT[0]_HSYNC**/ VOUT[1]_Y_YC[2] | AT11 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL118 | |
| VOUT[0]_R_CR[4]/ **VOUT[0]_FLD**/ VOUT[1]_Y_YC[4] | AG13 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL120 | Video Output 0 Field ID output. This is the discrete field identification output. This signal is not used for embedded sync modes. |
| VOUT[0]_R_CR[5]/ **VOUT[0]_AVID**/ VOUT[1]_Y_YC[5] | AT10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL121 | Video Output 0 Active Video output. This is the discrete active video indicator output. This signal is not used for embedded sync modes. |

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**Table 4-28. Video Output 0 [Pins AR8, AL9] Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Silicon Revision 1.x Devices** | | | | | |
| **HSYNC_VOUT[0]_AVID** | AR8 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL39 | Video Output 0 Active Video output. This is the discrete active video indicator output. This signal is not used for embedded sync modes. |
| **VSYNC_VOUT[0]_FLD** | AL9 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL38 | Video Output 0 Field ID output. This is the discrete field identification output. This signal is not used for embedded sync modes. |
| **Silicon Revision 2.x Devices** | | | | | |
| **DAC_HSYNC_ VOUT[0]_AVID** | AR8 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL39 | Pin supports two functions in silicon revision 2.x devices:<br>1. Video Output 0 Active Video output. This is the discrete active video indicator output. This signal is not used for embedded sync modes.<br>2. Discrete Horizontal Sync for HD-DACs.<br>Functionality is set in SPARE_CTRL0 register as defined in Section 9.10. |
| **DAC_VSYNC_ VOUT[0]_FLD** | AL9 | O | PULL: IPD / IPD<br>DRIVE: Z / Z<br>DVDD_3P3 | -<br>PINCTRL38 | Pin supports two functions in silicon revision 2.x devices:<br>1. Video Output 0 Field ID output. This is the discrete field identification output. This signal is not used for embedded sync modes.<br>2. Discrete Vertical Sync for HD-DACs.<br>Functionality is set in SPARE_CTRL0 register as defined in Section 9.10. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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**Table 4-29. Video Output 1 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_R_CR[0]/ VOUT[1]_C[8]/ **VOUT[1]_CLK** | AJ11 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL26 | Video Output 1 Clock output |
| **VOUT[1]_CLK**/ VIN[1]A_CLK | AT7 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL46 | |
| VOUT[0]_R_CR[9]/ VOUT[0]_B_CB_C[1]/ **VOUT[1]_Y_YC[9]** | AU9 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0] PINCTRL125 | Video Output 1 Data. These signals represent the 8 bits of Y/YC video data. For Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. |
| **VOUT[1]_Y_YC[9]**/ VIN[1]A_D[7] | AP6 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL19 | |
| VOUT[0]_R_CR[8]/ VOUT[0]_B_CB_C[0]/ **VOUT[1]_Y_YC[8]** | AK10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0] PINCTRL124 | |
| **VOUT[1]_Y_YC[8]**/ VIN[1]A_D[6] | AT6 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL18 | |
| VOUT[0]_R_CR[7]/ VOUT[0]_G_Y_YC[1]/ **VOUT[1]_Y_YC[7]** | AL10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0] PINCTRL123 | |
| **VOUT[1]_Y_YC[7]**/ VIN[1]A_D[5] | AR6 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL17 | |
| VOUT[0]_R_CR[6]/ VOUT[0]_G_Y_YC[0]/ **VOUT[1]_Y_YC[6]** | AU10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0] PINCTRL122 | |
| **VOUT[1]_Y_YC[6]**/ VIN[1]A_D[4] | AC13 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL16 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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**Table 4-29. Video Output 1 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_R_CR[5]/ VOUT[0]_AVID/ **VOUT[1]_Y_YC[5]** | AT10 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0] PINCTRL121 | Video Output 1 Data. These signals represent the 8 bits of Y/YC video data. For Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. |
| **VOUT[1]_Y_YC[5]**/ VIN[1]A_D[3] | AJ7 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL50 | |
| VOUT[0]_R_CR[4]/ VOUT[0]_FLD/ **VOUT[1]_Y_YC[4]** | AG13 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0] PINCTRL120 | |
| **VOUT[1]_Y_YC[4]**/ VIN[1]A_D[2] | AU6 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL49 | |
| VOUT[0]_R_CR[3]/ VOUT[0]_VSYNC / **VOUT[1]_Y_YC[3]** | AR11 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0] PINCTRL119 | |
| **VOUT[1]_Y_YC[3]** VIN[1]A_D[1] | AP7 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL48 | |
| VOUT[0]_R_CR[2]/ VOUT[0]_HSYNC/ **VOUT[1]_Y_YC[2]** | AT11 | O | PULL: IPD / DIS DRIVE: L / L DVDD_3P3 | VOUT[0] PINCTRL118 | |
| **VOUT[1]_Y_YC[2]**/ VIN[1]A_D[0] | AU7 | O | PULL: IPD / DIS DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL47 | |
| VOUT[0]_B_CB_C[0]/ **VOUT[1]_C[9]**/ VIN[1]B_HSYNC_DE | AR9 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VIN[1]B PINCTRL27 | Video Output 1 Data. These signals represent the 8 bits of C video data. For Y/C mode they are multiplexed Cb/Cr (Chroma) data bits, and for BT.656 mode they are unused. |
| VIN[0]A_D[19]/ VIN[1]A_DE/ **VOUT[1]_C[9]** | AK4 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VIN[1]A | |
| VIN[0]A_D[18]/ VIN[1]A_FLD/ **VOUT[1]_C[8]** | AK5 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VIN[1]A PINCTRL24 | |
| VOUT[0]_R_CR[0]/ **VOUT[1]_C[8]**/ VOUT[1]_CLK | AJ11 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL26 | |
| **VOUT[1]_C[7]**/ VIN[1]A_D[13] | AD13 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL10 | |
| **VOUT[1]_C[6]**/ VIN[1]A_D[12] | AN8 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL9 | |
| **VOUT[1]_C[5]**/ VIN[1]A_D[11] | AP8 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL8 | |
| **VOUT[1]_C[4]**/ VIN[1]A_D[10] | AN7 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL7 | |
| **VOUT[1]_C[3]**/ VIN[1]A_D[9]/ | AM8 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL6 | |
| **VOUT[1]_C[2]**/ VIN[1]A_D[8] | AK6 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL20 | |


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**Table 4-29. Video Output 1 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_D[16]/ VIN[1]A_HSYNC/ **VOUT[1]_FLD** | AT5 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VIN[1]A PINCTRL22 | Video Output 1 Field ID output. This is the discrete field identification output. This signal is not used for embedded sync modes. |
| VOUT[0]_G_Y_YC[1]/ **VOUT[1]_FLD**/ VIN[1]B_FLD | AU8 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VIN[1]B PINCTRL30 | |
| VOUT[0]_B_CB_C[1]/ VOUT[1]_HSYNC (silicon revision 1.x) DAC_VOUT[1]_HSYNC (silicon revision 2.x)/ **VOUT[1]_AVID** | AT9 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL28 | Video Output 1 Active Video output. This is the discrete active video indicator output. This signal is not used for embedded sync modes. |
| **VOUT[1]_AVID**/ VIN[1]B_CLK | AT4 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]B PINCTRL31 | |

**Table 4-30. Video Output 1 [Pins AT9, AR5, AP9, AL5] Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Silicon Revision 1.x Devices** | | | | | |
| VOUT[0]_B_CB_C[1]/ **VOUT[1]_HSYNC**/ VOUT[1]_AVID | AT9 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL28 | Video Output 1 Horizontal Sync output. This is the discrete horizontal synchronization output. This signal is not used for embedded sync modes. |
| **VOUT[1]_HSYNC**/ VIN[1]A_D[15] | AR5 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL21 | |
| VOUT[0]_G_Y_YC[0]/ **VOUT[1]_VSYNC**/ VIN[1]B_VSYNC | AP9 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VIN[1]B PINCTRL29 | Video Output 1 Vertical Sync output. This is the discrete vertical synchronization output. This signal is not used for embedded sync modes. |
| VIN[0]A_D[17]/ VIN[1]A_VSYNC/ **VOUT[1]_VSYNC** | AL5 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VIN[1]A PINCTRL23 | |
| **Silicon Revision 2.x Devices** | | | | | |
| VOUT[0]_B_CB_C[1]/ **DAC_VOUT[1]_HSYNC**/ VOUT[1]_AVID | AT9 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VOUT[1] PINCTRL28 | Pin supports two functions in silicon revision 2.x devices:<br>1. Video Output 1 Horizontal Sync output. This is the discrete horizontal synchronization output. This signal is not used for embedded sync modes.<br>2. Discrete Horizontal Sync for HD-DACs.<br>Functionality is set in SPARE_CTRL0 register as defined in Section 9.10. |
| **DAC_VOUT[1]_HSYNC**/ VIN[1]A_D[15] | AR5 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[1]A PINCTRL21 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PULL: A / B, where:
A is the state of the internal pull resistor during $\overline{\text{POR}}$ reset
B is the state of the internal pull resistor after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled
DRIVE: A / B, where;
A is the driving state of the pin during $\overline{\text{POR}}$ reset
B is the driving state of the pin after $\overline{\text{POR}}$ and Warm reset are de-asserted **and** during Warm reset
H = Driving High, L = Driving Low, Z = 3-State
For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.

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**Table 4-30. Video Output 1 [Pins AT9, AR5, AP9, AL5] Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_G_Y_YC[0]/ **DAC_VOUT[1]_VSYNC**/ VIN[1]B_VSYNC | AP9 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VOUT[0], VIN[1]B PINCTRL29 | Pin supports two functions in silicon revision 2.x devices:<br>1. Video Output 1 Vertical Sync output. This is the discrete vertical synchronization output. This signal is not used for embedded sync modes.<br>2. Discrete Vertical Sync for HD-DACs.<br>Functionality is set in SPARE_CTRL0 register as defined in Section 9.10. |
| VIN[0]A_D[17]/ VIN[1]A_VSYNC/ **DAC_VOUT[1]_VSYNC** | AL5 | O | PULL: IPD / IPD DRIVE: Z / Z DVDD_3P3 | VIN[0]A, VIN[1]A PINCTRL23 | |


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### 4.2.21 Analog Video Output Signals

**Table 4-31. Analog Video Output Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| **When a specific Video DAC output [IOUTA - IOUTG] is powered down, the corresponding Analog Video Output terminal functions should be left unconnected.** | | | | |
| IOUTA | AT21 | O | - | Video DAC A output. Analog HD Video DAC (G/Y) |
| IOUTB | AR21 | O | - | Video DAC B output. Analog HD Video DAC (B/Pb) |
| IOUTC | AP21 | O | - | Video DAC C output. Analog HD Video DAC (R/Pr) |
| IOUTD | AR20 | O | - | Video DAC D output. Analog SD Video DAC |
| IOUTE | AT19 | O | - | Video DAC E output. Analog SD Video DAC |
| IOUTF | AT20 | O | - | Video DAC F output. Analog SD Video DAC |
| IOUTG | AU20 | O | - | Video DAC G output. Analog SD Video DAC |
| DAC_VOUT[1]_HSYNC, DAC_HSYNC_ VOUT[0]_AVID | AR5, AT9, AR8 | O | - | Analog HD Video DAC Discrete HSYNC Output |
| DAC_VOUT[1]_VSYNC, DAC_VSYNC_ VOUT[0]_FLD | AL5, AP9, AL9 | O | - | Analog HD Video DAC Discrete VSYNC Output |
| VDAC_VREF | AH19 | I | - | Video DAC reference voltage (0.5 V).<br>When the video DACs are powered down, this pin should be left unconnected. |
| VDAC_RBIAS_HD | AE22 | IO | - | Video DAC HD current bias connection. This pin must be connected via an external 1.2-kΩ resistor to VSSA_HD.<br>When the HD DACs are powered down, this pin should be left unconnected. |
| VDAC_RBIAS_SD | AP19 | IO | - | Video DAC SD current bias connection. This pin must be connected via an external 1.2-kΩ resistor to VSSA_SD.<br>When the SD DACs are powered down, this pin should be left unconnected. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.

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### 4.2.22 Reserved Pins

**Table 4-32. Reserved Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| RSV1 | AB36 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV2 | P25 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV3 | N19 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV4 | N20 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV5 | T28 | IO | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV6 | T27 | IO | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV7 | AE23 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV8 | D24 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV9 | AU37 | I | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV10 | N28 | IO | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV11 | N29 | IO | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV12 | AG25 | S | - | Reserved. For proper device operation, this pin **must** be tied directly to the 1.8-V supply. |
| RSV13 | AG24 | S | - | Reserved. For proper device operation, this pin **must** be tied directly to the 1.8-V supply. |
| RSV14 | AH25 | S | - | Reserved. For proper device operation, this pin **must** be tied directly to the 1.8-V supply. |
| RSV15 | AH24 | S | - | Reserved. For proper device operation, this pin **must** be tied directly to the 1.8-V supply. |
| RSV16 | R34 | I | - | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |
| RSV17 | P34 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV18 | P33 | S | - | Reserved. For proper device operation, this pin **must** be tied directly to the 1.8-V supply. |
| RSV19 | P32 | GND | - | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |
| RSV20 | D14 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV21 | AN18 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV22 | AN19 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV23 | AP2 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV24 | AU3 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV25 | AN2 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV26 | AT1 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV27 | AR1 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV28 | AP1 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV29 | AM2 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV30 | AL2 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) IPD = Internal Pulldown Enabled, IPU = Internal Pullup Enabled, DIS = Internal Pull Disabled. This represents the default state of the internal pull after reset. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.3.1, *Pullup and Pulldown Resistors*.
(3) Specifies the operating IO supply voltage for each signal.


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**Table 4-32. Reserved Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| RSV31 | AK1 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV32 | AL1 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV33 | AM29 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV34 | AL28 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV35 | AL29 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV36 | AN29 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV37 | AP29 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV38 | AR29 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV39 | AT29 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV40 | AT28 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV41 | AU21 | O | - | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV42 | AJ1 | IO | IPU DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV43 | AK2 | IO | IPU DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV44 | AH8 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV45 | AJ2 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV46 | AK3 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV47 | AJ3 | O | DIS DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV48 | AJ4 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV49 | AJ5 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV50 | AJ6 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV51 | AB13 | I | IPD DVDD_3P3 | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV52 | AE21 | S | - | Reserved. For proper device operation, this pin should be connected to a 1.0-V power supply. |
| RSV53 | AG22 | S | - | Reserved. For proper device operation, this pin should be connected to a 1.8-V power supply. |
| RSV54 | AG23 | S | - | Reserved. For proper device operation, this pin should be connected to a 1.8-V power supply. |
| RSV55 | AH23 | S | - | Reserved. For proper device operation, this pin should be connected to a 1.8-V power supply. |
| RSV56 | AJ23 | S | - | Reserved. For proper device operation, this pin should be connected to a 1.8-V power supply. |
| RSV57 | AK22 | GND | - | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |
| RSV58 | AL22 | GND | - | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |

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**Table 4-32. Reserved Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| RSV59 | AM22 | GND | - | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |
| RSV60 | AM21 | GND | - | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |
| RSV61 | AN21 | GND | - | Reserved. For proper device operation, this pin **must** be tied directly to $V_{SS}$. |


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### 4.2.23 Supply Voltages

**Table 4-33. Supply Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| VREFSSTL_DDR[0] | A17 | S | - | Reference Power Supply DDR[0]:<br>• 0.75-V for DDR3 memory type<br>• 0.9-V for DDR2 memory type |
| VREFSSTL_DDR[1] | A21 | S | - | Reference Power Supply DDR[1]<br>• 0.75-V for DDR3 memory type<br>• 0.9-V for DDR2 memory type |
| CVDD | AD22, AD21, AD20, AD19, AD18, AD17, AD16, AC22, AC21, AC20, AC19, AC18, AC17, AC16, AB24, AB23, AB22, AB21, AB20, AB19, AB18, AB17, AB16, AB15, AB14, T24, T23, T22, T21, T20, T19, T18, T17, T16, T15, T14, R22, R21, R20, R19, R18, R17, R16, P22, P21, P20, P19, P18, P17, P16 | S | - | Variable Core Voltage Supply for the Always ON Domain |
| CVDDC | AE25, AE13, AD24, AD23, AD15, AD14, AC24, AC23, AC15, AC14, R24, R23, R15, R14, P24, P23, P15, P14, N25, N13 | S | - | 1.0-V Constant Power Supply for Memories and PLLs |
| VDD_USB_0P9 | N27 | S | - | 0.9-V Power Supply for USB PHYs.<br>**Note:** If the USB is not used, for proper device operation, this pin ***must*** be connected to a power supply (0.9 V or CVDDC). |
| VDDT_SATA | Y34, Y33, V34, V32 | S | - | 1.0-V Power Supply for SATA Termination and Analog Front End<br>**Note:** If the SATA is not used, for proper device operation, these pins ***must*** be connected to a 1.0-V power supply. |
| VDDT_PCIE | Y30, Y28, AB32, AB29, AB27 | S | - | 1.0-V Power Supply for PCIe Termination and Analog Front End<br>**Note:** If the PCIe is not used, these pins should be connected to a 1.0-V power supply. |
| VDDA_PLL | B18, A18 | S | - | 1.5-V Analog Power Supply for PLLs |
| VDDA_HDMI | AR27, AP24, AP23, AN24, AN23 | S | - | 1.0-V Analog Power Supply for HDMI<br>**Note:** If the HDMI is not used, these pins should be connected to a 1.0-V power supply. |
| VDDA_HD_1P0 | AG21 | S | - | 1.0-V Analog Power Supply for VDAC HD DAC<br>**Note:** If the HD DAC is not used, this pin should be connected to a 1.0-V power supply. |
| VDDA_SD_1P0 | AG20 | S | - | 1.0-V Analog Power Supply for VDAC SD DAC<br>**Note:** If the SD DAC is not used, this pin should be connected to a 1.0-V power supply. |
| VDDR_SATA | V25, U25 | S | - | 1.5-V Regulator Power Supply for SATA<br>**Note:** If the SATA is not used, for proper device operation, these pins ***must*** be connected to a 1.5-V power supply. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.

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**Table 4-33. Supply Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER | DESCRIPTION |
|---|---|---|---|---|
| VDDR_PCIE | Y25, W25 | S | - | 1.5-V Regulator Power Supply for PCIe<br>**Note:** If the PCIe is not used, for proper device operation, these pins ***must*** be connected to a 1.5-V power supply. |
| DVDD_DDR[0] | L19, L18, L17, L16, L15, L14, K19, K18, K17, K16, K15, K14, J18, J17, J16, J15, J14, E11, A11, E1, A2 | S | - | Power Supply for DDR[0] IOs:<br>• 1.5-V for DDR3 memory type<br>• 1.8-V for DDR2 memory type |
| DVDD_DDR[1] | L24, L23, L22, L21, L20, K24, K23, K22, K21, K20, J24, J23, J22, J21, J20, J19, E27, D37, A36, A27 | S | - | 1.5-V Power Supply for DDR[1] IOs:<br>• 1.5-V for DDR3 memory type<br>• 1.8-V for DDR2 memory type |
| DEVOSC_DVDD18 | E19 | S | - | 1.8-V Power Supply for Device Oscillator<br>**Note:** If the oscillator is not used, this pin should be connected to the 1.8-V power supply (DVDD1P8). |
| VDD_USB0_1P8 | R25 | S | - | 1.8-V Power Supply for USB0<br>**Note:** If the USB is not used, for proper device operation, this pin ***must*** be connected to a 1.8-V power supply, or when the USB PHY is not used, this pin can be *optionally* connected to CVDDC. |
| VDD_USB1_1P8 | T25 | S | - | 1.8-V Power Supply for USB1<br>**Note:** If the USB is not used, for proper device operation, this pin ***must*** be connected to a 1.8-V power supply, or when the USB PHY is not used, this pin can be *optionally* connected to CVDDC. |
| DVDD1P8 | AJ20, AJ24 | S | - | 1.8-V Power Supply |
| VDDA_REF_1P8 | AT22 | S | - | 1.8-V Reference Power Supply for VDAC<br>**Note:** If the VDAC is not used, these pins should be connected to a 1.8-V power supply. |
| VDDA_HD_1P8 | AJ22, AH22 | S | - | 1.8-V Analog Power Supply for VDAC HD DAC<br>**Note:** If the HD DAC is not used, these pins should be connected to a 1.8-V power supply. |
| VDDA_SD_1P8 | AJ21, AH21, AH20 | S | - | 1.8-V Analog Power Supply for VDAC SD DAC<br>**Note:** If the SD DAC is not used, these pins should be connected to a 1.8-V power supply. |


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**Table 4-33. Supply Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| DVDD_3P3 | AU29, AU11, AU2, AN37, AN27, AN11, AN1, AJ17, AJ16, AJ15, AJ14, AH17, AH16, AH15, AH14, AG33, AG17, AG16, AG15, AG14, AE29, AE28, AE27, AD29, AD28, AD27, AD11, AD10, AD9, AC29, AC28, AC27, AC11, AC10, AC9, AB11, AB10, AB9, AA11, AA10, AA9, AA1, Y9, U11, U10, U9, T11, T10, T9, R28, R27, R11, R10, R9, P30, P29, P28, P27, P11, P10, P9, P8, L35, L30, L5, L1 | S | - | 3.3-V Power Supply |
| VDD_USB0_3P3 | T29, R29 | S | - | 3.3-V Power Supply for USB0 |
| VDD_USB1_3P3 | T30, R30 | S | - | 3.3-V Power Supply for USB1 |

### 4.2.24 Ground Pins ($V_{SS}$)

**Table 4-34. Ground Terminal Functions**

| SIGNAL | | TYPE[1] | OTHER | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| VSS | AU28, AU23, AU12, AU1, AT23, AR25, AR24, AR23, AR15, AP37, AP15, AN15, AN14, AM31, AM25, AM24, AM23, AM19, AM18, AM17, AM16, AM15, AM7, AM1, AL32, AL31, AL24, AL23, AL19, AL18, AL17, AL16, AL15, AL7, AL6, AK27, AK24, AK23, AK19, AK18, AK17, AK16, AK15, AK11, AJ25, AJ18, AG30, AG26, AG12, AG8, AG5, AF27, AF11, AE20, AE19, AE18, AE17, AD34, AD33, AD32, AD31, AD30, AD7, AD6, AD5, AC34, AC33, AC32, AC31, AC30, AC8, AC7, AC6, AC4, AC3, AB37, AB35, AB8, AB7, AB6, AB1, AA24, AA23, AA22, AA21, AA20, AA19, AA18, AA17, AA16, AA15, AA14, AA13, AA8, AA7, AA6, AA5, Y37, Y36, Y32, Y31, Y24, Y23, Y22, Y21, Y20, Y19, Y18, Y17, Y16, Y15, Y14, Y13, Y8, Y7, Y6, Y5, Y4, W24, W23, W22, W21, W20, W19, W18, W17, W16 | GND | - | Ground (GND) |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.


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**Table 4-34. Ground Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| VSS | W15, W14, W13, W9, W8, W7, W6, V28, V27, V24, V23, V22, V21, V20, V19, V18, V17, V16, V15, V14, V13, V9, V8, V7, V6, V5, V4, U24, U23, U22, U21, U20, U18, U17, U16, U15, U14, U13, U8, U7, U6, U5, T35, T34, T33, T8, T7, T6, R33, R32, R31, R8, R7, R6, R4, R3, P31, P7, P6, P5, P4, N18, M27, M11, L33, L26, L12, L8, K37, K1, H27, H24, H23, H22, H21, H20, H19, H18, H17, H16, H15, H14, H11, G32, G31, G24, G23, G22, G21, G20, G18, G17, G16, G15, G14, G7, G6, F31, F24, F23, F22, F21, F17, F16, F15, F14, F7, E37, E24, E14, D1, C23, C21, C17, C15, A37, A28, A10, A1 | GND | - | Ground (GND) |
| VSSA_PLL | U19, B20, A20 | GND | - | Analog GND for PLLs |
| VSSA_HD | AK21, AK20, AL21 | GND | - | Analog GND for VDAC HD DAC |
| VSSA_SD | AU19, AM20, AN20, AL20 | GND | - | Analog GND for VDAC SD DAC |
| VSSA_REF_1P8 | AU22 | GND | - | Reference GND for VDAC (1.8 V) |
| DEVOSC_VSS | B19 | GND | - | Ground for Device Oscillator |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings (Unless Otherwise Noted)(1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Steady State Supply voltage ranges: | USB PHYs, 0.9 V (VDD_USB_0P9) | -0.3 | 1.35 | V |
| | Core (CVDD, CVDDC, VDDT_SATA, VDDT_PCIE, VDDA_HDMI, VDDA_HD_1P0, VDDA_SD_1P0) | -0.3 | 1.2 | V |
| | IO, 1.5 V (VDDA_PLL, VDDR_SATA, VDDR_PCIE, DVDD_DDR0, DVDD_DDR1)(3) | -0.3 | 2.45 | V |
| | IO, 1.8 V (DVDD1P8, DEVOSC_DVDD18, VDD_USB0_1P8, VDD_USB1_1P8, VDDA_REF_1P8, VDDA_HD_1P8, VDDA_SD_1P8, DVDD_DDR0, DVDD_DDR1)(3) | -0.3 | 2.45 | V |
| | IO, 3.3 V (DVDD_3P3, VDD_USB0_3P3, VDD_USB1_3P3) | 0 | 3.8 | V |
| Input and Output voltage ranges: | V IO, 1.5-V pins | -0.3<br>-0.3 | 2.45<br>DVDD_DDRx + 0.3(3) | V |
| | V IO, 1.8-V pins | -0.3<br>-0.3<br>-0.3 | 2.45<br>DVDD1P8 + 0.3<br>DVDD_DDRx + 0.3(3) | V |
| | V IO, 3.3-V pins (Steady State) | -0.3<br>-0.3 | 3.8<br>DVDD_3P3 + 0.3 | V |
| | V IO, 3.3-V pins (Transient Overshoot and Undershoot) | 20% of DVDD_3P3 for up to 20% of the signal period | | V |
| Operating junction temperature range, $T_J$:(4) | (default) | 0 | 95 | °C |
| | extended temperature | -40 | 105 | |
| Storage temperature range, $T_{stg}$: | (Default) | -55 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VSS.
(3) For supply voltage pins, DVDD_DDRx:
- 1.5 V is used for DDR3 SDRAM.
- 1.8 V is used for DDR2 SDRAM.

(4) A heat dissipation solution is required for proper device operation. Thermal performance of the overall system must be carefully considered to ensure conformance with the recommended operating conditions. Heat generated by this device must be removed with the help of heat sinks, heat spreaders, or airflow. SmartReflex can significantly lower the power consumption of this device and its use is required for proper device operation. A thermal model can be provided for thermal simulation to estimate the system thermal environment. Contact your local TI representative for availability.

## 5.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| ESD stress voltage, $V_{ESD}$:(1) | HBM (Human Body Model)(2) | ±1000 | V |
| | CDM (Charged-Device Model)(3) | ±250 | V |

(1) Electrostatic discharge (ESD) to measure device sensitivity or immunity to damage caused by electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001-2010. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500 V HBM is possible if necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have higher performance.


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## 5.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| CVDD | Supply voltage, Variable Core, Adaptive Voltage Scaling (CVDD)(1) | Initial Startup | VINITnom × 0.95 | 1.00 or 1.05(2) | VINITnom × 1.05 | V |
| | | CYGA2 & CYG4 | SRnom(3) × 0.95 | 0.85 - 1.00 | SRnom × 1.05 | |
| | | CYG & CYG2 | SRnom × 0.95 | 0.85-1.05(4) | SRnom × 1.05 | |
| CVDDC | Supply voltage, Constant Core (CVDDC, VDDT_SATA, VDDT_PCIE, VDDA_HDMI, VDDA_HD_1P0, VDDA_SD_1P0) | | 0.95 | 1 | 1.05 | V |
| DVDD | Supply voltage, IO, 3.3 V (DVDD_3P3, VDD_USB0_3P3, VDD_USB1_3P3) (except I2C pins) | | 3.13 | 3.3 | 3.47 | V |
| | Supply voltage, IO, I2C (DVDD_3P3) | | 3.13 | 3.3 | 3.47 | V |
| | Supply voltage, IO, 1.8 V (DVDD1P8, DEVOSC_DVDD18, VDD_USB0_1P8, VDD_USB1_1P8, VDDA_REF_1P8, VDDA_HD_1P8, VDDA_SD_1P8, DVDD_DDR0, DVDD_DDR1)(5) | | 1.71 | 1.8 | 1.89 | V |
| | Supply voltage, IO, 1.5 V (VDDA_PLL, VDDR_SATA, VDDR_PCIE, DVDD_DDR0, DVDD_DDR1)(5) | | 1.43 | 1.5 | 1.58 | V |
| | Supply voltage, IO, 0.9 V (VDD_USB_0P9) | | 0.85 | 0.9 | 0.95 | V |
| VSS | Supply ground (VSS, VSSA_PLL, VSSA_HD, VSSA_SD, VSSA_REF_1P8, DEVOSC_VSS)(6) | | 0 | 0 | 0 | V |
| DDR_VREF | DDR2 and DDR3 reference voltage(7) | | 0.48DVDD_DDRx | 0.5DVDD_DDRx | 0.52DVDD_DDRx | V |
| $V_{IH}$ | High-level input voltage, 3.3 V (except I2C pins) | | 2 | | | V |
| | High-level input voltage, I2C | | 0.7DVDD_3P3 | | | |
| | High-level input voltage, 1.8 V | | 0.65DVDD1P8 | | | |
| $V_{IL}$ | Low-level input voltage, 3.3 V (except I2C pins) | | | | 0.8 | V |
| | Low-level input voltage, I2C | | | | 0.3DVDD_3P3 | |
| | Low-level input voltage, 1.8 V | | | | 0.35DVDD1P8 | |
| $I_{OH}$ | High-level output current | 6-mA IO buffers | | | -6 | mA |
| | | DDR[0], DDR[1] buffers @ 50-Ω impedance setting | | | -8 | |
| $I_{OL}$ | Low-level output current | 6-mA IO buffers | | | 6 | mA |
| | | DDR[0], DDR[1] buffers @ 50-Ω impedance setting | | | 8 | |
| $V_{ID}$ | Differential input voltage (SERDES_CLKN and SERDES_CLKP), [AC coupled] | | 0.25 | | 2.0 | V |

(1) This device supports, and requires the use of, SmartReflex technology with Adaptive Voltage Scaling based on die temperature and performance. The SmartReflex codes output from the device correspond to up to 32 linear voltage steps within the specified voltage range (32 steps is the recommended software upper limit and is not constrained by the silicon design), with the option to use fewer steps if desired, with a minimum of eight steps. TI requires that users design a supply that can handle multiple voltage steps within this range with ± 5% tolerances. Not incorporating a flexible supply may limit the system's ability to use the power saving capabilities of the SmartReflex technology. TI recommends using a fault-tolerant power supply design to protect against over-current conditions. For more details about adaptive voltage scaling for this device, see the AVS FAQ. For AVS disable data to aid in design of robust power supplies that may withstand momentary AVS control failure, see the device Power Estimation Spreadsheet (literature number SPRABK3).
(2) The initial CVDD voltage at power on must be 1.00V nominal (for CYGA2 and CYG4 devices) or 1.05V nominal (for CYG and CYG2 devices) and it must transition to the AVS target value adjusted by a AVS driver. This is required to maintain full power functionality and reliability targets specified by TI.
(3) SRnom refers to the unique SmartReflex core supply voltage set from the factory for each individual device.
(4) Upper range limit of 1.10 nominal value allowed.
(5) For supply voltage pins, DVDD_DDRx:
- 1.5 V is used for DDR3 SDRAM.
- 1.8 V is used for DDR2 SDRAM.

(6) Oscillator ground (DEVOSC_VSS) must be kept separate from other grounds and connected directly to the crystal load capacitor ground.
(7) DDR_VREF is expected to equal 0.5DVDD_DDRx of the transmitting device and to track variations in the DVDD_DDRx.

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## Recommended Operating Conditions *(continued)*

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_t$ | Transition time, 10%-90%, All Inputs (unless otherwise specified in the electrical data sections) | | | Lesser of 0.25P or 10[8] | ns |
| $T_J$ | Operating junction temperature range[9] | 0 | | 95 | °C |
| | Extended operating junction temperature range | -40 | | 105 | |

(8) P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

(9) A heat dissipation solution is required for proper device operation. Thermal performance of the overall system must be carefully considered to ensure conformance with the recommended operating conditions. Heat generated by this device must be removed with the help of heat sinks, heat spreaders, or airflow. SmartReflex can significantly lower the power consumption of this device and its use is required for proper device operation. A thermal model can be provided for thermal simulation to estimate the system thermal environment. Contact your local TI representative for availability.


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## Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

| PARAMETER | | TEST CONDITIONS(1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Low and full speed: USB_DN and USB_DP | | 2.8 | | VDD_USBx_3P3 | V |
| | High speed: USB_DN and USB_DP | | 360 | | 440 | mV |
| | High-level output voltage (3.3-V IO) | DVDD_3P3 = MIN, $I_{OH}$ = MAX | 2.4 | | | V |
| $V_{OL}$ | Low and full speed: USB_DN and USB_DP | | 0.0 | | 0.3 | V |
| | High speed: USB_DN and USB_DP | | -10 | | 10 | mV |
| | Low-level output voltage (3.3-V IO except I2C pins) | DVDD_3P3 = MIN, $I_{OL}$ = MAX | | | 0.4 | V |
| | Low-level output voltage (3.3-V IO I2C pins) | IO = 3 mA | | | 0.4 | V |
| $I_I$(2) | Input current [DC] (except I2C pins) | VI = VSS to DVDD_3P3 without opposing internal resistor | | | ±1 | µA |
| | | VI = VSS to DVDD_3P3 with opposing internal pullup resistor(3) | | 100 | | µA |
| | | VI = VSS to DVDD_3P3 with opposing internal pulldown resistor(3) | | -100 | | µA |
| | Input current [DC] (I2C) | VI = VSS to DVDD_3P3 | | | ±20 | µA |
| $I_{OZ}$(4) | IO Off-state output current | VO = DVDD_3P3 or VSS; internal pull disabled | | | ±5 | µA |
| | | VO = DVDD_3P3 or VSS; internal pull enabled | | ±100 | | µA |

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.
(2) $I_I$ applies to input-only pins and bi-directional pins. For input-only pins, $I_I$ indicates the input leakage current. For bi-directional pins, $I_I$ indicates the input leakage current and off-state (Hi-Z) output leakage current.
(3) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.
(4) $I_{OZ}$ applies to output-only pins, indicating off-state (Hi-Z) output leakage current.

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## Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted) *(continued)*

| PARAMETER | | TEST CONDITIONS(1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CDD}$ | Constant Core (CVDDC) supply current(5) | • Case Temp = 60ºC<br>• ARM at 1.2 GHz, 75% utilization<br>• DSP at 1 GHz, 25% utilization<br>• HDVICP2-0 at 600 MHz, 1-ch 1080p60 encode<br>• HDVICP2-1 at 600 MHz, 1-ch 1080p60 decode<br>• HDMI display<br>• SGX530 at 150 MHz, 15 fps<br>• EMIF0 and EMIF1 at 800 MHz, 4480 MBps<br>• USB 1x, EMAC 1x, SATA | | 1491(6) | | mA |
| | Variable Core (CVDD) supply current(5) | | | 6463(6) | | |
| $I_{DDD}$ | 3.3-V IO (DVDD_3P3, USB_VDDA3P3) supply current(5) | • Case Temp = 60ºC<br>• ARM at 1.2 GHz, 75% utilization<br>• DSP at 1 GHz, 25% utilization<br>• HDVICP2-0 at 600 MHz, 1-ch 1080p60 encode<br>• HDVICP2-1 at 600 MHz, 1-ch 1080p60 decode<br>• HDMI display<br>• SGX530 at 150 MHz, 15 fps<br>• EMIF0 and EMIF1 at 800 MHz, 4480 MBps<br>• USB 1x, EMAC 1x, SATA | | 19(6) | | mA |
| | 1.8-V IO (DVDD1P8, DVDD_DDRx) supply current(5)(7) | | | 11(6) | | |
| | 1.5-V IO (DVDD_DDRx) supply current(5)(7) | | | 1241(6) | | |
| $C_I$ | Input capacitance | | | | 2.8 | pF |
| $C_o$ | Output capacitance | | | | 2.8 | pF |

(5) The actual current draw varies across manufacturing processes and is highly application-dependent. For use-case specific power estimates, see the device Power Estimation Spreadsheet (literature number SPRABK3).
(6) The $I_{CDD}$ and $I_{DDD}$ TYP power values shown in this table correspond to device speed grade 2 (CYG2).
(7) For supply voltage pins, DVDD_DDRx:
- 1.5 V is used for DDR3 SDRAM.
- 1.8 V is used for DDR2 SDRAM.

## 5.4 Thermal Resistance Characteristics

**Table 5-1. Thermal Resistance Characteristics (PBGA Package) [CYG]**

| NO. | | | °C/W(1) |
|---|---|---|---|
| 1 | $R\Theta_{JC}$ | Junction-to-case | 0.21 |
| 2 | $R\Theta_{JB}$ | Junction-to-board | 3.93 |

(1) For proper device operation, a heatsink is required.


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# 6 Device Configurations

## 6.1 Control Module

The device control module includes status and control logic not addressed within the peripherals or the remainder of the device infrastructure. This module is the primary point of control for the following areas of the device:

- Functional IO multiplexing
- Device status
- Static device configuration
- Open-core protocol (OCP) interface for standard and customer programmable e-Fuse bit shift registers.

The control module primarily implements a bank of registers accessible (read and write) by the software along with some read-only registers carrying status information. Most register bits are exported as control signals for other logic blocks on the device. Certain control module registers have default values based upon the device type as decoded from e-Fuse.

The read and write registers can be divided into the following classes:

- Static device configuration registers
- Status and configuration registers
- Boot registers

Table 6-1 shows the general register groupings and Table 6-2 through Table 6-4 provide register summaries for each group.

**Table 6-1. Control Module Register Map**

| ADDRESS OFFSET | REGISTER GROUP | SEE |
|---|---|---|
| 0x0000 - 0x0020 | OCP Configuration registers | Table 6-2 |
| 0x0024 - 0x003C | Reserved | |
| 0x0040 – 0x00FC | Device Boot registers | Table 6-7 |
| 0x0300 - 0x03FC | Reserved | |
| 0x0400 - 0x05FC | PLL Control registers | Table 6-3 |
| 0x0600 - 0x07FC | Device Configuration registers | Table 6-4 |
| 0x0800 - 0x0FFC | PAD Control registers | Section 6.5 |

**Table 6-2. OCP Configuration Registers Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0000 | CONTROL_REVISION | Control module Revision number |
| 0x4814 0004 - 0x4814 000C | - | Reserved |
| 0x4814 0010 | CONTROL_SYSCONFIG | Idle mode parameters |
| 0x4814 0014 - 0x4814 003C | - | Reserved |

**Table 6-3. PLL Control Registers Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0400 | MAINPLL_CTRL | Main PLL base frequency control |
| 0x4814 0404 | MAINPLL_PWD | Main PLL clock output powerdown |
| 0x4814 0408 | MAINPLL_FREQ1 | Main Clock 1 fractional divider |
| 0x4814 040C | MAINPLL_DIV1 | Main Clock 1 post divider |
| 0x4814 0410 | MAINPLL_FREQ2 | Main Clock 2 fractional divider |
| 0x4814 0414 | MAINPLL_DIV2 | Main Clock 2 post divider |

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**Table 6-3. PLL Control Registers Summary (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0418 | MAINPLL_FREQ3 | Main Clock 3 fractional divider |
| 0x4814 041C | MAINPLL_DIV3 | Main Clock 3 post divider |
| 0x4814 0420 | MAINPLL_FREQ4 | Main Clock 4 fractional divider |
| 0x4814 0424 | MAINPLL_DIV4 | Main Clock 4 post divider |
| 0x4814 0428 | MAINPLL_FREQ5 | Main Clock 5 fractional divider |
| 0x4814 042C | MAINPLL_DIV5 | Main Clock 5 post divider |
| 0x4814 0430 | - | Reserved |
| 0x4814 0434 | MAINPLL_DIV6 | Main Clock 6 post divider |
| 0x4814 0438 | - | Reserved |
| 0x4814 043C | MAINPLL_DIV7 | Main Clock 7 post divider |
| 0x4814 0440 | DDRPLL_CTRL | DDR PLL base frequency control |
| 0x4814 0444 | DDRPLL_PWD | DDR PLL clock output powerdown |
| 0x4814 0448 | - | Reserved |
| 0x4814 044C | DDR_PLL_DIV1 | DDR Clock 1 post divider |
| 0x4814 0450 | DDRPLL_FREQ2 | DDR Clock 2 fractional divider |
| 0x4814 0454 | DDR_PLL_DIV2 | DDR Clock 2 post divider |
| 0x4814 0458 | DDRPLL_FREQ3 | DDR Clock 3 fractional divider |
| 0x4814 045C | DDR_PLL_DIV3 | DDR Clock 3 post divider |
| 0x4814 0460 | DDRPLL_FREQ4 | DDR Clock 4 fractional divider |
| 0x4814 0464 | DDR_PLL_DIV4 | DDR Clock 4 post divider |
| 0x4814 0468 | DDRPLL_FREQ5 | DDR Clock 5 fractional divider |
| 0x4814 046C | DDR_PLL_DIV5 | DDR Clock 5 post divider |
| 0x4814 0470 | VIDEOPLL_CTRL | Video PLL base frequency control |
| 0x4814 0474 | VIDEOPLL_PWD | Video PLL clock output powerdown |
| 0x4814 0478 | VIDEOPLL_FREQ1 | Video Clock 1 fractional divider |
| 0x4814 047C | VIDEOPLL_DIV1 | Video Clock 1 post divider |
| 0x4814 0480 | VIDEOPLL_FREQ2 | Video Clock 2 fractional divider |
| 0x4814 0484 | VIDEOPLL_DIV2 | Video Clock 2 post divider |
| 0x4814 0488 | VIDEOPLL_FREQ3 | Video Clock 3 fractional divider |
| 0x4814 048C | VIDEOPLL_DIV3 | Video Clock 3 post divider |
| 0x4814 0490 - 0x4814 049C | - | Reserved |
| 0x4814 04A0 | AUDIOPLL_CTRL | Audio PLL base frequency control |
| 0x4814 04A4 | AUDIOPLL_PWD | Audio PLL clock output powerdown |
| 0x4814 04A8 | - | Reserved |
| 0x4814 04AC | - | Reserved |
| 0x4814 04B0 | AUDIOPLL_FREQ2 | Audio Clock 2 fractional divider |
| 0x4814 04B4 | AUDIOPLL_DIV2 | Audio Clock 2 post divider |
| 0x4814 04B8 | AUDIOPLL_FREQ3 | Audio Clock 3 fractional divider |
| 0x4814 04BC | AUDIOPLL_DIV3 | Audio Clock 3 post divider |
| 0x4814 04C0 | AUDIOPLL_FREQ4 | Audio Clock 4 fractional divider |
| 0x4814 04C4 | AUDIOPLL_DIV4 | Audio Clock 4 post divider |
| 0x4814 04C8 | AUDIOPLL_FREQ5 | Audio Clock 5 fractional divider |
| 0x4814 04CC | AUDIOPLL_DIV5 | Audio Clock 5 post divider |
| 0x4814 04D0 - 0x4814 05FC | - | Reserved |


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**Table 6-4. Device Configuration Registers Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0600 | DEVICE_ID | Device Identification |
| 0x4814 0604 | - | Reserved |
| 0x4814 0608 | INIT_PRESSURE_0 | L3 Initiator Pressure |
| 0x4814 060C | INIT_PRESSURE_1 | L3 Initiator Pressure |
| 0x4814 0610 | MMU_CFG | System MMU Configuration |
| 0x4814 0614 | TPTC_CFG | Transfer Controller Configuration |
| 0x4814 0618 | DDR_CTRL | DDR Interface Control |
| 0x4814 061C | DSP_IDLE_CFG | DSP Standby and Idle Management Configuration |
| 0x4814 0620 | USB_CTRL | USB Control |
| 0x4814 0624 | USBPHY_CTRL0 | USB0 Phy Control |
| 0x4814 0628 | - | Reserved |
| 0x4814 062C | USBPHY_CTRL1 | USB1 Phy Control |
| 0x4814 0630 | MAC_ID0_LO | Ethernet MAC Address 0 |
| 0x4814 0634 | MAC_ID0_HI | Ethernet MAC Address 0 |
| 0x4814 0638 | MAC_ID1_LO | Ethernet MAC Address 1 |
| 0x4814 063C | MAC_ID1_HI | Ethernet MAC Address 1 |
| 0x4814 0640 | PCIE_CFG | PCIe Module Configuration |
| 0x4814 0644 | - | Reserved |
| 0x4814 0648 | CLK_CTRL | Input Oscillator Control |
| 0x4814 064C | AUDIO_CTRL | Audio Control |
| 0x4814 0650 | DSPMEM_SLEEP | DSP Memory Sleep Mode Configuration |
| 0x4814 0654 | OCMEM_SLEEP | On-Chip Memory Sleep Mode Configuration |
| 0x4814 0658 - 0x4814 065C | - | Reserved |
| 0x4814 0660 | HD_DAC_CTRL | HD DAC Control |
| 0x4814 0664 | HD_DACA_CAL | HD DAC A Calibration |
| 0x4814 0668 | HD_DACB_CAL | HD DAC B Calibration |
| 0x4814 066C | HD_DACC_CAL | HD DAC C Calibration |
| 0x4814 0670 | SD_DAC_CTRL | SD DAC Control |
| 0x4814 0674 | SD_DACA_CAL | SD DAC A Calibration |
| 0x4814 0678 | SD_DACB_CAL | SD DAC B Calibration |
| 0x4814 067C | SD_DACC_CAL | SD DAC C Calibration |
| 0x4814 0680 | SD_DACD_CAL | SD DAC D Calibration |
| 0x4814 0684 - 0x4814 0688 | - | Reserved |
| 0x4814 068C | BANDGAP_CTRL | DAC Band-gap Control |
| 0x4814 0690 | HW_EVT_SEL_GRP1 | System Trace Hardware Event Select Group 1 |
| 0x4814 0694 | HW_EVT_SEL_GRP2 | System Trace Hardware Event Select Group 2 |
| 0x4814 0698 | HW_EVT_SEL_GRP3 | System Trace Hardware Event Select Group 3 |
| 0x4814 069C | HW_EVT_SEL_GRP4 | System Trace Hardware Event Select Group 4 |
| 0x4814 06A0 - 0x4814 06F4 | - | Reserved |
| 0x4814 06F8 | HDMI_OBSCLK_CTRL | HDMI Observe Clock Control |
| 0x4814 06FC | SERDES_CTRL | Serdes Control |
| 0x4814 0700 | UCB_CLK_CTL | USB Clock Control |
| 0x4814 0704 | PLL_OBSCLK_CTRL | PLL Observe Clock Control |
| 0x4814 0708 | - | Reserved |
| 0x4814 070C | DDR_RCD | RCD Power Enable or Disable |
| 0x4814 0710 - 0x4814 07FC | - | Reserved |

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## 6.2 Revision Identification

The silicon revision can be read in the DEVREV bit field value of the device identification (DEVICE_ID) register (located at 0x4814 0600). The DEVREV field of the DEVICE_ID register changes between silicon revisions. Table 6-5 lists the contents of the device revision (DEVREV) field value for each revision of the device.

**Table 6-5. Device Revision (DEVREV) Bit Field Value**

| SILICON REVISION | DEVICE REVISION FIELD VALUE DEVREV[31:28] |
|---|---|
| 2.1 | 0011 |
| 2.0 | 0010 |
| 1.1 | 0001 |
| 1.0 | 0000 |

More details on the DEVICE_ID register can be found in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

## 6.3 Debugging Considerations

### 6.3.1 Pullup and Pulldown Resistors

Proper board design should ensure that input pins to the device always be at a valid logic level and not floating. This may be achieved via pullup and pulldown resistors. The device features internal pullup (IPU) and internal pulldown (IPD) resistors on most pins to eliminate the need, unless otherwise noted, for external pullup or pulldown resistors.

An external pullup or pulldown resistor needs to be used in the following situations:

- *Boot and Configuration Pins*: If the pin is both routed out and 3-stated (not driven), an external pullup or pulldown resistor is ***strongly recommended***, even if the IPU or IPD matches the desired value or state.
- *Other Input Pins*: If the IPU or IPD *does not* match the desired value or state, use an external pullup or pulldown resistor to pull the signal to the opposite rail.

For the boot and configuration pins (listed in Table 4-1, *Boot Terminal Functions*), if they are both routed out and 3-stated (not driven), it is ***strongly recommended*** that an external pullup or pulldown resistor be implemented. Although, internal pullup and pulldown resistors exist on these pins and they may match the desired configuration value, providing external connectivity can help ensure that valid logic levels are latched on these device boot and configuration pins. In addition, applying external pullup or pulldown resistors on the boot and configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

Tips for choosing an external pullup or pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest $V_{IL}$ level of all inputs connected to the net. For a pullup resistor, this should be above the highest $V_{IH}$ level of all inputs on the net. A reasonable choice would be to target the $V_{OL}$ or $V_{OH}$ levels for the logic family of the limiting device; which, by definition, have margin to the $V_{IL}$ and $V_{IH}$ levels.
- Select a pullup or pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup and pulldown resistors on the net.


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- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the $DV_{DD}$ rail.

For most systems, a 1-kΩ resistor can be used to oppose the IPU or IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can be used to compliment the IPU or IPD on the boot and configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can also be used as an external pullup or pulldown on the pins that have IPUs or IPDs disabled and require an external pullup or pulldown resistor while still meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current ($I_I$), and the low-level or high-level input voltages ($V_{IL}$ and $V_{IH}$), see , *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*.

For the internal pullup and pulldown resistors for all device pins, see the peripheral-specific or system-specific terminal functions tables in Section 4.2.

## 6.4 Boot Sequence

The boot sequence is a process by which the device's memory is loaded with program and data sections, and by which some of the device's internal registers are programmed with predetermined values. The boot sequence is started automatically after each device-level global reset. For more details on device-level global resets, see Section 8.2. There are several methods by which the memory and register initialization can take place. Each of these methods is referred to as a boot mode. The boot mode to be used is selected at reset. The device is booted through multiple means—primary bootloaders within internal ROM or EMIF4, and secondary user bootloaders from peripherals or external memories. The maximum size of the boot image is 255KB (ROM uses 1KB internally). Boot modes, pin configurations, and register configurations required for booting the device, are described in the following subsections.

The following boot modes are supported:

- NOR Flash boot (muxed and non-muxed, 8-bit or 16-bit)
- NAND Flash boot (SLC and MLC with BCH ECC, 8-bit or 16-bit)
- SPI boot (EEPROM or Flash, SPI mode 3, 24-bit)
- SD boot (SD cards)
- EMAC boot (TFTP client)
- UART boot (X-modem client)
- PCIe boot (client mode, PCIe 32 and PCIe 64).

The state of the device after boot is determined by sampling the input states of the BTMODE[4:0] pins when device reset ($\overline{\text{POR}}$ or $\overline{\text{RESET}}$) is deasserted. The sampled values are latched into the CONTROL_STATUS register, which is part of the system configuration (SYSCFG) module.

The BTMODE [4:0] values determine the boot mode order according to Table 6-6. The first boot mode listed for each BTMODE[4:0] configuration is executed as the primary boot mode. If the primary boot mode fails, the second, third, and fourth boot modes are executed, in that order, until a successful boot is completed.

Additional boot configuration pins determine the following system boot settings as shown in Table 4-1:

- GPMC CS0 Default Bus Width
- GPMC Wait Enable

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- GPMC Address and Data Multiplexing.

The GPMC CS0 default operation is determined by the CS0BW, CS0WAIT, and CS0MUX[1:0] inputs.

For more detailed information on booting the device, see the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).


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**Table 6-6. Boot Mode Order**

| BTMODE[4] = 1 MEMORY BOOTING PREFERRED | | | | BTMODE[4] = 0 PERIPHERAL BOOTING PREFERRED | | | | BTMODE[3:0] |
|---|---|---|---|---|---|---|---|---|
| FIRST | SECOND | THIRD | FOURTH | FIRST | SECOND | THIRD | FOURTH | |
| XIP(1) | UART | EMAC | SD | RESERVED | RESERVED | RESERVED | RESERVED | 0000 |
| XIPWAIT(1) | UART | EMAC | SD | UART | XIPWAIT(1) | SD | SPI | 0001 |
| NAND | NANDI2C | SPI | UART | UART | SPI | NAND | NANDI2C | 0010 |
| NAND | NANDI2C | SD | UART | UART | SPI | XIP(1) | SD | 0011 |
| NAND | NANDI2C | SPI | EMAC | EMAC | SPI | NAND | NANDI2C | 0100 |
| NANDI2C | SD | EMAC | UART | RESERVED | RESERVED | RESERVED | RESERVED | 0101 |
| SPI | SD | UART | EMAC | RESERVED | RESERVED | RESERVED | RESERVED | 0110 |
| SD | SPI | UART | EMAC | EMAC | SD | SPI | XIP(1) | 0111 |
| SPI | SD | PCIE_32 | RESERVED | PCIE_32 | RESERVED | RESERVED | RESERVED | 1000 |
| SPI | SD | PCIE_64 | RESERVED | PCIE_64 | RESERVED | RESERVED | RESERVED | 1001 |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | 1010 |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | 1011 |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | 1100 |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | 1101 |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | 1110 |
| GP Fast External Boot | EMAC | UART | PCIE_32 | GP Fast External Boot | UART | EMAC | PCIE_64 | 1111 |

(1) GPMC CS0 eXecute In Place (XIP) and eXecute In Place with Wait Monitoring (XIPWAIT) boot for NOR. OneNAND, and ROM. For details, see the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### 6.4.1 Boot Mode Registers

For details on the boot mode registers, see the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

**Table 6-7. Device Boot Registers Summary**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0040 | CONTROL_STATUS | Device Status |
| 0x4814 0044 | BOOTSTAT | Device Boot Status |
| 0x4814 0048 | DSPBOOTADDR | DSP Boot Address Vector |
| 0x4814 004C - 0x4814 007C | - | Reserved |

## 6.5 Pin Multiplexing Control

Device-level pin multiplexing is controlled on a pin-by-pin basis by the MUXMODE bits of the PINCTRL1 - PINCTRL321 registers in the SYSCFG module. The default state for each multiplexed pin is MUXMODE = 0x000.

Pin multiplexing selects which of several peripheral pin functions control the pin's IO buffer output data values.

The input from each pin is routed to all of the peripherals that share the pin, regardless of the MUXMODE setting. For details, see the table below and the MUXED column in the each of the Terminal Functions tables in Section 4.2.

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### 6.5.1 PINCTRLx Register Descriptions

**Table 6-8. PINCTRLx Register Definition**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31:5 | Reserved | | Reserved; Read returns 0 |
| 4 | PULLTYPESEL | | Pad Pullup or Pulldown Type Selection |
| | | 0 | Pulldown selected |
| | | 1 | Pullup selected |
| 3 | PULLDIS | | Pad Pullup or Pulldown Disable |
| | | 0 | Pullup or Pulldown enabled |
| | | 1 | Pullup or Pulldown disabled |
| 2:0 | MUXMODE | | Pad Functional Signal Mux Select |

**Table 6-9. PINCTRLx Registers**

| HEX ADDRESS | REGISTER NAME | PULLTYPESEL | PULLDIS | MUXMODE[2:0] | | | |
|---|---|---|---|---|---|---|---|
| | | | | 000 | 001 | 010 | 011 |
| 0x4814 0800 | PINCTRL1 | 0 | 0 | | | | |
| 0x4814 0804 | PINCTRL2 | 0 | 0 | | | | |
| 0x4814 0808 | PINCTRL3 | 0 | 0 | | | | |
| 0x4814 080C | PINCTRL4 | 0 | 0 | | | | |
| 0x4814 0810 | PINCTRL5 | 0 | 0 | | | | |
| 0x4814 0814 | PINCTRL6 | 0 | 0 | | VOUT[1]_C[3] | VIN[1]A_D[9] | |
| 0x4814 0818 | PINCTRL7 | 0 | 0 | | VOUT[1]_C[4] | VIN[1]A_D[10] | |
| 0x4814 081C | PINCTRL8 | 0 | 0 | | VOUT[1]_C[5] | VIN[1]A_D[11] | |
| 0x4814 0820 | PINCTRL9 | 0 | 0 | | VOUT[1]_C[6] | VIN[1]A_D[12] | |
| 0x4814 0824 | PINCTRL10 | 0 | 0 | | VOUT[1]_C[7] | VIN[1]A_D[13] | |
| 0x4814 0828 | PINCTRL11 | 0 | 0 | | VIN[1]A_D[14] | | |
| 0x4814 082C | PINCTRL12 | 0 | 0 | | VIN[0]A_D[20] | VIN[0]B_DE | |
| 0x4814 0830 | PINCTRL13 | 0 | 0 | | VIN[0]A_D[21] | VIN[0]B_FLD | |
| 0x4814 0834 | PINCTRL14 | 0 | 0 | | VIN[0]A_D[22] | VIN[0]B_VSYNC | |
| 0x4814 0838 | PINCTRL15 | 0 | 0 | | VIN[0]A_D[23] | VIN[0]B_HSYNC | |
| 0x4814 083C | PINCTRL16 | 0 | 0 | | VOUT[1]_Y_YC[6] | VIN[1]A_D[4] | |
| 0x4814 0840 | PINCTRL17 | 0 | 0 | | VOUT[1]_Y_YC[7] | VIN[1]A_D[5] | |
| 0x4814 0844 | PINCTRL18 | 0 | 0 | | VOUT[1]_Y_YC[8] | VIN[1]A_D[6] | |
| 0x4814 0848 | PINCTRL19 | 0 | 0 | | VOUT[1]_Y_YC[9] | VIN[1]A_D[7] | |
| 0x4814 084C | PINCTRL20 | 0 | 0 | | VOUT[1]_C[2] | VIN[1]A_D[8] | |
| 0x4814 0850 | PINCTRL21 | 0 | 0 | | VOUT[1]_HSYNC (silicon revision 1.x)<br>DAC_VOUT[1]_HSYNC (silicon revision 2.x) | VIN[1]A_D[15] | |
| 0x4814 0854 | PINCTRL22 | 0 | 0 | | VIN[0]A_D[16] | VIN[1]A_HSYNC | VOUT[1]_FLD |
| 0x4814 0858 | PINCTRL23 | 0 | 0 | | VIN[0]A_D[17] | VIN[1]A_VSYNC | VOUT[1]_VSYNC (silicon revision 1.x)<br>DAC_VOUT[1]_VSYNC (silicon revision 2.x) |
| 0x4814 085C | PINCTRL24 | 0 | 0 | | VIN[0]A_D[18] | VIN[1]A_FLD | VOUT[1]_C[8] |
| 0x4814 0860 | PINCTRL25 | 0 | 0 | | VIN[0]A_D[19] | VIN[1]A_DE | VOUT[1]_C[9] |
| 0x4814 0864 | PINCTRL26 | 0 | 0 | | VOUT[0]_R_CR[0] | VOUT[1]_C[8] | VOUT[1]_CLK |
| 0x4814 0868 | PINCTRL27 | 0 | 0 | | VOUT[0]_B_CB_C[0] | VOUT[1]_C[9] | VIN[1]B_HSYNC_DE |
| 0x4814 086C | PINCTRL28 | 0 | 0 | | VOUT[0]_B_CB_C[1] | VOUT[1]_HSYNC (silicon revision 1.x)<br>DAC_VOUT[1]_HSYNC (silicon revision 2.x) | VOUT[1]_AVID |
| 0x4814 0870 | PINCTRL29 | 0 | 0 | | VOUT[0]_G_Y_YC[0] | VOUT[1]_VSYNC (silicon revision 1.x)<br>DAC_VOUT[1]_VSYNC (silicon revision 2.x) | VIN[1]B_VSYNC |
| 0x4814 0874 | PINCTRL30 | 0 | 0 | | VOUT[0]_G_Y_YC[1] | VOUT[1]_FLD | VIN[1]B_FLD |


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## Table 6-9. PINCTRLx Registers (continued)

| HEX ADDRESS | REGISTER NAME | PULLTYPESEL | PULLDIS | MUXMODE[2:0] | | | |
|---|---|---|---|---|---|---|---|
| | | | | 000 | 001 | 010 | 011 |
| 0x4814 0878 | PINCTRL31 | 0 | 0 | | VOUT[1]_AVID | VIN[1]B_CLK | |
| 0x4814 087C | PINCTRL32 | 0 | 0 | | VIN[0]A_HSYNC | | |
| 0x4814 0880 | PINCTRL33 | 0 | 0 | | VIN[0]A_VSYNC | | |
| 0x4814 0884 | PINCTRL34 | 0 | 0 | | VIN[0]A_FLD | | |
| 0x4814 0888 | PINCTRL35 | 0 | 0 | | VIN[0]A_DE | | |
| 0x4814 088C | PINCTRL36 | 0 | 0 | | VOUT[0]_HSYNC | | |
| 0x4814 0890 | PINCTRL37 | 0 | 0 | | VOUT[0]_VSYNC | | |
| 0x4814 0894 | PINCTRL38 | 0 | 0 | | VOUT[0]_FLD (silicon revision 1.x)<br>DAC_VSYNC_VOUT[0]_FLD (silicon revision 2.x) | | |
| 0x4814 0898 | PINCTRL39 | 0 | 0 | | VOUT[0]_AVID (silicon revision 1.x)<br>DAC_HSYNC_VOUT[0]_AVID (silicon revision 2.x) | | |
| 0x4814 089C | PINCTRL40 | 0 | 0 | | VOUT[0]_R_CR[1] | | |
| 0x4814 08A0 | PINCTRL41 | 0 | 1 | | | | |
| 0x4814 08A4 | PINCTRL42 | 0 | 1 | | | | |
| 0x4814 08A8 | PINCTRL43 | 0 | 1 | | | | |
| 0x4814 08AC | PINCTRL44 | 0 | 1 | | | | |
| 0x4814 08B0 | PINCTRL45 | 0 | 1 | | | | |
| 0x4814 08B4 | PINCTRL46 | 0 | 1 | | VOUT[1]_CLK | VIN[1]A_CLK | |
| 0x4814 08B8 | PINCTRL47 | 0 | 1 | | VOUT[1]_Y_YC[2] | VIN[1]A_D[0] | |
| 0x4814 08BC | PINCTRL48 | 0 | 1 | | VOUT[1]_Y_YC[3] | VIN[1]A_D[1] | |
| 0x4814 08C0 | PINCTRL49 | 0 | 1 | | VOUT[1]_Y_YC[4] | VIN[1]A_D[2] | |
| 0x4814 08C4 | PINCTRL50 | 0 | 1 | | VOUT[1]_Y_YC[5] | VIN[1]A_D[3] | |
| 0x4814 08C8 | PINCTRL51 | 0 | 0 | | EMAC[1]_RXCLK | | |
| 0x4814 08CC | PINCTRL52 | 0 | 0 | | EMAC[1]_RXD[0] | | |
| 0x4814 08D0 | PINCTRL53 | 0 | 0 | | EMAC[1]_RXD[1] | | |
| 0x4814 08D4 | PINCTRL54 | 0 | 0 | | EMAC[1]_RXD[2] | | |
| 0x4814 08D8 | PINCTRL55 | 0 | 0 | | EMAC[1]_RXD[3] | | |
| 0x4814 08DC | PINCTRL56 | 0 | 0 | | EMAC[1]_RXD[4] | | |
| 0x4814 08E0 | PINCTRL57 | 0 | 0 | | EMAC[1]_RXD[5] | | |
| 0x4814 08E4 | PINCTRL58 | 0 | 0 | | EMAC[1]_RXD[6] | | |
| 0x4814 08E8 | PINCTRL59 | 0 | 0 | | EMAC[1]_RXD[7] | | |
| 0x4814 08EC | PINCTRL60 | 0 | 0 | | EMAC[1]_RXDV | | |
| 0x4814 08F0 | PINCTRL61 | 0 | 1 | | EMAC[1]_GMTCLK | | |
| 0x4814 08F4 | PINCTRL62 | 0 | 1 | | EMAC[1]_TXD[0] | | |
| 0x4814 08F8 | PINCTRL63 | 0 | 1 | | EMAC[1]_TXD[1] | | |
| 0x4814 08FC | PINCTRL64 | 0 | 1 | | EMAC[1]_TXD[2] | | |
| 0x4814 0900 | PINCTRL65 | 0 | 1 | | EMAC[1]_TXD[3] | | |
| 0x4814 0904 | PINCTRL66 | 0 | 1 | | EMAC[1]_TXD[4] | | |
| 0x4814 0908 | PINCTRL67 | 0 | 1 | | EMAC[1]_TXD[5] | | |
| 0x4814 090C | PINCTRL68 | 0 | 1 | | EMAC[1]_TXD[6] | | |
| 0x4814 0910 | PINCTRL69 | 0 | 1 | | EMAC[1]_TXD[7] | | |
| 0x4814 0914 | PINCTRL70 | 0 | 1 | | EMAC[1]_TXEN | | |
| 0x4814 0918 | PINCTRL71 | 0 | 1 | | EMAC[1]_TXCLK | | |
| 0x4814 091C | PINCTRL72 | 0 | 1 | | EMAC[1]_COL | | |
| 0x4814 0920 | PINCTRL73 | 0 | 0 | | EMAC[1]_CRS | | |
| 0x4814 0924 | PINCTRL74 | 0 | 1 | | EMAC[1]_RXER | | |
| 0x4814 0928 | PINCTRL75 | 0 | 0 | | | | |
| 0x4814 092C | PINCTRL76 | 0 | 0 | | | | |
| 0x4814 0930 | PINCTRL77 | 0 | 0 | | | | |
| 0x4814 0934 | PINCTRL78 | 0 | 0 | | | | |
| 0x4814 0938 | PINCTRL79 | 0 | 0 | | | | |

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## Table 6-9. PINCTRLx Registers (continued)

| HEX ADDRESS | REGISTER NAME | PULLTYPESEL | PULLDIS | MUXMODE[2:0] | | | |
|---|---|---|---|---|---|---|---|
| | | | | 000 | 001 | 010 | 011 |
| 0x4814 093C | PINCTRL80 | 0 | 1 | | | | |
| 0x4814 0940 | PINCTRL81 | 0 | 1 | | | | |
| 0x4814 0944 | PINCTRL82 | 0 | 1 | | | | |
| 0x4814 0948 | PINCTRL83 | 0 | 0 | VIN[0]A_CLK | | | |
| 0x4814 094C | PINCTRL84 | 0 | 0 | VIN[0]B_CLK | | | |
| 0x4814 0950 | PINCTRL85 | 0 | 0 | VIN[0]A_D[0] | | | |
| 0x4814 0954 | PINCTRL86 | 0 | 0 | VIN[0]A_D[1] | | | |
| 0x4814 0958 | PINCTRL87 | 0 | 0 | VIN[0]A_D[2] | | | |
| 0x4814 095C | PINCTRL88 | 0 | 0 | VIN[0]A_D[3] | | | |
| 0x4814 0960 | PINCTRL89 | 0 | 0 | VIN[0]A_D[4] | | | |
| 0x4814 0964 | PINCTRL90 | 0 | 0 | VIN[0]A_D[5] | | | |
| 0x4814 0968 | PINCTRL91 | 0 | 0 | VIN[0]A_D[6] | | | |
| 0x4814 096C | PINCTRL92 | 0 | 0 | VIN[0]A_D[7] | | | |
| 0x4814 0970 | PINCTRL93 | 0 | 0 | VIN[0]A_D[8] | | | |
| 0x4814 0974 | PINCTRL94 | 0 | 0 | VIN[0]A_D[9] | | | |
| 0x4814 0978 | PINCTRL95 | 0 | 0 | VIN[0]A_D[10] | | | |
| 0x4814 097C | PINCTRL96 | 0 | 0 | VIN[0]A_D[11] | | | |
| 0x4814 0980 | PINCTRL97 | 0 | 0 | VIN[0]A_D[12] | | | |
| 0x4814 0984 | PINCTRL98 | 0 | 0 | VIN[0]A_D[13] | | | |
| 0x4814 0988 | PINCTRL99 | 0 | 0 | VIN[0]A_D[14] | | | |
| 0x4814 098C | PINCTRL100 | 0 | 0 | VIN[0]A_D[15] | | | |
| 0x4814 0990 | PINCTRL101 | 0 | 1 | VOUT[0]_CLK | | | |
| 0x4814 0994 | PINCTRL102 | 0 | 1 | VOUT[0]_G_Y_YC[2] | | | |
| 0x4814 0998 | PINCTRL103 | 0 | 1 | VOUT[0]_G_Y_YC[3] | | | |
| 0x4814 099C | PINCTRL104 | 0 | 1 | VOUT[0]_G_Y_YC[4] | | | |
| 0x4814 09A0 | PINCTRL105 | 0 | 1 | VOUT[0]_G_Y_YC[5] | | | |
| 0x4814 09A4 | PINCTRL106 | 0 | 1 | VOUT[0]_G_Y_YC[6] | | | |
| 0x4814 09A8 | PINCTRL107 | 0 | 1 | VOUT[0]_G_Y_YC[7] | | | |
| 0x4814 09AC | PINCTRL108 | 0 | 1 | VOUT[0]_G_Y_YC[8] | | | |
| 0x4814 09B0 | PINCTRL109 | 0 | 1 | VOUT[0]_G_Y_YC[9] | | | |
| 0x4814 09B4 | PINCTRL110 | 0 | 1 | VOUT[0]_B_CB_C[2] | | | |
| 0x4814 09B8 | PINCTRL111 | 0 | 1 | VOUT[0]_B_CB_C[3] | | | |
| 0x4814 09BC | PINCTRL112 | 0 | 1 | VOUT[0]_B_CB_C[4] | | | |
| 0x4814 09C0 | PINCTRL113 | 0 | 1 | VOUT[0]_B_CB_C[5] | | | |
| 0x4814 09C4 | PINCTRL114 | 0 | 1 | VOUT[0]_B_CB_C[6] | | | |
| 0x4814 09C8 | PINCTRL115 | 0 | 1 | VOUT[0]_B_CB_C[7] | | | |
| 0x4814 09CC | PINCTRL116 | 0 | 1 | VOUT[0]_B_CB_C[8] | | | |
| 0x4814 09D0 | PINCTRL117 | 0 | 1 | VOUT[0]_B_CB_C[9] | | | |
| 0x4814 09D4 | PINCTRL118 | 0 | 1 | VOUT[0]_R_CR[2] | VOUT[0]_HSYNC | VOUT[1]_Y_YC[2] | |
| 0x4814 09D8 | PINCTRL119 | 0 | 1 | VOUT[0]_R_CR[3] | VOUT[0]_VSYNC | VOUT[1]_Y_YC[3] | |
| 0x4814 09DC | PINCTRL120 | 0 | 1 | VOUT[0]_R_CR[4] | VOUT[0]_FLD | VOUT[1]_Y_YC[4] | |
| 0x4814 09E0 | PINCTRL121 | 0 | 1 | VOUT[0]_R_CR[5] | VOUT[0]_AVID | VOUT[1]_Y_YC[5] | |
| 0x4814 09E4 | PINCTRL122 | 0 | 1 | VOUT[0]_R_CR[6] | VOUT[0]_G_Y_YC[0] | VOUT[1]_Y_YC[6] | |
| 0x4814 09E8 | PINCTRL123 | 0 | 1 | VOUT[0]_R_CR[7] | VOUT[0]_G_Y_YC[1] | VOUT[1]_Y_YC[7] | |
| 0x4814 09EC | PINCTRL124 | 0 | 1 | VOUT[0]_R_CR[8] | VOUT[0]_B_CB_C[0] | VOUT[1]_Y_YC[8] | |
| 0x4814 09F0 | PINCTRL125 | 0 | 1 | VOUT[0]_R_CR[9] | VOUT[0]_B_CB_C[1] | VOUT[1]_Y_YC[9] | |
| 0x4814 09F4 | PINCTRL126 | 0 | 0 | MCA[0]_ACLKR | | | |
| 0x4814 09F8 | PINCTRL127 | 0 | 0 | MCA[0]_AHCLKR | | | |
| 0x4814 09FC | PINCTRL128 | 0 | 0 | MCA[0]_AFSR | | | |
| 0x4814 0A00 | PINCTRL129 | 0 | 0 | MCA[0]_ACLKX | | | |
| 0x4814 0A04 | PINCTRL130 | 0 | 0 | MCA[0]_ACLKHX | | | |
| 0x4814 0A08 | PINCTRL131 | 0 | 0 | MCA[0]_AFSX | | | |
| 0x4814 0A0C | PINCTRL132 | 0 | 0 | MCA[0]_AMUTE | | | |
| 0x4814 0A10 | PINCTRL133 | 0 | 0 | MCA[0]_AXR[0] | | | |
| 0x4814 0A14 | PINCTRL134 | 0 | 0 | MCA[0]_AXR[1] | | | |


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**Table 6-9. PINCTRLx Registers (continued)**

| HEX ADDRESS | REGISTER NAME | PULLTYPESEL | PULLDIS | MUXMODE[2:0] | | | |
|---|---|---|---|---|---|---|---|
| | | | | 000 | 001 | 010 | 011 |
| 0x4814 0A18 | PINCTRL135 | 0 | 0 | MCA[0]_AXR[2] | MCB_FSX | | |
| 0x4814 0A1C | PINCTRL136 | 0 | 0 | MCA[0]_AXR[3] | MCB_FSR | | |
| 0x4814 0A20 | PINCTRL137 | 0 | 0 | MCA[0]_AXR[4] | MCB_DX | | |
| 0x4814 0A24 | PINCTRL138 | 0 | 0 | MCA[0]_AXR[5] | MCB_DR | | |
| 0x4814 0A28 | PINCTRL139 | 0 | 0 | MCA[1]_ACLKR | | | |
| 0x4814 0A2C | PINCTRL140 | 0 | 0 | MCA[1]_AHCLKR | | | |
| 0x4814 0A30 | PINCTRL141 | 0 | 0 | MCA[1]_AFSR | | | |
| 0x4814 0A34 | PINCTRL142 | 0 | 0 | MCA[1]_ACLKX | | | |
| 0x4814 0A38 | PINCTRL143 | 0 | 0 | MCA[1]_ACLKHX | | | |
| 0x4814 0A3C | PINCTRL144 | 0 | 0 | MCA[1]_AFSX | | | |
| 0x4814 0A40 | PINCTRL145 | 0 | 0 | MCA[1]_AMUTE | | | |
| 0x4814 0A44 | PINCTRL146 | 0 | 0 | MCA[1]_AXR[0] | | | |
| 0x4814 0A48 | PINCTRL147 | 0 | 0 | MCA[1]_AXR[1] | | | |
| 0x4814 0A4C | PINCTRL148 | 0 | 0 | MCA[2]_ACLKR | MCB_CLKR | MCB_DR | |
| 0x4814 0A50 | PINCTRL149 | 0 | 0 | MCA[2]_AHCLKR | MCB_CLKS | | |
| 0x4814 0A54 | PINCTRL150 | 0 | 0 | MCA[2]_AFSR | MCB_CLKX | MCB_FSR | |
| 0x4814 0A58 | PINCTRL151 | 0 | 0 | MCA[2]_ACLKX | MCB_CLKX | | |
| 0x4814 0A5C | PINCTRL152 | 0 | 0 | MCA[2]_ACLKHX | MCB_CLKR | | |
| 0x4814 0A60 | PINCTRL153 | 0 | 0 | MCA[2]_AFSX | MCB_CLKS | MCB_FSX | |
| 0x4814 0A64 | PINCTRL154 | 0 | 0 | MCA[2]_AMUTE | | | |
| 0x4814 0A68 | PINCTRL155 | 0 | 0 | MCA[2]_AXR[0] | | | |
| 0x4814 0A6C | PINCTRL156 | 0 | 0 | MCA[2]_AXR[1] | MCB_DX | | |
| 0x4814 0A70 | PINCTRL157 | 0 | 1 | SD_POW | GPMC_A[14] | GP1[0] | |
| 0x4814 0A74 | PINCTRL158 | 0 | 1 | SD_CLK | GPMC_A[13] | GP1[1] | |
| 0x4814 0A78 | PINCTRL159 | 0 | 1 | SD_CMD | GPMC_A[21] | GP1[2] | |
| 0x4814 0A7C | PINCTRL160 | 0 | 0 | SD_DAT[0] | GPMC_A[20] | GP1[3] | |
| 0x4814 0A80 | PINCTRL161 | 0 | 0 | SD_DAT[1]_SDIRQ | GPMC_A[19] | GP1[4] | |
| 0x4814 0A84 | PINCTRL162 | 0 | 0 | SD_DAT[2]_SDRW | GPMC_A[18] | GP1[5] | |
| 0x4814 0A88 | PINCTRL163 | 0 | 0 | SD_DAT[3] | GPMC_A[17] | GP1[6] | |
| 0x4814 0A8C | PINCTRL164 | 0 | 0 | SD_SDCD | GPMC_A[16] | GP1[7] | |
| 0x4814 0A90 | PINCTRL165 | 0 | 0 | SD_SDWP | GPMC_A[15] | GP1[8] | |
| 0x4814 0A94 | PINCTRL166 | 0 | 0 | SPI_SCLK | | | |
| 0x4814 0A98 | PINCTRL167 | 1 | 0 | SPI_SCS[0] | | | |
| 0x4814 0A9C | PINCTRL168 | 1 | 0 | SPI_SCS[1] | GPMC_A[23] | | |
| 0x4814 0AA0 | PINCTRL169 | 1 | 0 | SPI_SCS[2] | GPMC_A[22] | | |
| 0x4814 0AA4 | PINCTRL170 | 1 | 0 | SPI_SCS[3] | GPMC_A[21] | GP1[22] | |
| 0x4814 0AA8 | PINCTRL171 | 0 | 0 | SPI_D[0] | | | |
| 0x4814 0AAC | PINCTRL172 | 0 | 0 | SPI_D[1] | | | |
| 0x4814 0AB0 | PINCTRL173 | 0 | 0 | UART0_RXD | | | |
| 0x4814 0AB4 | PINCTRL174 | 0 | 1 | UART0_TXD | | | |
| 0x4814 0AB8 | PINCTRL175 | 1 | 1 | $\overline{\text{UART0_RTS}}$ | GP1[27] | | |
| 0x4814 0ABC | PINCTRL176 | 1 | 0 | $\overline{\text{UART0_CTS}}$ | GP1[28] | | |
| 0x4814 0AC0 | PINCTRL177 | 1 | 1 | $\overline{\text{UART0_DTR}}$ | GPMC_A[20] | GPMC_A[12] | GP1[16] |
| 0x4814 0AC4 | PINCTRL178 | 1 | 0 | $\overline{\text{UART0_DSR}}$ | GPMC_A[19] | GPMC_A[24] | GP1[17] |
| 0x4814 0AC8 | PINCTRL179 | 1 | 0 | $\overline{\text{UART0_DCD}}$ | GPMC_A[18] | GPMC_A[23] | GP1[18] |
| 0x4814 0ACC | PINCTRL180 | 1 | 0 | UART0_RIN | GPMC_A[17] | GPMC_A[22] | GP1[19] |
| 0x4814 0AD0 | PINCTRL181 | 0 | 0 | UART1_RXD | GPMC_A[26] | GPMC_A[20] | |
| 0x4814 0AD4 | PINCTRL182 | 0 | 1 | UART1_TXD | GPMC_A[25] | GPMC_A[19] | |
| 0x4814 0AD8 | PINCTRL183 | 1 | 1 | $\overline{\text{UART1_RTS}}$ | GPMC_A[14] | GPMC_A[18] | GP1[25] |
| 0x4814 0ADC | PINCTRL184 | 1 | 0 | $\overline{\text{UART1_CTS}}$ | GPMC_A[13] | GPMC_A[17] | GP1[26] |
| 0x4814 0AE0 | PINCTRL185 | 0 | 0 | UART2_RXD | | | |
| 0x4814 0AE4 | PINCTRL186 | 0 | 0 | UART2_TXD | | | |
| 0x4814 0AE8 | PINCTRL187 | 1 | 1 | $\overline{\text{UART2_RTS}}$ | GPMC_A[15] | GPMC_A[26] | GP1[23] |
| 0x4814 0AEC | PINCTRL188 | 1 | 0 | $\overline{\text{UART2_CTS}}$ | GPMC_A[16] | GPMC_A[25] | GP1[24] |
| 0x4814 0AF0 | PINCTRL189 | 0 | 0 | | GPMC_A[27] | GP1[9] | |

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## Table 6-9. PINCTRLx Registers (continued)

| HEX ADDRESS | REGISTER NAME | PULLTYPESEL | PULLDIS | MUXMODE[2:0] | | | |
|---|---|---|---|---|---|---|---|
| | | | | 000 | 001 | 010 | 011 |
| 0x4814 0AF4 | PINCTRL190 | 0 | 1 | | GPMC_A[22] | GP1[10] | |
| 0x4814 0AF8 | PINCTRL191 | 0 | 1 | | GPMC_A[26] | GP1[11] | |
| 0x4814 0AFC | PINCTRL192 | 0 | 0 | | GPMC_A[25] | GP1[12] | |
| 0x4814 0B00 | PINCTRL193 | 0 | 1 | | GP1[13] | | |
| 0x4814 0B04 | PINCTRL194 | 0 | 1 | | GPMC_A[23] | GP1[14] | |
| 0x4814 0B08 | PINCTRL195 | 0 | 1 | | GPMC_A[24] | GP1[15] | |
| 0x4814 0B0C | PINCTRL196 | 0 | 0 | | GPMC_A[16] | GP0[21] | |
| 0x4814 0B10 | PINCTRL197 | 0 | 1 | | GPMC_A[15] | GP0[22] | |
| 0x4814 0B14 | PINCTRL198 | 0 | 1 | | GPMC_A[14] | GP0[23] | |
| 0x4814 0B18 | PINCTRL199 | 0 | 0 | | GPMC_A[13] | GP0[24] | |
| 0x4814 0B1C | PINCTRL200 | 0 | 1 | | GP0[25] | | |
| 0x4814 0B20 | PINCTRL201 | 0 | 1 | | GPMC_A[21] | GP0[26] | |
| 0x4814 0B24 | PINCTRL202 | 0 | 1 | | GPMC_A[12] | GP0[27] | |
| 0x4814 0B28 | PINCTRL203 | 0 | 0 | TIM4_OUT | GP0[28] | | |
| 0x4814 0B2C | PINCTRL204 | 0 | 0 | TIM5_OUT | GP0[29] | | |
| 0x4814 0B30 | PINCTRL205 | 0 | 0 | TIM6_OUT | GPMC_A[24] | GP0[30] | |
| 0x4814 0B34 | PINCTRL206 | 0 | 0 | TIM7_OUT | GPMC_A[12] | GP0[31] | |
| 0x4814 0B38 | PINCTRL207 | 1 | 0 | $\overline{\text{GPMC_CS[0]}}$ | | | |
| 0x4814 0B3C | PINCTRL208 | 1 | 0 | $\overline{\text{GPMC_CS[1]}}$ | | | |
| 0x4814 0B40 | PINCTRL209 | 1 | 0 | $\overline{\text{GPMC_CS[2]}}$ | | | |
| 0x4814 0B44 | PINCTRL210 | 1 | 0 | $\overline{\text{GPMC_CS[3]}}$ | | | |
| 0x4814 0B48 | PINCTRL211 | 1 | 0 | $\overline{\text{GPMC_CS[4]}}$ | GP1[21] | | |
| 0x4814 0B4C | PINCTRL212 | 1 | 0 | $\overline{\text{GPMC_CS[5]}}$ | GPMC_A[12] | | |
| 0x4814 0B50 | PINCTRL213 | 1 | 0 | GPMC_$\overline{\text{WE}}$ | | | |
| 0x4814 0B54 | PINCTRL214 | 1 | 1 | $\overline{\text{GPMC_OE_RE}}$ | | | |
| 0x4814 0B58 | PINCTRL215 | 0 | 1 | GPMC_$\overline{\text{BE0}}$_CLE | | | |
| 0x4814 0B5C | PINCTRL216 | 0 | 1 | $\overline{\text{GPMC_BE1}}$ | | | |
| 0x4814 0B60 | PINCTRL217 | 0 | 1 | GPMC_$\overline{\text{ADV}}$_ALE | | | |
| 0x4814 0B64 | PINCTRL218 | 0 | 1 | GPMC_DIR | GP1[20] | | |
| 0x4814 0B68 | PINCTRL219 | 0 | 0 | $\overline{\text{GPMC_WP}}$ | | | |
| 0x4814 0B6C | PINCTRL220 | 0 | 0 | GPMC_WAIT | | | |
| 0x4814 0B70 | PINCTRL221 | 0 | 1 | GPMC_A[0] | GP0[8] | | |
| 0x4814 0B74 | PINCTRL222 | 0 | 1 | GPMC_A[1] | GP0[9] | | |
| 0x4814 0B78 | PINCTRL223 | 0 | 1 | GPMC_A[2] | GP0[10] | | |
| 0x4814 0B7C | PINCTRL224 | 0 | 1 | GPMC_A[3] | GP0[11] | | |
| 0x4814 0B80 | PINCTRL225 | 0 | 1 | GPMC_A[4] | GP0[12] | | |
| 0x4814 0B84 | PINCTRL226 | 0 | 1 | GPMC_A[5] | GP0[13] | | |
| 0x4814 0B88 | PINCTRL227 | 0 | 1 | GPMC_A[6] | GP0[14] | | |
| 0x4814 0B8C | PINCTRL228 | 0 | 1 | GPMC_A[7] | GP0[15] | | |
| 0x4814 0B90 | PINCTRL229 | 0 | 1 | GPMC_A[8] | GP0[16] | | |
| 0x4814 0B94 | PINCTRL230 | 0 | 1 | GPMC_A[9] | GP0[17] | | |
| 0x4814 0B98 | PINCTRL231 | 0 | 1 | GPMC_A[10] | GP0[18] | | |
| 0x4814 0B9C | PINCTRL232 | 0 | 1 | GPMC_A[11] | GP0[19] | | |
| 0x4814 0BA0 | PINCTRL233 | 0 | 1 | GPMC_A[27] | GP0[20] | | |
| 0x4814 0BA4 | PINCTRL234 | 0 | 0 | GPMC_D[0] | | | |
| 0x4814 0BA8 | PINCTRL235 | 0 | 0 | GPMC_D[1] | | | |
| 0x4814 0BAC | PINCTRL236 | 0 | 0 | GPMC_D[2] | | | |
| 0x4814 0BB0 | PINCTRL237 | 0 | 0 | GPMC_D[3] | | | |
| 0x4814 0BB4 | PINCTRL238 | 0 | 0 | GPMC_D[4] | | | |
| 0x4814 0BB8 | PINCTRL239 | 0 | 0 | GPMC_D[5] | | | |
| 0x4814 0BBC | PINCTRL240 | 0 | 0 | GPMC_D[6] | | | |
| 0x4814 0BC0 | PINCTRL241 | 0 | 0 | GPMC_D[7] | | | |
| 0x4814 0BC4 | PINCTRL242 | 0 | 0 | GPMC_D[8] | | | |
| 0x4814 0BC8 | PINCTRL243 | 0 | 0 | GPMC_D[9] | | | |
| 0x4814 0BCC | PINCTRL244 | 0 | 0 | GPMC_D[10] | | | |


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**Table 6-9. PINCTRLx Registers (continued)**

| HEX ADDRESS | REGISTER NAME | PULLTYPESEL | PULLDIS | MUXMODE[2:0] | | | |
|---|---|---|---|---|---|---|---|
| | | | | 000 | 001 | 010 | 011 |
| 0x4814 0BD0 | PINCTRL245 | 0 | 0 | GPMC_D[11] | | | |
| 0x4814 0BD4 | PINCTRL246 | 0 | 0 | GPMC_D[12] | | | |
| 0x4814 0BD8 | PINCTRL247 | 0 | 0 | GPMC_D[13] | | | |
| 0x4814 0BDC | PINCTRL248 | 0 | 0 | GPMC_D[14] | | | |
| 0x4814 0BE0 | PINCTRL249 | 0 | 0 | GPMC_D[15] | | | |
| 0x4814 0BE4 | PINCTRL250 | 0 | 1 | GPMC_CLK | GP1[29] | | |
| 0x4814 0BE8 | PINCTRL251 | 0 | 0 | EMAC[0]_COL | | | |
| 0x4814 0BEC | PINCTRL252 | 0 | 0 | EMAC[0]_CRS | | | |
| 0x4814 0BF0 | PINCTRL253 | 0 | 1 | EMAC[0]_GMTCLK | | | |
| 0x4814 0BF4 | PINCTRL254 | 1 | 0 | EMAC[0]_RXCLK | | | |
| 0x4814 0BF8 | PINCTRL255 | 1 | 0 | EMAC[0]_RXD[0] | | | |
| 0x4814 0BFC | PINCTRL256 | 1 | 0 | EMAC[0]_RXD[1] | | | |
| 0x4814 0C00 | PINCTRL257 | 1 | 0 | EMAC[0]_RXD[2] | | | |
| 0x4814 0C04 | PINCTRL258 | 1 | 0 | EMAC[0]_RXD[3] | | | |
| 0x4814 0C08 | PINCTRL259 | 1 | 0 | EMAC[0]_RXD[4] | | | |
| 0x4814 0C0C | PINCTRL260 | 1 | 0 | EMAC[0]_RXD[5] | | | |
| 0x4814 0C10 | PINCTRL261 | 1 | 0 | EMAC[0]_RXD[6] | | | |
| 0x4814 0C14 | PINCTRL262 | 1 | 0 | EMAC[0]_RXD[7] | | | |
| 0x4814 0C18 | PINCTRL263 | 1 | 0 | EMAC[0]_RXDV | | | |
| 0x4814 0C1C | PINCTRL264 | 1 | 0 | EMAC[0]_RXER | | | |
| 0x4814 0C20 | PINCTRL265 | 0 | 1 | EMAC[0]_TXCLK | | | |
| 0x4814 0C24 | PINCTRL266 | 0 | 1 | EMAC[0]_TXD[0] | | | |
| 0x4814 0C28 | PINCTRL267 | 0 | 1 | EMAC[0]_TXD[1] | | | |
| 0x4814 0C2C | PINCTRL268 | 0 | 1 | EMAC[0]_TXD[2] | | | |
| 0x4814 0C30 | PINCTRL269 | 0 | 1 | EMAC[0]_TXD[3] | | | |
| 0x4814 0C34 | PINCTRL270 | 0 | 1 | EMAC[0]_TXD[4] | | | |
| 0x4814 0C38 | PINCTRL271 | 0 | 1 | EMAC[0]_TXD[5] | | | |
| 0x4814 0C3C | PINCTRL272 | 0 | 1 | EMAC[0]_TXD[6] | | | |
| 0x4814 0C40 | PINCTRL273 | 0 | 1 | EMAC[0]_TXD[7] | | | |
| 0x4814 0C44 | PINCTRL274 | 0 | 1 | EMAC[0]_TXEN | | | |
| 0x4814 0C48 | PINCTRL275 | 1 | 0 | MDIO_MCLK | | | |
| 0x4814 0C4C | PINCTRL276 | 1 | 0 | MDIO_MDIO | | | |
| 0x4814 0C50 | PINCTRL277 | 1 | 0 | | | | |
| 0x4814 0C54 | PINCTRL278 | 1 | 0 | | | | |
| 0x4814 0C58 | PINCTRL279 | 0 | 1 | | | | |
| 0x4814 0C5C | PINCTRL280 | 0 | 1 | | | | |
| 0x4814 0C60 | PINCTRL281 | 0 | 1 | | | | |
| 0x4814 0C64 | PINCTRL282 | 0 | 1 | | | | |
| 0x4814 0C68 | PINCTRL283 | 0 | 0 | | | | |
| 0x4814 0C6C | PINCTRL284 | 0 | 0 | | | | |
| 0x4814 0C70 | PINCTRL285 | 0 | 0 | | | | |
| 0x4814 0C74 | PINCTRL286 | 0 | 0 | | | | |
| 0x4814 0C78 | PINCTRL287 | 1 | 1 | I2C[0]_SCL | | | |
| 0x4814 0C7C | PINCTRL288 | 1 | 1 | I2C[0]_SDA | | | |
| 0x4814 0C80 | PINCTRL289 | 1 | 1 | I2C[1]_SCL | | | |
| 0x4814 0C84 | PINCTRL290 | 1 | 1 | I2C[1]_SDA | | | |
| 0x4814 0C88 | PINCTRL291 | 0 | 0 | GP0[0] | | | |
| 0x4814 0C8C | PINCTRL292 | 0 | 0 | GP0[1] | | | |
| 0x4814 0C90 | PINCTRL293 | 0 | 0 | GP0[2] | | | |
| 0x4814 0C94 | PINCTRL294 | 0 | 0 | GP0[3] | TCLKIN | | |
| 0x4814 0C98 | PINCTRL295 | 0 | 0 | GP0[4] | | | |
| 0x4814 0C9C | PINCTRL296 | 0 | 0 | GP0[5] | MCA[2]_AMUTEIN | GPMC_A[24] | |
| 0x4814 0CA0 | PINCTRL297 | 0 | 0 | GP0[6] | MCA[1]_AMUTEIN | GPMC_A[23] | |
| 0x4814 0CA4 | PINCTRL298 | 0 | 0 | GP0[7] | MCA[0]_AMUTEIN | | |

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**Table 6-9. PINCTRLx Registers (continued)**

| HEX ADDRESS | REGISTER NAME | PULLTYPESEL | PULLDIS | MUXMODE[2:0] | | | |
|---|---|---|---|---|---|---|---|
| | | | | 000 | 001 | 010 | 011 |
| 0x4814 0CA8 | PINCTRL299 | 0 | 0 | GP1[30] | SATA_ACT0_LED (silicon revision 1.x)<br>SATA_ACT1_LED (silicon revision 2.x) | | |
| 0x4814 0CAC | PINCTRL300 | 0 | 0 | GP1[31] | SATA_ACT1_LED (silicon revision 1.x)<br>SATA_ACT0_LED (silicon revision 2.x) | | |
| 0x4814 0CB0 | PINCTRL301 | 0 | 1 | HDMI_SCL | | | |
| 0x4814 0CB4 | PINCTRL302 | 0 | 1 | HDMI_SDA | | | |
| 0x4814 0CB8 | PINCTRL303 | 1 | 0 | HDMI_CEC | | | |
| 0x4814 0CBC | PINCTRL304 | 0 | 0 | HDMI_HPDET | | | |
| 0x4814 0CC0 | PINCTRL305 | 1 | 0 | TCLK | | | |
| 0x4814 0CC4 | PINCTRL306 | 0 | 1 | RTCK | | | |
| 0x4814 0CC8 | PINCTRL307 | 1 | 0 | TDI | | | |
| 0x4814 0CCC | PINCTRL308 | 0 | 1 | TDO | | | |
| 0x4814 0CD0 | PINCTRL309 | 1 | 0 | TMS | | | |
| 0x4814 0CD4 | PINCTRL310 | 0 | 0 | $\overline{\text{TRST}}$ | | | |
| 0x4814 0CD8 | PINCTRL311 | 1 | 0 | EMU0 | | | |
| 0x4814 0CDC | PINCTRL312 | 1 | 0 | EMU1 | | | |
| 0x4814 0CE0 | PINCTRL313 | 1 | 0 | EMU2 | | | |
| 0x4814 0CE4 | PINCTRL314 | 1 | 0 | EMU3 | | | |
| 0x4814 0CE8 | PINCTRL315 | 1 | 0 | EMU4 | | | |
| 0x4814 0CEC | PINCTRL316 | 1 | 0 | $\overline{\text{RESET}}$ | | | |
| 0x4814 0CF0 | PINCTRL317 | 1 | 0 | $\overline{\text{NMI}}$ | | | |
| 0x4814 0CF4 | PINCTRL318 | 1 | 0 | $\overline{\text{RSTOUT}}$ | | | |
| 0x4814 0CF8 | PINCTRL319 | 1 | 0 | WD_OUT | | | |
| 0x4814 0CFC | PINCTRL320 | 0 | 1 | CLKOUT | | | |
| 0x4814 0D00 | PINCTRL321 | 0 | 0 | CLKIN32 | | | |
| 0x4814 0D04 | PINCTRL322 | 0 | 0 | USB0_DRVVBUS | | | |
| 0x4814 0D08 | PINCTRL323 | 0 | 0 | USB1_DRVVBUS | | | |
| 0x4814 0D0C - 0x4814 0FFF | Reserved | | | | | | |

## 6.6 How to Handle Unused Pins

When device signal pins are unused in the system, they can be left unconnected unless otherwise instructed in the Terminal Functions tables. For unused input pins, the internal pull resistor should be enabled, or an external pull resistor should be used, to prevent floating inputs. All supply pins must always be connected to the correct voltage, even when their associated signal pins are unused, as instructed in the Terminal Functions tables in Section 4.2.


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# 7 System Interconnect

The L3 interconnect allows the sharing of resources, such as peripherals and external or on-chip memories, between all the initiators of the platform. The L4 interconnects control access to the peripherals.

Transfers between initiators and targets across the platform are physically conditioned by the chip interconnect.

## 7.1 L3 Interconnect

The L3 topology is driven by performance requirements, bus types, and clocking structure. Figure 7-1 shows the interconnect of the device and the main modules and subsystems in the platform. Arrows indicate the master-and-slave relationship, not data flow. Master-and-slave connectivity is shown in Table 7-1.

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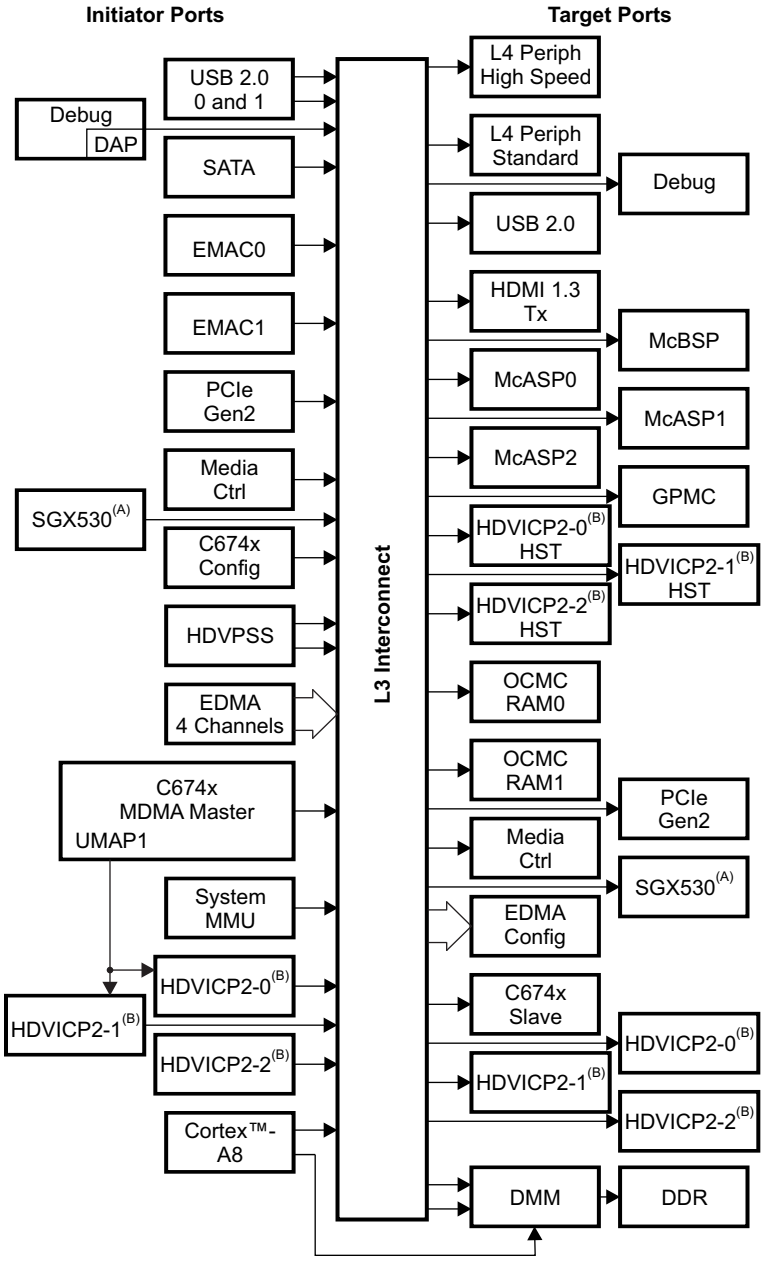


A. SGX530 is available only on the DM8168 device.

B. Three HDVICP2 modules are available on the DM8168 and DM8167 devices; two HDVICP2 modules (HDVICP2-0 and HDVICP2-1) are available on the DM8165 devices.

**Figure 7-1. Interconnect Overview**


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**Table 7-1. L3 Master-and-Slave Connectivity(1)(2)(3)**

| MASTERS | SLAVES | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYSTEM MMU | DMM TILER0 | DMM TILER1 | DMM ELLA | GPMC | SGX530 | C674x_SDMA | PCIe GEN2 SLAVE | McASPs | McBSP | HDMI 1.3 TX AUDIO | L4 HS PERIPH PORT 0 | L4 HS PERIPH PORT 1 | L4 STD PERIPH PORT 0 | L4 STD PERIPH PORT 1 | EDMA TPTC0 - 3 CFG | EDMA TPCC | OCMC RAM0 AND RAM1 | USB2.0 CFG |
| **ARM Cortex-A8 M1 (128-bit)** | | | | X | | | | | | | | | | | | | | | |
| **ARM Cortex-A8 M2 (64-bit)** | | | X | | X | X | X | X | X | X | X | X | | X | | X | X | X | X |
| **C674x MDMA** | X | | | | | | | | | | | | | | | | | | |
| **System MMU** | | | X | | | | | | | | | | | X | | | X | X | |
| **C674x CFG** | | | | | | | | | | | | | | X | | | X | | |
| **HDVICP2-0 VDMA** | | X | | | | | | | | | | | | | | | | X | |
| **HDVICP2-1 VDMA** | | | X | | | | | | | | | | | | | | | X | |
| **HDVICP2-2 VDMA** | | | X | | | | | | | | | | | | | | | X | |
| **HDVPSS Mstr0** | | X | | | | | | | | | | | | | | | | X | |
| **HDVPSS Mstr1** | | | X | | | | | | | | | | | | | | | X | |
| **SGX530 BIF** | | | X | | | | | | | | | | | | | | | | |
| **SATA** | | X | | | | | | | | | | | | | | | | X | |
| **EMAC0 Rx and Tx** | | X | | | | | | | | | | | | | | | | X | |
| **EMAC1 Rx and Tx** | | X | | | | | | | | | | | | | | | | X | |
| **USB2.0 DMA** | | X | | | | | | | | | | | | | | | | | |
| **USB2.0 Queue Mgr** | | X | | | | | | | | | | | | | | | | X | |
| **PCIe Gen2** | | X | | | X | | X | | | | | | | | | | | X | |
| **EDMA TPTC0** | S | | X | | X | | X | X | X | X | X | | X | | X | | X | X | |
| **EDMA TPTC1** | | X | | | X | | X | X | X | X | X | X | | X | | | X | X | |
| **EDMA TPTC2** | | | X | | X | | X | X | X | X | X | | X | | X | | X | X | |
| **EDMA TPTC3** | | X | | | X | | X | X | X | X | X | X | | X | | | X | X | |

(1) X = Connection exists.
S = Selectable path based on thirty-third address bit from control module register for System MMU accessible targets. Non-System MMU accessible targets (such as C674x SDMA) are always direct mapped.
(2) Three HDVICP2 modules are available on the DM8168 and DM8167 devices; two HDVICP2 modules (HDVICP2-0 and HDVICP2-1) are available on the DM8165 devices.
(3) SGX530 is available only on the DM8168 device.

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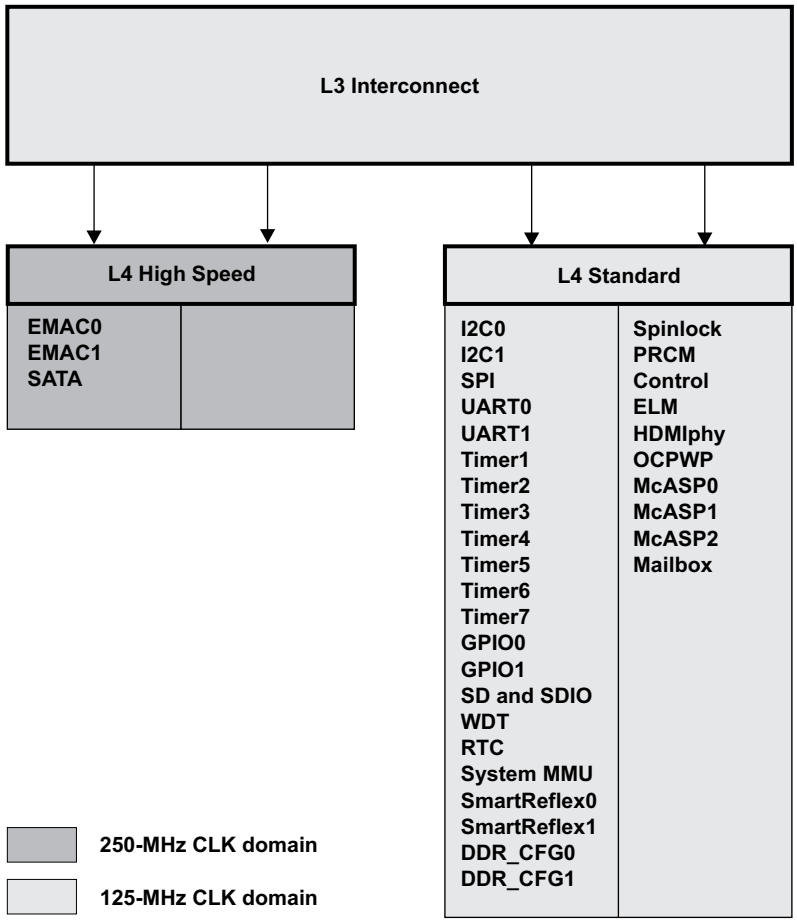
## 7.2 L4 Interconnect

The L4 interconnect is a non-blocking peripheral interconnect that provides low-latency access to a large number of low-bandwidth, physically-dispersed target cores. The L4 can handle incoming traffic from up to four initiators and can distribute those communication requests to and collect related responses from up to 63 targets.

The device provides three interfaces with L3 interconnect for high-speed peripheral and standard peripheral. Figure 7-2 and Table 7-2 show the L4 bus architecture and memory-mapped peripherals.




A. Three HDVICP2 modules are available on the DM8168 and DM8167 devices; two HDVICP2 modules are available on the DM8165 devices.
B. SGX530 is available only on the DM8168 device.

**Figure 7-2. L4 Architecture**


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**Table 7-2. L4 Peripheral Connectivity(1)**

| L4 PERIPHERALS | MASTERS | | | | | | |
|---|---|---|---|---|---|---|---|
| | Cortex-A8 M2 (64-bit) | EDMA TPTC0 | EDMA TPTC1 | EDMA TPTC2 | EDMA TPTC3 | C674x CONFIG | SYSTEM MMU |
| **L4 High-Speed Peripherals Port0 and Port1** | | | | | | | |
| EMAC0 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| EMAC1 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| SATA | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| **L4 Standard-Speed Peripherals Port0 and Port1** | | | | | | | |
| I2C0 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| I2C1 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| SPI | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| UART0 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| UART1 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| Timer1 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| Timer2 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| Timer3 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| Timer4 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | |
| Timer5 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | |
| Timer6 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | |
| Timer7 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| GPIO0 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| GPIO1 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| SD and SDIO | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| WDT | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| RTC | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| System MMU | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| SmartReflex0 | Port0 | | | | | | |
| SmartReflex1 | Port0 | | | | | | |
| DDR_CFG0 | Port0 | | | | | | |
| DDR_CFG1 | Port0 | | | | | | |
| Spinlock | Port0 | | | | | Port0 | Port0 |
| PRCM | Port0 | | | | | | |
| Control and Top Regs | Port0 | | | | | | |
| ELM | Port0 | | | | | | |
| HDMIphy | Port0 | | | | | | |
| OCPWP | Port0 | | | | | | |
| McASP0 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| McASP1 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| McASP2 | Port0 | Port1 | Port0 | Port1 | Port0 | | |
| Mailbox | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 |

(1) X, Port0, Port1 = Connection exists.

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# 8 Power, Reset, Clocking, and Interrupts

## 8.1 Power Supplies

### 8.1.1 Voltage and Power Domains

The device has the following voltage domains:

- 1-V adaptive voltage scaling (AVS) domain - Main voltage domain for all modules
- 1-V constant domain - Memories, PLLs, DACs, DDR IOs, HDMI, and USB PHYs
- 1.8-V constant domain - PLLs, DACs, HDMI, and USB PHYs
- 3.3-V constant domain - IOs and USB PHY
- 1.5-V constant domain - DDR IOs, PCIe, and SATA SERDES
- 0.9-V constant domain - USB PHY

These domains define groups of modules that share the same supply voltage for their core logic. Each voltage domain is powered by dedicated supply voltage rails. For the mapping between voltage domains and the supply pins associated with each, see Table 4-33.

**Note:** A regulated supply voltage must be supplied to each voltage domain at all times, regardless of the power domain states.

### 8.1.2 Power Domains

The device's 1-V AVS and 1-V constant voltage domains have seven power domains that supply power to both the core logic and SRAM within their associated modules. All other voltage domains have only always-on power domain.

Within the 1-V AVS and 1-V constant voltage domains, each power domain, except for the always-on domain, has an internal power switch that can completely remove power from that domain. At power-up, all domains, except always-on, come-up as power gated. Since there is an always-on domain in each voltage domain, all power supplies are expected to be ON all the time (as long as the device is in use).

For details on powering up or powering down the device power domains, see the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).

**Note:** All modules within a power domain are unavailable when the domain is powered OFF. For instructions on powering ON or powering OFF the domains, see the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).

### 8.1.3 1-V AVS and 1-V Constant Power Domains

- **HDVICP2-0 Domain**

  This power domain contains HDVICP2-0. If HDVICP2-0 is not used, it can be power gated.
- **HDVICP2-1 Domain**

  This power domain contains HDVICP2-1. If HDVICP2-1 is not used, it can be power gated.
- **HDVICP2-2 Domain**

  This power domain contains HDVICP2-2. If HDVICP2-2 is not used, it can be power gated.

  **Note:** Three HDVICP2 modules are available on the DM8168 and DM8167 devices and two HDVICP2 modules (HDVICP2-0 and HDVICP2-1) are available on the DM8165 devices.
- **Graphics Domain**

  This domain contains the SGX530 (available only on the DM8168 device).
- **Active Domain**

  The active domain has all modules that are only needed when the system is in "active" state. In any of the standby states, these modules are not needed. This domain contains the C674x DSP and HDVPSS peripheral.
- **Default Domain**


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The default domain contains modules that might be required even in standby mode. Having them in a separate power domain allows customers to power gate these modules when in standby mode. This domain has the DDR, SATA, PCIe, Media Controller and USB peripherals.

- **Always-On Domain**

  The always-on domain contains all modules that are required even when the system goes to standby mode. This includes the host ARM and modules that generate wake-up interrupts (for example, UART, RTC, GPIO, EMAC) as well as other low-power IOs.

### 8.1.4 SmartReflex™

The device contains SmartReflex modules that are required to minimize power consumption on the voltage domains using external variable-voltage power supplies. Based on the device process, temperature, and desired performance, the SmartReflex modules advise the host processor to raise or lower the supply voltage to each domain for minimal power consumption. The communication link between the host processor and the external regulators is a system-level decision and can be accomplished using GPIOs or I2C.

The major technique employed by SmartReflex in the device is adaptive voltage scaling (AVS). Based on the silicon process and temperature, the SmartReflex modules guide software in adjusting the core 1-V supply voltage within the desired range. This technique is called adaptive voltage scaling (AVS). AVS occurs continuously and in real time, helping to minimize power consumption in response to changing operating conditions.

**NOTE**

Implementation of SmartReflex AVS is **required** for proper device operation.

### 8.1.5 Memory Power Management

The device memories offer three different modes to save power when memories are not being used; Table 8-1 provides the details.

**Table 8-1. Memory Power Management Modes**

| MODE | POWER SAVING | WAKE-UP LATENCY | MEMORY CONTENTS |
|---|---|---|---|
| Light Sleep (LS) | ~60% | Low | Preserved |
| Deep Sleep (DS) | ~75% | Medium | Preserved |
| Shut Down (SD) | ~95% | High | Lost |

The device provides a feature that allows the software to put the chip-level memories (C674x L2, OCMC RAMs) in any of the three (LS, DS, and SD) modes. There are control registers in the control module to control the power-down state of C674x L2, OCMC RAM0, and OCMC RAM1. There are also status registers that can be used during power-up to check if memories are powered-up. For detailed instructions on entering and exiting from light sleep and deep sleep modes, see the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).

Memories inside switchable domains go to the shut down (SD) state whenever the power domain goes to the OFF state. Memories come back to functional state along with the domain power-up.

In order to reduce SRAM leakage, many SRAM blocks can be switched from active mode to shut-down mode. When SRAM is put in shut-down mode, the voltage supplied to it is automatically removed and all data in that SRAM is lost.

All SRAM located in a switchable power domain (all domains except always-on) automatically enters shut-down mode whenever its assigned associated power domain goes to the OFF state. The SRAM returns to the active state when the corresponding power domain returns to the ON state.

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For detailed instructions on powering up or powering down the various device SRAM, see the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).

### 8.1.6 IO Power-Down Modes

The DDR3 IOs are put into power-down mode automatically when the default power domain is turned OFF.

The HDMI PHY controller is in the always-on power domain, so software must configure the PHY into power-down mode.

There is no power-down mode for the other 3.3-V IOs.

### 8.1.7 Supply Sequencing

The device power supplies must be sequenced in the following order:

1. 3.3 V
2. 1-V AVS
3. 1-V Constant
4. 1.8 V
5. 1.5 V
6. 0.9 V

Each supply (represented by $VDD_B$ in Figure 8-1) must begin actively ramping between 0 ms and 50 ms after the previous supply (represented by $VDD_A$ in Figure 8-1) in the sequence has reached 80% of its nominal value, as shown in Figure 8-1.

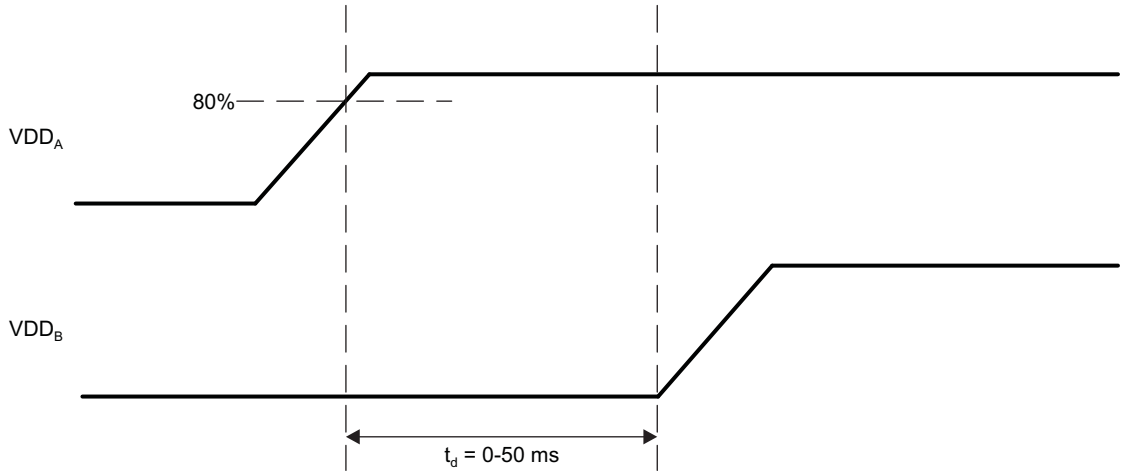


**Figure 8-1. Power Sequencing Requirements**

**NOTE**

The device pins are not fail-safe. Device pins should not be externally driven before the corresponding supply rail has been powered up. The corresponding supply rail for each pin can be found in Section 4.2, *Terminal Functions*.

### 8.1.8 Power-Supply Decoupling

Recommended capacitors for power supply decoupling are all 0.1 µF in the smallest body size that can be used. Capacitors are more effective in the smallest physical size to limit lead inductance. For example, 0402 sized capacitors are better than 0603 sized capacitors, and so on.


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**Table 8-2. Recommended Power-Supply Decoupling Capacitors**

| SUPPLY | MINIMUM CAPACITOR NO. |
|---|---|
| VDDA_PLL | 2(1) |
| DVDD1P8 | 2 |
| VDDT_SATA | 2(1) |
| VDDT_PCIE | 3(1) |
| CVDDC | 20(2) |
| DVDD_3p3 | 64(2) |
| CVDD | 28(2) |

(1) PLL supplies benefit from filters or ferrite beads to keep the noise from causing clock jitter. The minimum recommendation is a ferrite bead with a resonance at 100 MHz along with at least one capacitor on the device side of the bead. Additional recommendation is to add one capacitor just before the bead to form a Pi filter. The filter needs to be as close as possible to the device pin, with the device-side capacitor being the most important component to be close to the device pin. PLL pins close together can be combined on the same supply. PLL pins spaced farther away from one another may need individual filtered supplies.

(2) It is recommended to have one bulk (15 µF or larger) capacitor for every 10 smaller capacitors placed as closely as possible to the device.

DDR-related supply capacitor numbers are provided in Section 9.3.

## 8.2 Reset

### 8.2.1 System-Level Reset Sources

The device has several types of system-level resets. Table 8-3 lists these reset types, along with the reset initiator and the effects of each reset on the device.

**Table 8-3. System-Level Reset Types**

| TYPE | INITIATOR | RESETS ALL MODULES, EXCLUDING EMULATION | RESETS EMULATION | LATCHES BOOT PINS | ASSERTS $\overline{\text{RSTOUT}}$ PIN |
|---|---|---|---|---|---|
| Power-On Reset (POR) | $\overline{\text{POR}}$ pin | Yes | Yes | Yes | Yes |
| External Warm Reset | $\overline{\text{RESET}}$ pin | Yes | No | Yes | Yes |
| Emulation Warm Reset | On-Chip Emulation Logic | Yes | No | No | Yes |
| Watchdog Reset | Watchdog Timer | Yes | No | No | Yes |
| Software Global Cold Reset | Software | Yes | Yes | No | Yes |
| Software Global Warm Reset | Software | Yes | No | No | Yes |
| Test Reset | $\overline{\text{TRST}}$ pin | No | Yes | No | No |

### 8.2.2 Power-On Reset ($\overline{\text{POR}}$ pin)

Power-on reset (POR) is initiated by the $\overline{\text{POR}}$ pin and is used to reset the entire chip, including the test and emulation logic. POR is also referred to as a cold reset since it is required to be asserted when the devices goes through a power-up cycle. However, a device power-up cycle is not required to initiate a power-on reset.

The following sequence must be followed during a power-on reset:

1. Wait for the power supplies to reach normal operating conditions while keeping the $\overline{\text{POR}}$ pin asserted.
2. Wait for the input clock sources SERDES_CLKN and SERDES_CLKNP to be stable (if used by the

system) while keeping the POR pin asserted (low).

3. Once the power supplies and the input clock source are stable, the POR pin must remain asserted (low) for a minimum of 32 DEV_MXI cycles. Within the low period of the POR pin, the following happens:
   (a) All pins enter a Hi-Z mode.
   (b) The PRCM asserts reset to all modules within the device.
   (c) The PRCM begins propagating these clocks to the chip with the PLLs in bypass mode.
4. The POR pin may now be deasserted (driven high). When the POR pin is deasserted (high):
   (a) The BOOT pins are latched.
   (b) Reset to the ARM Cortex-A8 is de-asserted, provided the processor clock is running.
   (c) All other domain resets are released, provided the domain clocks are running.
   (d) The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
   (e) The ARM Cortex-A8 begins executing from the default address (Boot ROM).

### 8.2.3 External Warm Reset (RESET pin)

An external warm reset is activated by driving the RESET pin active-low. This resets everything in the device, except the ARM Cortex-A8 interrupt controller, test, and emulation. An emulator session stays alive during warm reset.

The following sequence must be followed during a warm reset:

1. Power supplies and input clock sources should already be stable.
2. The RESET pin must be asserted (low) for a minimum of 32 DEV_MXI cycles. Within the low period of the RESET pin, the following happens:
   (a) All pins, except test and emulation pins, enter a Hi-Z mode.
   (b) The PRCM asserts reset to all modules within the device, except for the ARM Cortex-A8 interrupt controller, test, and emulation.
   (c) RSTOUT is asserted.
3. The RESET pin may now be de-asserted (driven high). When the RESET pin is de-asserted (high):
   (a) The BOOT pins are latched.
   (b) Reset to the ARM Cortex-A8 and modules without a local processor is de-asserted, with the exception of the ARM Cortex-A8 interrupt controller, test, and emulation.
   (c) RSTOUT is de-asserted.
   (d) The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
   (e) The ARM Cortex-A8 begins executing from the default address (Boot ROM).
   (f) Since the ARM Cortex-A8 interrupt controller is not impacted by warm reset, application software needs to explicitly clear all pending interrupts in the ARM Cortex-A8 interrupt controller.

### 8.2.4 Emulation Warm Reset

An emulation warm reset is activated by the on-chip emulation module. It has the same effect and requirements as an external warm reset (RESET), with the exception that it does not re-latch the BOOT pins.

The emulator initiates an emulation warm reset via the ICEPick module. To invoke the emulation warm reset via the ICEPick module, the user can perform the following from the Code Composer Studio™ IDE menu:

Debug → Advanced Resets → System Reset.


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### 8.2.5 Watchdog Reset

A watchdog reset is initiated when the watchdog timer counter reaches zero. It has the same effect and requirements as an external warm reset (RESET), with the exception that it does not re-latch the BOOT pins. In addition, a watchdog reset always results in RSTOUT being asserted.

### 8.2.6 Software Global Cold Reset

A software global cold reset is initiated under software control. It has the same effect and requirements as a power-on reset (POR), with the exception that it does not re-latch the BOOT pins.

Software initiates a software global cold reset by writing to RST_GLOBAL_COLD_SW in the PRM_RST_CTRL register.

### 8.2.7 Software Global Warm Reset

A software global warm reset is initiated under software control. It has the same effect and requirements as a external warm reset (RESET), with the exception that it does not re-latch the BOOT pins.

Software initiates a software global warm reset by writing to RST_GLOBAL_WARM_SW in the PRM_RST_CTRL register.

### 8.2.8 Test Reset (TRST pin)

A test reset is activated by the emulator asserting the TRST pin. The only effect of a test reset is to reset the emulation logic.

### 8.2.9 Local Reset

The local reset for various modules within the device is controlled by programming the PRCM and the module's internal registers. Only the associated module is reset when a local reset is asserted, leaving the rest of the device unaffected.

For details on local reset, see the PRCM chapter of the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8) and individual subsystem and peripheral user's guides.

### 8.2.10 Reset Priority

If any of the above reset sources occur simultaneously, the device only processes the highest-priority reset request. The reset request priorities, from high to low, are as follows:

1. Power-on reset (POR)
2. Test reset (TRST)
3. External warm reset (RESET)
4. Emulation warm resets
5. Watchdog reset
6. Software global cold and warm resets.

### 8.2.11 Reset Status Register

The Reset Status Register (PRM_RSTST) contains information about the last reset that occurred in the system. For more information on this register, see the PRCM chapter of the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).

### 8.2.12 PCIe Reset Isolation

The device supports reset isolation for the PCI Express (PCIe) module. This means that the PCI Express subsystem can be reset without resetting the rest of the device.

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When the device is a PCI Express Root Complex (RC), the PCIe subsystem can be reset by software through the PRCM. Software should ensure that there are no ongoing PCIe transactions before asserting this reset by first taking the PCIe subsystem into the IDLE state by programming the register CM_DEFAULT_PCI_CLKCTRL inside the PRCM. After bringing the PCIe subsystem out of reset, bus enumeration should be performed again and should treat all endpoints (EP) as if they had just been connected.

When the device is a PCI Express Endpoint (EP), the PCIe subsystem generates an interrupt when an in-band reset is received. Software should process this interrupt by putting the PCIe subsystem in the IDLE state and then asserting the PCIe local reset through the PRCM.

All device-level resets mentioned in the previous sections, except Test Reset, also reset the PCIe subsystem. Therefore, the device should issue a Hot Reset to all downstream devices and re-enumerate the bus upon coming out of reset.

### 8.2.13 $\overline{\text{RSTOUT}}$

The $\overline{\text{RSTOUT}}$ pin on the device reflects device reset status and is de-asserted (high) when the device is out of reset. In addition, this output is always 3-stated and the internal pull resistor is disabled on this pin while $\overline{\text{POR}}$ or $\overline{\text{RESET}}$ is asserted; therefore, an external pullup or pulldown can be used to set the state of this pin (high or low) while $\overline{\text{POR}}$ or $\overline{\text{RESET}}$ is asserted. For more detailed information on external pullups and pulldowns, see Section 6.3.1. This output is always asserted low when any of the following resets occur:

- Power-on reset ($\overline{\text{POR}}$)
- External warm reset
- Emulation warm reset ($\overline{\text{RESET}}$)
- Software global cold or warm reset
- Watchdog timer reset.

The $\overline{\text{RSTOUT}}$ pin remains asserted until PRCM releases the host ARM Cortex-A8 processor for reset.

### 8.2.14 Effect of Reset on Emulation and Trace

The device emulation and trace is only reset by the following sources:

- Power-on reset ($\overline{\text{POR}}$)
- Software global cold reset
- Test reset ($\overline{\text{TRST}}$).

Other than these three, none of the other resets affect emulation and trace functionality.

### 8.2.15 Reset During Power Domain Switching

Each power domain has a dedicated warm reset and cold reset. Warm reset for a power domain is asserted under either of the following two conditions:

1. A power-on reset, external warm reset, emulation warm reset, or software global cold or warm reset occurs.
2. When that power domain switches from the ON state to the OFF state.

Cold reset for a power domain is asserted under either of the following two conditions:

1. A power-on reset or software global cold reset occurs.
2. When that power domain switches from the ON state to the OFF state.

### 8.2.16 Pin Behaviors at Reset

When any reset (other than test reset) described in Section 8.2.1 is asserted, all device pins are put into a Hi-Z state except for:


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- Emulation pins. These pins are only put into a Hi-Z state when $\overline{\text{POR}}$ or global software cold reset is asserted.
- $\overline{\text{RSTOUT}}$ pin.

In addition, the PINCNTL registers, which control pin multiplexing, slew control, enabling the pullup or pulldown, and enabling the receiver, are reset to the default state. For a description of the RESET_ISO register, see the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).

Internal pullup or pulldown (IPU or IPD) resistors are enabled during and immediately after reset as described in the OTHER column in the tables in Section 4.2, *Terminal Functions*.

### 8.2.17 Reset Electrical Data and Timing

**NOTE**

If a configuration pin must be routed out from the device, the internal pullup or pulldown (IPU or IPD) resistor should not be relied upon; TI recommends the use of an external pullup or pulldown resistor.

**Table 8-4. Timing Requirements for Reset**

(see Figure 8-2 and Figure 8-3)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(RESET)}$ | Pulse duration, $\overline{\text{POR}}$ low or $\overline{\text{RESET}}$ low | 32C(1) | | ns |
| 2 | $t_{su(CONFIG)}$ | Setup time, boot and configuration pins valid before $\overline{\text{POR}}$ high or $\overline{\text{RESET}}$ high(2) | 12C(1) | | ns |
| 3 | $t_{h(CONFIG)}$ | Hold time, boot and configuration pins valid after $\overline{\text{POR}}$ high or $\overline{\text{RESET}}$ high(2) | 0 | | ns |

(1) C = 1/DEV_MXI clock frequency, in ns. The device clock source must be stable and at a valid frequency prior to meeting the $t_{w(RESET)}$ requirement.
(2) For the list of boot and configuration pins, see Table 4-1, *Boot Terminal Functions*.

**Table 8-5. Switching Characteristics Over Recommended Operating Conditions During Reset**

(see Figure 8-2)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | $t_{w(RSTL)}$ | Pulse width, $\overline{\text{RESET}}$ low | 10C(1) | | ns |
| 4 | $t_{d(RSTL_IORST)}$ | Delay time, $\overline{\text{RESET}}$ falling to all IO entering reset state | 0 | 14 | ns |
| 5 | $t_{d(RSTL_IOFUNC)}$ | Delay time, $\overline{\text{RESET}}$ rising to IO exiting reset state | 0 | 14 | ns |

(1) C = 1/DEV_CLKIN clock frequency, in ns.

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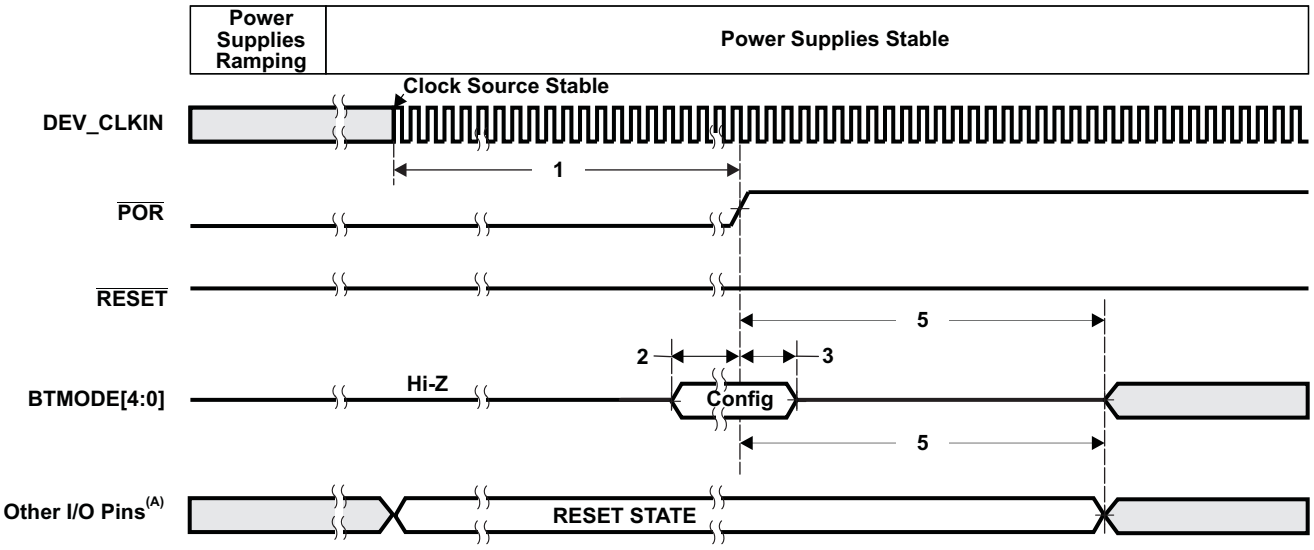
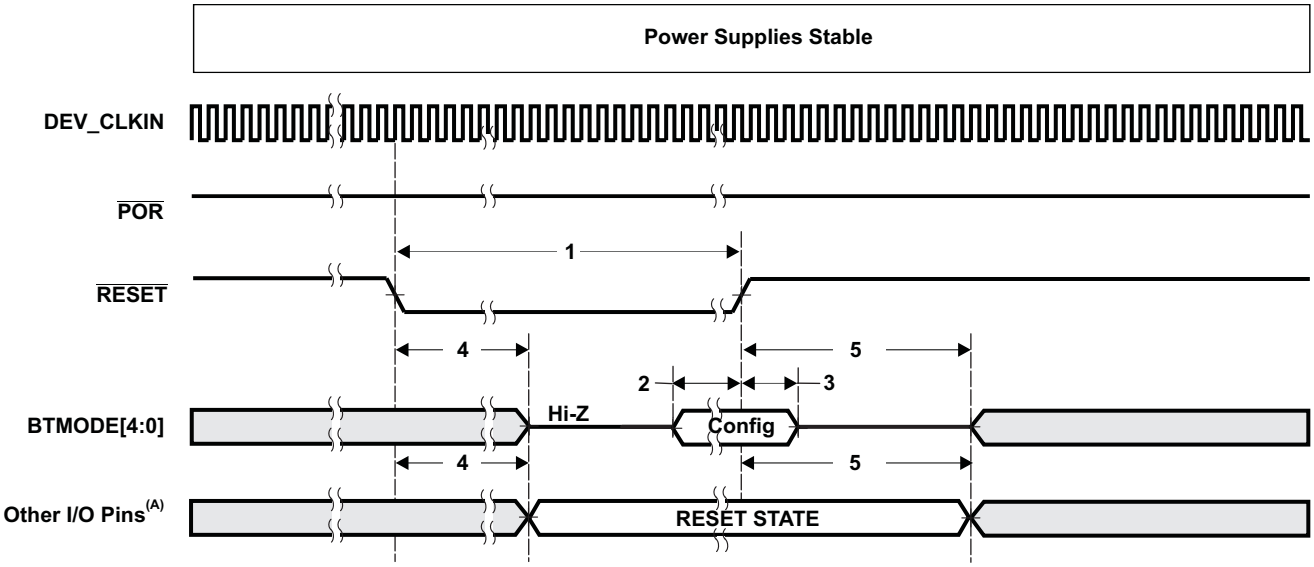



A. For more detailed information on the reset state of each pin, see Section 8.2.16, *Pin Behaviors at Reset*. For the IPU and IPD settings during reset, see Section 4.2, *Terminal Functions*.

**Figure 8-2. Power-Up Timing**




A. For more detailed information on the reset state of each pin, see Section 8.2.16, *Pin Behaviors at Reset*. For the IPU and IPD settings during reset, see Section 4.2, *Terminal Functions*.

**Figure 8-3. Warm Reset ($\overline{\text{RESET}}$) Timing**

## 8.3 Clocking

The device clocks are generated from several external reference clocks that are fed to on-chip PLLs and dividers (both inside and outside of the PRCM Module). Figure 8-4 shows a high-level overview of the device clocking structure. Note that to reduce complexity, all clocking connections are not shown. For detailed information on the device clocks, see the Device Clocking and Flying Adder PLL section of the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).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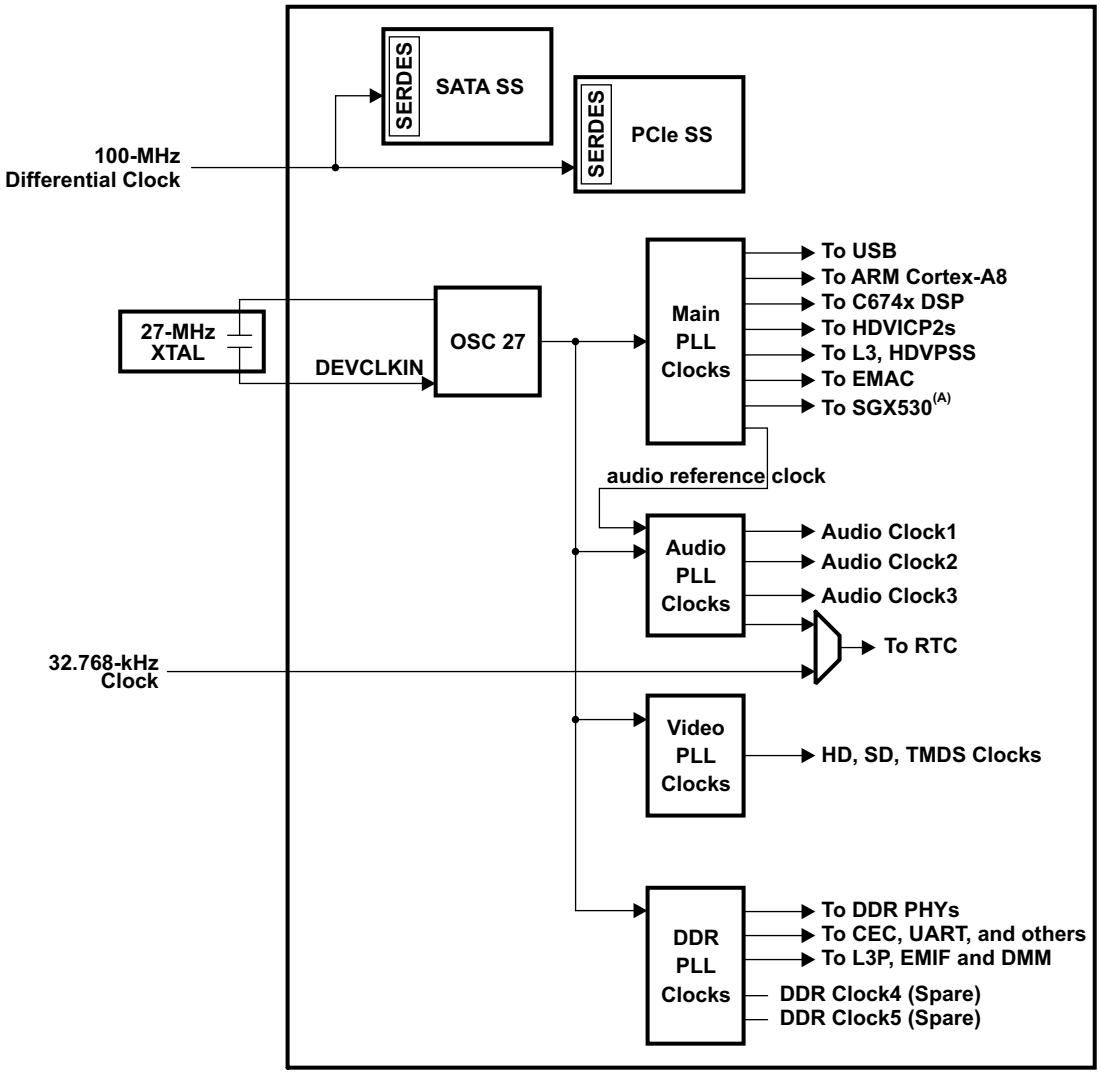


A. SGX530 is available only on the DM8168 device.

**Figure 8-4. System Clocking Overview**

### 8.3.1 Device Clock Inputs

The device has four on-chip PLLs and one reference clock which are generated by on-chip oscillators. In addition to the 27-MHz reference clock, a 100-MHz differential clock input is required for SATA and PCIe. A third clock input is an optional 32.768-kHz clock input (no on-chip oscillator) for the RTC.

The device clock input (DEV_MXI and DEV_CLKIN) is used to generate the majority of the internal reference clocks. An external square-wave clock can be supplied to DEV_CLKIN instead of using a crystal input. The device clock should be 27 MHz.

Section 8.3.1.1 provides details on using the on-chip oscillators with external crystals for the 27-MHz system oscillator.

#### 8.3.1.1 Using the Internal Oscillators

When the internal oscillators are used to generate the device clock, external crystals are required to be connected across the MXI and MXO pins, along with two load capacitors, as shown in Figure 8-5. The external crystal load capacitors should also be connected to the associated oscillator ground pin (DEVOSC_VSS). The capacitors should not be connected to board ground (VSS).

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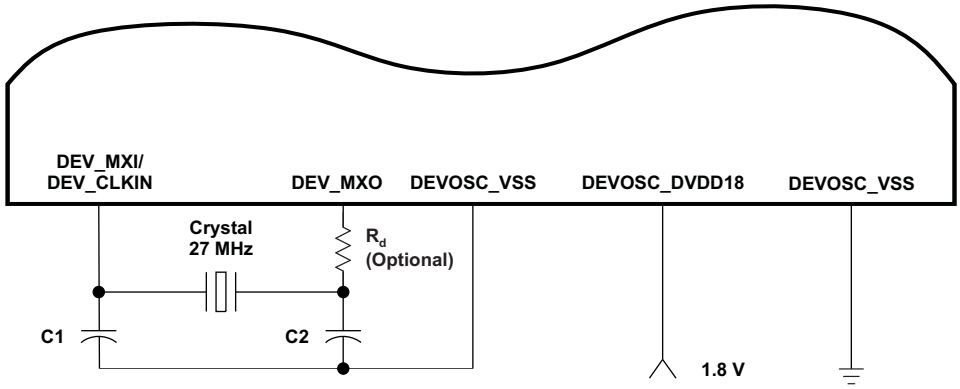


**Figure 8-5. 27-MHz System Oscillator**

The load capacitors, C1 and C2 in Figure 8-5, should be chosen such that the equation below is satisfied. $C_L$ in the equation is the load specified by the crystal manufacturer. $R_d$ is an optional damping resistor. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator MXI, MXO, and VSS pins.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

**Table 8-6. Input Requirements for Crystal Circuit on the Device Oscillator**

| PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Start-up time (from power up until oscillating at stable frequency of 27 MHz) | | | 4 | ms |
| Crystal Oscillation frequency | | 27 | | MHz |
| Parallel Load Capacitance (C1 and C2) | 12 | | 24 | pF |
| Crystal ESR | | | 60 | Ohm |
| Crystal Shunt Capacitance | | | 5 | pF |
| Crystal Oscillation Mode | | Fundamental Only | | |
| Crystal Frequency stability | | | ±50 | ppm |


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**Table 8-7. DEV_CLKIN Clock Source Requirements(1)(2)(3)**

(see Figure 8-6)

| NO. | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(DCK)}$ | Cycle time, DEV_CLKIN | | 37.037 | | ns |
| 2 | $t_{w(DCKH)}$ | Pulse duration, DEV_CLKIN high | 0.45C | | 0.55C | ns |
| 3 | $t_{w(DCKL)}$ | Pulse duration, DEV_CLKIN low | 0.45C | | 0.55C | ns |
| 4 | $t_{t(DCK)}$ | Transition time, DEV_CLKIN | | | 7 | ns |
| 5 | $t_{J(DCK)}$ | Period jitter, DEV_CLKIN (VDACs not used) | | | 150 | ps |
| | | Period jitter, DEV_CLKIN (VDACs used) | | | A | s |
| | $S_f$ | Frequency stability, DEV_CLKIN | | | ±50 | ppm |

(1) The reference points for the rise and fall transitions are measured at $V_{IL}$ MAX and $V_{IH}$ MIN.
(2) C = DEV_CLKIN cycle time in ns.
(3)

$$A = 10 * \frac{10^{\frac{-SNR}{20}}}{2 * \pi * BW} * \sqrt{\frac{BW}{27\ MHz}}(s)$$

Where SNR is the desired signal-to-noise ratio and BW is the highest DAC signal bandwidth used in the system (SD = 6 MHz, 720p or 1080i = 30 MHz, 1080p = 60 MHz).

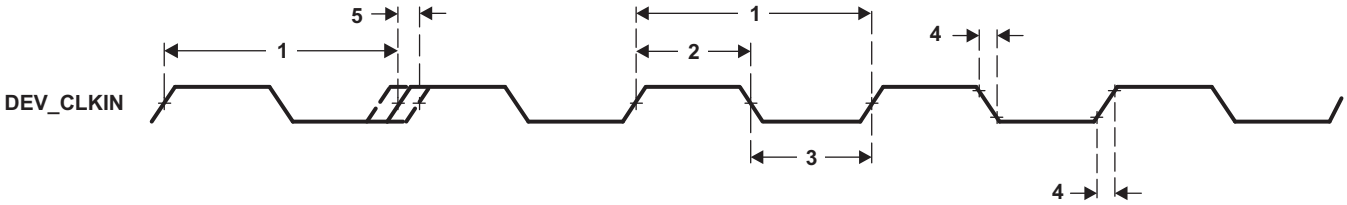


**Figure 8-6. DEV_CLKIN Timing**

### 8.3.2 SERDES_CLKN and SERDES_CLKP Input Clock

A high-quality, low-jitter differential clock source is required for the PCIe and SATA PHYs. The clock is required to be AC coupled to the device's SERDES_CLKP and SERDES_CLKN pins according to the specifications in Table 8-11. Both the clock source and the coupling capacitors should be placed physically as close as possible to the processor.

When the PCIe interface is used, the SERDES_CLKN or SERDES_CLKP clock is required to meet the REFCLK AC specifications outlined in the *PCI Express Card Electromechanical Specification (Gen.1 and Gen.2)*. When the SATA interface is used, the SERDES_CLKN or SERDES_CLKP clock is required to meet the specifications in Table 8-8. When both the PCIe and SATA interfaces are used, both sets of specifications must be met simultaneously.

**Table 8-8. SERDES_CLKN and SERDES_CLKP Clock Source Requirements for SATA**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Clock Frequency | | 100 | | MHz |
| Jitter | | | 50 | Ps pk-pk |
| Duty Cycle | 40 | | 60 | % |
| Rise and Fall Time | | 700 | | ps |

An HCSL differential clock source is required to meet the REFCLK AC specifications outlined in the PCI Express Card Electromechanical Specification, Rev. 2.0, at the input to the AC coupling capacitors. In addition, LVDS clock sources that are compliant to the above specification, but with the exceptions shown in Table 8-9, are also acceptable.

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**Table 8-9. Exceptions to REFCLK AC Specification for LVDS Clock Sources**

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IH}$ | Differential input high voltage ($V_{IH}$) | 125 | 1000 | mV |
| $V_{IL}$ | Differential input high voltage ($V_{IL}$) | -1000 | -125 | mV |

**Table 8-10. SERDES_CLKN and SERDES_CLKP Routing Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Number of stubs allowed on SERDES_CLKN and SERDES_CLKP traces | | | 0 | Stubs |
| SERDES_CLKN and SERDES_CLKP trace length from oscillator to device | | | 24000 (1) | Mils |
| SERDES_CLKN and SERDES_CLKP pair differential impedance | | 100 | | Ohms |
| Number of vias on each SERDES_CLKN and SERDES_CLKP trace (2) | | | 3 | Vias |
| SERDES_CLKN and SERDES_CLKP differential pair to any other trace spacing | 2*DS (3) | | | |

(1) Keep trace length as short as possible.
(2) Vias must be used in pairs with their distance minimized.
(3) DS is the differential spacing of the SERDES_CLKN and SERDES_CLKP traces.

AC coupling capacitors are required on the SERDES_CLKN and SERDES_CLKP pair. Table 8-11 shows the requirements for these capacitors.

**Table 8-11. SERDES_CLKN and SERDES_CLKP AC Coupling Capacitors Requirements**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| SERDES_CLKN and SERDES_CLKP AC coupling capacitor value (1) | 0.24 | 0.27 | 4 | nF |
| SERDES_CLKN and SERDES_CLKP AC coupling capacitor package size | | | 0402 | 10 Mils (2) (3) |

(1) The value of this capacitor depends on several factors including differential input clock swing. For a 100-MHz differential clock with an approximate 1-V voltage swing, the recommended typical value for the SERDES clock AC coupling capacitors is 270 pF. Deviating from this recommendation can result in the reduction of clock signal amplitude or lowering the noise rejection characteristics.
(2) LxW, 10 mil units; a 0402 is a 40x20 mil surface mount capacitor.
(3) The physical size of the capacitor should be as small as possible.

### 8.3.3 CLKIN32 Input Clock

An external 32.768-kHz clock input can optionally be provided at the CLKIN32 pin to serve as a reference clock in place of the RTCDIVIDER clock for the RTC and Timer modules. If the CLKIN32 pin is not connected to a 32.768-kHz clock input, this pin should be pulled low. The CLKIN32 source must meet the timing requirements shown in Table 8-12.

**Table 8-12. Timing Requirements for CLKIN32 (1) (2)**

(see Figure 8-7)

| NO. | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(CLKIN32)}$ | Cycle time, CLKIN32 | 1/32768 | | | s |
| 2 | $t_{w(CLKIN32H)}$ | Pulse duration, CLKIN32 high | 0.45C | | 0.55C | ns |
| 3 | $t_{w(CKIN32L)}$ | Pulse duration, CLKIN32 low | 0.45C | | 0.55C | ns |
| 4 | $t_{t(CLKIN32)}$ | Transition time, CLKIN32 | | | 7 | ns |
| 5 | $t_{J(CLKIN32)}$ | Period jitter, CLKIN32 | | | 0.02C | ns |

(1) The reference points for the rise and fall transitions are measured at $V_{IL}$ MAX and $V_{IH}$ MIN.
(2) C = CLKIN32 cycle time, in ns. For example, when CLKIN32 frequency is 32768 Hz, use C = 1/32768 s.


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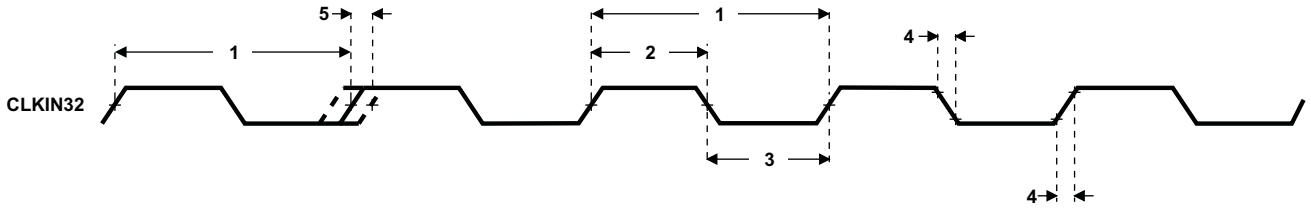


**Figure 8-7. CLKIN32 Timing**

### 8.3.4 PLLs

The device contains four embedded PLLs (Main, Audio, Video and DDR) that provide clocks to different parts of the system. For a high-level view of the device clock architecture, including the PLL reference clock sources and connections, see Figure 8-4.

The reference clock for most of the PLLs comes from the DEV_CLKIN input clock. Also, each PLL supports a bypass mode in which the reference clock can be directly passed to the PLL CLKOUT. All device PLLs (except the DDR PLL) come-up in bypass mode after reset.

Flying-adder PLLs are used for all the on-chip PLLs. Figure 8-8 shows the basic structure of the flying-adder PLL.

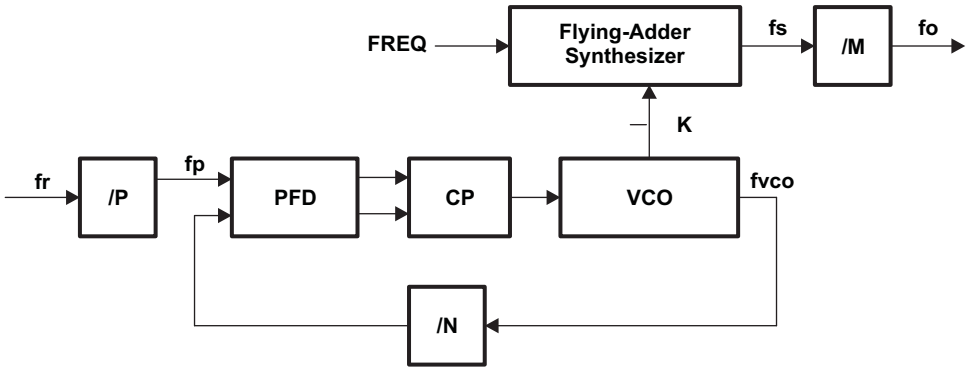


**Figure 8-8. Flying-Adder PLL**

The flying-adder PLL has two main components: a multi-phase PLL and the flying-adder synthesizer. The multi-phase PLL takes an input reference clock (fr), multiplies it with factor, N, and provides a K-phase output to the flying-adder synthesizer. The flying-adder synthesizer takes this multi-phase clock input and produces a variable frequency clock (fs). There can be a post divider on this clock which takes in clock fs and drives out clock fo. The frequency of the clock driven out is given by:

$$fo = \left[ \frac{(N * K)}{(FREQ * P * M)} \right] * fr$$

There can be multiple flying-adder synthesizers attached to one multi-phase PLL to generate different frequencies. In this case, FREQ (4 bits of integer and 24 bits of fractional value) and M (1 to 255) values can be adjusted for each clock separately, based on the frequency needed. The multi-phase PLL used in this device has a value of K = 8.

For details on programming the device PLLs, see the PLL chapter of the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).

#### 8.3.4.1 PLL Programming Limits

The PLL and Flying Adder Synthesizers support generation of a wide range of clocks that are all generated from the same input clock source. Therefore, these clocks are all synchronous. The flying-adder synthesizers take the multi-phase clock from the PLL and produce variable frequency clocks (fs) as stated in the previous section. Each variable frequency clock is then divided by a post divider before use.

The clock outputs from the PLL, Synthesizer and Post Divider contain period variations that must be considered. The minimum period of the generated clock is effectively the maximum clock rate. Different configurations of the PLL dividers, Synthesizer and output dividers will have larger or smaller amounts of phase variation. The equation below will calculate the minimum cycle period for a given set of settings. The result of the following minimum cycle equation must be greater than the value shown in Table 8-13.

The first term of the below equation is a characteristic of the Flying Adder PLL. The selection of M*FREQ is important. Choosing a non-integer value of M*FREQ will cause larger period variation and a higher peak instantaneous frequency. Use of non-integer M*FREQ can be done to create specific average frequencies at the cost of higher phase variation. Using integer values of M*FREQ result in minimum phase variation. The second and third terms are PLL phase jitter terms associated with the frequency synthesis. The second term is about 20ps and the third is normally 10ps.

Please refer to the Technical Reference Manual (SPRUGX8) for examples using this equation. The TRM also contains a standard set of configurations that we recommend for customer use.

$$\left(\frac{\text{Floor}(M * FREQ) * P * 10^6}{PLL_CLKIN * 8 * N}\right) - \sqrt{\frac{A * M * FREQ}{8}} - H$$

Where:

- PLL_CLKIN is the input clock frequency (in MHz) to the PLL before the P divider
- Floor( ) = round down
- M = PLL divider
- FREQ = PLL frequency setting
- A = 169 for all PLLs with the following exception: A = 218 for the audio PLL when its input is sourced from the main PLL output
- H = 0 if M * FREQ is a multiple of 8; otherwise, H = 10
- 800 MHz ≤ PLL_CLKIN * N / P ≤ 1600 MHz
- 10 MHz ≤ PLL_CLKIN / P ≤ 60 MHz


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**Table 8-13. PLL Clock Frequencies(1)**

| CLOCK | DEVICE SPEED RANGE | MIN CYCLE (ps) |
|---|---|---|
| **Main PLL** | | |
| Clock 1 | Blank | 1250 |
| | 2 | 1000 |
| | 4 | 889 |
| Clock 2 | Blank | 1000 |
| | 2 | 833 |
| | 4 | 741 |
| Clock 3 | Blank | 1876 |
| | 2 | 1667 |
| | 4 | 1481 |
| Clock 4 | Blank | 2000 |
| | 2 | 1786 |
| | 4 | 1667 |
| **DDR PLL** | | |
| Clock 2 | Blank, 2, 4 | 18519 |
| Clock 3 | Blank | 2632 |
| | 2 | 2632 |
| | 4 | 2222 |
| **Video PLL** | | |
| Clock 1 | Blank, 2, 4 | 1515 |
| Clock 2 | Blank, 2, 4 | 1515 |
| Clock 3 | Blank, 2, 4 | 1515 |
| **Audio PLL** | | |
| Clock 2 | Blank, 2, 4 | 6329 |
| Clock 3 | Blank, 2, 4 | 5076 |
| Clock 4 | Blank, 2, 4 | 5076 |
| Clock 5 | Blank, 2, 4 | 5076 |

(1) For more information on the available device speed ranges for each part number, see Table 10-1

### 8.3.4.2 PLL Power Supply Filtering

The device PLLs are supplied externally via the VDDA_PLL power-supply pins. External filtering must be added on the PLL supply pins to ensure that the requirements in Table 8-14 are met.

**Table 8-14. Power Supply Requirements**

| PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|
| Dynamic noise at VDDA_PLL pins | | 50 | mV p-p |

### 8.3.4.3 PLL Locking Sequence

All of the flying-adder PLLs (except the DDR PLL) come-up in bypass mode at reset. All of the registers (P, N, FREQ, and M) need to be programmed appropriately and then wait approximately 8 µs for PLL_Audio and 5 µs for the other PLLS to be locked. Verification that the PLL is locked can be checked by accessing the lock status bit in the PLL control register for each PLL (bit = 1 when the PLL is locked). Once the PLL is locked, then the FA-PLL can be taken out of bypass mode. Control for bypass mode is through chip-level registers. For more details on the PLL registers and bypass logic, see the PLL chapter of the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (SPRUGX8).

### 8.3.4.4 PLL Registers

The PLL control registers reside in the control module and are listed in Table 6-3.

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### 8.3.5 SYSCLKs

In some cases, the system clock inputs and PLL outputs are sent to the PRCM module for division and multiplexing before being routed to the various device modules. These clock outputs from the PRCM module are called SYSCLKs. Table 8-15 lists the main device SYSCLKs along with their maximum supported clock frequencies. In addition, limits shown in the table may be further restricted by the clock frequency limitations of the device modules using these clocks. For more details on module clock frequency limits, see Section 8.3.6.

**Table 8-15. SYSCLK Frequencies**

| SYSCLK | PLL Type | DEVICE SPEED RANGE(1) | MAXIMUM FREQUENCY (MHz)(2) | DESTINATION |
|---|---|---|---|---|
| SYSCLK1 | Main | Blank | 750 | To C674x DSP |
| | | 2 | 930 | |
| | | 4 | 1000 | |
| SYSCLK2 | Main | Blank | 930 | To ARM Cortex-A8 |
| | | 2 | 1100 | |
| | | 4 | 1200 | |
| SYSCLK3 | Main | Blank | 500 | To HDVICP2s |
| | | 2 | 550 | |
| | | 4 | 630 | |
| SYSCLK4 | Main | Blank | 460 | L3, OCP clock for HDVPSS, TPTCs, TPCC, DMM, Unicache clock for Media Controller, EDMA |
| | | 2 | 550 | |
| | | 4 | 570 | |
| SYSCLK5 | Main | Blank | 230 | L3, L4_HS, OCP clock for EMAC, SATA, PCIe, Media Controller, OCMC RAM |
| | | 2 | 275 | |
| | | 4 | 285 | |
| SYSCLK6 | Main | Blank | 115 | L3, L4_STD, UART, I2C, SPI, SD, SDIO, TIMER, GPIO, PRCM, McASP, McBSP, GPMC, ELM, HDMI, WDT, Mailbox, RTC, Spinlock, SmartReflex and USB |
| | | 2 | 137 | |
| | | 4 | 143 | |
| SYSCLK7 | Main | Blank | 90 | Reserved |
| | | 2 | 110 | |
| | | 4 | 115 | |
| SYSCLK8 | Main | Blank | 364 | DMM, DDR OCP clock |
| | | 2 | 364 | |
| | | 4 | 425 | |
| SYSCLK9 | DDR | Blank, 2, 4 | 16 | CEC clock, VTP |
| SYSCLK10 | DDR | Blank, 2, 4 | 48 | SPI, I2C, SDIO, and UART functional clock |
| SYSCLK11 | Video | Blank, 2, 4 | 216 | Reserved |
| SYSCLK13 | Video | Blank, 2, 4 | 165 | HDVPSS |
| SYSCLK14 | Video | Blank, 2, 4 | 27 | Reserved |
| SYSCLK15 | Video | Blank, 2, 4 | 165 | HDVPSS |
| SYSCLK16 | Video | Blank, 2, 4 | 27 | Reserved |
| SYSCLK17 | Video | Blank, 2, 4 | 54 | HDVPSS |
| SYSCLK18 | Audio | Blank, 2, 4 | 32 KHz | RTC |
| SYSCLK19 | Audio | Blank, 2, 4 | 160 | Reserved |
| SYSCLK20 | Audio | Blank, 2, 4 | 196 | Audio clock 1 |
| SYSCLK21 | Audio | Blank, 2, 4 | 196 | Audio clock 2 |
| SYSCLK22 | Audio | Blank, 2, 4 | 196 | Audio clock 3 |
| SYSCLK23 | Main | Blank | 310 | SGX530 OCP clock |
| | | 2 | 275 | |
| | | 4 | 300 | |
| SYSCLK24 | Main | Blank, 2, 4 | 125 | GMII clock |

(1) For more information on the available device speed ranges for each part number, see Table 10-1.
(2) Maximum frequency must respect the minimum cycle limitations described in Section 8.3.4.1.


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### 8.3.6 Module Clocks

Device modules receive their clock directly from an external clock input, directly from a PLL, or from a PRCM SYSCLK output. Table 8-16 lists the clock source options for each module, along with the maximum frequency that module can accept. The device PLLs and dividers must be programmed not to exceed the maximum frequencies listed in this table to ensure proper module functionality.

**Table 8-16. Module Clock Frequencies**

| MODULE | CLOCK SOURCES | DEVICE SPEED RANGE(1) | MAX. FREQUENCY (MHz)(2) |
|---|---|---|---|
| C674x DSP | SYSCLK1 | Blank | 750 |
| | | 2 | 930 |
| | | 4 | 1000 |
| Cortex-A8 | SYSCLK2 | Blank | 930 |
| | | 2 | 1100 |
| | | 4 | 1200 |
| DMM | SYSCLK4 | Blank | 460 |
| | | 2 | 550 |
| | | 4 | 570 |
| DMM, DDR OCP | SYSCLK8 | Blank | 364 |
| | | 2 | 364 |
| | | 4 | 425 |
| EDMA | SYSCLK4 | Blank | 460 |
| | | 2 | 550 |
| | | 4 | 570 |
| ELM | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| EMAC | SYSCLK5 | Blank | 230 |
| | | 2 | 275 |
| | | 4 | 285 |
| GPIO0 and GPIO1 | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| | SYSCLK18 | Blank, 2, 4 | 32.768 KHz |
| GPMC | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| HDMI | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| HDMI CEC | SYSCLK9 | Blank, 2, 4 | 16 |
| HDVICP2-0, HDVICP2-1, HDVICP2-2 | SYSCLK3 | Blank | 500 |
| | | 2 | 550 |
| | | 4 | 630 |
| HDVPSS VPDMA | SYSCLK4 | Blank | 460 |
| | | 2 | 550 |
| | | 4 | 570 |

(1) For more information on the available device speed ranges for each part number, see Table 10-1.
(2) Maximum frequency must respect the minimum cycle limitations described in Section 8.3.4.1.

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**Table 8-16. Module Clock Frequencies (continued)**

| MODULE | CLOCK SOURCES | DEVICE SPEED RANGE(1) | MAX. FREQUENCY (MHz)(2) |
|---|---|---|---|
| HDVPSS | SYSCLK5 | Blank | 230 |
| | | 2 | 275 |
| | | 4 | 285 |
| HDVPSS Interface | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| HDVPSS HD VENCD | SYSCLK13 | Blank, 2, 4 | 165 |
| HDVPSS HD VENCA | SYSCLK15 | Blank, 2, 4 | 165 |
| HDVPSS SD VENC | SYSCLK17 | Blank, 2, 4 | 54 |
| I2C0, I2C1 | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| | SYSCLK10 | Blank, 2, 4 | 48 |
| L3 | SYSCLK4 | Blank | 460 |
| | | 2 | 550 |
| | | 4 | 570 |
| L3 | SYSCLK5 | Blank | 230 |
| | | 2 | 275 |
| | | 4 | 285 |
| L3 | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| L4 HS | SYSCLK5 | Blank | 230 |
| | | 2 | 275 |
| | | 4 | 285 |
| L4 STD | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| Mailbox | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| McASP0, McASP1, McASP2 | SYSCLK6 | Blank, 2, 4 | 125 |
| McBSP | SYSCLK6 | Blank, 2, 4 | 125 |
| Media Controller | SYSCLK5 | Blank | 230 |
| | | 2 | 275 |
| | | 4 | 285 |
| System MMU | SYSCLK4 | Blank | 460 |
| | | 2 | 550 |
| | | 4 | 570 |
| OCMC RAM | SYSCLK5 | Blank | 230 |
| | | 2 | 275 |
| | | 4 | 285 |
| PCIe | SYSCLK5 | Blank | 230 |
| | | 2 | 275 |
| | | 4 | 285 |


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**Table 8-16. Module Clock Frequencies (continued)**

| MODULE | CLOCK SOURCES | DEVICE SPEED RANGE(1) | MAX. FREQUENCY (MHz)(2) |
|---|---|---|---|
| RTC | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| | SYSCLK18 | Blank, 2, 4 | 32.768 KHz |
| SATA | SYSCLK5 | Blank | 230 |
| | | 2 | 275 |
| | | 4 | 285 |
| SD, SDIO | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| | SYSCLK10 | Blank, 2, 4 | 48 |
| SGX530 | SYSCLK23 | Blank | 310 |
| | | 2 | 275 |
| | | 4 | 300 |
| SmartReflex | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| SPI | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| | SYSCLK10 | Blank, 2, 4 | 48 |
| Spinlock | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| Timers, WDT | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| | SYSCLK18 | Blank, 2, 4 | 32.768 KHz |
| UART0, UART1, UART2 | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |
| | SYSCLK10 | Blank, 2, 4 | 48 |
| USB0, USB1 | SYSCLK6 | Blank | 115 |
| | | 2 | 137 |
| | | 4 | 143 |

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### 8.3.7 Output Clock Select Logic

The device includes one selectable general-purpose clock output (CLKOUT). The source for these output clocks is controlled by the CLKOUT_MUX register in the control module and shown in Figure 8-9.

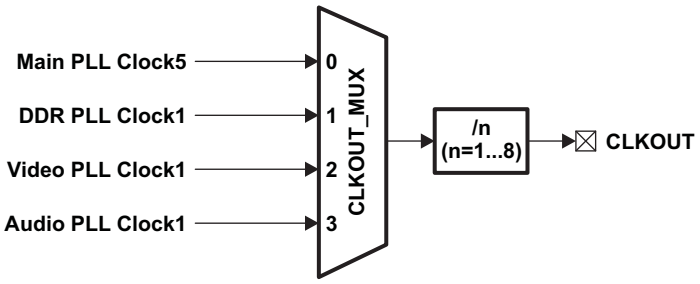


**Figure 8-9. CLKOUT Source Selection Logic**

As shown in the figure, there are four possible sources for CLKOUT, one clock from each of the four PLLs. The selected clock can be further divided by any ratio from 1 to 1/8 before going out on the CLKOUT pin. The default selection is to select main PLL clock5, divider set to 1/1, and clock disabled.

**Table 8-17. Switching Characteristics Over Recommended Operating Conditions for CLKOUT(1) (2)**

(see Figure 8-10)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLKOUT)}$ | Cycle time, CLKOUT | 10 | | ns |
| 2 | $t_{w(CLKOUTH)}$ | Pulse duration, CLKOUT high | 0.45P | 0.55P | ns |
| 3 | $t_{w(CLKOUTL)}$ | Pulse duration, CLKOUT low | 0.45P | 0.55P | ns |
| 4 | $t_{t(CLKOUT)}$ | Transition time, CLKOUT | | 0.05P | ns |

(1) The reference points for the rise and fall transitions are measured at $V_{OL}$ MAX and $V_{OH}$ MIN.
(2) P = 1/CLKOUT clock frequency in nanoseconds (ns). For example, when CLKOUT frequency is 100 MHz, use P = 10 ns.

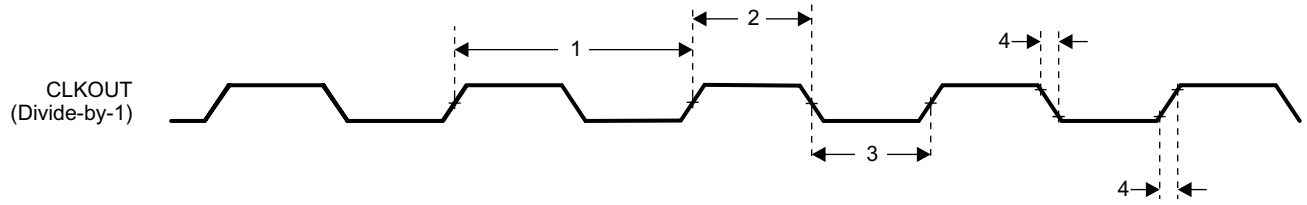


**Figure 8-10. CLKOUT Timing**


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## 8.4 Interrupts

The device has a large number of interrupts. It also has masters (ARM Cortex™-A8, C674x DSP) capable of servicing interrupts. Specific details, such as the processing flow, configuration steps, and interrupt controller registers, for each of these masters are found in their respective subsystem documentation.

### *8.4.1 Interrupt Summary List*

Table 8-18 lists all the device interrupts by module and indicates the interrupt destination: ARM Cortex™-A8, C674x DSP.

**Table 8-18. Interrupts By Module**

| MODULE | INTERRUPT | DESTINATION | | DESCRIPTION |
|---|---|---|---|---|
| | | Cortex™-A8 | C674x | |
| HDVICP2-0[1] | POMBINTRREQ0 | | | Mailbox interrupt 0 |
| | POMBINTRPEND0 | X | | |
| | POMBINTRREQ1 | | | Mailbox interrupt 1 |
| | POMBINTRPEND1 | | X | |
| | POMBINTRREQ2 | | | Mailbox interrupt 2 |
| | POMBINTRPEND2 | | | |
| | POSYNCINTRREQ0 | | | iCONT1 sync interrupt |
| | POSYNCINTRPEND0 | X | X | |
| | POSYNCINTRREQ1 | | | iCONT2 sync interrupt |
| | POSYNCINTRPEND1 | X | X | |
| HDVICP2-1[1] | POMBINTRREQ0 | | | Mailbox interrupt 0 |
| | POMBINTRPEND0 | X | | |
| | POMBINTRREQ1 | | | Mailbox interrupt 1 |
| | POMBINTRPEND1 | | X | |
| | POMBINTRREQ2 | | | Mailbox interrupt 2 |
| | POMBINTRPEND2 | | | |
| | POSYNCINTRREQ0 | | | iCONT1 sync interrupt |
| | POSYNCINTRPEND0 | X | X | |
| | POSYNCINTRREQ1 | | | iCONT2 sync interrupt |
| | POSYNCINTRPEND1 | X | X | |
| HDVICP2-2[1] | POMBINTRREQ0 | | | Mailbox interrupt 0 |
| | POMBINTRPEND0 | X | | |
| | POMBINTRREQ1 | | | Mailbox interrupt 1 |
| | POMBINTRPEND1 | | X | |
| | POMBINTRREQ2 | | | Mailbox interrupt 2 |
| | POMBINTRPEND2 | | | |
| | POSYNCINTRREQ0 | | | iCONT1 sync interrupt |
| | POSYNCINTRPEND0 | X | X | |
| | POSYNCINTRREQ1 | | | iCONT2 sync interrupt |
| | POSYNCINTRPEND1 | X | X | |
| Serial ATA | INTRQ | | | SATA Module interrupt |
| | INTRQ_PEND_N | X | | |

(1) Three HDVICP2 modules are available on the DM8168 and DM8167 devices; two HDVICP2 modules (HDVICP2-0 and HDVICP2-1) are available on the DM8165 devices.

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**Table 8-18. Interrupts By Module (continued)**

| MODULE | INTERRUPT | DESTINATION | | DESCRIPTION |
|---|---|---|---|---|
| | | Cortex™-A8 | C674x | |
| EMAC SS0 | C0_RX_THRESH_INTR_REQ | | | Receive threshold (non paced) |
| | C0_RX_THRESH_INTR_PEND | X | X | |
| | C0_RX_INTR_REQ | | | Receive pending interrupt (paced) |
| | C0_RX_INTR_PEND | X | X | |
| | C0_TX_INTR_REQ | | | Transmit pending interrupt (paced) |
| | C0_TX_INTR_PEND | X | X | |
| | C0_MISC_INTR_REQ | | | Stat, Host, MDIO LINKINT or MDIO USERINT |
| | C0_MISC_INTR_PEND | X | X | |
| EMAC SS1 | C0_RX_THRESH_INTR_REQ | | | Receive threshold (non paced) |
| | C0_RX_THRESH_INTR_PEND | X | X | |
| | C0_RX_INTR_REQ | | | Receive pending interrupt (paced) |
| | C0_RX_INTR_PEND | X | X | |
| | C0_TX_INTR_REQ | | | Transmit pending interrupt (paced) |
| | C0_TX_INTR_PEND | X | X | |
| | C0_MISC_INTR_REQ | | | Stat, Host, MDIO LINKINT or MDIO USERINT |
| | C0_MISC_INTR_PEND | X | X | |
| USB2.0 SS | USBSS_INTR_REQ | | | Queue MGR or CPPI Completion interrupt |
| | USBSS_INTR_PEND | X | | |
| | USB0_INTR_REQ | | | RX and TX DMA, Endpoint ready or error, or USB2.0 interrupt |
| | USB0_INTR_PEND | X | | |
| | USB1_INTR_REQ | | | |
| | USB1_INTR_PEND | X | | |
| | SLV0P_SWAKEUP | X | | USB wakeup |


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**Table 8-18. Interrupts By Module (continued)**

| MODULE | INTERRUPT | DESTINATION | | DESCRIPTION |
|---|---|---|---|---|
| | | Cortex™-A8 | C674x | |
| PCIe Gen2 | PCIE_INT_I_INTR0 | | | Legacy interrupt (RC mode only) |
| | PCIE_INT_I_INTR_PEND_N0 | X | | |
| | PCIE_INT_I_INTR1 | | | MSI interrupt (RC mode only) |
| | PCIE_INT_I_INTR_PEND_N1 | X | | |
| | PCIE_INT_I_INTR2 | | | Error interrupt |
| | PCIE_INT_I_INTR_PEND_N2 | X | | |
| | PCIE_INT_I_INTR3 | | | Power Management interrupt |
| | PCIE_INT_I_INTR_PEND_N3 | X | | |
| | PCIE_INT_I_INTR4 | | | Reserved |
| | PCIE_INT_I_INTR_PEND_N4 | | | |
| | PCIE_INT_I_INTR5 | | | |
| | PCIE_INT_I_INTR_PEND_N5 | | | |
| | PCIE_INT_I_INTR6 | | | |
| | PCIE_INT_I_INTR_PEND_N6 | | | |
| | PCIE_INT_I_INTR7 | | | |
| | PCIE_INT_I_INTR_PEND_N7 | | | |
| | PCIE_INT_I_INTR8 | | | |
| | PCIE_INT_I_INTR_PEND_N8 | | | |
| | PCIE_INT_I_INTR9 | | | |
| | PCIE_INT_I_INTR_PEND_N9 | | | |
| | PCIE_INT_I_INTR10 | | | |
| | PCIE_INT_I_INTR_PEND_N10 | | | |
| | PCIE_INT_I_INTR11 | | | |
| | PCIE_INT_I_INTR_PEND_N11 | X | | |
| | PCIE_INT_I_INTR12 | | | |
| | PCIE_INT_I_INTR_PEND_N12 | X | | |
| | PCIE_INT_I_INTR13 | | | |
| | PCIE_INT_I_INTR_PEND_N13 | X | | |
| | PCIE_INT_I_INTR14 | | | |
| | PCIE_INT_I_INTR_PEND_N14 | X | | |
| | PCIE_INT_I_INTR15 | | | |
| | PCIE_INT_I_INTR_PEND_N15 | X | | |
| | SLE_IDLEP_SWAKEPUP | X | | PCIe wakeup |

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**Table 8-18. Interrupts By Module (continued)**

| MODULE | INTERRUPT | DESTINATION | | DESCRIPTION |
|---|---|---|---|---|
| | | Cortex™-A8 | C674x | |
| TPCC | TPCC_INT_PO[0] | | | Region 0 DMA completion |
| | TPCC_INT_PEND_N[0] | X | | |
| | TPCC_INT_PO[1] | | | Region 1 DMA completion |
| | TPCC_INT_PEND_N[1] | | X | |
| | TPCC_INT_PO[2] | | | Region 2 DMA completion |
| | TPCC_INT_PEND_N[2] | | | |
| | TPCC_INT_PO[3] | | | Region 3 DMA completion |
| | TPCC_INT_PEND_N[3] | | | |
| | TPCC_INT_PO[4] | | | Region 4 DMA completion |
| | TPCC_INT_PEND_N[4] | | | |
| | TPCC_INT_PO[5] | | | Region 5 DMA completion |
| | TPCC_INT_PEND_N[5] | | | |
| | TPCC_INT_PO[6] | | | Region 6 DMA completion |
| | TPCC_INT_PEND_N[6] | | | |
| | TPCC_INT_PO[7] | | | Region 7 DMA completion |
| | TPCC_INT_PEND_N[7] | | | |
| | TPCC_MPINT_PO | | | Memory protection error |
| | TPCC_MPINT_PEND_N | X | | |
| | TPCC_ERRINT_PO | | | TPCC error |
| | TPCC_ERRINT_PEND_N | X | X | |
| | TPCC_INTG_PO | | | DMA Global completion |
| | TPCC_INTG_PEND_N | | | |
| TPTC 0 | TPTC_ERRINT_PO | | | TPTC0 error |
| | TPTC_LERRINT_PO | X | X | |
| | TPTC_INT_PO | | | TPTC0 completion |
| | TPTC_LINT_PO | | | |
| TPTC 1 | TPTC_ERRINT_PO | | | TPTC1 error |
| | TPTC_LERRINT_PO | X | | |
| | TPTC_INT_PO | | | TPTC1 completion |
| | TPTC_LINT_PO | | | |
| TPTC 2 | TPTC_ERRINT_PO | | | TPTC2 error |
| | TPTC_LERRINT_PO | X | | |
| | TPTC_INT_PO | | | TPTC2 completion |
| | TPTC_LINT_PO | | | |
| TPTC 3 | TPTC_ERRINT_PO | | | TPTC3 error |
| | TPTC_LERRINT_PO | X | | |
| | TPTC_INT_PO | | | TPTC3 completion |
| | TPTC_LINT_PO | | | |
| DDR EMIF4d 0 | SYS_ERR_INTR | | | EMIF error |
| | SYS_ERR_INTR_PEND_N | X | | |
| DDR EMIF4d 1 | SYS_ERR_INTR | | | |
| | SYS_ERR_INTR_PEND_N | X | | |
| GPMC | GPMC_SINTERRUPT | X | | GPMC interrupt |
| UART 0 | NIRQ | X | X | UART and IrDA 0 interrupt |
| UART 1 | NIRQ | X | X | UART and IrDA 1 interrupt |
| UART 2 | NIRQ | X | X | UART and IrDA 2 interrupt |
| Timer1 | POINTR_REQ | | | 32-bit Timer1 interrupt |
| | POINTR_PEND | X | X | |
| Timer2 | POINTR_REQ | | | 32-bit Timer2 interrupt |
| | POINTR_PEND | X | X | |


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**Table 8-18. Interrupts By Module (continued)**

| MODULE | INTERRUPT | DESTINATION | | DESCRIPTION |
|---|---|---|---|---|
| | | Cortex™-A8 | C674x | |
| Timer3 | POINTR_REQ | | | 32-bit Timer3 interrupt |
| | POINTR_PEND | X | X | |
| Timer4 | POINTR_REQ | | | 32-bit Timer4 interrupt |
| | POINTR_PEND | X | X | |
| Timer5 | POINTR_REQ | | | 32-bit Timer5 interrupt |
| | POINTR_PEND | X | X | |
| Timer6 | POINTR_REQ | | | 32-bit Timer6 interrupt |
| | POINTR_PEND | X | X | |
| Timer7 | POINTR_REQ | | | 32-bit Timer7 interrupt |
| | POINTR_PEND | X | X | |
| WDTimer1 | PO_INT_REQ | X | X | Watchdog Timer |
| I2C0 | POINTRREQ | | | I2C Bus interrupt |
| | POINTRPEND | X | X | |
| I2C1 | POINTRREQ | | | |
| | POINTRPEND | X | X | |
| SPI | SINTERRUPTN | X | X | SPI Interrupt |
| SDIO | IRQOQN | X | X | SDIO interrupt |
| McASP 0 | MCASP_X_INTR_REQ | | | McASP 0 Transmit interrupt |
| | MCASP_X_INTR_PEND | X | X | |
| | MCASP_R_INTR_REQ | | | McASP 0 Receive interrupt |
| | MCASP_R_INTR_PEND | X | X | |
| McASP 1 | MCASP_X_INTR_REQ | | | McASP 1 Transmit interrupt |
| | MCASP_X_INTR_PEND | X | X | |
| | MCASP_R_INTR_REQ | | | McASP 1 Receive interrupt |
| | MCASP_R_INTR_PEND | X | X | |
| McASP 2 | MCASP_X_INTR_REQ | | | McASP 2 Transmit interrupt |
| | MCASP_X_INTR_PEND | X | X | |
| | MCASP_R_INTR_REQ | | | McASP 2 Receive interrupt |
| | MCASP_R_INTR_PEND | X | X | |
| McBSP | PORRINTERRUPT | | | McBSP Receive Int (legacy mode) |
| | PORXINTERRUPT | | | McBSP Transmit Int (legacy mode) |
| | PORROVFLINTERRUPT | | | McBSP Receive Overflow Int (legacy mode) |
| | PORCOMMONIRQ | X | X | McBSP Common Int |
| RTC | TIMER_INTR_REQ | | | Timer interrupt |
| | TIMER_INTR_PEND | X | | |
| | ALARM_INTR_REQ | | | Alarm interrupt |
| | ALARM_INTR_PEND | X | | |
| GPIO 0 | POINTRREQ1 | | | GPIO 0 interrupt 1 |
| | POINTRPEND1 | X | X | |
| | POINTRREQ2 | | | GPIO 0 interrupt 2 |
| | POINTRPEND2 | X | X | |
| GPIO 1 | POINTRREQ1 | | | GPIO 1 interrupt 1 |
| | POINTRPEND1 | X | X | |
| | POINTRREQ2 | | | GPIO 1 interrupt 2 |
| | POINTRPEND2 | X | X | |
| PRCM | | | | Reserved |

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**Table 8-18. Interrupts By Module (continued)**

| MODULE | INTERRUPT | DESTINATION | | DESCRIPTION |
|---|---|---|---|---|
| | | Cortex™-A8 | C674x | |
| HDVPSS | INTR0_INTR | | | Intr0 pulse version |
| | INTR0_INTR_PEND_N | X | | Intr0 level version |
| | INTR1_INTR | | | Intr1 pulse version |
| | INTR1_INTR_PEND_N | | X | Intr1 level version |
| | INTR2_INTR | | | Intr2 pulse version |
| | INTR2_INTR_PEND_N | | | Intr2 level version |
| | INTR3_INTR | | | Intr3 pulse version |
| | INTR3_INTR_PEND_N | | | Intr3 level version |
| SGX530 (DM8168 only) | THALIAIRQ | X | | Error in the IMG bus |
| | TARGETSINTERRUPT | | | Target slave error interrupt |
| | INITMINTERRUPT | | | Initiator master error interrupt |
| HDMI 1.3 Transmit | INTR0_INTR | | | Intr0 pulse version |
| | INTR0_INTR_PEND_N | X | X | Intr0 level version |
| SmartReflex0 | INTRREQ | | | SVT SmartReflex interrupt pulse version |
| | INTRPEND | X | | SVT SmartReflex interrupt level version |
| SmartReflex1 | INTRREQ | | | HVT SmartReflex interrupt pulse version |
| | INTRPEND | X | | HVT SmartReflex interrupt level version |
| PBIST | | | | Reserved |
| Mailbox | MAIL_U0_IRQ | X | | Mailbox interrupt |
| | MAIL_U1_IRQ | | X | |
| | MAIL_U2_IRQ | | | |
| | MAIL_U3_IRQ | | | |
| NMI | NMI_INT | X | | NMI Interrupt |
| Infrastructure | L3_DBG_IRQ | X | | L3 debug error |
| | L3_APP_IRQ | X | | L3 application error |
| System MMU | MMU_INTR | X | | Table walk abort |
| DMM | DMM_HIGH_INTRPEND | X | | PAT fault |
| Cortex™-A8 SS | COMMTX | X | | ARM ICECrusher interrupt |
| | COMMRX | X | | |
| | BENCH | X | | ARM NPMUIRQ |
| | ELM_IRQ | X | | Error Location process completion |
| | EMUINT | X | | E2ICE interrupt |
| C674x (Int Ctrl) | EVT0 | | X | C674x Internal |
| | EVT1 | | X | |
| | EVT2 | | X | |
| | EVT3 | | X | |
| | INTERR | | X | |
| C674x (ECM) | EMU_DTDMA | | X | |
| C674x (RTDX) | EMU_RTDXRX | | X | |
| | EMU_RTDXTX | | X | |
| C674x (EMC) | IDMAINT0 | | X | |
| | IDMAINT1 | | X | |
| | EMC_IDMAERR | | X | |
| C674x (PBIST) | PBISTINT | | X | |
| C674x (EFI A) | EFIINTA | | X | |
| C674x (EFI B) | EFIINTB | | X | |
| C674x (PMC) | PMC_ED | | X | |
| C674x (UMC) | UMC_ED1 | | X | |
| | UMC_ED2 | | X | |
| C674x (PDC) | PDC_INT | | X | |


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**Table 8-18. Interrupts By Module (continued)**

| MODULE | INTERRUPT | DESTINATION | | DESCRIPTION |
|---|---|---|---|---|
| | | Cortex™-A8 | C674x | |
| SYS | SYS_CMPA | | X | Sys |
| C674x (PMC) | PMC_CMPA | | X | C674x Internal |
| | PMC_DMPA | | X | |
| C674x (DMC) | DMC_CMPA | | X | |
| | DMC_DMPA | | X | |
| C674x (UMC) | UMC_CMPA | | X | |
| | UMC_DMPA | | X | |
| C674x (EMC) | EMC_CMPA | | X | |
| | EMC_BUSERR | | X | |

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### 8.4.2 Cortex™-A8 Interrupts

The Cortex™-A8 Interrupt Controller (AINTC) takes ARM device interrupts and maps them to either the interrupt request (IRQ) or fast interrupt request (FIQ) of the ARM with an individual priority level. The AINTC interrupts must be active low-level interrupts.

The AINTC is responsible for prioritizing all service requests from the system peripherals directed to the Cortex™-A8 SS and generating either nIRQ or nFIQ to the host. The type of the interrupt (nIRQ or nFIQ) and the priority of the interrupt inputs are programmable. It has the capability to handle up to 128 requests which can be steered or prioritized as nFIQ or nIRQ interrupt requests.

The general features of the AINTC are:

- Up to 128 level-sensitive interrupts inputs
- Individual priority for each interrupt input
- Each interrupt can be steered to nFIQ or nIRQ
- Independent priority sorting for nFIQ and nIRQ.

**Table 8-19. Cortex™-A8 Interrupt Controller Connections**

| INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 0 | EMUINT | Internal |
| 1 | COMMTX | Internal |
| 2 | COMMRX | Internal |
| 3 | BENCH | Internal |
| 4 | ELM_IRQ | ELM |
| 5-6 | - | |
| 7 | NMI | External Pin |
| 8 | - | |
| 9 | L3DEBUG | L3 |
| 10 | L3APPINT | L3 |
| 11 | - | |
| 12 | EDMACOMPINT | TPCC |
| 13 | EDMAMPERR | TPCC |
| 14 | EDMAERRINT | TPCC |
| 15 | - | |
| 16 | SATAINT | SATA |
| 17 | USBSSINT | USBSS |
| 18 | USBINT0 | USBSS |
| 19 | USBINT1 | USBSS |
| 20-33 | - | |
| 34 | USBWAKEUP | USBSS |
| 35 | PCIeWAKEUP | PCIe |
| 36 | DSSINT | HDVPSS |
| 37 | GFXINT | SGX530 (DM8168 only) |
| 38 | HDMIINT | HDMI |
| 39 | - | |
| 40 | MACRXTHR0 | EMAC0 |
| 41 | MACRXINT0 | EMAC0 |
| 42 | MACTXINT0 | EMAC0 |
| 43 | MACMISC0 | EMAC0 |


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**Table 8-19. Cortex™-A8 Interrupt Controller Connections (continued)**

| INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 44 | MACRXTHR1 | EMAC1 |
| 45 | MACRXINT1 | EMAC1 |
| 46 | MACTXINT1 | EMAC1 |
| 47 | MACMISC1 | EMAC1 |
| 48 | PCIINT0 | PCIe |
| 49 | PCIINT1 | PCIe |
| 50 | PCIINT2 | PCIe |
| 51 | PCIINT3 | PCIe |
| 52-63 | - | |
| 64 | SDINT | SD, SDIO |
| 65 | SPIINT | SPI |
| 66 | - | |
| 67 | TINT1 | Timer1 |
| 68 | TINT2 | Timer2 |
| 69 | TINT3 | Timer3 |
| 70 | I2CINT0 | I2C0 |
| 71 | I2CINT1 | I2C1 |
| 72 | UARTINT0 | UART0 |
| 73 | UARTINT1 | UART1 |
| 74 | UARTINT2 | UART2 |
| 75 | RTCINT | RTC |
| 76 | RTCALARMINT | RTC |
| 77 | MBINT | Mailbox |
| 78-79 | - | |
| 80 | MCATXINT0 | McASP0 |
| 81 | MCARXINT0 | McASP0 |
| 82 | MCATXINT1 | McASP1 |
| 83 | MCARXINT1 | McASP1 |
| 84 | MCATXINT2 | McASP2 |
| 85 | MCARXINT2 | McASP2 |
| 86 | MCBSPINT | McBSP |
| 87-90 | - | |
| 91 | WDTINT | WDTIMER1 |
| 92 | TINT4 | Timer4 |
| 93 | TINT5 | Timer5 |
| 94 | TINT6 | Timer6 |
| 95 | TINT7 | Timer7 |
| 96 | GPIOINT0A | GPIO 0 |
| 97 | GPIOINT0B | GPIO 0 |
| 98 | GPIOINT1A | GPIO 1 |
| 99 | GPIOINT1B | GPIO 1 |
| 100 | GPMCINT | GPMC |
| 101 | DDRERR0 | DDR EMIF0 |
| 102 | DDRERR1 | DDR EMIF1 |
| 103 | HDVICP0CONT1SYNC | HDVICP2-0 |
| 104 | HDVICP0CONT2SYNC | HDVICP2-0 |
| 105 | HDVICP1CONT1SYNC | HDVICP2-1 |

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**Table 8-19. Cortex™-A8 Interrupt Controller Connections (continued)**

| INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 106 | HDVICP1CONT2SYNC | HDVICP2-1 |
| 107 | HDVICP0MBOXINT | HDVICP2-0 |
| 108 | HDVICP1MBOXINT | HDVICP2-1 |
| 109 | HDVICP2MBOXINT | HDVICP2-2 |
| 110 | HDVICP2CONT1SYNC | HDVICP2-2 |
| 111 | HDVICP2CONT2SYNC | HDVICP2-2 |
| 112 | TCERRINT0 | TPTC0 |
| 113 | TCERRINT1 | TPTC1 |
| 114 | TCERRINT2 | TPTC2 |
| 115 | TCERRINT3 | TPTC3 |
| 116-119 | - | |
| 120 | SMRFLX0 | SmartReflex0 |
| 121 | SMRFLX1 | SmartReflex1 |
| 122 | SYSMMUINT | System MMU |
| 123 | - | |
| 124 | DMMINT | DMM |
| 125-127 | - | |

### 8.4.3 C674x Interrupts

The C674x DSP interrupt controller is contained within the C674x module itself. This controller includes an event combiner, interrupt selector, exception combiner, and advanced event generator which allow a large number of system interrupts to be routed to its 12 maskable interrupts, grouped together for an exception input or used as an event trigger.

The controller combines device events into 12 CPU interrupts. It also controls the generation of the CPU exception and emulation interrupts and the generation of AEG events. The C674x interrupt controller captures all events on the rising-edge. (C674x interrupt inputs must be active high pulse interrupts.) On the device, only the level interrupts of the IP blocks are used and are converted into pulse interrupts by chip-level logic before connection to the C674x interrupt inputs.

Within the C674x interrupt controller, the interrupt selector contains registers that allow the user to program the source for each of 12 CPU interrupts. Some of the event sources come from within the C674x module itself.

Table 8-20 shows the connection of device interrupts to the C674x. Shaded entries are hard coded within the C674x module and cannot be changed.

**Table 8-20. C674x Interrupt Controller Connections(1)**

| INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 0 | EVT0 | C674x (INTC) |
| 1 | EVT1 | C674x (INTC) |
| 2 | EVT2 | C674x (INTC) |
| 3 | EVT3 | C674x (INTC) |
| 4-8 | - | |
| 9 | EMU_DTDMA | C674x (ECM) |
| 10 | Reserved | C674x |
| 11 | EMU_RTDXRX | C674x (RTDX) |

(1) Shaded interrupts are reserved for C674x internal use.


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**Table 8-20. C674x Interrupt Controller Connections[(1)] (continued)**

| INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 12 | EMU_RTDXTX | C674x (RTDX) |
| 13 | IDMAINT0 | C674x (EMC) |
| 14 | IDMAINT1 | C674x (EMC) |
| 15 | SDINT | SD, SDIO |
| 16 | SPIINT | SPI |
| 17-19 | - | |
| 20 | EDMAINT | TPCC |
| 21 | EDMAERRINT | TPCC |
| 22 | TCERRINT0 | TPTC0 |
| 23-31 | - | |
| 32 | MACRXTHR0 | EMAC0 |
| 33 | MACRXINT0 | EMAC0 |
| 34 | MACTXINT0 | EMAC0 |
| 35 | MACMISC0 | EMAC0 |
| 36 | MACRXTHR1 | EMAC1 |
| 37 | MACRXINT1 | EMAC1 |
| 38 | MACTXINT1 | EMAC1 |
| 39 | MACMISC1 | EMAC1 |
| 40 | DSSINT | HDVPSS |
| 41 | HDMIINT | HDMI |
| 42-46 | - | |
| 47 | WDTINT | WDTIMER1 |
| 48 | - | |
| 49 | TINT1 | Timer1 |
| 50 | TINT2 | Timer2 |
| 51 | TINT3 | Timer3 |
| 52 | TINT4 | Timer4 |
| 53 | TINT5 | Timer5 |
| 54 | TINT6 | Timer6 |
| 55 | TINT7 | Timer7 |
| 56 | MBINT | Mailbox |
| 57 | - | |
| 58 | I2CINT0 | I2C0 |
| 59 | I2CINT1 | I2C1 |
| 60 | UARTINT0 | UART0 |
| 61 | UARTINT1 | UART1 |
| 62 | UARTINT2 | UART2 |
| 63 | - | |
| 64 | GPIOINT0A | GPIO 0 |
| 65 | GPIOINT0B | GPIO 0 |
| 66 | GPIOINT1A | GPIO 1 |
| 67 | GPIOINT1B | GPIO 1 |
| 68-69 | - | |
| 70 | MCATXINT0 | McASP0 |
| 71 | MCARXINT0 | McASP0 |
| 72 | MCATXINT1 | McASP1 |
| 73 | MCARXINT1 | McASP1 |

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**Table 8-20. C674x Interrupt Controller Connections[(1)] (continued)**

| INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 74 | MCATXINT2 | McASP2 |
| 75 | MCARXINT2 | McASP2 |
| 76 | MCBSPINT | McBSP |
| 77-86 | - | |
| 87 | HDVICP2CONT1SYNC | HDVICP2-2 |
| 88 | HDVICP2CONT2SYNC | HDVICP2-2 |
| 89 | HDVICP2MBOXINT | HDVICP2-2 |
| 90 | HDVICP0CONT1SYNC | HDVICP2-0 |
| 91 | HDVICP0CONT2SYNC | HDVICP2-0 |
| 92 | HDVICP1CONT1SYNC | HDVICP2-1 |
| 93 | HDVICP1CONT2SYNC | HDVICP2-1 |
| 94 | HDVICP0MBOXINT | HDVICP2-0 |
| 95 | HDVICP1MBOXINT | HDVICP2-1 |
| 96 | INTERR | C674x (INTC) |
| 97 | EMC_IDMAERR | C674x (EMC) |
| 98 | PBISTINT | C674x (PBIST) |
| 99 | Reserved | C674x |
| 100 | EFIINTA | C674x (EFI A) |
| 101 | EFIINTB | C674x (EFI B) |
| 102-112 | Reserved | C674x |
| 113 | PMC_ED | C674x (PMC) |
| 114-115 | Reserved | C674x |
| 116 | UMC_ED1 | C674x (UMC) |
| 117 | UMC_ED2 | C674x (UMC) |
| 118 | PDC_INT | C674x (PDC) |
| 119 | SYS_CMPA | SYS |
| 120 | PMC_CMPA | C674x (PMC) |
| 121 | PMC_DMPA | C674x (PMC) |
| 122 | DMC_CMPA | C674x (DMC) |
| 123 | DMC_DMPA | C674x (DMC) |
| 124 | UMC_CMPA | C674x (UMC) |
| 125 | UMC_DMPA | C674x (UMC) |
| 126 | EMC_CMPA | C674x (EMC) |
| 127 | EMC_BUSERR | C674x (EMC) |


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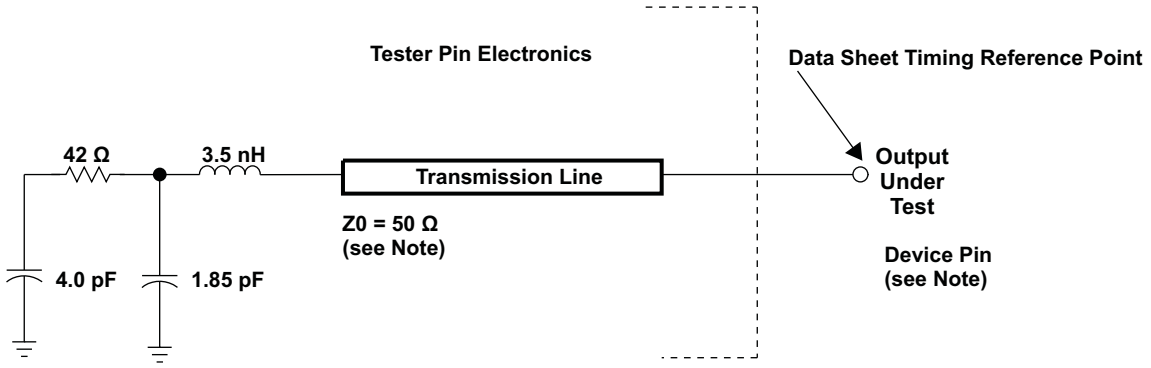
# 9 Peripheral Information and Timings

## 9.1 Parameter Information




NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

**Figure 9-1. Test Load Circuit for AC Timing Measurements**

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

### *9.1.1 1.8-V and 3.3-V Signal Transition Levels*

All input and output timing parameters are referenced to $V_{ref}$ for both "0" and "1" logic levels. For 3.3-V IO, $V_{ref}$ = 1.5 V. For 1.8-V IO, $V_{ref}$ = 0.9 V.

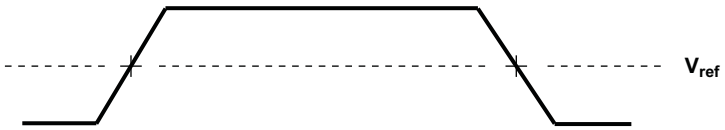



**Figure 9-2. Input and Output Voltage Reference Levels for AC Timing Measurements**

All rise and fall transition timing parameters are referenced to $V_{IL}$ MAX and $V_{IH}$ MIN for input clocks, $V_{OL}$ MAX and $V_{OH}$ MIN for output clocks.

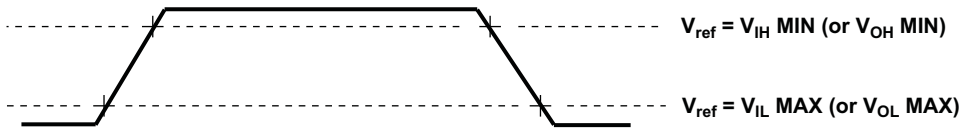



**Figure 9-3. Rise and Fall Transition Time Voltage Reference Levels**

### *9.1.2 3.3-V Signal Transition Rates*

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V per ns).

### 9.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing or decreasing such delays. TI recommends utilizing the available IO buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

For the DDR2 and DDR3, PCIe, SATA, USB, and HDMI interfaces, IBIS models are not used for timing specification. TI provides, in this document, a PCB routing rule solution for each interface that describes the routing rules used to ensure the interface timings are met. Video DAC guidelines (Section 9.10.2) are also included to discuss important layout considerations.

## 9.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.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## 9.3 DDR2 and DDR3 Memory Controller

The device has a dedicated interface to DDR3 and DDR2 SDRAM. It supports JEDEC standard-compliant DDR2 and DDR3 SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: 64Mb, 128Mb, 256Mb, 512Mb, 1Gb, 2Gb and 4Gb (x16-bit only) devices
- Support for two independent chip selects, with their corresponding register sets, and independent page tracking
- Two interfaces with associated DDR2 and DDR3 PHYs
- Dynamic memory manager allows for interleaving of data between the two DDR interfaces.

For details on the DDR2 and DDR3 Memory Controller, see the DDR2 and DDR3 Memory Controller chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### *9.3.1 DDR2 Routing Specifications*

#### 9.3.1.1 Board Designs

TI only supports board designs that follow the specifications outlined in this document. The switching characteristics and the timing diagram for the DDR2 memory controller are shown in Table 9-1 and Figure 9-4.

**Table 9-1. Switching Characteristics Over Recommended Operating Conditions for DDR2 Memory Controller**

| NO. | PARAMETER | | -1G | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(DDR_CLK)}$ | Cycle time, DDR_CLK | 2.5 | 8 | ns |

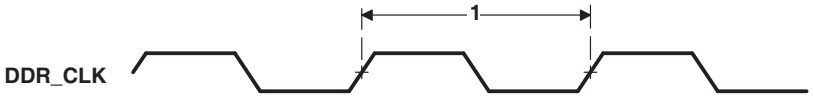


**Figure 9-4. DDR2 Memory Controller Clock Timing**

#### 9.3.1.2 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR2 specification, see *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* Application Report (SPRAAV0).

#### 9.3.1.2.1 DDR2 Interface Schematic

Figure 9-5 shows the DDR2 interface schematic for a x32 DDR2 memory system. In Figure 9-6 the x16 DDR2 system schematic is identical except that the high-word DDR2 device is deleted.

When not using a DDR2 interface, the proper method of handling the unused pins is to tie off the DQS pins by pulling the non-inverting DQS pin to the DDR_1V8 supply via a 1k-Ω resistor and pulling the inverting $\overline{\text{DQS}}$ pin to ground via a 1k-Ω resistor. This needs to be done for each byte not used. Also, include the 50-Ω pulldown for DDR[x]_VTP. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32 bits wide, 16 bits wide, or not used.


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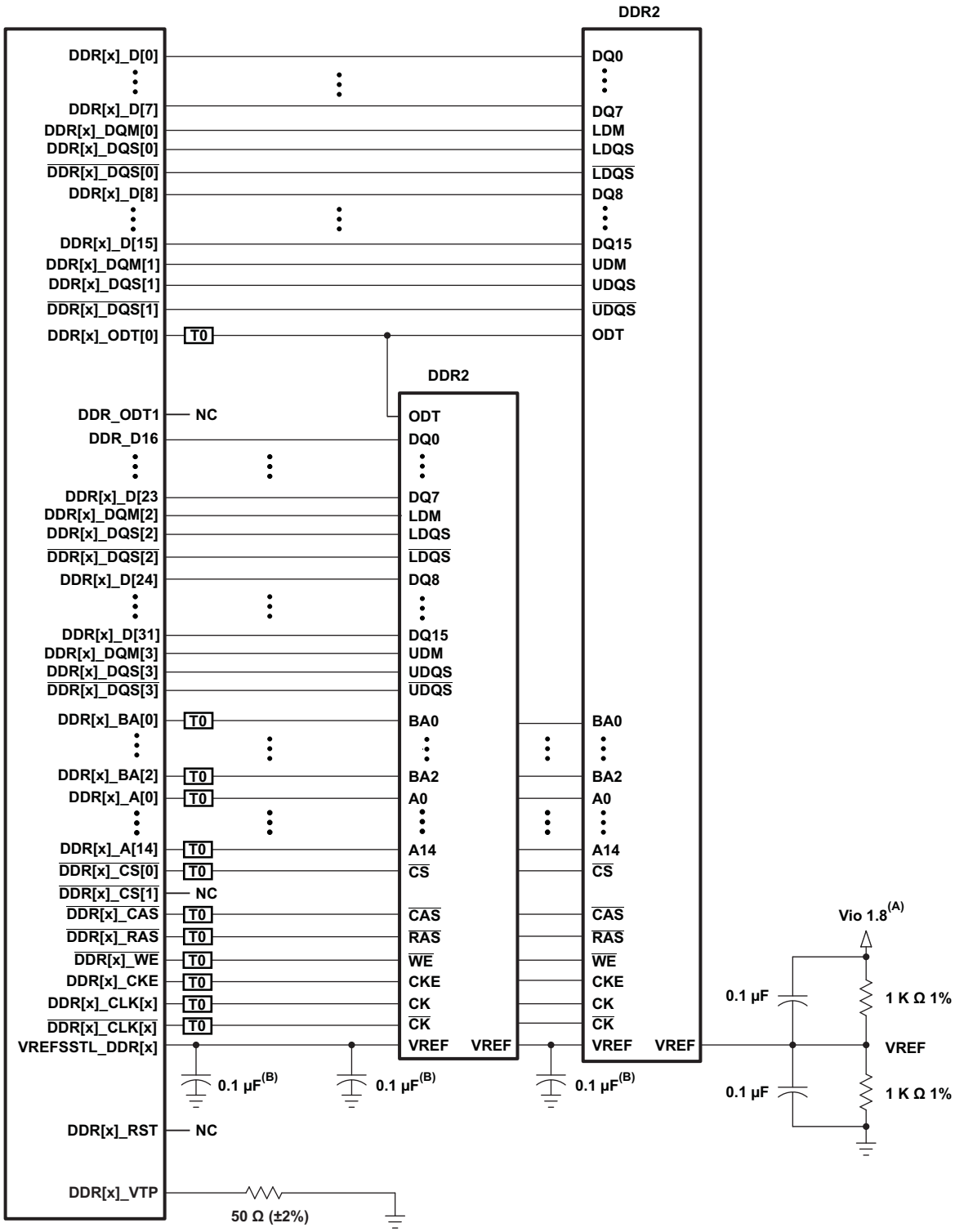
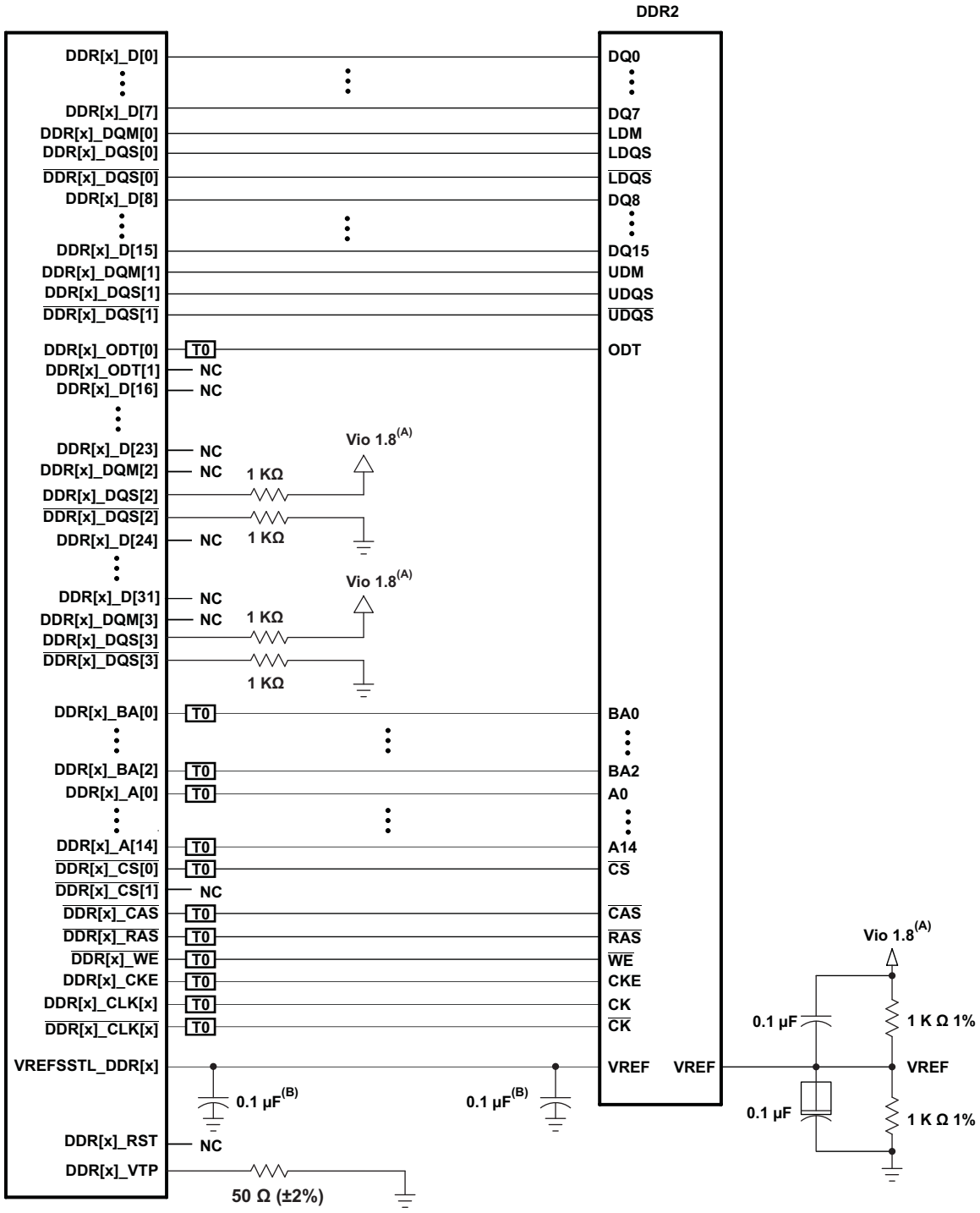



T0 Termination is required. See terminator comments.

A. Vio1.8 is the power supply for the DDR2 memories and the DM816x DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

**Figure 9-5. 32-Bit DDR2 High-Level Schematic**




T0 Termination is required. See terminator comments.

A. Vio1.8 is the power supply for the DDR2 memories and the DM816x DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

**Figure 9-6. 16-Bit DDR2 High-Level Schematic**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#### 9.3.1.2.2 Compatible JEDEC DDR2 Devices

Table 9-2 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-800 speed grade DDR2 devices.

**Table 9-2. Compatible JEDEC DDR2 Devices**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | JEDEC DDR2 device speed grade(1) | DDR2-800 | | |
| 2 | JEDEC DDR2 device bit width | x16 | x16 | Bits |
| 3 | JEDEC DDR2 device count(2) | 1 | 2 | Devices |
| 4 | JEDEC DDR2 device ball count(3) | 84 | 92 | Balls |

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
(2) One DDR2 device is used for a 16-bit DDR2 memory system. Two DDR2 devices are used for a 32-bit DDR2 memory system.
(3) The 92-ball devices are retained for legacy support. New designs will migrate to 84-ball DDR2 devices. Electrically, the 92- and 84-ball DDR2 devices are the same.

#### 9.3.1.2.3 PCB Stackup

The minimum stackup required for routing the DM816x device is a six-layer stackup as shown in Table 9-3. Additional layers may be added to the PCB stackup to accommodate other circuitry or to reduce the size of the PCB footprint.

**Table 9-3. Minimum PCB Stackup**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top routing mostly horizontal |
| 2 | Plane | Ground |
| 3 | Plane | Power |
| 4 | Signal | Internal routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom routing mostly vertical |

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Complete stackup specifications are provided in Table 9-4.

**Table 9-4. PCB Stackup Specifications**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | PCB routing and plane layers | 6 | | | |
| 2 | Signal routing layers | 3 | | | |
| 3 | Full ground layers under DDR2 routing region | 2 | | | |
| 4 | Number of ground plane cuts allowed within DDR routing region | | | 0 | |
| 5 | Number of ground reference planes required for each DDR2 routing layer | 1 | | | |
| 6 | Number of layers between DDR2 routing layer and reference ground plane | | | 0 | |
| 7 | PCB routing feature size | | 4 | | Mils |
| 8 | PCB trace width, w | | 4 | | Mils |
| 9 | PCB BGA escape via pad size(1) | | 18 | 20 | Mils |
| 10 | PCB BGA escape via hole size(1) | | 10 | | Mils |
| 11 | Processor BGA pad size | | 0.3 | | mm |
| 12 | DDR2 device BGA pad size(2) | | | | |
| 13 | Single-ended impedance, Zo | 50 | | 75 | Ω |
| 14 | Impedance control(3) | Z-5 | Z | Z+5 | Ω |

(1) A 20/10 via may be used if enough power routing resources are available. An 18/10 via allows for more flexible power routing to the processor.
(2) For the DDR2 device BGA pad size, see the DDR2 device manufacturer documentation.
(3) Z is the nominal singled-ended impedance selected for the PCB specified by item 13.


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#### 9.3.1.2.4 Placement

Figure 9-7 shows the required placement for the processor as well as the DDR2 devices. The dimensions for this figure are defined in Table 9-5. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR2 device is omitted from the placement.

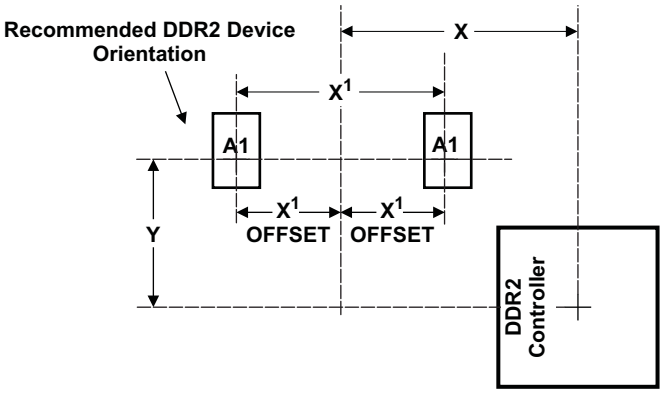


**Figure 9-7. DM816x Device and DDR2 Device Placement**

**Table 9-5. Placement Specifications**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | X + Y (1) (2) | | 1660 | Mils |
| 2 | X' (1) (2) | | 1280 | Mils |
| 3 | X' Offset (1) (2) (3) | | 650 | Mils |
| 4 | DDR2 keepout region (4) | | | |
| 5 | Clearance from non-DDR2 signal to DDR2 keepout region (5) | 4 | | w |

(1) For dimension definitions, see Figure 9-5.
(2) Measurements from center of processor to center of DDR2 device.
(3) For 16-bit memory systems, it is recommended that X' offset be as small as possible.
(4) DDR2 keepout region to encompass entire DDR2 routing area.
(5) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

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#### 9.3.1.2.5 DDR2 Keepout Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keepout region is defined for this purpose and is shown in Figure 9-8. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 9-5.

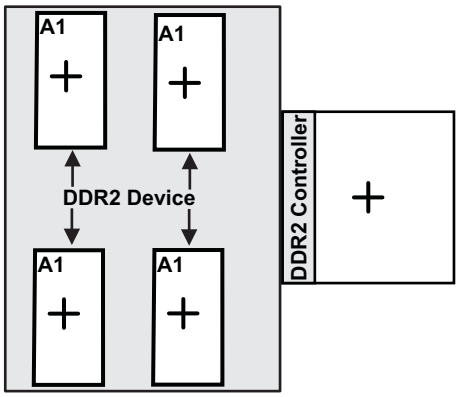


**Figure 9-8. DDR2 Keepout Region**

**NOTE**

The region shown in should encompass all the DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keepout region. Non-DDR2 signals may be routed in the region, provided t hey are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8V power plane should cover the entire keepout region. Routes for the two DDR interfaces must be separated by at least 4x; the more separation, the better.

#### 9.3.1.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 9-6 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR2 interfaces and DDR2 device. Additional bulk bypass capacitance may be needed for other circuitry.

**Table 9-6. Bulk Bypass Capacitors**

| No. | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 1 | DVDD18 bulk bypass capacitor count(1) | 6 | | Devices |
| 2 | DVDD18 bulk bypass total capacitance | 60 | | µF |
| 3 | DDR#1 bulk bypass capacitor count(1) | 1 | | Devices |
| 4 | DDR#1 bulk bypass total capacitance(1) | 10 | | µF |
| 5 | DDR#2 bulk bypass capacitor count(2) | 1 | | Devices |
| 6 | DDR#2 bulk bypass total capacitance(1)(2) | 10 | | µF |

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors. Use half of these capacitors for DDR[0] and half for DDR[1].
(2) Only used on 32-bit wide DDR2 memory systems.


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#### 9.3.1.2.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor DDR power, and processor DDR ground connections. Table 9-7 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

**Table 9-7. High-Speed Bypass Capacitors**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | HS bypass capacitor package size(1) | | 0402 | 10 Mils |
| 2 | Distance from HS bypass capacitor to device being bypassed | | 250 | Mils |
| 3 | Number of connection vias for each HS bypass capacitor(2) | 2 | | Vias |
| 4 | Trace length from bypass capacitor contact to connection via | 1 | 30 | Mils |
| 5 | Number of connection vias for each processor power and ground ball | 1 | | Vias |
| 6 | Trace length from processor power and ground ball to connection via | | 35 | Mils |
| 7 | Number of connection vias for each DDR2 device power and ground ball | 1 | | Vias |
| 8 | Trace length from DDR2 device power and ground ball to connection via | | 35 | Mils |
| 9 | DVDD18 HS bypass capacitor count(3)(4) | 40 | | Devices |
| 10 | DVDD18 HS bypass capacitor total capacitance(4) | 2.4 | | µF |
| 11 | DDR device HS bypass capacitor count(3)(5) | 8 | | Devices |
| 12 | DDR device HS bypass capacitor total capacitance(5) | 0.4 | | µF |

(1) LxW, 10-mil units; for example, a 0402 is a 40x20-mil surface-mount capacitor.
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) Use half of these capacitors for DDR[0] and half for DDR[1].
(5) Per DDR device.

#### 9.3.1.2.8 Net Classes

Table 9-8 lists the clock net classes for the DDR2 interface. Table 9-9 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

**Table 9-8. Clock Net Class Definitions**

| CLOCK NET CLASS | PROCESSOR PIN NAMES |
|---|---|
| CK | DDR[x]_CLK[x] and $\overline{\text{DDR[x]_CLK[x]}}$ |
| DQS0 | DDR[x]_DQS[0] and $\overline{\text{DDR[x]_DQS[0]}}$ |
| DQS1 | DDR[x]_DQS[1] and $\overline{\text{DDR[x]_DQS[1]}}$ |
| DQS2(1) | DDR[x]_DQS[2] and $\overline{\text{DDR[x]_DQS[2]}}$ |
| DQS3(1) | DDR[x]_DQS[3] and $\overline{\text{DDR[x]_DQS[3]}}$ |

(1) Only used on 32-bit wide DDR2 memory systems.

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**Table 9-9. Signal Net Class Definitions**

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | PROCESSOR PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | DDR[x]_BA[2:0], DDR[x]_A[14:0], DDR[x]_CS[x], DDR[x]_CAS, DDR[x]_RAS, DDR[x]_WE, DDR[x]_CKE, DDR[x]_ODT[x] |
| DQ0 | DQS0 | DDR[x]_D[7:0], DDR[x]_DQM[0] |
| DQ1 | DQS1 | DDR[x]_D[15:8], DDR[x]_DQM[1] |
| DQ2 (1) | DQS2 | DDR[x]_D[23:16], DDR[x]_DQM[2] |
| DQ3 (1) | DQS3 | DDR[x]_D[31:24], DDR[x]_DQM[3] |

(1) Only used on 32-bit wide DDR2 memory systems.

#### 9.3.1.2.9 DDR2 Signal Termination

Signal terminators are required in CK and ADDR_CTRL net classes. Serial terminators may be used on data lines to reduce EMI risk; however, serial terminations are the only type permitted. ODT's are integrated on the data byte net classes. They should be enabled to ensure signal integrity.Table 9-10 shows the specifications for the series terminators.

**Table 9-10. DDR2 Signal Terminations**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | CK net class (1) (2) | 0 | | 10 | Ω |
| 2 | ADDR_CTRL net class (1) (3) (4) (2) | 0 | 22 | Zo | Ω |
| 3 | Data byte net classes (DQS0-DQS3, DQ0-DQ3) (5) | 0 | | 0 | Ω |

(1) Only series termination is permitted, parallel or SST specifically disallowed on board.
(2) Only required for EMI reduction.
(3) Terminator values larger than typical only recommended to address EMI issues.
(4) Termination value should be uniform across net class.
(5) No external terminations allowed for data byte net classes. ODT is to be used.

#### 9.3.1.2.10 VREFSSTL_DDR Routing

VREFSSTL_DDR is used as a reference by the input buffers of the DDR2 memories as well as the processor. VREF is intended to be half the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 9-6. Other methods of creating VREF are not recommended. Figure 9-9 shows the layout guidelines for VREF.

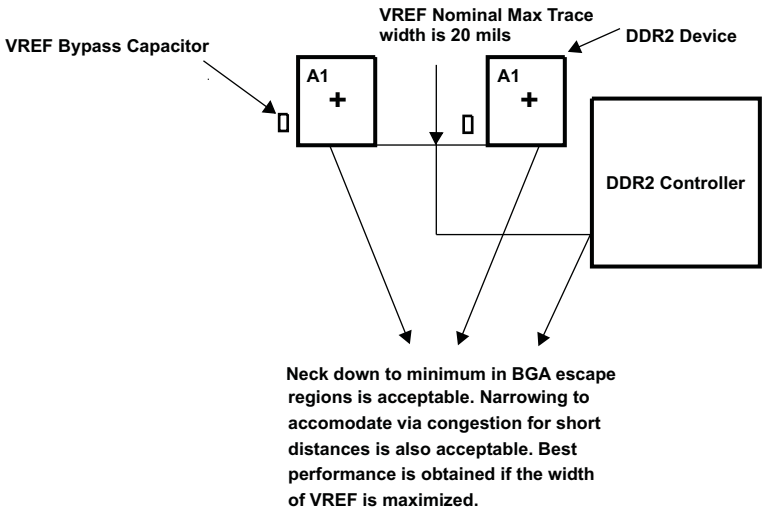


**Figure 9-9. VREF Routing and Topology**


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### 9.3.1.3 DDR2 CK and ADDR_CTRL Routing

Figure 9-10 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A (A'+A") should be maximized.

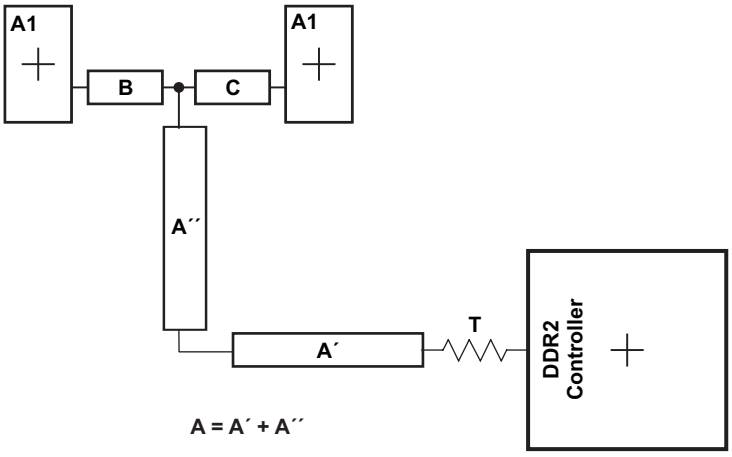


**Figure 9-10. CK and ADDR_CTRL Routing and Topology**

**Table 9-11. CK and ADDR_CTRL Routing Specification (1)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | Center-to-center CK-$\overline{CK}$ spacing | | | 2w | |
| 2 | CK and $\overline{CK}$ skew(1) | | | 25 | Mils |
| 3 | CK B-to-C skew length mismatch | | | 25 | Mils |
| 4 | Center-to-center CK to other DDR2 trace spacing(2) | 4w | | | |
| 5 | CK and ADDR_CTRL nominal trace length(3) | CACLM-50 | CACLM | CACLM+50 | Mils |
| 6 | ADDR_CTRL-to-CK skew length mismatch | | | 100 | Mils |
| 7 | ADDR_CTRL-to-ADDR_CTRL skew length mismatch | | | 100 | Mils |
| 8 | Center-to-center ADDR_CTRL to other DDR2 trace spacing(2) | 4w | | | |
| 9 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(2) | 3w | | | |
| 10 | ADDR_CTRL B-to-C skew length mismatch | | | 100 | Mils |

(1) The length of segment A=A'+A″ as shown in Figure 9-10.
(2) Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(3) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

Figure 9-11 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

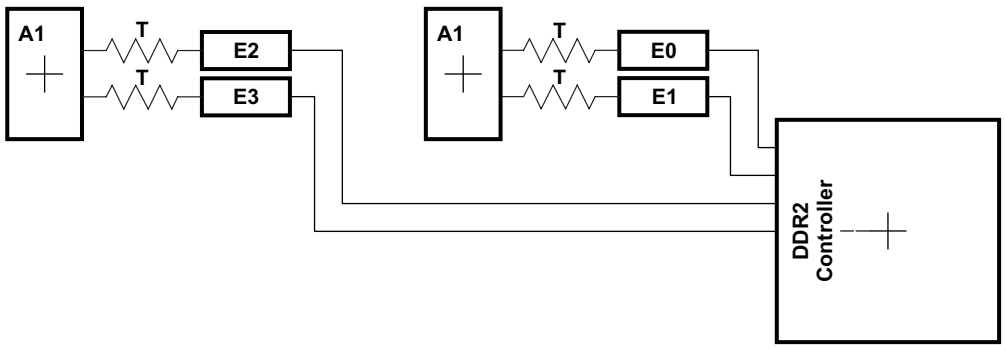


**Figure 9-11. DQS and DQ Routing and Toplogy**

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**Table 9-12. DQS and DQ Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | Center-to-center DQS-DQSn spacing in E0\|E1\|E2\|E3 | | | 2w | |
| 2 | DQS-DQSn skew in E0\|E1\|E2\|E3 | | | 25 | Mils |
| 3 | Center-to-center DQS to other DDR2 trace spacing(1) | 4w | | | |
| 4 | DQS and DQ nominal trace length (2)(3)(4) | DQLM-50 | DQLM | DQLM+50 | Mils |
| 5 | DQ-to-DQS skew length mismatch(2)(3)(4) | | | 100 | Mils |
| 6 | DQ-to-DQ skew length mismatch(2)(3)(4) | | | 100 | Mils |
| 7 | DQ-to-DQ and DQS via count mismatch(2)(3)(4) | | | 1 | Vias |
| 8 | Center-to-center DQ to other DDR2 trace spacing(1)(5) | 4w | | | |
| 9 | Center-to-center DQ to other DQ trace spacing(1)(6)(7) | 3w | | | |
| 10 | DQ and DQS E skew length mismatch(2)(3)(4) | | | 100 | Mils |

(1) Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) A 16-bit DDR memory system has two sets of data net classes; one for data byte 0, and one for data byte 1, each with an associated DQS (2 DQSs) per DDR EMIF used.
(3) A 32-bit DDR memory system has four sets of data net classes; one each for data bytes 0 through 3, and each associated with a DQS (4 DQSs) per DDR EMIF used.
(4) There is no need, and it is not recommended, to skew match across data bytes; that is, from DQS0 and data byte 0 to DQS1 and data byte 1.
(5) DQs from other DQS domains are considered *other DDR2 trace*.
(6) DQs from other data bytes are considered *other DDR2 trace*.
(7) DQLM is the longest Manhattan distance of each of the DQS and DQ net classes.

## 9.3.2 DDR3 Routing Specifications

### 9.3.2.1 Board Designs

TI only supports board designs utilizing DDR3 memory that follow the specifications in this document. The switching characteristics and timing diagram for the DDR3 memory controller are shown in Table 9-13 and Figure 9-12.

**Table 9-13. Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller**

| NO. | PARAMETER | -1G | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| 1 | $t_{c(DDR_CLK)}$ Cycle time, DDR_CLK | 1.25 | 3.3(1) | ns |

(1) This is the absolute maximum the clock period can be. Actual maximum clock period may be limited by DDR3 speed grade and operating frequency (see the DDR3 memory device data sheet).

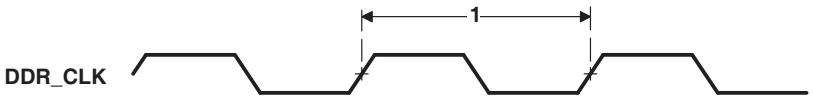


**Figure 9-12. DDR3 Memory Controller Clock Timing**

#### 9.3.2.1.1 DDR3 versus DDR2

This specification only covers TMS320DM816x processor PCB designs that utilize DDR3 memory. Designs using DDR2 memory should use the PCB design specifications for DDR2 memory in Section 9.3.1. While similar, the two memory systems have different requirements. It is currently not possible to design one PCB that covers both DDR2 and DDR3.

### 9.3.2.2 DDR3 Device Combinations

Since there are several possible combinations of device counts and single- or dual-side mounting, Table 9-14 summarizes the supported device configurations.


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**Table 9-14. Supported DDR3 Device Combinations(1)**

| NUMBER OF DDR3 DEVICES | DDR3 DEVICE WIDTH (BITS) | MIRRORED? | DDR3 EMIF WIDTH (BITS) |
|---|---|---|---|
| 1 | 16 | N | 16 |
| 2 | 8 | Y(2) | 16 |
| 2 | 16 | N | 32 |
| 2 | 16 | Y(2) | 32 |
| 4 | 8 | N | 32 |
| 4 | 8 | Y(3) | 32 |

(1) This table is per EMIF.
(2) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.
(3) This is two mirrored pairs of DDR3 devices.

#### *9.3.2.2.1 DDR3 EMIFs*

The processor contains two separate DDR3 EMIFs. This specification covers one of these EMIFs (DDR[0]) and, thus, needs to be implemented twice, once for each EMIF. The PCB layout generally turns out to be a semi-mirror with DDR[1] being a flipped version of DDR[0]; the only exception being the DDR3 devices themselves are not flipped unless mounted on opposite sides of the PCB. Requirements are identical between the two EMIFs.

### 9.3.2.3 DDR3 Interface Schematic

#### *9.3.2.3.1 32-Bit DDR3 Interface*

The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. Figure 9-13 and Figure 9-14 show the schematic connections for 32-bit interfaces using x16 devices.

#### *9.3.2.3.2 16-Bit DDR3 Interface*

Note that the 16-bit wide interface schematic is practically identical to the 32-bit interface (see Figure 9-13 and Figure 9-14); only the high-word DDR memories are removed and the unused DQS inputs are tied off. The processor DDR[x]_DQS[2] and DDR[x]_DQS[3] pins should be pulled to the DDR supply via 1-kΩ resistors. Similarly, the $\overline{\text{DDR[x]_DQS[2]}}$ and $\overline{\text{DDR[x]_DQS[3]}}$ pins should be pulled to ground via 1-kΩ resistors.

When not using a DDR interface, the proper method of handling the unused pins is to tie off the DQS pins by pulling the non-inverting DQS pin to the DDR_1V5 supply via a 1k-Ω resistor and pulling the inverting DQSn pin to ground via a 1k-Ω resistor. This needs to be done for each byte not used. Also, include the 50-Ω pulldown for DDR[x]_VTP. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32 bits wide, 16 bits wide, or not used.

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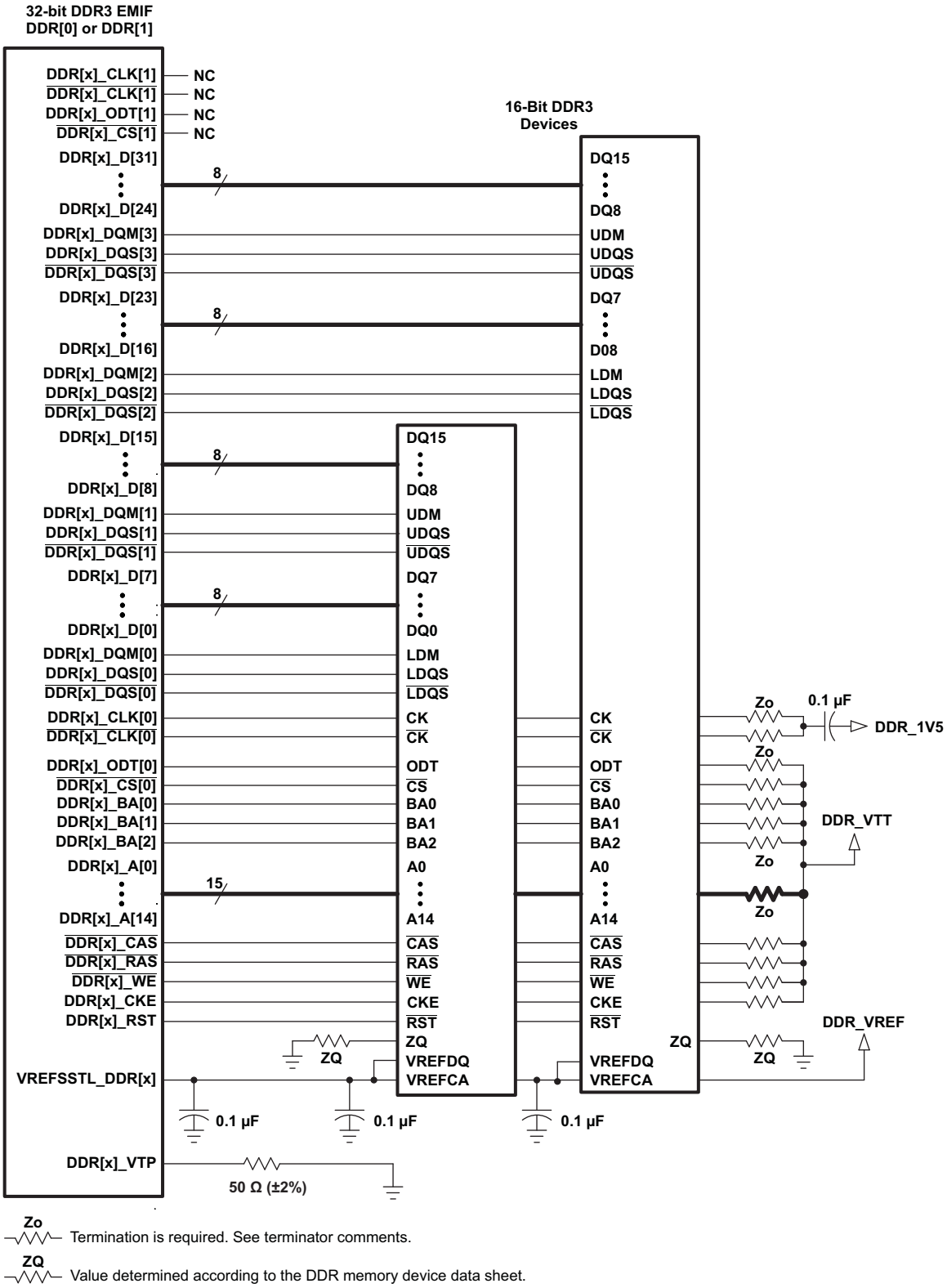


**Figure 9-13. 32-Bit, One-Bank DDR3 Interface Schematic Using Two 16-Bit DDR3 Devices**


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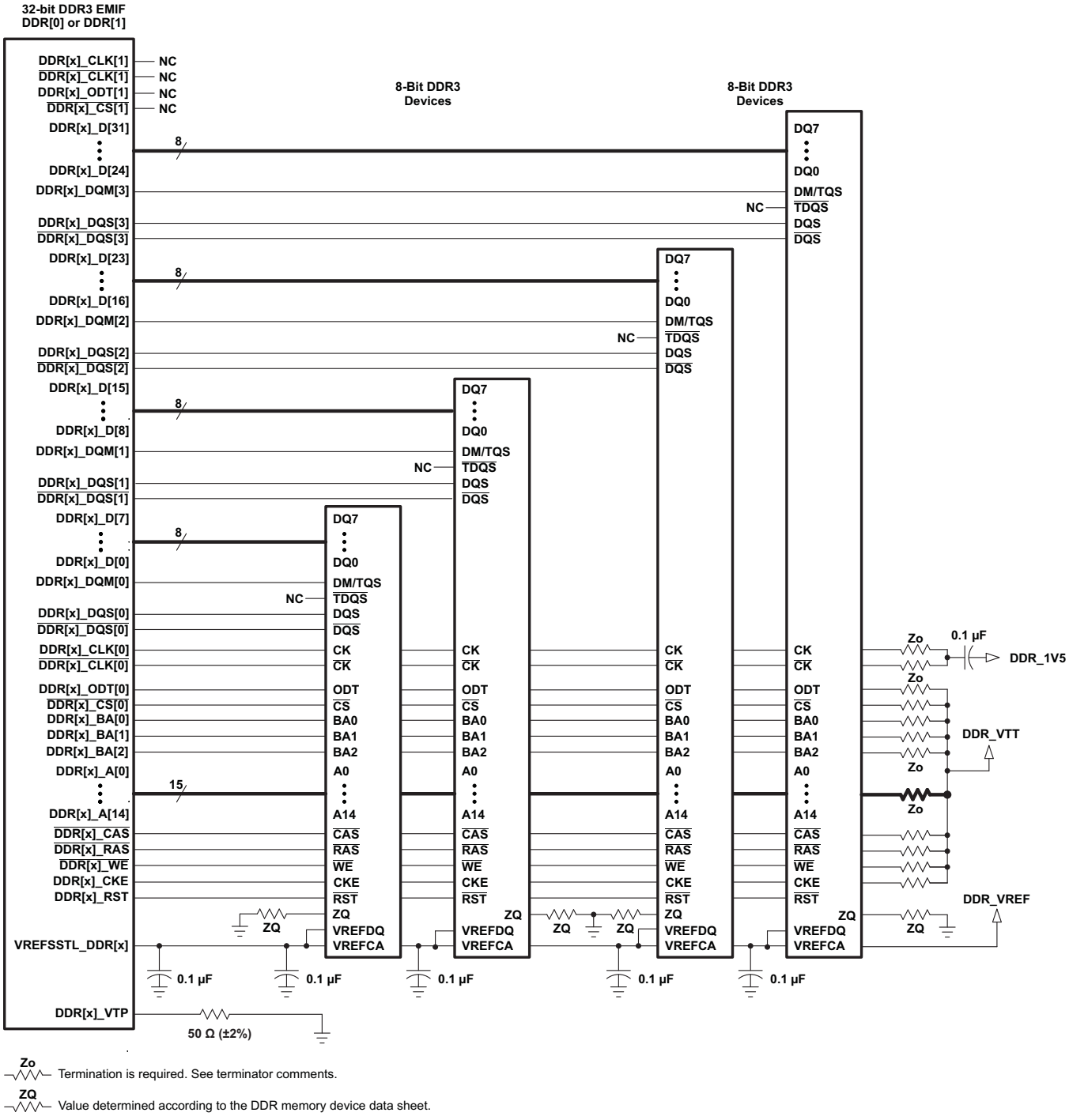


Zo — Termination is required. See terminator comments.

ZQ — Value determined according to the DDR memory device data sheet.

**Figure 9-14. 32-Bit, One-Bank DDR3 Interface Schematic Using Four 8-Bit DDR3 Devices**

#### 9.3.2.4 Compatible JEDEC DDR3 Devices

Table 9-15 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface. Generally, the DDR3 interface is compatible with DDR3-1600 devices in the x8 or x16 widths.

**Table 9-15. Compatible JEDEC DDR3 Devices**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | JEDEC DDR3 device speed grade(1) | DDR3-800 | DDR3-1600 | |
| 2 | JEDEC DDR3 device bit width | x8 | x16 | Bits |
| 3 | JEDEC DDR3 device count(2) | 2 | 8 | Devices |

(1) DDR3 speed grade depends on desired clock rate. Data rate is 2x the clock rate. For DDR3-1600, the clock rate is 800 MHz.
(2) For valid DDR3 device configurations and device counts, see Section 9.3.2.3, Figure 9-13, and Figure 9-14.

#### 9.3.2.5 PCB Stackup

The minimum stackup for routing the DDR3 interface is a four-layer stack up as shown in Table 9-16. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI and EMI performance, or to reduce the size of the PCB footprint. A six-layer stackup is shown in Table 9-17. Complete stackup specifications are provided in Table 9-18.

**Table 9-16. Minimum PCB Stackup**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top routing mostly vertical |
| 2 | Plane | Split power plane |
| 3 | Plane | Full ground plane |
| 4 | Signal | Bottom routing mostly horizontal |

**Table 9-17. Six-Layer PCB Stackup Suggestion**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top routing mostly vertical |
| 2 | Plane | Ground |
| 3 | Plane | Split power plane |
| 4 | Plane | Split power plane or Internal routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom routing mostly horizontal |


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**Table 9-18. PCB Stackup Specifications**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | PCB routing and plane layers | 4 | 6 | | |
| 2 | Signal routing layers | 2 | | | |
| 3 | Full ground reference layers under DDR3 routing region (1) | 1 | | | |
| 4 | Full 1.5-V power reference layers under the DDR3 routing region (1) | 1 | | | |
| 5 | Number of reference plane cuts allowed within DDR routing region (2) | | | 0 | |
| 6 | Number of layers between DDR3 routing layer and reference plane (3) | | | 0 | |
| 7 | PCB routing feature size | | 4 | | Mils |
| 8 | PCB trace width, w | | 4 | | Mils |
| 9 | PCB BGA escape via pad size (4) | | 18 | 20 | Mils |
| 10 | PCB BGA escape via hole size | | 10 | | Mils |
| 11 | Processor BGA pad size | | 0.3 | | mm |
| 12 | DDR3 device BGA pad size (5) | | | | |
| 13 | Single-ended impedance, Zo | 50 | | 75 | Ω |
| 14 | Impedance control (6) | Z-5 | Z | Z+5 | Ω |

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.
(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.
(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.
(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.
(5) For the DDR3 device BGA pad size, see the DDR3 device manufacturer documentation.
(6) Z is the nominal singled-ended impedance selected for the PCB specified by item 13.

### 9.3.2.6 Placement

Figure 9-15 shows the required placement for the processor as well as the DDR3 devices. The dimensions for this figure are defined in Table 9-19. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3 devices are omitted from the placement.

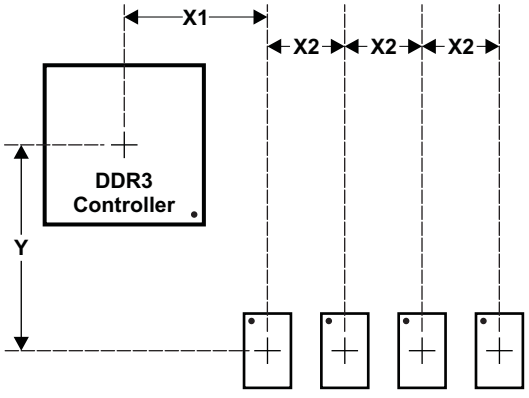


**Figure 9-15. Placement Specifications**

**Table 9-19. Placement Specifications**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | X1[1][2][3] | | 1000 | Mils |
| 2 | X2[1][2] | | 600 | Mils |
| 3 | Y Offset[1][2][3] | | 1500 | Mils |
| 4 | DDR3 keepout region | | | |
| 5 | Clearance from non-DDR3 signal to DDR3 keepout region[4][5][6] | 4 | | w |

(1) For dimension definitions, see Figure 9-15.
(2) Measurements from center of processor to center of DDR3 device.
(3) Minimizing X1 and Y improves timing margins.
(4) w is defined as the signal trace width.
(5) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.
(6) Note that DDR3 signals from one DDR3 controller are considered *non-DDR3* to the other controller. In other words, keep the two DDR3 interfaces separated by this specification.

### 9.3.2.7 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in Figure 9-16. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 9-19. Non-DDR3 signals should not be routed on the DDR signal layers within the DDR3 keepout region. Non-DDR3 signals may be routed in the region, provided they are routed on layers separated from the DDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.5-V DDR3 power plane should cover the entire keepout region. Also note that the two DDR3 controller's signals should be separated from each other by the specification in Table 9-19, item 5.

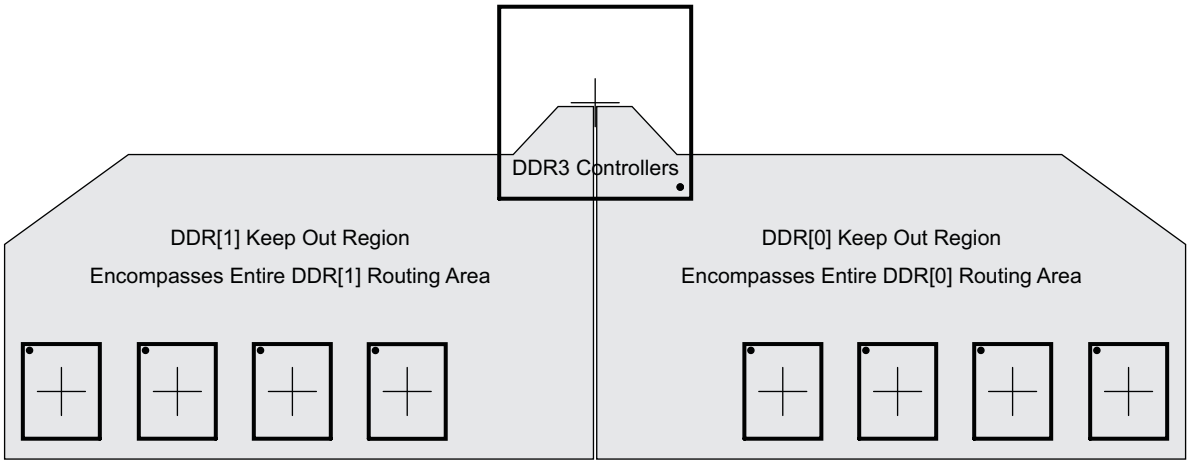


**Figure 9-16. DDR3 Keepout Region**

### 9.3.2.8 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. Table 9-20 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 controllers and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry. Also note that Table 9-20 is *per DDR3 controller*; thus, systems using both controllers have to meet the needs of Table 9-20 twice, once for each controller.


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**Table 9-20. Bulk Bypass Capacitors**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | DDR_1V5 bulk bypass capacitor count(1) | 6 | | Devices |
| 2 | DDR_1V5 bulk bypass total capacitance | 140 | | µF |

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

### 9.3.2.9 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor DDR power, and processor DDR ground connections. Table 9-21 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the pins (balls) being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limits on via sharing shown in Table 9-21.

**Table 9-21. High-Speed Bypass Capacitors**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | HS bypass capacitor package size(1) | | 201 | 402 | 10 Mils |
| 2 | Distance, HS bypass capacitor to processor being bypassed(2)(3)(4) | | | 400 | Mils |
| 3 | Processor DDR_1V5 HS bypass capacitor count | 70 | | | Devices |
| 4 | Processor DDR_1V5 HS bypass capacitor total capacitance | 5 | | | µF |
| 5 | Number of connection vias for each device power and ground ball(5) | | | | Vias |
| 6 | Trace length from device power and ground ball to connection via(2) | | 35 | 70 | Mils |
| 7 | Distance, HS bypass capacitor to DDR device being bypassed(6) | | | 150 | Mils |
| 8 | DDR3 device HS bypass capacitor count(7) | 12 | | | Devices |
| 9 | DDR3 device HS bypass capacitor total capacitance(7) | 0.85 | | | µF |
| 10 | Number of connection vias for each HS capacitor(8)(9) | 2 | | | Vias |
| 11 | Trace length from bypass capacitor connect to connection via(2)(9) | | 35 | 100 | Mils |
| 12 | Number of connection vias for each DDR3 device power and ground ball(10) | 1 | | | Vias |
| 13 | Trace length from DDR3 device power and ground ball to connection via(2)(8) | | 35 | 60 | Mils |

(1) LxW, 10-mil units, for example, a 0402 is a 40x20-mil surface-mount capacitor.
(2) Closer and shorter is better.
(3) Measured from the nearest processor power and ground ball to the center of the capacitor package.
(4) Three of these capacitors should be located underneath the processor, between the cluster of DDR_1V5 balls and ground balls, between the DDR interfaces on the package.
(5) See the Via Channel™ escape for the processor package.
(6) Measured from the DDR3 device power and ground ball to the center of the capacitor package.
(7) Per DDR3 device.
(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.
(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.
(10) Up to a total of two pairs of DDR power and ground balls may share a via.

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#### 9.3.2.9.1 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Since these are returns for signal current, the signal via size may be used for these capacitors.

### 9.3.2.10 Net Classes

Table 9-22 lists the clock net classes for the DDR3 interface. Table 9-23 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

**Table 9-22. Clock Net Class Definitions**

| CLOCK NET CLASS | PROCESSOR PIN NAMES |
|---|---|
| CK | DDR[x]_CLK[x] and $\overline{\text{DDR[x]_CLK[x]}}$ |
| DQS0 | DDR[x]_DQS[0] and $\overline{\text{DDR[x]_DQS[0]}}$ |
| DQS1 | DDR[x]_DQS[1] and $\overline{\text{DDR[x]_DQS[1]}}$ |
| DQS2(1) | DDR[x]_DQS[2] and $\overline{\text{DDR[x]_DQS[2]}}$ |
| DQS3(1) | DDR[x]_DQS[3] and $\overline{\text{DDR[x]_DQS[3]}}$ |

(1) Only used on 32-bit wide DDR3 memory systems.

**Table 9-23. Signal Net Class Definitions**

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | PROCESSOR PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | DDR[x]_BA[2:0], DDR[x]_A[14:0], $\overline{\text{DDR[x]_CS[x]}}$, $\overline{\text{DDR[x]_CAS}}$, $\overline{\text{DDR[x]_RAS}}$, $\overline{\text{DDR[x]_WE}}$, DDR[x]_CKE, DDR[x]_ODT[x] |
| DQ0 | DQS0 | DDR[x]_D[7:0], DDR[x]_DQM[0] |
| DQ1 | DQS1 | DDR[x]_D[15:8], DDR[x]_DQM[1] |
| DQ2(1) | DQS2 | DDR[x]_D[23:16], DDR[x]_DQM[2] |
| DQ3(1) | DQS3 | DDR[x]_D[31:24], DDR[x]_DQM[3] |

(1) Only used on 32-bit wide DDR3 memory systems.

### 9.3.2.11 DDR3 Signal Termination

Signal terminators are required for the CK and ADDR_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

### 9.3.2.12 VREFSSTL_DDR Routing

VREFSSTL_DDR (VREF) is used as a reference by the input buffers of the DDR3 memories as well as the processor. VREF is intended to be half the DDR3 power supply voltage and is typically generated with the DDR3 1.5-V and VTT power supply. It should be routed as a nominal 20-mil wide trace with 0.1 µF bypass capacitors near each device connection. Narrowing of VREF is allowed to accommodate routing congestion.

### 9.3.2.13 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.


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### 9.3.2.14 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in Table 9-24.

#### *9.3.2.14.1 Four DDR3 Devices*

Four DDR3 devices are supported on the DDR EMIF consisting of four x8 DDR3 devices arranged as one bank (CS). These four devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

##### *9.3.2.14.1.1 CK and ADDR_CTRL Topologies, Four DDR3 Devices*

Figure 9-17 shows the topology of the CK net classes and Figure 9-18 shows the topology for the corresponding ADDR_CTRL net classes.

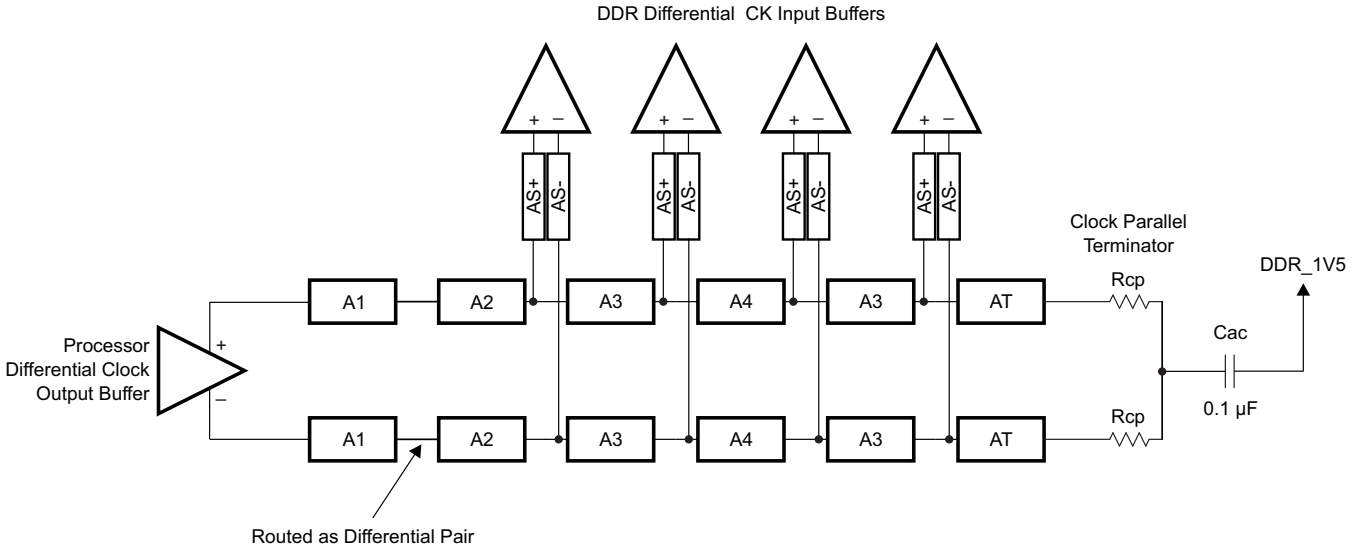


**Figure 9-17. CK Topology for Four x8 DDR3 Devices**

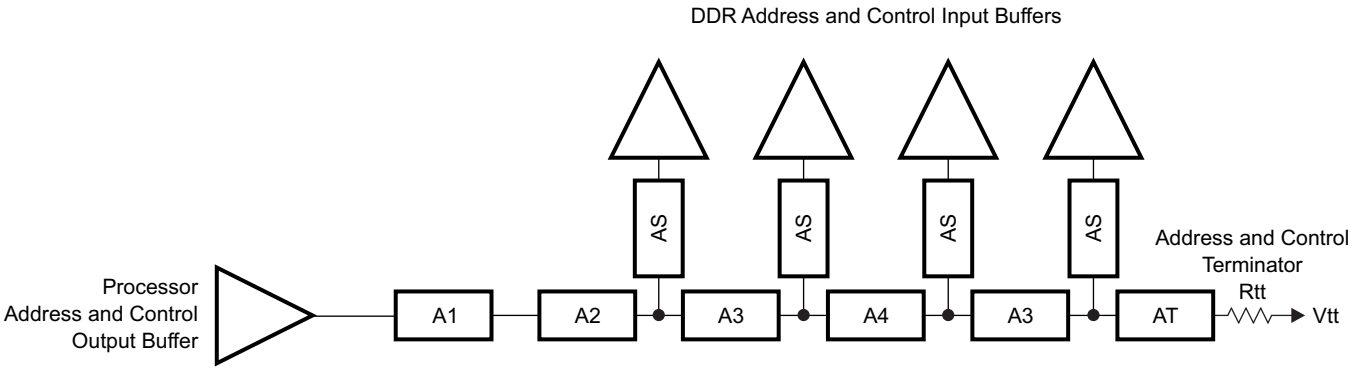


**Figure 9-18. ADDR_CTRL Topology for Four x8 DDR3 Devices**

##### *9.3.2.14.1.2 CK and ADDR_CTRL Routing, Four DDR3 Devices*

Figure 9-19 shows the CK routing for four DDR3 devices placed on the same side of the PCB. Figure 9-20 shows the corresponding ADDR_CTRL routing.

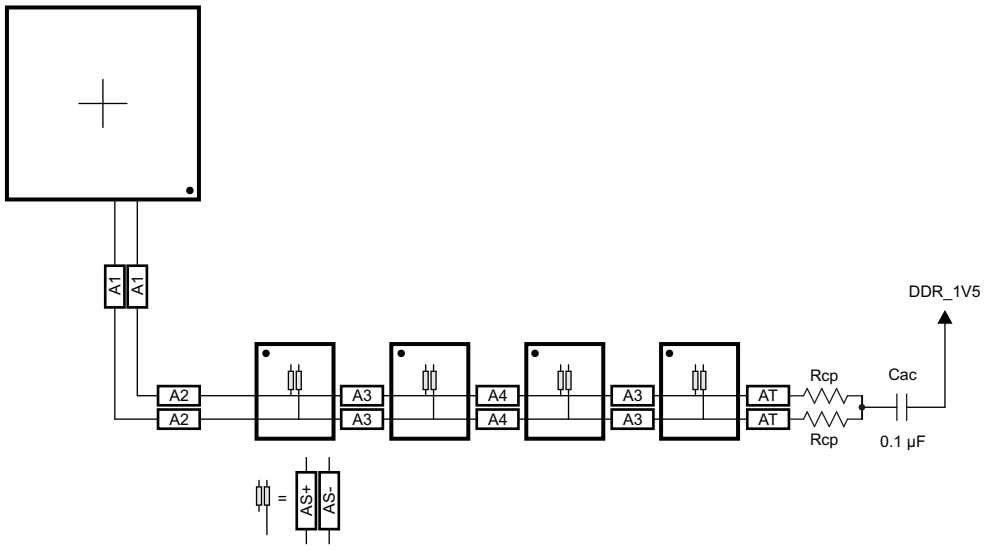


**Figure 9-19. CK Routing for Four Single-Side DDR3 Devices**

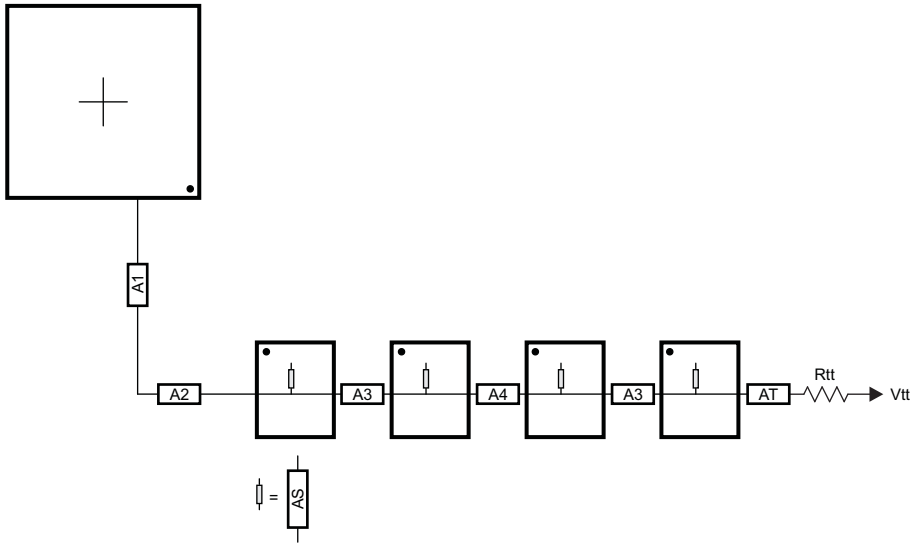


**Figure 9-20. ADDR_CTRL Routing for Four Single-Side DDR3 Devices**

To save PCB space, the four DDR3 memories may be mounted as two mirrored pairs at a cost of increased routing and assembly complexity. Figure 9-21 and Figure 9-22 show the routing for CK and ADDR_CTRL, respectively, for four DDR3 devices mirrored in a two-pair configuration.


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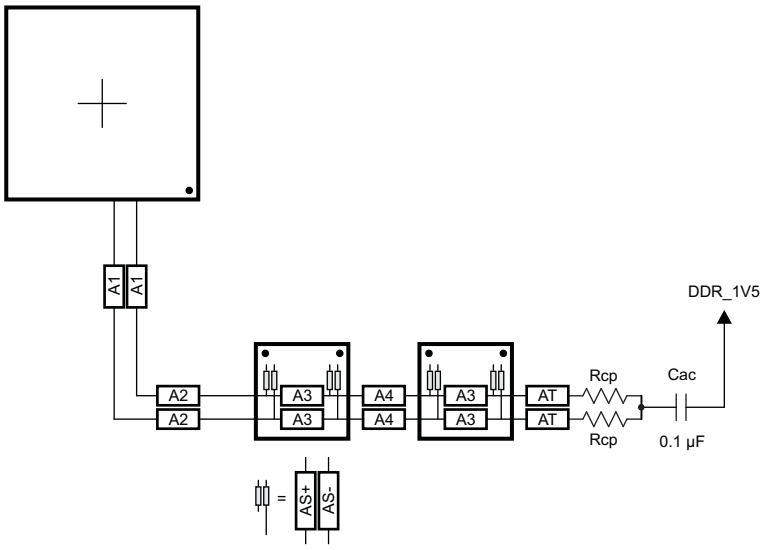


**Figure 9-21. CK Routing for Four Mirrored DDR3 Devices**

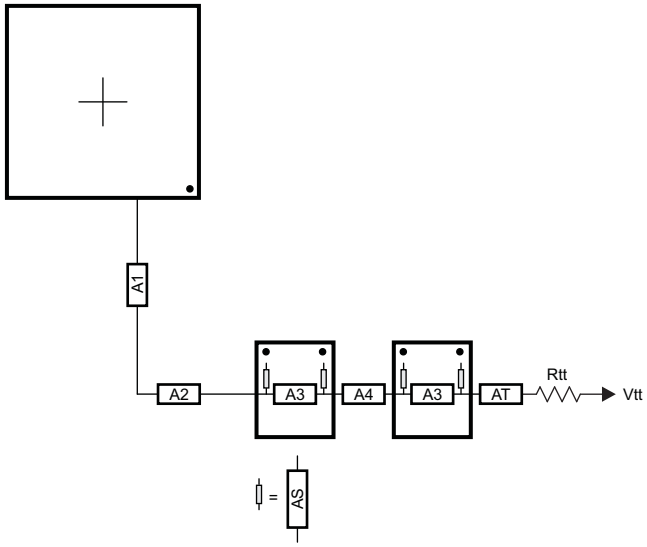


**Figure 9-22. ADDR_CTRL Routing for Four Mirrored DDR3 Devices**

#### *9.3.2.14.2 Two DDR3 Devices*

Two DDR3 devices are supported on the DDR EMIF consisting of two x8 DDR3 devices arranged as one bank (CS), 16 bits wide, or two x16 DDR3 devices arranged as one bank (CS), 32 bits wide. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

##### *9.3.2.14.2.1 CK and ADDR_CTRL Topologies, Two DDR3 Devices*

Figure 9-23 shows the topology of the CK net classes and Figure 9-24 shows the topology for the corresponding ADDR_CTRL net classes.

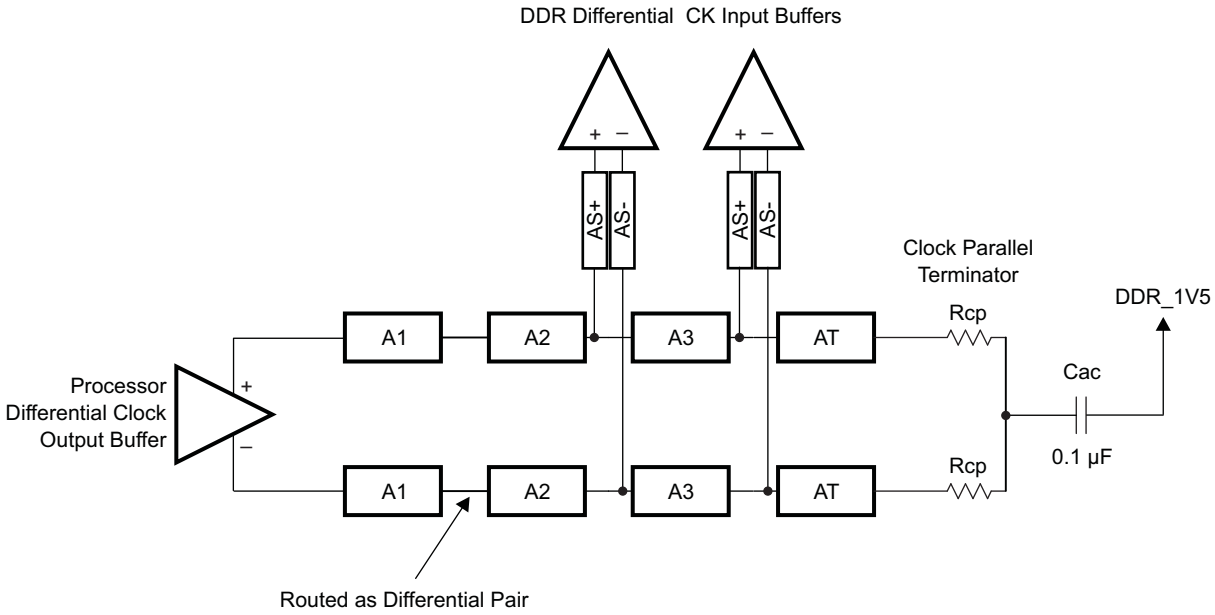


**Figure 9-23. CK Topology for Two DDR3 Devices**

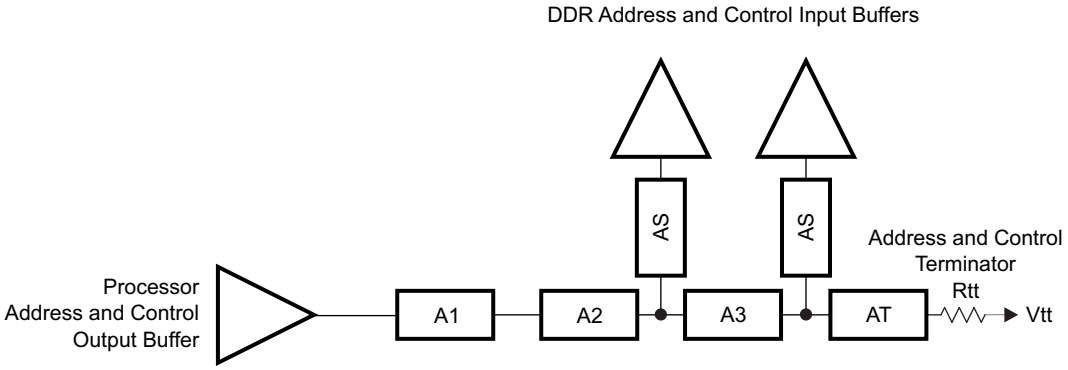


**Figure 9-24. ADDR_CTRL Topology for Two DDR3 Devices**

### *9.3.2.14.2.2 CK and ADDR_CTRL Routing, Two DDR3 Devices*

Figure 9-25 shows the CK routing for two DDR3 devices placed on the same side of the PCB. Figure 9-26 shows the corresponding ADDR_CTRL routing.


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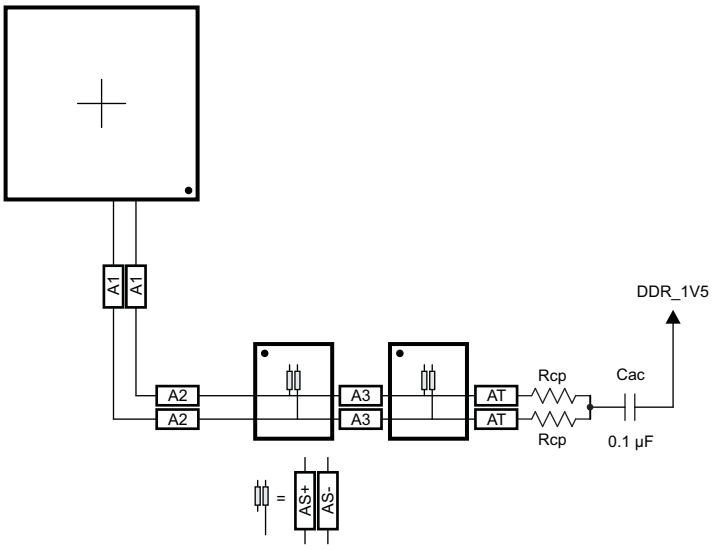


**Figure 9-25. CK Routing for Two Single-Side DDR3 Devices**

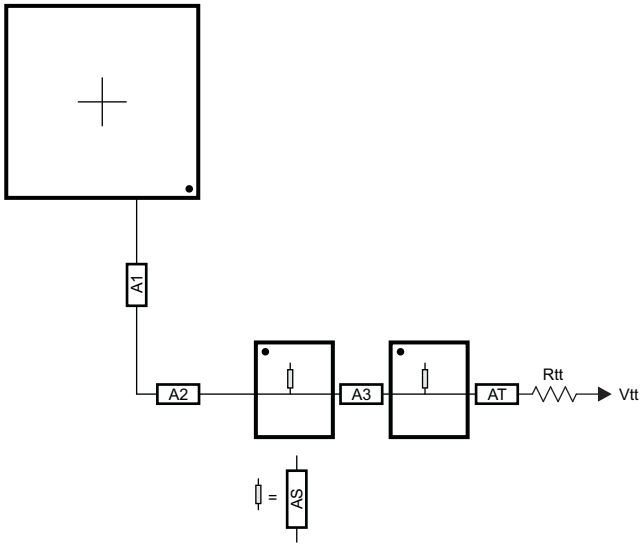


**Figure 9-26. ADDR_CTRL Routing for Two Single-Side DDR3 Devices**

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. Figure 9-27 and Figure 9-28 show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.

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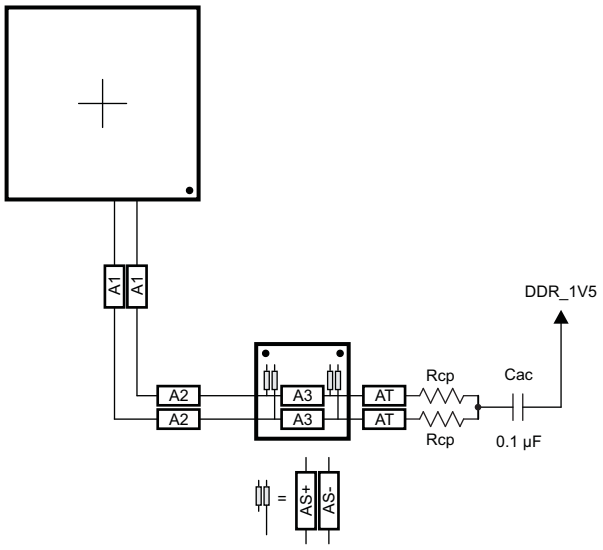


**Figure 9-27. CK Routing for Two Mirrored DDR3 Devices**

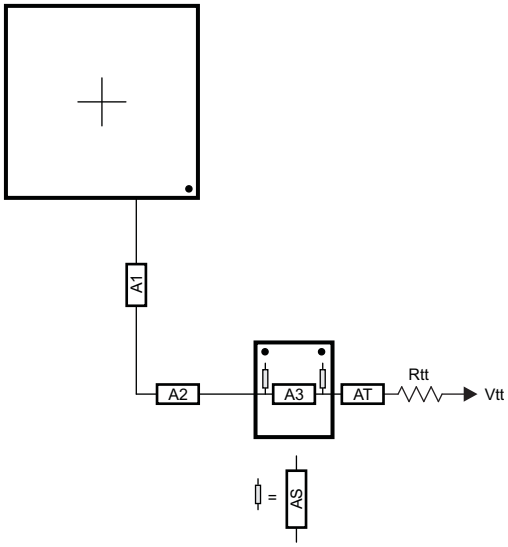


**Figure 9-28. ADDR_CTRL Routing for Two Mirrored DDR3 Devices**

#### *9.3.2.14.3 One DDR3 Device*

A single DDR3 device is supported on the DDR EMIF consisting of one x16 DDR3 device arranged as one bank (CS), 16 bits wide.

##### *9.3.2.14.3.1 CK and ADDR_CTRL Topologies, One DDR3 Device*

Figure 9-29 shows the topology of the CK net classes and Figure 9-30 shows the topology for the corresponding ADDR_CTRL net classes.


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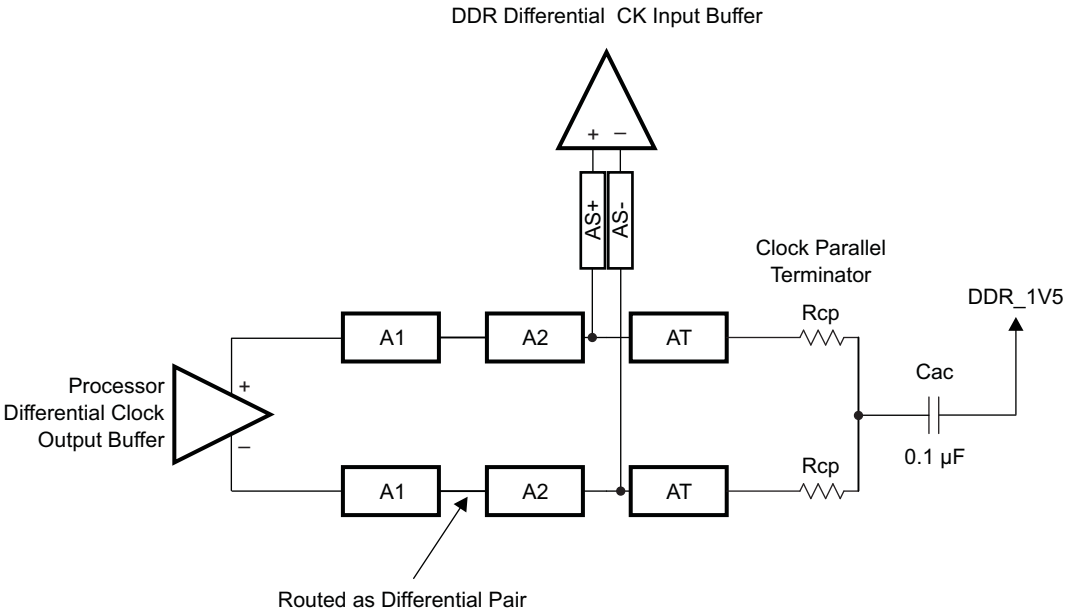


**Figure 9-29. CK Topology for One DDR3 Device**

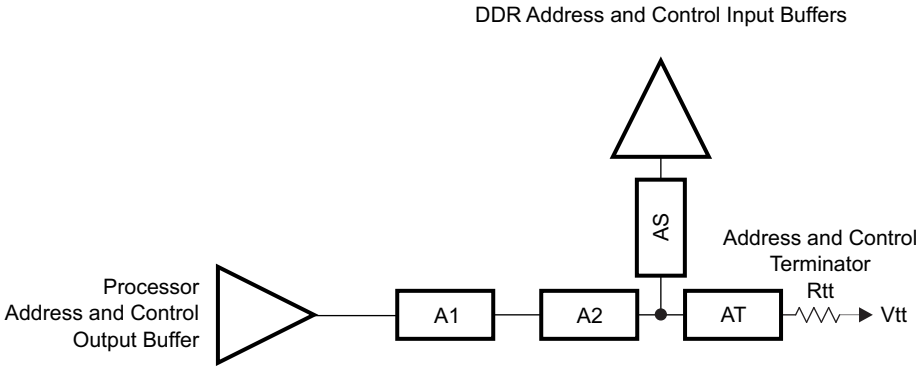


**Figure 9-30. ADDR_CTRL Topology for One DDR3 Device**

### *9.3.2.14.3.2 CK and ADDR_CTRL Routing, One DDR3 Device*

Figure 9-31 shows the CK routing for one DDR3 device placed on the same side of the PCB. Figure 9-32 shows the corresponding ADDR_CTRL routing.

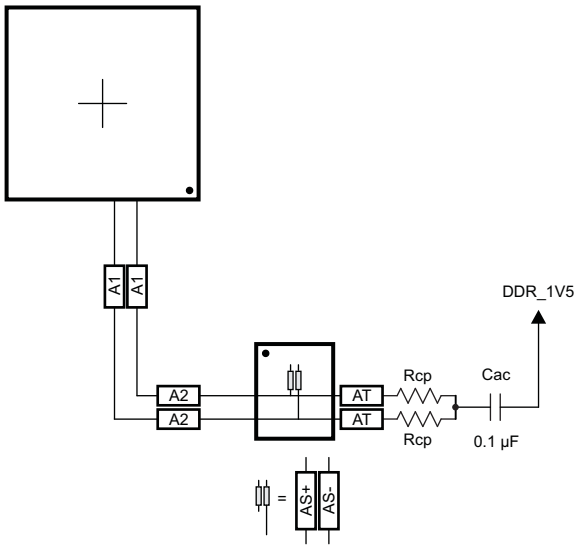


**Figure 9-31. CK Routing for One DDR3 Device**

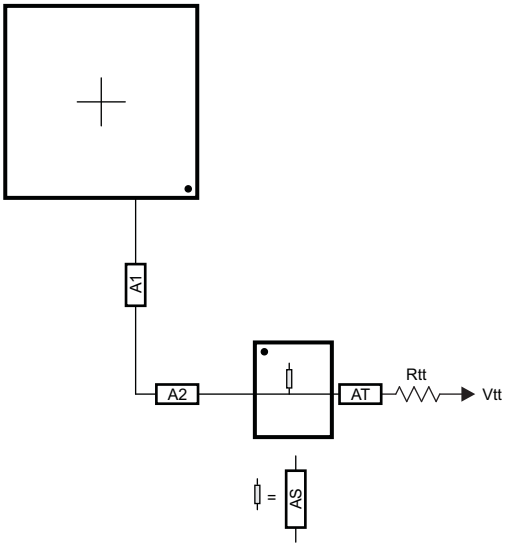


**Figure 9-32. ADDR_CTRL Routing for One DDR3 Device**

### 9.3.2.15 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

#### *9.3.2.15.1 DQS, DQ and DM Topologies, Any Number of Allowed DDR3 Devices*

DQS lines are point-to-point differential, and DQ and DM lines are point-to-point singled ended. Figure 9-33 and Figure 9-34 show these topologies.


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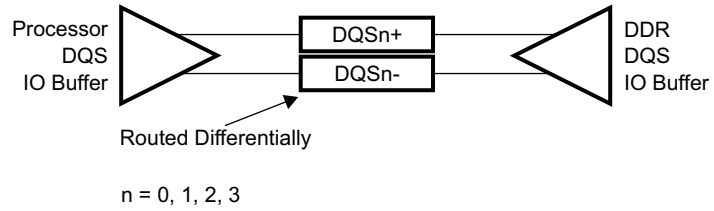



**Figure 9-33. DQS Topology**

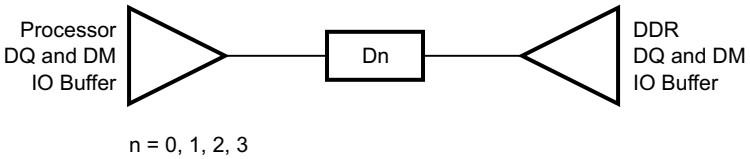



**Figure 9-34. DQ/DM Topology**

### *9.3.2.15.2 DQS, DQ and DM Routing, Any Number of Allowed DDR3 Devices*

Figure 9-35 and Figure 9-36 show the DQS, DQ and DM routing.

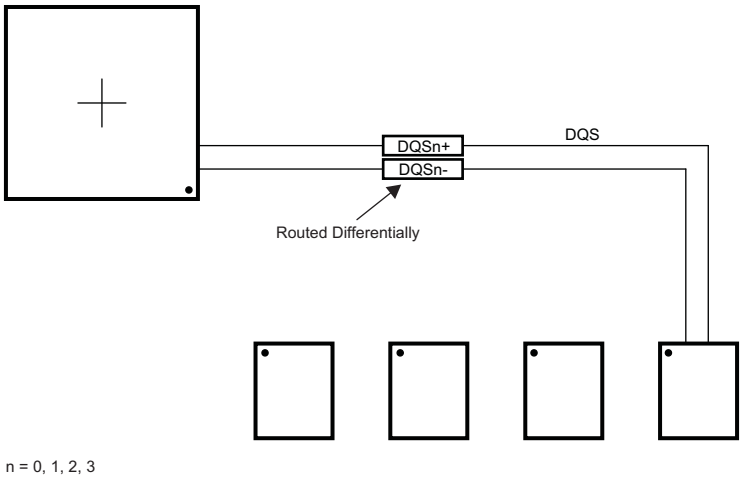



**Figure 9-35. DQS Routing With Any Number of Allowed DDR3 Devices**

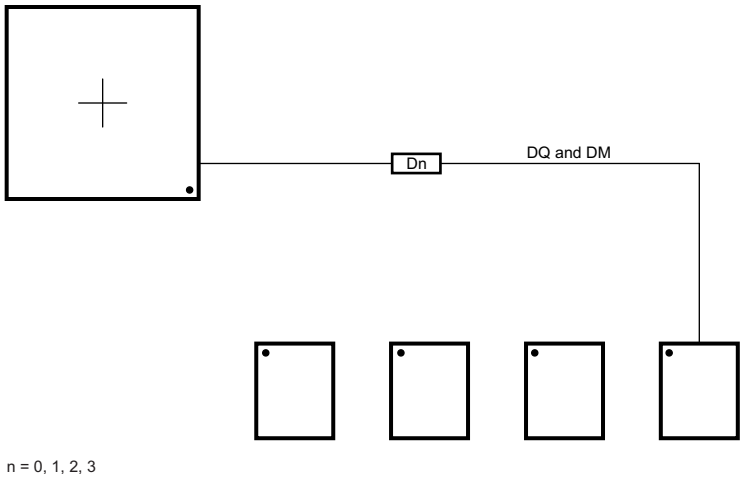


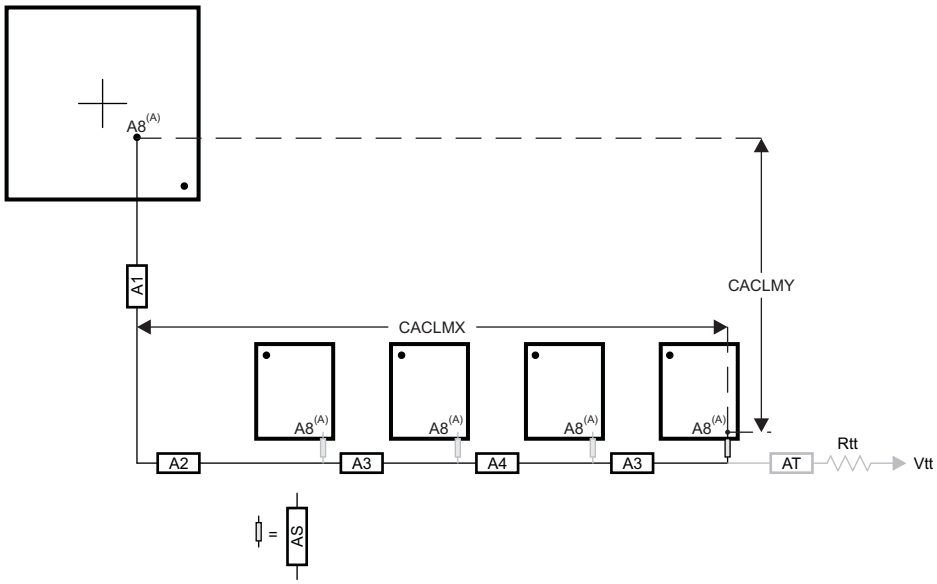

**Figure 9-36. DQ and DM Routing With Any Number of Allowed DDR3 Devices**

### 9.3.2.16 Routing Specification

#### *9.3.2.16.1 CK and ADDR_CTRL Routing Specification*

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 9-37 and Figure 9-38 show this distance for four loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK and ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 9-24.




A. It is very likely that the longest CK and ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK and ADDR_CTRL skew matching and length control.

The length of shorter CK and ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length caculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

**Figure 9-37. CACLM for Four Address Loads on One Side of PCB**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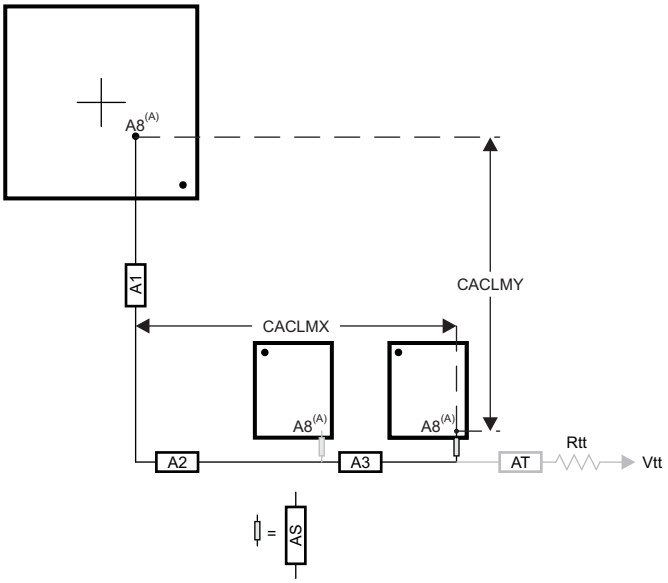


A. It is very likely that the longest CK and ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK and ADDR_CTRL skew matching and length control.

The length of shorter CK and ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length caculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

**Figure 9-38. CACLM for Two Address Loads on One Side of PCB**

**Table 9-24. CK and ADDR_CTRL Routing Specification(1)(2)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | A1+A2 length | | | 2500 | mils |
| 2 | A1+A2 skew | | | 25 | mils |
| 3 | A3 length | | | 660 | mils |
| 4 | A3 skew(3) | | | 25 | mils |
| 5 | A3 skew(4) | | | 125 | mils |
| 6 | A4 length | | | 660 | mils |
| 7 | A4 skew | | | 25 | mils |
| 8 | AS length | | | 100 | mils |
| 9 | AS skew | | | 100 | mils |
| 10 | AS+ and AS- length | | | 70 | mils |
| 11 | AS+ and AS- skew | | | 5 | mils |
| 12 | AT length(5) | | 500 | | mils |
| 13 | AT skew(6) | | 100 | | mils |
| 14 | AT skew(7) | | | 5 | mils |
| 15 | CK and ADDR_CTRL nominal trace length(8) | CACLM-50 | CACLM | CACLM+50 | mils |

(1) The use of vias should be minimized.
(2) Additional bypass capacitors are required when using the DDR_1V5 plane as the reference plane to allow the return current to jump between the DDR_1V5 plane and the ground plane when the net class swtiches layers at a via.
(3) Non-mirrored configuration (all DDR3 memories on same side of PCB).
(4) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).
(5) While this length can be increased for convienience, its length should be minimized.
(6) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.
(7) CK net class only.
(8) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes + 300 mils. For definition, see Section 9.3.2.16.1, Figure 9-37, and Figure 9-38.

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**Table 9-24. CK and ADDR_CTRL Routing Specification(1)(2) (continued)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 16 | Center-to-center CK to other DDR3 trace spacing(9) | 4w | | | |
| 17 | Center-to-center ADDR_CTRL to other DDR3 trace spacing(9)(10) | 4w | | | |
| 18 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(9) | 3w | | | |
| 19 | CK center-to-center spacing(11) | | | | |
| 20 | CK spacing to other net(9) | 4w | | | |
| 21 | Rcp(12) | Zo-1 | Zo | Zo+ | Ω |
| 22 | Rtt(12)(13) | Zo-5 | Zo | Zo+5 | Ω |

(9) Center-to-center spacing is allowed to fall to minimum (w) for up to 1250 mils of routed length.
(10) The ADDR_CTRL net class of the other DDR EMIF is considered *other DDR3 trace spacing*.
(11) CK spacing set to ensure proper differential impedance.
(12) Source termination (series resistor at driver) is specifically not allowed.
(13) Termination values should be uniform across the net class.

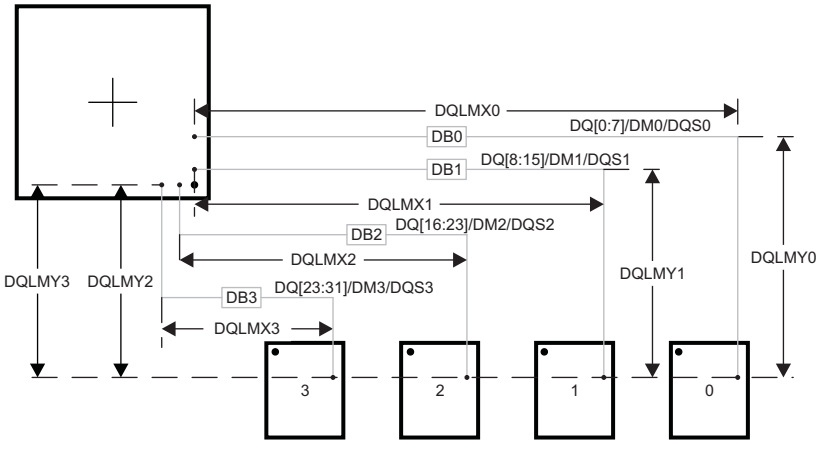
#### *9.3.2.16.2 DQS and DQ Routing Specification*

Skew within the DQS, DQ and DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are four DQLMs, DQLM0-DQLM3. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

**NOTE**

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

Given the DQS, DQ and DM pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 9-39 shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS, DQ and DM routing, these specifications are contained in Table 9-25.




DB0 - DB3 represent data bytes 0 - 3.

There are four DQLMs, one for each byte (32-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:
DQLM0 = DQLMX0 + DQLMY0
DQLM1 = DQLMX1 + DQLMY1
DQLM2 = DQLMX2 + DQLMY2
DQLM3 = DQLMX3 + DQLMY3

**Figure 9-39. DQLM for Any Number of Allowed DDR3 Devices**


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**Table 9-25. Data Routing Specification(1)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | DB0 nominal length(2)(3) | | | DQLM0 | mils |
| 2 | DB1 nominal length(2)(4) | | | DQLM1 | mils |
| 3 | DB2 nominal length(2)(5) | | | DQLM2 | mils |
| 4 | DB3 nominal length(2)(6) | | | DQLM3 | mils |
| 5 | DBn skew(7) | | | 25 | mils |
| 6 | DQSn+ to DQSn- skew | | | 5 | mils |
| 7 | DQSn to DBn skew(7)(8) | | | 25 | mils |
| 8 | Center-to-center DBn to other DDR3 trace spacing(9)(10) | 4w | | | |
| 9 | Center-to-center DBn to other DBn trace spacing(9)(11) | 3w | | | |
| 10 | DQSn center-to-center spacing(12) | | | | |
| 11 | DQSn center-to-center spacing to other net(9) | 4w | | | |

(1) External termination disallowed. Data termination should use built-in ODT functionality.
(2) DQLMn is the longest Manhattan distance of a byte. For definition, see Section 9.3.2.16.2 and Figure 9-39.
(3) DQLM0 is the longest Manhattan length for the net classes of Byte 0.
(4) DQLM1 is the longest Manhattan length for the net classes of Byte 1.
(5) DQLM2 is the longest Manhattan length for the net classes of Byte 2.
(6) DQLM3 is the longest Manhattan length for the net slasses of Byte 3.
(7) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.
(8) Each DQS pair is length matched to its associated byte.
(9) Center-to-center spacing is allowed to fall to minimum (w) for up to 1250 mils of routed length.
(10) Other DDR3 trace spacing means other DDR3 net classes not within the byte.
(11) This applies to spacing within the net classes of a byte.
(12) DQS pair spacing is set to ensure proper differential impedance.

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### 9.3.3 DDR2 and DDR3 Memory Controller Register Descriptions

**Table 9-26. DDR2 and DDR3 Memory Controller Registers**

| DDR0 HEX ADDRESS | DDR1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4C00 0004 | 0x4D00 0004 | SDRSTAT | SDRAM Status |
| 0x4C00 0008 | 0x4D00 0008 | SDRCR | SDRAM Config |
| 0x4C00 000C | 0x4D00 000C | SDRCR2 | SDRAM Config 2 |
| 0x4C00 0010 | 0x4D00 0010 | SDRRCR | SDRAM Refresh Control |
| 0x4C00 0014 | 0x4D00 0014 | SDRRCSR | SDRAM Refresh Control Shadow |
| 0x4C00 0018 | 0x4D00 0018 | SDRTIM1 | SDRAM Timing 1 |
| 0x4C00 001C | 0x4D00 001C | SDRTIM1SR | SDRAM Timing 1 Shadow |
| 0x4C00 0020 | 0x4D00 0020 | SDRTIM2 | SDRAM Timing 2 |
| 0x4C00 0024 | 0x4D00 0024 | SDRTIM2SR | SDRAM Timing 2 Shadow |
| 0x4C00 0028 | 0x4D00 0028 | SDRTIM3 | SDRAM Timing 3 |
| 0x4C00 002C | 0x4D00 002C | SDRTIM3SR | SDRAM Timing 3 Shadow |
| 0x4C00 0038 | 0x4D00 0038 | PMCR | Power Management Control |
| 0x4C00 003C | 0x4D00 003C | PMCSR | Power Management Control Shadow |
| 0x4C00 0054 | 0x4D00 0054 | PBBPR | Peripheral Bus Burst Priority |
| 0x4C00 00A0 | 0x4D00 00A0 | EOI | End of Interrupt |
| 0x4C00 00A4 | 0x4D00 00A4 | SOIRSR | System OCP Interrupt Raw Status |
| 0x4C00 00AC | 0x4D00 00AC | SOISR | System OCP Interrupt Status |
| 0x4C00 00B4 | 0x4D00 00B4 | SOIESR | System OCP Interrupt Enable Set |
| 0x4C00 00BC | 0x4D00 00BC | SOIECR | System OCP Interrupt Enable Clear |
| 0x4C00 00C8 | 0x4D00 00C8 | ZQCR | SDRAM output Impedance Calibration Config |
| 0x4C00 00DC | 0x4D00 00DC | RWLCR | Read-Write Leveling Control |
| 0x4C00 00E4 | 0x4D00 00E4 | DDRPHYCR | DDR PHY Control |
| 0x4C00 00E8 | 0x4D00 00E8 | DDRPHYCSR | DDR PHY Control Shadow |

### 9.3.4 DDR2 and DDR3 PHY Register Descriptions

**Table 9-27. DDR2 and DDR3 PHY Registers**

| DDR0 HEX ADDRESS | DDR1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4819 800C | 0x4819 A00C | CMD0_IO_CONFIG_I_0 | Command 0 Address and Command Pad Configuration |
| 0x4819 8010 | 0x4819 A010 | CMD0_IO_CONFIG_I_CLK_0 | Command 0 Clock Pad Configuration |
| 0x4819 8014 | 0x4819 A014 | CMD0_IO_CONFIG_SR_0 | Command 0 Address and Command Slew Rate Configuration |
| 0x4819 8018 | 0x4819 A018 | CMD0_IO_CONFIG_SR_CLK_0 | Command 0 Clock Pad Slew Rate Configuration |
| 0x4819 801C | 0x4819 A01C | CMD0_REG_PHY_CTRL_SLAVE_RATIO_0 | Command 0 Address and Command Slave Ratio |
| 0x4819 802C | 0x4819 A02C | CMD0_REG_PHY_INVERT_CLKOUT_0 | Command 0 Invert Clockout Selection |
| 0x4819 8040 | 0x4819 A040 | CMD1_IO_CONFIG_I_0 | Command 1 Address and Command Pad Configuration |
| 0x4819 8044 | 0x4819 A044 | CMD1_IO_CONFIG_I_CLK_0 | Command 1 Clock Pad Configuration |
| 0x4819 8048 | 0x4819 A048 | CMD1_IO_CONFIG_SR_0 | Command 1 Address and Command Slew Rate Configuration |
| 0x4819 804C | 0x4819 A04C | CMD1_IO_CONFIG_SR_CLK_0 | Command 1 Clock Pad Slew Rate Configuration |
| 0x4819 8050 | 0x4819 A050 | CMD1_REG_PHY_CTRL_SLAVE_RATIO_0 | Command 1 Address and Command Slave Ratio |


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**Table 9-27. DDR2 and DDR3 PHY Registers (continued)**

| DDR0 HEX ADDRESS | DDR1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4819 8060 | 0x4819 A060 | CMD1_REG_PHY_INVERT_CLKOUT_0 | Command 1 Invert Clockout Selection |
| 0x4819 8074 | 0x4819 A074 | CMD2_IO_CONFIG_I_0 | Command 2 Address and Command Pad Configuration |
| 0x4819 8078 | 0x4819 A078 | CMD2_IO_CONFIG_I_CLK_0 | Command 2 Clock Pad Configuration |
| 0x4819 807C | 0x4819 A07C | CMD2_IO_CONFIG_SR_0 | Command 2 Address and Command Slew Rate Configuration |
| 0x4819 8080 | 0x4819 A080 | CMD2_IO_CONFIG_SR_CLK_0 | Command 2 Clock Pad Slew Rate Configuration |
| 0x4819 8084 | 0x4819 A084 | CMD2_REG_PHY_CTRL_SLAVE_RATIO_0 | Command 2 Address and Command Slave Ratio |
| 0x4819 8094 | 0x4819 A094 | CMD2_REG_PHY_INVERT_CLKOUT_0 | Command 2 Invert Clockout Selection |
| 0x4819 80A8 | 0x4819 A0A8 | DATA0_IO_CONFIG_I_0 | Data Macro 0 Data Pad Configuration |
| 0x4819 80AC | 0x4819 A0AC | DATA0_IO_CONFIG_I_CLK_0 | Data Macro 0 Data Strobe Pad Configuration |
| 0x4819 80B0 | 0x4819 A0B0 | DATA0_IO_CONFIG_SR_0 | Data Macro 0 Data Slew Rate Configuration |
| 0x4819 80B4 | 0x4819 A0B4 | DATA0_IO_CONFIG_SR_CLK_0 | Data Macro 0 Data Strobe Slew Rate Configuration |
| 0x4819 80C8 | 0x4819 A0C8 | DATA0_REG_PHY_RD_DQS_SLAVE_RATIO_0 | Data Macro 0 Read DQS Slave Ratio |
| 0x4819 80DC | 0x4819 A0DC | DATA0_REG_PHY_WR_DQS_SLAVE_RATIO_0 | Data Macro 0 Write DQS Slave Ratio |
| 0x4819 80F0 | 0x4819 A0F0 | DATA0_REG_PHY_WRLVL_INIT_RATIO_0 | Data Macro 0 Write Leveling Init Ratio |
| 0x4819 80F8 | 0x4819 A0F8 | DATA0_REG_PHY_WRLVL_INIT_MODE_0 | Data Macro 0 Write Leveling Init Mode Ratio Selection |
| 0x4819 80FC | 0x4819 A0FC | DATA0_REG_PHY_GATELVL_INIT_RATIO_0 | Data Macro 0 DQS Gate Training Init Ratio |
| 0x4819 8104 | 0x4819 A104 | DATA0_REG_PHY_GATELVL_INIT_MODE_0 | Data Macro 0 DQS Gate Training Init Mode Ratio Selection |
| 0x4819 8108 | 0x4819 A108 | DATA0_REG_PHY_FIFO_WE_SLAVE_RATIO_0 | Data Macro 0 DQS Gate Slave Ratio |
| 0x4819 8120 | 0x4819 A120 | DATA0_REG_PHY_WR_DATA_SLAVE_RATIO_0 | Data Macro 0 Write Data Slave Ratio |
| 0x4819 8134 | 0x4819 A134 | DATA0_REG_PHY_USE_RANK0_DELAYS | Data Macro 0 Delay Selection |
| 0x4819 814C | 0x4819 A14C | DATA1_IO_CONFIG_I_0 | Data Macro 1 Data Pad Configuration |
| 0x4819 8150 | 0x4819 A150 | DATA1_IO_CONFIG_I_CLK_0 | Data Macro 1 Data Strobe Pad Configuration |
| 0x4819 8154 | 0x4819 A154 | DATA1_IO_CONFIG_SR_0 | Data Macro 1 Data Slew Rate Configuration |
| 0x4819 8158 | 0x4819 A158 | DATA1_IO_CONFIG_SR_CLK_0 | Data Macro 1 Data Strobe Slew Rate Configuration |
| 0x4819 816C | 0x4819 A16C | DATA1_REG_PHY_RD_DQS_SLAVE_RATIO_0 | Data Macro 1 Read DQS Slave Ratio |
| 0x4819 8180 | 0x4819 A180 | DATA1_REG_PHY_WR_DQS_SLAVE_RATIO_0 | Data Macro 1 Write DQS Slave Ratio |
| 0x4819 8194 | 0x4819 A194 | DATA1_REG_PHY_WRLVL_INIT_RATIO_0 | Data Macro 1 Write Leveling Init Ratio |
| 0x4819 819C | 0x4819 A19C | DATA1_REG_PHY_WRLVL_INIT_MODE_0 | Data Macro 1 Write Leveling Init Mode Ratio Selection |
| 0x4819 81A0 | 0x4819 A1A0 | DATA1_REG_PHY_GATELVL_INIT_RATIO_0 | Data Macro 1 DQS Gate Training Init Ratio |
| 0x4819 81A8 | 0x4819 A1A8 | DATA1_REG_PHY_GATELVL_INIT_MODE_0 | Data Macro 1 DQS Gate Training Init Mode Ratio Selection |
| 0x4819 81AC | 0x4819 A1AC | DATA1_REG_PHY_FIFO_WE_SLAVE_RATIO_0 | Data Macro 1 DQS Gate Slave Ratio |
| 0x4819 81C4 | 0x4819 A1C4 | DATA1_REG_PHY_WR_DATA_SLAVE_RATIO_0 | Data Macro 1 Write Data Slave Ratio |
| 0x4819 81D8 | 0x4819 A1D8 | DATA1_REG_PHY_USE_RANK0_DELAYS | Data Macro 1 Delay Selection |
| 0x4819 81F0 | 0x4819 A1F0 | DATA2_IO_CONFIG_I_0 | Data Macro 2 Data Pad Configuration |
| 0x4819 81F4 | 0x4819 A1F4 | DATA2_IO_CONFIG_I_CLK_0 | Data Macro 2 Data Strobe Pad Configuration |
| 0x4819 81F8 | 0x4819 A1F8 | DATA2_IO_CONFIG_SR_0 | Data Macro 2 Data Slew Rate Configuration |
| 0x4819 81FC | 0x4819 A1FC | DATA2_IO_CONFIG_SR_CLK_0 | Data Macro 2 Data Strobe Slew Rate Configuration |
| 0x4819 8210 | 0x4819 A210 | DATA2_REG_PHY_RD_DQS_SLAVE_RATIO_0 | Data Macro 2 Read DQS Slave Ratio |
| 0x4819 8224 | 0x4819 A224 | DATA2_REG_PHY_WR_DQS_SLAVE_RATIO_0 | Data Macro 2 Write DQS Slave Ratio |

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**Table 9-27. DDR2 and DDR3 PHY Registers (continued)**

| DDR0 HEX ADDRESS | DDR1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4819 8238 | 0x4819 A238 | DATA2_REG_PHY_WRLVL_INIT_RATIO_0 | Data Macro 2 Write Leveling Init Ratio |
| 0x4819 8240 | 0x4819 A240 | DATA2_REG_PHY_WRLVL_INIT_MODE_0 | Data Macro 2 Write Leveling Init Mode Ratio Selection |
| 0x4819 8244 | 0x4819 A244 | DATA2_REG_PHY_GATELVL_INIT_RATIO_0 | Data Macro 2 DQS Gate Training Init Ratio |
| 0x4819 824C | 0x4819 A24C | DATA2_REG_PHY_GATELVL_INIT_MODE_0 | Data Macro 2 DQS Gate Training Init Mode Ratio Selection |
| 0x4819 8250 | 0x4819 A250 | DATA2_REG_PHY_FIFO_WE_SLAVE_RATIO_0 | Data Macro 2 DQS Gate Slave Ratio |
| 0x4819 8268 | 0x4819 A268 | DATA2_REG_PHY_WR_DATA_SLAVE_RATIO_0 | Data Macro 2 Write Data Slave Ratio |
| 0x4819 827C | 0x4819 A27C | DATA2_REG_PHY_USE_RANK0_DELAYS | Data Macro 2 Delay Selection |
| 0x4819 8294 | 0x4819 A294 | DATA3_IO_CONFIG_I_0 | Data Macro 3 Data Pad Configuration |
| 0x4819 8298 | 0x4819 A298 | DATA3_IO_CONFIG_I_CLK_0 | Data Macro 3 Data Strobe Pad Configuration |
| 0x4819 829C | 0x4819 A29C | DATA3_IO_CONFIG_SR_0 | Data Macro 3 Data Slew Rate Configuration |
| 0x4819 82A0 | 0x4819 A2A0 | DATA3_IO_CONFIG_SR_CLK_0 | Data Macro 3 Data Strobe Slew Rate Configuration |
| 0x4819 82B4 | 0x4819 A2B4 | DATA3_REG_PHY_RD_DQS_SLAVE_RATIO_0 | Data Macro 3 Read DQS Slave Ratio |
| 0x4819 82C8 | 0x4819 A2C8 | DATA3_REG_PHY_WR_DQS_SLAVE_RATIO_0 | Data Macro 3 Write DQS Slave Ratio |
| 0x4819 82DC | 0x4819 A2DC | DATA3_REG_PHY_WRLVL_INIT_RATIO_0 | Data Macro 3 Write Leveling Init Ratio |
| 0x4819 82E4 | 0x4819 A2E4 | DATA3_REG_PHY_WRLVL_INIT_MODE_0 | Data Macro 3 Write Leveling Init Mode Ratio Selection |
| 0x4819 82E8 | 0x4819 A2E8 | DATA3_REG_PHY_GATELVL_INIT_RATIO_0 | Data Macro 3 DQS Gate Training Init Ratio |
| 0x4819 82F0 | 0x4819 A2F0 | DATA3_REG_PHY_GATELVL_INIT_MODE_0 | Data Macro 3 DQS Gate Training Init Mode Ratio Selection |
| 0x4819 82F4 | 0x4819 A2F4 | DATA3_REG_PHY_FIFO_WE_SLAVE_RATIO_0 | Data Macro 3 DQS Gate Slave Ratio |
| 0x4819 830C | 0x4819 A30C | DATA3_REG_PHY_WR_DATA_SLAVE_RATIO_0 | Data Macro 3 Write Data Slave Ratio |
| 0x4819 8320 | 0x4819 A320 | DATA3_REG_PHY_USE_RANK0_DELAYS | Data Macro 3 Delay Selection |
| 0x4819 8358 | 0x4819 A358 | DDR_VTP_CTRL_0 | DDR VTP Control |

### 9.3.5 DDR2 and DDR3 Memory Controller Electrical Data and Timing

Section 9.3.1, *DDR2 Routing Specifications* and Section 9.3.2, *DDR3 Routing Specifications* specify a complete DDR2 and DDR3 interface solution for the device. TI has performed the simulation and system characterization to ensure all DDR2 and DDR3 interface timings in this solution are met.

TI ***only*** supports board designs that follow the specifications outlined in the *DDR2 Routing Specifications* and *DDR3 Routing Specifications* sections of this data sheet.


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## 9.4 Emulation Features and Capability

### 9.4.1 Advanced Event Triggering (AET)

The device supports Advanced Event Triggering (AET). This capability can be used to debug complex problems as well as understand performance characteristics of user applications. AET provides the following capabilities:

- **Hardware Program Breakpoints:** specify addresses or address ranges that can generate events such as halting the processor or triggering the trace capture.
- **Data Watchpoints:** specify data variable addresses, address ranges, or data values that can generate events such as halting the processor or triggering the trace capture.
- **Counters:** count the occurrence of an event or cycles for performance monitoring.
- **State Sequencing:** allows combinations of hardware program breakpoints and data watchpoints to precisely generate events for complex sequences.

For more information on AET, see the following documents:

- *Using Advanced Event Triggering to Find and Fix Intermittent Real-Time Bugs* application report (literature number SPRA753)
- *Using Advanced Event Triggering to Debug Real-Time Problems in High Speed Embedded Microprocessor Systems* application report (literature number SPRA387)

### 9.4.2 Trace

The device supports Trace at the Cortex™-A8, C674x, and System levels. Trace is a debug technology that provides a detailed, historical account of application code execution, timing, and data accesses. Trace collects, compresses, and exports debug information for analysis. The debug information can be exported to the Embedded Trace Buffer (ETB), or to the 5-pin Trace Interface (system trace only). Trace works in real-time and does not impact the execution of the system.

For more information on board design guidelines for Trace Advanced Emulation, see the *Emulation and Trace Headers Technical Reference Manual* (literature number SPRU655).

### 9.4.3 IEEE 1149.1 JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture) interface is used for BSDL testing and emulation of the device. The $\overline{\text{TRST}}$ pin only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. For maximum reliability, the device includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ is always asserted upon power up and the device's internal emulation logic is always properly initialized. JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of a pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the device after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary-scan operations.

The main JTAG features include:

- 32KB embedded trace buffer (ETB)
- 5-pin system trace interface for debug
- Supports Advanced Event Triggering (AET)
- All processors can be emulated via JTAG ports
- All functions on EMU pins of the device:
  - EMU[1:0] - cross-triggering, boot mode (WIR), STM trace
  - EMU[4:2] - STM trace only (single direction)
  - EMU[2] - only valid pin to use as clock

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### 9.4.3.1 JTAG ID (JTAGID) Register Description

**Table 9-28. JTAG ID Register(1)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0600 | JTAGID | JTAG Identification Register(2) |

(1) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.
(2) Read-only. Provides the device 32-bit JTAG ID.

The JTAG ID register is a read-only register that identifies to the customer the JTAG device ID. For this device, the JTAG ID register resides at address location 0x4814 0600. The register hex value for the device depends on the silicon revision being used. For more information, see the *TMS320DM816x DaVinci Digital Media Processors Silicon Errata* (literature number SPRZ329). For the actual register bit names and their associated bit field descriptions, see Figure 9-40 and Table 9-29.

| 31 28 | 27 12 | 11 1 | 0 |
|---|---|---|---|
| VARIANT (4-bit) | PART NUMBER (16-bit) | MANUFACTURER (11-bit) | LSB |
| R-x | R-1011 1000 0001 1110 | R-0000 0010 111 | R-1 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 9-40. JTAG ID Register Description - 0x4814 0600**

**Table 9-29. JTAG ID Register Selection Bit Descriptions**

| Bit | Field | Description |
|---|---|---|
| 31:28 | VARIANT | Variant (4-bit) value. Device value: The value of this field depends on the silicon revision being used. For more information, see the *TMS320DM816x DaVinci Digital Media Processors Silicon Errata* (literature number SPRZ329). |
| 27:12 | PART NUMBER | Part Number (16-bit) value. Device value: 0xB81E |
| 11:1 | MANUFACTURER | Manufacturer (11-bit) value. Device value: 0x017 |
| 0 | LSB | LSB. This bit is read as a 1 for this device. |

### 9.4.3.2 JTAG Electrical Data and Timing

**Table 9-30. Timing Requirements for IEEE 1149.1 JTAG**

(see Figure 9-41)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 51.15 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 20.46 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 20.46 | | ns |
| 3 | $t_{su(TDI-TCK)}$ | Input setup time, TDI valid to TCK high (20% of ($t_c$ * 0.5)) | 5.115 | | ns |
| 3 | $t_{su(TMS-TCK)}$ | Input setup time, TMS valid to TCK high (20% of ($t_c$ * 0.5)) | 5.115 | | ns |
| 4 | $t_{h(TCK-TDI)}$ | Input hold time, TDI valid from TCK high | 10 | | ns |
| | $t_{h(TCK-TMS)}$ | Input hold time, TMS valid from TCK high | 10 | | ns |

**Table 9-31. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG**

(see Figure 9-41)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 2 | $t_{d(TCKL-TDOV)}$ | Delay time, TCK low to TDO valid | 0 | 23.575(1) | ns |

(1) (0.5 * $t_c$) - 2


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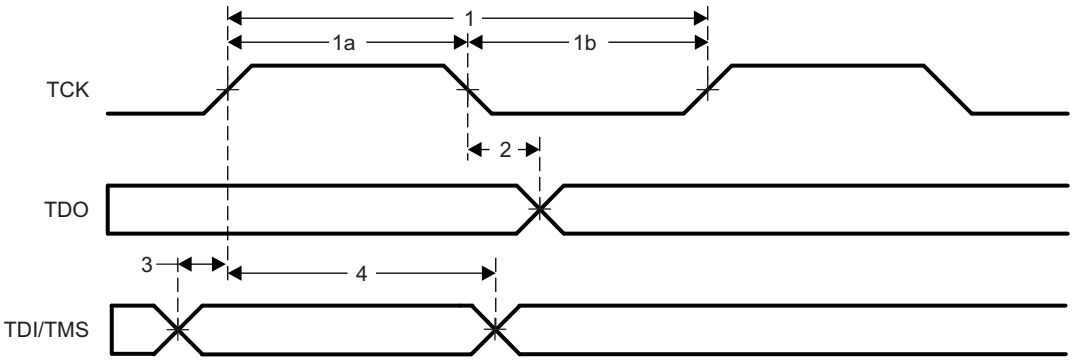


**Figure 9-41. JTAG Timing**

**Table 9-32. Timing Requirements for IEEE 1149.1 JTAG With RTCK**

(see Figure 9-41)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 51.15 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 20.46 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 20.46 | | ns |
| 3 | $t_{su(TDI-TCK)}$ | Input setup time, TDI valid to TCK high (20% of ($t_c$ * 0.5)) | 5.115 | | ns |
| 3 | $t_{su(TMS-TCK)}$ | Input setup time, TMS valid to TCK high (20% of ($t_c$ * 0.5)) | 5.115 | | ns |
| 4 | $t_{h(TCK-TDI)}$ | Input hold time, TDI valid from TCK high | 10 | | ns |
| | $t_{h(TCK-TMS)}$ | Input hold time, TMS valid from TCK high | 10 | | ns |

**Table 9-33. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG With RTCK**

(see Figure 9-42)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 5 | $t_{d(TCK-RTCK)}$ | Delay time, TCK to RTCK with no selected subpaths (that is, ICEPick module is the only tap selected - when the ARM is in the scan chain, the delay time is a function of the ARM functional clock.) | 0 | 21 | ns |
| 6 | $t_{c(RTCK)}$ | Cycle time, RTCK | 51.15 | | ns |
| 7 | $t_{w(RTCKH)}$ | Pulse duration, RTCK high (40% of $t_c$) | 20.46 | | ns |
| 8 | $t_{w(RTCKL)}$ | Pulse duration, RTCK low (40% of $t_c$) | 20.46 | | ns |

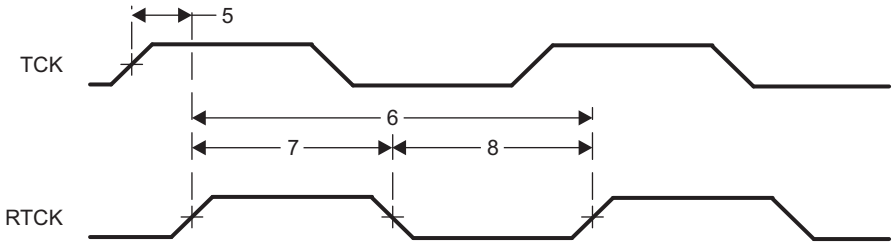


**Figure 9-42. JTAG With RTCK Timing**

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### 9.4.4 IEEE 1149.7 cJTAG

Besides the standard (legacy) JTAG mode of operation, the target debug interface can also be switched to a compressed JTAG (cJTAG) mode of operation, commonly referred to as IEEE1149.7 standard. An IEEE1149.7 adapter module runs a 2-pin communication protocol on top of an IEEE1149.1 JTAG TAP. The debug-IP logic serializes the IEEE1149.1 transactions, using a variety of compression formats, to reduce the number of pins needed to implement a JTAG debug port. This device implements only a subset of the IEEE1149.7 protocol; it supports Class 0 and Class 1 operation. On this device the cJTAG ID[7:0] is tied to 0x00.

**NOTE**

The default setting of the scan port is IEEE 1149.1. A cJTAG emulator connected only to TCLK and TMS can re-configure the port to cJTAG by scanning in a special command sequence. For the scan sequence required to switch modes, see the IEEE1149.7 specification.


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## 9.5 Enhanced Direct Memory Access (EDMA) Controller

The EDMA controller handles all data transfers between memories and the device slave peripherals on the device. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses.

### *9.5.1 EDMA Channel Synchronization Events*

The EDMA channel controller supports up to 64 channels that service peripherals and memory. Each EDMA channel is mapped to a default EDMA synchronization event as shown in Table 9-34. By default, each event uses the parameter entry that matches its event number. However, because the device includes a channel mapping feature, each event may be mapped to any of 512 parameter table entries. For more detailed information on the EDMA module and how EDMA events are enabled, captured, processed, linked, chained, and cleared, see the EDMA chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

**Table 9-34. EDMA Default Synchronization Events**

| EVENT NUMBER | DEFAULT EVENT NAME | DEFAULT EVENT DESCRIPTION |
|---|---|---|
| 0 - 7 | - | Unused |
| 8 | AXEVT0 | McASP0 Transmit |
| 9 | AREVT0 | McASP0 Receive |
| 10 | AXEVT1 | McASP1 Transmit |
| 11 | AREVT1 | McASP1 Receive |
| 12 | AXEVT2 | McASP2 Transmit |
| 13 | AREVT2 | McASP2 Receive |
| 14 | BXEVT | McBSP Transmit |
| 15 | BREVT | McBSP Receive |
| 16 | SPIXEVT0 | SPI0 Transmit 0 |
| 17 | SPIREVT0 | SPI0 Receive 0 |
| 18 | SPIXEVT1 | SPI0 Transmit 1 |
| 19 | SPIREVT1 | SPI0 Receive 1 |
| 20 | SPIXEVT2 | SPI0 Transmit 2 |
| 21 | SPIREVT2 | SPI0 Receive 2 |
| 22 | SPIXEVT3 | SPI0 Transmit 3 |
| 23 | SPIREVT3 | SPI0 Receive 3 |
| 24 | SDTXEVT | SD0 Transmit |
| 25 | SDRXEVT | SD0 Receive |
| 26 | UTXEVT0 | UART0 Transmit |
| 27 | URXEVT0 | UART0 Receive |
| 28 | UTXEVT1 | UART1 Transmit |
| 29 | URXEVT1 | UART1 Receive |
| 30 | UTXEVT2 | UART2 Transmit |
| 31 | URXEVT2 | UART2 Receive |
| 32 - 47 | - | Unused |
| 48 | TINT4 | TIMER4 |
| 49 | TINT5 | TIMER5 |
| 50 | TINT6 | TIMER6 |
| 51 | TINT7 | TIMER7 |
| 52 | GPMCEVT | GPMC |
| 53 | HDMIEVT | HDMI |
| 54 - 57 | - | Unused |
| 58 | I2CTXEVT0 | I2C0 Transmit |

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**Table 9-34. EDMA Default Synchronization Events (continued)**

| EVENT NUMBER | DEFAULT EVENT NAME | DEFAULT EVENT DESCRIPTION |
|---|---|---|
| 59 | I2CRXEVT0 | I2C0 Receive |
| 60 | I2CTXEVT1 | I2C1 Transmit |
| 61 | I2CRXEVT1 | I2C1 Receive |
| 62 - 63 | - | Unused |

### 9.5.2 EDMA Peripheral Register Descriptions

**Table 9-35. EDMA Channel Controller (EDMA TPCC) Control Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4900 0000 | PID | Peripheral Identification |
| 0x4900 0004 | CCCFG | EDMA3CC Configuration |
| 0x4900 0100 - 0x4900 01FC | DCHMAP0-63 | DMA Channel 0-63 Mappings |
| 0x4900 0200 | QCHMAP0 | QDMA Channel 0 Mapping |
| 0x4900 0204 | QCHMAP1 | QDMA Channel 1 Mapping |
| 0x4900 0208 | QCHMAP2 | QDMA Channel 2 Mapping |
| 0x4900 020C | QCHMAP3 | QDMA Channel 3 Mapping |
| 0x4900 0210 | QCHMAP4 | QDMA Channel 4 Mapping |
| 0x4900 0214 | QCHMAP5 | QDMA Channel 5 Mapping |
| 0x4900 0218 | QCHMAP6 | QDMA Channel 6 Mapping |
| 0x4900 021C | QCHMAP7 | QDMA Channel 7 Mapping |
| 0x4900 0240 | DMAQNUM0 | DMA Queue Number 0 |
| 0x4900 0244 | DMAQNUM1 | DMA Queue Number 1 |
| 0x4900 0248 | DMAQNUM2 | DMA Queue Number 2 |
| 0x4900 024C | DMAQNUM3 | DMA Queue Number 3 |
| 0x4900 0250 | DMAQNUM4 | DMA Queue Number 4 |
| 0x4900 0254 | DMAQNUM5 | DMA Queue Number 5 |
| 0x4900 0258 | DMAQNUM6 | DMA Queue Number 6 |
| 0x4900 025C | DMAQNUM7 | DMA Queue Number 7 |
| 0x4900 0260 | QDMAQNUM | QDMA Queue Number |
| 0x4900 0284 | QUEPRI | Queue Priority |
| 0x4900 0300 | EMR | Event Missed |
| 0x4900 0304 | EMRH | Event Missed High |
| 0x4900 0308 | EMCR | Event Missed Clear |
| 0x4900 030C | EMCRH | Event Missed Clear High |
| 0x4900 0310 | QEMR | QDMA Event Missed |
| 0x4900 0314 | QEMCR | QDMA Event Missed Clear |
| 0x4900 0318 | CCERR | EDMA3CC Error |
| 0x4900 031C | CCERRCLR | EDMA3CC Error Clear |
| 0x4900 0320 | EEVAL | Error Evaluate |
| 0x4900 0340 | DRAE0 | DMA Region Access Enable for Region 0 |
| 0x4900 0344 | DRAEH0 | DMA Region Access Enable High for Region 0 |
| 0x4900 0348 | DRAE1 | DMA Region Access Enable for Region 1 |
| 0x4900 034C | DRAEH1 | DMA Region Access Enable High for Region 1 |
| 0x4900 0350 | DRAE2 | DMA Region Access Enable for Region 2 |
| 0x4900 0354 | DRAEH2 | DMA Region Access Enable High for Region 2 |
| 0x4900 0358 | DRAE3 | DMA Region Access Enable for Region 3 |
| 0x4900 035C | DRAEH3 | DMA Region Access Enable High for Region 3 |


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**Table 9-35. EDMA Channel Controller (EDMA TPCC) Control Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4900 0360 | DRAE4 | DMA Region Access Enable for Region 4 |
| 0x4900 0364 | DRAEH4 | DMA Region Access Enable High for Region 4 |
| 0x4900 0368 | DRAE5 | DMA Region Access Enable for Region 5 |
| 0x4900 036C | DRAEH5 | DMA Region Access Enable High for Region 5 |
| 0x4900 0370 | DRAE6 | DMA Region Access Enable for Region 6 |
| 0x4900 0374 | DRAEH6 | DMA Region Access Enable High for Region 6 |
| 0x4900 0378 | DRAE7 | DMA Region Access Enable for Region 7 |
| 0x4900 037C | DRAEH7 | DMA Region Access Enable High for Region 7 |
| 0x4900 0380 - 0x4900 039C | QRAE0-7 | QDMA Region Access Enable for Region 0-7 |
| 0x4900 0400 - 0x4900 04FC | Q0E0-Q3E15 | Event Queue Entry Q0E0-Q3E15 |
| 0x4900 0600 - 0x4900 060C | QSTAT0-3 | Queue Status 0-3 |
| 0x4900 0620 | QWMTHRA | Queue Watermark Threshold A |
| 0x4900 0640 | CCSTAT | EDMA3CC Status |
| 0x4900 0800 | MPFAR | Memory Protection Fault Address |
| 0x4900 0804 | MPFSR | Memory Protection Fault Status |
| 0x4900 0808 | MPFCR | Memory Protection Fault Command |
| 0x4900 080C | MPPAG | Memory Protection Page Attribute Global |
| 0x4900 0810 - 0x4900 082C | MPPA0-7 | Memory Protection Page Attribute 0-7 |
| 0x4900 1000 | ER | Event |
| 0x4900 1004 | ERH | Event High |
| 0x4900 1008 | ECR | Event Clear |
| 0x4900 100C | ECRH | Event Clear High |
| 0x4900 1010 | ESR | Event Set |
| 0x4900 1014 | ESRH | Event Set High |
| 0x4900 1018 | CER | Chained Event |
| 0x4900 101C | CERH | Chained Event High |
| 0x4900 1020 | EER | Event Enable |
| 0x4900 1024 | EERH | Event Enable High |
| 0x4900 1028 | EECR | Event Enable Clear |
| 0x4900 102C | EECRH | Event Enable Clear High |
| 0x4900 1030 | EESR | Event Enable Set |
| 0x4900 1034 | EESRH | Event Enable Set High |
| 0x4900 1038 | SER | Secondary Event |
| 0x4900 103C | SERH | Secondary Event High |
| 0x4900 1040 | SECR | Secondary Event Clear |
| 0x4900 1044 | SECRH | Secondary Event Clear High |
| 0x4900 1050 | IER | Interrupt Enable |
| 0x4900 1054 | IERH | Interrupt Enable High |
| 0x4900 1058 | IECR | Interrupt Enable Clear |
| 0x4900 105C | IECRH | Interrupt Enable Clear High |
| 0x4900 1060 | IESR | Interrupt Enable Set |
| 0x4900 1064 | IESRH | Interrupt Enable Set High |
| 0x4900 1068 | IPR | Interrupt Pending |
| 0x4900 106C | IPRH | Interrupt Pending High |
| 0x4900 1070 | ICR | Interrupt Clear |
| 0x4900 1074 | ICRH | Interrupt Clear High |
| 0x4900 1078 | IEVAL | Interrupt Evaluate |

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**Table 9-35. EDMA Channel Controller (EDMA TPCC) Control Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4900 1080 | QER | QDMA Event |
| 0x4900 1084 | QEER | QDMA Event Enable |
| 0x4900 1088 | QEECR | QDMA Event Enable Clear |
| 0x4900 108C | QEESR | QDMA Event Enable Set |
| 0x4900 1090 | QSER | QDMA Secondary Event |
| 0x4900 1094 | QSECR | QDMA Secondary Event Clear |
| **Shadow Region 0 Channel Registers** | | |
| 0x4900 2000 | ER | Event |
| 0x4900 2004 | ERH | Event High |
| 0x4900 2008 | ECR | Event Clear |
| 0x4900 200C | ECRH | Event Clear High |
| 0x4900 2010 | ESR | Event Set |
| 0x4900 2014 | ESRH | Event Set High |
| 0x4900 2018 | CER | Chained Event |
| 0x4900 201C | CERH | Chained Event High |
| 0x4900 2020 | EER | Event Enable |
| 0x4900 2024 | EERH | Event Enable High |
| 0x4900 2028 | EECR | Event Enable Clear |
| 0x4900 202C | EECRH | Event Enable Clear High |
| 0x4900 2030 | EESR | Event Enable Set |
| 0x4900 2034 | EESRH | Event Enable Set High |
| 0x4900 2038 | SER | Secondary Event |
| 0x4900 203C | SERH | Secondary Event High |
| 0x4900 2040 | SECR | Secondary Event Clear |
| 0x4900 2044 | SECRH | Secondary Event Clear High |
| 0x4900 2050 | IER | Interrupt Enable |
| 0x4900 2054 | IERH | Interrupt Enable High |
| 0x4900 2058 | IECR | Interrupt Enable Clear |
| 0x4900 205C | IECRH | Interrupt Enable Clear High |
| 0x4900 2060 | IESR | Interrupt Enable Set |
| 0x4900 2064 | IESRH | Interrupt Enable Set High |
| 0x4900 2068 | IPR | Interrupt Pending |
| 0x4900 206C | IPRH | Interrupt Pending High |
| 0x4900 2070 | ICR | Interrupt Clear |
| 0x4900 2074 | ICRH | Interrupt Clear High |
| 0x4900 2078 | IEVAL | Interrupt Evaluate |
| 0x4900 2080 | QER | QDMA Event |
| 0x4900 2084 | QEER | QDMA Event Enable |
| 0x4900 2088 | QEECR | QDMA Event Enable Clear |
| 0x4900 208C | QEESR | QDMA Event Enable Set |
| 0x4900 2090 | QSER | QDMA Secondary Event |
| 0x4900 2094 | QSECR | QDMA Secondary Event Clear |
| 0x4900 2200 - 0x4900 2294 | - | Shadow Region 1 Channels |
| 0x4900 2400 - 0x4900 2494 | - | Shadow Region 2 Channels |
| ... | | ... |
| 0x4900 2E00 - 0x4900 2E94 | - | Shadow Channels for MP Space 7 |


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**Table 9-36. EDMA Transfer Controller (EDMA TPTC) Control Registers**

| TPTC0 HEX ADDRESS | TPTC1 HEX ADDRESS | TPTC2 HEX ADDRESS | TPTC3 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|
| 0x4980 0000 | 0x4990 0000 | 0x49A0 0000 | 0x49B0 0000 | PID | Peripheral Identification |
| 0x4980 0004 | 0x4990 0004 | 0x49A0 0004 | 0x49B0 0004 | TCCFG | EDMA3TC Configuration |
| 0x4980 0100 | 0x4990 0100 | 0x49A0 0100 | 0x49B0 0100 | TCSTAT | EDMA3TC Channel Status |
| 0x4980 0120 | 0x4990 0120 | 0x49A0 0120 | 0x49B0 0120 | ERRSTAT | Error Status |
| 0x4980 0124 | 0x4990 0124 | 0x49A0 0124 | 0x49B0 0124 | ERREN | Error Enable |
| 0x4980 0128 | 0x4990 0128 | 0x49A0 0128 | 0x49B0 0128 | ERRCLR | Error Clear |
| 0x4980 012C | 0x4990 012C | 0x49A0 012C | 0x49B0 012C | ERRDET | Error Details |
| 0x4980 0130 | 0x4990 0130 | 0x49A0 0130 | 0x49B0 0130 | ERRCMD | Error Interrupt Command |
| 0x4980 0140 | 0x4990 0140 | 0x49A0 0140 | 0x49B0 0140 | RDRATE | Read Rate Register |
| 0x4980 0240 | 0x4990 0240 | 0x49A0 0240 | 0x49B0 0240 | SAOPT | Source Active Options |
| 0x4980 0244 | 0x4990 0244 | 0x49A0 0244 | 0x49B0 0244 | SASRC | Source Active Source Address |
| 0x4980 0248 | 0x4990 0248 | 0x49A0 0248 | 0x49B0 0248 | SACNT | Source Active Count |
| 0x4980 024C | 0x4990 024C | 0x49A0 024C | 0x49B0 024C | SADST | Source Active Destination Address |
| 0x4980 0250 | 0x4990 0250 | 0x49A0 0250 | 0x49B0 0250 | SABIDX | Source Active Source B-Index |
| 0x4980 0254 | 0x4990 0254 | 0x49A0 0254 | 0x49B0 0254 | SAMPPRXY | Source Active Memory Protection Proxy |
| 0x4980 0258 | 0x4990 0258 | 0x49A0 0258 | 0x49B0 0258 | SACNTRLD | Source Active Count Reload |
| 0x4980 025C | 0x4990 025C | 0x49A0 025C | 0x49B0 025C | SASRCBREF | Source Active Source Address B-Reference |
| 0x4980 0260 | 0x4990 0260 | 0x49A0 0260 | 0x49B0 0260 | SADSTBREF | Source Active Destination Address B-Reference |
| 0x4980 0280 | 0x4990 0280 | 0x49A0 0280 | 0x49B0 0280 | DFCNTRLD | Destination FIFO Set Count Reload |
| 0x4980 0284 | 0x4990 0284 | 0x49A0 0284 | 0x49B0 0284 | DFSRCBREF | Destination FIFO Set Destination Address B Reference |
| 0x4980 0288 | 0x4990 0288 | 0x49A0 0288 | 0x49B0 0288 | DFDSTBREF | Destination FIFO Set Destination Address B Reference |
| 0x4980 0300 | 0x4990 0300 | 0x49A0 0300 | 0x49B0 0300 | DFOPT0 | Destination FIFO Options 0 |
| 0x4980 0304 | 0x4990 0304 | 0x49A0 0304 | 0x49B0 0304 | DFSRC0 | Destination FIFO Source Address 0 |
| 0x4980 0308 | 0x4990 0308 | 0x49A0 0308 | 0x49B0 0308 | DFCNT0 | Destination FIFO Count 0 |
| 0x4980 030C | 0x4990 030C | 0x49A0 030C | 0x49B0 030C | DFDST0 | Destination FIFO Destination Address 0 |
| 0x4980 0310 | 0x4990 0310 | 0x49A0 0310 | 0x49B0 0310 | DFBIDX0 | Destination FIFO BIDX 0 |
| 0x4980 0314 | 0x4990 0314 | 0x49A0 0314 | 0x49B0 0314 | DFMPPRXY0 | Destination FIFO Memory Protection Proxy 0 |
| 0x4980 0340 | 0x4990 0340 | 0x49A0 0340 | 0x49B0 0340 | DFOPT1 | Destination FIFO Options 1 |
| 0x4980 0344 | 0x4990 0344 | 0x49A0 0344 | 0x49B0 0344 | DFSRC1 | Destination FIFO Source Address 1 |
| 0x4980 0348 | 0x4990 0348 | 0x49A0 0348 | 0x49B0 0348 | DFCNT1 | Destination FIFO Count 1 |
| 0x4980 034C | 0x4990 034C | 0x49A0 034C | 0x49B0 034C | DFDST1 | Destination FIFO Destination Address 1 |
| 0x4980 0350 | 0x4990 0350 | 0x49A0 0350 | 0x49B0 0350 | DFBIDX1 | Destination FIFO BIDX 1 |
| 0x4980 0354 | 0x4990 0354 | 0x49A0 0354 | 0x49B0 0354 | DFMPPRXY1 | Destination FIFO Memory Protection Proxy 1 |
| 0x4980 0380 | 0x4990 0380 | 0x49A0 0380 | 0x49B0 0380 | DFOPT2 | Destination FIFO Options 2 |
| 0x4980 0384 | 0x4990 0384 | 0x49A0 0384 | 0x49B0 0384 | DFSRC2 | Destination FIFO Source Address 2 |
| 0x4980 0388 | 0x4990 0388 | 0x49A0 0388 | 0x49B0 0388 | DFCNT2 | Destination FIFO Count 2 |

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**Table 9-36. EDMA Transfer Controller (EDMA TPTC) Control Registers (continued)**

| TPTC0 HEX ADDRESS | TPTC1 HEX ADDRESS | TPTC2 HEX ADDRESS | TPTC3 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|
| 0x4980 038C | 0x4990 038C | 0x49A0 038C | 0x49B0 038C | DFDST2 | Destination FIFO Destination Address 2 |
| 0x4980 0390 | 0x4990 0390 | 0x49A0 0390 | 0x49B0 0390 | DFBIDX2 | Destination FIFO BIDX 2 |
| 0x4980 0394 | 0x4990 0394 | 0x49A0 0394 | 0x49B0 0394 | DFMPPRXY2 | Destination FIFO Memory Protection Proxy 2 |
| 0x4980 03C0 | 0x4990 03C0 | 0x49A0 03C0 | 0x49B0 03C0 | DFOPT3 | Destination FIFO Options 3 |
| 0x4980 03C4 | 0x4990 03C4 | 0x49A0 03C4 | 0x49B0 03C4 | DFSRC3 | Destination FIFO Source Address 3 |
| 0x4980 03C8 | 0x4990 03C8 | 0x49A0 03C8 | 0x49B0 03C8 | DFCNT3 | Destination FIFO Count 3 |
| 0x4980 03CC | 0x4990 03CC | 0x49A0 03CC | 0x49B0 03CC | DFDST3 | Destination FIFO Destination Address 3 |
| 0x4980 03D0 | 0x4990 03D0 | 0x49A0 03D0 | 0x49B0 03D0 | DFBIDX3 | Destination FIFO BIDX 3 |
| 0x4980 03D4 | 0x4990 03D4 | 0x49A0 03D4 | 0x49B0 03D4 | DFMPPRXY3 | Destination FIFO Memory Protection Proxy 3 |


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## 9.6 Ethernet Media Access Controller (EMAC)

The device includes two Ethernet Media Access Controller (EMAC) modules which provide an efficient interface between the device and the networked community. The EMAC supports 10Base-T (10 Mbits per second [Mbps]) and 100Base-TX (100 Mbps) in either half- or full-duplex mode, and 1000Base-T (1000 Mbps) in full-duplex mode, with hardware flow control and quality-of-service (QOS) support. The EMAC controls the flow of packet data from the device to an external PHY. A single MDIO interface is pinned out to control the PHY configuration and status monitoring. Multiple external PHYs can be controlled by the MDIO interface.

The EMAC module conforms to the IEEE 802.3-2002 standard, describing the *Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer* specifications. The IEEE 802.3 standard has also been adopted by ISO/IEC and re-designated as ISO/IEC 8802-3:2000(E). Deviating from this standard, the EMAC module does not use the transmit coding error signal, MTXER. Instead of driving the error pin when an underflow condition occurs on a transmitted frame, the EMAC intentionally generates an incorrect checksum by inverting the frame CRC so that the transmitted frame is detected as an error by the network. In addition, the EMAC IOs operate at 3.3 V and are not compatible with 2.5-V IO signaling; therefore, only Ethernet PHYs with 3.3-V IO interface should be used. The EMAC module incorporates 8K bytes of internal RAM to hold EMAC buffer descriptors and contains the necessary components to enable the EMAC to make efficient use of device memory and control device interrupts.

The EMAC module on the device supports two interface modes: Media Independent Interface (MII) and Gigabit Media Independent Interface (GMII). The MII and GMII interface modes are defined in the IEEE 802.3-2002 standard. The EMAC uses the same pins for the MII and GMII modes of operation. Only one mode can be used at a time.

The MII and GMII modes-of-operation pins are as follows:

- **MII:** EMAC[1:0]_TXCLK, EMAC[1:0]_RXCLK, EMAC[1:0]_TXD[3:0], EMAC[1:0]_RXD[3:0], EMAC[1:0]_TXEN, EMAC[1:0]_RXDV, EMAC[1:0]_RXER, EMAC[1:0]_COL, EMAC[1:0]_CRS, MDIO_MCLK, and MDIO_MDIO.
- **GMII:** EMAC[1:0]_GMTCLK, EMAC[1:0]_TXCLK, EMAC[1:0]_RXCLK, EMAC[1:0]_TXD[7:0], EMAC[1:0]_RXD[7:0], EMAC[1:0]_TXEN, EMAC[1:0]_RXDV, EMAC[1:0]_RXER, EMAC[1:0]_COL, EMAC[1:0]_CRS, MDIO_MCLK, and MDIO_MDIO.

For more detailed information on the EMAC module, see the EMAC and MDIO chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### *9.6.1 EMAC Peripheral Register Descriptions*

**Table 9-37. EMAC Control Registers**

| EMAC0 HEX ADDRESS | EMAC1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4A10 0000 | 0x4A12 0000 | TXIDVER | Transmit Identification and Version |
| 0x4A10 0004 | 0x4A12 0004 | TXCONTROL | Transmit Control |
| 0x4A10 0008 | 0x4A12 0008 | TXTEARDOWN | Transmit Teardown |
| 0x4A10 0010 | 0x4A12 0010 | RXIDVER | Receive Identification and Version |
| 0x4A10 0014 | 0x4A12 0014 | RXCONTROL | Receive Control |
| 0x4A10 0018 | 0x4A12 0018 | RXTEARDOWN | Receive Teardown |
| 0x4A10 0080 | 0x4A12 0080 | TXINTSTATRAW | Transmit Interrupt Status (Unmasked) |
| 0x4A10 0084 | 0x4A12 0084 | TXINTSTATMASKED | Transmit Interrupt Status (Masked) |
| 0x4A10 0088 | 0x4A12 0088 | TXINTMASKSET | Transmit Interrupt Mask Set |
| 0x4A10 008C | 0x4A12 008C | TXINTMASKCLEAR | Transmit Interrupt Clear |
| 0x4A10 0090 | 0x4A12 0090 | MACINVECTOR | MAC Input Vector |
| 0x4A10 0094 | 0x4A12 0094 | MACEOIVECTOR | MAC End of Interrupt Vector |

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**Table 9-37. EMAC Control Registers (continued)**

| EMAC0 HEX ADDRESS | EMAC1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4A10 00A0 | 0x4A12 00A0 | RXINTSTATRAW | Receive Interrupt Status (Unmasked) |
| 0x4A10 00A4 | 0x4A12 00A4 | RXINTSTATMASKED | Receive Interrupt Status (Masked) |
| 0x4A10 00A8 | 0x4A12 00A8 | RXINTMASKSET | Receive Interrupt Mask Set |
| 0x4A10 00AC | 0x4A12 00AC | RXINTMASKCLEAR | Receive Interrupt Mask Clear |
| 0x4A10 00B0 | 0x4A12 00B0 | MACINTSTATRAW | MAC Interrupt Status (Unmasked) |
| 0x4A10 00B4 | 0x4A12 00B4 | MACINTSTATMASKED | MAC Interrupt Status (Masked) |
| 0x4A10 00B8 | 0x4A12 00B8 | MACINTMASKSET | MAC Interrupt Mask Set |
| 0x4A10 00BC | 0x4A12 00BC | MACINTMASKCLEAR | MAC Interrupt Mask Clear |
| 0x4A10 0100 | 0x4A12 0100 | RXMBPENABLE | Receive Multicast, Broadcast, Promiscuous Channel Enable |
| 0x4A10 0104 | 0x4A12 0104 | RXUNICASTSET | Receive Unicast Enable Set |
| 0x4A10 0108 | 0x4A12 0108 | RXUNICASTCLEAR | Receive Unicast Clear |
| 0x4A10 010C | 0x4A12 010C | RXMAXLEN | Receive Maximum Length |
| 0x4A10 0110 | 0x4A12 0110 | RXBUFFEROFFSET | Receive Buffer Offset |
| 0x4A10 0114 | 0x4A12 0114 | RXFILTERLOWTHRESH | Receive Filter Low Priority Frame Threshold |
| 0x4A10 0120 | 0x4A12 0120 | RX0FLOWTHRESH | Receive Channel 0 Flow Control Threshold |
| 0x4A10 0124 | 0x4A12 0124 | RX1FLOWTHRESH | Receive Channel 1 Flow Control Threshold |
| 0x4A10 0128 | 0x4A12 0128 | RX2FLOWTHRESH | Receive Channel 2 Flow Control Threshold |
| 0x4A10 012C | 0x4A12 012C | RX3FLOWTHRESH | Receive Channel 3 Flow Control Threshold |
| 0x4A10 0130 | 0x4A12 0130 | RX4FLOWTHRESH | Receive Channel 4 Flow Control Threshold |
| 0x4A10 0134 | 0x4A12 0134 | RX5FLOWTHRESH | Receive Channel 5 Flow Control Threshold |
| 0x4A10 0138 | 0x4A12 0138 | RX6FLOWTHRESH | Receive Channel 6 Flow Control Threshold |
| 0x4A10 013C | 0x4A12 013C | RX7FLOWTHRESH | Receive Channel 7 Flow Control Threshold |
| 0x4A10 0140 | 0x4A12 0140 | RX0FREEBUFFER | Receive Channel 0 Free Buffer Count |
| 0x4A10 0144 | 0x4A12 0144 | RX1FREEBUFFER | Receive Channel 1 Free Buffer Count |
| 0x4A10 0148 | 0x4A12 0148 | RX2FREEBUFFER | Receive Channel 2 Free Buffer Count |
| 0x4A10 014C | 0x4A12 014C | RX3FREEBUFFER | Receive Channel 3 Free Buffer Count |
| 0x4A10 0150 | 0x4A12 0150 | RX4FREEBUFFER | Receive Channel 4 Free Buffer Count |
| 0x4A10 0154 | 0x4A12 0154 | RX5FREEBUFFER | Receive Channel 5 Free Buffer Count |
| 0x4A10 0158 | 0x4A12 0158 | RX6FREEBUFFER | Receive Channel 6 Free Buffer Count |
| 0x4A10 015C | 0x4A12 015C | RX7FREEBUFFER | Receive Channel 7 Free Buffer Count |
| 0x4A10 0160 | 0x4A12 0160 | MACCONTROL | MAC Control |
| 0x4A10 0164 | 0x4A12 0164 | MACSTATUS | MAC Status |
| 0x4A10 0168 | 0x4A12 0168 | EMCONTROL | Emulation Control |
| 0x4A10 016C | 0x4A12 016C | FIFOCONTROL | FIFO Control |
| 0x4A10 0170 | 0x4A12 0170 | MACCONFIG | MAC Configuration |
| 0x4A10 0174 | 0x4A12 0174 | SOFTRESET | Soft Reset |
| 0x4A10 01D0 | 0x4A12 01D0 | MACSRCADDRLO | MAC Source Address Low Bytes |
| 0x4A10 01D4 | 0x4A12 01D4 | MACSRCADDRHI | MAC Source Address High Bytes |
| 0x4A10 01D8 | 0x4A12 01D8 | MACHASH1 | MAC Hash Address 1 |
| 0x4A10 01DC | 0x4A12 01DC | MACHASH2 | MAC Hash Address 2 |


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**Table 9-37. EMAC Control Registers (continued)**

| EMAC0 HEX ADDRESS | EMAC1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4A10 01E0 | 0x4A12 01E0 | BOFFTEST | Back Off Test |
| 0x4A10 01E4 | 0x4A12 01E4 | TPACETEST | Transmit Pacing Algorithm Test |
| 0x4A10 01E8 | 0x4A12 01E8 | RXPAUSE | Receive Pause Timer |
| 0x4A10 01EC | 0x4A12 01EC | TXPAUSE | Transmit Pause Timer |
| 0x4A10 0200 - 0x4A10 02FC | 0x4A12 0200 - 0x4A12 02FC | (see Table 9-38) | EMAC Network Statistics Registers |
| 0x4A10 0500 | 0x4A12 0500 | MACADDRLO | MAC Address Low Bytes, Used in Receive Address Matching |
| 0x4A10 0504 | 0x4A12 0504 | MACADDRHI | MAC Address High Bytes, Used in Receive Address Matching |
| 0x4A10 0508 | 0x4A12 0508 | MACINDEX | MAC Index |
| 0x4A10 0600 | 0x4A12 0600 | TX0HDP | Transmit Channel 0 DMA Head Descriptor Pointer |
| 0x4A10 0604 | 0x4A12 0604 | TX1HDP | Transmit Channel 1 DMA Head Descriptor Pointer |
| 0x4A10 0608 | 0x4A12 0608 | TX2HDP | Transmit Channel 2 DMA Head Descriptor Pointer |
| 0x4A10 060C | 0x4A12 060C | TX3HDP | Transmit Channel 3 DMA Head Descriptor Pointer |
| 0x4A10 0610 | 0x4A12 0610 | TX4HDP | Transmit Channel 4 DMA Head Descriptor Pointer |
| 0x4A10 0614 | 0x4A12 0614 | TX5HDP | Transmit Channel 5 DMA Head Descriptor Pointer |
| 0x4A10 0618 | 0x4A12 0618 | TX6HDP | Transmit Channel 6 DMA Head Descriptor Pointer |
| 0x4A10 061C | 0x4A12 061C | TX7HDP | Transmit Channel 7 DMA Head Descriptor Pointer |
| 0x4A10 0620 | 0x4A12 0620 | RX0HDP | Receive Channel 0 DMA Head Descriptor Pointer |
| 0x4A10 0624 | 0x4A12 0624 | RX1HDP | Receive Channel 1 DMA Head Descriptor Pointer |
| 0x4A10 0628 | 0x4A12 0628 | RX2HDP | Receive Channel 2 DMA Head Descriptor Pointer |
| 0x4A10 062C | 0x4A12 062C | RX3HDP | Receive Channel 3 DMA Head Descriptor Pointer |
| 0x4A10 0630 | 0x4A12 0630 | RX4HDP | Receive Channel 4 DMA Head Descriptor Pointer |
| 0x4A10 0634 | 0x4A12 0634 | RX5HDP | Receive Channel 5 DMA Head Descriptor Pointer |
| 0x4A10 0638 | 0x4A12 0638 | RX6HDP | Receive Channel 6 DMA Head Descriptor Pointer |
| 0x4A10 063C | 0x4A12 063C | RX7HDP | Receive Channel 7 DMA Head Descriptor Pointer |
| 0x4A10 0640 | 0x4A12 0640 | TX0CP | Transmit Channel 0 Completion Pointer |
| 0x4A10 0644 | 0x4A12 0644 | TX1CP | Transmit Channel 1 Completion Pointer |
| 0x4A10 0648 | 0x4A12 0648 | TX2CP | Transmit Channel 2 Completion Pointer |
| 0x4A10 064C | 0x4A12 064C | TX3CP | Transmit Channel 3 Completion Pointer |
| 0x4A10 0650 | 0x4A12 0650 | TX4CP | Transmit Channel 4 Completion Pointer |
| 0x4A10 0654 | 0x4A12 0654 | TX5CP | Transmit Channel 5 Completion Pointer |

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**Table 9-37. EMAC Control Registers (continued)**

| EMAC0 HEX ADDRESS | EMAC1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4A10 0658 | 0x4A12 0658 | TX6CP | Transmit Channel 6 Completion Pointer |
| 0x4A10 065C | 0x4A12 065C | TX7CP | Transmit Channel 7 Completion Pointer |
| 0x4A10 0660 | 0x4A12 0660 | RX0CP | Receive Channel 0 Completion Pointer |
| 0x4A10 0664 | 0x4A12 0664 | RX1CP | Receive Channel 1 Completion Pointer |
| 0x4A10 0668 | 0x4A12 0668 | RX2CP | Receive Channel 2 Completion Pointer |
| 0x4A10 066C | 0x4A12 066C | RX3CP | Receive Channel 3 Completion Pointer |
| 0x4A10 0670 | 0x4A12 0670 | RX4CP | Receive Channel 4 Completion Pointer |
| 0x4A10 0674 | 0x4A12 0674 | RX5CP | Receive Channel 5 Completion Pointer |
| 0x4A10 0678 | 0x4A12 0678 | RX6CP | Receive Channel 6 Completion Pointer |
| 0x4A10 067C | 0x4A12 067C | RX7CP | Receive Channel 7 Completion Pointer |

**Table 9-38. EMAC Network Statistics Registers**

| EMAC0 HEX ADDRESS | EMAC1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4A10 0200 | 0x4A12 0200 | RXGOODFRAMES | Good Receive Frames |
| 0x4A10 0204 | 0x4A12 0204 | RXBCASTFRAMES | Broadcast Receive Frames |
| 0x4A10 0208 | 0x4A12 0208 | RXMCASTFRAMES | Multicast Receive Frames |
| 0x4A10 020C | 0x4A12 020C | RXPAUSEFRAMES | Pause Receive Frames |
| 0x4A10 0210 | 0x4A12 0210 | RXCRCERRORS | Receive CRC Errors |
| 0x4A10 0214 | 0x4A12 0214 | RXALIGNCODEERRORS | Receive Alignment Code Errors |
| 0x4A10 0218 | 0x4A12 0218 | RXOVERSIZED | Receive Oversized Frames |
| 0x4A10 021C | 0x4A12 021C | RXJABBER | Receive Jabber Frames |
| 0x4A10 0220 | 0x4A12 0220 | RXUNDERSIZED | Receive Undersized Frames |
| 0x4A10 0224 | 0x4A12 0224 | RXFRAGMENTS | Receive Frame Fragments |
| 0x4A10 0228 | 0x4A12 0228 | RXFILTERED | Filtered Receive Frames |
| 0x4A10 022C | 0x4A12 022C | RXQOSFILTERED | Receive QOS Filtered Frames |
| 0x4A10 0230 | 0x4A12 0230 | RXOCTETS | Receive Octet Frames |
| 0x4A10 0234 | 0x4A12 0234 | TXGOODFRAMES | Good Transmit Frames |
| 0x4A10 0238 | 0x4A12 0238 | TXBCASTFRAMES | Broadcast Transmit Frames |
| 0x4A10 023C | 0x4A12 023C | TXMCASTFRAMES | Multicast Transmit Frames |
| 0x4A10 0240 | 0x4A12 0240 | TXPAUSEFRAMES | Pause Transmit Frames |
| 0x4A10 0244 | 0x4A12 0244 | TXDEFERRED | Deferred Transmit Frames |
| 0x4A10 0248 | 0x4A12 0248 | TXCOLLISION | Transmit Collision Frames |
| 0x4A10 024C | 0x4A12 024C | TXSINGLECOLL | Transmit Single Collision Frames |
| 0x4A10 0250 | 0x4A12 0250 | TXMULTICOLL | Transmit Multiple Collision Frames |
| 0x4A10 0254 | 0x4A12 0254 | TXEXCESSIVECOLL | Transmit Excessive Collision Frames |
| 0x4A10 0258 | 0x4A12 0258 | TXLATECOLL | Transmit Late Collision Frames |
| 0x4A10 025C | 0x4A12 025C | TXUNDERRUN | Transmit Underrun Error |
| 0x4A10 0260 | 0x4A12 0260 | TXCARRIERSENSE | Transmit Carrier Sense Errors |
| 0x4A10 0264 | 0x4A12 0264 | TXOCTETS | Transmit Octet Frames |
| 0x4A10 0268 | 0x4A12 0268 | FRAME64 | Transmit and Receive 64 Octet Frames |
| 0x4A10 026C | 0x4A12 026C | FRAME65T127 | Transmit and Receive 65 to 127 Octet Frames |
| 0x4A10 0270 | 0x4A12 0270 | FRAME128T255 | Transmit and Receive 128 to 255 Octet Frames |
| 0x4A10 0274 | 0x4A12 0274 | FRAME256T511 | Transmit and Receive 256 to 511 Octet Frames |
| 0x4A10 0278 | 0x4A12 0278 | FRAME512T1023 | Transmit and Receive 512 to 1023 Octet Frames |
| 0x4A10 027C | 0x4A12 027C | FRAME1024TUP | Transmit and Receive 1024 to RXMAXLEN Octet Frames |


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**Table 9-38. EMAC Network Statistics Registers (continued)**

| EMAC0 HEX ADDRESS | EMAC1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4A10 0280 | 0x4A12 0280 | NETOCTETS | Network Octet Frames |
| 0x4A10 0284 | 0x4A12 0284 | RXSOFOVERRUNS | Receive FIFO or DMA Start of Frame Overruns |
| 0x4A10 0288 | 0x4A12 0288 | RXMOFOVERRUNS | Receive FIFO or DMA Middle of Frame Overruns |
| 0x4A10 028C | 0x4A12 028C | RXDMAOVERRUNS | Receive DMA Overruns |

**Table 9-39. EMAC Control Module Registers**

| EMAC0 HEX ADDRESS | EMAC1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4A10 0900 | 0x4A12 0900 | CMIDVER | Identification and Version |
| 0x4A10 0904 | 0x4A12 0904 | CMSOFTRESET | Software Reset |
| 0x4A10 0908 | 0x4A12 0908 | CMEMCONTROL | Emulation Control |
| 0x4A10 090C | 0x4A12 090C | CMINTCTRL | Interrupt Control |
| 0x4A10 0910 | 0x4A12 0910 | CMRXTHRESHINTEN | Receive Threshold Interrupt Enable |
| 0x4A10 0914 | 0x4A12 0914 | CMRXINTEN | Receive Interrupt Enable |
| 0x4A10 0918 | 0x4A12 0918 | CMTXINTEN | Transmit Interrupt Enable |
| 0x4A10 091C | 0x4A12 091C | CMMISCINTEN | Miscellaneous Interrupt Enable |
| 0x4A10 0940 | 0x4A12 0940 | CMRXTHRESHINTSTAT | Receive Threshold Interrupt Status |
| 0x4A10 0944 | 0x4A12 0944 | CMRXINTSTAT | Receive Interrupt Status |
| 0x4A10 0948 | 0x4A12 0948 | CMTXINTSTAT | Transmit Interrupt Status |
| 0x4A10 094C | 0x4A12 094C | CMMISCINTSTAT | Miscellaneous Interrupt Status |
| 0x4A10 0970 | 0x4A12 0970 | CMRXINTMAX | Receive Interrupts Per Millisecond |
| 0x4A10 0974 | 0x4A12 0974 | CMTXINTMAX | Transmit Interrupts Per Millisecond |

**Table 9-40. EMAC Descriptor Memory RAM**

| EMAC0 HEX ADDRESS | EMAC1 HEX ADDRESS | DESCRIPTION |
|---|---|---|
| 0x4A10 2000 - 0x4A10 3FFF | 0x4A12 2000 - 0x4A12 3FFF | EMAC Control Module Descriptor Memory |

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### 9.6.2 EMAC Electrical Data and Timing

**Table 9-41. Timing Requirements for EMAC[1:0]_RXCLK - [G]MII Operation**

(see Figure 9-43)

| NO. | | | 1000 Mbps (1 Gbps) (GMII Only) | | 100 Mbps | | 10 Mbps | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(RXCLK)}$ | Cycle time, EMAC[1:0]_RXCLK | 8 | | 40 | | 400 | | ns |
| 2 | $t_{w(RXCLKH)}$ | Pulse duration, EMAC1:0]_RXCLK high | 2.8 | | 14 | | 140 | | ns |
| 3 | $t_{w(RXCLKL)}$ | Pulse duration, EMAC[1:0]_RXCLK low | 2.8 | | 14 | | 140 | | ns |
| 4 | $t_{t(RXCLK)}$ | Transition time, EMAC[1:0]_RXCLK | | 1 | | 3 | | 3 | ns |

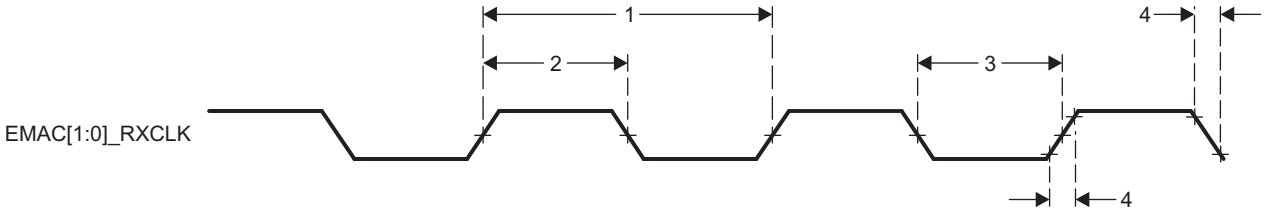


**Figure 9-43. EMAC[1:0]_RXCLK Timing**

**Table 9-42. Timing Requirements for EMAC[1:0]_TXCLK - [G]MII Operation**

(see Figure 9-44)

| NO. | | | 1000 Mbps (1 Gbps) (GMII Only) | | 100 Mbps | | 10 Mbps | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(TXCLK)}$ | Cycle time, EMAC[1:0]_TXCLK | 8 | | 40 | | 400 | | ns |
| 2 | $t_{w(TXCLKH)}$ | Pulse duration, EMAC[1:0]_TXCLK high | 2.8 | | 14 | | 140 | | ns |
| 3 | $t_{w(TXCLKL)}$ | Pulse duration, EMAC[1:0]_TXCLK low | 2.8 | | 14 | | 140 | | ns |
| 4 | $t_{t(TXCLK)}$ | Transition time, EMAC[1:0]_TXCLK | | 1 | | 3 | | 3 | ns |

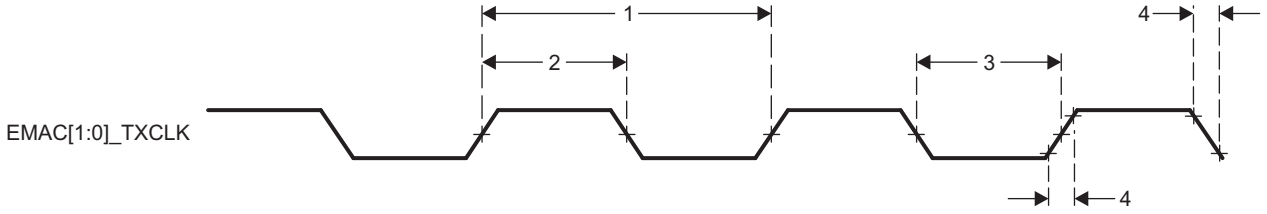


**Figure 9-44. EMAC[1:0]_TXCLK Timing**


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**Table 9-43. Timing Requirements for EMAC [G]MII Receive 10 Mbps,100 Mbps, and 1000 Mbps**

(see Figure 9-45)

| NO. | | | 1000 Mbps (1 Gbps) | | 100 Mbps and 10 Mbps | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(RXD-RXCLK)}$<br>$t_{su(RXDV-RXCLK)}$<br>$t_{su(RXER-RXCLK)}$ | Setup time, receive selected signals valid before EMAC[1:0]_RXCLK | 2 | | 8 | | ns |
| 2 | $t_{h(RXCLK-RXD)}$<br>$t_{h(RXCLK-RXDV)}$<br>$t_{h(RXCLK-RXER)}$ | Hold time, receive selected signals valid after EMAC[1:0]_RXCLK | 0 | | 8 | | ns |

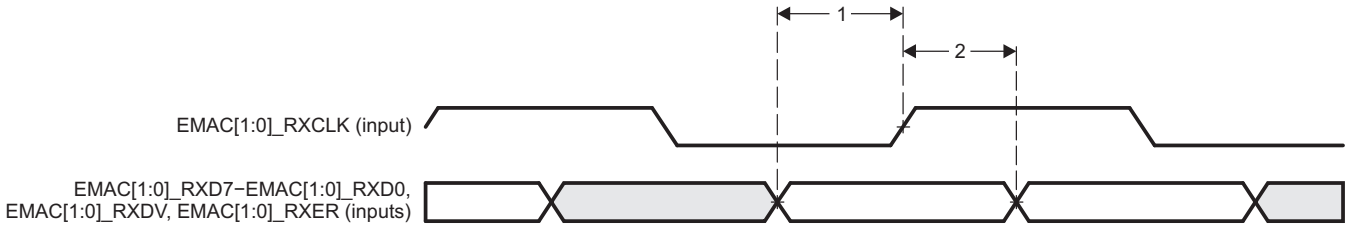


**Figure 9-45. EMAC Receive Timing**

**Table 9-44. Switching Characteristics Over Recommended Operating Conditions for EMAC [G]MII Transmit 10 Mbps and 100 Mbps**

(see Figure 9-46)

| NO. | PARAMETER | | 100 Mbps and 10 Mbps | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{d(TXCLK-TXD)}$<br>$t_{d(TXCLK-TXEN)}$ | Delay time, EMAC[1:0]_TXCLK to transmit selected signals valid | 5 | 25 | ns |

**Table 9-45. Switching Characteristics Over Recommended Operating Conditions for EMAC [G]MII Transmit 1000 Mbps**

(see Figure 9-46)

| NO. | PARAMETER | | 1000 Mbps (1 Gbps) | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{d(GMTCLK-TXD)}$<br>$t_{d(GMTCLK-TXEN)}$ | Delay time, EMAC[1:0]_GMTCLK to transmit selected signals valid | 0.5 | 5 | ns |

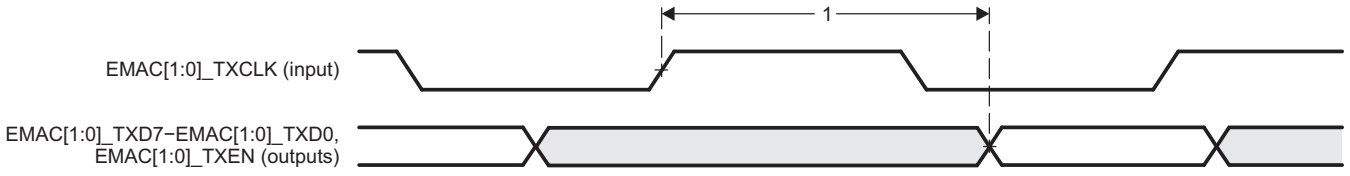


**Figure 9-46. EMAC Transmit Timing**

### 9.6.3 Management Data Input and Output (MDIO)

The Management Data Input and Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The MDIO module implements the 802.3 serial management interface to interrogate and control Ethernet PHYs using a shared two-wire bus. Host software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. A single MDIO interface is pinned out to control the PHY configuration and status monitoring. Multiple external PHYs can be controlled by the MDIO interface.

For more detailed information on the MDIO peripheral, see the EMAC and MDIO chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

#### 9.6.3.1 MDIO Peripheral Register Descriptions

**Table 9-46. MDIO Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 0800 | VERSION | MDIO Version |
| 0x4A10 0804 | CONTROL | MDIO Control |
| 0x4A10 0808 | ALIVE | PHY Alive Status |
| 0x4A10 080C | LINK | PHY Link Status |
| 0x4A10 0810 | LINKINTRAW | MDIO Link Status Change Interrupt (Unmasked) |
| 0x4A10 0814 | LINKINTMASKED | MDIO Link Status Change Interrupt (Masked) |
| 0x4A10 0818 | - | Reserved |
| 0x4A10 081C | USERINTRAW | MDIO User Command Complete Interrupt (Unmasked) |
| 0x4A10 0820 | USERINTMASKED | MDIO User Command Complete Interrupt (Masked) |
| 0x4A10 0824 | USERINTMASKSET | MDIO User Command Complete Interrupt Mask Set |
| 0x4A10 0828 | USERINTMASKCLEAR | MDIO User Command Complete Interrupt Mask Clear |
| 0x4A10 082C | - | Reserved |
| 0x4A10 0880 | USERACCESS0 | MDIO User Access 0 |
| 0x4A10 0884 | USERPHYSEL0 | MDIO User PHY Select 0 |
| 0x4A10 0888 | USERACCESS1 | MDIO User Access 1 |
| 0x4A10 088C | USERPHYSEL1 | MDIO User PHY Select 1 |

#### 9.6.3.2 MDIO Electrical Data and Timing

**Table 9-47. Timing Requirements for MDIO Input**

(see Figure 9-47)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(MCLK)}$ | Cycle time, MDIO_MCLK | 400 | | ns |
| | $t_{w(MCLK)}$ | Pulse duration, MDIO_MCLK high or low | 180 | | ns |
| 4 | $t_{su(MDIO-MCLKH)}$ | Setup time, MDIO_MDIO data input valid before MDIO_MCLK high | 20 | | ns |
| 5 | $t_{h(MCLKH-MDIO)}$ | Hold time, MDIO_MDIO data input valid after MDIO_MCLK high | 0 | | ns |


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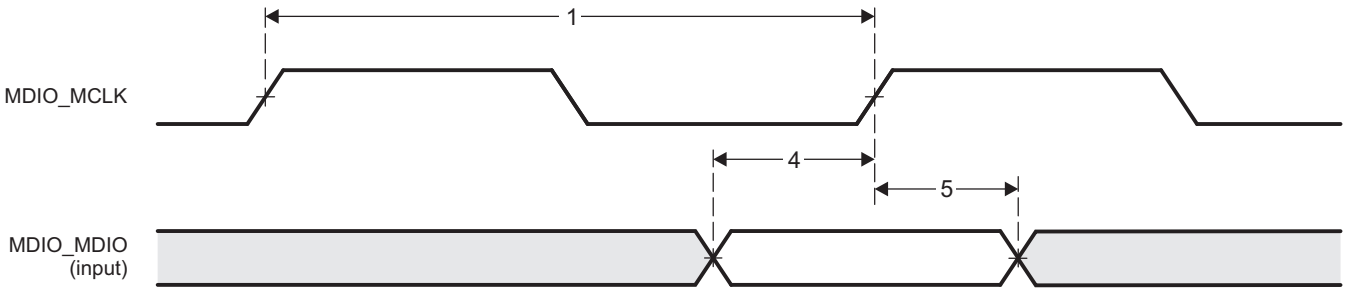


**Figure 9-47. MDIO Input Timing**

**Table 9-48. Switching Characteristics Over Recommended Operating Conditions for MDIO Output**

(see Figure 9-48)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 7 | $t_{d(MCLKL-MDIO)}$ | Delay time, MDIO_MCLK low to MDIO_MDIO data output valid | | 100 | ns |

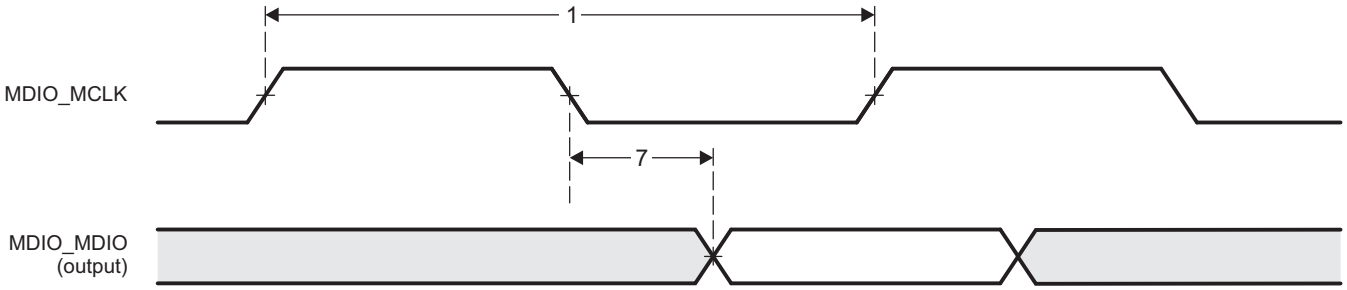


**Figure 9-48. MDIO Output Timing**

## 9.7 General-Purpose Input and Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register controls the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts in different interrupt generation modes. The GPIO peripheral provides generic connections to external devices.

The device contains two GPIO modules and each GPIO module is made up of 32 identical channels.

The device GPIO peripheral supports the following:

- Up to 64 3.3-V GPIO pins, GP0[31:0] and GP1[31:0] (the exact number available varies as a function of the device configuration). Each channel can be configured to be used in the following applications:
  - Data input and output
  - Keyboard interface with a de-bouncing cell
  - Synchronous interrupt generation (in active mode) upon the detection of external events (signal transitions or signal levels).
- Synchronous interrupt requests from each channel are processed by two identical interrupt generation sub-modules to be used independently by the ARM or DSP. Interrupts can be triggered by rising or falling edge, specified for each interrupt-capable GPIO signal.
- Shared registers can be accessed through "Set & Clear" protocol. Software writes 1 to corresponding bit positions to set or to clear GPIO signals. This allows multiple software processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to another process during GPIO programming).
- Separate input and output registers.
- Output register in addition to set or clear so that, if preferred by software, some GPIO output signals can be toggled by direct write to the output registers.
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain IO cell, allows wired logic to be implemented.

For more detailed information on GPIOs, see the GPIO chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### *9.7.1 GPIO Peripheral Register Descriptions*

**Table 9-49. GPIO Registers**

| GPIO0 HEX ADDRESS | GPIO1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4803 2000 | 0x4804 C000 | GPIO_REVISION | GPIO Revision |
| 0x4803 2010 | 0x4804 C010 | GPIO_SYSCONFIG | System Configuration |
| 0x4803 2020 | 0x4804 C020 | GPIO_EOI | End of Interrupt |
| 0x4803 2024 | 0x4804 C024 | GPIO_IRQSTATUS_RAW_0 | Status Raw for Interrupt 1 |
| 0x4803 2028 | 0x4804 C028 | GPIO_IRQSTATUS_RAW_1 | Status Raw for Interrupt 2 |
| 0x4803 202C | 0x4804 C02C | GPIO_IRQSTATUS_0 | Status for Interrupt 1 |
| 0x4803 2030 | 0x4804 C030 | GPIO_IRQSTATUS_1 | Status for Interrupt 2 |
| 0x4803 2034 | 0x4804 C034 | GPIO_IRQSTATUS_SET_0 | Enable Set for Interrupt 1 |
| 0x4803 2038 | 0x4804 C038 | GPIO_IRQSTATUS_SET_1 | Enable Set for Interrupt 2 |
| 0x4803 203C | 0x4804 C03C | GPIO_IRQSTATUS_CLR_0 | Enable Clear for Interrupt 1 |
| 0x4803 2040 | 0x4804 C040 | GPIO_IRQSTATUS_CLR_1 | Enable Clear for Interrupt 2 |
| 0x4803 2044 | 0x4804 C044 | GPIO_IRQWAKEN_0 | Wakeup Enable for Interrupt 1 |
| 0x4803 2048 | 0x4804 C048 | GPIO_IRQWAKEN_1 | Wakeup Enable for Interrupt 2 |
| 0x4803 2114 | 0x4804 C114 | GPIO_SYSSTATUS | System Status |
| 0x4803 2130 | 0x4804 C130 | GPIO_CTRL | Module Control |
| 0x4803 2134 | 0x4804 C134 | GPIO_OE | Output Enable |


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**Table 9-49. GPIO Registers (continued)**

| GPIO0 HEX ADDRESS | GPIO1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4803 2138 | 0x4804 C138 | GPIO_DATAIN | Data Input |
| 0x4803 213C | 0x4804 C13C | GPIO_DATAOUT | Data Output |
| 0x4803 2140 | 0x4804 C140 | GPIO_LEVELDETECT0 | Detect Low Level |
| 0x4803 2144 | 0x4804 C144 | GPIO_LEVELDETECT1 | Detect High Level |
| 0x4803 2148 | 0x4804 C148 | GPIO_RISINGDETECT | Detect Rising Edge |
| 0x4803 214C | 0x4804 C14C | GPIO_FALLINGDETECT | Detect Falling Edge |
| 0x4803 2150 | 0x4804 C150 | GPIO_DEBOUNCENABLE | Debouncing Enable |
| 0x4803 2154 | 0x4804 C154 | GPIO_DEBOUNCINGTIME | Debouncing Value |
| 0x4803 2190 | 0x4804 C190 | GPIO_CLEARDATAOUT | Clear Data Output |
| 0x4803 2194 | 0x4804 C194 | GPIO_SETDATAOUT | Set Data Output |

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### 9.7.2 GPIO Electrical Data and Timing

**Table 9-50. Timing Requirements for GPIO Inputs**

(see Figure 9-49)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(GPIH)}$ | Pulse duration, GP[x] input high | 12P(1) | | ns |
| 2 | $t_{w(GPIL)}$ | Pulse duration, GP[x] input low | 12P(1) | | ns |

(1) P = Module clock.

**Table 9-51. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs**

(see Figure 9-49)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 3 | $t_{w(GPOH)}$ | Pulse duration, GP[x] output high | 36P-8(1) | | ns |
| 4 | $t_{w(GPOL)}$ | Pulse duration, GP[x] output low | 36P-8(1) | | ns |

(1) P = Module clock.

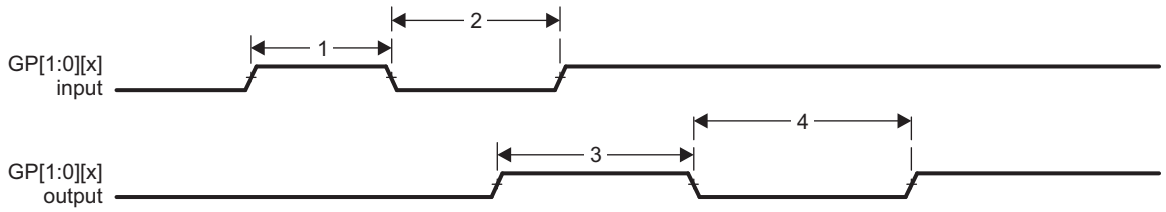


**Figure 9-49. GPIO Port Timing**


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## 9.8 General-Purpose Memory Controller (GPMC) and Error Locator Module (ELM)

The GPMC is a device memory controller used to provide a glueless interface to external memory devices such as NOR Flash, NAND Flash (with BCH and Hamming Error Code Detection for 8-bit or 16-bit NAND Flash), SRAM, and Pseudo-SRAM. It includes flexible asynchronous protocol control for interface to SRAM-like memories and custom logic (FPGA, CPLD, ASICs, and others).

The first section of GPMC memory (0x0 - 0x00FF_FFFF) is reserved for BOOTROM. Accessible memory starts at location 0x0100_0000.

Other supported features include:

- 8-bit and 6-bit wide multiplexed address and data bus
- Up to 6 chip selects with up to 256M-byte address space per chip select pin
- Non-multiplexed address and data mode
- Pre-fetch and write posting engine associated with system DMA to get full performance from NAND device with minimum impact on NOR and SRAM concurrent access.

The device also contains an Error Locator Module (ELM) which is used to extract error addresses from syndrome polynomials generated using a BCH algorithm. Each of these polynomials gives a status of the read operations for a 512 bytes block from a NAND flash and its associated BCH parity bits, plus optionally spare area information. The ELM has the following features:

- 4-bit, 8-bit, and 16-bit per 512-byte block error location based on BCH algorithms
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation on error location process completion
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode.

For more detailed information on the GPMC, see the GPMC chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### 9.8.1 GPMC and ELM Peripheral Register Descriptions

**Table 9-52. GPMC Registers(1)(2)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5000 0000 | GPMC_REVISION | GPIO Revision |
| 0x5000 0010 | GPMC_SYSCONFIG | System Configuration |
| 0x5000 0014 | GPMC_SYSSTATUS | System Status |
| 0x5000 0018 | GPMC_IRQSTATUS | Status for Interrupt |
| 0x5000 001C | GPMC_IRQENABLE | Interrupt Enable |
| 0x5000 0040 | GPMC_TIMEOUT_CONTROL | Timeout Counter Start Value |
| 0x5000 0044 | GPMC_ERR_ADDRESS | Error Address |
| 0x5000 0048 | GPMC_ERR_TYPE | Error Type |
| 0x5000 0050 | GPMC_CONFIG | GPMC Global Configuration |
| 0x5000 0054 | GPMC_STATUS | GPMC Global Status |
| 0x5000 0060 + (0x0000 0030 * i) | GPMC_CONFIG1_0 - GPMC_CONFIG1_5 | Parameter Configuration 1_0-5 |
| 0x5000 0064 + (0x0000 0030 * i) | GPMC_CONFIG2_0 - GPMC_CONFIG2_5 | Parameter Configuration 2_0-5 |
| 0x5000 0068 + (0x0000 0030 * i) | GPMC_CONFIG3_0 - GPMC_CONFIG3_5 | Parameter Configuration 3_0-5 |
| 0x5000 006C + (0x0000 0030 * i) | GPMC_CONFIG4_0 - GPMC_CONFIG4_5 | Parameter Configuration 4_0-5 |

(1) i = 0 to 5.
(2) j = 0 to 8.

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**Table 9-52. GPMC Registers[1][2] (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5000 0070 + (0x0000 0030 * i) | GPMC_CONFIG5_0 - GPMC_CONFIG5_5 | Parameter Configuration 5_0-5 |
| 0x5000 0074 + (0x0000 0030 * i) | GPMC_CONFIG6_0 - GPMC_CONFIG6_5 | Parameter Configuration 6_0-5 |
| 0x5000 0078 + (0x0000 0030 * i) | GPMC_CONFIG7_0 - GPMC_CONFIG7_5 | Parameter Configuration 7_0-5 |
| 0x5000 007C + (0x0000 0030 * i) | GPMC_NAND_COMMAND_0 - GPMC_NAND_COMMAND_5 | NAND Command 0-5 |
| 0x5000 0080 + (0x0000 0030 * i) | GPMC_NAND_ADDRESS_0 - GPMC_NAND_ADDRESS_5 | NAND Address 0-5 |
| 0x5000 0084 + (0x0000 0030 * i) | GPMC_NAND_DATA_0 - GPMC_NAND_DATA_5 | NAND Data 0-5 |
| 0x5000 01E0 | GPMC_PREFETCH_CONFIG1 | Prefetch Configuration 1 |
| 0x5000 01E4 | GPMC_PREFETCH_CONFIG2 | Prefetch Configuration 2 |
| 0x5000 01EC | GPMC_PREFETCH_CONTROL | Prefetch Control |
| 0x5000 01F0 | GPMC_PREFETCH_STATUS | Prefetch Status |
| 0x5000 01F4 | GPMC_ECC_CONFIG | ECC Configuration |
| 0x5000 01F8 | GPMC_ECC_CONTROL | ECC Control |
| 0x5000 01FC | GPMC_ECC_SIZE_CONFIG | ECC Size Configuration |
| 0x5000 0200 + (0x0000 0004 * j) | GPMC_ECC0_RESULT - GPMC_ECC8_RESULT | ECC0-8 Result |
| 0x5000 0240 + (0x0000 0010 * i) | GPMC_BCH_RESULT0_0 - GPMC_BCH_RESULT0_5 | BCH Result 0_0-5 |
| 0x5000 0244 + (0x0000 0010 * i) | GPMC_BCH_RESULT1_0 - GPMC_BCH_RESULT1_5 | BCH Result 1_0-5 |
| 0x5000 0248 + (0x0000 0010 * i) | GPMC_BCH_RESULT2_0 - GPMC_BCH_RESULT2_5 | BCH Result 2_0-5 |
| 0x5000 024C + (0x0000 0010 * i) | GPMC_BCH_RESULT3_0 - GPMC_BCH_RESULT3_5 | BCH Result 3_0-5 |
| 0x5000 0300 + (0x0000 0010 * i) | GPMC_BCH_RESULT4_0 - GPMC_BCH_RESULT4_5 | BCH Result 4_0-5 |
| 0x5000 0304 + (0x0000 0010 * i) | GPMC_BCH_RESULT5_0 - GPMC_BCH_RESULT5_5 | BCH Result 5_0-5 |
| 0x5000 0308 + (0x0000 0010 * i) | GPMC_BCH_RESULT6_0 - GPMC_BCH_RESULT6_5 | BCH Result 6_0-5 |
| 0x5000 02D0 | GPMC_BCH_SWDATA | BCH Data |

**Table 9-53. ELM Registers[1]**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4808 0000 | ELM_REVISION | Revision |
| 0x4808 0010 | ELM_SYSCONFIG | Configuration |
| 0x4808 0014 | ELM_SYSSTATUS | Status |
| 0x4808 0018 | ELM_IRQSTATUS | Interrupt status |
| 0x4808 001C | ELM_IRQENABLE | Interrupt enable |
| 0x4808 0020 | ELM_LOCATION_CONFIG | ECC algorithm parameters |
| 0x4808 0080 | ELM_PAGE_CTRL | Page definition |
| 0x4808 0400 + (0x40 * i) | ELM_SYNDROME_FRAGMENT_0_i | Input syndrome polynomial bits 0 to 31 |
| 0x4808 0404 + (0x40 * i) | ELM_SYNDROME_FRAGMENT_1_i | Input syndrome polynomial bits 32 to 63 |
| 0x4808 0408 + (0x40 * i) | ELM_SYNDROME_FRAGMENT_2_i | Input syndrome polynomial bits 64 to 95 |
| 0x4808 040C + (0x40 * i) | ELM_SYNDROME_FRAGMENT_3_i | Input syndrome polynomial bits 96 to 127 |
| 0x4808 0410 + (0x40 * i) | ELM_SYNDROME_FRAGMENT_4_i | Input syndrome polynomial bits 128 to 159 |

(1) i = 0 to 7.


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**Table 9-53. ELM Registers[1] (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4808 0414 + (0x40 * i) | ELM_SYNDROME_FRAGMENT_5_i | Input syndrome polynomial bits 160 to 191 |
| 0x4808 0418 + (0x40 * i) | ELM_SYNDROME_FRAGMENT_6_i | Input syndrome polynomial bits 192 to 207 |
| 0x4808 0800 + (0x100 * i) | ELM_LOCATION_STATUS_i | Exit status |
| 0x4808 0880 + (0x100 * i) | ELM_ERROR_LOCATION_0_i | Error location |
| 0x4808 0884 + (0x100 * i) | ELM_ERROR_LOCATION_1_i | Error location |
| 0x4808 0888 + (0x100 * i) | ELM_ERROR_LOCATION_2_i | Error location |
| 0x4808 088C + (0x100 * i) | ELM_ERROR_LOCATION_3_i | Error location |
| 0x4808 0890 + (0x100 * i) | ELM_ERROR_LOCATION_4_i | Error location |
| 0x4808 0894 + (0x100 * i) | ELM_ERROR_LOCATION_5_i | Error location |
| 0x4808 0898 + (0x100 * i) | ELM_ERROR_LOCATION_6_i | Error location |
| 0x4808 089C + (0x100 * i) | ELM_ERROR_LOCATION_7_i | Error location |
| 0x4808 08A0 + (0x100 * i) | ELM_ERROR_LOCATION_8_i | Error location |
| 0x4808 08A4 + (0x100 * i) | ELM_ERROR_LOCATION_9_i | Error location |
| 0x4808 08A8 + (0x100 * i) | ELM_ERROR_LOCATION_10_i | Error location |
| 0x4808 08AC + (0x100 * i) | ELM_ERROR_LOCATION_11_i | Error location |
| 0x4808 08B0 + (0x100 * i) | ELM_ERROR_LOCATION_12_i | Error location |
| 0x4808 08B4 + (0x100 * i) | ELM_ERROR_LOCATION_13_i | Error location |
| 0x4808 08B8 + (0x100 * i) | ELM_ERROR_LOCATION_14_i | Error location |
| 0x4808 08BC + (0x100 * i) | ELM_ERROR_LOCATION_15_i | Error location |

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## 9.8.2 GPMC Electrical Data and Timing

### 9.8.2.1 GPMC and NOR Flash Interface Synchronous Mode Timing

**Table 9-54. Timing Requirements for GPMC and NOR Flash Interface - Synchronous Mode**

(see Figure 9-50, Figure 9-51, Figure 9-52, Figure 9-53, Figure 9-54, Figure 9-55)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 13 | $t_{su(DV-CLKH)}$ | Setup time, read GPMC_D[15:0] valid before GPMC_CLK high | 3.2 | | ns |
| 14 | $t_{h(CLKH-DV)}$ | Hold time, read GPMC_D[15:0] valid after GPMC_CLK high | 2.5 | | ns |
| 22 | $t_{su(WAITV-CLKH)}$ | Setup time, GPMC_WAIT valid before GPMC_CLK high | 3.2 | | ns |
| 23 | $t_{h(CLKH-WAITV)}$ | Hold time, GPMC_WAIT valid after GPMC_CLK high | 2.5 | | ns |

**Table 9-55. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Synchronous Mode**

(see Figure 9-50, Figure 9-51, Figure 9-52, Figure 9-53, Figure 9-54, Figure 9-55)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLK)}$ | Cycle time, output clock GPMC_CLK period | 16(1) | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse duration, output clock GPMC_CLK high | 0.5P(2) | | ns |
| | $t_{w(CLKL)}$ | Pulse duration, output clock GPMC_CLK low | 0.5P(2) | | |
| 3 | $t_{d(CLKH-nCSV)}$ | Delay time, GPMC_CLK rising edge to $\overline{\text{GPMC_CS[x]}}$ transition | F - 2.2(3) | F + 4.5(3) | ns |
| 4 | $t_{d(CLKH-nCSIV)}$ | Delay time, GPMC_CLK rising edge to $\overline{\text{GPMC_CS[x]}}$ invalid | E - 2.2(4) | E + 4.5(4) | ns |
| 5 | $t_{d(ADDV-CLK)}$ | Delay time, GPMC_A[27:0] address bus valid to GPMC_CLK first edge | B - 4.5(5) | B + 2.3(5) | ns |
| 6 | $t_{d(CLKH-ADDIV)}$ | Delay time, GPMC_CLK rising edge to GPMC_A[27:0] GPMC address bus invalid | -2.3 | | ns |
| 7 | $t_{d(nBEV-CLK)}$ | Delay time, GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC_BE1}}$ valid to GPMC_CLK first edge | B - 1.9(5) | B + 2.3(5) | ns |
| 8 | $t_{d(CLKH-nBEIV)}$ | Delay time, GPMC_CLK rising edge to GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC_BE1}}$ invalid | D - 2.3(6) | D + 1.9(6) | ns |

(1) Sync mode = 62.5 MHz; Async mode = 125 MHz.
(2) P = GPMC_CLK period.
(3) For nCS falling edge (CS activated):
- For GpmcFCLKDivider = 0:
  F = 0.5 * CSExtraDelay * GPMC_FCLK
- For GpmcFCLKDivider = 1:
  F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK otherwise
- For GpmcFCLKDivider = 2:
  F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(4) For single read: E = (CSRdOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: E = (CSRdOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: E = (CSWrOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(5) B = ClkActivationTime * GPMC_FCLK
(6) For single read: D = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: D = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: D = (WrCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK


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**Table 9-55. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Synchronous Mode (continued)**

(see Figure 9-50, Figure 9-51, Figure 9-52, Figure 9-53, Figure 9-54, Figure 9-55)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 9 | $t_{d(CLKH-nADV)}$ | Delay time, GPMC_CLK rising edge to GPMC_$\overline{ADV}$_ALE transition | G - 2.3(7) | G + 4.5(7) | ns |
| 10 | $t_{d(CLKH-nADVIV)}$ | Delay time, GPMC_CLK rising edge to GPMC_$\overline{ADV}$_ALE invalid | D - 2.3(6) | D + 4.5(6) | ns |
| 11 | $t_{d(CLKH-nOE)}$ | Delay time, GPMC_CLK rising edge to $\overline{GPMC_OE_RE}$ transition | H - 2.3(8) | H + 3.5(8) | ns |
| 12 | $t_{d(CLKH-nOEIV)}$ | Delay time, GPMC_CLK rising edge to $\overline{GPMC_OE_RE}$ invalid | E - 2.3(4) | E + 3.5(4) | ns |

(7) For ADV falling edge (ADV activated):
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) or IO DIR rising edge (IN direction) :
- Case GpmcFCLKDivider = 0:
  H = 0.5 * OEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):
- Case GpmcFCLKDivider = 0:
  H = 0.5 * OEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

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**Table 9-55. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Synchronous Mode (continued)**

(see Figure 9-50, Figure 9-51, Figure 9-52, Figure 9-53, Figure 9-54, Figure 9-55)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 15 | $t_{d(CLKH-nWE)}$ | Delay time, GPMC_CLK rising edge to $\overline{\text{GPMC_WE}}$ transition | I - 2.3(9) | I + 4.5(9) | ns |
| 16 | $t_{d(CLKH-Data)}$ | Delay time, GPMC_CLK rising edge to GPMC_D[15:0] data bus transition | J - 2.3(10) | J + 1.9(10) | ns |
| 18 | $t_{d(CLKH-nBE)}$ | Delay time, GPMC_CLK rising edge to GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC_BE1}}$ transition | J - 2.3(10) | J + 1.9(10) | ns |
| 19 | $t_{w(nCSV)}$ | Pulse duration, $\overline{\text{GPMC_CS[x]}}$ low | A(11) | | ns |
| 20 | $t_{w(nBEV)}$ | Pulse duration, GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC_BE1}}$ low | C(12) | | ns |
| 21 | $t_{w(nADVV)}$ | Pulse duration, GPMC_$\overline{\text{ADV}}$_ALE low | K(13) | | ns |
| 24 | $t_{d(CLKH-DIR)}$ | Delay time, GPMC_CLK rising edge to GPMC_DIR high (IN direction) | H - 2.3(8) | H + 4.5(8) | ns |
| 25 | $t_{d(CLKH-DIRIV)}$ | Delay time, GPCM_CLK rising edge to GPMC_DIR low (OUT direction) | M - 2.3(14) | M + 4.5(14) | ns |

(9) For WE falling edge (WE activated):
- Case GpmcFCLKDivider = 0:
  I = 0.5 * WEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):
- Case GpmcFCLKDivider = 0:
  I = 0.5 * WEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10) J = GPMC_FCLK period.

(11) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period [n = page burst access number]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period [n = page burst access number]

(12) For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: C = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK [n = page burst access number]
For Burst write: C = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK [n = page burst access number]

(13) For read: K = (ADVRdOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For write: K = (ADVWrOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(14) M = ( RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK.
Parameter M expression is given as one example of GPMC programming. The IO DIR signal goes from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of the IO direction signal depends on the kind of successive read and write accesses performed to the memory and multiplexed or non-multiplexed memory addressing scheme, whether the bus keeping feature is enabled or not. The IO DIR behavior is automatically handled by the GPMC controller.


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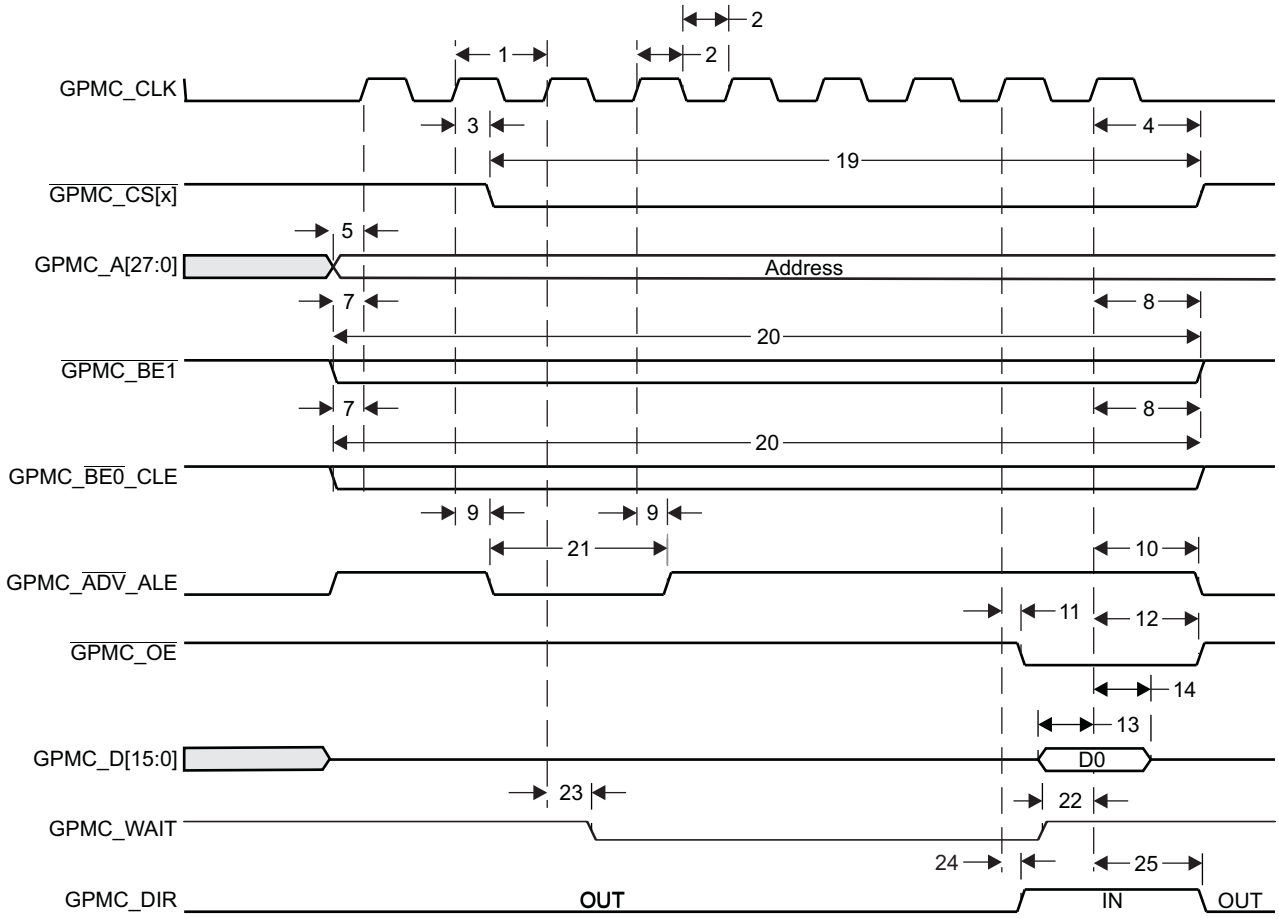


**Figure 9-50. GPMC Non-Multiplexed NOR Flash - Synchronous Single Read (GPMCFCLKDIVIDER = 0)**

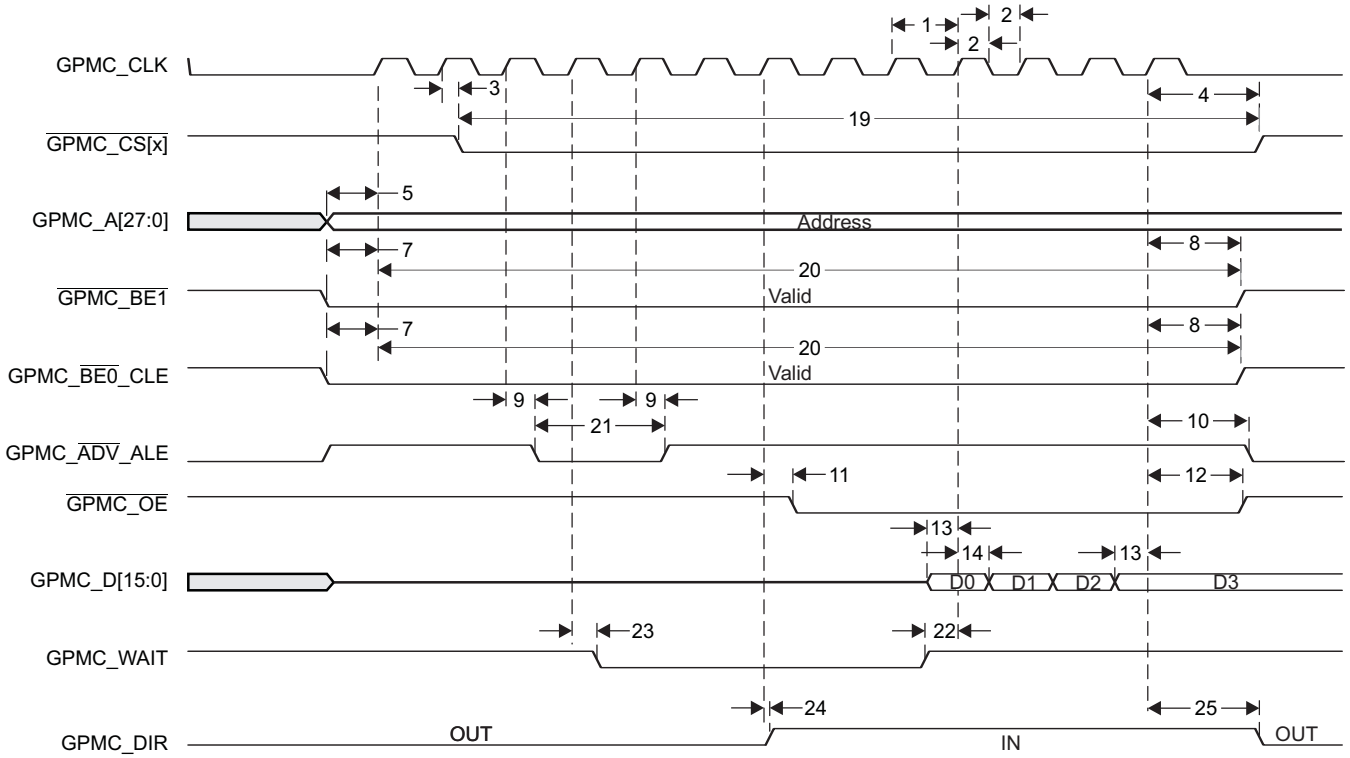


**Figure 9-51. GPMC Non-Multiplexed NOR Flash - 4x16-bit Synchronous Burst Read (GPMCFCLKDIVIDER = 0)**

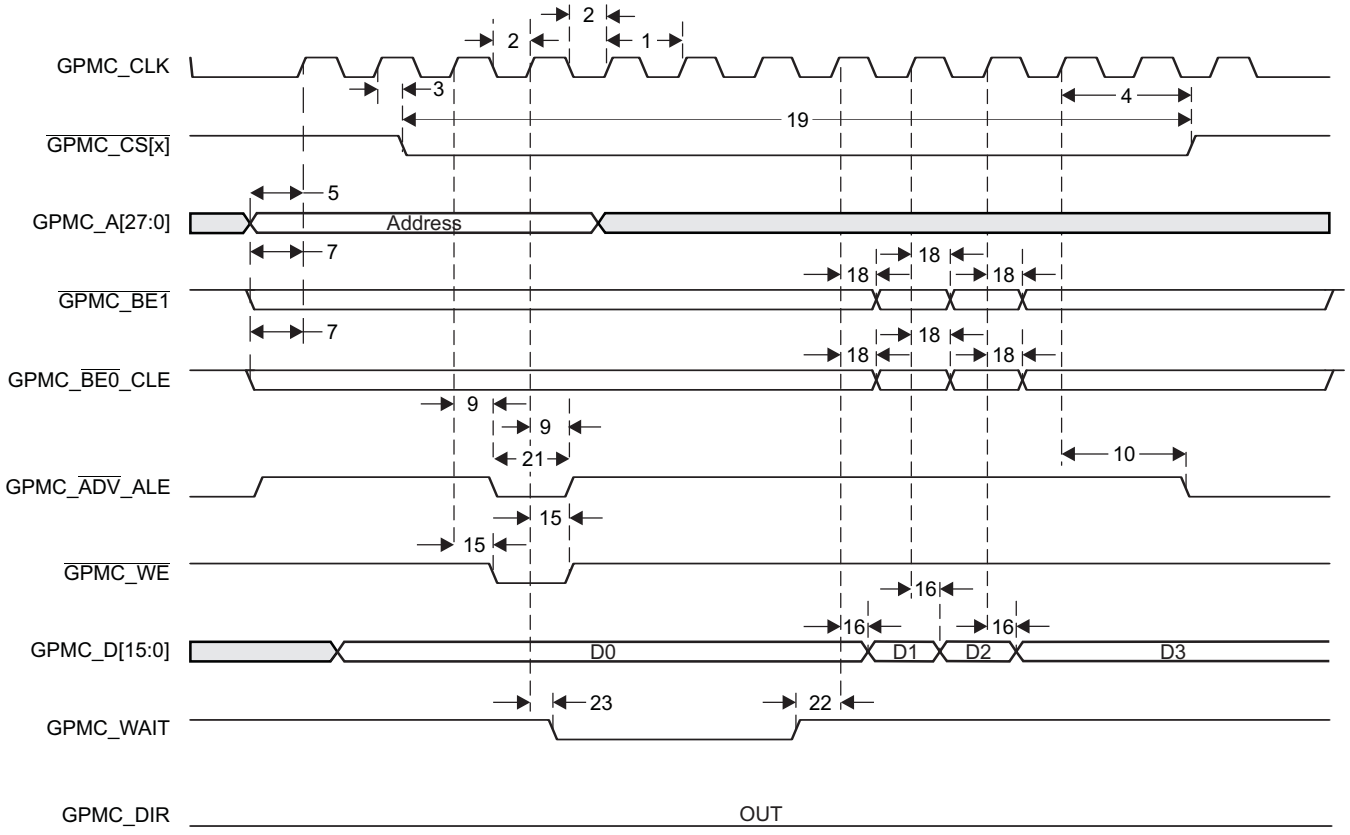


**Figure 9-52. GPMC Non-Multiplexed NOR Flash - Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**


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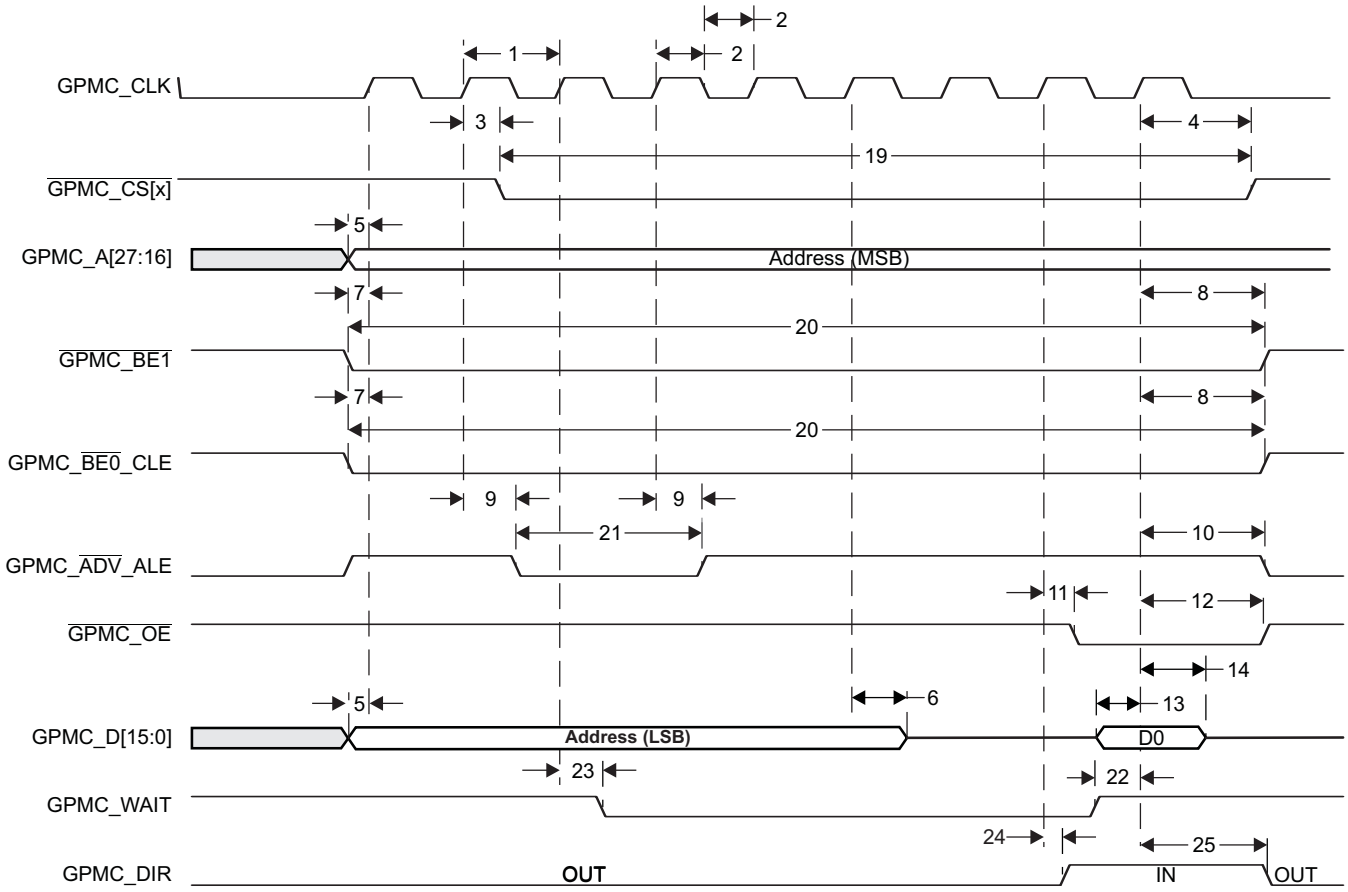


**Figure 9-53. GPMC Multiplexed NOR Flash - Synchronous Single Read (GPMCFCLKDIVIDER = 0)**

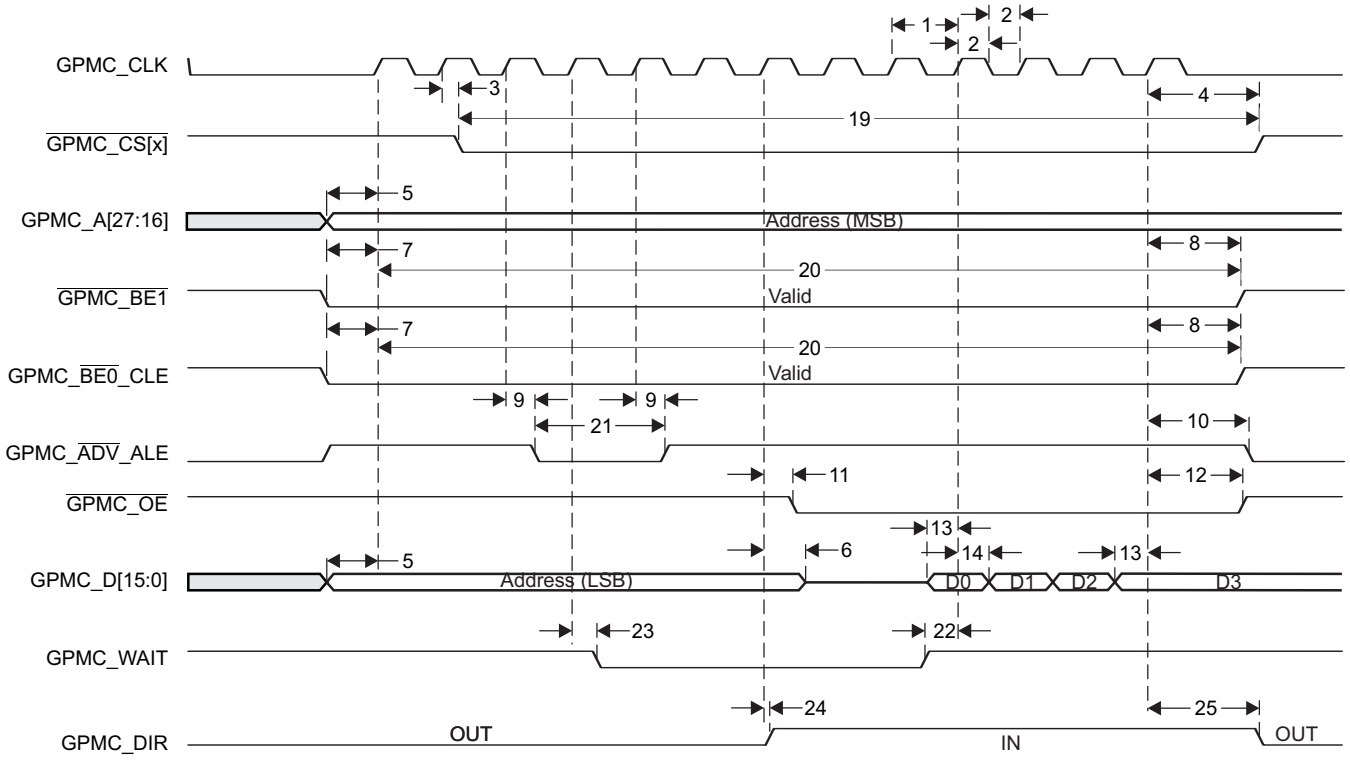


**Figure 9-54. GPMC Multiplexed NOR Flash - 4x16-bit Synchronous Burst Read (GPMCFCLKDIVIDER = 0)**

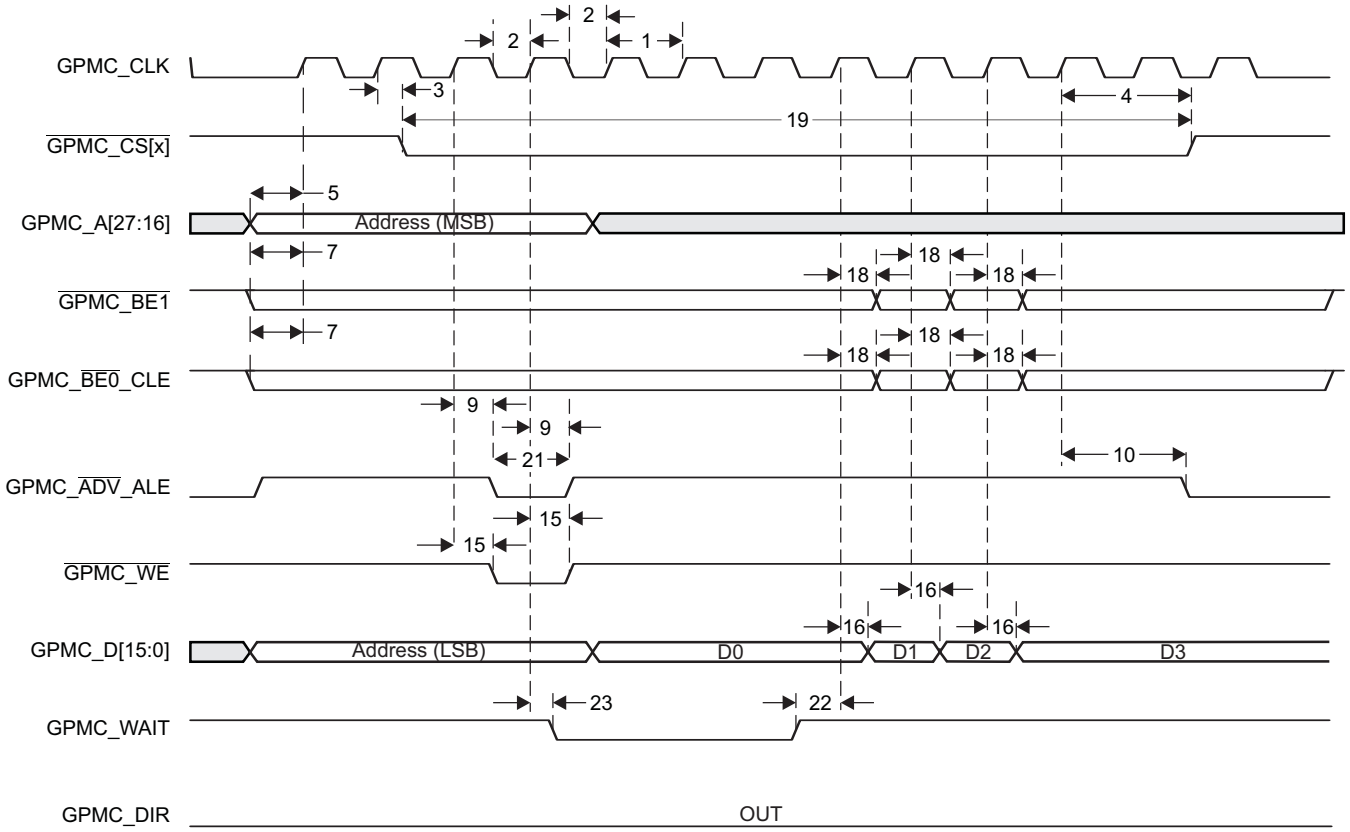


**Figure 9-55. GPMC Multiplexed NOR Flash - Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**


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### 9.8.2.2 GPMC and NOR Flash Interface Asynchronous Mode Timing

**Table 9-56. GPMC and NOR Flash Interface Asynchronous Mode Timing - Internal Parameters**

| NO. | | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | Max. output data generation delay from internal functional clock | | 6.5 | ns |
| 2 | Max. input data capture delay by internal functional clock | | 4 | ns |
| 3 | Max. chip select generation delay from internal functional clock | | 6.5 | ns |
| 4 | Max. address generation delay from internal functional clock | | 6.5 | ns |
| 5 | Max. address valid generation delay from internal functional clock | | 6.5 | ns |
| 6 | Max. byte enable generation delay from internal functional clock | | 6.5 | ns |
| 7 | Max. output enable generation delay from internal functional clock | | 6.5 | ns |
| 8 | Max. write enable generation delay from internal functional clock | | 6.5 | ns |
| 9 | Max. functional clock skew | | 100 | ps |

**Table 9-57. Timing Requirements for GPMC and NOR Flash Interface - Asynchronous Mode**

(see Figure 9-56, Figure 9-57, Figure 9-58, Figure 9-60)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 6 | $t_{acc(DAT)}$ | Data maximum access time (GPMC_FCLK cycles) | | H (1) | cycles |
| 21 | $t_{acc1-pgmode(DAT)}$ | Page mode successive data maximum access time (GPMC_FCLK cycles) | | P (2) | cycles |
| 22 | $t_{acc2-pgmode(DAT)}$ | Page mode first data maximum access time (GPMC_FCLK cycles) | | H (1) | cycles |

(1) H = AccessTime * (TimeParaGranularity + 1)
(2) P = PageBurstAccessTime * (TimeParaGranularity + 1).

**Table 9-58. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Asynchronous Mode**

(see Figure 9-56, Figure 9-57, Figure 9-58, Figure 9-59, Figure 9-60, Figure 9-61)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(nBEV)}$ | Pulse duration, GPMC_$\overline{BE0}$_CLE, $\overline{GPMC_BE1}$ valid time | | N (1) | ns |
| 2 | $t_{w(nCSV)}$ | Pulse duration, $\overline{GPMC_CS[x]}$ low | | A (2) | ns |
| 4 | $t_{d(nCSV-nADVIV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to GPMC_NADV_ALE invalid | B - 0.2 (3) | B + 2.0 (3) | ns |
| 5 | $t_{d(nCSV-nOEIV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to $\overline{GPMC_OE_RE}$ invalid (single read) | C - 0.2 (4) | C + 2.0 (4) | ns |
| 10 | $t_{d(AV-nCSV)}$ | Delay time, address bus valid to $\overline{GPMC_CS[x]}$ valid | J - 0.2 (5) | J + 2.0 (5) | ns |
| 11 | $t_{d(nBEV-nCSV)}$ | Delay time, GPMC_$\overline{BE0}$_CLE, $\overline{GPMC_BE1}$ valid to $\overline{GPMC_CS[x]}$ valid | J - 0.2 (5) | J + 2.0 (5) | ns |
| 13 | $t_{d(nCSV-nADVV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to GPMC_$\overline{ADV}$_ALE valid | K - 0.2 (6) | K + 2.0 (6) | ns |
| 14 | $t_{d(nCSV-nOEV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to $\overline{GPMC_OE_RE}$ valid | L - 0.2 (7) | L + 2.0 (7) | ns |

(1) For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(3) = B - nCS Max Delay + nADV Min Delay
For reading: B = ((ADVRdOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
(4) = C - nCS Max Delay + nOE Min Delay
C = ((OEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(5) = J - Address Max Delay + nCS Min Delay
J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK
(6) = K - nCS Max Delay + nADV Min Delay
K = ((ADVOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
(7) = L - nCS Max Delay + nOE Min Delay
L = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK

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**Table 9-58. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Asynchronous Mode (continued)**

(see Figure 9-56, Figure 9-57, Figure 9-58, Figure 9-59, Figure 9-60, Figure 9-61)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 15 | $t_{d(nCSV-DIR)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to GPMC_DIR high | L - 0.2(7) | L + 2.0(7) | ns |
| 16 | $t_{d(nCSV-DIR)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to GPMC_DIR low | M - 0.2(8) | M + 2.0(8) | ns |
| 17 | $t_{w(AIV)}$ | Address invalid duration between 2 successive read or write accesses | G(9) | | ns |
| 19 | $t_{d(nCSV-nOEIV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to $\overline{GPMC_OE_RE}$ invalid (burst read) | I - 0.2(10) | I + 2.0(10) | ns |
| 21 | $t_{w(AV)}$ | Pulse duration, address valid: second, third and fourth accesses | D(11) | | ns |
| 26 | $t_{d(nCSV-nWEV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to $\overline{GPMC_WE}$ valid | E - 0.2(12) | E + 2.0(12) | ns |
| 28 | $t_{d(nCSV-nWEIV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to $\overline{GPMC_WE}$ invalid | F - 0.2(13) | F + 2.0(13) | ns |
| 29 | $t_{d(nWEV-DV)}$ | Delay time, $\overline{GPMC_WE}$ valid to data bus valid | | 2.0 | ns |
| 30 | $t_{d(DV-nCSV)}$ | Delay time, data bus valid to $\overline{GPMC_CS[x]}$ valid | J - 0.2(5) | J + 2.0(5) | ns |
| 38 | $t_{d(nOEV-AIV)}$ | Delay time, $\overline{GPMC_OE_RE}$ valid to GPMC_A[16:1]_D[15:0] address phase end | | 2.0 | ns |

(8) = M - nCS Max Delay + nOE Min Delay
M = ((RdCycleTime - CSOnTime) * (TimeParaGranularity + 1) - 0.5 * CSExtraDelay) * GPMC_FCLK.
Parameter M expression is given as one example of GPMC programming. The IO DIR signal goes from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of the IO direction signal depends on the kind of successive read and write accesses performed to the memory and multiplexed or non-multiplexed memory addressing scheme, whether the bus keeping feature is enabled or not. The IO DIR behavior is automatically handled by the GPMC controller.
(9) G = Cycle2CycleDelay * GPMC_FCLK
(10) = I - nCS Max Delay + nOE Min Delay
I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(11) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK
(12) = E - nCS Max Delay + nWE Min Delay
E = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(13) = F - nCS Max Delay + nWE Min Delay
F = ((WEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK


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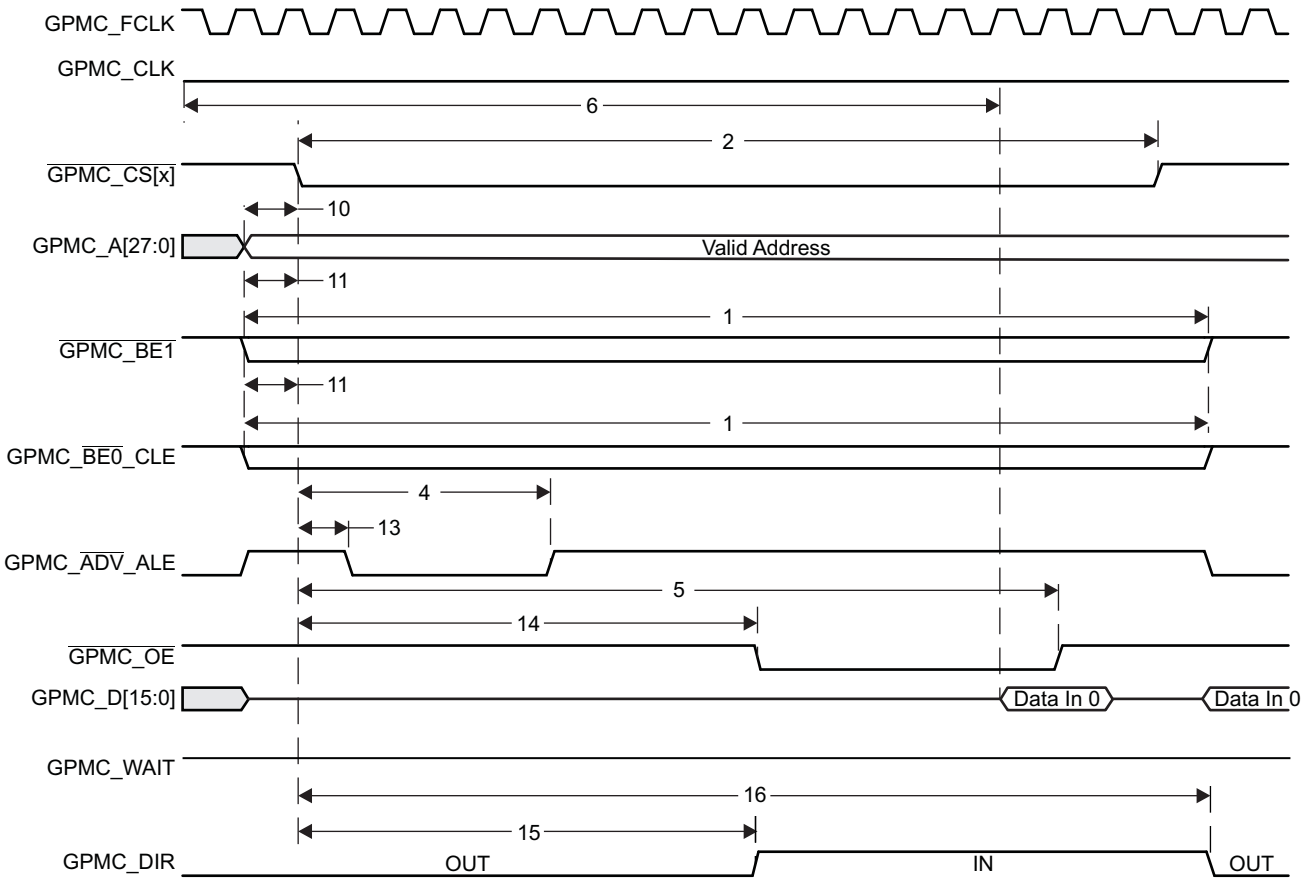


**Figure 9-56. GPMC Non-Multiplexed NOR Flash - Asynchronous Read - Single Word Timing**

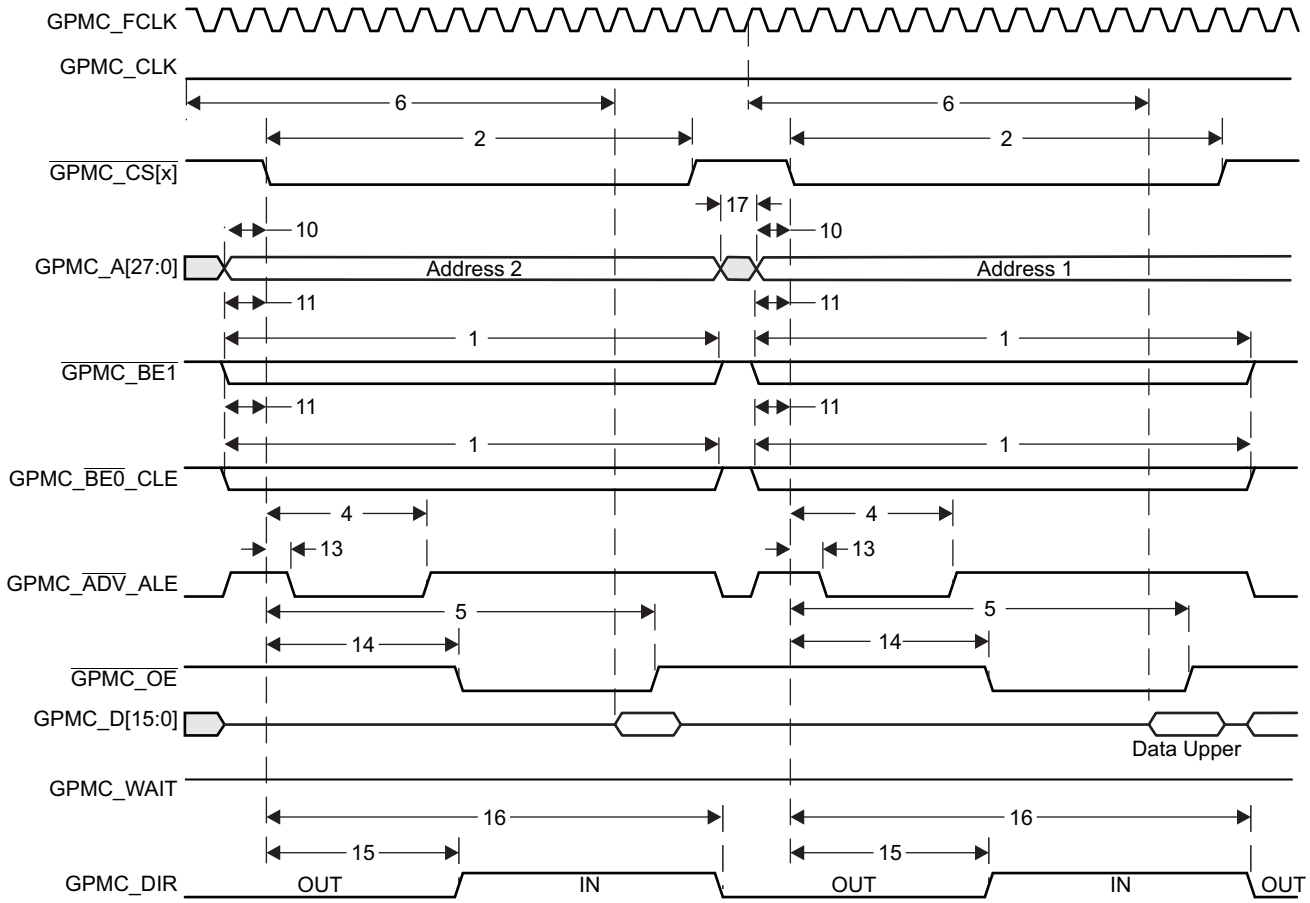


**Figure 9-57. GPMC Non-Multiplexed NOR Flash - Asynchronous Read - 32-Bit Timing**


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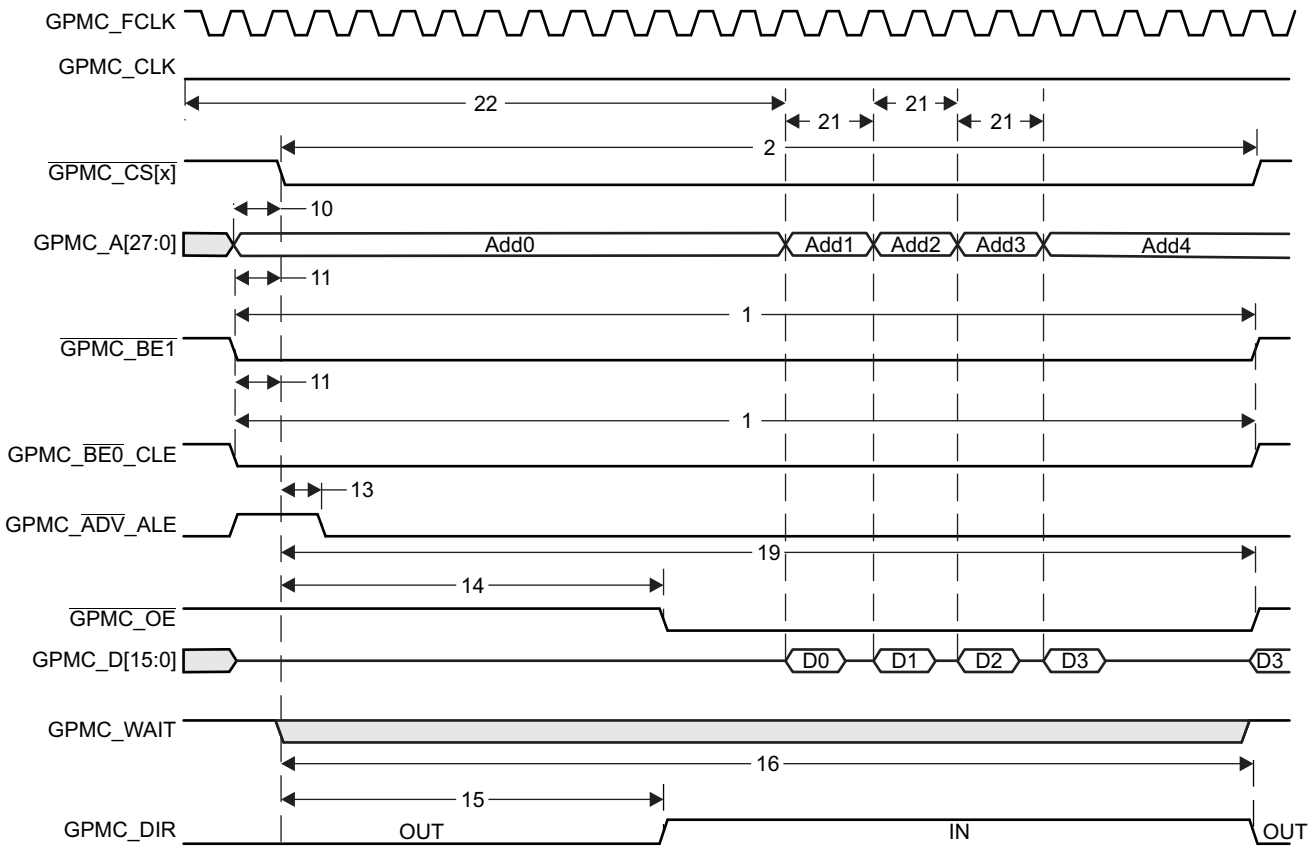


**Figure 9-58. GPMC Non-Multiplexed Only NOR Flash - Asynchronous Read - Page Mode 4x16-Bit Timing**

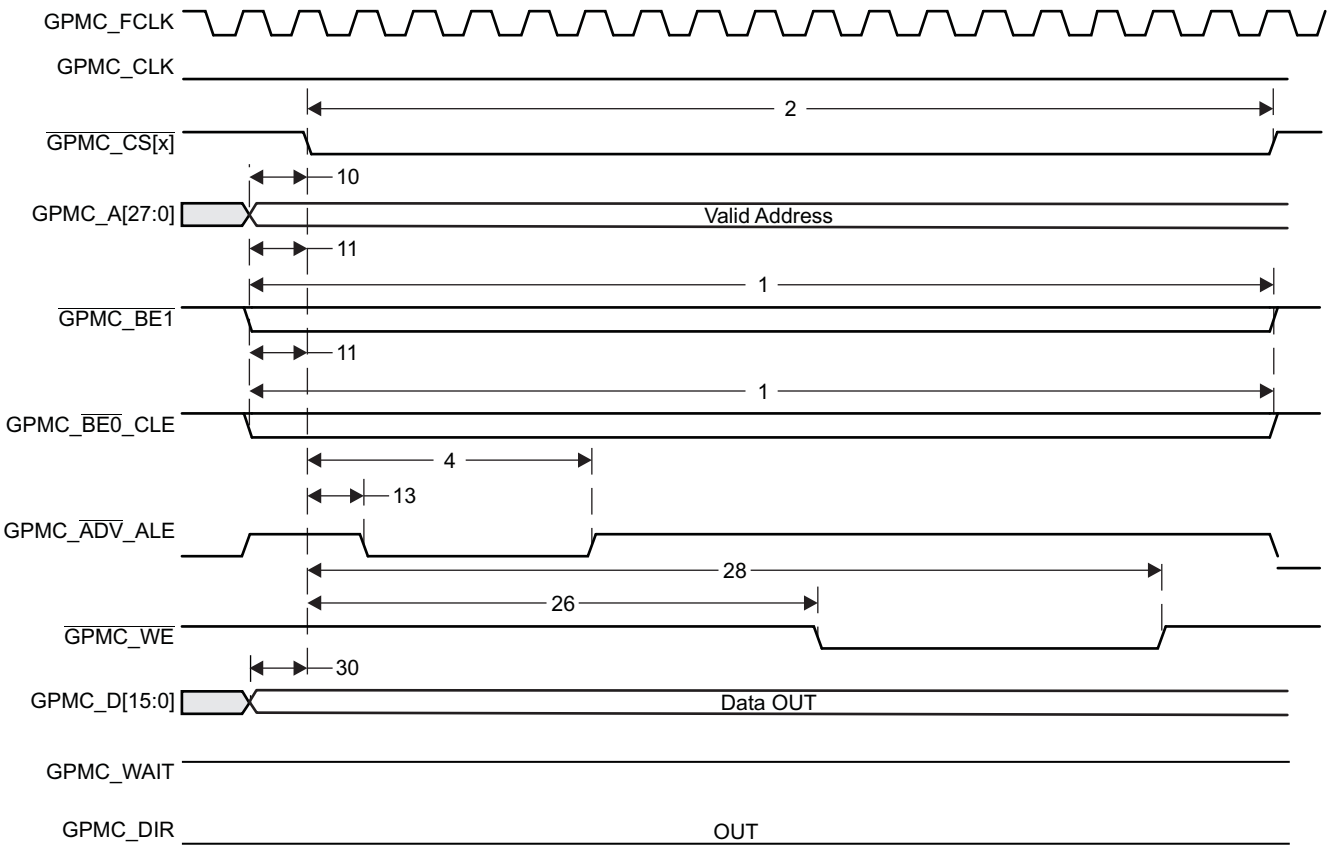


**Figure 9-59. GPMC Non-Multiplexed NOR Flash - Asynchronous Write - Single Word Timing**


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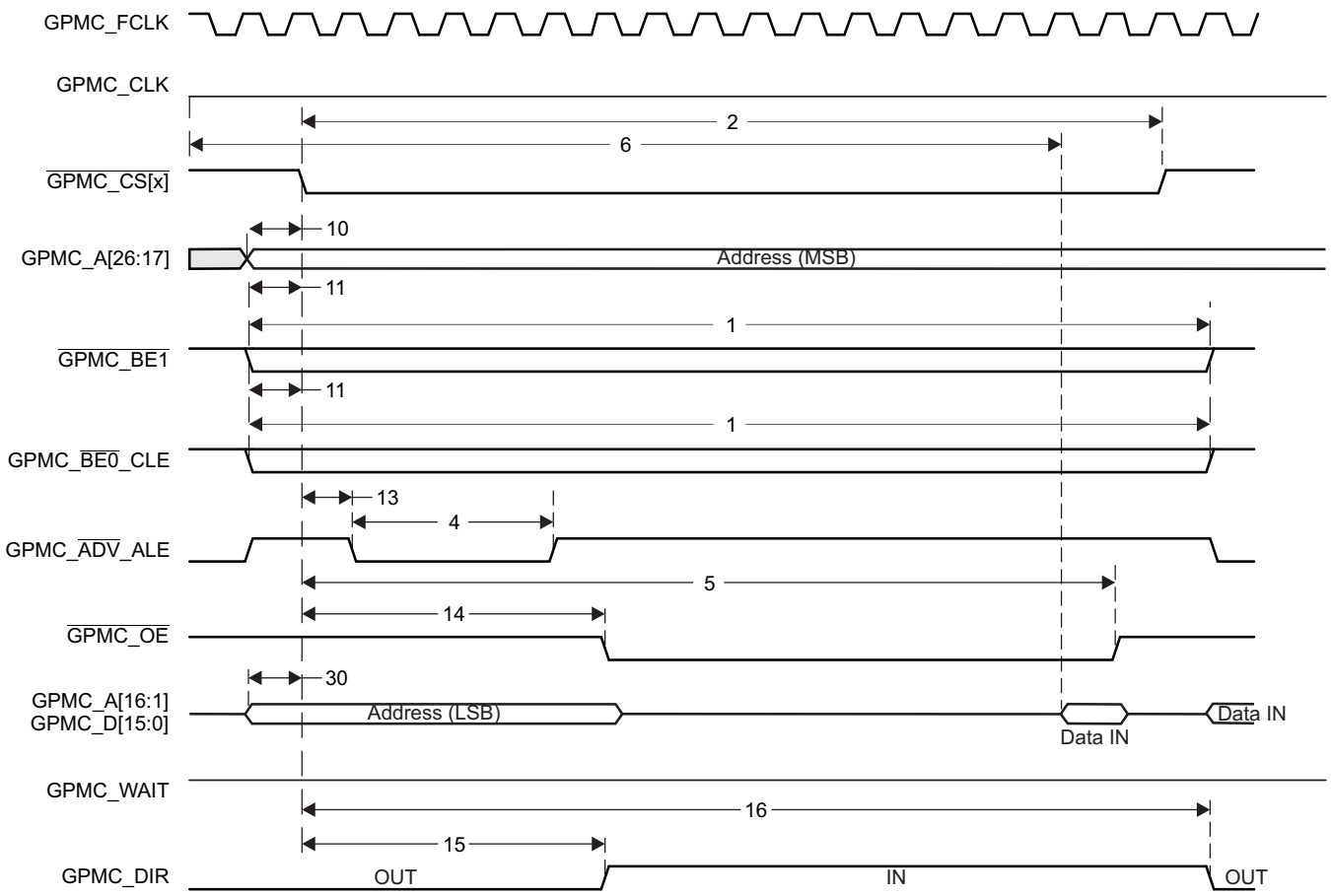


**Figure 9-60. GPMC Multiplexed NOR Flash - Asynchronous Read - Single Word Timing**

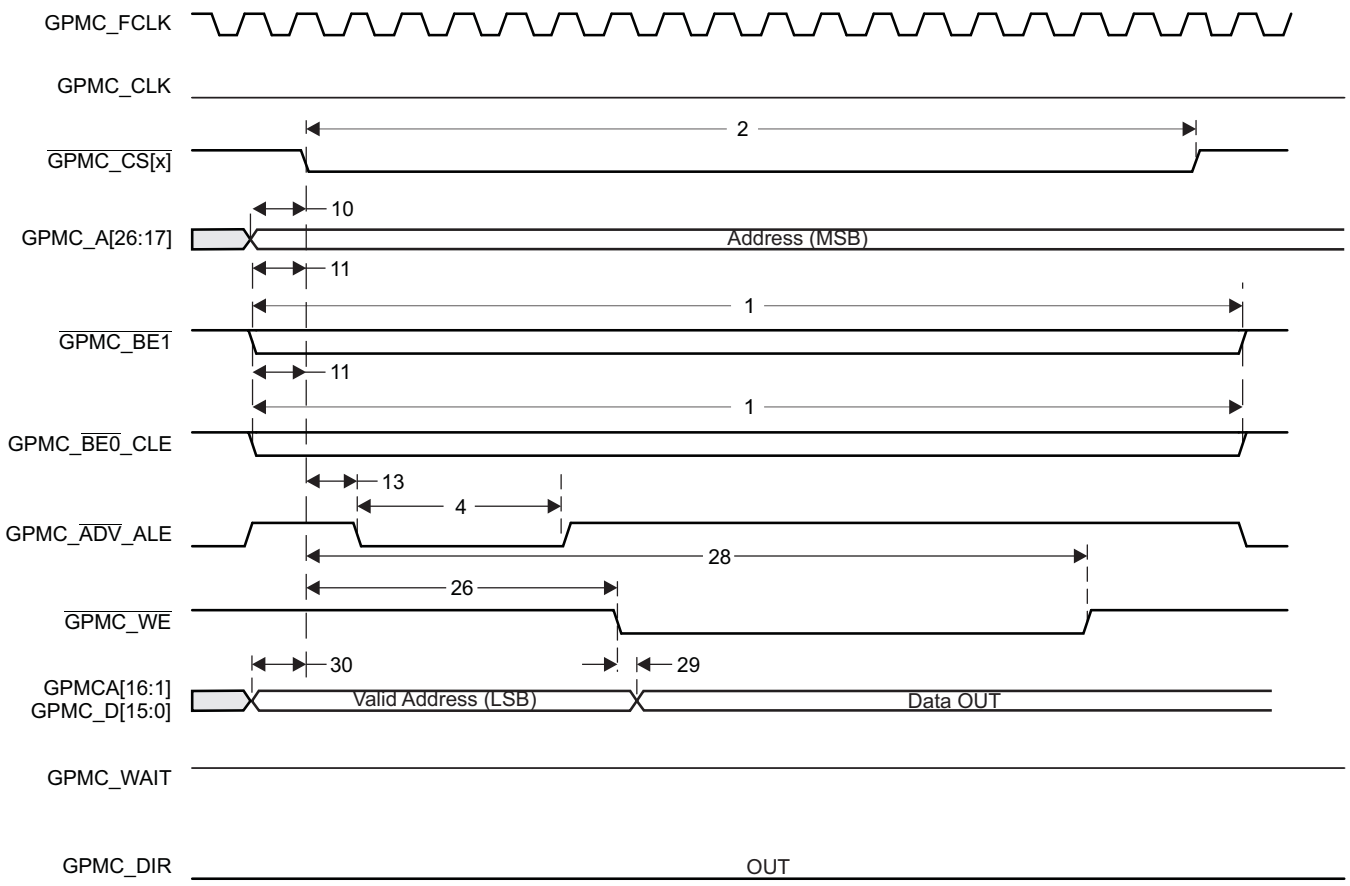


**Figure 9-61. GPMC Multiplexed NOR Flash - Asynchronous Write - Single Word Timing**


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### 9.8.2.3 GPMC and NAND Flash Interface Asynchronous Mode Timing

**Table 9-59. GPMC and NAND Flash Interface Asynchronous Mode Timing - Internal Parameters**

| NO. | | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | Max. output data generation delay from internal functional clock | | 6.5 | ns |
| 2 | Max. input data capture delay by internal functional clock | | 4.0 | ns |
| 3 | Max. chip select generation delay from internal functional clock | | 6.5 | ns |
| 4 | Max. address latch enable generation delay from internal functional clock | | 6.5 | ns |
| 5 | Max. command latch enable generation delay from internal functional clock | | 6.5 | ns |
| 6 | Max. output enable generation delay from internal functional clock | | 6.5 | ns |
| 7 | Max. write enable generation delay from internal functional clock | | 6.5 | ns |
| 8 | Max. functional clock skew | | 100.0 | ps |

**Table 9-60. Timing Requirements for GPMC and NAND Flash Interface**

(see Figure 9-64)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 13 | $t_{acc(DAT)}$ | Data maximum access time (GPMC_FCLK cycles) | | J(1) | cycles |

(1) J = AccessTime * (TimeParaGranularity + 1)

**Table 9-61. Switching Characteristics Over Recommended Operating Conditions for GPMC and NAND Flash Interface**

(see Figure 9-62, Figure 9-63, Figure 9-64, Figure 9-65)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(nWEV)}$ | Pulse duration, $\overline{\text{GPMC_WE}}$ valid time | | A(1) | ns |
| 2 | $t_{d(nCSV-nWEV)}$ | Delay time, $\overline{\text{GPMC_CS[x]}}$ valid to $\overline{\text{GPMC_WE}}$ valid | B - 0.2(2) | B + 2.0(2) | ns |
| 3 | $t_{d(CLEH-nWEV)}$ | Delay time, GPMC_$\overline{\text{BE0}}$_CLE high to $\overline{\text{GPMC_WE}}$ valid | C - 0.2(3) | C + 2.0(3) | ns |
| 4 | $t_{d(nWEV-DV)}$ | Delay time, GPMC_D[15:0] valid to $\overline{\text{GPMC_WE}}$ valid | D - 0.2(4) | D + 2.0(4) | ns |
| 5 | $t_{d(nWEIV-DIV)}$ | Delay time, $\overline{\text{GPMC_WE}}$ invalid to GPMC_D[15:0] invalid | E - 0.2(5) | E + 2.0(5) | ns |
| 6 | $t_{d(nWEIV-CLEIV)}$ | Delay time, $\overline{\text{GPMC_WE}}$ invalid to GPMC_$\overline{\text{BE0}}$_CLE invalid | F - 0.2(6) | F + 2.0(6) | ns |
| 7 | $t_{d(nWEIV-nCSIV)}$ | Delay time, $\overline{\text{GPMC_WE}}$ invalid to $\overline{\text{GPMC_CS[x]}}$ invalid | G - 0.2(7) | G + 2.0(7) | ns |
| 8 | $t_{d(ALEH-nWEV)}$ | Delay time, GPMC_$\overline{\text{ADV}}$_ALE High to $\overline{\text{GPMC_WE}}$ valid | C - 0.2(3) | C + 2.0(3) | ns |
| 9 | $t_{d(nWEIV-ALEIV)}$ | Delay time, $\overline{\text{GPMC_WE}}$ invalid to GPMC_$\overline{\text{ADV}}$_ALE invalid | F - 0.2(6) | F + 2.0(6) | ns |
| 10 | $t_{c(nWE)}$ | Cycle time, write cycle time | | H(8) | ns |
| 11 | $t_{d(nCSV-nOEV)}$ | Delay time, $\overline{\text{GPMC_CS[x]}}$ valid to $\overline{\text{GPMC_OE_RE}}$ valid | I - 0.2(9) | I + 2.0(9) | ns |
| 12 | $t_{w(nOEV)}$ | Pulse duration, $\overline{\text{GPMC_OE_RE}}$ valid time | | K(10) | ns |
| 13 | $t_{c(nOE)}$ | Cycle time, read cycle time | | L(11) | ns |

(1) A = (WEOffTime - WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) = B + nWE Min Delay - nCS Max Delay
B = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(3) = C + nWE Min Delay - CLE Max Delay
C = ((WEOnTime - ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - ADVExtraDelay)) * GPMC_FCLK
(4) = D + nWE Min Delay - Data Max Delay
D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay ) * GPMC_FCLK
(5) =E + Data Min Delay - nWE Max Delay
E = ((WrCycleTime - WEOffTime) * (TimeParaGranularity + 1) - 0.5 * WEExtraDelay ) * GPMC_FCLK
(6) = F + CLE Min Delay - nWE Max Delay
F = ((ADVWrOffTime - WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - WEExtraDelay )) * GPMC_FCLK
(7) =G + nCS Min Delay - nWE Max Delay
G = ((CSWrOffTime - WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - WEExtraDelay )) * GPMC_FCLK
(8) H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(9) = I + nOE Min Delay - nCS Max Delay
I = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(10) K = (OEOffTime - OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK
(11) L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK

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**Table 9-61. Switching Characteristics Over Recommended Operating Conditions for GPMC and NAND Flash Interface (continued)**

(see Figure 9-62, Figure 9-63, Figure 9-64, Figure 9-65)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 14 | $t_{d(nOEIV-nCSIV)}$ | Delay time, GPMC_OE_RE invalid to GPMC_CS[x] invalid | M - 0.2(12) | M + 2.0(12) | ns |

(12) =M + nCS Min Delay - nOE Max Delay
M = ((CSRdOffTime - OEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - OEExtraDelay ))* GPMC_FCLK

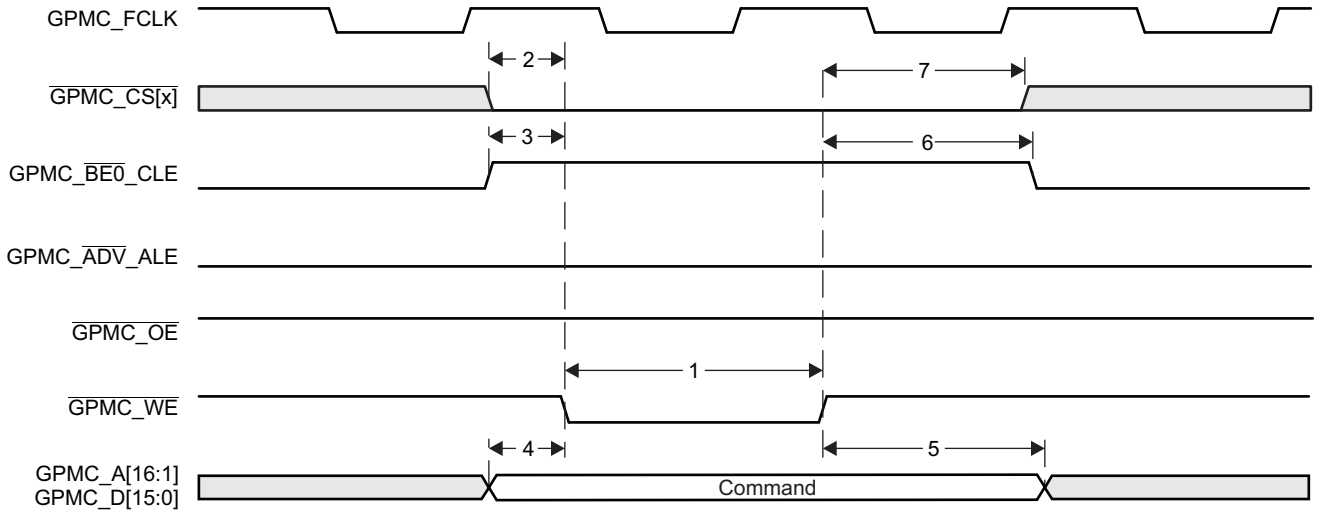


**Figure 9-62. GPMC and NAND Flash - Command Latch Cycle Timing**

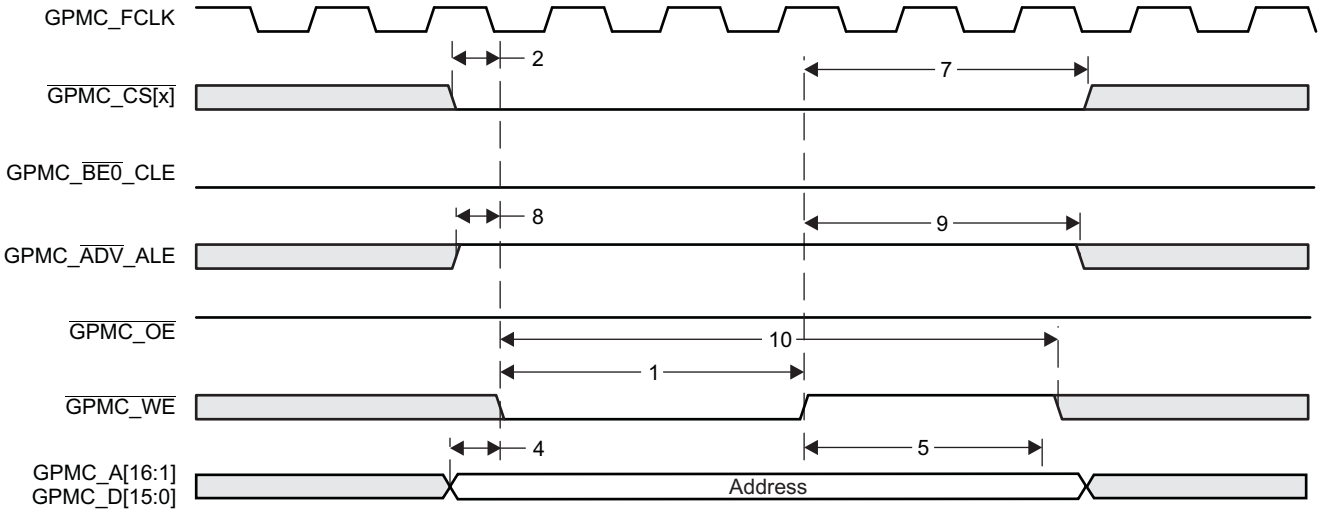


**Figure 9-63. GPMC and NAND Flash - Address Latch Cycle Timing**


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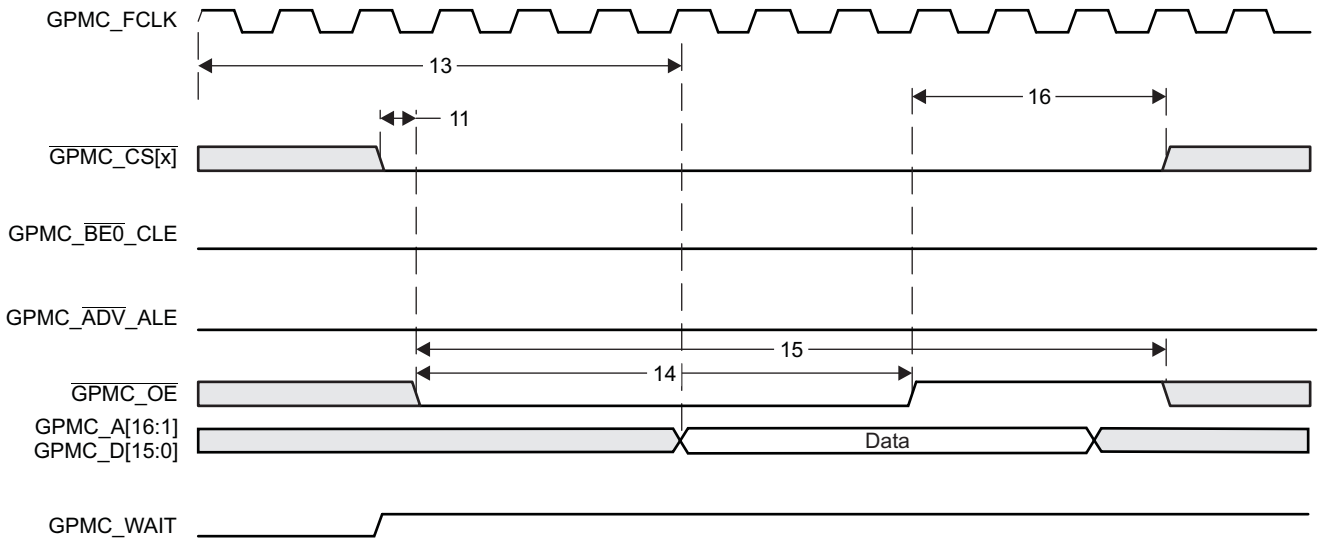


**Figure 9-64. GPMC and NAND Flash - Data Read Cycle Timing**

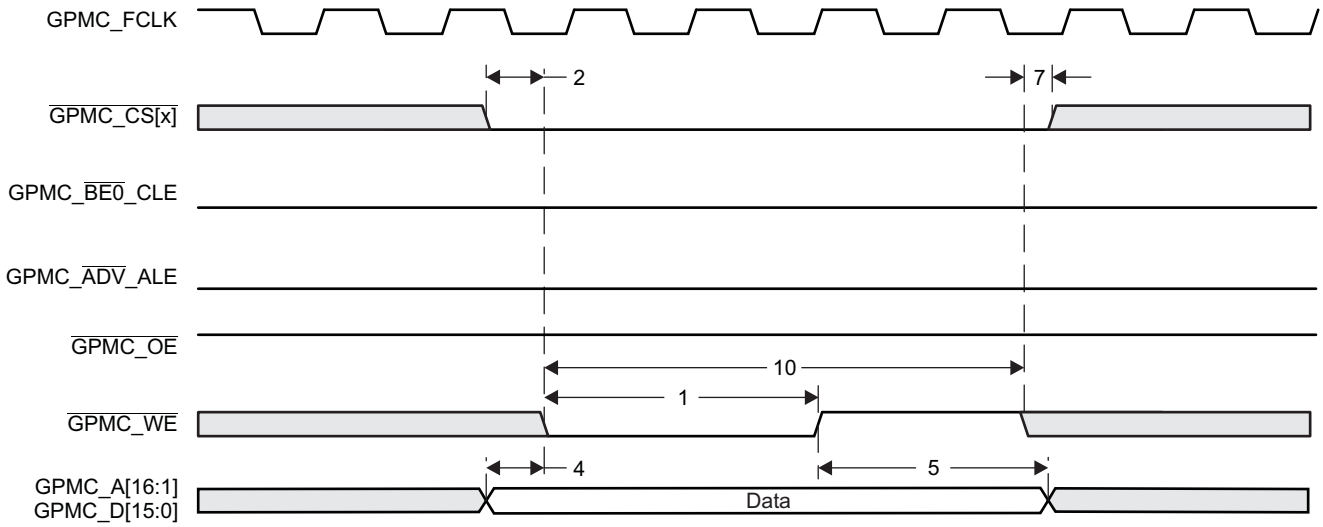


**Figure 9-65. GPMC and NAND Flash - Data Write Cycle Timing**

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## 9.9 High-Definition Multimedia Interface (HDMI)

The device includes an HDMI 1.3a-compliant transmitter for digital video and audio data to display devices. The HDMI interface consists of a digital HDMI transmitter core with TMDS encoder, a core wrapper with interface logic and control registers, and a transmit PHY, with the following features:

- Hot-plug detection
- Consumer electronics control (CEC) messages
- DVI 1.0 compliant (only RGB pixel format)
- CEA 861-D and VESA DMT formats
- Supports up to 165-MHz pixel clock:
  - 1920 x 1080p @75 Hz with 8-bit component color depth
  - 1920 x 1200 @60 Hz with 8-bit component color depth
  - 1600 x 1200 @60 Hz with 8-bit component color depth
- Support for deep-color mode:
  - 10-bit component color depth up to 1080p @60 Hz (maximum pixel clock = 148.5 MHz)
  - 12-bit component color depth at 720p or 1080i @60 Hz (maximum pixel clock = 123.75 MHz)
- Uncompressed multichannel (up to eight channels) audio (L-PCM) support
- Master I2C interface for display data channel (DDC) connection
- TMDS clock to the HDMI-PHY is up to 185.625 MHz
- Maximum supported pixel clock:
  - 165 MHz for 8-bit color depth
  - 148.5 MHz for 10-bit color depth
  - 123.75 MHz for 12-bit color depth
- Options available to support HDCP encryption engine for transmitting protected audio and video (contact local TI sales representative for information).

For more details on the HDMI, see the HDMI chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### *9.9.1 HDMI Interface Design Specifications*

**NOTE**

For more information on PCB layout, see the *DM816xx Easy CYG Package PCB Escape Routing* application report (literature number SPRABK6).

This section provides PCB design and layout specifications for the HDMI interface. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. Simulation and system design work has been done to ensure the HDMI interface requirements are met.

#### 9.9.1.1 HDMI Interface Schematic

The HDMI bus is separated into three main sections:

1. Transition Minimized Differential Signaling (TMDS) high-speed digital video interface
2. Display Data Channel (I2C bus for configuration and status exchange between two devices)
3. Consumer Electronics Control (optional) for remote control of connected devices.

The DDC and CEC are low-speed interfaces, so nothing special is required for PCB layout of these signals. Their connection is shown in Figure 9-66.

The TMDS channels are high-speed differential pairs and, therefore, require the most care in layout. Specifications for TMDS layout are below.


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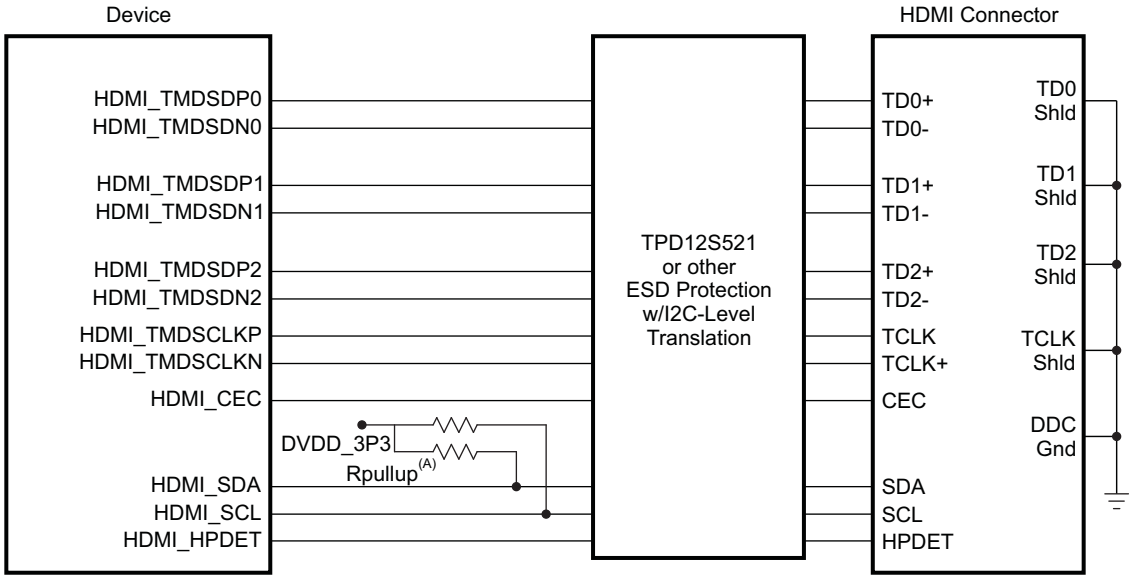
Figure 9-66 shows the HDMI interface schematic. The specific pin numbers can be obtained from Table 4-7, *HDMI Terminal Functions*.




A. 5K-10K Ω pullup resistors are required if not integrated in the ESD protection chip.

**Figure 9-66. HDMI Interface High-Level Schematic**

### 9.9.1.2 TMDS Routing

The TMDS signals are high-speed differential pairs. Care must be taken in the PCB layout of these signals to ensure good signal integrity.

The TMDS differential signal traces must be routed to achieve 100 Ω (±10%) differential impedance and 60 Ω (±10%) single-ended impedance. Single-ended impedance control is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 60 Ω impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations do not affect impedance as much; therefore, it is easier to maintain an accurate impedance over the length of the signal. The wider traces also show reduced skin effect and, therefore, often result in better signal integrity.

Table 9-62 shows the routing specifications for the TMDS signals.

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**Table 9-62. TMDS Routing Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Processor-to-HDMI header trace length | | | 7000 | Mils |
| Number of stubs allowed on TMDS traces | | | 0 | Stubs |
| TX and RX pair differential impedance | 90 | 100 | 110 | Ω |
| TX and RX single-ended impedance | 54 | 60 | 66 | Ω |
| Number of vias on each TMDS trace | | | 2 | Vias(1) |
| TMDS differential pair to any other trace spacing | 2*DS(2) | | | |

(1) Vias must be used in pairs with their distance minimized.
(2) DS = differential spacing of the HDMI traces.

#### 9.9.1.3 DDC Signals

As shown in Figure 9-66, the DDC connects just like a standard I2C bus. As such, resistor pullups must be used to pull up the open drain buffer signals unless they are integrated into the ESD protection chip used. If used, these pullup resistors should be connected to a 3.3-V supply.

#### 9.9.1.4 HDMI ESD Protection Device (Required)

Interfaces that connect to a cable such as HDMI generally require more ESD protection than can be built into the processor's outputs. Therefore, this HDMI interface requires the use of an ESD protection chip to provide adequate ESD protection and to translate I2C voltage levels from the 3.3 V supplied by the device to the 5 volts required by the HDMI specification.

When selecting an ESD protection chip, choose the lowest capacitance ESD protection available to minimize signal degradation. In no case should the ESD protection circuit capacitance be more than 5 pF.

TI manufactures devices that provide ESD protection for HDMI signals such as the TPD12S521. For more information see the www.ti.com website.

#### 9.9.1.5 PCB Stackup Specifications

Table 9-63 shows the stackup and feature sizes required for HDMI.

**Table 9-63. HDMI PCB Stackup Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCB routing and plane layers | 4 | 6 | - | Layers |
| Signal routing layers | 2 | 3 | - | Layers |
| Number of ground plane cuts allowed within HDMI routing region | - | - | 0 | Cuts |
| Number of layers between HDMI routing region and reference ground plane | - | - | 0 | Layers |
| PCB trace width | - | 4 | - | Mils |
| PCB BGA escape via pad size | - | 20 | - | Mils |
| PCB BGA escape via hole size | - | 10 | | Mils |
| Processor device BGA pad size(1)(2) | | 0.3 | | mm |

(1) Non-solder mask defined pad.
(2) Per IPC-7351A BGA pad size guideline.


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#### 9.9.1.6 Grounding

Each TMDS channel has its own shield pin which should be grounded to provide a return current path for the TMDS signal.

### *9.9.2 HDMI Peripheral Register Descriptions*

**Table 9-64. HDMI Wrapper Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 0000 | HDMI_WP_REVISION | IP Revision Identifier |
| 0x46C0 0010 | HDMI_WP_SYSCONFIG | Clock Management Configuration |
| 0x46C0 0024 | HDMI_WP_IRQSTATUS_RAW | Raw Interrupt Status |
| 0x46C0 0028 | HDMI_WP_IRQSTATUS | Interrupt Status |
| 0x46C0 002C | HDMI_WP_IRQENABLE_SET | Interrupt Enable |
| 0x46C0 0030 | HDMI_WP_IRQENABLE_CLR | Interrupt Disable |
| 0x46C0 0034 | HDMI_WP_IRQWAKEEN | IRQ Wakeup |
| 0x46C0 0050 | HDMI_WP_VIDEO_CFG | Configuration of HDMI Wrapper Video |
| 0x46C0 0070 | HDMI_WP_CLK | Configuration of Clocks |
| 0x46C0 0080 | HDMI_WP_AUDIO_CFG | Audio Configuration in FIFO |
| 0x46C0 0084 | HDMI_WP_AUDIO_CFG2 | Audio Configuration of DMA |
| 0x46C0 0088 | HDMI_WP_AUDIO_CTRL | Audio FIFO Control |
| 0x46C0 008C | HDMI_WP_AUDIO_DATA | TX Data of FIFO |

**Table 9-65. HDMI Core System Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 0400 | VND_IDL | Vendor ID |
| 0x46C0 0404 | VND_IDH | Vendor ID |
| 0x46C0 0408 | DEV_IDL | Device ID |
| 0x46C0 040C | DEV_IDH | Device ID |
| 0x46C0 0410 | DEV_REV | Device Revision |
| 0x46C0 0414 | SRST | Software Reset |
| 0x46C0 0420 | SYS_CTRL1 | System Control 1 |
| 0x46C0 0424 | SYS_STAT | System Status |
| 0x46C0 0428 | SYS_CTRL3 | Legacy |
| 0x46C0 0434 | DCTL | Data Control |
| 0x46C0 043C - 0x46C0 0494 | - | Reserved |
| 0x46C0 0498 | RI_STAT | Ri Status |
| 0x46C0 049C | RI_CMD | Ri Command |
| 0x46C0 04A0 | RI_START | Ri Line Start |
| 0x46C0 04A4 | RI_RX_L | Ri From RX |
| 0x46C0 04A8 | RI_RX_H | Ri From RX |
| 0x46C0 04AC | RI_DEBUG | Ri Debug |
| 0x46C0 04C8 | DE_DLY | VIDEO DE Delay |
| 0x46C0 04C8 | DE_DLY | VIDEO DE Delay |
| 0x46C0 04CC | DE_CTRL | VIDEO DE Control |
| 0x46C0 04D0 | DE_TOP | VIDEO DE Top |
| 0x46C0 04D8 | DE_CNTL | VIDEO DE Count |
| 0x46C0 04DC | DE_CNTH | VIDEO DE Count |
| 0x46C0 04E0 | DE_LINL | VIDEO DE Line |
| 0x46C0 04E4 | DE_LINH_1 | VIDEO DE Line |

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**Table 9-65. HDMI Core System Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 04E8 | HRES_L | Video H Resolution |
| 0x46C0 04EC | HRES_H | Video H Resolution |
| 0x46C0 04F0 | VRES_L | Video V Resolution |
| 0x46C0 04F4 | VRES_H | Video V Resolution |
| 0x46C0 04F8 | IADJUST | Video Interlace Adjustment |
| 0x46C0 04FC | POL_DETECT | Video SYNC Polarity Detection |
| 0x46C0 0500 | HBIT_2HSYNC1 | Video Hbit to HSYNC |
| 0x46C0 0504 | HBIT_2HSYNC2 | Video Hbit to HSYNC |
| 0x46C0 0508 | FLD2_HS_OFSTL | Video Field2 HSYNC Offset |
| 0x46C0 050C | FLD2_HS_OFSTH | Video Field2 HSYNC Offset |
| 0x46C0 0510 | HWIDTH1 | Video HSYNC Length |
| 0x46C0 0514 | HWIDTH2 | Video HSYNC Length |
| 0x46C0 0518 | VBIT_TO_VSYNC | Video Vbit to VSYNC |
| 0x46C0 051C | VWIDTH | Video VSYNC Length |
| 0x46C0 0520 | VID_CTRL | Video Control |
| 0x46C0 0524 | VID_ACEN | Video Action Enable |
| 0x46C0 0528 | VID_MODE | Video Mode1 |
| 0x46C0 052C | VID_BLANK1 | Video Blanking |
| 0x46C0 0530 | VID_BLANK2 | Video Blanking |
| 0x46C0 0534 | VID_BLANK3 | Video Blanking |
| 0x46C0 0538 | DC_HEADER | Deep Color Header |
| 0x46C0 053C | VID_DITHER | Video Mode2 |
| 0x46C0 0540 | RGB2XVYCC_CT | RGB_2_xvYCC control |
| 0x46C0 0544 | R2Y_COEFF_LOW | RGB_2_xvYCC Conversion R_2_Y |
| 0x46C0 0548 | R2Y_COEFF_UP | RGB_2_xvYCC Conversion R_2_Y |
| 0x46C0 054C | G2Y_COEFF_LOW | RGB_2_xvYCC Conversion G_2_Y |
| 0x46C0 0550 | G2Y_COEFF_UP | RGB_2_xvYCC Conversion G_2_Y |
| 0x46C0 0554 | B2Y_COEFF_LOW | RGB_2_xvYCC Conversion B_2_Y |
| 0x46C0 0558 | B2Y_COEFF_UP | RGB_2_xvYCC Conversion B_2_Y |
| 0x46C0 055C | R2CB_COEFF_LOW | RGB_2_xvYCC Conversion R_2_Cb |
| 0x46C0 0560 | R2CB_COEFF_UP | RGB_2_xvYCC Conversion R_2_Cb |
| 0x46C0 0564 | G2CB_COEFF_LOW | RGB_2_xvYCC Conversion G_2_Cb |
| 0x46C0 0568 | G2CB_COEFF_UP | RGB_2_xvYCC Conversion G_2_Cb |
| 0x46C0 056C | B2CB_COEFF_LOW | RGB_2_xvYCC Conversion B_2_Cb |
| 0x46C0 0570 | B2CB_COEFF_UP | RGB_2_xvYCC Conversion B_2_Cb |
| 0x46C0 0574 | R2CR_COEFF_LOW | RGB_2_xvYCC Conversion R_2_Cr |
| 0x46C0 0578 | R2CR_COEFF_UP | RGB_2_xvYCC Conversion R_2_Cr |
| 0x46C0 057C | G2CR_COEFF_LOW | RGB_2_xvYCC Conversion G_2_Cr |
| 0x46C0 0580 | G2CR_COEFF_UP | RGB_2_xvYCC Conversion G_2_Cr |
| 0x46C0 0584 | B2CR_COEFF_LOW | RGB_2_xvYCC Conversion B_2_Cr |
| 0x46C0 0588 | B2CR_COEFF_UP | RGB_2_xvYCC Conversion B_2_Cr |
| 0x46C0 058C | RGB_OFFSET_LOW | RGB_2_xvYCC RGB Input Offset |
| 0x46C0 0590 | RGB_OFFSET_UP | RGB_2_xvYCC RGB Input Offset |
| 0x46C0 0594 | Y_OFFSET_LOW | RGB_2_xvYCC Conversion Y Output Offset |
| 0x46C0 0598 | Y_OFFSET_UP | RGB_2_xvYCC Conversion Y Output Offset |
| 0x46C0 059C | CBCR_OFFSET_LOW | RGB_2_xvYCC Conversion CbCr Output Offset |
| 0x46C0 05A0 | CBCR_OFFSET_UP | RGB_2_xvYCC Conversion CbCr Output Offset |


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**Table 9-65. HDMI Core System Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 05C0 | INTR_STATE | Interrupt State |
| 0x46C0 05C4 | INTR1 | Interrupt Source |
| 0x46C0 05C8 | INTR2 | Interrupt Source |
| 0x46C0 05CC | INTR3 | Interrupt Source |
| 0x46C0 05D0 | INTR4 | Interrupt Source |
| 0x46C0 05D4 | INT_UNMASK1 | Interrupt Unmask |
| 0x46C0 05D8 | INT_UNMASK2 | Interrupt Unmask |
| 0x46C0 05DC | INT_UNMASK3 | Interrupt Unmask |
| 0x46C0 05E0 | INT_UNMASK4 | Interrupt Unmask |
| 0x46C0 05E4 | INT_CTRL | Interrupt Control |
| 0x46C0 0640 | XVYCC2RGB_CTL | xvYCC_2_RGB Control |
| 0x46C0 0644 | Y2R_COEFF_LOW | xvYCC_2_RGB Conversion Y_2_R |
| 0x46C0 0648 | Y2R_COEFF_UP | xvYCC_2_RGB Conversion Y_2_R |
| 0x46C0 064C | CR2R_COEFF_LOW | xvYCC_2_RGB Conversion Cr_2_R |
| 0x46C0 0650 | CR2R_COEFF_UP | xvYCC_2_RGB Conversion Cr_2_R |
| 0x46C0 0654 | CB2B_COEFF_LOW | xvYCC_2_RGB Conversion Cb_2_B |
| 0x46C0 0658 | CB2B_COEFF_UP | xvYCC_2_RGB Conversion Cb_2_B |
| 0x46C0 065C | CR2G_COEFF_LOW | xvYCC_2_RGB Conversion Cr_2_G |
| 0x46C0 0660 | CR2G_COEFF_UP | xvYCC_2_RGB Conversion Cr_2_G |
| 0x46C0 0664 | CB2G_COEFF_LOW | xvYCC_2_RGB Conversion Cb_2_G |
| 0x46C0 0668 | CB2G_COEFF_UP | xvYCC_2_RGB Conversion Cb_2_G |
| 0x46C0 066C | YOFFSET1_LOW | xvYCC_2_RGB Conversion Y Offset |
| 0x46C0 0670 | YOFFSET1_UP | xvYCC_2_RGB Conversion Y Offset |
| 0x46C0 0674 | OFFSET1_LOW | xvYCC_2_RGB Conversion Offset1 |
| 0x46C0 0678 | OFFSET1_MID | xvYCC_2_RGB Conversion Offset1 |
| 0x46C0 067C | OFFSET1_UP | xvYCC_2_RGB Conversion Offset1 |
| 0x46C0 0680 | OFFSET2_LOW | xvYCC_2_RGB Conversion Offset2 |
| 0x46C0 0684 | OFFSET2_UP | xvYCC_2_RGB Conversion Offset2 |
| 0x46C0 0688 | DCLEVEL_LOW | xvYCC_2_RGB Conversion DC Level |
| 0x46C0 068C | DCLEVEL_UP | xvYCC_2_RGB Conversion DC Level |
| 0x46C0 07B0 | DDC_MAN | DDC I2C Manual |
| 0x46C0 07B4 | DDC_ADDR | DDC I2C Target Slave Address |
| 0x46C0 07B8 | DDC_SEGM | DDC I2C Target Segment Address |
| 0x46C0 07BC | DDC_OFFSET | DDC I2C Target Offset Address |
| 0x46C0 07C0 | DDC_COUNT1 | DDC I2C Data Count |
| 0x46C0 07C4 | DDC_COUNT2 | DDC I2C Data Count |
| 0x46C0 07C8 | DDC_STATUS | DDC I2C Status |
| 0x46C0 07CC | DDC_CMD | DDC I2C Command |
| 0x46C0 07D0 | DDC_DATA | DDC I2C Data |
| 0x46C0 07D4 | DDC_FIFOCNT | DDC I2C FIFO Count |
| 0x46C0 07E4 | EPST | ROM Status |
| 0x46C0 07E8 | EPCM | ROM Command |

**Table 9-66. HDMI IP Core Gamut Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 0800 | GAMUT_HEADER1 | Gamut Metadata |
| 0x46C0 0804 | GAMUT_HEADER2 | Gamut Metadata |

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**Table 9-66. HDMI IP Core Gamut Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 0808 | GAMUT_HEADER3 | Gamut Metadata |
| 0x46C0 080C - 0x46C0 0878 (0x4 byte increments) | GAMUT_DBYTE__0 - GAMUT_DBYTE__27 | Gamut Metadata |

**Table 9-67. HDMI IP Core Audio Video Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 0904 | ACR_CTRL | ACR Control |
| 0x46C0 0908 | FREQ_SVAL | ACR Audio Frequency |
| 0x46C0 090C | N_SVAL1 | ACR N Software Value |
| 0x46C0 0910 | N_SVAL2 | ACR N Software Value |
| 0x46C0 0914 | N_SVAL3 | ACR N Software Value |
| 0x46C0 0918 | CTS_SVAL1 | ACR CTS Software Value |
| 0x46C0 091C | CTS_SVAL2 | ACR CTS Software Value |
| 0x46C0 0920 | CTS_SVAL3 | ACR CTS Software Value |
| 0x46C0 0924 | CTS_HVAL1 | ACR CTS Hardware Value |
| 0x46C0 0928 | CTS_HVAL2 | ACR CTS Hardware Value |
| 0x46C0 092C | CTS_HVAL3 | ACR CTS Hardware Value |
| 0x46C0 0950 | AUD_MODE | Audio In Mode |
| 0x46C0 0954 | SPDIF_CTRL | Audio In SPDIF Control |
| 0x46C0 0960 | HW_SPDIF_FS | Audio In SPDIF Extracted Fs and Length |
| 0x46C0 0964 | SWAP_I2S | Audio In I2S Channel Swap |
| 0x46C0 096C | SPDIF_ERTH | Audio Error Threshold |
| 0x46C0 0970 | I2S_IN_MAP | Audio In I2S Data In Map |
| 0x46C0 0974 | I2S_IN_CTRL | Audio In I2S Control |
| 0x46C0 0978 | I2S_CHST0 | Audio In I2S Channel Status |
| 0x46C0 097C | I2S_CHST1 | Audio In I2S Channel Status |
| 0x46C0 0980 | I2S_CHST2 | Audio In I2S Channel Status |
| 0x46C0 0984 | I2S_CHST4 | Audio In I2S Channel Status |
| 0x46C0 0988 | I2S_CHST5 | Audio In I2S Channel Status |
| 0x46C0 098C | ASRC | Audio Sample Rate Conversion |
| 0x46C0 0990 | I2S_IN_LEN | Audio I2S Input Length |
| 0x46C0 09BC | HDMI_CTRL | HDMI Control |
| 0x46C0 09C0 | AUDO_TXSTAT | Audio Path Status |
| 0x46C0 09CC | AUD_PAR_BUSCLK_1 | Audio Input Data Rate Adjustment |
| 0x46C0 09D0 | AUD_PAR_BUSCLK_2 | Audio Input Data Rate Adjustment |
| 0x46C0 09D4 | AUD_PAR_BUSCLK_3 | Audio Input Data Rate Adjustment |
| 0x46C0 09F0 | TEST_TXCTRL | Test Control |
| 0x46C0 09F4 | DPD | Diagnostic Power Down |
| 0x46C0 09F8 | PB_CTRL1 | Packet Buffer Control 1 |
| 0x46C0 09FC | PB_CTRL2 | Packet Buffer Control 2 |
| 0x46C0 0A00 | AVI_TYPE | Packet |
| 0x46C0 0A04 | AVI_VERS | Packet |
| 0x46C0 0A08 | AVI_LEN | Packet |
| 0x46C0 0A0C | AVI_CHSUM | Packet |
| 0x46C0 0A10 - 0x46C0 0A48 (0x4 byte increments) | AVI_DBYTE__0 - AVI_DBYTE__14 | Packet |
| 0x46C0 0A80 | SPD_TYPE | SPD InfoFrame |
| 0x46C0 0A84 | SPD_VERS | SPD InfoFrame |


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**Table 9-67. HDMI IP Core Audio Video Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 0A88 | SPD_LEN | SPD InfoFrame |
| 0x46C0 0A8C | SPD_CHSUM | SPD InfoFrame |
| 0x46C0 0A90 - 0x46C0 0AF8 (0x4 byte increments) | SPD_DBYTE__0 - SPD_DBYTE__26 | SPD InfoFrame |
| 0x46C0 0B00 | AUDIO_TYPE | Audio InfoFrame |
| 0x46C0 0B04 | AUDIO_VERS | Audio InfoFrame |
| 0x46C0 0B08 | AUDIO_LEN | Audio InfoFrame |
| 0x46C0 0B0C | AUDIO_CHSUM | Audio InfoFrame |
| 0x46C0 0B10 - 0x46C0 0B34 (0x4 byte increments) | AUDIO_DBYTE__0 - AUDIO_DBYTE__9 | Audio InfoFrame |
| 0x46C0 0B80 | MPEG_TYPE | MPEG InfoFrame |
| 0x46C0 0B84 | MPEG_VERS | MPEG InfoFrame |
| 0x46C0 0B88 | MPEG_LEN | MPEG InfoFrame |
| 0x46C0 0B8C | MPEG_CHSUM | MPEG InfoFrame |
| 0x46C0 0B90 - 0x46C0 0BF8 (0x4 byte increments) | MPEG_DBYTE__0 - MPEG_DBYTE__26 | MPEG InfoFrame |
| 0x46C0 0C00 - 0x46C0 0C78 (0x4 byte increments) | GEN_DBYTE__0 - GEN_DBYTE__30 | Generic Packet |
| 0x46C0 0C7C | CP_BYTE1 | General Control Packet |
| 0x46C0 0C80 - 0x46C0 0CF8 (0x4 byte increments) | GEN2_DBYTE__0 - GEN2_DBYTE__30 | Generic Packet 2 |
| 0x46C0 0CFC | CEC_ADDR_ID | CEC Slave ID |

**Table 9-68. HDMI IP Core CEC Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 0D00 | CEC_DEV_ID | CEC Device ID |
| 0x46C0 0D04 | CEC_SPEC | CEC Specification |
| 0x46C0 0D08 | CEC_SUFF | CEC Specification Suffix |
| 0x46C0 0D0C | CEC_FW | CEC Firmware Revision |
| 0x46C0 0D10 | CEC_DBG_0 | CEC Debug 0 |
| 0x46C0 0D14 | CEC_DBG_1 | CEC Debug 1 |
| 0x46C0 0D18 | CEC_DBG_2 | CEC Debug 2 |
| 0x46C0 0D1C | CEC_DBG_3 | CEC Debug 3 |
| 0x46C0 0D20 | CEC_TX_INIT | CEC Tx Initialization |
| 0x46C0 0D24 | CEC_TX_DEST | CEC Tx Destination |
| 0x46C0 0D38 | CEC_SETUP | CEC Set Up |
| 0x46C0 0D3C | CEC_TX_COMMAND | CEC Tx Command |
| 0x46C0 0D40 - 0x46C0 0D78 (0x4 byte increments) | CEC_TX_OPERAND__0 - CEC_TX_OPERAND__14 | CEC Tx Operand |
| 0x46C0 0D7C | CEC_TRANSMIT_DATA | CEC Transmit Data |
| 0x46C0 0D88 | CEC_CA_7_0 | CEC Capture ID0 |
| 0x46C0 0D8C | CEC_CA_15_8 | CEC Capture ID0 |
| 0x46C0 0D90 | CEC_INT_ENABLE_0 | CEC Interrupt Enable 0 |
| 0x46C0 0D94 | CEC_INT_ENABLE_1 | CEC Interrupt Enable 1 |
| 0x46C0 0D98 | CEC_INT_STATUS_0 | CEC Interrupt Status 0 |
| 0x46C0 0D9C | CEC_INT_STATUS_1 | CEC Interrupt Status 1 |
| 0x46C0 0DB0 | CEC_RX_CONTROL | CEC RX Control |
| 0x46C0 0DB4 | CEC_RX_COUNT | CEC Rx Count |
| 0x46C0 0DB8 | CEC_RX_CMD_HEADER | CEC Rx Command Header |

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**Table 9-68. HDMI IP Core CEC Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x46C0 0DBC | CEC_RX_COMMAND | CEC Rx Command |
| 0x46C0 0DC0 - 0x46C0 0DF8 (0x4 byte increments) | CEC_RX_OPERAND__0 - CEC_RX_OPERAND__14 | CEC Rx Operand |

**Table 9-69. HDMI PHY Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4812 2004 | TMDS_CNTL2 | TMDS Control |
| 0x4812 2008 | TMDS_CNTL3 | TMDS Control |
| 0x4812 200C | BIST_CNTL | BIST Control |
| 0x4812 2020 | TMDS_CNTL9 | TMDS Control |


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## 9.10 High-Definition Video Processing Subsystem (HDVPSS)

The device High-Definition Video Processing Subsystem (HDVPSS) provides a video input interface for external imaging peripherals (that is, image sensors, video decoders, and others) and a video output interface for display devices, such as analog SDTV displays, analog and digital HDTV displays, and digital LCD panels. It includes HD and SD video encoders, and an HDMI transmitter interface.

The device HDVPSS features include:

- High quality (HD) and medium quality (SD) display processing pipelines with de-interlacing, scaling, noise reduction, alpha blending, chroma keying, color space conversion, flicker filtering, and pixel format conversion.
- HD and SD compositor features for PIP support.
- Format conversions (up to 1080p 60 Hz) include scan format conversion, scan rate conversion, aspect-ratio conversion, and frame size conversion.
- Supports additional video processing capabilities by using the subsystem's memory-to-memory feature.
- Two parallel video processing pipelines support HD (up to 1080p60) and SD (NTSC and PAL) simultaneous outputs.
  - HD analog component output with OSD and embedded timing codes (BT.1120)
    - 3-channel HD-DAC with 12-bit resolution.
    - External HSYNC and VSYNC signals available on silicon revision 2.x devices. For more details, see below.
  - SD analog output with OSD with embedded timing codes (BT.656)
    - Simultaneous component, S-video and composite
    - 4-channel SD-DAC with 10-bit resolution
    - Options available to support MacroVision and CGMS-A (contact local TI Sales rep for information).
  - Digital HDMI 1.3a compliant transmitter (for details, see Section 9.9, *High-Definition Multimedia Interface (HDMI)*).
- Up to two (one 16-bit, 24-bit, 30-bit and one 16-bit) digital video outputs (up to 165 MHz).
  - VOUT[0] can output up to 30-bit video and supports RGB, YUV444, Y and C and BT.656 modes.
  - VOUT[1] can output up to 16-bit video and supports Y and C and BT.656 modes.
- Two (one 16-bit, 24-bit and one 16-bit) independently configurable external video input capture ports (up to 165 MHz).
  - 16-bit and 24-bit HD digital video input or dual clock independent 8-bit SD inputs on each capture port.
    - VIN[0] can accept single-channel 16-bit, 24-bit (YCbCr and RGB) video or dual-channel 8-bit (YCbCr) video.
    - VIN[1] can accept single-channel 16-bit (YCbCr) video or dual-channel 8-bit (YCbCr) video.
  - Embedded sync and external sync modes are supported for all input configurations.
  - De-multiplexing of both pixel-to-pixel and line-to-line multiplexed streams, effectively supporting up to 16 simultaneous SD inputs with a glueless interface to an external multiplexer such as the TVP5158.
  - Additional features include: programmable color space conversion, scaler and chroma downsampler, ancillary VANC and VBI data capture (decoded by software), noise reduction.

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- Availability of a combination of these digital video input and output port configurations, control signals for multiple 8-bit ports, as well as separate synchronization signals is limited by the device pin multiplexing (for details, see Section 6.5). The following video inputs and outputs are not multiplexed and are always available:
  - SD DAC composite, S-video, component out
  - HD DAC component out
  - HDMI output (same as VOUT[1])
  - 16-bit VOUT[0] (embedded sync)
  - Single 16-bit, dual 8-bit VIN[0] (embedded sync).
- Graphics features:
  - Three independently-generated graphics layers.
  - Each supports full-screen resolution graphics in HD, SD or both.
  - Up and down scaler optimized for graphics.
  - Global and pixel-level alpha blending supported.
- Discrete external HSYNC and VSYNC signals for the HD-DAC are available on silicon revision 2.x devices. These signals are mapped to the following pins (for details, see Section 4.2.20):
  - HSYNC - AR5, AT9, AR8
  - VSYNC - AL5, AP9, AL9

    The functionality of these pins is set using the SPARE_CTRL0 register (address: 0x4814 0724). Figure 9-67 and Table 9-70 describe the SPARE_CTRL0 register.

    **Note:** When changing this register, read original value and write back same value in Reserved fields.

    For example, these are the steps required to use the pins AR8 and AL9 as the DAC_HSYNC and VSYNC signals:

    1. Set the PINCTRLx registers for AR8 and AL9 as follows:
       - 0x4814 0894 = 0x00000001
       - 0x4814 0898 = 0x00000001
    2. Select analog VENC sync out option as follows:
       - 0x4814 0724 = 0x00000004

| 31 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Reserved | | SPR_CTL0_2 | SPR_CTL0_1 | Rsvd |

**Figure 9-67. SPARE_CTRL0 Register**

**Table 9-70. SPARE_CTRL0 Register Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31:3 | Reserved | 0 | Reserved |
| 2 | SPR_CTL0_2 | | To Select DAC or VOUT[0] Source Signals |
| | | 0 | Selects VOUT[0]_AVID and VOUT[0]_FLD |
| | | 1 | Selects DAC_HSYNC and DAC_VSYNC |
| 1 | SPR_CTL0_1 | | To Select DAC or VOUT[1] Source Signals |
| | | 0 | Selects VOUT[1]_HSYNC and VOUT[1]_VSYNC |
| | | 1 | Selects DAC_HSYNC and DAC_VSYNC |
| 0 | Reserved | 0 | Reserved |

For more detailed information on specific features, see the HDVPSS chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).


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### 9.10.1 HDVPSS Electrical Data and Timing

**Table 9-71. Timing Requirements for HDVPSS Input**

(see Figure 9-68 and Figure 9-69)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **VIN[x]A_CLK** | | | | | |
| 1 | $t_{c(CLK)}$ | Cycle time, VIN[x]A_CLK | 6.06 (1) | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse duration, VIN[x]A_CLK high (45% of $t_c$) | 2.73 | | ns |
| 3 | $t_{w(CLKH)}$ | Pulse duration, VIN[x]A_CLK low (45% of $t_c$) | 2.73 | | ns |
| 7 | $t_{t(CLK)}$ | Transition time, VIN[x]A_CLK (10%-90%) | | 2.64 | ns |
| 4 | $t_{su(DE-CLK)}$ | Input setup time, control valid to VIN[x]A_CLK high | 3.75 | | ns |
| | $t_{su(VSYNC-CLK)}$ | | | | |
| | $t_{su(FLD-CLK)}$ | | | | |
| | $t_{su(HSYNC-CLK)}$ | | | | |
| | $t_{su(D-CLK)}$ | Input setup time, data valid to VIN[x]A_CLK high | 3.75 | | |
| 5 | $t_{h(CLK-DE)}$ | Input hold time, control valid from VIN[x]A_CLK high | 0 (2) | | ns |
| | $t_{h(CLK-VSYNC)}$ | | | | |
| | $t_{h(CLK-FLD)}$ | | | | |
| | $t_{h(CLK-HSYNC)}$ | | | | |
| | $t_{h(CLK-D)}$ | Input hold time, data valid from VIN[x]A_CLK high | 0 (2) | | |
| **VIN[x]B_CLK** | | | | | |
| 1 | $t_{c(CLK)}$ | Cycle time, VIN[x]B_CLK | 6.06 (1) | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse duration, VIN[x]B_CLK high (45% of $t_c$) | 2.73 | | ns |
| 3 | $t_{w(CLKH)}$ | Pulse duration, VIN[x]B_CLK low (45% of $t_c$) | 2.73 | | ns |
| 7 | $t_{t(CLK)}$ | Transition time, VIN[x]B_CLK (10%-90%) | | 2.64 | ns |
| 4 | $t_{su(DE-CLK)}$ | Input setup time, control valid to VIN[x]B_CLK high | 3.75 | | ns |
| | $t_{su(VSYNC-CLK)}$ | | | | |
| | $t_{su(FLD-CLK)}$ | | | | |
| | $t_{su(HSYNC-CLK)}$ | | | | |
| | $t_{su(D-CLK)}$ | Input setup time, data valid to VIN[x]B_CLK high | 3.75 | | |
| 5 | $t_{h(CLK-DE)}$ | Input hold time, control valid from VIN[x]B_CLK high | 0 (2) | | ns |
| | $t_{h(CLK-VSYNC)}$ | | | | |
| | $t_{h(CLK-FLD)}$ | | | | |
| | $t_{h(CLK-HSYNC)}$ | | | | |
| | $t_{h(CLK-D)}$ | Input hold time, data valid from VIN[x]B_CLK high | 0 (2) | | |

(1) For maximum frequency of 165 MHz.
(2) When interfacing to a device with a minimum delay time of 0 ns, propagation delay of the data traces must be bigger than that of the clock traces.

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### Table 9-72. Switching Characteristics Over Recommended Operating Conditions for HDVPSS Output

(see Figure 9-68 and Figure 9-70)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLK)}$ | Cycle time, VOUT[x]_CLK | 6.06(1) | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse duration, VOUT[x]_CLK high (45% of $t_c$) | 2.73 | | ns |
| 3 | $t_{w(CLKL)}$ | Pulse duration, VOUT[x]_CLK low (45% of $t_c$) | 2.73 | | ns |
| 7 | $t_{t(CLK)}$ | Transition time, VOUT[x]_CLK (10%-90%) | | 2.64 | ns |
| 6 | $t_{d(CLK-AVID)}$ | Delay time, VOUT[x]_CLK to control valid | 1.64(2) | 4.85(3) | ns |
| | $t_{d(CLK-FLD)}$ | | | | |
| | $t_{d(CLK-VSYNC)}$ | | | | |
| | $t_{d(CLK-HSYNC)}$ | | | | |
| | $t_{d(CLK-RCR)}$ | Delay time, VOUT[0]_CLK to data valid | 1.64(2) | 4.85(3) | ns |
| | $t_{d(CLK-GYYC)}$ | | | | |
| | $t_{d(CLK-BCBC)}$ | | | | |
| | $t_{d(CLK-YYC)}$ | Delay time, VOUT[1]_CLK to data valid | | | |
| | $t_{d(CLK-C)}$ | | | | |

(1) For maximum frequency of 165 MHz.
(2) Min Delay Time = $T_c$ * 0.27, where $T_c$ is the clock cycle time. **Note:** When interfacing to devices where setup and hold margins are minimal, care must be taken to match board trace length delay for clock and data signals.
(3) Max Delay Time = $T_c$ * 0.80, where $T_c$ is the clock cycle time. **Note:** When interfacing to devices where setup and hold margins are minimal, care must be taken to match board trace length delay for clock and data signals.

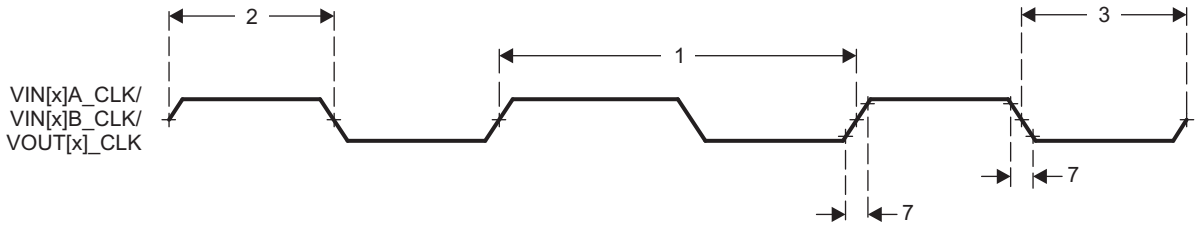


**Figure 9-68. HDVPSS Clock Timing**


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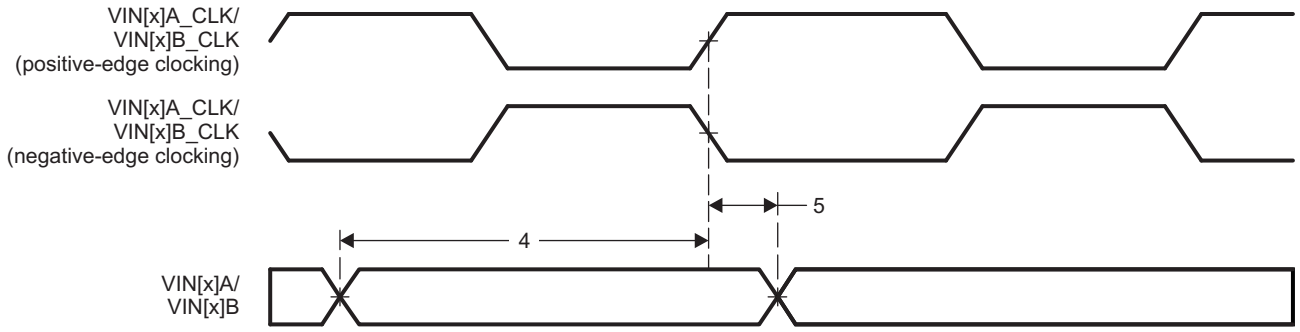


**Figure 9-69. HDVPSS Input Timing**

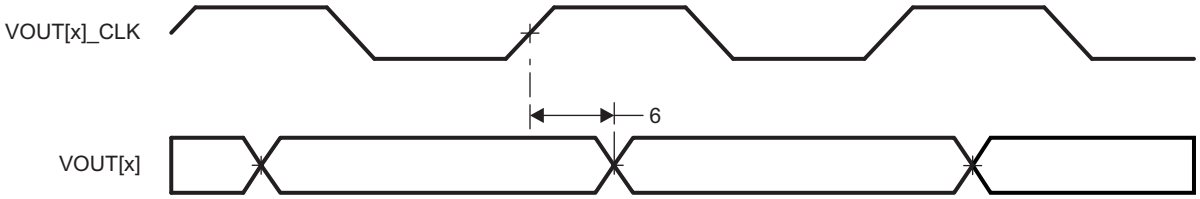


**Figure 9-70. HDVPSS Output Timing**

### 9.10.2 Video DAC Guidelines and Electrical Data and Timing

The device's analog video DAC outputs are designed to drive a 37.5-Ω load. Figure 9-71 describes a typical circuit that permits connecting the analog video output from the device to standard 75-Ω impedance video systems. The device requires the use of a buffer to drive the actual video outputs, so one solution is to use a video amplifier with integrated buffer and internal filter, such as the Texas Instruments THS7360, which provides a complete solution for the typical output circuit shown in Figure 9-71.

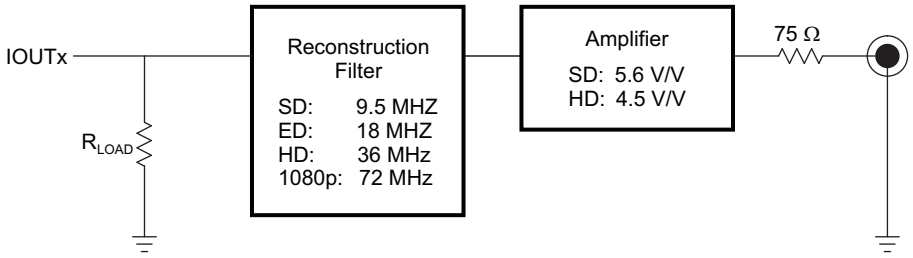


**Figure 9-71. Typical Output Circuits for Analog Video from DACs**

During board design, the onboard traces and parasitics must be matched for the channel. The video DAC output pin (IOUTx) is a very high-frequency analog signal and must be routed with extreme care. As a result, the path of this signal must be as short as possible, and as isolated as possible from other interfering signals. The load resistor and amplifier or buffer should be placed close together and as close as possible to the device pins. Other layout guidelines include:

- Take special care to bypass the DAC power supply pin with a capacitor.
- Place the 75-Ω resistor as close as possible (<0.5") to the amplifier or buffer (THS7360) output pin.
- To maintain a high quality video signal, 75-Ω (±10%) characteristic impedance traces should be used after the 75-Ω series resistor.
- Minimize input trace lengths to the device to reduce parasitic capacitance.
- Include solid ground return paths.
- Match trace lengths as close as possible within a video format group (that is, Y, Pb, and Pr for component output, and Y and C for s-video output should match each other).

For additional video DAC design guidelines, see the HDVPSS chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

**Table 9-73. DAC Specifications**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | HD DACs | | 12 | | Bits |
| | SD DACs | | 10 | | Bits |
| DC Accuracy - HD DACs | | | | | |
| Integral Non-Linearity (INL), best fit | HD DACs | | | 1.5 | LSB |
| | SD DACs | | | 1.0 | LSB |
| Differential Non-Linearity (DNL) | HD DACs | | | 1.0 | LSB |
| | SD DACs | | | 0.5 | LSB |
| Analog Output | | | | | |
| Output Resistor ($R_{LOAD}$) | HD and SD DACs | -1% | 37.5 | +1% | Ω |
| Full-Scale Output Current (IFS) | HD and SD DACs $R_{LOAD}$ | | 13.3 | | mA |
| Output Compliance Range | HD and SD DACs IFS = 13.3 mA, $R_{LOAD}$ = 37.5 Ω | 0 | | Vref | V |
| Zero Scale Offset Error (ZSET) | HD and SD DACs | | 0.5 | | LSB |
| Gain Error | HD and SD DACs | -10 | | 10 | % |


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**Table 9-73. DAC Specifications (continued)**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Channel matching | HD and SD DACs | | | 2 | % |
| Recommended External Amplification | HD DACs | | 4.5 | | V/V |
| | SD DACs | | 5.6 | | V/V |
| Reference | | | | | |
| Reference Voltage Range (VREF) | Input with External Reference | -5% | 0.5 | +5% | V |
| Full-Scale Current Adjust Resistors | $R_{BIAS_HD}$ and $R_{BIAS_SD}$ | -1% | 1.2 | +1% | kΩ |
| Dynamic Specifications | | | | | |
| Output Update Rate (FCLK) | HD DACs at 1080i60 | | 74.25 | | MHz |
| | HD DACs at 1080p60 | | 148.5 | | MHz |
| | SD DACs | | 27 | 54 | MHz |
| Signal Bandwidth | HD DACs at 1080i60 | | 30 | | MHz |
| | HD DACs at 1080p60 | | 60 | | MHz |
| | SD DACs | | 6 | | MHz |
| Spurious - Free Dynamic Range (SFDR) | HD DACs at 1080i60 FCLK = 74.25 MHz, FOUT = 30 MHz | | 60 | | dB |
| | HD DACs at 1080p60 FCLK = 148.5 MHz, FOUT = 60 MHz | | 60 | | dB |
| | SD DACs FCLK = 27 MHz / 54 MHz, FOUT = 6 MHz | | 60 | | dB |

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## 9.11 Inter-Integrated Circuit (I2C)

The device includes two inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit or receive 8-bit data to or from the device through the I2C module. The I2C port *does not* support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Standard and fast modes from 10 - 400 Kbps (no fail-safe IO buffers)
- Noise filter to remove noise 50 ns or less
- Seven- and ten-bit device addressing modes
- Multimaster transmitter or slave receiver mode
- Multimaster receiver or slave transmitter mode
- Combined master transmit/receive and receive or transmit modes
- Two DMA channels, one interrupt line
- Built-in FIFO (32 byte) for buffered read or write.

For more detailed information on the I2C peripheral, see the I2C chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### 9.11.1 I2C Peripheral Register Descriptions

**Table 9-74. I2C Registers**

| I2C0 HEX ADDRESS | I2C1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4802 8000 | 0x4802 A000 | I2C_REVNB_LO | Module Revision (LOW BYTES) |
| 0x4802 8004 | 0x4802 A004 | I2C_REVNB_HI | Module Revision (HIGH BYTES) |
| 0x4802 8010 | 0x4802 A010 | I2C_SYSC | System configuration |
| 0x4802 8020 | 0x4802 A020 | I2C_EOI | I2C End of Interrupt |
| 0x4802 8024 | 0x4802 A024 | I2C_IRQSTATUS_RAW | I2C Status Raw |
| 0x4802 8028 | 0x4802 A028 | I2C_IRQSTATUS | I2C Status |
| 0x4802 802C | 0x4802 A02C | I2C_IRQENABLE_SET | I2C Interrupt Enable Set |
| 0x4802 8030 | 0x4802 A030 | I2C_IRQENABLE_CLR | I2C Interrupt Enable Clear |
| 0x4802 8034 | 0x4802 A034 | I2C_WE | I2C Wakeup Enable |
| 0x4802 8038 | 0x4802 A038 | I2C_DMARXENABLE_SET | Receive DMA Enable Set |
| 0x4802 803C | 0x4802 A03C | I2C_DMATXENABLE_SET | Transmit DMA Enable Set |
| 0x4802 8040 | 0x4802 A040 | I2C_DMARXENABLE_CLR | Receive DMA Enable Clear |
| 0x4802 8044 | 0x4802 A044 | I2C_DMATXENABLE_CLR | Transmit DMA Enable Clear |
| 0x4802 8048 | 0x4802 A048 | I2C_DMARXWAKE_EN | Receive DMA Wakeup |
| 0x4802 804C | 0x4802 A04C | I2C_DMATXWAKE_EN | Transmit DMA Wakeup |
| 0x4802 8090 | 0x4802 A090 | I2C_SYSS | System Status |
| 0x4802 8094 | 0x4802 A094 | I2C_BUF | Buffer Configuration |
| 0x4802 8098 | 0x4802 A098 | I2C_CNT | Data Counter |
| 0x4802 809C | 0x4802 A09C | I2C_DATA | Data Access |
| 0x4802 80A4 | 0x4802 A0A4 | I2C_CON | I2C Configuration |
| 0x4802 80A8 | 0x4802 A0A8 | I2C_OA | I2C Own Address |
| 0x4802 80AC | 0x4802 A0AC | I2C_SA | I2C Slave Address |
| 0x4802 80B0 | 0x4802 A0B0 | I2C_PSC | I2C Clock Prescaler |
| 0x4802 80B4 | 0x4802 A0B4 | I2C_SCLL | I2C SCL Low Time |
| 0x4802 80B8 | 0x4802 A0B8 | I2C_SCLH | I2C SCL High Time |
| 0x4802 80BC | 0x4802 A0BC | I2C_SYSTEST | System Test |


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**Table 9-74. I2C Registers (continued)**

| I2C0 HEX ADDRESS | I2C1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4802 80C0 | 0x4802 A0C0 | I2C_BUFSTAT | I2C Buffer Status |
| 0x4802 80C4 | 0x4802 A0C4 | I2C_OA1 | I2C Own Address 1 |
| 0x4802 80C8 | 0x4802 A0C8 | I2C_OA2 | I2C Own Address 2 |
| 0x4802 80CC | 0x4802 A0CC | I2C_OA3 | I2C Own Address 3 |
| 0x4802 80D0 | 0x4802 A0D0 | I2C_ACTOA | Active Own Address |
| 0x4802 80D4 | 0x4802 A0D4 | I2C_SBLOCK | I2C Clock Blocking Enable |

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### 9.11.2 I2C Electrical Data and Timing

**Table 9-75. Timing Requirements for I2C Input**

(see Figure 9-72)

| NO. | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SCL)}$ | Cycle time, SCL | Standard_IC | 10 | | µs |
| | | | Fast_IC | 2.5 | | |
| 2 | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated Start condition) | Standard_IC | 4.7 | | µs |
| | | | Fast_IC | 0.6 | | |
| 3 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a Start and a repeated Start condition) | Standard_IC | 4 | | µs |
| | | | Fast_IC | 0.6 | | |
| 4 | $t_{w(SCLL)}$ | Pulse duration, SCL low | Standard_IC | 4.7 | | µs |
| | | | Fast_IC | 1.3 | | |
| 5 | $t_{w(SCLH)}$ | Pulse duration, SCL high | Standard_IC | 4 | | µs |
| | | | Fast_IC | 0.6 | | |
| 6 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | Standard_IC | 250 | | ns |
| | | | Fast_IC | 100 | | |
| 7 | $t_{h(SCLL-SDA)}$ | Hold time, SDA valid after SCL low (for I2C bus devices) | Standard_IC | 0 | 3.45 | µs |
| | | | Fast_IC | 0 | 0.9 | |
| 8 | $t_{w(SDAH)}$ | Pulse duration, SDA high between Stop and Start conditions | Standard_IC | 4.7 | | µs |
| | | | Fast_IC | 1.3 | | |
| 13 | $t_{su(SCLH-SDAH)}$ | Setup time, high before SDA high (for Stop condition) | Standard_IC | 4 | | µs |
| | | | Fast_IC | 0.6 | | |
| 14 | $t_{w(SDA)}$ | Pulse duration, spike (must be suppressed) | Fast_IC | 0 | 50 | ns |
| | $t_{w(SCL)}$ | | Fast_IC | 0 | 50 | |

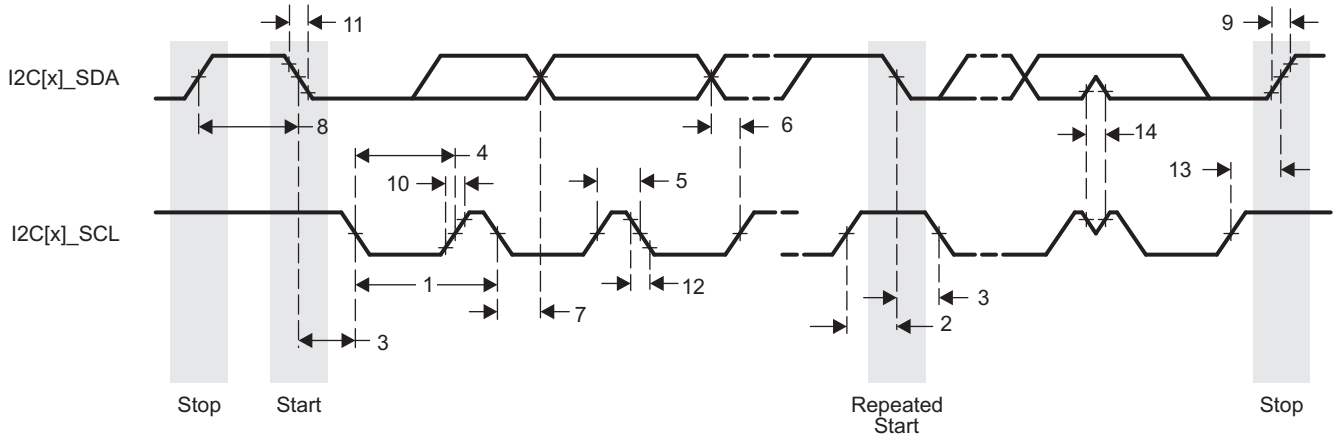


**Figure 9-72. I2C Receive Timing**


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**Table 9-76. Switching Characteristics Over Recommended Operating Conditions for I2C Output**

(see Figure 9-73)

| NO. | PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 16 | $t_{c(SCL)}$ | Cycle time, SCL | Standard_OC | 10 | | µs |
| | | | Fast_OC | 2.5 | | |
| 17 | $t_{su(SCLH-SDAL)}$ | Setup Time, SCL high before SDA low (for a repeated START condition) | Standard_OC | 4.7 | | µs |
| | | | Fast_OC | 0.6 | | |
| 18 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition | Standard_OC | 4 | | µs |
| | | | Fast_OC | 0.6 | | |
| 19 | $t_{w(SCLL)}$ | Pulse duration, SCL low | Standard_OC | 4.7 | | µs |
| | | | Fast_OC | 1.3 | | |
| 20 | $t_{w(SCLH)}$ | Pulse duration, SCL high | Standard_OC | 4 | | µs |
| | | | Fast_OC | 0.6 | | |
| 21 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | Standard_OC | 250 | | ns |
| | | | Fast_OC | 100 | | |
| 22 | $t_{h(SCLL-SDA)}$ | Hold time, SDA valid after SCL low (For IIC bus devices) | Standard_OC | 0 | 3.45 | µs |
| | | | Fast_OC | 0 | 0.9 | |
| 23 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | Standard_OC | 4.7 | | µs |
| | | | Fast_OC | 1.3 | | |
| 28 | $t_{su(SCLH-SDAH)}$ | Setup time, high before SDA high (for STOP condition) | Standard_OC | 4 | | µs |
| | | | Fast_OC | 0.6 | | |

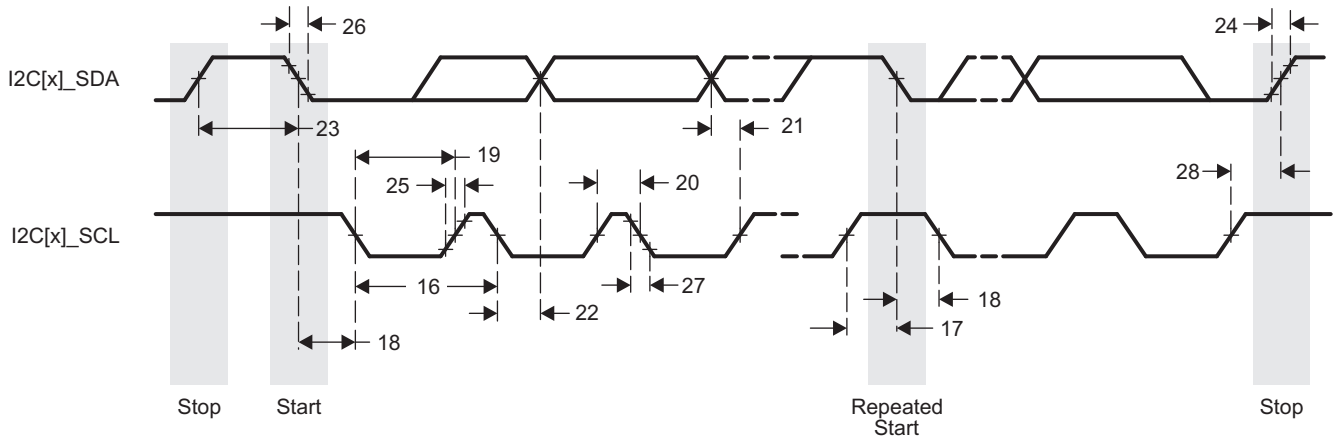


**Figure 9-73. I2C Transmit Timing**

## 9.12 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT).

### *9.12.1 McASP Device-Specific Information*

The device includes three multichannel audio serial port (McASP) interface peripherals (McASP0, McASP1, and McASP2). The McASP module consists of a transmit and receive section. These sections can operate completely independently with different data formats, separate master clocks, bit clocks, and frame syncs or, alternatively, the transmit and receive sections may be synchronized. The McASP module also includes shift registers that may be configured to operate as either transmit data or receive data. The transmit section of the McASP can transmit data in either a time-division-multiplexed (TDM) synchronous serial format or in a digital audio interface (DIT) format where the bit stream is encoded for SPDIF, AES-3, IEC-60958, CP-430 transmission. The receive section of the McASP peripheral supports the TDM synchronous serial format.

The McASP module can support one transmit data format (either a TDM format or DIT format) and one receive format at a time. All transmit shift registers use the same format and all receive shift registers use the same format; however, the transmit and receive formats need not be the same. Both the transmit and receive sections of the McASP also support burst mode, which is useful for non-audio data (for example, passing control information between two devices).

The McASP peripheral has additional capability for flexible clock generation and error detection and handling, as well as error management.

The device McASP0 module has six serial data pins, while McASP1 and McASP2 are limited to two serial data pins each.

The McASP FIFO size is 256 bytes and two DMA and two interrupt requests are supported. Buffers are used transparently to better manage DMA, which can be leveraged to manage data flow more efficiently.

For more detailed information on and the functionality of the McASP peripheral, see the McASP chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).


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### 9.12.2 McASP0, McASP1, and McASP2 Peripheral Register Descriptions

**Table 9-77. McASP0, McASP1, and McASP2 Registers**

| MCASP0 ADDRESS | MCASP1 ADDRESS | MCASP2 ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|
| 0x4803 8000 | 0x4803 C000 | 0x4805 0000 | PID | Peripheral ID |
| 0x4803 8004 | 0x4803 C004 | 0x4805 0004 | PWRIDLE SYSCONFIG | Power Idle SYSCONFIG |
| 0x4803 8010 | 0x4803 C010 | 0x4805 0010 | PFUNC | Pin Function |
| 0x4803 8014 | 0x4803 C014 | 0x4805 0014 | PDIR | Pin Direction |
| 0x4803 8018 | 0x4803 C018 | 0x4805 0018 | PDOUT | Pin Data Out |
| 0x4803 801C | 0x4803 C01C | 0x4805 001C | PDIN | Pin Data Input (Read)<br>Read returns pin data input |
| | | | PDSET | Pin Data Set (Write)<br>Writes effect pin data set (alternate write address PDOUT) |
| 0x4803 8020 | 0x4803 C020 | 0x4805 0020 | PDCLR | Pin Data Clear |
| 0x4803 8044 | 0x4803 C044 | 0x4805 0044 | GBLCTL | Global Control |
| 0x4803 8048 | 0x4803 C048 | 0x4805 0048 | AMUTE | Mute Control |
| 0x4803 804C | 0x4803 C04C | 0x4805 004C | LBCTL | Loop-Back Test Control |
| 0x4803 8050 | 0x4803 C050 | 0x4805 0050 | TXDITCTL | Transmit DIT Mode Control |
| 0x4803 8060 | 0x4803 C060 | 0x4805 0060 | GBLCTLR | Alias of GBLCTL containing only receiver reset bits; allows transmit to be reset independently from receive |
| 0x4803 8064 | 0x4803 C064 | 0x4805 0064 | RXMASK | Receiver Bit Mask |
| 0x4803 8068 | 0x4803 C068 | 0x4805 0068 | RXFMT | Receive Bitstream Format |
| 0x4803 806C | 0x4803 C06C | 0x4805 006C | RXFMCTL | Receive Frame Sync Control |
| 0x4803 8070 | 0x4803 C070 | 0x4805 0070 | ACLKRCTL | Receive Clock Control |
| 0x4803 8074 | 0x4803 C074 | 0x4805 0074 | AHCLKRCTL | High Frequency Receive Clock Control |
| 0x4803 8078 | 0x4803 C078 | 0x4805 0078 | RXTDM | Receive TDM Slot 0-31 |
| 0x4803 807C | 0x4803 C07C | 0x4805 007C | EVTCTLR | Receiver Interrupt Control |
| 0x4803 8080 | 0x4803 C080 | 0x4805 0080 | RXSTAT | Status Receiver |
| 0x4803 8084 | 0x4803 C084 | 0x4805 0084 | RXTDMSLOT | Current Receive TDM Slot |
| 0x4803 8088 | 0x4803 C088 | 0x4805 0088 | RXCLKCHK | Receiver Clock Check Control |
| 0x4803 808C | 0x4803 C08C | 0x4805 008C | REVTCTL | Receiver DMA Event Control |
| 0x4803 80A0 | 0x4803 C0A0 | 0x4805 00A0 | GBLCTLX | Alias of GBLCTL containing only transmit reset bits; allows transmit to be reset independently from receive |
| 0x4803 80A4 | 0x4803 C0A4 | 0x4805 00A4 | TXMASK | Transmit Format Unit Bit Mask |
| 0x4803 80A8 | 0x4803 C0A8 | 0x4805 00A8 | TXFMT | Transmit Bitstream Format |
| 0x4803 80AC | 0x4803 C0AC | 0x4805 00AC | TXFMCTL | Transmit Frame Sync Control |
| 0x4803 80B0 | 0x4803 C0B0 | 0x4805 00B0 | ACLKXCTL | Transmit Clock Control |
| 0x4803 80B4 | 0x4803 C0B4 | 0x4805 00B4 | AHCLKXCTL | High Frequency Transmit Clock Control |
| 0x4803 80B8 | 0x4803 C0B8 | 0x4805 00B8 | TXTDM | Transmit TDM Slot 0-31 |
| 0x4803 80BC | 0x4803 C0BC | 0x4805 00BC | EVTCTLX | Transmitter Interrupt Control |
| 0x4803 80C0 | 0x4803 C0C0 | 0x4805 00C0 | TXSTAT | Status Transmitter |

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**Table 9-77. McASP0, McASP1, and McASP2 Registers (continued)**

| MCASP0 ADDRESS | MCASP1 ADDRESS | MCASP2 ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|
| 0x4803 80C4 | 0x4803 C0C4 | 0x4805 00C4 | TXTDMSLOT | Current Transmit TDM Slot |
| 0x4803 80C8 | 0x4803 C0C8 | 0x4805 00C8 | TXCLKCHK | Transmit Clock Check Control |
| 0x4803 80CC | 0x4803 C0CC | 0x4805 00CC | XEVTCTL | Transmitter DMA Control |
| 0x4803 80D0 | 0x4803 C0D0 | 0x4805 00D0 | CLKADJEN | One-shot Clock Adjust Enable |
| 0x4803 8100 | 0x4803 C100 | 0x4805 0100 | DITCSRA0 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8104 | 0x4803 C104 | 0x4805 0104 | DITCSRA1 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8108 | 0x4803 C108 | 0x4805 0108 | DITCSRA2 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 810C | 0x4803 C10C | 0x4805 010C | DITCSRA3 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8110 | 0x4803 C110 | 0x4805 0110 | DITCSRA4 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8114 | 0x4803 C114 | 0x4805 0114 | DITCSRA5 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8118 | 0x4803 C118 | 0x4805 0118 | DITCSRB0 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 811C | 0x4803 C11C | 0x4805 011C | DITCSRB1 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 8120 | 0x4803 C120 | 0x4805 0120 | DITCSRB2 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 8124 | 0x4803 C124 | 0x4805 0124 | DITCSRB3 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 8128 | 0x4803 C128 | 0x4805 0128 | DITCSRB4 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 812C | 0x4803 C12C | 0x4805 012C | DITCSRB5 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 8130 | 0x4803 C130 | 0x4805 0130 | DITUDRA0 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8134 | 0x4803 C134 | 0x4805 0134 | DITUDRA1 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8138 | 0x4803 C138 | 0x4805 0138 | DITUDRA2 | Left (Even TDM Slot) User Data Register File |
| 0x4803 813C | 0x4803 C13C | 0x4805 013C | DITUDRA3 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8140 | 0x4803 C140 | 0x4805 0140 | DITUDRA4 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8144 | 0x4803 C144 | 0x4805 0144 | DITUDRA5 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8148 | 0x4803 C148 | 0x4805 0148 | DITUDRB0 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 814C | 0x4803 C14C | 0x4805 014C | DITUDRB1 | Right (Odd TDM Slot) User Data Register File |


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**Table 9-77. McASP0, McASP1, and McASP2 Registers (continued)**

| MCASP0 ADDRESS | MCASP1 ADDRESS | MCASP2 ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|
| 0x4803 8150 | 0x4803 C150 | 0x4805 0150 | DITUDRB2 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 8154 | 0x4803 C154 | 0x4805 0154 | DITUDRB3 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 8158 | 0x4803 C158 | 0x4805 0158 | DITUDRB4 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 815C | 0x4803 C15C | 0x4805 015C | DITUDRB5 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 8180 - 0x4803 81BC | 0x4803 C180 - 0x4803 C1BC | 0x4805 0180 - 0x4805 01BC | XRSRCTL0 - XRSRCTL15 | Serializer 0 Control - Serializer 15 Control |
| 0x4803 8200 - 0x4803 8 23C | 0x4803 C200 - 0x4803 C23C | 0x4805 0200 - 0x4805 023C | TXBUF0 - TXBUF15 | Transmit Buffer for Serializer 0 - Transmit Buffer for Serializer 15 |
| 0x4803 8280 - 0x4803 82BC | 0x4803 C280 - 0x4803 C2BC | 0x4805 0280 - 0x4805 02BC | RXBUF0 - RXBUF15 | Receive Buffer for Serializer 0 - Receive Buffer for Serializer 15 |
| 0x4803 9000 | 0x4803 D000 | 0x4805 1000 | BUFFER_CFGRD_WFIFOCTL | Write FIFO Control |
| 0x4803 9004 | 0x4803 D004 | 0x4805 1004 | BUFFER_CFGRD_WFIFOSTS | Write FIFO Status |
| 0x4803 9008 | 0x4803 D008 | 0x4805 1008 | BUFFER_CFGRD_RFIFOCTL | Read FIFO Control |
| 0x4803 900C | 0x4803 D00C | 0x4805 100C | BUFFER_CFGRD_RFIFOSTS | Read FIFO Status |

**Table 9-78. McASP Registers Accessed Through DAT Port**

| HEX ADDRESS | REGISTER NAME | McASP0 BYTE ADDRESS | McASP0 BYTE ADDRESS | McASP0 BYTE ADDRESS | REGISTER DESCRIPTION |
|---|---|---|---|---|---|
| Read Accesses | RBUF | 4600 0000 | 4640 0000 | 4680 0000 | Receive buffer DMA port address. Cycles through receive serializers, skipping over transmit serializers and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Reads from DMA port only if XBUSEL = 0 in XFMT. |
| Write Accesses | XBUF | 4600 0000 | 4640 0000 | 4680 0000 | Transmit buffer DMA port address. Cycles through transmit serializers, skipping over receive and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Writes to DMA port only if RBUSEL = 0 in RFMT. |

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### 9.12.3 McASP Electrical Data and Timing

**Table 9-79. Timing Requirements for McASP(1)**

(see Figure 9-74)

| NO. | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, MCA[x]_AHCLKR or MCA[x]_AHCLKX | | 20 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, MCA[x]_AHCLKR or MCA[x]_AHCLKX high or low | | 10 | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, MCA[x]_ACLKR or MCA[x]_AHCLKX | | 20 | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, MCA[x]_ACLKR or MCA[x]_AHCLKX high or low | | 10 | | ns |
| 5 | $t_{su(AFSRX-ACLKRX)}$ | Setup time, MCA[x]_AFSR or MCA[x]_AFSX input valid before MCA[x]_ACLKR or MCA[x]_ACLKX | ACLKR or ACLKX int | 11.5 | | ns |
| | | | ACLKR or ACLKX ext in | 4 | | |
| | | | ACLKR or ACLKX ext out | 4 | | |
| 6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, MCA[x]_AFSR or MCA[x]_AFSX input valid after MCA[x]_ACLKR or MCA[x]_ACLKX | ACLKR or ACLKX int | -1 | | ns |
| | | | ACLKR or ACLKX ext in | 0.5 | | |
| | | | ACLKR or ACLKX ext out | 0.5 | | |
| 7 | $t_{su(AXR-ACLKRX)}$ | Setup time, MCA[x]_AXR input valid before MCA[x]_ACLKR or MCA[x]_ACLKX | ACLKR or ACLKX int | 11.5 | | ns |
| | | | ACLKR or ACLKX ext in | 4 | | |
| | | | ACLKR or ACLKX ext out | 4 | | |
| 8 | $t_{h(ACLKRX-AXR)}$ | Hold time, MCA[x]_AXR input valid after MCA[x]_ACLKR or MCA[x]_ACLKX | ACLKR or ACLKX int | -1 | | ns |
| | | | ACLKR or ACLKX ext in | 0.5 | | |
| | | | ACLKR or ACLKX ext out | 0.5 | | |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1


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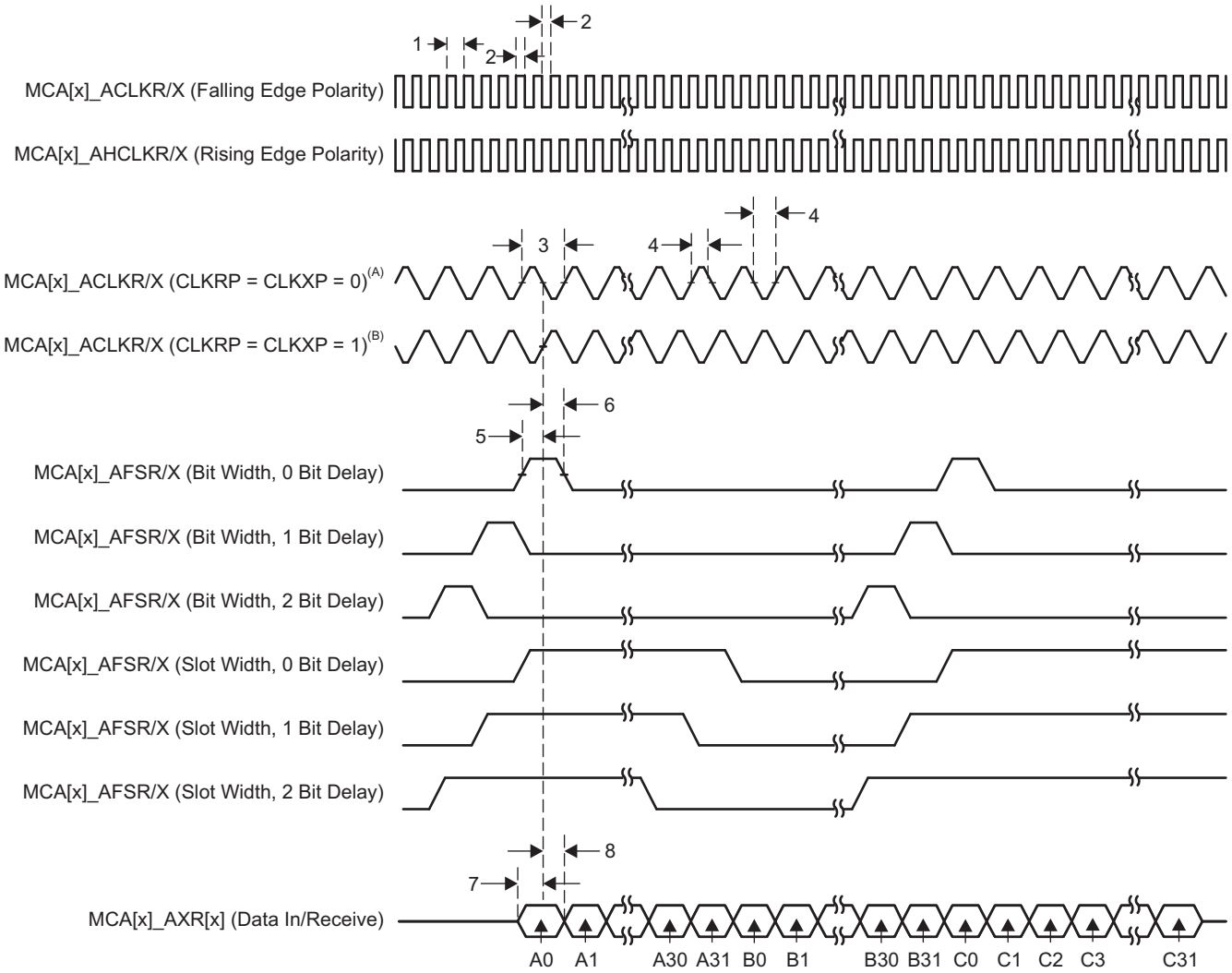


A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

**Figure 9-74. McASP Input Timing**

### Table 9-80. Switching Characteristics Over Recommended Operating Conditions for McASP[1]

(see Figure 9-75)

| NO. | PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, MCA[x]_AHCLKR/X | | 20[2] | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, MCA[x]_AHCLKR/X high or low | | 0.5P - 2.5[3] | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, MCA[x]_ACLKR or ACLKX | | 20 | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, MCA[x]_ACLKR or ACLKX high or low | | 0.5P - 2.5[3] | | ns |
| 13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, MCA[x]_ACLKR or ACLKX transmit edge to MCA[x]_AFSR/X output valid | ACLKR or ACLKX int | 0 | 6 | ns |
| | | | ACLKR or ACLKX ext in | 2 | 13.5 | |
| | | Delay time, MCA[x]_ACLKR or ACLKX transmit edge to MCA[x]_AFSR/X output valid with Pad Loopback | ACLKR or ACLKX ext out | 2 | 13.5 | |
| 14 | $t_{d(ACLKX-AXR)}$ | Delay time, MCA[x]_ACLKX transmit edge to MCA[x]_AXR output valid | ACLKX int | -1 | 5 | ns |
| | | | ACLKX ext in | 2 | 13.5 | |
| | | Delay time, MCA[x]_ACLKX transmit edge to MCA[x]_AXR output valid with Pad Loopback | ACLKX ext out | 2 | 13.5 | |
| 15 | $t_{dis(ACLKX-AXR)}$ | Disable time, MCA[x]_ACLKX transmit edge to MCA[x]_AXR output high impedance | ACLKX int | -1 | 5 | ns |
| | | | ACLKX ext in | 2 | 13.5 | |
| | | Disable time, MCA[x]_ACLKX transmit edge to MCA[x]_AXR output high impedance with Pad Loopback | ACLKX ext out | 2 | 13.5 | |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) 50 MHz
(3) P = AHCLKR or AHCLKX period.


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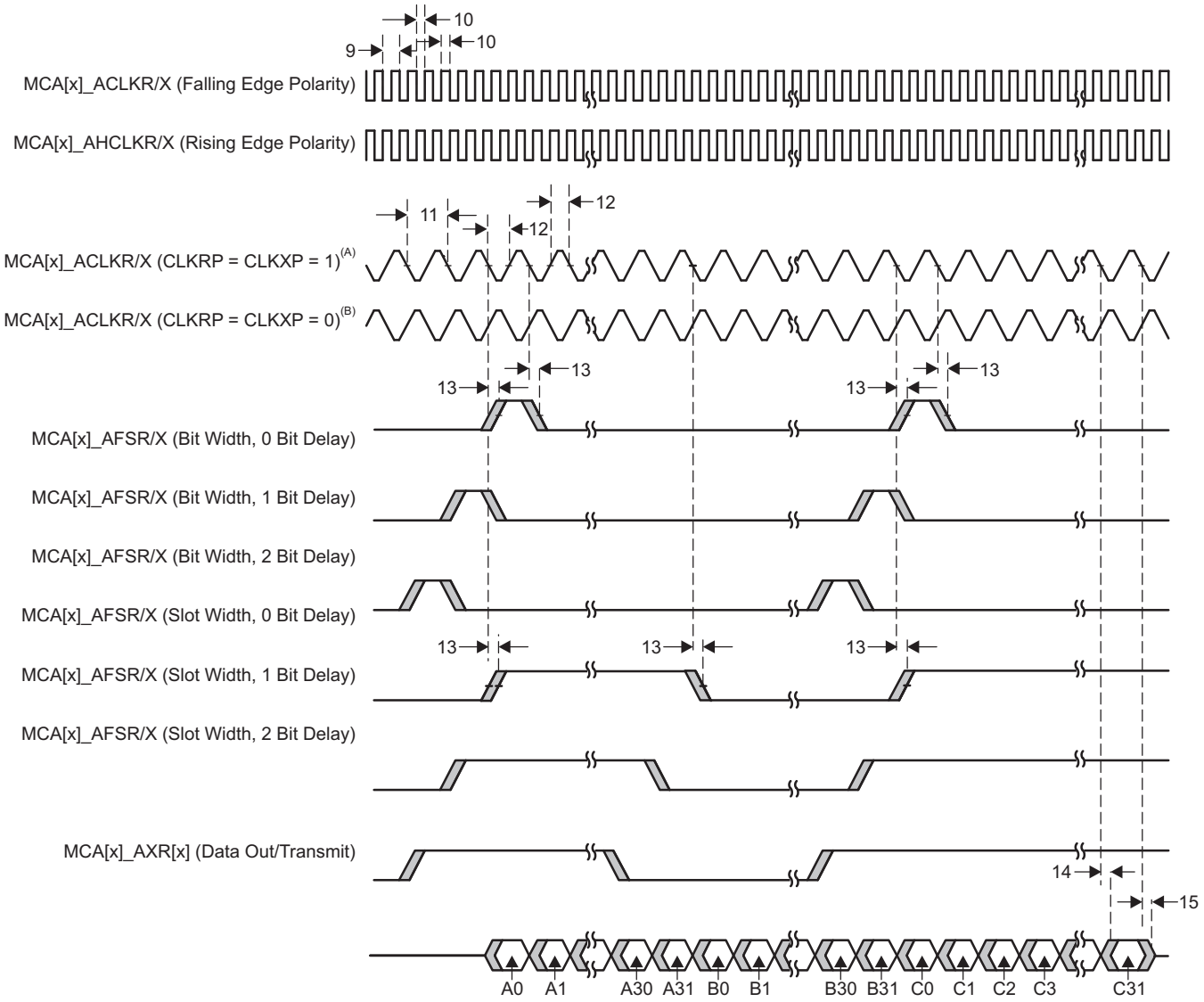


A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

**Figure 9-75. McASP Output Timing**

## 9.13 Multichannel Buffered Serial Port (McBSP)

The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (AD) and digital-to-analog (DA) devices
- Supports TDM, I2S, and similar formats
- External shift clock or an internal, programmable frequency shift clock for data transfer
- 5KB Tx and Rx buffer
- Supports three interrupt and two DMA requests.

The McBSP module may support two types of data transfer at the system level:

- The full-cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later).
- The half-cycle mode, for which one half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one half clock period later). Note that a new data is generated only every clock period, which secures the required hold time. The interface clock (CLKX or CLKR) activation edge (data or frame sync capture and generation) has to be configured accordingly with the external peripheral (activation edge capability) and the type of data transfer required at the system level.

For more detailed information on the McBSP peripheral, see the McBSP chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

The following sections describe the timing characteristics for applications in normal mode (that is, the McBSP connected to one peripheral) and TDM applications in multipoint mode.

### *9.13.1 McBSP Peripheral Registers*

This McBSP peripheral registers are described in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8). Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are shown in Table 3-26, *L3 Memory Map*.


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### 9.13.2 McBSP Electrical Data and Timing

**Table 9-81. Timing Requirements for McBSP - Master Mode(1)**

(see Figure 9-76)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 6 | $t_{su(DRV-CLKAE)}$ | Setup time, MCB_DR valid before MCB_CLK active edge(2) | 3.5 | | ns |
| 7 | $t_{h(CLKAE-DRV)}$ | Hold time, MCB_DR valid after MCB_CLK active edge(2) | 0.1 | | ns |

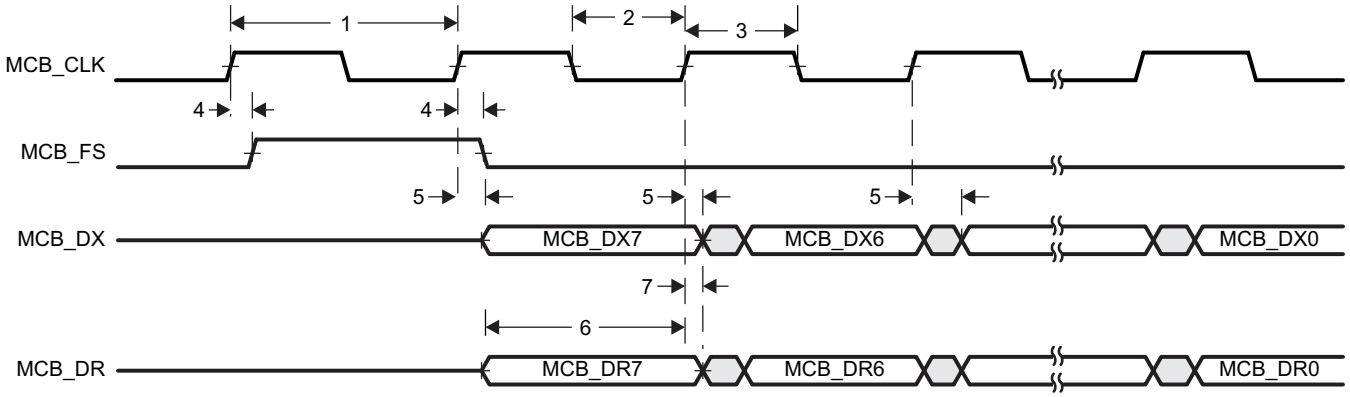
(1) The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) MCB_CLK corresponds to either MCB_CLKX or MCB_CLKR.

**Table 9-82. Switching Characteristics Over Recommended Operating Conditions for McBSP - Master Mode(1)**

(see Figure 9-76)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLK)}$ | Cycle time, output MCB_CLK period(2) | 20.83 | | ns |
| 2 | $t_{w(CLKL)}$ | Pulse duration, output MCB_CLK low(2) | 0.5*P - 1(3) | | ns |
| 3 | $t_{w(CLKH)}$ | Pulse duration, output MCB_CLK high(2) | 0.5*P - 1(3) | | ns |
| 4 | $t_{d(CLKAE-FSV)}$ | Delay time, output MCB_CLK active edge to output MCB_FS valid(2)(4) | 0.7 | 9.4 | ns |
| 5 | $t_{d(CLKXAE-DXV)}$ | Delay time, output MCB_CLKX active edge to output MCB_DX valid | 0.7 | 9.4 | ns |

(1) The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) MCB_CLK corresponds to either MCB_CLKX or MCB_CLKR.
(3) P = MCB_CLKX or MCB_CLKR output CLK period, in ns; use whichever value is greater. This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKX or CLKR) in the reasonable range of 40-60 duty cycle.
(4) MCB_FS corresponds to either MCB_FSX or MCB_FSR.




A. The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.
B. MCBSP_CLK corresponds to either MCBSP_CLKX or MCBSP_CLKR; MCBSP_FS corresponds to either MCBSP_FSX or MCBSP_FSR. McBSP in 6-pin mode: DX and DR as data pins; CLKX, CLKR, FSX and FSR as control pins. McBSP in 4-pin mode: DX and DR as data pins; CLKX and FSX pins as control pins. The CLKX and FSX pins are internally looped back via software configuration, respectively to the CLKR and FSR internal signals for data receive.
C. The polarity of McBSP frame synchronization is software configurable.
D. The active clock edge selection of MCBSP_CLK (rising or falling) on which MCBSP_DX data is latched and MCBSP_DR data is sampled is software configurable.
E. Timing diagrams are for data delay set to 1.
F. For further details about the registers used to configure McBSP, see the McBSP chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

**Figure 9-76. McBSP Master Mode Timing**

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### Table 9-83. Timing Requirements for McBSP - Slave Mode[1]

(see Figure 9-77)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLK)}$ | Cycle time, MCB_CLK period[2] | 20.83 | | ns |
| 2 | $t_{w(CLKL)}$ | Pulse duration, MCB_CLK low[2] | 0.5*P - 1[3] | | ns |
| 3 | $t_{w(CLKH)}$ | Pulse duration, MCB_CLK high[2] | 0.5*P - 1[3] | | ns |
| 4 | $t_{su(FSV-CLKAE)}$ | Setup time, MCB_FS valid before MCB_CLK active edge[2][4] | 3.8 | | ns |
| 5 | $t_{h(CLKAE-FSV)}$ | Hold time, MCB_FS valid after MCB_CLK active edge[2][4] | 0 | | ns |
| 7 | $t_{su(DRV-CLKAE)}$ | Setup time, MCB_DR valid before MCB_CLK active edge[2] | 3.8 | | ns |
| 8 | $t_{h(CLKAE-DRV)}$ | Hold time, MCB_DR valid after MCB_CLK active edge[2] | 0 | | ns |

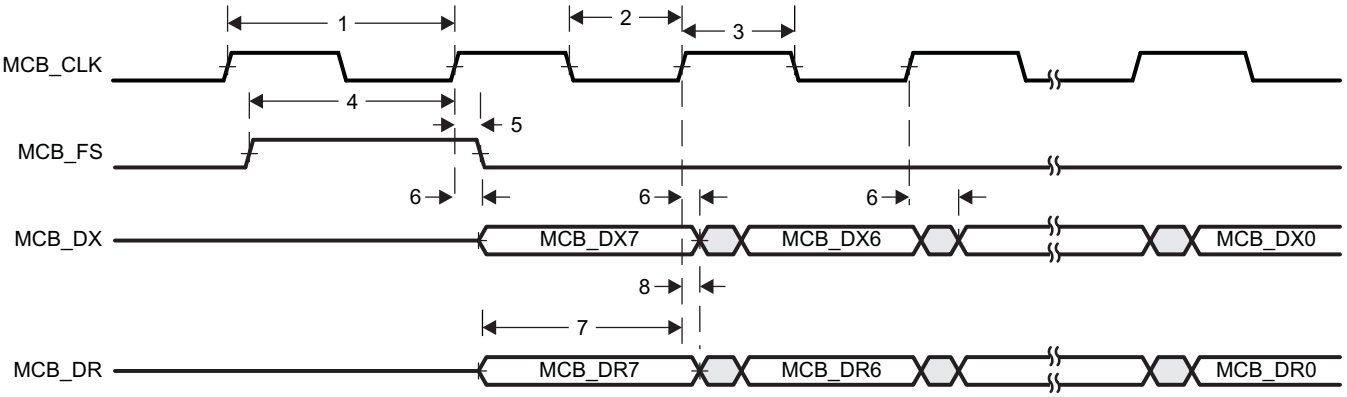
(1) The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) MCB_CLK corresponds to either MCB_CLKX or MCB_CLKR.
(3) P = MCB_CLKX or MCB_CLKR output CLK period, in ns; use whichever value is greater. This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKX or CLKR) in the reasonable range of 40-60 duty cycle.
(4) MCB_FS corresponds to either MCB_FSX or MCB_FSR.

### Table 9-84. Switching Characteristics Over Recommended Operating Conditions for McBSP - Slave Mode[1]

(see Figure 9-77)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 6 | $t_{d(CLKXAE-DXV)}$ | Delay time, input MCB_CLKx active edge to output MCB_DX valid | 0.5 | 12.5 | ns |

(1) The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.




A. The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.
B. MCBSP_CLK corresponds to either MCBSP_CLKX or MCBSP_CLKR; MCBSP_FS corresponds to either MCBSP_FSX or MCBSP_FSR. McBSP in 6-pin mode: DX and DR as data pins; CLKX, CLKR, FSX and FSR as control pins. McBSP in 4-pin mode: DX and DR as data pins; CLKX and FSX pins as control pins. The CLKX and FSX pins are internally looped back via software configuration, respectively to the CLKR and FSR internal signals for data receive.
C. The polarity of McBSP frame synchronization is software configurable.
D. The active clock edge selection of MCBSP_CLK (rising or falling) on which MCBSP_DX data is latched and MCBSP_DR data is sampled is software configurable.
E. Timing diagrams are for data delay set to 1.
F. For further details about the registers used to configure McBSP, see the McBSP chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

**Figure 9-77. McBSP Slave Mode Timing**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## 9.14 Peripheral Component Interconnect Express (PCIe)

The device supports connections to PCIe-compliant devices via the integrated PCIe master or slave bus interface. The PCIe module is comprised of a dual-mode PCIe core and a SerDes PHY. The device implements a single two-lane PCIe 2.0 (5.0 GT/s) endpoint or root complex port.

The device PCIe supports the following features:

- Supports Gen1 and Gen2 in x1 or x2 mode
- One port with up to 2 x 5 GT/s lanes
- Single virtual channel (VC), single traffic class (TC)
- Single function in end-point mode
- Automatic width and speed negotiation and lane reversal
- Max payload: 128 byte outbound, 256 byte inbound
- Automatic credit management
- ECRC generation and checking
- Configurable BAR filtering
- Supports PCIe messages
- Legacy interrupt reception (RC) and generation (EP)
- MSI generation and reception
- PCI device power management, except D3 cold with vaux
- Active state power management state L0 and L1.

For more detailed information on the PCIe port peripheral module, see the PCIe chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

The PCIe peripheral on the device conforms to the PCI Express Base 2.0 Specification.

### *9.14.1 PCIe Design and Layout Specifications*

**NOTE**

For more information on PCB layout, see the *DM816xx Easy CYG Package PCB Escape Routing* application report (literature number SPRABK6).

#### 9.14.1.1 Clock Source

A standard 100-MHz PCIe differential clock source must be used for PCIe operation (for details, see Section 8.3.2).

#### 9.14.1.2 PCIe Connections and Interface Compliance

The PCIe interface on the device is compliant with the PCI Express Base 2.0 Specification. Refer to the PCIe specifications for all connections that are described in it. For coupling capacitor selection, see Section 9.14.1.2.1.

The use of PCIe-compatible bridges and switches is allowed for interfacing with more than one other processor or PCIe device.

##### *9.14.1.2.1 Coupling Capacitors*

AC coupling capacitors are required on the transmit data pair. Table 9-85 shows the requirements for these capacitors.

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**Table 9-85. AC Coupling Capacitors Requirements**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCIe AC coupling capacitor value | 75 | | 200 | nF |
| PCIe AC coupling capacitor package size(1) | | 0402 | 0603 | EIA(2) |

(1) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair, placed side by side.
(2) EIA LxW units; for example, a 0402 is a 40x20 mil (thousandths of an inch) surface-mount capacitor.

#### *9.14.1.2.2 Polarity Inversion*

The PCIe specification requires polarity inversion support. This means, for layout purposes, polarity is unimportant since each signal can change its polarity on-die inside the chip. This means polarity within a lane is unimportant for layout.

#### *9.14.1.2.3 Lane Reversal*

The device supports lane reversal. Since there are two lanes, this means the lanes can be switched in layout for better PCB routing.

### 9.14.1.3 Non-Standard PCIe Connections

The following sections contain suggestions for any PCIe connection that is ***not*** described in the official PCIe specification, such as an on-board device-to-device connection, or device-to-other PCIe-compliant processor connection.

#### *9.14.1.3.1 PCB Stackup Specifications*

Table 9-86 shows the stackup and feature sizes required for these types of PCIe connections.

**Table 9-86. PCIe PCB Stackup Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCB Routing and Plane Layers | 4 | 6 | - | Layers |
| Signal Routing Layers | 2 | 3 | - | Layers |
| Number of ground plane cuts allowed within PCIe routing region | - | - | 0 | Cuts |
| Number of layers between PCIe routing area and reference plane(1) | - | - | 0 | Layers |
| PCB Routing clearance | - | 4 | - | Mils |
| PCB Trace width(2) | - | 4 | - | Mils |
| PCB BGA escape via pad size | - | 20 | - | Mils |
| PCB BGA escape via hole size | - | 10 | | Mils |
| Processor BGA pad size(3)(4) | | 0.3 | | mm |

(1) A reference plane may be a ground plane or the power plane referencing the PCIe signals.
(2) In breakout area.
(3) Non-solder mask defined pad.
(4) Per IPC-7351A BGA pad size guideline.

#### *9.14.1.3.2 Routing Specifications*

The PCIe data signal traces must be routed to achieve 100 Ω (±20%) differential impedance and 60 Ω (±15%) single-ended impedance. The single-ended impedance is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important. These requirements are the same as those recommended in the *PCIe Motherboard Checklist 1.0* document, available from PCI-SIG.

These impedances are impacted by trace width, trace spacing, distance between signals and referencing planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs result in as close to 100 Ω differential impedance and 60 Ω single-ended impedance as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.


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In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations do not affect impedance as much; therefore, it is easier to maintain an accurate impedance over the length of the signal. The wider traces also show reduced skin effect and, therefore, often result in better signal integrity.

Table 9-87 shows the routing specifications for the PCIe data signals.

**Table 9-87. PCIe Routing Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCIe signal trace length | | | 10 (1) | Inches |
| Differential pair trace matching | | | 10 (2) | Mils |
| Number of stubs allowed on PCIe traces (3) | | | 0 | Stubs |
| TX or RX pair differential impedance | 80 | 100 | 120 | Ω |
| TX or RX single-ended impedance | 51 | 60 | 69 | Ω |
| Pad size of vias on PCIe trace | | | 25 (4) | Mils |
| Hole size of vias on PCIe trace | | | 14 | Mils |
| Number of vias on each PCIe trace | | | 3 | Vias (5) |
| PCIe differential pair to any other trace spacing | 2*DS (6) | | | |

(1) Beyond this, signal integrity may suffer.
(2) For example, RXP0 within 10 Mils of RXN0.
(3) In-line pads may be used for probing.
(4) 35-Mil antipad max recommended.
(5) Vias must be used in pairs with their distance minimized.
(6) DS = differential spacing of the PCIe traces.

### 9.14.2 PCIe Peripheral Register Descriptions

**Table 9-88. PCIe Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5100 0000 | PID | Peripheral Version and ID |
| 0x5100 0004 | CMD_STATUS | Command Status |
| 0x5100 0008 | CFG_SETUP | Config Transaction Setup |
| 0x5100 000C | IOBASE | IO TLP Base |
| 0x5100 0010 | TLPCFG | TLP Attribute Configuration |
| 0x5100 0014 | RSTCMD | Reset Command and Status |
| 0x5100 0020 | PMCMD | Power Management Command |
| 0x5100 0024 | PMCFG | Power Management Configuration |
| 0x5100 0028 | ACT_STATUS | Activity Status |
| 0x5100 0030 | OB_SIZE | Outbound Size |
| 0x5100 0034 | DIAG_CTRL | Diagnostic Control |
| 0x5100 0038 | ENDIAN | Endian Mode |
| 0x5100 003C | PRIORITY | CBA Transaction Priority |
| 0x5100 0050 | IRQ_EOI | End of Interrupt |
| 0x5100 0054 | MSI_IRQ | MSI Interrupt IRQ |
| 0x5100 0064 | EP_IRQ_SET | Endpoint Interrupt Request Set |
| 0x5100 0068 | EP_IRQ_CLR | Endpoint Interrupt Request Clear |
| 0x5100 006C | EP_IRQ_STATUS | Endpoint Interrupt Status |
| 0x5100 0070 | GPRO | General Purpose 0 |

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**Table 9-88. PCIe Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5100 0074 | GPR1 | General Purpose 1 |
| 0x5100 0078 | GPR2 | General Purpose 2 |
| 0x5100 007C | GPR3 | General Purpose 3 |
| 0x5100 0100 | MSI0_IRQ_STATUS_RAW | MSI 0 Interrupt Raw Status |
| 0x5100 0104 | MSI0_IRQ_STATUS | MSI 0 Interrupt Enabled Status |
| 0x5100 0108 | MSI0_IRQ_ENABLE_SET | MSI 0 Interrupt Enable Set |
| 0x5100 010C | MSI0_IRQ_ENABLE_CLR | MSI 0 Interrupt Enable Clear |
| 0x5100 0180 | IRQ_STATUS_RAW | Raw Interrupt Status |
| 0x5100 0184 | IRQ_STATUS | Interrupt Enabled Status |
| 0x5100 0188 | IRQ_ENABLE_SET | Interrupt Enable Set |
| 0x5100 018C | IRQ_ENABLE_CLR | Interrupt Enable Clear |
| 0x5100 01C0 | ERR_IRQ_STATUS_RAW | Raw ERR Interrupt Status |
| 0x5100 01C4 | ERR_IRQ_STATUS | ERR Interrupt Enabled Status |
| 0x5100 01C8 | ERR_IRQ_ENABLE_SET | ERR Interrupt Enable Set |
| 0x5100 01CC | ERR_IRQ_ENABLE_CLR | ERR Interrupt Enable Clear |
| 0x5100 01D0 | PMRST_IRQ_STATUS_RAW | Power Management and Reset Interrupt Status |
| 0x5100 01D4 | PMRST_IRQ_STATUS | Power Management and Reset Interrupt Enabled Status |
| 0x5100 01D8 | PMRST_ENABLE_SET | Power Management and Reset Interrupt Enable Set |
| 0x5100 01DC | PMRST_ENABLE_CLR | Power Management and Reset Interrupt Enable Clear |
| 0x5100 0200 | OB_OFFSET_INDEXn | Outbound Translation Region N Offset Low and Index |
| 0x5100 0204 | OB_OFFSETn_HI | Outbound Translation Region N Offset High |
| 0x5100 0300 | IB_BAR0 | Inbound Translation Bar Match 0 |
| 0x5100 0304 | IB_START0_LO | Inbound Translation 0 Start Address Low |
| 0x5100 0308 | IB_START0_HI | Inbound Translation 0 Start Address High |
| 0x5100 030C | IB_OFFSET0 | Inbound Translation 0 Address Offset |
| 0x5100 0310 | IB_BAR1 | Inbound Translation Bar Match 1 |
| 0x5100 0314 | IB_START1_LO | Inbound Translation 1 Start Address Low |
| 0x5100 0318 | IB_START1_HI | Inbound Translation 1 Start Address High |
| 0x5100 031C | IB_OFFSET1 | Inbound Translation 1 Address Offset |
| 0x5100 0320 | IB_BAR2 | Inbound Translation Bar Match 2 |
| 0x5100 0324 | IB_START2_LO | Inbound Translation 2 Start Address Low |
| 0x5100 0328 | IB_START2_HI | Inbound Translation 2 Start Address High |
| 0x5100 032C | IB_OFFSET2 | Inbound Translation 2 Address Offset |
| 0x5100 0330 | IB_BAR3 | Inbound Translation Bar Match 3 |
| 0x5100 0334 | IB_START3_LO | Inbound Translation 3 Start Address Low |
| 0x5100 0338 | IB_START3_HI | Inbound Translation 3 Start Address High |
| 0x5100 033C | IB_OFFSET3 | Inbound Translation 3 Address Offset |
| 0x5100 0380 | PCS_CFG0 | PCS Configuration 0 |
| 0x5100 0384 | PCS_CFG1 | PCS Configuration 1 |
| 0x5100 0388 | PCS_STATUS | PCS Status |
| 0x5100 0390 | SERDES_CFG0 | SerDes Configuration for Lane 0 |
| 0x5100 0394 | SERDES_CFG1 | SerDes Configuration for Lane 1 |


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### 9.14.3 PCIe Electrical Data and Timing

Texas Instruments (TI) has performed the simulation and system characterization to ensure that the PCIe peripheral meets all AC timing specifications as required by the PCI Express Base 2.0 Specification. Therefore, the AC timing specifications are not reproduced here. For more information on the AC timing specifications, see Sections 4.3.3.5 and 4.3.4.4 of the PCI Express Base 2.0 Specification.

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## 9.15 Real-Time Clock (RTC)

The real-time clock is a precise timer that can generate interrupts on intervals specified by the user. Interrupts can occur every second, minute, hour, or day. The clock, itself, can track the passage of real time for durations of several years, provided it has a sufficient power source the whole time.

The basic purpose for the RTC is to keep time of day. The other equally important purpose of the RTC is for Digital Rights management. Some degree of tamper-proofing is needed to ensure that simply stopping, resetting, or corrupting the RTC does not go unnoticed; so, if this occurs, the application can re-acquire the time of day from a trusted source. The final purpose of RTC is to wake up the rest of the device from a power-down state. The RTC features include:

- Time information (hours, minutes, seconds) directly in binary coded decimal (BCD), for easy decoding.
- Calendar information (day, month, year, day of week) directly in BCD code up to year 2099.
- Shadow time and calendar access; ease of reading time.
- Interrupt generation, periodically (1d, 1h, 1m, 1s) or at a precise time of day or date.
- 30-second time correction (crystal frequency compensation).
- OCP slave port for register access.
- Supports power idle protocol with SWakeUp capable on alarm or timer events.

The RTC is driven by SYSCLK18 (32.768 kHz) or an optional 32.768-kHz clock can be input on the CLKIN32 clock input pin for RTC reference. If the CLKIN32 pin is not connected to a 32.768-kHz clock input, this pin should be pulled low.

Figure 9-78 shows the major components of the RTC.

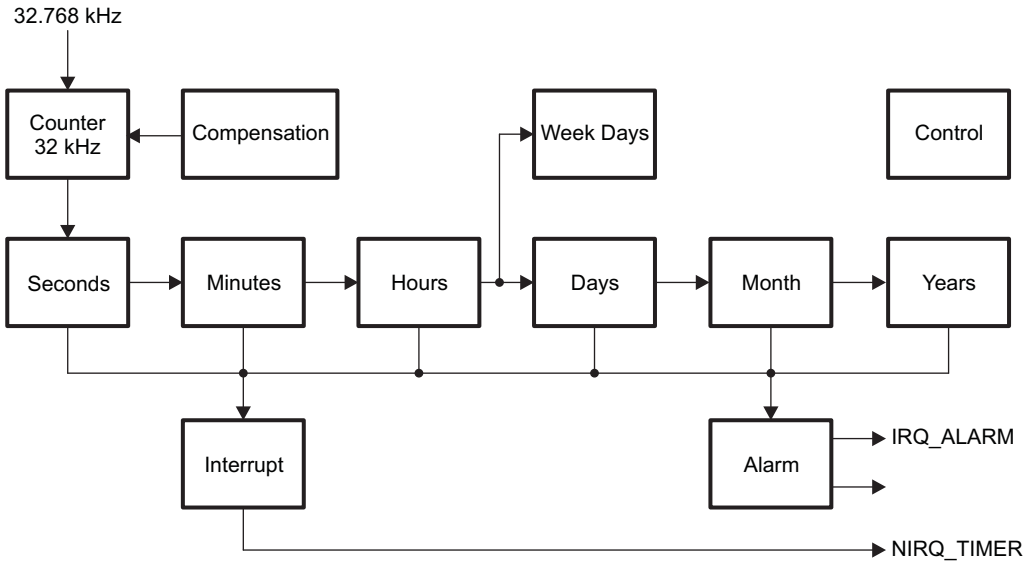


**Figure 9-78. Real-Time Clock Block Diagram**

### *9.15.1 RTC Register Descriptions*

**Table 9-89. RTC Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x480C 0000 | SECONDS_REG | Seconds |
| 0x480C 0004 | MINUTES_REG | Minutes |
| 0x480C 0008 | HOURS_REG | Hours |
| 0x480C 000C | DAYS_REG | Day of the Month |
| 0x480C 0010 | MONTHS_REG | Month |


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**Table 9-89. RTC Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x480C 0014 | YEARS_REG | Year |
| 0x480C 0018 | WEEK_REG | Day of the Week |
| 0x480C 0020 | ALARM_SECONDS_REG | Alarm Seconds |
| 0x480C 0024 | ALARM_MINUTES_REG | Alarm Minutes |
| 0x480C 0028 | ALARM_HOURS_REG | Alarm Hours |
| 0x480C 002C | ALARM_DAYS_REG | Alarm Days |
| 0x480C 0030 | ALARM_MONTHS_REG | Alarm Months |
| 0x480C 0034 | ALARM_YEARS_REG | Alarm Years |
| 0x480C 0040 | RTC_CTRL_REG | Control |
| 0x480C 0044 | RTC_STATUS_REG | Status |
| 0x480C 0048 | RTC_INTERRUPTS_REG | Interrupt Enable |
| 0x480C 004C | RTC_COMP_LSB_REG | Compensation (LSB) |
| 0x480C 0050 | RTC_COMP_MSB_REG | Compensation (MSB) |
| 0x480C 0054 | RTC_OSC_REG | Oscillator |
| 0x480C 0060 | RTC_SCRATCH0_REG | Scratch 0 (general-purpose) |
| 0x480C 0064 | RTC_SCRATCH1_REG | Scratch 1 (general-purpose) |
| 0x480C 0068 | RTC_SCRATCH2_REG | Scratch 2 (general-purpose) |
| 0x480C 006C | KICK0 | Kick 0 (write protect) |
| 0x480C 0070 | KICK1 | Kick 1 (write protect) |
| 0x480C 0074 | RTC_REVISION | Revision |
| 0x480C 0078 | RTC_SYSCONFIG | Clock Management Configuration |
| 0x480C 007A | RTC_IRQWAKEEN_0 | Wakeup Generation |

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## 9.16 Secure Digital and Secure Digital Input Output (SD and SDIO)

The device SD and SDIO Controller has following features:

- Secure Digital (SD) memory card with Secure Data IO (SDIO)
- Supports SDHC (SD high capacity)
- SD and SDIO protocol support
- Programmable clock frequency
- 1024 byte read or write FIFO to lower system overhead
- Slave DMA transfer capability
- Full compliance with SD command and response sets, as defined in the SD physical layer specification v2.00
- Full compliance with SDIO command and response sets and interrupt and read-wait suspend-resume operations, as defined in the SD part E1 specification v 2.00
- Full compliance with SD host controller standard specification sets as defined in the SD card specification part A2 v2.00.

For more detailed information on SD and SDIO, see the SD and SDIO chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### *9.16.1 SD and SDIO Peripheral Register Descriptions*

**Table 9-90. SD and SDIO Registers(1)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4806 0000 | SD_HL_REV | IP Revision Identifier |
| 0x4806 0004 | SD_HL_HWINFO | Hardware Configuration |
| 0x4806 0010 | SD_HL_SYSCONFIG | Clock Management Configuration |
| 0x4806 0110 | SD_SYSCONFIG | System Configuration |
| 0x4806 0114 | SD_SYSSTATUS | System Status |
| 0x4806 0124 | SD_CSRE | Card status response error |
| 0x4806 0128 | SD_SYSTEST | System Test |
| 0x4806 012C | SD_CON | Configuration |
| 0x4806 0130 | SD_PWCNT | Power counter |
| 0x4806 0200 | SD_SDMASA | SDMA System address: |
| 0x4806 0204 | SD_BLK | Transfer Length Configuration |
| 0x4806 0208 | SD_ARG | Command argument |
| 0x4806 020C | SD_CMD | Command and transfer mode |
| 0x4806 0210 | SD_RSP10 | Command Response 0 and 1 |
| 0x4806 0214 | SD_RSP32 | Command Response 2 and 3 |
| 0x4806 0218 | SD_RSP54 | Command Response 4 and 5 |
| 0x4806 021C | SD_RSP76 | Command Response 6 and 7 |
| 0x4806 0220 | SD_DATA | Data |
| 0x4806 0224 | SD_PSTATE | Present state |
| 0x4806 0228 | SD_HCTL | Host Control |
| 0x4806 022C | SD_SYSCTL | SD system control |
| 0x4806 0230 | SD_STAT | Interrupt status |
| 0x4806 0234 | SD_IE | Interrupt SD enable |
| 0x4806 0238 | SD_ISE | |
| 0x4806 023C | SD_AC12 | Auto CMD12 Error Status |
| 0x4806 0240 | SD_CAPA | Capabilities |
| 0x4806 0248 | SD_CUR_CAPA | Maximum current capabilities |

(1) SD and SDIO registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.


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**Table 9-90. SD and SDIO Registers[1] (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4806 0250 | SD_FE | Force Event |
| 0x4806 0254 | SD_ADMAES | ADMA Error Status |
| 0x4806 0258 | SD_ADMASAL | ADMA System address Low bits |
| 0x4806 025C | SD_ADMASAH | ADMA System address High bits |
| 0x4806 02FC | SD_REV | Versions |

## 9.16.2 SD and SDIO Electrical Data and Timing

### 9.16.2.1 SD Identification and Standard SD Mode

**Table 9-91. Timing Requirements for SD and SDIO—SD Identification and Standard SD Mode**

(see Figure 9-80, Figure 9-82)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **SD Identification Mode** | | | | | |
| 1 | $t_{su(CMDV-CLKH)}$ | Setup time, SD_CMD valid before SD_CLK rising clock edge | 1198.2 | | ns |
| 2 | $t_{h(CLKH-CMDIV)}$ | Hold time, SD_CMD valid after SD_CLK rising clock edge | 1249.0 | | ns |
| **Standard SD Mode** | | | | | |
| 1 | $t_{su(CMDV-CLKH)}$ | Setup time, SD_CMD valid before SD_CLK rising clock edge | 4.1 | | ns |
| 2 | $t_{h(CLKH-CMDIV)}$ | Hold time, SD_CMD valid after SD_CLK rising clock edge | 1.9 | | ns |
| 3 | $t_{su(DATV-CLKH)}$ | Setup time, SD_DATx valid before SD_CLK rising clock edge | 4.1 | | ns |
| 4 | $t_{h(CLKH-DATV)}$ | Hold time, SD_DATx valid after SD_CLK rising clock edge | 1.9 | | ns |

**Table 9-92. Switching Characteristics Over Recommended Operating Conditions for SD and SDIO—SD Identification and Standard SD Mode**

(see Figure 9-79, Figure 9-80, Figure 9-81, Figure 9-82)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **SD Identification Mode** | | | | | |
| 8 | $f_{op(CLKID)}$ | Identification mode frequency, SD_CLK | | 400 | kHz |
| | $t_{c(CLKID)}$ | Identification mode period, SD_CLK | 2500.0 | | ns |
| 13 | $t_{d(CLKH-CMD)}$ | Delay time, SD_CLK rising clock edge to SD_CMD transition | 6.5 | 2492.5 | ns |
| **Standard SD Mode** | | | | | |
| 7 | $f_{op(CLK)}$ | Operating frequency, SD_CLK | | 24 | MHz |
| | $t_{c(CLK)}$ | Operating period, SD_CLK | 41.7 | | ns |
| 9 | $t_{w(CLKL)}$ | Pulse duration, SD_CLK low | 0.45*P[1] | 0.55*P[1] | ns |
| 10 | $t_{w(CLKH)}$ | Pulse duration, SD_CLK high | 0.45*P[1] | 0.55*P[1] | ns |
| 13 | $t_{d(CLKH-CMD)}$ | Delay time, SD_CLK rising clock edge to SD_CMD transition | 6.3 | 35.3 | ns |
| 14 | $t_{d(CLKH-DAT)}$ | Delay time, SD_CLK rising clock edge to SD_DATx transition | 6.3 | 35.3 | ns |

(1) P = SD_CLK period.

### 9.16.2.2 High-Speed SD Mode

**Table 9-93. Timing Requirements for SD and SDIO—High-Speed SD Mode**

(see Figure 9-80, Figure 9-82)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{su(CMDV-CLKH)}$ | Setup time, SD_CMD valid before SD_CLK rising clock edge | 4.1 | | ns |
| 2 | $t_{h(CLKH-CMDV)}$ | Hold time, SD_CMD valid after SD_CLK rising clock edge | 1.9 | | ns |
| 3 | $t_{su(DATV-CLKH)}$ | Setup time, SD_DATx valid before SD_CLK rising clock edge | 4.1 | | ns |
| 4 | $t_{h(CLKH-DATV)}$ | Hold time, SD_DATx valid after SD_CLK rising clock edge | 1.9 | | ns |

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**Table 9-94. Switching Characteristics Over Recommended Operating Conditions for SD and SDIO—High-Speed SD Mode**

(see Figure 9-79, Figure 9-80, Figure 9-81, Figure 9-82)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 7 | $f_{op(CLK)}$ | Operating frequency, SD_CLK | | 48 | MHz |
| | $t_{c(CLK)}$ | Operating period: SD_CLK | 20.8 | | ns |
| 8 | $f_{op(CLKID)}$ | Identification mode frequency, SD_CLK | | 400 | kHz |
| | $t_{c(CLKID)}$ | Identification mode period: SD_CLK | 2500.0 | | ns |
| 9 | $t_{w(CLKL)}$ | Pulse duration, SD_CLK low | 0.5*P (1) | | ns |
| 10 | $t_{w(CLKH)}$ | Pulse duration, SD_CLK high | 0.5*P (1) | | ns |
| 11 | $t_{r(CLK)}$ | Rise time, All Signals (10% to 90%) | | 2.2 | ns |
| 12 | $t_{f(CLK)}$ | Fall time, All Signals (10% to 90%) | | 2.2 | ns |
| 13 | $t_{d(CLKL-CMD)}$ | Delay time, SD_CLK rising clock edge to SD_CMD transition | 2.5 (2) | 13.9 | ns |
| 14 | $t_{d(CLKL-DAT)}$ | Delay time, SD_CLK rising clock edge to SD_DATx transition | 2.5 (2) | 13.9 | ns |

(1) P = SD_CLK period.
(2) Longer DATA and CMD PCB track routing than clock trace routing may be needed to meet SD device input hold time.

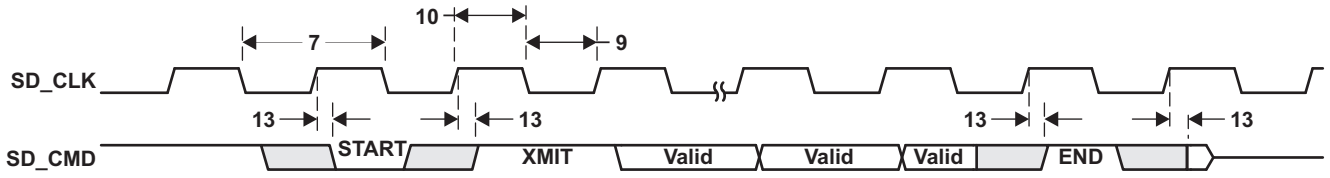


**Figure 9-79. SD Host Command Timing**

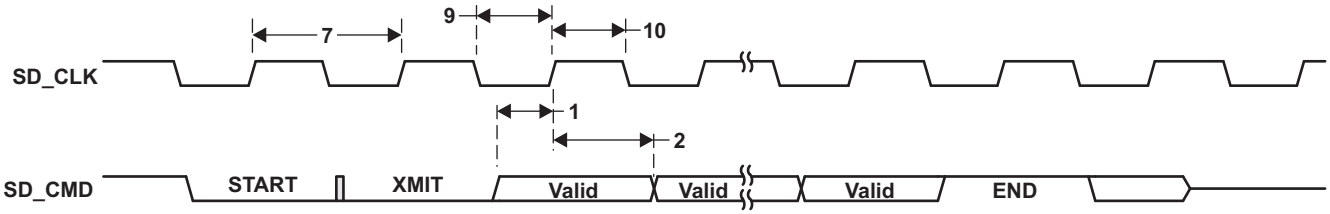


**Figure 9-80. SD Card Response Timing**

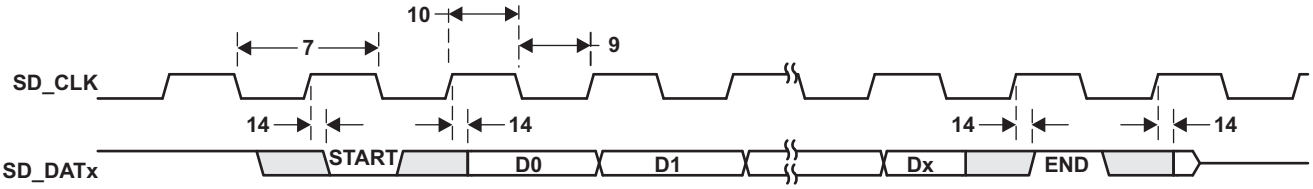


**Figure 9-81. SD Host Write Timing**

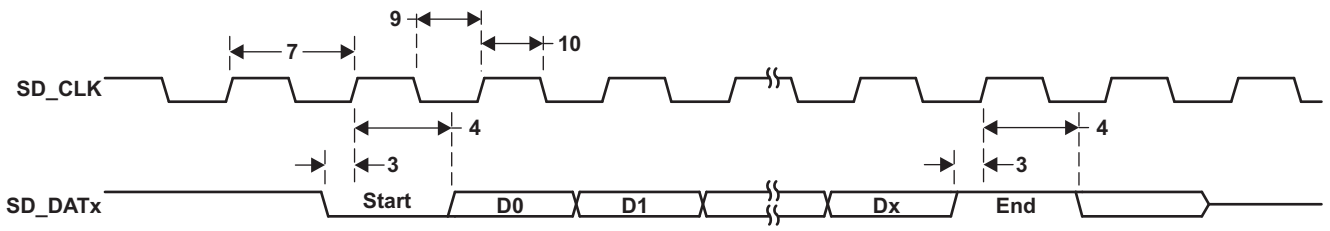


**Figure 9-82. SD Host Read and Card CRC Status Timing**


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## 9.17 Serial ATA Controller (SATA)

The Serial ATA (SATA) peripheral provides a direct interface for up to two hard disk drives (SATA) and supports the following features:

- Serial ATA 1.5 Gbps and 3 Gbps speeds
- Integrated PHY
- Integrated Rx and Tx data buffers
- Supports all SATA power management features
- Hardware-assisted native command queuing (NCQ) for up to 32 entries
- Supports port multiplier with command-based switching for connection to multiple hard disk drives
- Activity LED support.

For more detailed information on the SATA, see the SATA chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### *9.17.1 SATA Interface Design Specifications*

**NOTE**

For more information on PCB layout, see the *DM816xx Easy CYG Package PCB Escape Routing* application report (literature number SPRABK6).

This section provides PCB design and layout specifications for the SATA interface. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. Simulation and system design work has been done to ensure the SATA interface requirements are met.

A standard 100-MHz differential clock source must be used for SATA operation (for details, see Section 8.3.2).

#### 9.17.1.1 SATA Interface Schematic

Figure 9-83 shows the data portion of the SATA interface schematic. The specific pin numbers can be obtained from Table 4-17, *Serial ATA Terminal Functions*.

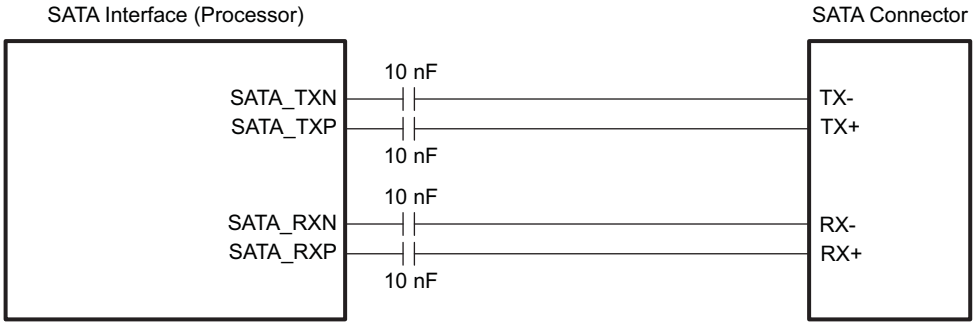


**Figure 9-83. SATA Interface High-Level Schematic**

#### 9.17.1.2 Compatible SATA Components and Modes

Table 9-95 shows the compatible SATA components and supported modes. Note that the only supported configuration is an internal cable from the processor host to the SATA device.

**Table 9-95. SATA Supported Modes**

| PARAMETER | MIN | MAX | UNIT | SUPPORTED |
|---|---|---|---|---|
| Transfer Rates | 1.5 | 3.0 | Gbps | |
| eSATA | - | - | - | No |

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**Table 9-95. SATA Supported Modes (continued)**

| PARAMETER | MIN | MAX | UNIT | SUPPORTED |
|---|---|---|---|---|
| xSATA | - | - | - | No |
| Backplane | - | - | - | No |
| Internal Cable | - | - | - | Yes |

### 9.17.1.3 PCB Stackup Specifications

Table 9-96 shows the PCB stackup and feature sizes required for SATA.

**Table 9-96. SATA PCB Stackup Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCB routing and plane layers | 4 | 6 | - | Layers |
| Signal routing layers | 2 | 3 | - | Layers |
| Number of ground plane cuts allowed within SATA routing region | - | - | 0 | Cuts |
| Number of layers between SATA routing region and reference ground plane | - | - | 0 | Layers |
| PCB trace width, w | - | 4 | - | Mils |
| PCB BGA escape via pad size | - | 20 | - | Mils |
| PCB BGA escape via hole size | - | 10 | | Mils |
| Processor BGA pad size(1) | | 0.3 | | mm |

(1) NSMD pad, per IPC-7351A BGA pad size guideline.

### 9.17.1.4 Routing Specifications

The SATA data signal traces must be routed to achieve 100 Ω (±20%) differential impedance and 60 Ω (±15%) single-ended impedance. The single-ended impedance is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important. 60 Ω is chosen for the single-ended impedance to minimize problems caused by too low an impedance.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 100 Ω differential impedance and 60 Ω single-ended impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

Table 9-97 shows the routing specifications for the SATA data signals.

**Table 9-97. SATA Routing Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Processor-to-SATA header trace length | | | 10(1) | Inches |
| Number of stubs allowed on SATA traces(2) | | | 0 | Stubs |
| TX and RX pair differential impedance | 80 | 100 | 120 | Ω |
| TX and RX single-ended impedance | 51 | 60 | 69 | Ω |
| Number of vias on each SATA trace | | | 3 | Vias(3) |
| SATA differential pair to any other trace spacing | 2*DS(4) | | | |

(1) Beyond this, signal integrity may suffer.
(2) In-line pads may be used for probing.
(3) Vias must be used in pairs with their distance minimized.
(4) DS = differential spacing of the SATA traces.


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#### 9.17.1.5 Coupling Capacitors

AC coupling capacitors are required on the receive data pair. Table 9-98 shows the requirements for these capacitors.

**Table 9-98. SATA AC Coupling Capacitors Requirements**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| SATA AC coupling capacitor value | 1 | 10 | 12 | nF |
| SATA AC coupling capacitor package size(1) | | 0402 | 0603 | EIA(2) |

(1) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair, placed side by side.
(2) EIA LxW units; for example, a 0402 is a 40x20 mil surface-mount capacitor.

### 9.17.2 SATA Peripheral Register Descriptions

**Table 9-99. SATA Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A14 0000 | CAP | HBA Capabilities |
| 0x4A14 0004 | GHC | Global HBA Control |
| 0x4A14 0008 | IS | Interrupt Status |
| 0x4A14 000C | PI | Ports Implemented |
| 0x4A14 0010 | VS | AHCI Version |
| 0x4A14 0014 | CCC_CTL | Command Completion Coalescing Control |
| 0x4A14 0018 | CCC_PORTS | Command Completion Coalescing Ports |
| 0x4A14 001C - 0x4A14 009C | - | Reserved |
| 0x4A14 00A0 | BISTAFR | BIST Active FIS |
| 0x4A14 00A4 | BISTCR | BIST Control |
| 0x4A14 00A8 | BISTFCTR | BIST FIS Count |
| 0x4A14 00AC | BISTSR | BIST Status |
| 0x4A14 00B0 | BISTDECR | BIST DWORD Error Count |
| 0x4A14 00B4 - 0x4A14 00DF | - | Reserved |
| 0x4A14 00E0 | TIMER1MS | BIST DWORD Error Count |
| 0x4A14 00E4 | - | Reserved |
| 0x4A14 00E8 | GPARAM1R | Global Parameter 1 |
| 0x4A14 00EC | GPARAM2R | Global Parameter 2 |
| 0x4A14 00F0 | PPARAMR | Port Parameter |
| 0x4A14 00F4 | TESTR | Test |
| 0x4A14 00F8 | VERSIONR | Version |
| 0x4A14 00FC | IDR (PID) | ID |
| 0x4A14 0100 | P0CLB | Port 0 Command List Base Address |
| 0x4A14 0104 | - | Reserved |
| 0x4A14 0108 | P0FB | Port 0 FIS Base Address |
| 0x4A14 010C | - | Reserved |
| 0x4A14 0110 | P0IS | Port 0 Interrupt Status |
| 0x4A14 0114 | P0IE | Port 0 Interrupt Enable |
| 0x4A14 0118 | P0CMD | Port 0 Command |
| 0x4A14 011C | - | Reserved |
| 0x4A14 0120 | P0TFD | Port 0 Task File Data |
| 0x4A14 0124 | P0SIG | Port 0 Signature |
| 0x4A14 0128 | P0SSTS | Port 0 Serial ATA Status (SStatus) |
| 0x4A14 012C | P0SCTL | Port 0 Serial ATA Control (SControl) |
| 0x4A14 0130 | P0SERR | Port 0 Serial ATA Error (SError) |

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**Table 9-99. SATA Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A14 0134 | P0SACT | Port 0 Serial ATA Active (SActive) |
| 0x4A14 0138 | P0CI | Port 0 Command Issue |
| 0x4A14 013C | P0SNTF | Port 0 Serial ATA Notification |
| 0x4A14 0140 - 0x4A14 016C | - | Reserved |
| 0x4A14 0170 | P0DMACR | Port 0 DMA Control |
| 0x4A14 0174 | - | Reserved |
| 0x4A14 0178 | P0PHYCR | Port 0 PHY Control |
| 0x4A14 017C | P0PHYSR | Port 0 PHY Status |
| 0x4A14 0180 | P1CLB | Port 1 Command List Base Address |
| 0x4A14 0184 | - | Reserved |
| 0x4A14 0188 | P1FB | Port 1 FIS Base Address |
| 0x4A14 018C | - | Reserved |
| 0x4A14 0190 | P1IS | Port 1 Interrupt Status |
| 0x4A14 0194 | P1IE | Port 1 Interrupt Enable |
| 0x4A14 0198 | P1CMD | Port 1 Command |
| 0x4A14 019C | - | Reserved |
| 0x4A14 01A0 | P1TFD | Port 1 Task File Data |
| 0x4A14 01A4 | P1SIG | Port 1 Signature |
| 0x4A14 01A8 | P1SSTS | Port 1 Serial ATA Status (SStatus) |
| 0x4A14 01AC | P1SCTL | Port 1 Serial ATA Control (SControl) |
| 0x4A14 01B0 | P1SERR | Port 1 Serial ATA Error (SError) |
| 0x4A14 01B4 | P1SACT | Port 1 Serial ATA Active (SActive) |
| 0x4A14 01B8 | P1CI | Port 1 Command Issue |
| 0x4A14 01BC | P1SNTF | Port 1 Serial ATA Notification |
| 0x4A14 01C0 - 0x4A14 01EC | - | Reserved |
| 0x4A14 01F0 | P1DMACR | Port 1 DMA Control |
| 0x4A14 01F4 | - | Reserved |
| 0x4A14 01F8 | P1PHYCR | Port 1 PHY Control |
| 0x4A14 01FC | P1PHYSR | Port 1 PHY Status |
| 0x4A14 1100 | IDLE | Idle and Standby Modes |
| 0x4A14 1104 | PHYCFGR2 | PHY Configuration 2 |


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## 9.18 Serial Peripheral Interface (SPI)

The SPI is a high-speed synchronous serial input and output port that allows a serial bit stream of programmed length (4 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the device and external peripherals. Typical applications include an interface-to-external IO or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMs, and analog-to-digital converters (ADCs).

The SPI supports the following features:

- Master and slave operation
- Four chip selects for interfacing and control to up to four SPI slave devices and connection to a single external master
- 32-bit shift register
- Buffered receive and transmit data register per channel (1 word deep), FIFO size is 64 bytes
- Programmable SPI configuration per channel (clock definition, enable polarity and word width)
- Supports one interrupt request and two DMA requests per channel.

For more detailed information on the SPI, see the SPI chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### 9.18.1 SPI Peripheral Register Descriptions

**Table 9-100. SPI Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4803 0000 - 0x4803 010C | - | RESERVED |
| 0x4803 0110 | MCSPI_SYSCONFIG | SYSTEM CONFIGURATION |
| 0x4803 0114 | MCSPI_SYSSTATUS | SYSTEM STATUS |
| 0x4803 0118 | MCSPI_IRQSTATUS | INTERRUPT STATUS |
| 0x4803 011C | MCSPI_IRQENABLE | INTERRUPT ENABLE |
| 0x4803 0120 | - | RESERVED |
| 0x4803 0124 | MCSPI_SYST | SYSTEM TEST |
| 0x4803 0128 | MCSPI_MODULCTRL | MODULE CONTROL |
| 0x4803 012C | MCSPI_CH0CONF | CHANNEL 0 CONFIGURATION |
| 0x4803 0130 | MCSPI_CH0STAT | CHANNEL 0 STATUS |
| 0x4803 0134 | MCSPI_CH0CTRL | CHANNEL 0 CONTROL |
| 0x4803 0138 | MCSPI_TX0 | CHANNEL 0 TRANSMITTER |
| 0x4803 013C | MCSPI_RX0 | CHANNEL 0 RECEIVER |
| 0x4803 0140 | MCSPI_CH1CONF | CHANNEL 1 CONFIGURATION |
| 0x4803 0144 | MCSPI_CH1STAT | CHANNEL 1 STATUS |
| 0x4803 0148 | MCSPI_CH1CTRL | CHANNEL 1 CONTROL |
| 0x4803 014C | MCSPI_TX1 | CHANNEL 1 TRANSMITTER |
| 0x4803 0150 | MCSPI_RX1 | CHANNEL 1 RECEIVER |
| 0x4803 0154 | MCSPI_CH2CONF | CHANNEL 2 CONFIGURATION |
| 0x4803 0158 | MCSPI_CH2STAT | CHANNEL 2 STATUS |
| 0x4803 015C | MCSPI_CH2CTRL | CHANNEL 2 CONTROL |
| 0x4803 0160 | MCSPI_TX2 | CHANNEL 2 TRANSMITTER |
| 0x4803 0164 | MCSPI_RX2 | CHANNEL 2 RECEIVER |
| 0x4803 0168 | MCSPI_CH3CONF | CHANNEL 3 CONFIGURATION |
| 0x4803 016C | MCSPI_CH3STAT | CHANNEL 3 STATUS |
| 0x4803 0170 | MCSPI_CH3CTRL | CHANNEL 3 CONTROL |
| 0x4803 0174 | MCSPI_TX3 | CHANNEL 3 TRANSMITTER |
| 0x4803 0178 | MCSPI_RX3 | CHANNEL 3 RECEIVER |

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**Table 9-100. SPI Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4803 017C | MCSPI_XFERLEVEL | TRANSFER LEVELS |
| 0x4803 0180 - 0x4803 01FF | - | RESERVED |


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### 9.18.2 SPI Electrical Data and Timing

**Table 9-101. Timing Requirements for SPI - Master Mode**

(see Figure 9-84 and Figure 9-85)

| NO. | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| **MASTER: 1 LOAD AT A MAXIMUM OF 5 pF** | | | | | | |
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK (1)(2) | | 20.8 (3) | | ns |
| 2 | $t_{w(SPICLKL)}$ | Pulse duration, SPI_CLK low (1) | | 0.5*P - 1 (4) | | ns |
| 3 | $t_{w(SPICLKH)}$ | Pulse duration, SPI_CLK high (1) | | 0.5*P - 1 (4) | | ns |
| 4 | $t_{su(MISO-SPICLK)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge (1) | | 2.29 | | ns |
| 5 | $t_{h(SPICLK-MISO)}$ | Hold time, SPI_D[x] valid after SPI_CLK active edge (1) | | 2.67 | | ns |
| 6 | $t_{d(SPICLK-MOSI)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition (1) | | -3.57 | 3.57 | ns |
| 7 | $t_{d(SCS-MOSI)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active edge to SPI_D[x] transition | | | 3.57 | ns |
| 8 | $t_{d(SCS-SPICLK)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active to SPI_CLK first edge (1) | MASTER_PHA0 (5) | B-4.2 (6) | | ns |
| | | | MASTER_PHA1 (5) | A-4.2 (7) | | ns |
| 9 | $t_{d(SPICLK-SCS)}$ | Delay time, SPI_CLK last edge to $\overline{\text{SPI_SCS[x]}}$ inactive (1) | MASTER_PHA0 (5) | A-4.2 (7) | | ns |
| | | | MASTER_PHA1 (5) | B-4.2 (6) | | ns |
| **MASTER: UP TO 4 LOADS AT A MAXIMUM TOTAL OF 25 pF** | | | | | | |
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK (1)(2) | | 41.7 (8) | | ns |
| 2 | $t_{w(SPICLKL)}$ | Pulse duration, SPI_CLK low (1) | | 0.5*P - 2 (4) | | ns |
| 3 | $t_{w(SPICLKH)}$ | Pulse duration, SPI_CLK high (1) | | 0.5*P - 2 (4) | | ns |
| 4 | $t_{su(MISO-SPICLK)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge (1) | | 3.02 | | ns |
| 5 | $t_{h(SPICLK-MISO)}$ | Hold time, SPI_D[x] valid after SPI_CLK active edge (1) | | 2.76 | | ns |
| 6 | $t_{d(SPICLK-MOSI)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition (1) | | -4.62 | 4.62 | ns |
| 7 | $t_{d(SCS-MOSI)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active edge to SPI_D[x] transition | | | 4.62 | ns |
| 8 | $t_{d(SCS-SPICLK)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active to SPI_CLK first edge (1) | MASTER_PHA0 (5) | B-2.54 (6) | | ns |
| | | | MASTER_PHA1 (5) | A-2.54 (7) | | ns |
| 9 | $t_{d(SPICLK-SCS)}$ | Delay time, SPI_CLK last edge to $\overline{\text{SPI_SCS[x]}}$ inactive (1) | MASTER_PHA0 (5) | A-2.54 (7) | | ns |
| | | | MASTER_PHA1 (5) | B-2.54 (6) | | ns |

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) Related to the SPI_CLK maximum frequency.
(3) Maximum frequency = 48 MHz
(4) P = SPICLK period.
(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.
(6) B = (TCS + 0.5) * TSPICLKREF * $F_{ratio}$, where TCS is a bit field of the SPI_CH(i)CONF register and $F_{ratio}$ = Even ≥2.
(7) When P = 20.8 ns, A = (TCS + 1) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) * $F_{ratio}$ * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(8) Maximum frequency = 24 MHz

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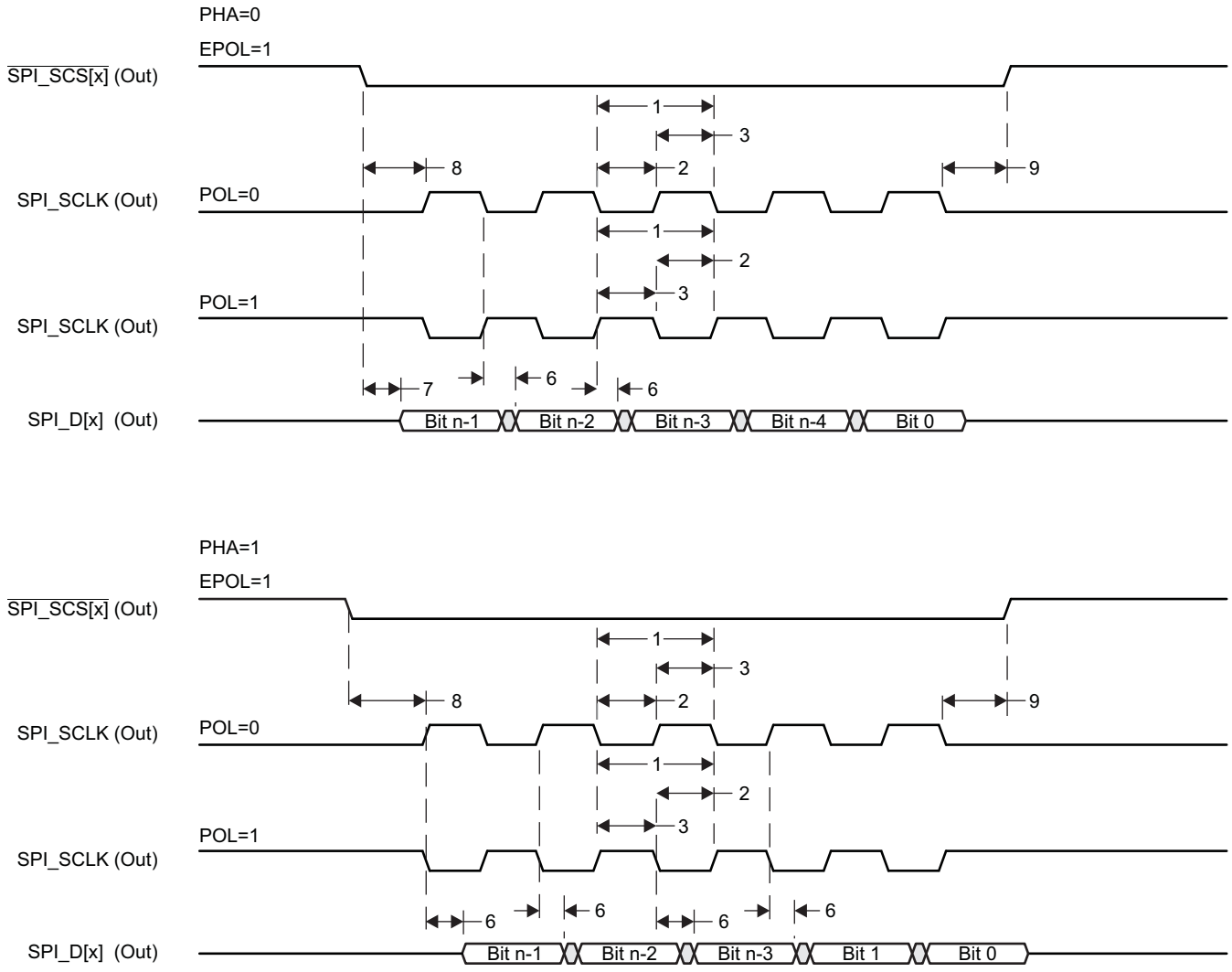


**Figure 9-84. SPI Master Mode Transmit Timing**


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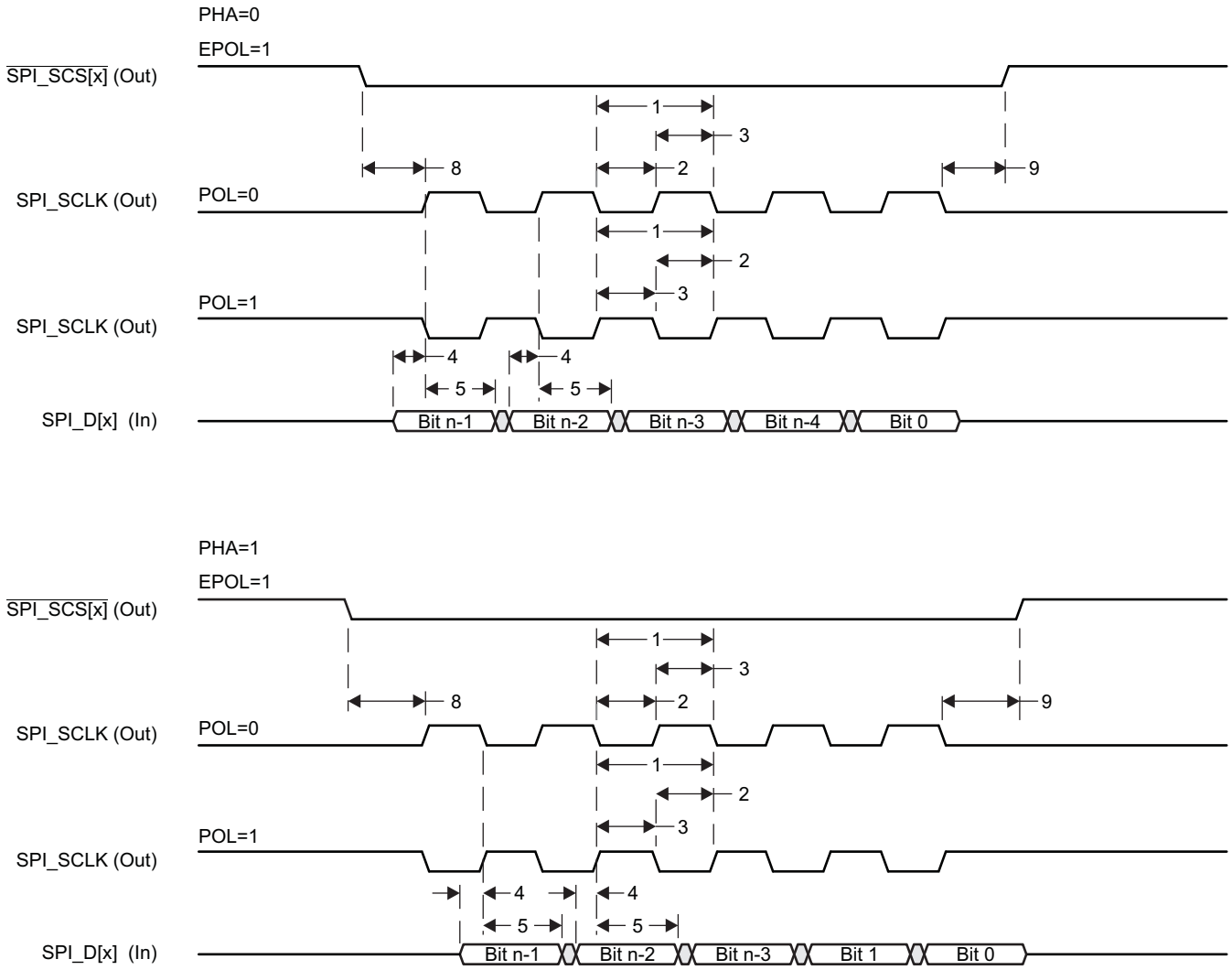


**Figure 9-85. SPI Master Mode Receive Timing**

## Table 9-102. Timing Requirements for SPI - Slave Mode

(see Figure 9-86 and Figure 9-87)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK (1) (2) | 62.5 (3) | | ns |
| 2 | $t_{w(SPICLKL)}$ | Pulse duration, SPI_CLK low (1) | 0.5*P - 3 (4) | | ns |
| 3 | $t_{w(SPICLKH)}$ | Pulse duration, SPI_CLK high (1) | 0.5*P - 3 (4) | | ns |
| 4 | $t_{su(MOSI-SPICLK)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge (1) | 12.92 | | ns |
| 5 | $t_{h(SPICLK-MOSI)}$ | Hold time, SPI_D[x] valid after SPI_CLK active edge (1) | 12.92 | | ns |
| 6 | $t_{d(SPICLK-MISO)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition (1) | -4.00 | 17.1 | ns |
| 7 | $t_{d(SCS-MISO)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active edge to SPI_D[x] transition (5) | | 17.1 | ns |
| 8 | $t_{su(SCS-SPICLK)}$ | Setup time, $\overline{\text{SPI_SCS[x]}}$ valid before SPI_CLK first edge (1) | 12.92 | | ns |
| 9 | $t_{h(SPICLK-SCS)}$ | Hold time, $\overline{\text{SPI_SCS[x]}}$ valid after SPI_CLK last edge (1) | 12.92 | | ns |

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) Related to the input maximum frequency supported by the SPI module.
(3) Maximum frequency = 16 MHz
(4) P = SPICLK period.
(5) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

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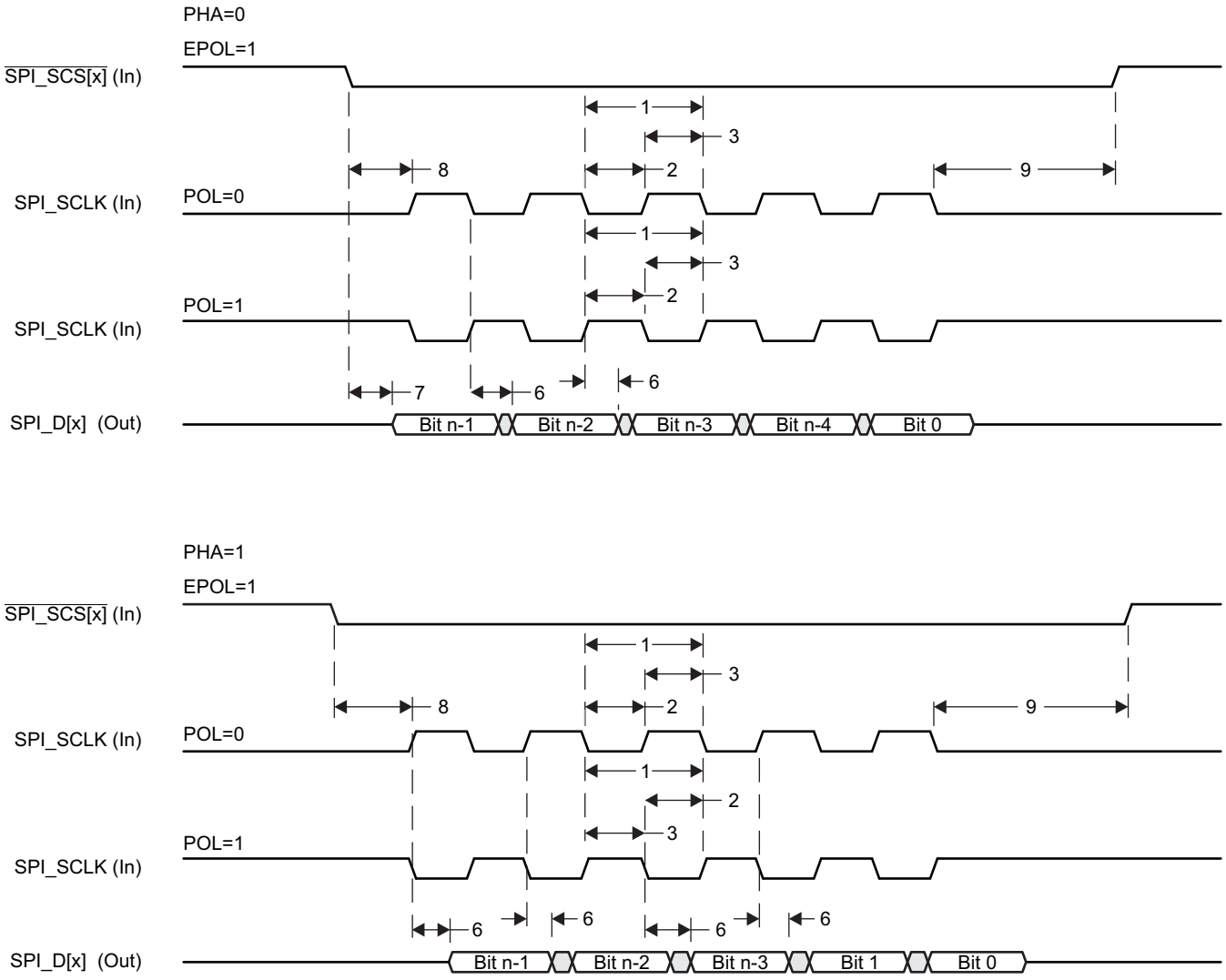


**Figure 9-86. SPI Slave Mode Transmit Timing**


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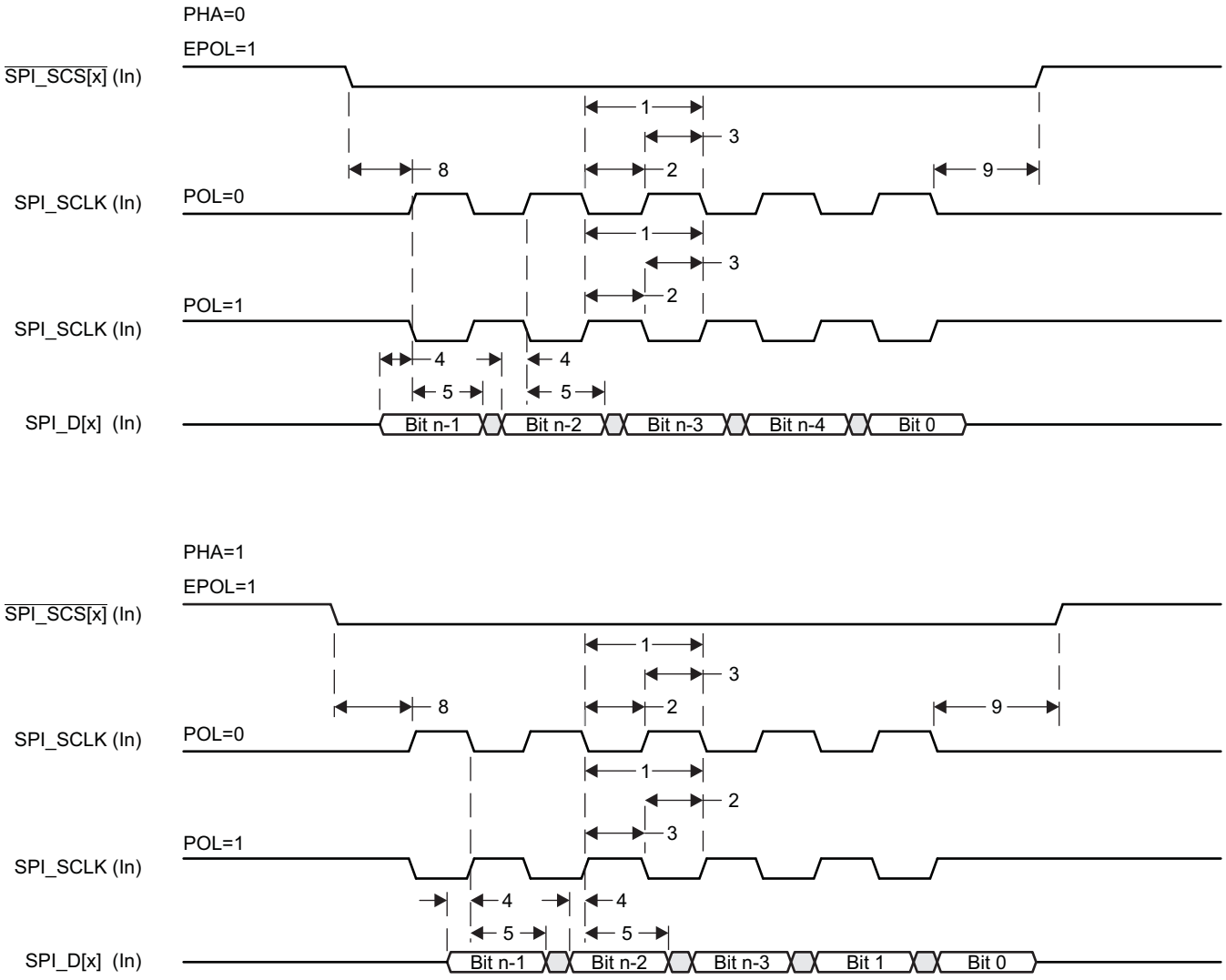


**Figure 9-87. SPI Slave Mode Receive Timing**

## 9.19 Timers

The device has seven 32-bit general-purpose (GP) timers that have the following features:

- Timers 1-3 are for software use and do not have an external connection
- Dedicated input trigger for capture mode and dedicated output trigger or pulse width modulation (PWM) signal
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- Timer[7:1] functional clock is sourced from either the 27-MHz system clock, 32.768-kHz RTC clock or the TCLKIN external timer input clock, as selected within the PRCM
- On-the-fly read and write register (while counting)
- Generates interrupts to the ARM and DSP CPUs.

The device has one system watchdog timer that has the following features:

- Free-running 32-bit upward counter
- On-the-fly read and write register (while counting)
- Reset upon occurrence of a timer overflow condition
- Two possible clock sources:
  - Internal 32.768-kHz clock derived from 27-MHz system clock.
  - External clock input on the CLKIN32 input pin.

The watchdog timer is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

For more detailed information, see the Timers chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

### *9.19.1 Timer Peripheral Register Descriptions*

**Table 9-103. Timer1-7 Registers(1)**

| TIMER1 HEX ADDRESS | TIMER2 HEX ADDRESS | TIMER3 HEX ADDRESS | TIMER4 HEX ADDRESS | TIMER5 HEX ADDRESS | TIMER6 HEX ADDRESS | TIMER7 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|---|---|---|
| 0x4802 E000 | 0x4804 0000 | 0x4804 2000 | 0x4804 4000 | 0x4804 6000 | 0x4804 8000 | 0x4804 A000 | TIDR | Identification |
| 0x4802 E010 | 0x4804 0010 | 0x4804 2010 | 0x4804 4010 | 0x4804 6010 | 0x4804 8010 | 0x4804 A010 | TIOCP_CFG | Timer OCP Configuration |
| 0x4802 E020 | 0x4804 0020 | 0x4804 2020 | 0x4804 4020 | 0x4804 6020 | 0x4804 8020 | 0x4804 A020 | IRQ_EOI | Timer IRQ End-Of-Interrupt |
| 0x4802 E024 | 0x4804 0024 | 0x4804 2024 | 0x4804 4024 | 0x4804 6024 | 0x4804 8024 | 0x4804 A024 | IRQSTATUS_RAW | Timer IRQSTATUS Raw |
| 0x4802 E028 | 0x4804 0028 | 0x4804 2028 | 0x4804 4028 | 0x4804 6028 | 0x4804 8028 | 0x4804 A028 | IRQSTATUS | Timer IRQSTATUS |
| 0x4802 E02C | 0x4804 002C | 0x4804 202C | 0x4804 402C | 0x4804 602C | 0x4804 802C | 0x4804 A02C | IRQSTATUS_SET | Timer IRQENABLE Set |
| 0x4802 E030 | 0x4804 0030 | 0x4804 2030 | 0x4804 4030 | 0x4804 6030 | 0x4804 8030 | 0x4804 A030 | IRQSTATUS_CLR | Timer IRQENABLE Clear |
| 0x4802 E034 | 0x4804 0034 | 0x4804 2034 | 0x4804 4034 | 0x4804 6034 | 0x4804 8034 | 0x4804 A034 | IRQWAKEEN | Timer IRQ Wakeup Enable |
| 0x4802 E038 | 0x4804 0038 | 0x4804 2038 | 0x4804 4038 | 0x4804 6038 | 0x4804 8038 | 0x4804 A038 | TCLR | Timer Control |
| 0x4802 E03C | 0x4804 003C | 0x4804 203C | 0x4804 403C | 0x4804 603C | 0x4804 803C | 0x4804 A03C | TCRR | Timer Counter |
| 0x4802 E040 | 0x4804 0040 | 0x4804 2040 | 0x4804 4040 | 0x4804 6040 | 0x4804 8040 | 0x4804 A040 | TLDR | Timer Load |
| 0x4802 E044 | 0x4804 0044 | 0x4804 2044 | 0x4804 4044 | 0x4804 6044 | 0x4804 8044 | 0x4804 A044 | TTGR | Timer Trigger |

(1) All Timer registers are: 32-bit register accessible in 16-bit mode and use little-endian addressing.


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**Table 9-103. Timer1-7 Registers[(1)] (continued)**

| TIMER1 HEX ADDRESS | TIMER2 HEX ADDRESS | TIMER3 HEX ADDRESS | TIMER4 HEX ADDRESS | TIMER5 HEX ADDRESS | TIMER6 HEX ADDRESS | TIMER7 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|---|---|---|
| 0x4802 E048 | 0x4804 0048 | 0x4804 2048 | 0x4804 4048 | 0x4804 6048 | 0x4804 8048 | 0x4804 A048 | TWPS | Timer Write Posted Status |
| 0x4802 E04C | 0x4804 004C | 0x4804 204C | 0x4804 404C | 0x4804 604C | 0x4804 804C | 0x4804 A04C | TMAR | Timer Match |
| 0x4802 E050 | 0x4804 0050 | 0x4804 2050 | 0x4804 4050 | 0x4804 6050 | 0x4804 8050 | 0x4804 A050 | TCAR1 | Timer Capture |
| 0x4802 E054 | 0x4804 0054 | 0x4804 2054 | 0x4804 4054 | 0x4804 6054 | 0x4804 8054 | 0x4804 A054 | TSICR | Timer Synchronous Interface Control |
| 0x4802 E058 | 0x4804 0058 | 0x4804 2058 | 0x4804 4058 | 0x4804 6058 | 0x4804 8058 | 0x4804 A058 | TCAR2 | Timer Capture |

**Table 9-104. Watchdog Timer Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x480C 2000 | WIDR | IP Revision Identifier |
| 0x480C 2010 | WDSC | OCP interface parameters |
| 0x480C 2014 | WDST | Status information |
| 0x480C 2018 | WISR | Interrupt events pending |
| 0x480C 201C | WIER | Interrupt events control |
| 0x480C 2020 | WWER | Wakeup events control |
| 0x480C 2024 | WCLR | Counter prescaler control |
| 0x480C 2028 | WCRR | Internal counter value |
| 0x480C 202C | WLDR | Timer load value |
| 0x480C 2030 | WTGR | Watchdog counter reload |
| 0x480C 2034 | WWPS | Write posting bits |
| 0x480C 2044 | WDLY | Event detection delay value |
| 0x480C 2048 | WSPR | Start-stop value |
| 0x480C 2050 | WIRQEOI | Software End Of Interrupt |
| 0x480C 2054 | WIRQSTATRAW | IRQ unmasked status |
| 0x480C 2058 | WIRQSTAT | IRQ masked status |
| 0x480C 205C | WIRQENSET | IRQ enable |
| 0x480C 2060 | WIRQENCLR | IRQ enable clear |
| 0x480C 2064 | WIRQWAKEEN | IRQ wakeup events control |

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### 9.19.2 Timer Electrical Data and Timing

**Table 9-105. Timing Requirements for Timer**

(see Figure 9-88)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EVTIH)}$ | Pulse duration, high | 4P(1) | | ns |
| 2 | $t_{w(EVTIL)}$ | Pulse duration, low | 4P(1) | | ns |

(1) P = module clock.

**Table 9-106. Switching Characteristics Over Recommended Operating Conditions for Timer**

(see Figure 9-88)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 3 | $t_{w(EVTOH)}$ | Pulse duration, high | 4P-3(1) | | ns |
| 4 | $t_{w(EVTOL)}$ | Pulse duration, low | 4P-3(1) | | ns |

(1) P = module clock.

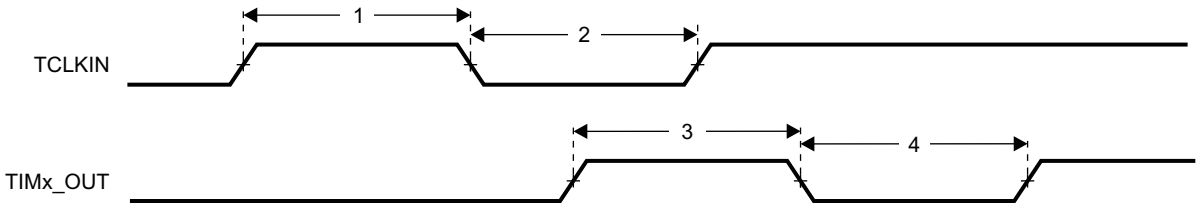


**Figure 9-88. Timer Timing**


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## 9.20 Universal Asynchronous Receiver and Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. The device provides up to three UART peripheral interfaces, depending on the selected pin multiplexing.

Each UART has the following features:

- Selectable UART, IrDA (SIR, MIR) and CIR modes
- Dual 64-entry FIFOs for received and transmitted data payload
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Baud-rate generation based upon programmable divisors N (N=1…16384)
- Two DMA requests and one interrupt request to the system
- Can connect to any RS-232 compliant device.

UART functions include:

- Baud-rate up to 3.6 Mbps
- Programmable serial interfaces characteristics
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity-bit generation and detection
  - 1, 1.5, or 2 stop-bit generation
  - Flow control: hardware (RTS and CTS) or software (XON and XOFF)
- Additional modem control functions (UART0_DTR, UART0_DSR, UART0_DCD, and UART0_RIN) for UART0 only; UART1 and UART2 do not support full-flow control signaling.

IR-IrDA functions include:

- Support of IrDA 1.4 slow infrared (SIR, baud-rate up to 115.2 Kbps), medium infrared (MIR, baud-rate up to 1.152 Mbps) and fast infrared (FIR baud-rate up to 4.0 Mbps) communications
- Supports framing error, cyclic redundancy check (CRC) error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection
- 8-entry status FIFO (with selectable trigger levels) available to monitor frame length and frame errors.

IR-CIR functions include:

- Consumer infrared (CIR) remote control mode with programmable data encoding
- Free data format (supports any remote control private standards)
- Selectable bit rate and configurable carrier frequency.

For more detailed information on the UART peripheral, see the UART chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8).

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### 9.20.1 UART Peripheral Register Descriptions

Table 9-107 lists the UART register name summary. Table 9-108 shows the UART registers along with their configuration requirements.

**Table 9-107. UART Register Summary**

| ACRONYM | REGISTER NAME | ACRONYM | REGISTER NAME |
|---|---|---|---|
| RHR | Receive Holding | RXFLH | Receive Frame Length High |
| THR | Transmit Holding | BLR | BOF Control |
| IER | Interrupt Enable | ACREG | Auxilliary Control |
| IIR | Interrupt Identification | SCR | Supplementary Control |
| FCR | FIFO Control | SSR | Supplementary Status |
| LCR | Line Control | EBLR | BOF Length |
| MCR | Modem Control | MVR | Module Version |
| LSR | Line Status | SYSC | System Configuration |
| MSR | Modem Status | SYSS | System Status |
| SPR | Scratchpad | WER | Wake-up Enable |
| TCR | Transmission Control | CFPS | Carrier Frequency Prescaler |
| TLR | Trigger Level | DLL | Divisor Latch Low |
| MDR1 | Mode Definition 1 | DLH | Divisor Latch High |
| MDR2 | Mode Definition 2 | UASR | UART Autobauding Status |
| SFLSR | Status FIFO Line Status | EFR | Enhanced Feature |
| RESUME | Resume | XON1 | UART XON1 Character |
| SFREGL | Status FIFO Low | XON2 | UART XON2 Character |
| SFREGH | Status FIFO High | XOFF1 | UART XOFF1 Character |
| TXFLL | Transmit Frame Length Low | XOFF2 | UART XOFF2 Character |
| TXFLH | Transmit Frame Length High | ADDR1 | IrDA Address 1 |
| RXFLL | Receive Frame Length Low | ADDR2 | IrDA Address 2 |

**Table 9-108. UART Registers Configuration Requirements[1][2][3]**

| UART0 HEX ADDRESS | UART1 HEX ADDRESS | UART2 HEX ADDRESS | REGISTER | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LCR[7] = 0 | | LCR[7] = 1 and LCR[7:0] ≠ 0xBF | | LCR[7:0] = 0xBF | |
| | | | READ | WRITE | READ | WRITE | READ | WRITE |
| 0x4802 0000 | 0x4802 2000 | 0x4802 4000 | RHR | THR | DLL | DLL | DLL | DLL |
| 0x4802 0004 | 0x4802 2004 | 0x4802 4004 | IER | IER | DLH | DLH | DLH | DLH |
| 0x4802 0008 | 0x4802 2008 | 0x4802 4008 | IIR | FCR | IIR | FCR | EFR | EFR |
| 0x4802 000C | 0x4802 200C | 0x4802 400C | LCR | LCR | LCR | LCR | LCR | LCR |
| 0x4802 0010 | 0x4802 2010 | 0x4802 4010 | MCR | MCR | MCR | MCR | XON1 or ADDR1 | XON1 or ADDR1 |
| 0x4802 0014 | 0x4802 2014 | 0x4802 4014 | LSR | - | LSR | - | XON2 or ADDR2 | XON2 or ADDR2 |
| 0x4802 0018 | 0x4802 2018 | 0x4802 4018 | MSR or TCR | TCR | MSR or TCR | TCR | XOFF1 or TCR | XOFF1 or TCR |
| 0x4802 001C | 0x4802 201C | 0x4802 401C | SPR orTLR | SPR orTLR | SPR or TLR | SPR orTLR | XOFF2 or TLR | XOFF2 or TLR |
| 0x4802 0020 | 0x4802 2020 | 0x4802 4020 | MDR1 | MDR1 | MDR1 | MDR1 | MDR1 | MDR1 |
| 0x4802 0024 | 0x4802 2024 | 0x4802 4024 | MDR2 | MDR2 | MDR2 | MDR2 | MDR2 | MDR2 |
| 0x4802 0028 | 0x4802 2028 | 0x4802 4028 | SFLSR | TXFLL | SFLSR | TXFLL | SFLSR | TXFLL |

(1) The transmission control register (TCR) and the trigger level register (TLR) are accessible only when EFR[4]=1 and MCR[6]=1.
(2) MCR[7:5] and FCR[5:4] can only be written when EFR[4]=1.
(3) In UART modes, IER[7:4] can only be written when EFR[4]=1. In IrDA and CIR modes, EFR[4] has no impact on the access to IER[7:4].


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**Table 9-108. UART Registers Configuration Requirements[1][2][3] (continued)**

| UART0 HEX ADDRESS | UART1 HEX ADDRESS | UART2 HEX ADDRESS | REGISTER | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LCR[7] = 0 | | LCR[7] = 1 and LCR[7:0] ≠ 0xBF | | LCR[7:0] = 0xBF | |
| | | | READ | WRITE | READ | WRITE | READ | WRITE |
| 0x4802 002C | 0x4802 202C | 0x4802 402C | RESUME | TXFLH | RESUME | TXFLH | RESUME | TXFLH |
| 0x4802 0030 | 0x4802 2030 | 0x4802 4030 | SFREGL | RXFLL | SFREGL | RXFLL | SFREGL | RXFLL |
| 0x4802 0034 | 0x4802 2034 | 0x4802 4034 | SFREGH | RXFLH | SFREGH | RXFLH | SFREGH | RXFLH |
| 0x4802 0038 | 0x4802 2038 | 0x4802 4038 | BLR | BLR | UASR | - | UASR | - |
| 0x4802 003C | 0x4802 203C | 0x4802 403C | ACREG | ACREG | - | - | - | - |
| 0x4802 0040 | 0x4802 2040 | 0x4802 4040 | SCR | SCR | SCR | SCR | SCR | SCR |
| 0x4802 0044 | 0x4802 2044 | 0x4802 4044 | SSR | SSR[2] | SSR | SSR[2] | SSR | SSR[2] |
| 0x4802 0048 | 0x4802 2048 | 0x4802 4048 | EBLR | EBLR | - | - | - | - |
| 0x4802 004C | 0x4802 204C | 0x4802 404C | - | - | - | - | - | - |
| 0x4802 0050 | 0x4802 2050 | 0x4802 4050 | MVR | - | MVR | - | MVR | - |
| 0x4802 0054 | 0x4802 2054 | 0x4802 4054 | SYSC | SYSC | SYSC | SYSC | SYSC | SYSC |
| 0x4802 0058 | 0x4802 2058 | 0x4802 4058 | SYSS | | SYSS | | SYSS | |
| 0x4802 005C | 0x4802 205C | 0x4802 405C | WER | WER | WER | WER | WER | WER |
| 0x4802 0060 | 0x4802 2060 | 0x4802 4060 | CFPS | CFPS | CFPS | CFPS | CFPS | CFPS |
| 0x4802 0064 - 0x4802 00C4 | 0x4802 2064 - 0x4802 20C4 | 0x4802 4064 - 0x4802 40C4 | - | - | - | - | - | - |

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### 9.20.2 UART Electrical Data and Timing

**Table 9-109. Timing Requirements for UART**

(see Figure 9-89)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 4 | $t_{w(RX)}$ | Pulse width, receive data bit, 15 pF, 30 pF, 100 pF high or low | 0.96U(1) | 1.05U(1) | ns |
| 5 | $t_{w(CTS)}$ | Pulse width, receive start bit, 15 pF, 30 pF, 100 pF high or low | 0.96U(1) | 1.05U(1) | ns |
| | $t_{d(RTS-TX)}$ | Delay time, transmit start bit to transmit data | P(2) | | ns |
| | $t_{d(CTS-TX)}$ | Delay time, receive start bit to transmit data | P(2) | | ns |

(1) U = UART baud time = 1/programmed baud rate.
(2) P = clock period of the reference clock (FCLK, usually 48 MHz).

**Table 9-110. Switching Characteristics Over Recommended Operating Conditions for UART**

(see Figure 9-89)

| NO. | PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| | $f_{(baud)}$ | Maximum programmable baud rate | 15 pF | | 5 | MHz |
| | | | 30 pF | | 0.23 | |
| | | | 100 pF | | 0.115 | |
| 2 | $t_{w(TX)}$ | Pulse width, transmit data bit, 15 pF, 30 pF, 100 pF high or low | | U - 2(1) | U + 2(1) | ns |
| 3 | $t_{w(RTS)}$ | Pulse width, transmit start bit, 15 pF, 30 pF, 100 pF high or low | | U - 2(1) | U + 2(1) | ns |

(1) U = UART baud time = 1/programmed baud rate.

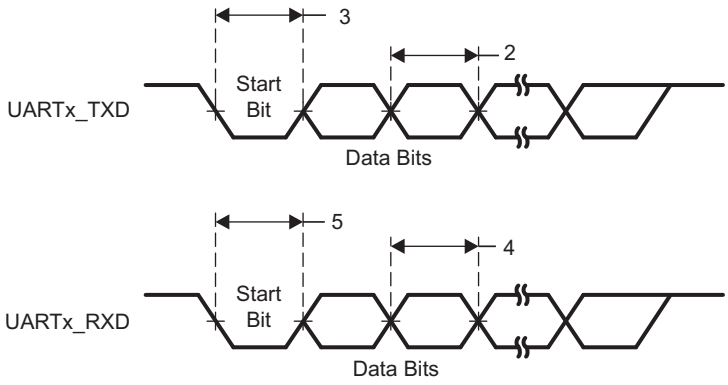


**Figure 9-89. UART Timing**


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## 9.21 Universal Serial Bus (USB2.0)

The device includes two USB2.0 modules which support the Universal Serial Bus Specification Revision 2.0. The following are some of the major USB features that are supported:

- USB 2.0 peripheral at high speed (HS: 480 Mbps) and full speed (FS: 12 Mbps)
- USB 2.0 host at HS, FS, and low speed (LS: 1.5 Mbps)
- Each endpoint (other than endpoint 0, control only) can support all transfer modes (control, bulk, interrupt, and isochronous)
- Supports high-bandwidth ISO mode
- Supports 16 Transmit (TX) and 16 Receive (RX) endpoints including endpoint 0
- FIFO RAM - 32K endpoint - Programmable size
- Includes two integrated PHYs; requires a low-jitter 24-MHz source clock for its PLL
- RNDIS-like mode for terminating RNDIS-type protocols without using short-packet termination for support of MSC applications.

The USB2.0 modules do not support the following features:

- On-chip charge pump (VBUS power must be generated external to the device)
- RNDIS mode acceleration for USB sizes that are not multiples of 64 bytes
- Endpoint max USB packet sizes that do not conform to the USB2.0 spec (for FS and LS: 8, 16, 32, 64, and 1023 are defined; for HS: 64, 128, 512, and 1024 are defined).

For more detailed information on the USB2.0 peripheral, see the USB2.0 chapter in the *TMS320DM816x DaVinci Digital Media Processors Technical Reference Manual* (literature number SPRUGX8). For detailed information on USB board design and layout guidelines, see the *USB 2.0 Board Design and Layout Guidelines* application report (literature number SPRAAR7). For general information on PCB layout, see the *DM816xx Easy CYG Package PCB Escape Routing* application report (literature number SPRABK6).

### 9.21.1 USB2.0 Peripheral Register Descriptions

**Table 9-111. USB2.0 Submodules**

| SUBMODULE ADDRESS OFFSET | SUBMODULE NAME |
|---|---|
| 0x0000 | USBSS registers |
| 0x1000 | USB0 controller registers |
| 0x1800 | USB1 controller registers |
| 0x2000 | CPPI DMA controller registers |
| 0x3000 | CPPI DMA scheduler registers |
| 0x4000 | CPPI DMA Queue Manager registers |

**Table 9-112. USB Subsystem (USBSS) Registers(1)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 0000 | REVREG | USBSS REVISION |
| 0x4740 0004 - 0x4740 000C | - | Reserved |
| 0x4740 0010 | SYSCONFIG | USBSS SYSCONFIG |
| 0x4740 0014 - 0x4740 001C | - | Reserved |
| 0x4740 0020 | EOI | USBSS IRQ_EOI |
| 0x4740 0024 | IRQSTATRAW | USBSS IRQ_STATUS_RAW |
| 0x4740 0028 | IRQSTAT | USBSS IRQ_STATUS |

(1) USBSS registers contain the registers that are used to control at the global level and apply to all submodules.

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**Table 9-112. USB Subsystem (USBSS) Registers[(1)] (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 002C | IRQENABLER | USBSS IRQ_ENABLE_SET |
| 0x4740 0030 | IRQCLEARR | USBSS IRQ_ENABLE_CLR |
| 0x4740 0034 - 0x4740 00FC | - | Reserved |
| 0x4740 0100 | IRQDMATHOLDTX00 | USBSS IRQ_DMA_THRESHOLD_TX0_0 |
| 0x4740 0104 | IRQDMATHOLDTX01 | USBSS IRQ_DMA_THRESHOLD_TX0_1 |
| 0x4740 0108 | IRQDMATHOLDTX02 | USBSS IRQ_DMA_THRESHOLD_TX0_2 |
| 0x4740 010C | IRQDMATHOLDTX03 | USBSS IRQ_DMA_THRESHOLD_TX0_3 |
| 0x4740 0110 | IRQDMATHOLDRX00 | USBSS IRQ_DMA_THRESHOLD_RX0_0 |
| 0x4740 0114 | IRQDMATHOLDRX01 | USBSS IRQ_DMA_THRESHOLD_RX0_1 |
| 0x4740 0118 | IRQDMATHOLDRX02 | USBSS IRQ_DMA_THRESHOLD_RX0_2 |
| 0x4740 011C | IRQDMATHOLDRX03 | USBSS IRQ_DMA_THRESHOLD_RX0_3 |
| 0x4740 0120 | IRQDMATHOLDTX10 | USBSS IRQ_DMA_THRESHOLD_TX1_0 |
| 0x4740 0124 | IRQDMATHOLDTX11 | USBSS IRQ_DMA_THRESHOLD_TX1_1 |
| 0x4740 0128 | IRQDMATHOLDTX12 | USBSS IRQ_DMA_THRESHOLD_TX1_2 |
| 0x4740 012C | IRQDMATHOLDTX13 | USBSS IRQ_DMA_THRESHOLD_TX1_3 |
| 0x4740 0130 | IRQDMATHOLDRX10 | USBSS IRQ_DMA_THRESHOLD_RX1_0 |
| 0x4740 0134 | IRQDMATHOLDRX11 | USBSS IRQ_DMA_THRESHOLD_RX1_1 |
| 0x4740 0138 | IRQDMATHOLDRX12 | USBSS IRQ_DMA_THRESHOLD_RX1_2 |
| 0x4740 013C | IRQDMATHOLDRX13 | USBSS IRQ_DMA_THRESHOLD_RX1_3 |
| 0x4740 0140 | IRQDMAENABLE0 | USBSS IRQ_DMA_ENABLE_0 |
| 0x4740 0144 | IRQDMAENABLE1 | USBSS IRQ_DMA_ENABLE_1 |
| 0x4740 0148 - 0x4740 01FC | - | Reserved |
| 0x4740 0200 | IRQFRAMETHOLDTX00 | USBSS IRQ_FRAME_THRESHOLD_TX0_0 |
| 0x4740 0204 | IRQFRAMETHOLDTX01 | USBSS IRQ_FRAME_THRESHOLD_TX0_1 |
| 0x4740 0208 | IRQFRAMETHOLDTX02 | USBSS IRQ_FRAME_THRESHOLD_TX0_2 |
| 0x4740 020C | IRQFRAMETHOLDTX03 | USBSS IRQ_FRAME_THRESHOLD_TX0_3 |
| 0x4740 0210 | IRQFRAMETHOLDRX00 | USBSS IRQ_FRAME_THRESHOLD_RX0_0 |
| 0x4740 0214 | IRQFRAMETHOLDRX01 | USBSS IRQ_FRAME_THRESHOLD_RX0_1 |
| 0x4740 0218 | IRQFRAMETHOLDRX02 | USBSS IRQ_FRAME_THRESHOLD_RX0_2 |
| 0x4740 021C | IRQFRAMETHOLDRX03 | USBSS IRQ_FRAME_THRESHOLD_RX0_3 |
| 0x4740 0220 | IRQFRAMETHOLDTX10 | USBSS IRQ_FRAME_THRESHOLD_TX1_0 |
| 0x4740 0224 | IRQFRAMETHOLDTX11 | USBSS IRQ_FRAME_THRESHOLD_TX1_1 |
| 0x4740 0228 | IRQFRAMETHOLDTX12 | USBSS IRQ_FRAME_THRESHOLD_TX1_2 |
| 0x4740 022C | IRQFRAMETHOLDTX13 | USBSS IRQ_FRAME_THRESHOLD_TX1_3 |
| 0x4740 0230 | IRQFRAMETHOLDRX10 | USBSS IRQ_FRAME_THRESHOLD_RX1_0 |
| 0x4740 0234 | IRQFRAMETHOLDRX11 | USBSS IRQ_FRAME_THRESHOLD_RX1_1 |
| 0x4740 0238 | IRQFRAMETHOLDRX12 | USBSS IRQ_FRAME_THRESHOLD_RX1_2 |
| 0x4740 023C | IRQFRAMETHOLDRX13 | USBSS IRQ_FRAME_THRESHOLD_RX1_3 |
| 0x4740 0240 | IRQFRAMEENABLE0 | USBSS IRQ_FRAME_ENABLE_0 |
| 0x4740 0244 | IRQFRAMEENABLE1 | USBSS IRQ_FRAME_ENABLE_1 |
| 0x4740 0248 - 0x4740 0FFC | - | Reserved |

**Table 9-113. USB0 Controller Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 1000 | USB0REV | USB0 REVISION |
| 0x4740 1004 - 0x4740 1010 | - | Reserved |
| 0x4740 1014 | USB0CTRL | USB0 Control |


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**Table 9-113. USB0 Controller Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 1018 | USB0STAT | USB0 Status |
| 0x4740 101C | - | Reserved |
| 0x4740 1020 | USB0IRQMSTAT | USB0 IRQ_MERGED_STATUS |
| 0x4740 1024 | USB0IRQEOI | USB0 IRQ_EOI |
| 0x4740 1028 | USB0IRQSTATRAW0 | USB0 IRQ_STATUS_RAW_0 |
| 0x4740 102C | USB0IRQSTATRAW1 | USB0 IRQ_STATUS_RAW_1 |
| 0x4740 1030 | USB0IRQSTAT0 | USB0 IRQ_STATUS_0 |
| 0x4740 1034 | USB0IRQSTAT1 | USB0 IRQ_STATUS_1 |
| 0x4740 1038 | USB0IRQENABLESET0 | USB0 IRQ_ENABLE_SET_0 |
| 0x4740 103C | USB0IRQENABLESET1 | USB0 IRQ_ENABLE_SET_1 |
| 0x4740 1040 | USB0IRQENABLECLR0 | USB0 IRQ_ENABLE_CLR_0 |
| 0x4740 1044 | USB0IRQENABLECLR1 | USB0 IRQ_ENABLE_CLR_1 |
| 0x4740 1048 - 0x4740 106C | - | Reserved |
| 0x4740 1070 | USB0TXMODE | USB0 Tx Mode |
| 0x4740 1074 | USB0RXMODE | USB0 Rx Mode |
| 0x4740 1078 - 0x4740 107C | - | Reserved |
| 0x4740 1080 | USB0GENRNDISEP1 | USB0 Generic RNDIS Size EP1 |
| 0x4740 1084 | USB0GENRNDISEP2 | USB0 Generic RNDIS Size EP2 |
| 0x4740 1088 | USB0GENRNDISEP3 | USB0 Generic RNDIS Size EP3 |
| 0x4740 108C | USB0GENRNDISEP4 | USB0 Generic RNDIS Size EP4 |
| 0x4740 1090 | USB0GENRNDISEP5 | USB0 Generic RNDIS Size EP5 |
| 0x4740 1094 | USB0GENRNDISEP6 | USB0 Generic RNDIS Size EP6 |
| 0x4740 1098 | USB0GENRNDISEP7 | USB0 Generic RNDIS Size EP7 |
| 0x4740 109C | USB0GENRNDISEP8 | USB0 Generic RNDIS Size EP8 |
| 0x4740 10A0 | USB0GENRNDISEP9 | USB0 Generic RNDIS Size EP9 |
| 0x4740 10A4 | USB0GENRNDISEP10 | USB0 Generic RNDIS Size EP10 |
| 0x4740 10A8 | USB0GENRNDISEP11 | USB0 Generic RNDIS Size EP11 |
| 0x4740 10AC | USB0GENRNDISEP12 | USB0 Generic RNDIS Size EP12 |
| 0x4740 10B0 | USB0GENRNDISEP13 | USB0 Generic RNDIS Size EP13 |
| 0x4740 10B4 | USB0GENRNDISEP14 | USB0 Generic RNDIS Size EP14 |
| 0x4740 10B8 | USB0GENRNDISEP15 | USB0 Generic RNDIS Size EP15 |
| 0x4740 10BC - 0x4740 10CC | - | Reserved |
| 0x4740 10D0 | USB0AUTOREQ | USB0 Auto Req |
| 0x4740 10D4 | USB0SRPFIXTIME | USB0 SRP Fix Time |
| 0x4740 10D8 | USB0TDOWN | USB0 Teardown |
| 0x4740 10DC | - | Reserved |
| 0x4740 10E0 | USB0UTMI | USB0 PHY UTMI |
| 0x4740 10E4 | USB0UTMILB | USB0 MGC UTMI Loopback |
| 0x4740 10E8 | USB0MODE | USB0 Mode |
| 0x4740 10E8 - 0x4740 13FF | - | Reserved |
| 0x4740 1400 - 0x4740 159C | - | USB0 Mentor Core Registers |
| 0x4740 15A0 - 0x4740 17FC | - | Reserved |

**Table 9-114. USB1 Controller Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 1800 | USB1REV | USB1 Revision |
| 0x4740 1804 - 0x4740 1810 | - | Reserved |

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**Table 9-114. USB1 Controller Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 1814 | USB1CTRL | USB1 Control |
| 0x4740 1818 | USB1STAT | USB1 Status |
| 0x4740 181C | - | Reserved |
| 0x4740 1820 | USB1IRQMSTAT | USB1 IRQ_MERGED_STATUS |
| 0x4740 1824 | USB1IRQEOI | USB1 IRQ_EOI |
| 0x4740 1828 | USB1IRQSTATRAW0 | USB1 IRQ_STATUS_RAW_0 |
| 0x4740 182C | USB1IRQSTATRAW1 | USB1 IRQ_STATUS_RAW_1 |
| 0x4740 1830 | USB1IRQSTAT0 | USB1 IRQ_STATUS_0 |
| 0x4740 1834 | USB1IRQSTAT1 | USB1 IRQ_STATUS_1 |
| 0x4740 1838 | USB1IRQENABLESET0 | USB1 IRQ_ENABLE_SET_0 |
| 0x4740 183C | USB1IRQENABLESET1 | USB1 IRQ_ENABLE_SET_1 |
| 0x4740 1840 | USB1IRQENABLECLR0 | USB1 IRQ_ENABLE_CLR_0 |
| 0x4740 1844 | USB1IRQENABLECLR1 | USB1 IRQ_ENABLE_CLR_1 |
| 0x4740 1848 - 0x4740 186C | - | Reserved |
| 0x4740 1870 | USB1TXMODE | USB1 Tx Mode |
| 0x4740 1874 | USB1RXMODE | USB1 Rx Mode |
| 0x4740 1878 - 0x4740 187C | - | Reserved |
| 0x4740 1880 | USB1GENRNDISEP1 | USB1 Generic RNDIS Size EP1 |
| 0x4740 1884 | USB1GENRNDISEP2 | USB1 Generic RNDIS Size EP2 |
| 0x4740 1888 | USB1GENRNDISEP3 | USB1 Generic RNDIS Size EP3 |
| 0x4740 188C | USB1GENRNDISEP4 | USB1 Generic RNDIS Size EP4 |
| 0x4740 1890 | USB1GENRNDISEP5 | USB1 Generic RNDIS Size EP5 |
| 0x4740 1894 | USB1GENRNDISEP6 | USB1 Generic RNDIS Size EP6 |
| 0x4740 1898 | USB1GENRNDISEP7 | USB1 Generic RNDIS Size EP7 |
| 0x4740 189C | USB1GENRNDISEP8 | USB1 Generic RNDIS Size EP8 |
| 0x4740 18A0 | USB1GENRNDISEP9 | USB1 Generic RNDIS Size EP9 |
| 0x4740 18A4 | USB1GENRNDISEP10 | USB1 Generic RNDIS Size EP10 |
| 0x4740 18A8 | USB1GENRNDISEP11 | USB1 Generic RNDIS Size EP11 |
| 0x4740 18AC | USB1GENRNDISEP12 | USB1 Generic RNDIS Size EP12 |
| 0x4740 18B0 | USB1GENRNDISEP13 | USB1 Generic RNDIS Size EP13 |
| 0x4740 18B4 | USB1GENRNDISEP14 | USB1 Generic RNDIS Size EP14 |
| 0x4740 18B8 | USB1GENRNDISEP15 | USB1 Generic RNDIS Size EP15 |
| 0x4740 18BC - 0x4740 18CC | - | Reserved |
| 0x4740 18D0 | USB1AUTOREQ | USB1 Auto Req |
| 0x4740 18D4 | USB1SRPFIXTIME | USB1 SRP Fix Time |
| 0x4740 18D8 | USB1TDOWN | USB1 Teardown |
| 0x4740 18DC | - | Reserved |
| 0x4740 18E0 | USB1UTMI | USB1 PHY UTMI |
| 0x4740 18E4 | USB1UTMILB | USB1 MGC UTMI Loopback |
| 0x4740 18E8 | USB1MODE | USB1 Mode |
| 0x4740 18E8 - 0x4740 1BFF | - | Reserved |
| 0x4740 1C00 - 0x4740 1D9C | - | USB1 Mentor Core Registers |
| 0x4740 1DA0 - 0x4740 1FFC | - | Reserved |


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**Table 9-115. CPPI DMA Controller Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 2000 | DMAREVID | Revision |
| 0x4740 2004 | TDFDQ | Teardown Free Descriptor Queue Control |
| 0x4740 2008 | DMAEMU | Emulation Control |
| 0x4740 2010 | DMAMEM1BA | CPPI Mem1 Base Address |
| 0x4740 2014 | DMAMEM1MASK | CPPI Mem1 Mask Address |
| 0x4740 200C - 0x4740 27FF | - | Reserved |
| 0x4740 2800 | TXGCR0 | Tx Channel 0 Global Configuration |
| 0x4740 2804 | - | Reserved |
| 0x4740 2808 | RXGCR0 | Rx Channel 0 Global Configuration |
| 0x4740 280C | RXHPCRA0 | Rx Channel 0 Host Packet Configuration A |
| 0x4740 2810 | RXHPCRB0 | Rx Channel 0 Host Packet Configuration B |
| 0x4740 2814 - 0x4740 281C | - | Reserved |
| 0x4740 2820 | TXGCR1 | Tx Channel 1 Global Configuration |
| 0x4740 2824 | - | Reserved |
| 0x4740 2828 | RXGCR1 | Rx Channel 1 Global Configuration |
| 0x4740 282C | RXHPCRA1 | Rx Channel 1 Host Packet Configuration A |
| 0x4740 2830 | RXHPCRB1 | Rx Channel 1 Host Packet Configuration B |
| 0x4740 2834 - 0x4740 283C | - | Reserved |
| 0x4740 2840 | TXGCR2 | Tx Channel 2 Global Configuration |
| 0x4740 2844 | - | Reserved |
| 0x4740 2848 | RXGCR2 | Rx Channel 2 Global Configuration |
| 0x4740 284C | RXHPCRA2 | Rx Channel 2 Host Packet Configuration A |
| 0x4740 2850 | RXHPCRB2 | Rx Channel 2 Host Packet Configuration B |
| 0x4740 2854 - 0x4740 285F | - | Reserved |
| 0x4740 2860 | TXGCR3 | Tx Channel 3 Global Configuration |
| 0x4740 2864 | - | Reserved |
| 0x4740 2868 | RXGCR3 | Rx Channel 3 Global Configuration |
| 0x4740 286C | RXHPCRA3 | Rx Channel 3 Host Packet Configuration A |
| 0x4740 2870 | RXHPCRB3 | Rx Channel 3 Host Packet Configuration B |
| 0x4740 2880 - 0x4740 2B9F | - | ... |
| 0x4740 2BA0 | TXGCR29 | Tx Channel 29 Global Configuration |
| 0x4740 2BA4 | - | Reserved |
| 0x4740 2BA8 | RXGCR29 | Rx Channel 29 Global Configuration |
| 0x4740 2BAC | RXHPCRA29 | Rx Channel 29 Host Packet Configuration A |
| 0x4740 2BB0 | RXHPCRB29 | Rx Channel 29 Host Packet Configuration B |
| 0x4740 2BB4 - 0x4740 2FFF | - | Reserved |

**Table 9-116. CPPI DMA Scheduler Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 3000 | DMA_SCHED_CTRL | CPPI DMA Scheduler Control Register |
| 0x4740 3804 - 0x4740 38FF | - | Reserved |
| 0x4740 3800 | WORD0 | CPPI DMA Scheduler Table Word 0 |
| 0x4740 3804 | WORD1 | CPPI DMA Scheduler Table Word 1 |
| … | … | … |
| 0x4740 38F8 | WORD62 | CPPI DMA Scheduler Table Word 62 |
| 0x4740 38FC | WORD63 | CPPI DMA Scheduler Table Word 63 |
| 0x4740 38FF - 0x4740 3FFF | - | Reserved |

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**Table 9-117. CPPI DMA Queue Manager Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 4000 | QMGRREVID | Queue Manager Revision |
| 0x4740 4004 | - | Reserved |
| 0x4740 4008 | DIVERSION | Queue Manager Queue Diversion |
| 0x4740 4020 | FDBSC0 | Queue Manager Free Descriptor and Buffer Starvation Count 0 |
| 0x4740 4024 | FDBSC1 | Queue Manager Free Descriptor and Buffer Starvation Count 1 |
| 0x4740 4028 | FDBSC2 | Queue Manager Free Descriptor and Buffer Starvation Count 2 |
| 0x4740 402C | FDBSC3 | Queue Manager Free Descriptor and Buffer Starvation Count 3 |
| 0x4740 4030 | FDBSC4 | Queue Manager Free Descriptor and Buffer Starvation Count 4 |
| 0x4740 4034 | FDBSC5 | Queue Manager Free Descriptor and Buffer Starvation Count 5 |
| 0x4740 4038 | FDBSC6 | Queue Manager Free Descriptor and Buffer Starvation Count 6 |
| 0x4740 403C | FDBSC7 | Queue Manager Free Descriptor and Buffer Starvation Count 7 |
| 0x4740 4030 - 0x4740 407C | - | Reserved |
| 0x4740 4080 | LRAM0BASE | Queue Manager Linking RAM Region 0 Base Address |
| 0x4740 4084 | LRAM0SIZE | Queue Manager Linking RAM Region 0 Size |
| 0x4740 4088 | LRAM1BASE | Queue Manager Linking RAM Region 1 Base Address |
| 0x4740 408C | - | Reserved |
| 0x4740 4090 | PEND0 | Queue Manager Queue Pending 0 |
| 0x4740 4094 | PEND1 | Queue Manager Queue Pending 1 |
| 0x4740 4098 | PEND2 | Queue Manager Queue Pending 2 |
| 0x4740 409C | PEND3 | Queue Manager Queue Pending 3 |
| 0x4740 40A0 | PEND4 | Queue Manager Queue Pending 4 |
| 0x4740 40A4 - 0x4740 4FFF | - | Reserved |
| 0x4740 5000 + 16xR | QMEMRBASEr | Memory Region R Base Address (R ranges from 0 to 15) |
| 0x4740 5000 + 16xR + 4 | QMEMRCTRLr | Memory Region R Control (R ranges from 0 to 15) |
| 0x4740 50F8 - 0x4740 5FFF | - | Reserved |
| 0x4740 6000 + 16xN | CTRLAn | Queue N Register A (N ranges from 0 to 155) |
| 0x4740 6004 + 16xN | CTRLBn | Queue N Register B (N ranges from 0 to 155) |
| 0x4740 6008 + 16xN | CTRLCn | Queue N Register C (N ranges from 0 to 155) |
| 0x4740 600C + 16xN | CTRLDn | Queue N Register D (N ranges from 0 to 155) |
| 0x4740 69C0 - 0x4740 6FFF | - | Reserved |
| 0x4740 7000 + 16xN | QSTATAn | Queue N Status A (N ranges from 0 to 155) |
| 0x4740 7004 + 16xN | QSTATBn | Queue N Status B (N ranges from 0 to 155) |
| 0x4740 7008 + 16xN | QSTATCn | Queue N Status C (N ranges from 0 to 155) |
| 0x4740 700C + 16xN | - | Reserved |
| 0x4740 79C0 - 0x4740 7FFF | - | Reserved |


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### 9.21.2 USB2.0 Electrical Data and Timing

**Table 9-118. Switching Characteristics Over Recommended Operating Conditions for USB2.0**

(see Figure 9-90)

| NO. | PARAMETER | | LOW SPEED 1.5 Mbps | | FULL SPEED 12 Mbps | | HIGH SPEED 480 Mbps | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{r(D)}$ | Rise time, USB_DP and USB_DN signals(1) | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 2 | $t_{f(D)}$ | Fall time, USB_DP and USB_DN signals(1) | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 3 | $t_{rfM}$ | Rise and Fall time, matching(2) | 80 | 125 | 90 | 111.11 | – | – | % |
| 4 | $V_{CRS}$ | Output signal cross-over voltage(1) | 1.3 | 2 | 1.3 | 2 | – | – | V |
| 5 | $t_{jr(source)NT}$ | Source (Host) Driver jitter, next transition | | 2 | | 2 | | (3) | ns |
| | $t_{jr(FUNC)NT}$ | Function Driver jitter, next transition | | 25 | | 2 | | (3) | ns |
| 6 | $t_{jr(source)PT}$ | Source (Host) Driver jitter, paired transition(4) | | 1 | | 1 | | (3) | ns |
| | $t_{jr(FUNC)PT}$ | Function Driver jitter, paired transition | | 10 | | 1 | | (3) | ns |
| 7 | $t_{w(EOPT)}$ | Pulse duration, EOP transmitter | 1250 | 1500 | 160 | 175 | – | – | ns |
| 8 | $t_{w(EOPR)}$ | Pulse duration, EOP receiver | 670 | | 82 | | – | | ns |
| 9 | $t_{(DRATE)}$ | Data Rate | | 1.5 | | 12 | | 480 | Mb per s |
| 10 | $Z_{DRV}$ | Driver Output Resistance | – | – | 28 | 49.5 | 40.5 | 49.5 | Ω |
| 11 | USB_R1 | USB reference resistor | 43.8 | 44.6 | 43.8 | 44.6 | 43.8 | 44.6 | Ω |

(1) Low Speed: $C_L$ = 200 pF, Full Speed: $C_L$ = 50 pF, High Speed: $C_L$ = 50 pF
(2) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(3) For more detailed information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7, *Electrical*.
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$

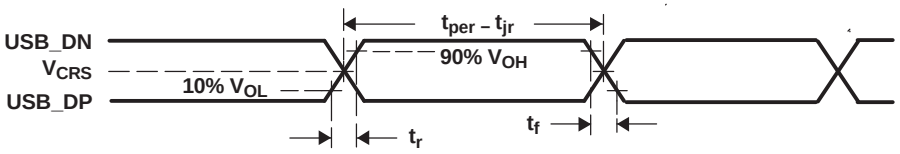
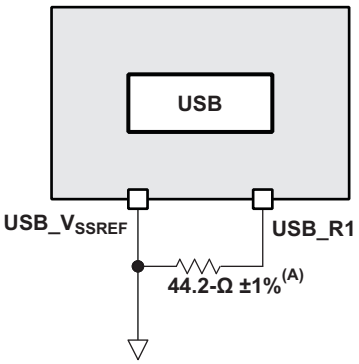



**Figure 9-90. USB2.0 Integrated Transceiver Interface Timing**




A. Place the 44.2-Ω ± 1% as close to the device as possible.

**Figure 9-91. USB Reference Resistor Routing**

# 10 Device and Documentation Support

## 10.1 Device Support

### *10.1.1 Development Support*

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of TMS320DM816x processor applications:

**Software Development Tools:** Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++ and Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software DSP/BIOS™, which provides the basic run-time target software needed to support any DaVinci Video Processor application.

**Hardware Development Tools:** Extended Development System ( XDS™) Emulator

For a complete listing of development-support tools for the DM816x DaVinci™ Video Processor platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

### *Device and Development Support-Tool Nomenclature*

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, TMS320DM8168CYG). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

**TMP** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

**TMS** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.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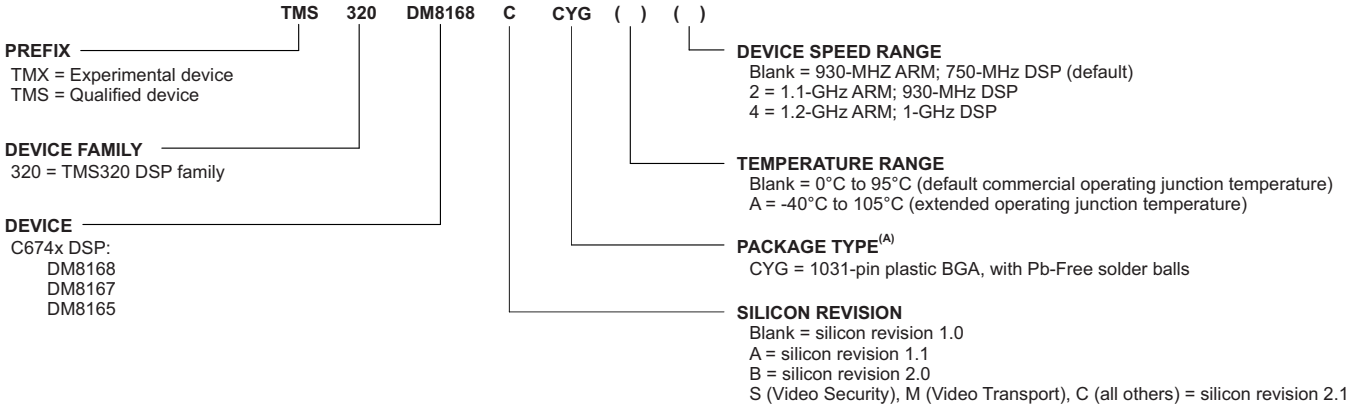
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, CYG), the temperature range (for example, blank is the default commercial operating junction temperature range), and the device speed range (for example, blank is the default [930-MHz ARM, 750-MHz DSP]).
Figure 10-1 provides a legend for reading the complete device name for any TMS320DM816x device. For a comparison of device features, see Table 3-1.

For device part numbers and further ordering information of TMS320DM816x devices in the CYG package type, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320DM816x DaVinci Digital Media Processors Silicon Errata* (literature number SPRZ329).




A. BGA = Ball-Grid Array.

**Figure 10-1. Device Nomenclature**

### *10.1.2 Device Speed Range Overview*

Table 10-1 specifies all clock frequencies with respect to device speed range.

**Table 10-1. Device Speed Ranges**

| PART NUMBER | ARM (MHz) | DSP (MHz) | HDVICP2 (MHz) | SGX530 (MHz) | Media Controller (M3) (MHz) | DDR3 (MTps) | DDR2 (MTps) | EMIF (MHz) | DMM (MHz) |
|---|---|---|---|---|---|---|---|---|---|
| CYG | 930 | 750 | 500 | 310 | 230 | 1600 | 1066 | 400 | 364 |
| CYG2 | 1100 | 930 | 550 | 275 | 275 | 1600 | 1066 | 400 | 364 |
| CYGA2 | | | | | | | | | |
| CYG4 | 1200 | 1000 | 630 | 300 | 285 | 1600 | 1066 | 400 | 425 |

## 10.2 Documentation Support

The following documents describe the DM816x DaVinci™ Video Processors. Copies of these documents are available on the Internet at www.ti.com. Tip: Enter the literature number in the search box.

**SPRUGX8** ***TMS320DM816x Digital Media Processors Technical Reference Manual*** details the integrations, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

**SPRZ329** ***TMS320DM816x DaVinci™ Digital Media Processors*** describes the usage notes and known exceptions to the functional specifications for the device.

**SPRABK6** ***DM816xx Easy CYG Package PCB Escape Routing.***

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## 10.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 10-2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TMS320DM8168 | Click here | Click here | Click here | Click here | Click here |
| TMS320DM8167 | Click here | Click here | Click here | Click here | Click here |
| TMS320DM8165 | Click here | Click here | Click here | Click here | Click here |

## 10.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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## 10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.


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# 11 Mechanical Packaging and Orderable Information

## 11.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS320DM8165SCYG | NRND | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 0 | TMS320 DM8165SCYG | |
| TMS320DM8165SCYG2 | NRND | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 0 | TMS320 DM8165SCYG 2 | |
| TMS320DM8165SCYG4 | NRND | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 0 | TMS320 DM8165SCYG 4 | |
| TMS320DM8167SCYG | NRND | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 0 | TMS320 DM8167SCYG | |
| TMS320DM8167SCYG2 | NRND | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 0 | TMS320 DM8167SCYG 2 | |
| TMS320DM8167SCYG4 | NRND | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 0 | TMS320 DM8167SCYG 4 | |
| TMS320DM8168CCYG | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 95 | TMS320 DM8168CCYG | Samples |
| TMS320DM8168CCYG2 | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 95 | TMS320 DM8168CCYG 2 | Samples |
| TMS320DM8168CCYG4 | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 95 | TMS320 DM8168CCYG 4 | Samples |
| TMS320DM8168CCYGA2 | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | -40 to 105 | TMS320 DM8168CCYG A2 | Samples |
| TMS320DM8168CCYGH | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 95 | TMS320 DM8168CCYGH | Samples |
| TMS320DM8168SCYG | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 95 | TMS320 DM8168SCYG | Samples |
| TMS320DM8168SCYG2 | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 95 | TMS320 DM8168SCYG 2 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS320DM8168SCYG4 | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | 0 to 95 | TMS320 DM8168SCYG 4 | Samples |
| TMS320DM8168SCYGA2 | ACTIVE | FCBGA | CYG | 1031 | 44 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-245C-72HR | -40 to 105 | TMS320 DM8168SCYG A2 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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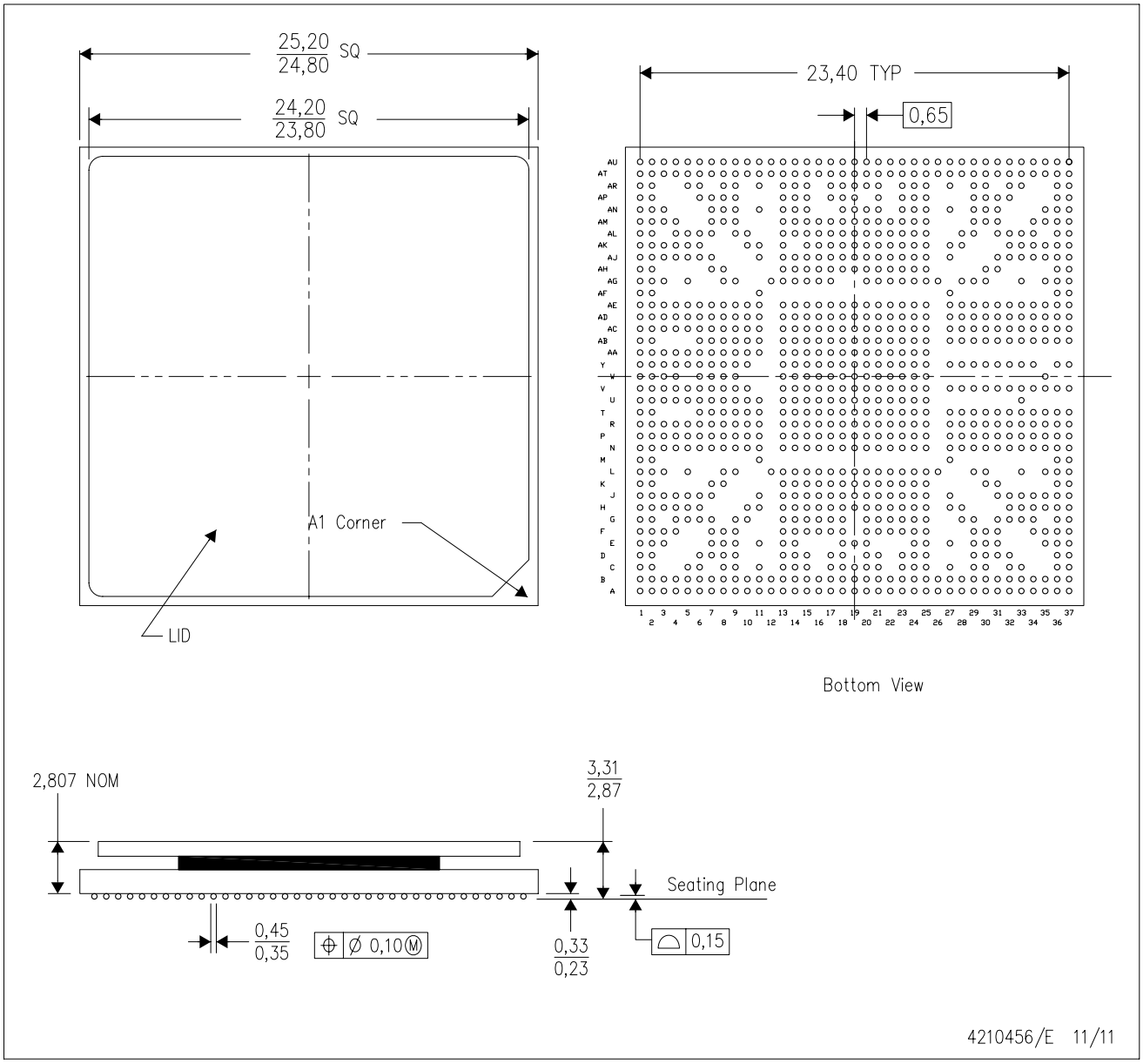
CYG (S–PBGA–N1031) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Thermally enhanced package with a lid.
D. Flip chip application only.
E. Pb–free die bump and solder ball.

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