THE DATASHEET OF

TPS73133MDBVREP

CAP-FREE NMOS 150 mA LOW DROPOUT REGULATOR WITH REVERSE CURRENT PROTECTION

FEATURES

- **Controlled Baseline**
  - **One Assembly**
  - **Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Stable With No Output Capacitor or Any Value or Type of Capacitor**
- **Input Voltage Range of 1.7 V to 5.5 V**
- **Ultralow Dropout Voltage: 30 mV Typical**
- **Excellent Load Transient Response—With or Without Optional Output Capacitor**
- **New NMOS Topology Provides Low Reverse Leakage Current**
- **Low Noise: 30 μV_{RMS} Typ (10 kHz to 100 kHz)**
- **0.5% Initial Accuracy**
- **1% Overall Accuracy Over Line, Load, and Temperature**
- **Less Than 1 µA Maximum I_Q in Shutdown Mode**
- **Thermal Shutdown and Specified Min/Max Current Limit Protection**
- **Available in Multiple Output Voltage Versions**
  - **Fixed Outputs of 1.2 V to 5 V**
  - **Adjustable Outputs from 1.2 V to 5.5 V**
  - **Custom Outputs Available**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

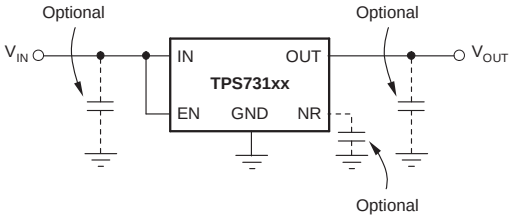
APPLICATIONS

- **Portable/Battery-Powered Equipment**
- **Post-Regulation for Switching Supplies**
- **Noise-Sensitive Circuitry such as VCOs**
- **Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors**

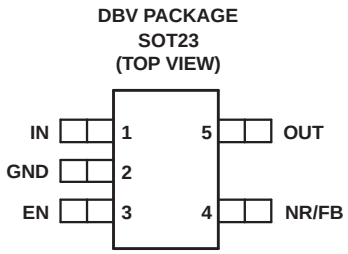
DESCRIPTION/ORDERING INFORMATION

The TPS731xx family of low-dropout (LDO) linear voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS731xx uses an advanced BiCMOS process to yield high precision while delivering low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 µA and ideal for portable applications. The low output noise (30 μV_{RMS} with 0.1 µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.



Typical Application Circuit for Fixed-Voltage Versions



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS731**xx**M**yyyz**EP	**XX** is nominal output voltage (for example, 25 = 2.5 V, 01 = Adjustable(3)). **YYY** is package designator. **Z** is package quantity.

(1) For the most current specification and package information, see the Package Option Addendum located at the end of this data sheet or see the Texas Instruments website at www.ti.com.
(2) Output voltages from 1.3 V to 4 V in 100 mV increments are available through the use of innovative factory EEPROM programming. Minimum order quantities apply; contact factory for details and availability.
(3) For fixed 1.2 V operation, tie FB to OUT

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT23 - DBV	TPS73101MDBVREP	PKAM
		TPS73115MDBVREP	PKBM
		TPS731125MDBVREP	PMMM
		TPS73118MDBVREP	PKCM
		TPS73125MDBVREP	PKDM
		TPS73130MDBVREP	PKEM
		TPS73132MDBVREP	PKFM
		TPS73133MDBVREP	PKHM
		TPS73150MDBVREP	PKIM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted(1)

V_{IN} range	–0.3 V to 6 V
V_{EN} range	–0.3 V to 6 V
V_{OUT} range	–0.3 V to 5.5 V
Peak output current	Internally limited
Output short-circuit duration	Indefinite
Continuous total power dissipation	See *Power Dissipation Ratings Table*
Ambient temperature range, T_A	–55°C to 150°C
Storage temperature range	–65°C to 150°C
ESD rating, HBM	2 kV
ESD rating, CDM	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS(1)

BOARD	PACKAGE	$R_{\Theta JC}$	$R_{\Theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
Low-K(2)	DBV	64°C/W	255°C/W	3.9 mW/°C	450 mW	275 mW	215 mW	58 mW
High-K (3)	DBV	64°C/W	180°C/W	5.6 mW/°C	638 mW	388 mW	305 mW	83 mW

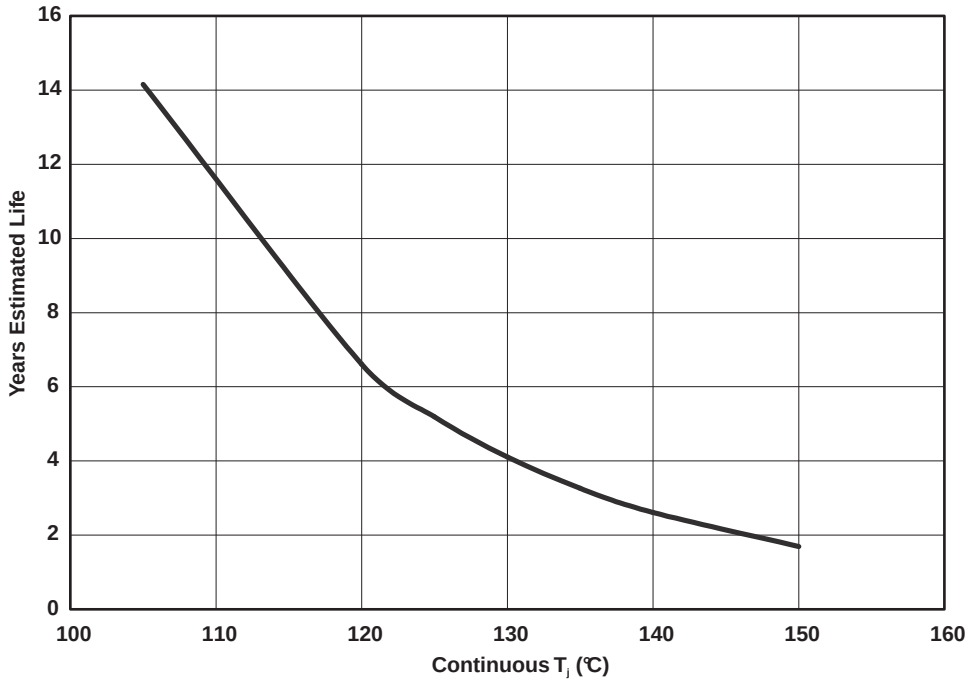
(1) See *Power Dissipation* in the *Application Information* section for more information related to thermal design.
(2) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch × 3 inch, two-layer board with 2-ounce copper traces on top of the board.
(3) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_A = –55°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			1.7		5.5	V
V_{FB}	Internal reference (TPS73101)		T_A = 25°C	1.198	1.2	1.21	V
V_{OUT}	Output voltage range (TPS73101)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1)	Nominal	T_A = 25°C		±0.5		%
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 150 mA	–1	±0.5	+1	%
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation(1)		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1 mA ≤ I_{OUT} ≤ 150 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 150 mA		0.0005		
V_{DO}	Dropout voltage(2) (V_{IN} = V_{OUT} (nom) – 0.1 V)		I_{OUT} = 150 mA		30	100	mV
Z_O(DO)	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	150	360	500	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		200		mA
I_{REV}	Reverse leakage current(3) (–I_{IN})		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1	15	µA
I_{GND}	Ground pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 150 mA		550	750	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5		0.02	1	µA
I_{FB}	FB pin current (TPS73101)				0.1	0.475	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 150 mA		58		dB
			f = 10 kHz, I_{OUT} = 150 mA		37		
V_N	Output noise voltage BW = 10 Hz to 100 kHz		C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 3 V, R_L = 30Ω, C_{OUT} = 1 µF, C_{NR} = 0.01 µF		600		µs
V_{EN}(HI)	Enable high (enabled)			1.7		V_{IN}	V
V_{EN}(LO)	Enable low (shutdown)			0		0.5	V
I_{EN}(HI)	Enable pin current (enabled)		V_{EN} = 5.5 V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature		Shutdown, Temperature increasing		160		°C
			Reset, Temperature decreasing		140		
T_A	Operating ambient temperature			–55		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) V_{DO} is not measured for the TPS73115 ($V_{O(nom)}$ = 1.5 V) and TPS731125 ($V_{O(nom)}$ = 1.25 V) since minimum V_{IN} = 1.7 V.
(3) Fixed-voltage versions only; see the ***Applications Infomation*** section for more information.



A. $T_j = \theta_{JA} \times W + T_A$ (at standard JESD 51 conditions)

Figure 1. Estimated Device Life at Elevated Temperatures Electromigration Fail Mode

FUNCTIONAL BLOCK DIAGRAMS

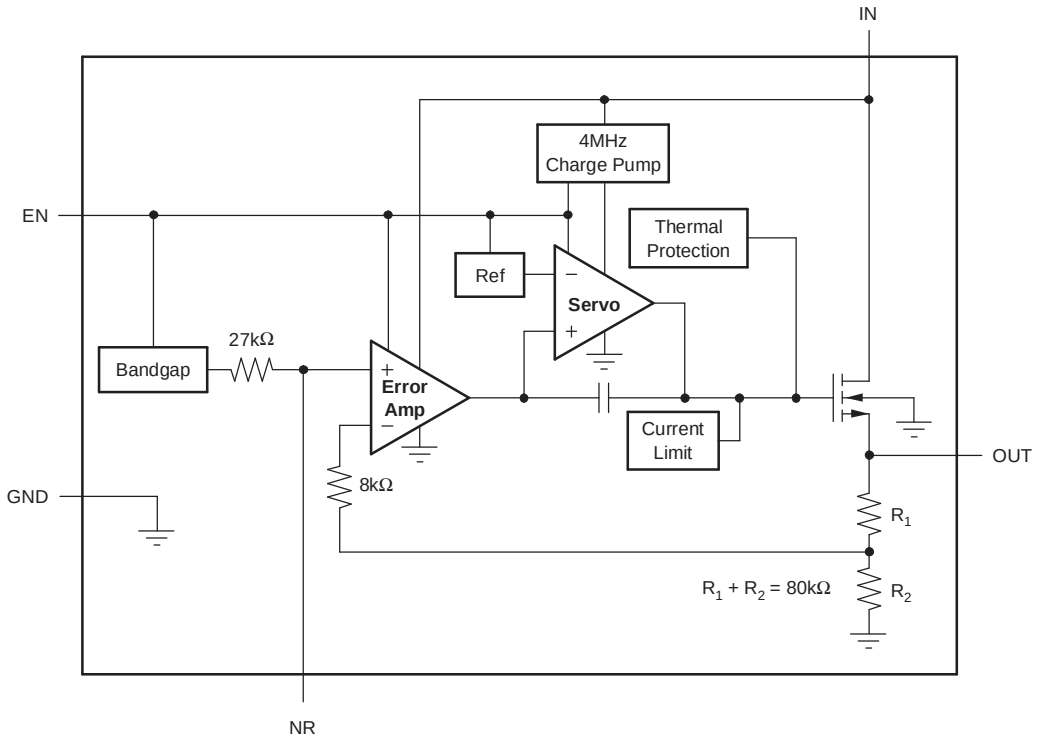


Figure 2. Fixed Voltage Version

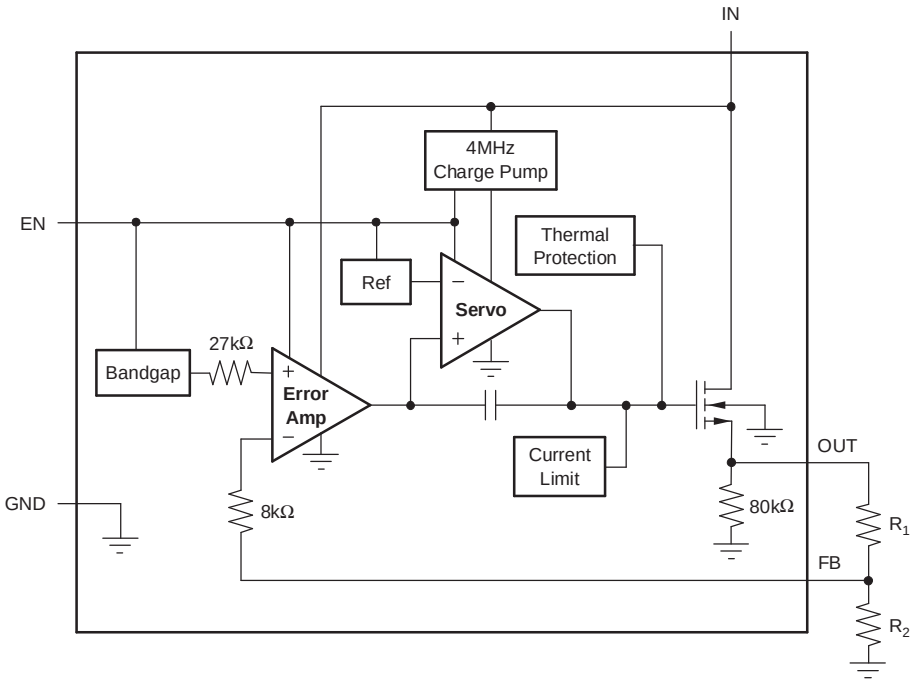


Figure 3. Adjustable Voltage Version

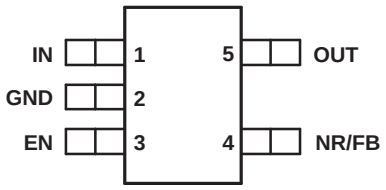
Table 1. Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ
5.0V	78.7kΩ	24.9kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

PIN ASSIGNMENTS

DBV PACKAGE
SOT23
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	SOT23 (DBV) PIN NO.	
IN	1	Unregulated input supply
GND	2	Ground
EN	3	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the *Shutdown* section under *Application Information* for more details. EN can be connected to IN if not used.
NR	4	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	4	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	Output of the regulator. There are no output capacitor requirements for stability.

TYPICAL CHARACTERISTICS

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

LOAD REGULATION

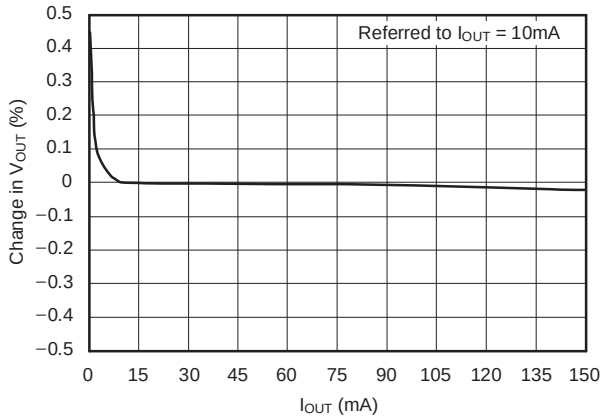


Figure 4.

LINE REGULATION

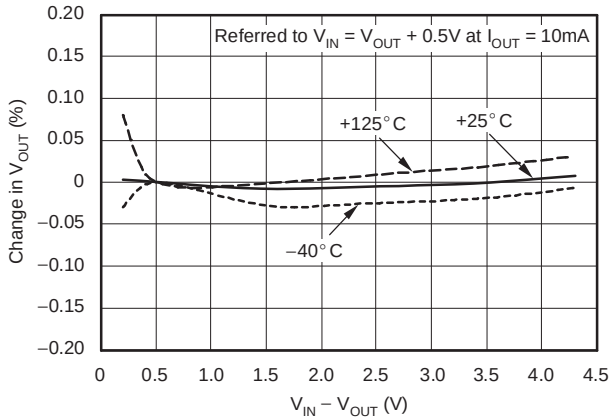


Figure 5.

DROPOUT VOLTAGE vs OUTPUT CURRENT

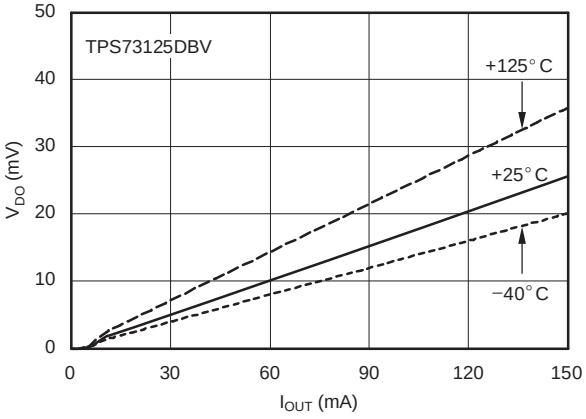


Figure 6.

DROPOUT VOLTAGE vs TEMPERATURE

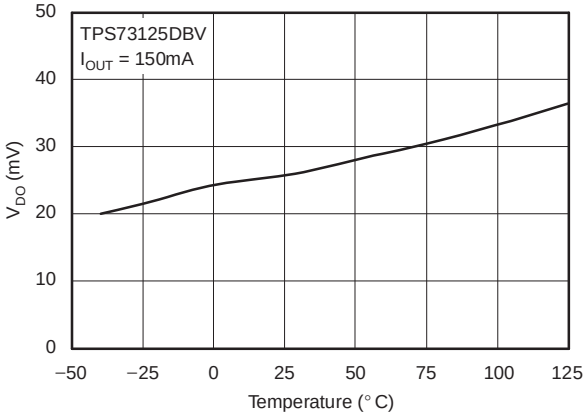


Figure 7.

OUTPUT VOLTAGE ACCURACY HISTOGRAM

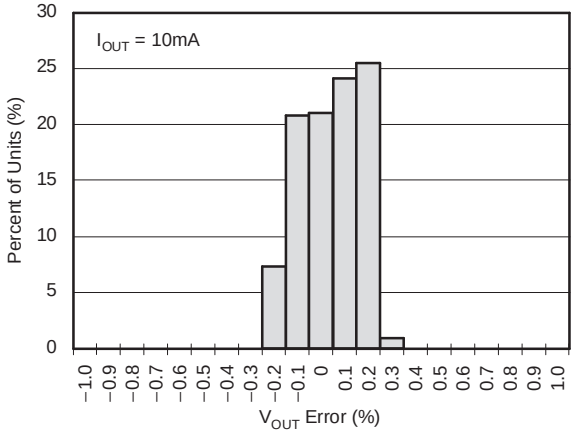


Figure 8.

OUTPUT VOLTAGE DRIFT HISTOGRAM

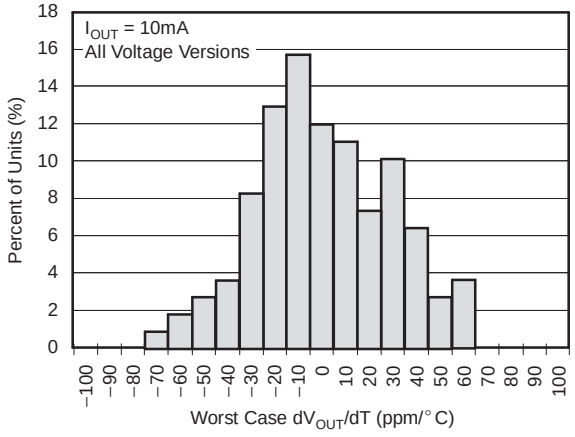


Figure 9.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J= 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

GROUND PIN CURRENT vs OUTPUT CURRENT

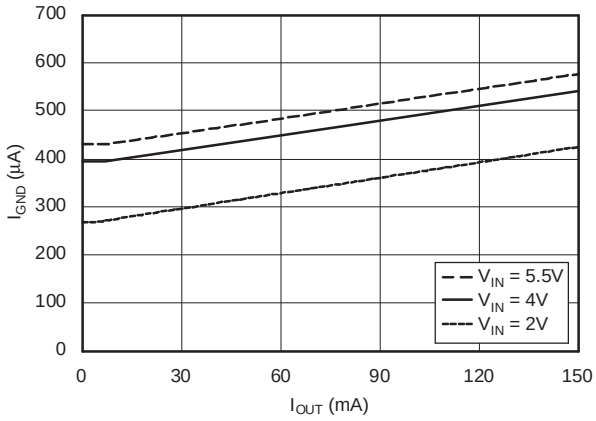


Figure 10.

GROUND PIN CURRENT vs TEMPERATURE

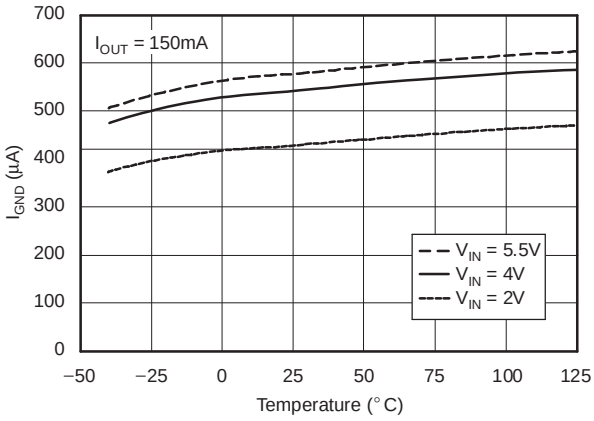


Figure 11.

CURRENT LIMIT vs V_{OUT} (FOLDBACK)

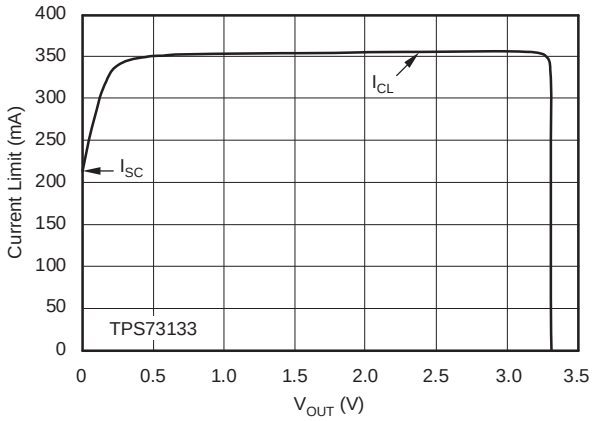


Figure 12.

GROUND PIN CURRENT in SHUTDOWN vs TEMPERATURE

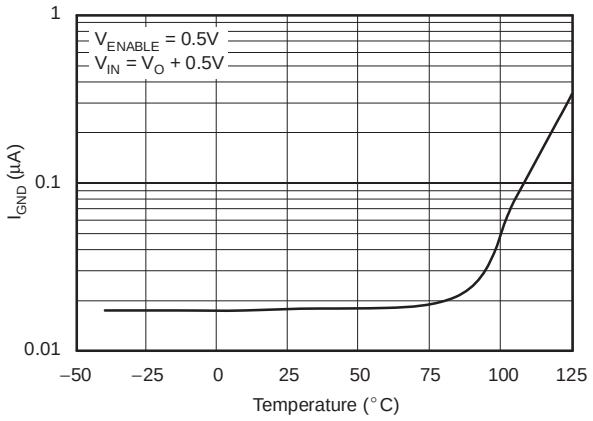


Figure 13.

CURRENT LIMIT vs V_{IN}

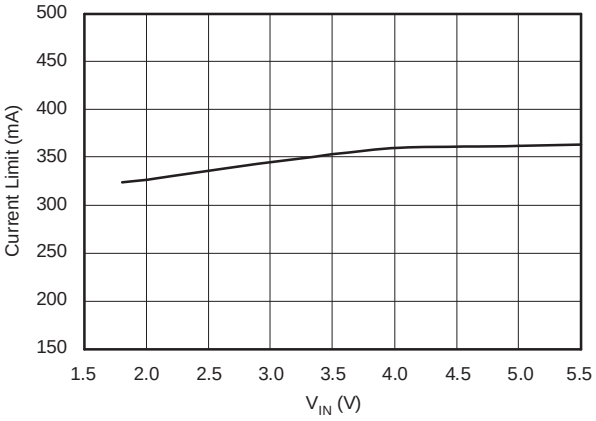


Figure 14.

CURRENT LIMIT vs TEMPERATURE

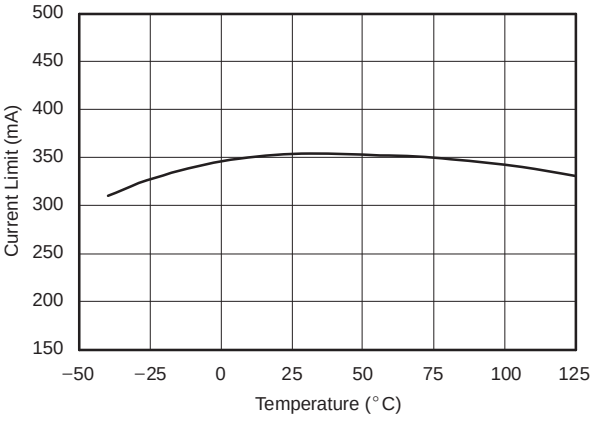


Figure 15.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J= 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

PSRR (RIPPLE REJECTION) vs FREQUENCY

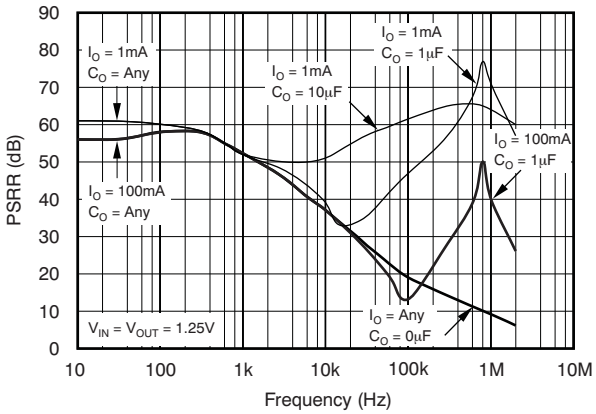


Figure 16.

PSRR (RIPPLE REJECTION) vs $V_{IN} - V_{OUT}$

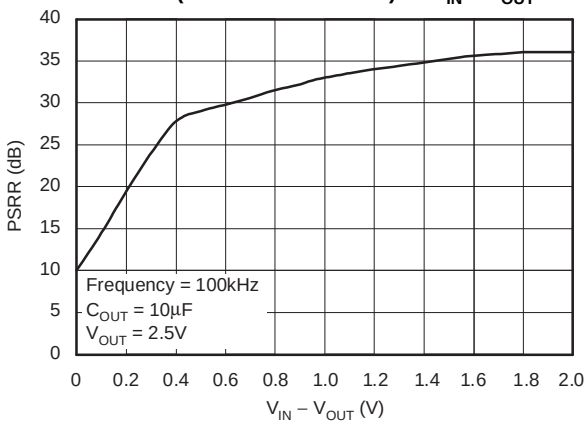


Figure 17.

NOISE SPECTRAL DENSITY
C_{NR} = 0 µF

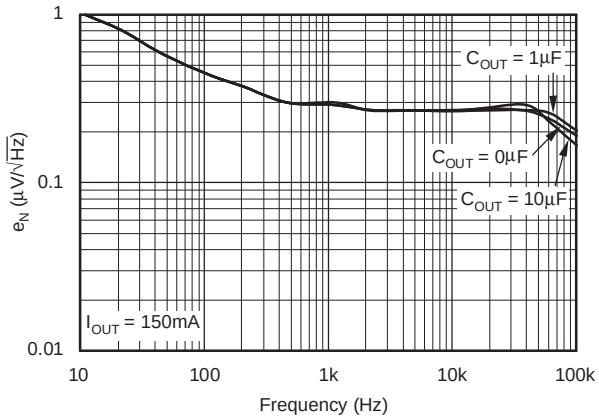


Figure 18.

NOISE SPECTRAL DENSITY
C_{NR} = 0.01 µF

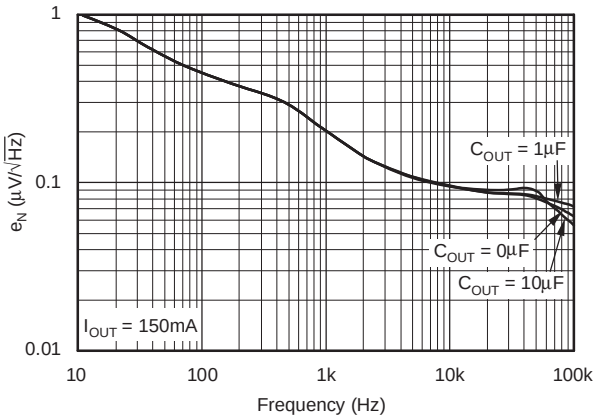


Figure 19.

RMS NOISE VOLTAGE vs C_{OUT}

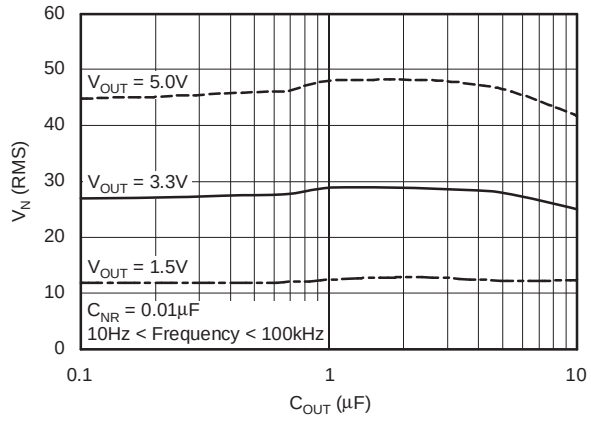


Figure 20.

RMS NOISE VOLTAGE vs C_{NR}

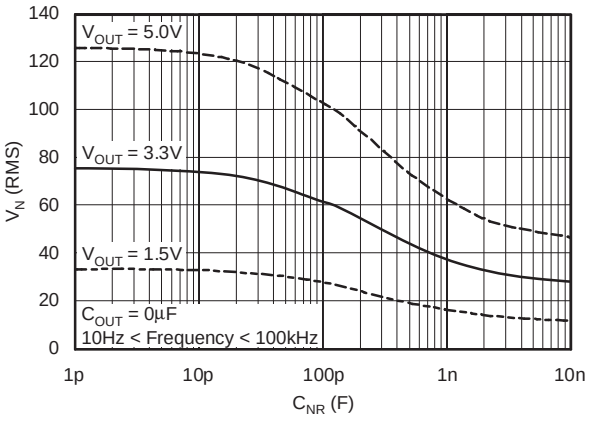


Figure 21.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

TPS73133
LOAD TRANSIENT RESPONSE

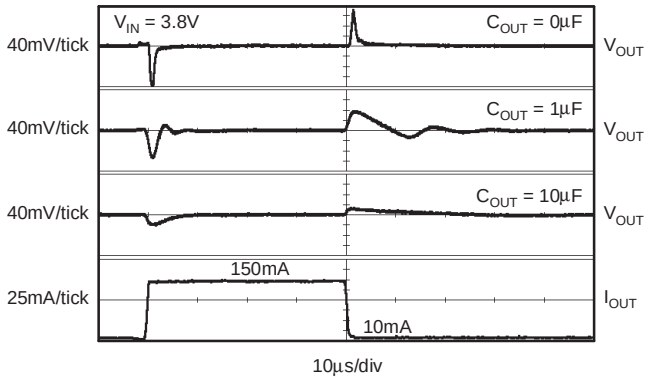


Figure 22.

TPS73133
LINE TRANSIENT RESPONSE

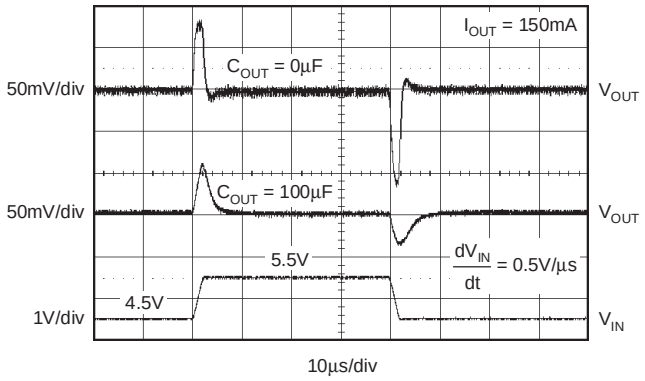


Figure 23.

TPS73133
TURN-ON RESPONSE

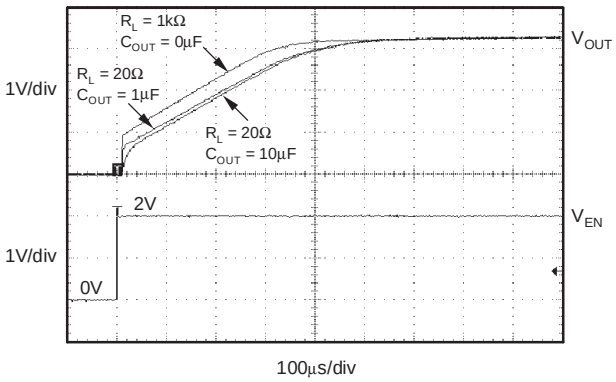


Figure 24.

TPS73133
TURN-OFF RESPONSE

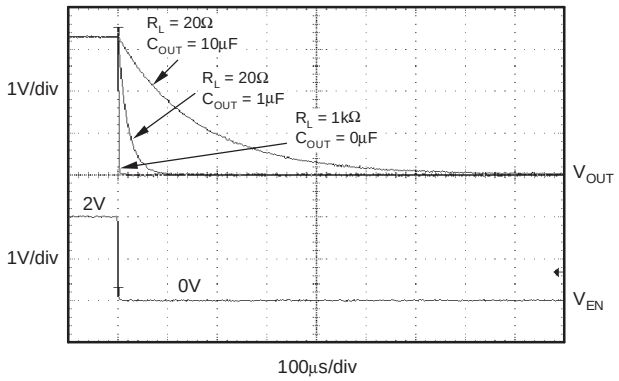


Figure 25.

TPS73133
POWER UP / POWER DOWN

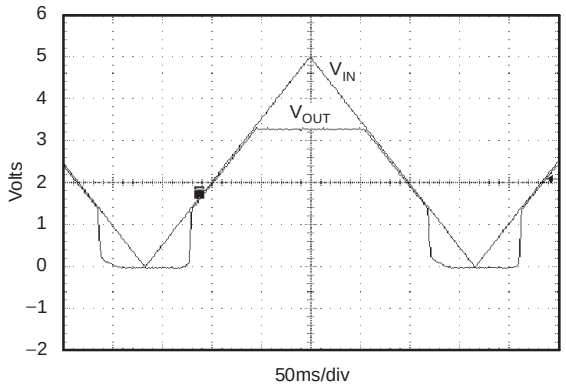


Figure 26.

I_{ENABLE} vs TEMPERATURE

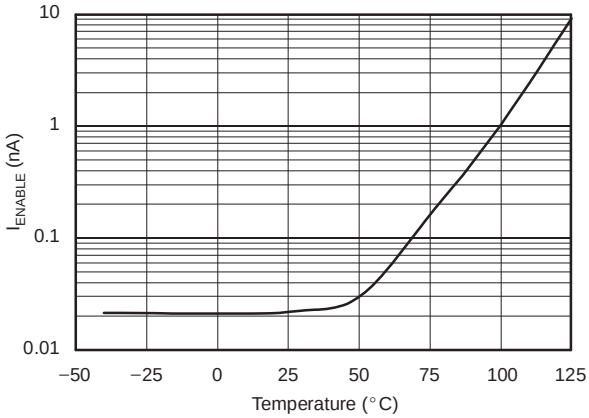


Figure 27.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J= 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

TPS73101
RMS NOISE VOLTAGE vs C_{ADJ}

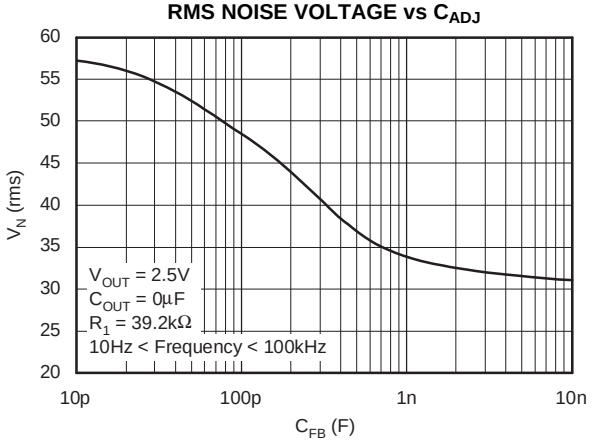


Figure 28.

TPS73101
I_{FB} vs TEMPERATURE

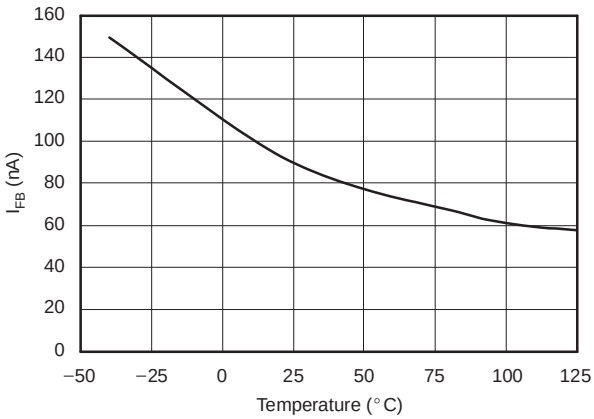


Figure 29.

TPS73101
LOAD TRANSIENT, ADJUSTABLE VERSION

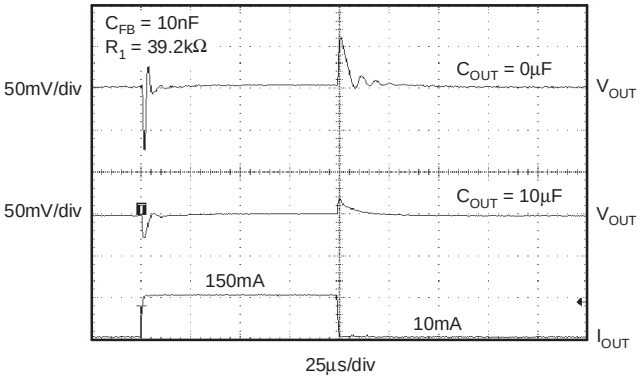


Figure 30.

TPS73101
LINE TRANSIENT, ADJUSTABLE VERSION

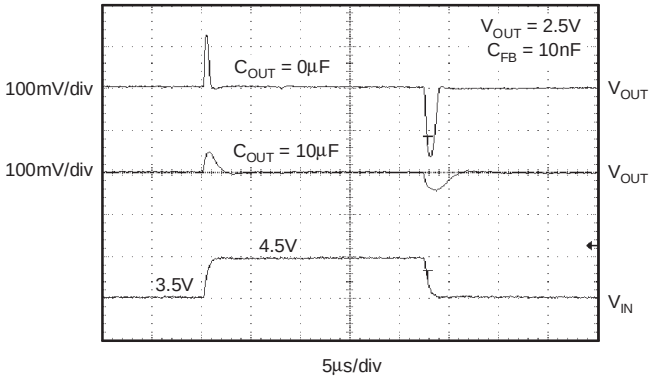


Figure 31.

APPLICATION INFORMATION

The TPS731xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS731xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 32 shows the basic circuit connections for the fixed voltage models. Figure 33 gives the connections for the adjustable output version (TPS73101).

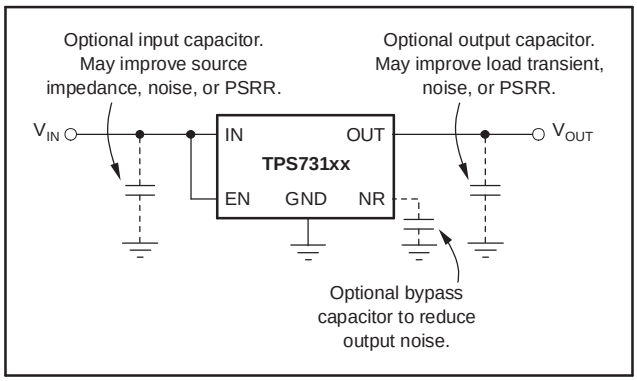


Figure 32. Typical Application Circuit for Fixed-Voltage Versions

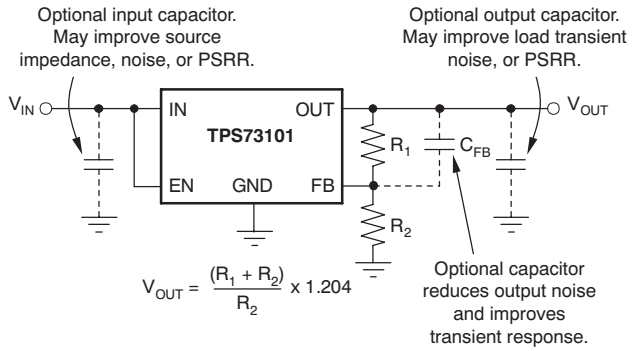


Figure 33. Typical Application Circuit for Adjustable-Voltage Versions

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 33. Sample resistor values for common output voltages are shown in Figure 3. For the best accuracy, make the parallel combination of R_1 and R_2 approximately 19 kΩ.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1 µF to 1 µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS731xx does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where $V_{IN} - V_{OUT} < 0.5$ V and multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

OUTPUT NOISE

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS731xx and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2 V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27 kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10 Hz to 100 kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10nF.

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in the *Typical Characteristics* section.

The TPS73101 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the FB pin reduces output noise and improves load transient performance.

The TPS731xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates ~250 μV of switching noise at ~4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TPS731xx internal current limit helps protect the regulator during fault conditions. Foldback current helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 12 in the **Typical Characteristics** section for a graph of I_{OUT} vs V_{OUT}.

SHUTDOWN

The Enable pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5 V (max) turns the regulator off and drops the ground pin current to approximately 10 nA. When shutdown capability is not required, the Enable pin can be connected to V_{IN}. When a pullup resistor is used and operation down to 1.8 V is required, use pullup resistor values below 50 kΩ.

DROPOUT VOLTAGE

The TPS731xx uses an NMOS pass transistor to achieve extremely low dropout. When ($V_{IN} – V_{OUT}$) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the R_{DS-ON} of the NMOS pass element.

For large step changes in load current, the TPS731xx requires a larger voltage drop across it to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of $V_{IN} – V_{OUT}$ above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions (full-scale instantaneous load change with ($V_{IN} – V_{OUT}$) close to dc dropout levels), the TPS731xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

TRANSIENT RESPONSE

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 μF) from the output pin to ground reduces undershoot magnitude but increases duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the output to the adjust pin also improves the transient response.

The TPS731xx does not have active pulldown when the output is overvoltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

REVERSE CURRENT

The NMOS pass element of the TPS731xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80-kΩ internal resistor divider to ground (see Figure 2 and Figure 3).

For the TPS73101, reverse current may flow when V_{FB} is more than 1 V above V_{IN}.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS731xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS731xx into thermal shutdown will degrade device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low-K and high-K boards are shown in the *Power Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$

Power dissipation can be minimized by using the lowest possible input voltage necessary to ensure the required output voltage.

Package Mounting

Solder pad footprint recommendations for the TPS731xx are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (AB-132), available from the Texas Instruments web site at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73101MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKAM	Samples
TPS731125MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PMMM	Samples
TPS73115MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKBM	Samples
TPS73118MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKCM	Samples
TPS73125MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKDM	Samples
TPS73130MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKEM	Samples
TPS73132MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKFM	Samples
TPS73133MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKHM	Samples
TPS73150MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKIM	Samples
V62/06652-01XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKAM	Samples
V62/06652-02XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKBM	Samples
V62/06652-03XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKCM	Samples
V62/06652-04XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKDM	Samples
V62/06652-05XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKEM	Samples
V62/06652-06XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKFM	Samples
V62/06652-07XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKHM	Samples
V62/06652-08XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKIM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
V62/06652-09XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	PMMM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

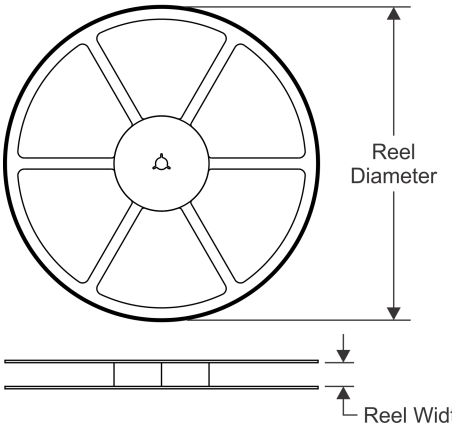
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

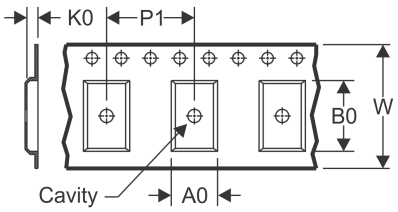
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

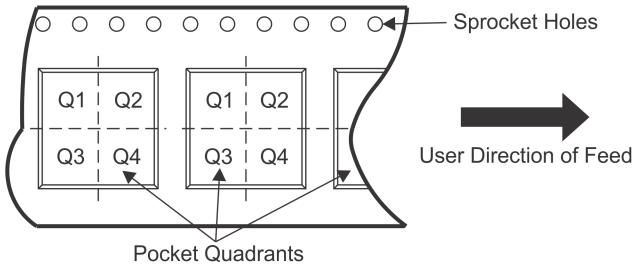


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

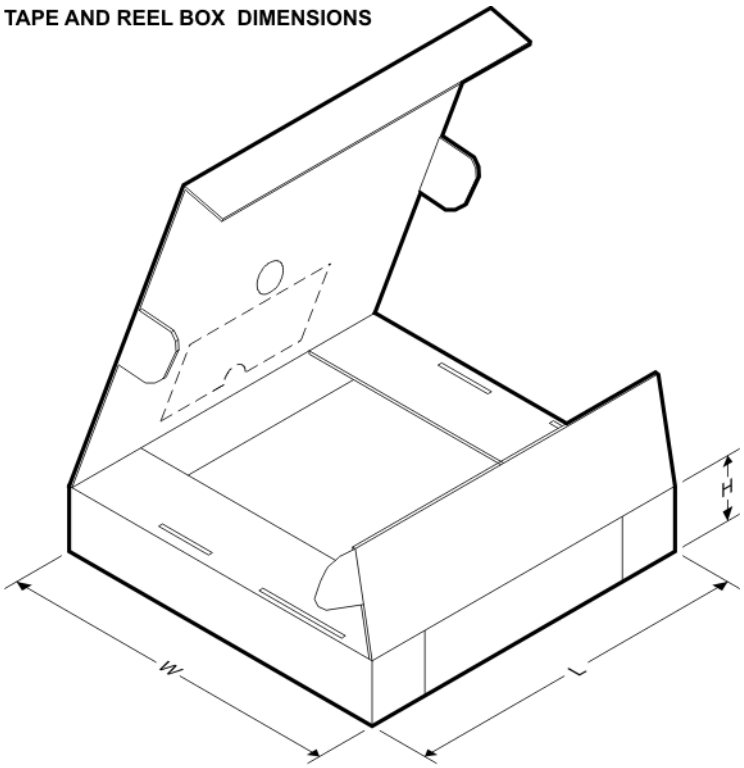
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73101MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS731125MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73115MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73118MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73125MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73130MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73132MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73133MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73150MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

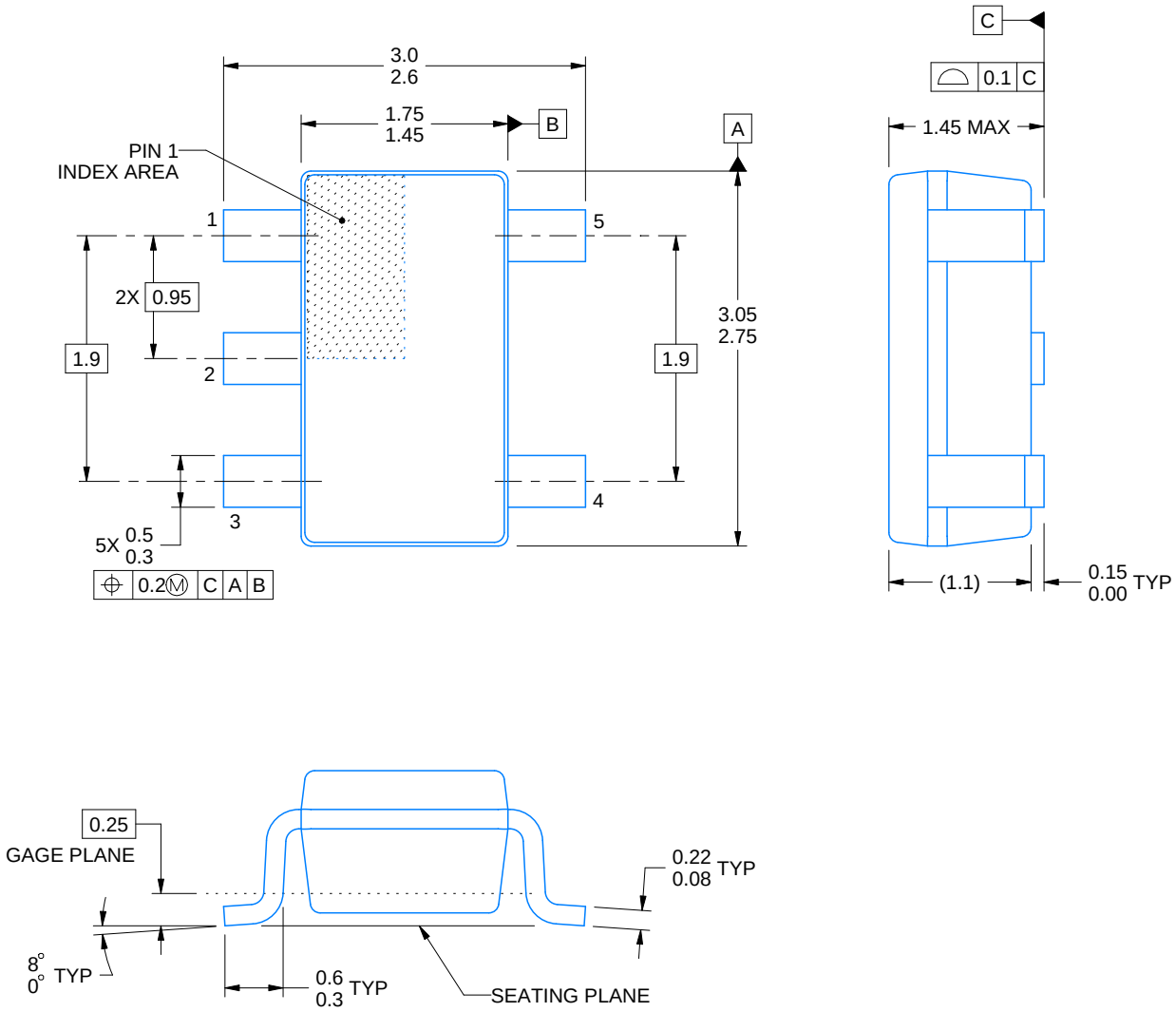
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73101MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS731125MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73115MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73118MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73125MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73130MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73132MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73133MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73150MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

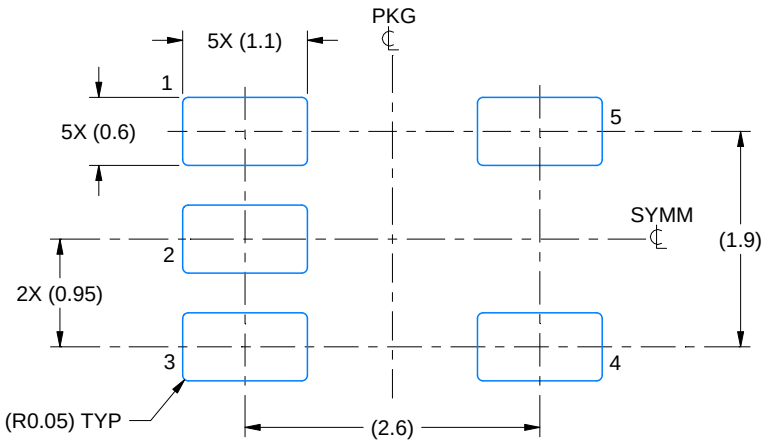
SMALL OUTLINE TRANSISTOR



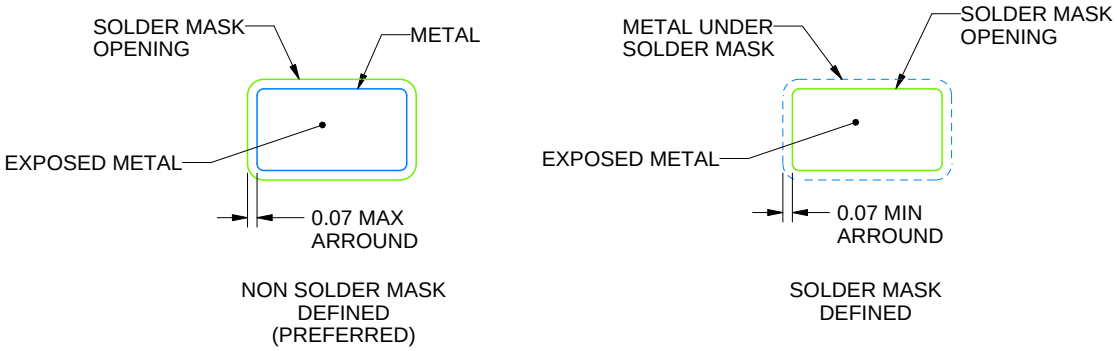
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

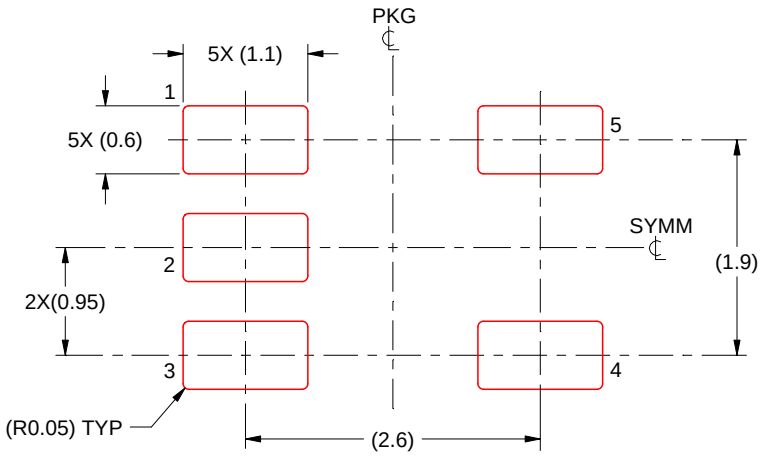


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View TPS73133MDBVREP on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management