THE DATASHEET OF

AD7173-8BCPZ

Low Power, 8-/16-Channel, 31.25 kSPS, 24-Bit, Highly Integrated Sigma-Delta ADC

Data Sheet **AD7173-8**

FEATURES

- Low power, 8-/16-channel, highly integrated multiplexed analog-to-digital converter (ADC)
- Integration
  - Precision analog input buffers and reference input buffers
  - 2.5 V precision reference (3.5 ppm/°C)
  - Cross point multiplexer (enable system diagnostic)
  - 8 full differential or 16 single-ended channels
  - Clock oscillator
  - GPIO and GPO pins with automatic external mux control
- Fast and flexible output rate: 1.25 SPS to 31.25 kSPS
- Channel scan data rate: 6.21 kSPS/channel (161 µs settling)
- Performance specifications
  - 17.5 noise free bits at 31.25 kSPS
  - 24 noise free bits at 1.25 SPS
  - INL: ±3 ppm/FSR
- 85 dB rejection of 50 Hz and 60 Hz with 50 ms settling
- Operates with either 3.3 V or5 V supply
  - Single supply
    - 3.3 V or 5 V AVDD1, 2 V to 5 V AVDD2, and 2 V to 5 V IOVDD
  - Optional split supply
    - AVDD1 and AVSS ± 2.5 V or AVDD1 and AVSS ± 1.65 V
  - Current: 1.4 mA
- 3-/4-wire serial digital interface (Schmitt trigger on SCLK)
  - CRC error checking
  - SPI, QSPI, MICROWIRE, and DSP compatible
- Package: 40-lead 6 mm × 6 mm LFCSP
- Temperature range: −40°C to +105°C

APPLICATIONS

- Process control: PLC/DCS modules
  - Voltage, current, temperature, and pressure measurement
  - Flow meters
- Medical and scientific multichannel instrumentation
- Seismic instrumentation
- Chemical analysis instrumentation: chromatography

GENERAL DESCRIPTION

Fast settling, highly accurate, low power, 8-/16-channel, multiplexed ADC for low bandwidth input signals with integrated input buffers.

Integrated precision, 2.5 V, low drift (3.5 ppm/°C), band gap reference and integrated oscillator.

Eight flexible setups with configurability for output data rate, digital filter mode, offset/gain error correction, reference selection, buffer enables and more. This per channel configurability extends to the output data rate used for each channel when using sinc5 + sinc1 filter.

Sinc5 + sinc1 filter maximizes channel scan rate, and sinc3 filter maximizes resolution and enhanced 50 Hz/60 Hz rejection, with four selectable options to maximize rejection.

Integrated diagnostic features, including CRC, register checksum, temperature sensor, crosspoint multiplexer, burnout currents, and GPIOs/GPOs.

FUNCTIONAL BLOCK DIAGRAM

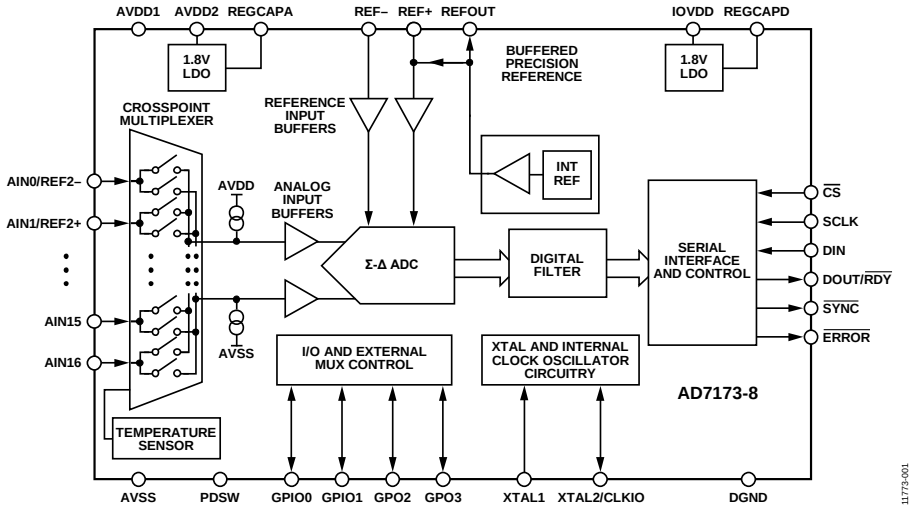

Figure 1.

Rev. B Document Feedback

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REVISION HISTORY

5/2017—Rev. A to Rev. B

Changed LFCSP_WQ to LFCSP ..... Throughout
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Updated Outline Dimensions 63

4/2014—Rev. 0 to Rev. A

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10/2013—Revision 0: Initial Version

SPECIFICATIONS

AVDD1 = 3.0 V to 5.5 V, AVDD2 = 2 V to 5.5 V, IOVDD = 2 V to 5.5 V, AVSS = DGND = 0 V, REF+ = 2.5 V, REF− = AVSS, internal master clock = 2 MHz, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR)		1.25		31250	SPS
No Missing Codes[1]	Excluding sinc3 filter at 31.25 kSPS	24			Bits
Resolution	See Table 6				
Noise	See Table 6				
Noise Free Resolution	Sinc5 + sinc1 filter (default)				
	31.25 kSPS, REF+ = 5 V		17.5		Bits
	2.6 kSPS, REF+ = 5 V		18.4		Bits
	1.25 SPS, REF+ = 5 V		24		Bits
ACCURACY					
Integral Nonlinearity (INL)	2.5 V reference		±3	±7.5	ppm/FSR
	5 V reference		±5		ppm/FSR
Offset Error[2]	Internal short		±40		µV
Offset Drift	Internal short		±350		nV/°C
Offset Drift vs. Time[3]			±450		nV/1000 hrs
Gain Error[2]	25°C, AVDD1 = 5 V		±10	±50	ppm/FSR
Gain Drift vs. Temperature[1]			±0.5	±1	ppm/FSR/°C
Gain Drift vs. Time[3]			±3		ppm/FSR/ 1000 hrs
REJECTION					
Power Supply Rejection	AVDD1 and AVDD2, V_{IN} = 1 V		90		dB
Common-Mode Rejection	V_{IN} = 0.1 V				
At DC		95			dB
At 50 Hz and 60 Hz[1]	20 SPS ODR (post filter); 50 Hz ± 1 Hz and 60 Hz ± 1 Hz	120			dB
Normal Mode Rejection[1]	50 Hz ± 1 Hz and 60 Hz ± 1 Hz				
	Internal clock, 20 SPS ODR (post filter)	71	90		dB
	External clock, 20 SPS ODR (post filter)	85	90		dB
ANALOG INPUTS					
Differential Input Voltage Range			$\pm V_{REF}$		V
Absolute AIN Voltage Limits[1]					
Buffers Disabled		AVSS − 0.05		AVDD1 + 0.05	V
Buffers Enabled		AVSS		AVDD1 − 1.1	V
Analog Input Current					
Buffers Enabled	Single cycle settling enabled (default)				
Input Current			±2		nA
Input Current Drift			±25		pA/°C
Buffers Disabled					
Input Current			±6		µA/V
Input Current Drift	External clock		±0.1		nA/V/°C
	Internal clock (±2.5% clock)		±0.5		nA/V/°C
Crosstalk	1 kHz input		−120		dB
INTERNAL REFERENCE	100 nF external capacitor on REFOUT to AVSS				
Output Voltage	REFOUT with respect to AVSS		2.5		V
Initial Accuracy[1]	T_A = 25°C[4]	−0.1		+0.1	% of V
Temperature Coefficient					
0°C to +105°C			3.5	8[1]	ppm/°C
−40°C to +105°C			3.5	10[1]	ppm/°C
Reference Load Current, I_{LOAD}	I_L	−10		+10	mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power Supply Rejection (Line Regulation)	AVDD1 and AVDD2		90		dB
Load Regulation	$\Delta V_{OUT}/\Delta I_L$		140		ppm/mA
Voltage Noise	e_N, 0.1 Hz to 10 Hz		6.5		μV rms
Voltage Noise Density	e_N, 1 kHz		215		nV/√Hz
Turn-On Settling Time	100 nF capacitor		60		μs
Long-Term Stability[3]	1000 hours		460		ppm
Short Circuit	I_{SC}		25		mA
EXTERNAL REFERENCE					
Reference Input Voltage	Reference input = (REF+) − (REF−)	1	2.5	AVDD1	V
Absolute Reference Input Voltage Limits[1]					
Buffers Disabled		AVSS − 0.05		AVDD1 + 0.05	V
Buffers Enabled		AVSS		AVDD1	V
Average Reference Input Current					
Buffers Disabled			±9		μA/V
Buffers Enabled			±50		nA
Average Reference Input Current Drift	Buffers disabled				
External clock			±5		nA/V/°C
Internal clock			±6		nA/V/°C
Normal Mode Rejection[1]	See the Rejection parameter				
Common-Mode Rejection			83		dB
TEMPERATURE SENSOR					
Accuracy	After user calibration at 25°C		±2		°C
Sensitivity			477		μV/°C
BURNOUT CURRENTS					
Source/Sink Current	Analog input buffers must be enabled		±10		μA
BRIDGE POWER-DOWN SWITCH					
R_{ON}			24		Ω
Allowable Currents				16	mA
GENERAL-PURPOSE I/O (GPIO0, GPIO1, GPO2, GPO3)	With respect to AVSS				
Input Mode Leakage Current[1]		−10		+10	μA
Floating State Output Capacitance			5		pF
AVDD1 − AVSS = 5 V					
Output High Voltage, V_{OH}[1]	I_{SOURCE} = 200 μA	AVSS + 4			V
Output Low Voltage, V_{OL}[1]	I_{SINK} = 800 μA			AVSS + 0.4	V
Input High Voltage, V_{IH}[1]		AVSS + 3			V
Input Low Voltage, V_{IL}[1]				AVSS + 0.7	V
AVDD1 − AVSS = 3.3 V					
Output High Voltage, V_{OH}[1]	I_{SOURCE} = 200 μA	AVSS + 2.7			V
Output Low Voltage, V_{OL}[1]	I_{SINK} = 800 μA			AVSS + 0.27	V
Input High Voltage, V_{IH}[1]		AVSS + 2			V
Input Low Voltage, V_{IL}[1]				AVSS + 0.45	V
CLOCK					
Internal Clock					
Frequency			2		MHz
Accuracy		−2.5		+2.5	%
Duty Cycle			50:50		
Output Low Voltage, V_{OL}				0.4	V
Output High Voltage, V_{OH}		0.8 × IOVDD			V
Crystal					
Frequency		14	16	16.384	MHz
Start-Up Time			10		μs
External Clock (CLKIO)			2	2.048	MHz
Duty Cycle[1]	Typical duty cycle 50:50 (maximum:minimum)	30:70	50:50	70:30	

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input High Voltage, V_{INH}[1]	2 V ≤ IOVDD ≤ 2.3 V	0.65 × IOVDD			V
	2.3 V ≤ IOVDD ≤ 5.5 V	0.7 × IOVDD			V
Input Low Voltage, V_{INL}[1]	2 V ≤ IOVDD ≤ 2.3 V			0.35 × IOVDD	V
	2.3 V ≤ IOVDD ≤ 5.5 V			0.7	V
Hysteresis[1]	IOVDD > 2.7 V	0.08		0.25	V
	IOVDD < 2.7 V	0.04		0.2	V
Leakage Currents		−10		+10	µA
LOGIC OUTPUT (DOUT/$\overline{RDY}$)					
Output High Voltage, V_{OH}[1]	IOVDD ≥ 4.5 V, I_{SOURCE} = 1 mA	0.8 × IOVDD			V
	2.7 V ≤ IOVDD < 4.5 V, I_{SOURCE} = 500 µA	0.8 × IOVDD			V
	IOVDD < 2.7 V, I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Output Low Voltage, V_{OL}[1]	IOVDD ≥ 4.5 V, I_{SINK} = 2 mA			0.4	V
	2.7 V ≤ IOVDD < 4.5 V, I_{SINK} = 1 mA			0.4	V
	IOVDD < 2.7 V, I_{SINK} = 400 µA			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
SYSTEM CALIBRATION[1]					
Full-Scale Calibration Limit				1.05 × FS	V
Zero-Scale Calibration Limit		−1.05 × FS			V
Input Span		0.8 × FS		2.1 × FS	V
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD1 − AVSS		3.0		5.5	V
AVDD2 − AVSS		2		5.5	V
AVSS − DGND		−2.75		0	V
IOVDD − DGND		2		5.5	V
IOVDD − AVSS	For AVSS < DGND			6.35	V
POWER SUPPLY CURRENTS	All outputs unloaded				
Full Operating Mode					
AVDD1 Current					
AVDD1 = 5 V Typical, 5.5 V Maximum	AIN± and REF± buffers disabled; external reference		0.23	0.27	mA
	AIN± and REF± buffers disabled; internal reference		0.42	0.49	mA
	AIN± and REF± buffers enabled; external reference		2.12	2.71	mA
	Each enabled buffered pair: AIN+, AIN− and REF+, REF−		0.945	1.22	mA
AVDD1 = 3.3 V Typical, 3.6 V Maximum[1]	AIN± and REF± buffers disabled; external reference		0.16	0.19	mA
	AIN± and REF± buffers disabled; internal reference		0.34	0.4	mA
	AIN± and REF± buffers enabled; external reference		1.9	2.45	mA
	Each enabled buffered pair: AIN+, AIN− and REF+, REF−		0.87	1.13	mA
AVDD2 Current	External reference		1	1.15	mA
	Internal reference		1.25	1.4	mA
IOVDD Current	External clock		0.24	0.39	mA
	Internal clock		0.52	0.76	mA
	External crystal		0.9		mA
Standby Mode					
Standby (LDO on)	Reference off, total current consumption		25		µA
	Reference on, total current consumption		400		µA
Power-Down Mode	Full power-down, LDO, REF±		2	10	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER DISSIPATION					
Full Operating Mode	Unbuffered, external clock and reference; AVDD1 = 3.3 V, AVDD2 = 2 V, IOVDD = 2 V		3		mW
	Unbuffered, external clock and reference; all supplies = 5 V		7.35		mW
	Unbuffered, external clock and reference; all supplies = 5.5 V			9.96	mW
	Fully buffered, internal clock and reference (note that REFOUT has no load); AVDD1 = 3.3 V, AVDD2 = 2 V, IOVDD = 2 V		10.4		mW
	Fully buffered, internal clock and reference (note that REFOUT has no load); all supplies = 5 V		20.4		mW
	Fully buffered, internal clock and reference (note that REFOUT has no load); all supplies = 5.5 V			28	mW
Standby Mode	Reference off, all supplies = 5 V		125		µW
	Reference on, all supplies = 5 V		2		mW
Power-Down Mode	Full power-down, all supplies = 5 V		10		µW
	Full power-down, all supplies = 5.5 V			55	µW

[1] Specification is not production tested but is supported by characterization data at the initial product release.
[2] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[3] This specification is noncumulative and includes MSL preconditioning effects.
[4] This specification includes MSL preconditioning effects.

TIMING CHARACTERISTICS

IOVDD = 2 V to 5.5 V, DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, C_{LOAD} = 20 pF, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Test Conditions/Comments[1, 2]
SCLK PULSE WIDTH			
t_3	25	ns min	SCLK high pulse width
t_4	25	ns min	SCLK low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	15	ns max	IOVDD = 4.5 V to 5.5 V
	40	ns max	IOVDD = 2 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	12	ns max	IOVDD = 4.5 V to 5.5 V
	25	ns max	IOVDD = 2 V to 3.6 V
t_5[5]	2.5	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	20	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high/low
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	8	ns min	Data valid to SCLK edge setup time
t_{10}	8	ns min	Data valid to SCLK edge hold time
t_{11}	5	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance.
[2] See Figure 2 and Figure 3.
[3] The time required for the output to cross the V_{OL} or V_{OH} limits.
[4] The SCLK active edge is the falling edge of SCLK.
[5] $\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high. It is important to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

Timing Diagrams

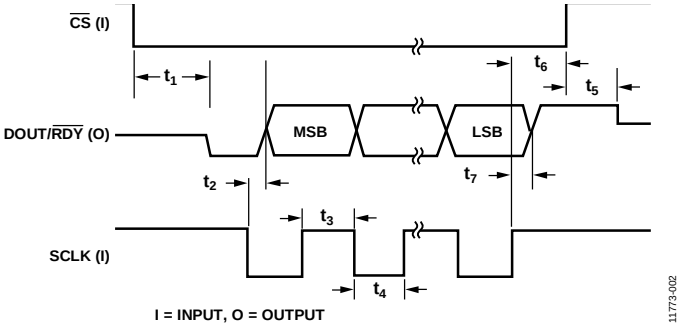


Figure 2. Read Cycle Timing Diagram

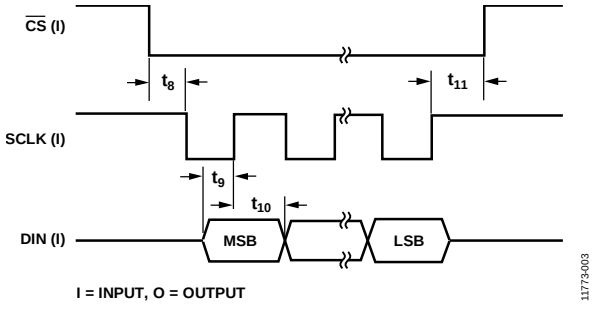


Figure 3. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD1, AVDD2 to AVSS	−0.3 V to +6.5 V
AVDD1 to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
IOVDD to AVSS	−0.3 V to +7.5 V
AVSS to DGND	−3.25 V to +0.3 V
Analog Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Reference Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOVDD + 0.3 V
AIN[16:0] or Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Soldering, Reflow Temperature	260°C
ESD Rating (HBM)	4 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device soldered on a JEDEC test board for surface-mount packages. The values listed in Table 4 are based on simulated data.

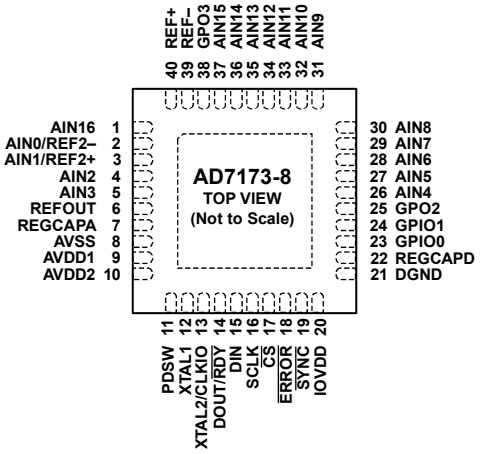
Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
40-Lead, 6 mm × 6 mm LFCSP		
1-Layer JEDEC Board	114	°C/W
4-Layer JEDEC Board	54	°C/W
4-Layer JEDEC Board with 16 Thermal Vias	34	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD SHOULD BE SOLDERED TO A SIMILAR PAD ON THE PCB UNDER THE EXPOSED PAD TO CONFER MECHANICAL STRENGTH AND FOR HEAT DISSIPATION. THE EXPOSED PAD MUST BE CONNECTED TO AVSS THROUGH THIS PAD ON THE PCB.

11773-004

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	AIN16	AI	Analog Input 16. Selectable through cross point mux.
2	AIN0/REF2−	AI	Analog Input 0 (AIN0)/Reference 2, Negative Input (REF2−). An external reference can be applied between REF2+ and REF2−. REF2− can span from AVSS to AVDD1 − 1 V. Analog Input 0 is selectable through cross point mux. Reference 2 can be selected through the REFSEL bits in the setup configuration register.
3	AIN1/REF2+	AI	Analog Input 1 (AIN0)/Reference 2, Positive Input (REF2+). An external reference can be applied between REF2+ and REF2−. REF2+ can span from AVDD1 to AVSS + 1 V. Analog Input 1 is selectable through cross point mux. Reference 2 can be selected through the REFSEL bits in the setup configuration register.
4	AIN2	AI	Analog Input 2. Selectable through cross point mux.
5	AIN3	AI	Analog Input 3. Selectable through cross point mux.
6	REFOUT	AO	Buffered Output of Internal Reference. The output is 2.5 V with respect to AVSS.
7	REGCAPA	AO	Analog LDO Regulator Output. Decouple this pin to AVSS using a 1 µF capacitor.
8	AVSS	P	Negative Analog Supply. This supply ranges from 0 V to −2.75 V and is nominally set to 0 V.
9	AVDD1	P	Analog Supply Voltage 1. This voltage ranges from 3.0 V minimum to 5.5 V maximum with respect to AVSS.
10	AVDD2	P	Analog Supply Voltage 2. This voltage ranges from 2 V to AVDD1 with respect to AVSS.
11	PDSW	AO	Power-Down Switch Connected to AVSS. This pin is controlled by the PDSW bit in the GPIOCON register.
12	XTAL1	AI	Input 1 for Crystal.
13	XTAL2/CLKIO	AI/DI	Input 2 for Crystal (XTAL2)/Clock Input or Output (CLKIO). See the CLOCKSEL bit settings in the ADCMODE register (Table 25) for more information.
14	DOUT/$\overline{\text{RDY}}$	DO	Serial Data Output (DOUT)/Data Ready Output ($\overline{\text{RDY}}$). This pin serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. The data-word/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. When $\overline{\text{CS}}$ is low, and a register is not being read, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available.

Pin No.	Mnemonic	Type[1]	Description
15	DIN	DI	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register address (RA) bits of the communications register identifying the appropriate register. Data is clocked in on the rising edge of SCLK.
16	SCLK	DI	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. SCLK has a Schmitt trigger input, making the interface suitable for opto-isolated applications.
17	$\overline{CS}$	DI	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ output is tristated.
18	$\overline{ERROR}$	DI/O	This pin can be used in one of the following three modes: Active low error input mode. This mode sets the ADC_ERROR bit in the STATUS register. Active low, open-drain error output mode. The STATUS register error bits are mapped to the $\overline{ERROR}$ pin. The $\overline{ERROR}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed. General-purpose output mode. The status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. The pin is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the GPIO1 and GPIO2 pins. The $\overline{ERROR}$ pin has an active pull-up in this case.
19	$\overline{SYNC}$	DI	Synchronization Input. Allows synchronization of the digital filters and analog modulators when using multiple AD7173-8 devices.
20	IOVDD	P	Digital I/O Supply Voltage. IOVDD voltage ranges from 2 V to 5 V. IOVDD is independent of AVDD1 and AVDD2. For example, IOVDD can be operated at 3.3 V when AVDD1 or AVDD2 equals 5 V, or vice versa. If AVSS is set to −2.5 V, the voltage on IOVDD must not exceed 3.6 V.
21	DGND	P	Digital Ground.
22	REGCAPD	AO	Digital LDO Regulator Output. This pin is for decoupling purposes only. Decouple this pin to DGND using a 1 µF capacitor.
23	GPIO0	DI/O	General-Purpose Input/Output. Logic input/output on this this pin is referred to the AVDD1 and AVSS supplies.
24	GPIO1	DI/O	General-Purpose Input/Output. Logic input/output on this this pin is referred to the AVDD1 and AVSS supplies.
25	GPO2	DO	General-Purpose Output. Logic output on this this pin is referred to the AVDD1 and AVSS supplies.
26	AIN4	AI	Analog Input 4. Selectable through cross point mux.
27	AIN5	AI	Analog Input 5. Selectable through cross point mux.
28	AIN6	AI	Analog Input 6. Selectable through cross point mux.
29	AIN7	AI	Analog Input 7. Selectable through cross point mux.
30	AIN8	AI	Analog Input 8. Selectable through cross point mux.
31	AIN9	AI	Analog Input 9. Selectable through cross point mux.
32	AIN10	AI	Analog Input 10. Selectable through cross point mux.
33	AIN11	AI	Analog Input 11. Selectable through cross point mux.
34	AIN12	AI	Analog Input 12. Selectable through cross point mux.
35	AIN13	AI	Analog Input 13. Selectable through cross point mux.
36	AIN14	AI	Analog Input 14. Selectable through cross point mux.
37	AIN15	AI	Analog Input 15. Selectable through cross point mux.
38	GPO3	DO	General-Purpose Output. Logic output on this this pin is referred to the AVDD1 and AVSS supplies.
39	REF−	AI	Reference 1 Input Negative Terminal. REF− can span from AVSS to AVDD1 − 1 V. Reference 1 can be selected through the REFSEL bits in the SETUP CONFIGURATION register.
40	REF+	AI	Reference 1 Input Positive Terminal. An external reference can be applied between REF+ and REF−. REF+ can span from AVDD1 to AVSS + 1 V. Reference 1 can be selected through the REFSEL bits in the SETUP CONFIGURATION register.
	EP	P	Exposed Pad. The exposed pad should be soldered to a similar pad on the PCB under the exposed paddle to confer mechanical strength to the package and for heat dissipation. The exposed pad must be connected to AVSS through this pad on the PCB.

[1] AI = analog input, AO = analog output, DI/O = bidirectional digital input/output, DO = digital output, DI = digital input, P = power supply.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 3.3 V, unless otherwise noted.

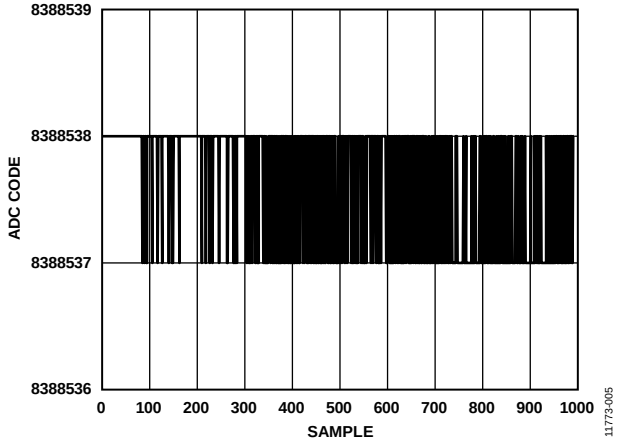


Figure 5. Noise
(Output Data Rate = 1.25 SPS, Analog Input Buffers Disabled)

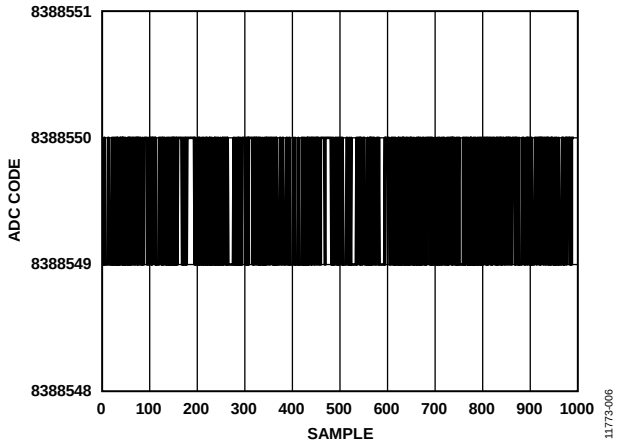


Figure 6. Noise
(Output Data Rate = 1.25 SPS, Analog Input Buffers Enabled)

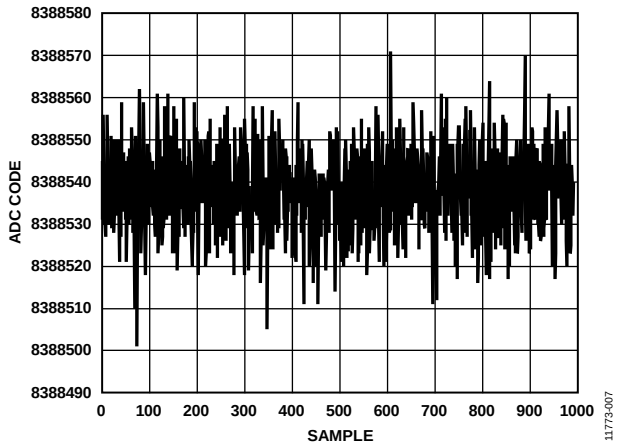


Figure 7. Noise
(Output Data Rate = 10 kSPS, Analog Input Buffers Disabled)

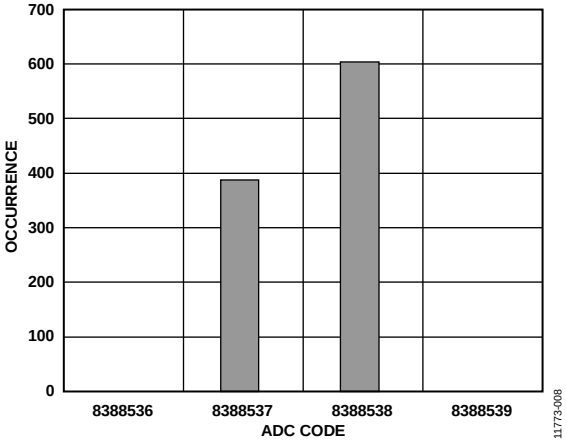


Figure 8. Noise Distribution Histogram
(Output Data Rate = 1.25 SPS, Analog Input Buffers Disabled))

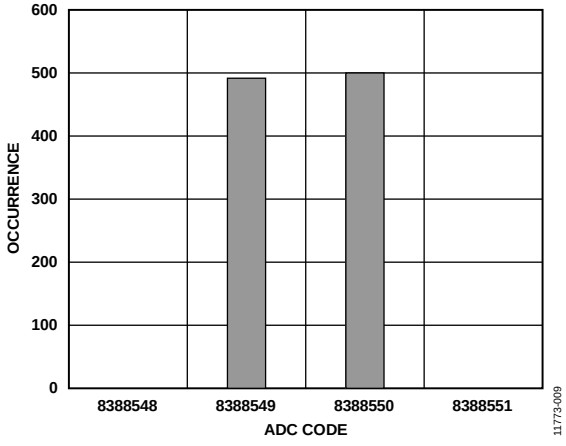


Figure 9. Noise Distribution Histogram
(Output Data Rate = 1.25 SPS, Analog Input Buffers Enabled)

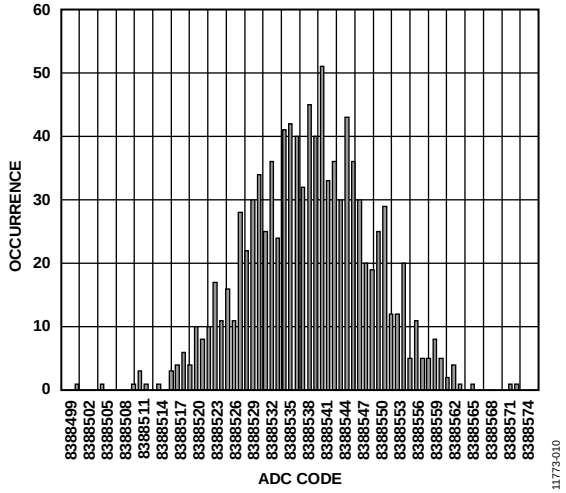


Figure 10. Noise Distribution Histogram
(Output Data Rate = 10 kSPS, Analog Input Buffers Disabled))

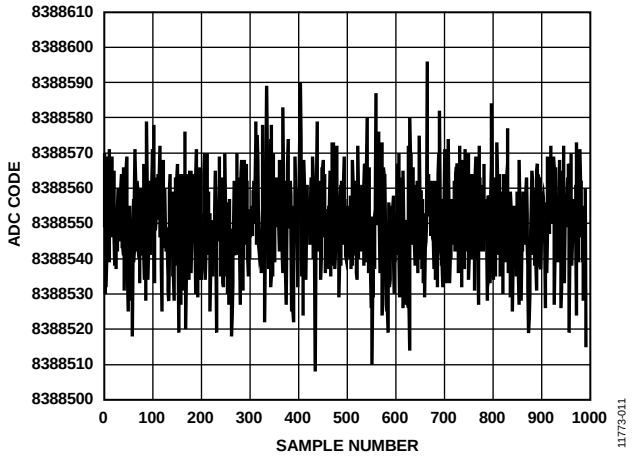


Figure 11. Noise
(Output Data Rate = 10 kSPS, Analog Input Buffers Enabled)

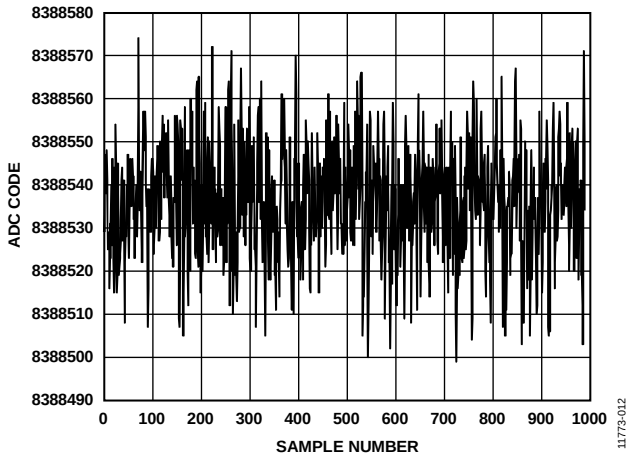


Figure 12. Noise
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Disabled)

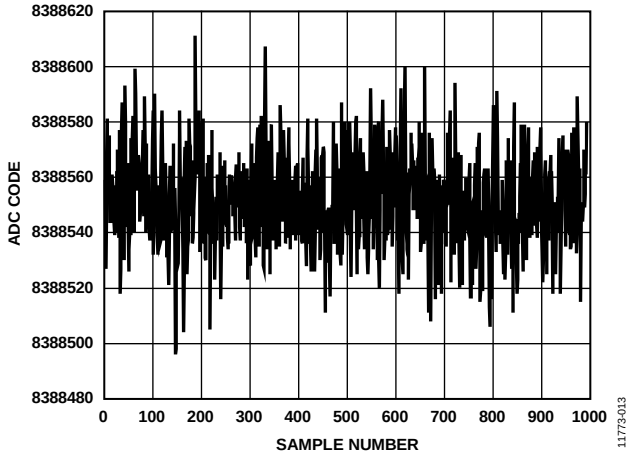


Figure 13. Noise
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Enabled)

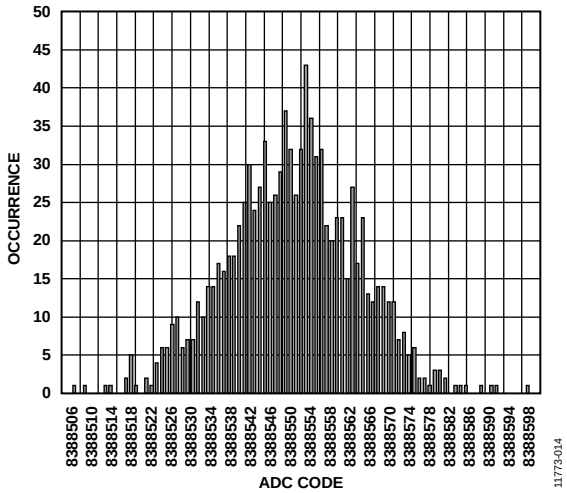


Figure 14. Noise Distribution Histogram
(Output Data Rate = 10 kSPS, Analog Input Buffers Enabled))

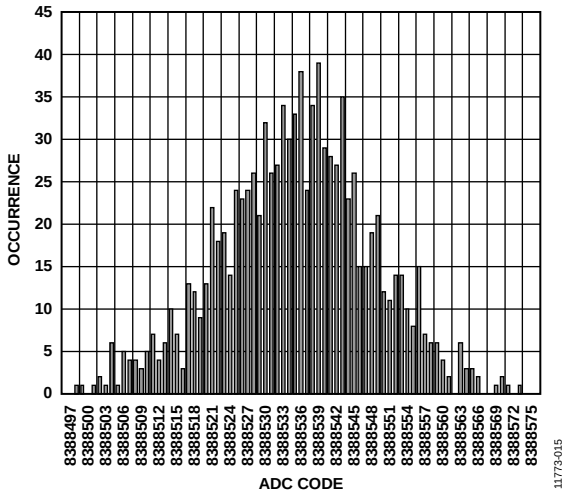


Figure 15. Noise Distribution Histogram
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Disabled)

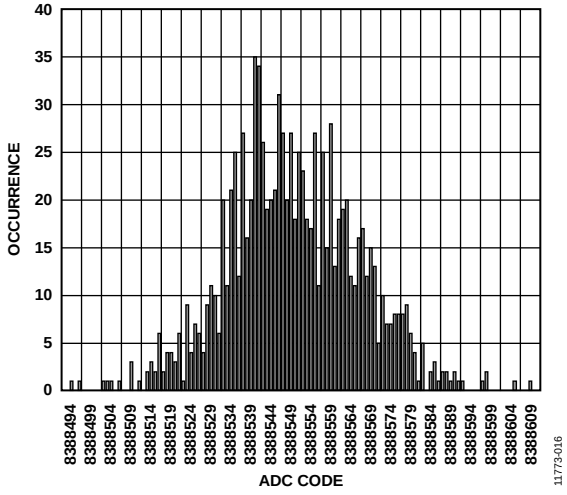


Figure 16. Noise Distribution Histogram
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Enabled)

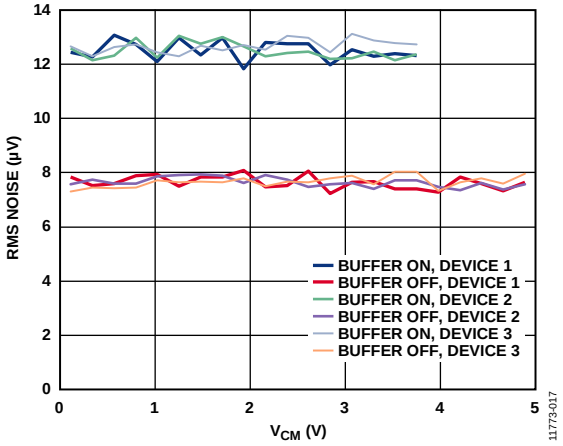


Figure 17. RMS Noise vs. Common-Mode Input Voltage

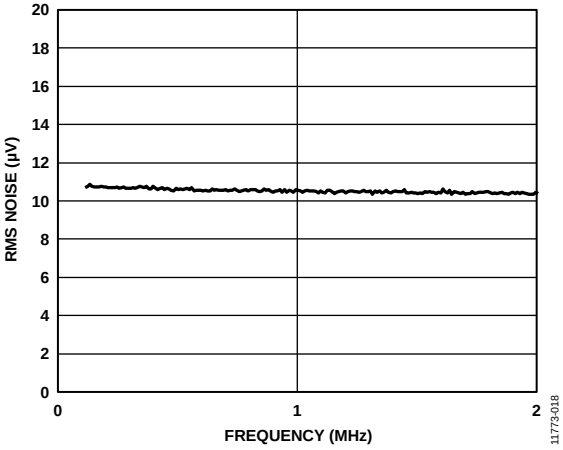


Figure 18. RMS Noise vs. Master Clock Frequency
(Output Data Rate = 31.25 kSPS, Analog Input Buffers Enabled)

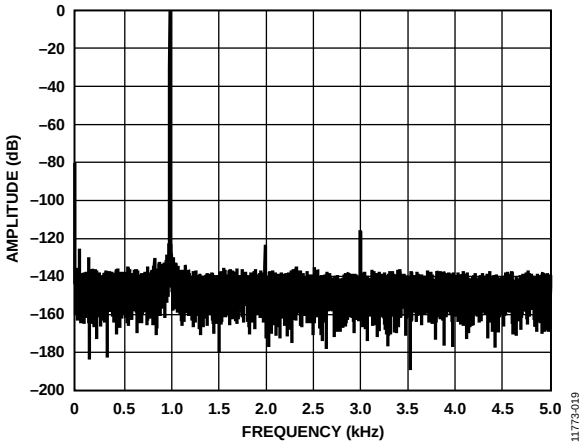


Figure 19. ADC Output FFT; 1 kHz Input Tone, −0.5 dBFS Input FFT
(Output Data Rate = 10 kSPS, External Reference,
External Clock, Buffers Enabled)

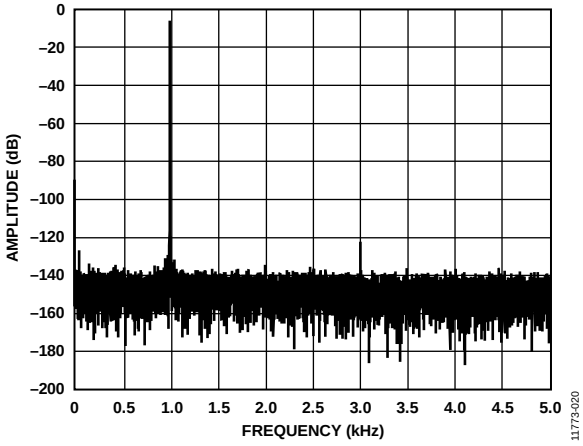


Figure 20. ADC Output FFT; 1 kHz Input Tone, −6 dBFS Input FFT
(Output Data Rate = 10 kSPS, External Reference,
External Clock, Buffers Enabled)

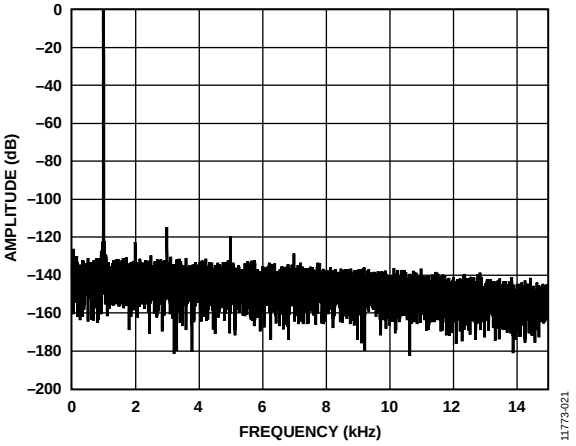


Figure 21. ADC Output FFT; 1 kHz Input Tone, −0.5 dBFS Input FFT
(Output Data Rate = 31.25 kSPS, External Reference,
External Clock, Buffers Enabled)

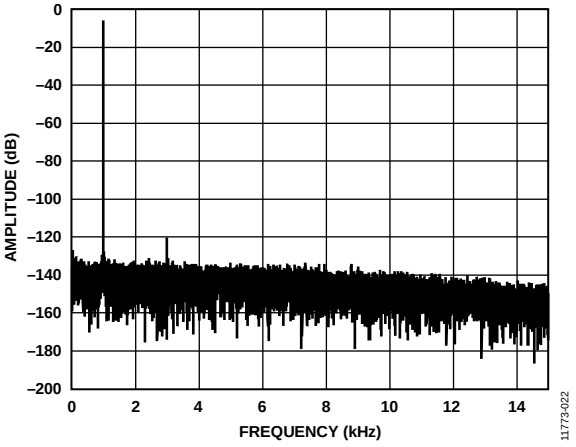


Figure 22. ADC Output FFT; 1 kHz Input Tone, −6 dBFS Input FFT
(Output Data Rate = 31.25 kSPS, External Reference,
External Clock, Buffers Enabled)

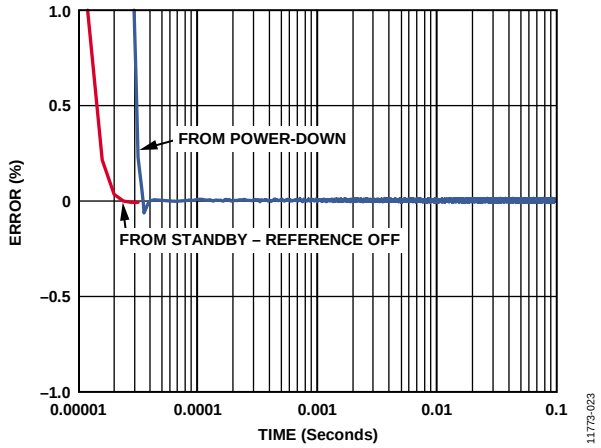


Figure 23. Internal Reference Settling Time

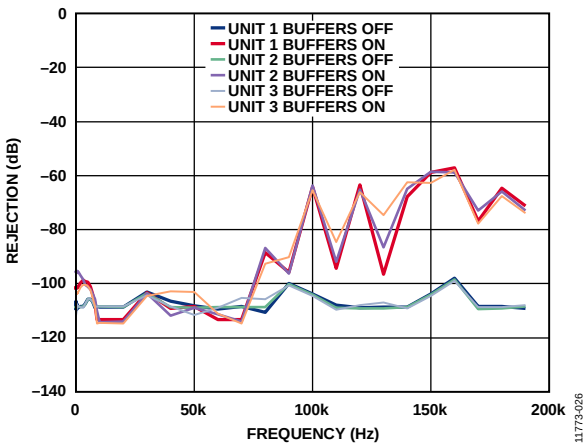


Figure 26. Common-Mode Rejection Ratio vs. Frequency (Output Data Rate = 31.25 kSPS)

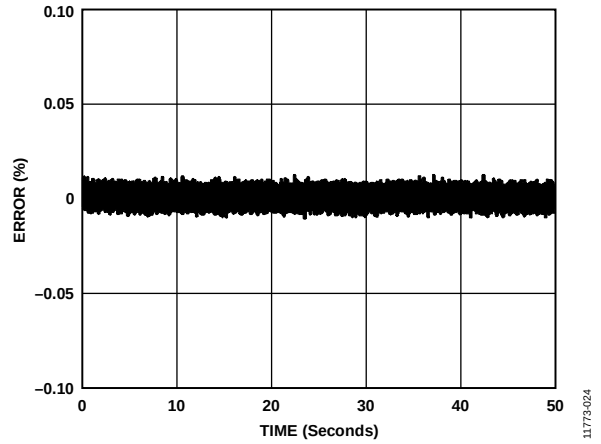


Figure 24. Internal Reference Settling Time (Extended)

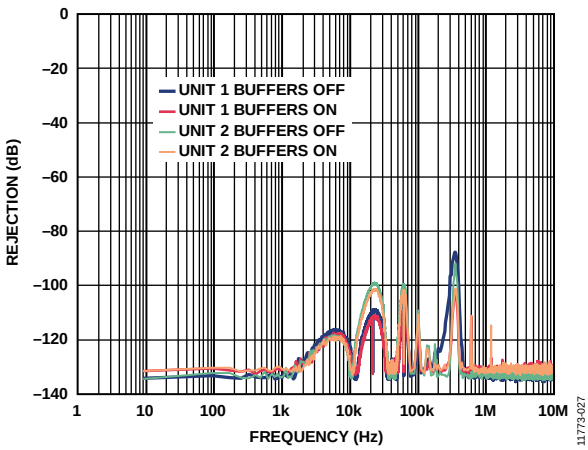


Figure 27. Power Supply Rejection Ratio vs. Frequency

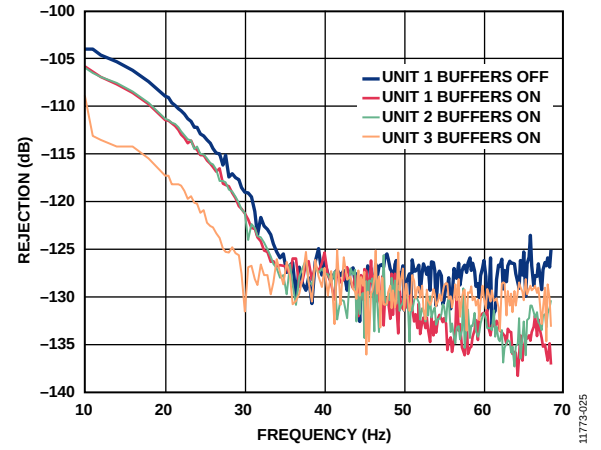


Figure 25. Common-Mode Rejection Ratio (10 Hz to 70 Hz) vs. Frequency (20 SPS Enhanced Filter)

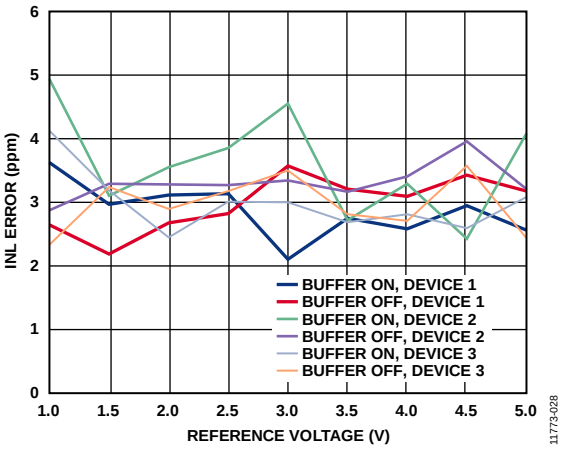


Figure 28. Integral Nonlinearity (INL) Error vs. Reference Voltage (Differential Input, External Reference)

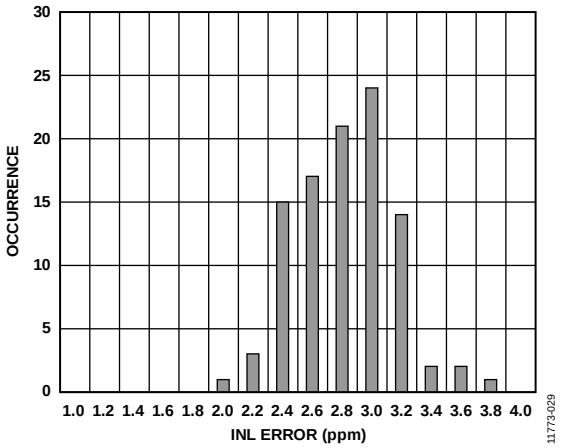


Figure 29. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, V_{REF} = 2.5 V External)

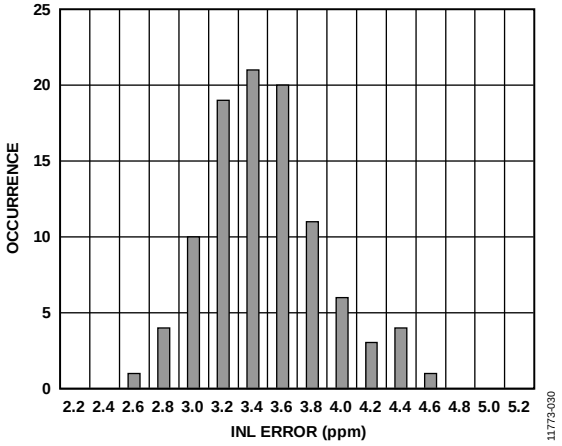


Figure 30. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, V_{REF} = 5 V External)

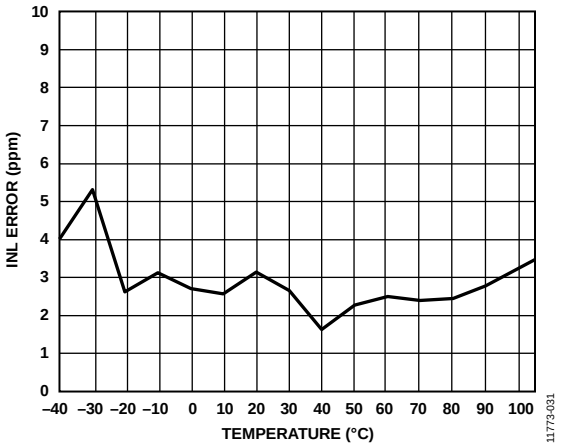


Figure 31. Integral Nonlinearity (INL) Error vs. Temperature (Differential Input, V_{REF} = 2.5 V)

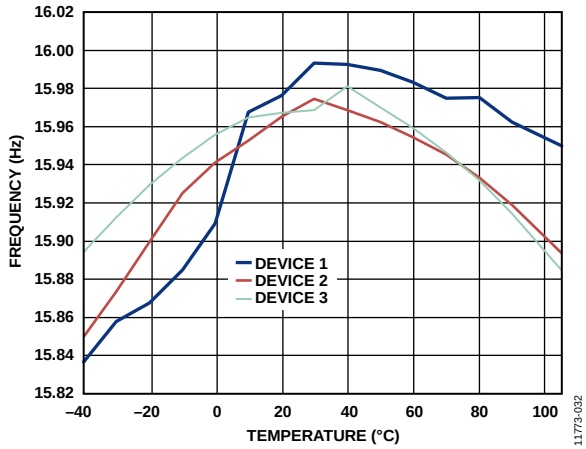


Figure 32. Internal Oscillator Frequency vs. Temperature

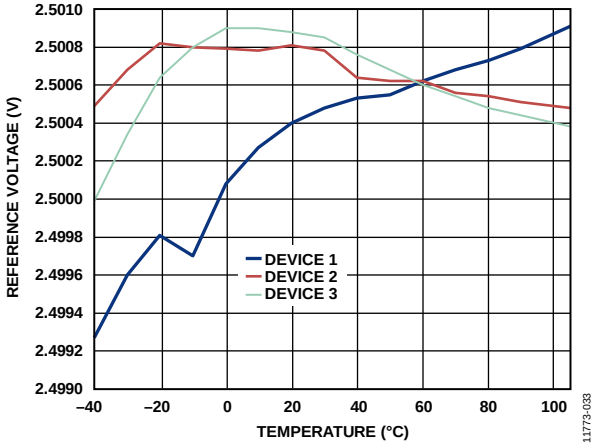


Figure 33. Internal Reference Voltage vs. Temperature

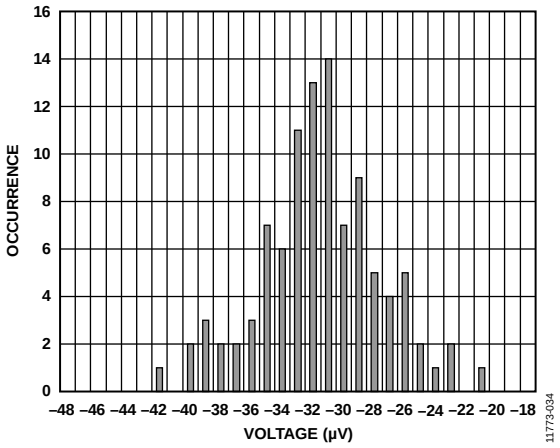


Figure 34. Offset Error Distribution Histogram (Internal Short)

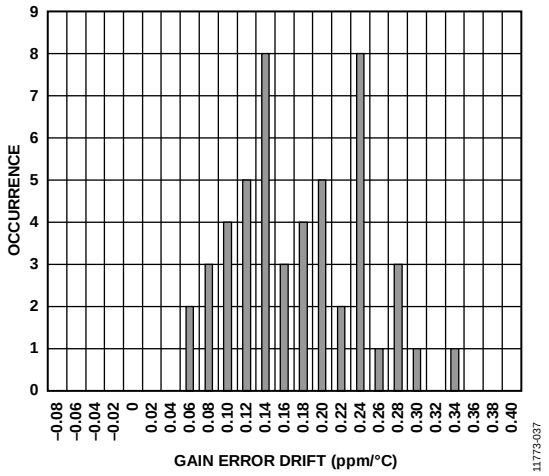


Figure 37. Gain Error Drift Distribution Histogram

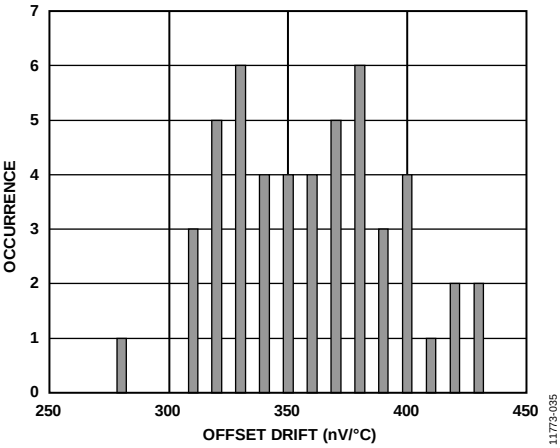


Figure 35. Offset Error Drift Distribution Histogram (Internal Short)

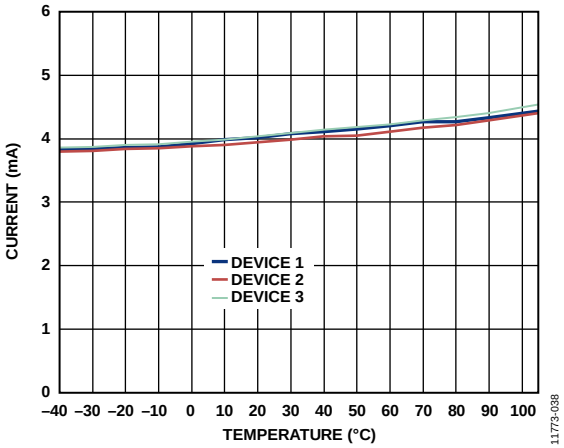


Figure 38. Current Consumption vs. Temperature (Continuous Conversion Mode, Buffers Enabled, Internal Reference, Internal Clock)

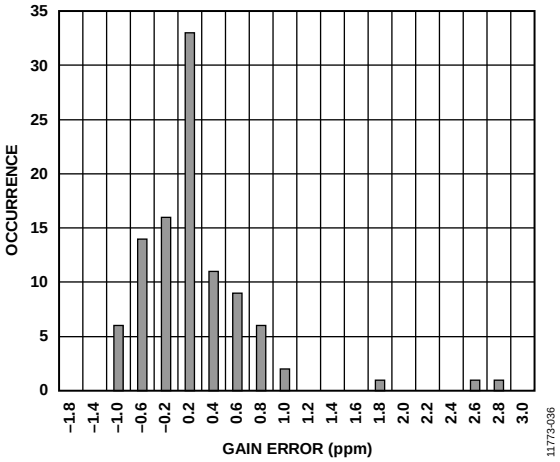


Figure 36. Gain Error Distribution Histogram

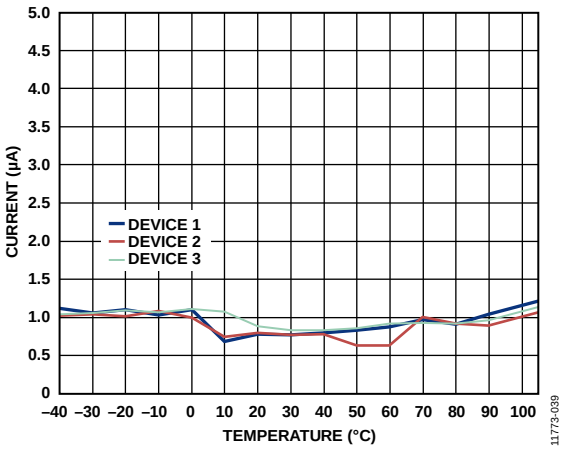


Figure 39. Current Consumption vs. Temperature (Power-Down Mode)

NOISE PERFORMANCE AND RESOLUTION

Table 6 shows the rms noise, peak-to-peak noise, effective resolution, and the noise free (peak-to-peak) resolution of the AD7173-8 for various output data rates and filters. The values listed are for the bipolar input range with an external 5 V reference.

These values are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker. Using the sinc3 filter at the fastest rate results in the noise being quantization limited. This limitation degrades the noise specification at this rate and does not give a result of 24 bits, no missing codes.

Table 6. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate using Sinc5 + Sinc1 Filter (Default)[1]

	Sinc5 + Sinc1 Filter (Default)			
Output Data Rate (SPS)	**RMS Noise (μV rms)**	**Effective Resolution (Bits)**	**Peak-to-Peak Noise (μV rms)**	**Peak-to-Peak Resolution (Bits)**
31,250	8.0	20.2	67	17.5
5208	4.5	21.1	30	18.3
1007	2.2	22.2	15	19.3
381	1.3	22.9	8.9	20.1
100.5	0.71	23.8	5.1	21
20.01	0.32	24	1.7	22.2
5	0.15	24	0.75	23.4
1.25	0.07	24	0.32	24

[1] Selected rates only; 1000 samples.

Table 7. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate using Sinc3 Filter[1]

	Sinc3 Filter			
Output Data Rate (SPS)	**RMS Noise (μV rms)**	**Effective Resolution (Bits)**	**Peak-to-Peak Noise (μV rms)**	**Peak-to-Peak Resolution (Bits)**
31,250	210	15.5	1665	12.8
5208	3.6	21.4	28	18.7
1008	1.5	22.7	12	19.9
400.6	1	23.3	6.6	20.5
100.5	0.55	24	3.5	21.4
20.01	0.25	24	1.2	22.4
5	0.11	24	0.56	23.4
1.25	0.07	24	0.27	24

[1] Selected rates only; 1000 samples.

GETTING STARTED

The AD7173-8 offers the user a fast settling, high resolution, multiplexed ADC with high levels of configurability.

- Eight fully differential or 16 single-ended analog inputs.
- Cross point mux. Selects any analog input combination as a pairing to be converted. The signals are routed to the input buffers and onto the modulator positive or negative input.
- ADC input. Selectable as a fully differential input or as a single-ended input.
- Per setup configurability. Up to eight different setups can be defined. A separate setup can be mapped to each of the channels. Each setup allows the user to configure the following:
  - Output data rate when using sinc5 + sinc1 filter
  - Digital filter mode
  - Offset/gain error correction
  - Reference source selection (internal/external)
  - Analog and reference input buffer enables
  - Digital output coding

The AD7173-8 includes a precision 2.5 V low drift (3.5 ppm/°C) band gap internal reference. This reference can be selected to be used for the ADC conversions, reducing the external component count. When enabled, the internal reference is output to the REFOUT pin and can be used as a low noise biasing voltage for the external circuitry. An example of this is using the REFOUT signal to set the input common mode for an external single-ended to differential amplifier.

The AD7173-8 includes two separate linear regulator blocks for both the analog and digital circuitry. The analog LDO regulates the AVDD2 supply to 1.8 V, supplying the ADC core. The user can tie the AVDD1 and AVDD2 supplies together for easiest connection. If a clean analog supply rail is in the system in the range of 2 V to 5.5 V (minimum to maximum), the user can also choose to connect this supply rail to the AVDD2 input, allowing for lower power dissipation.

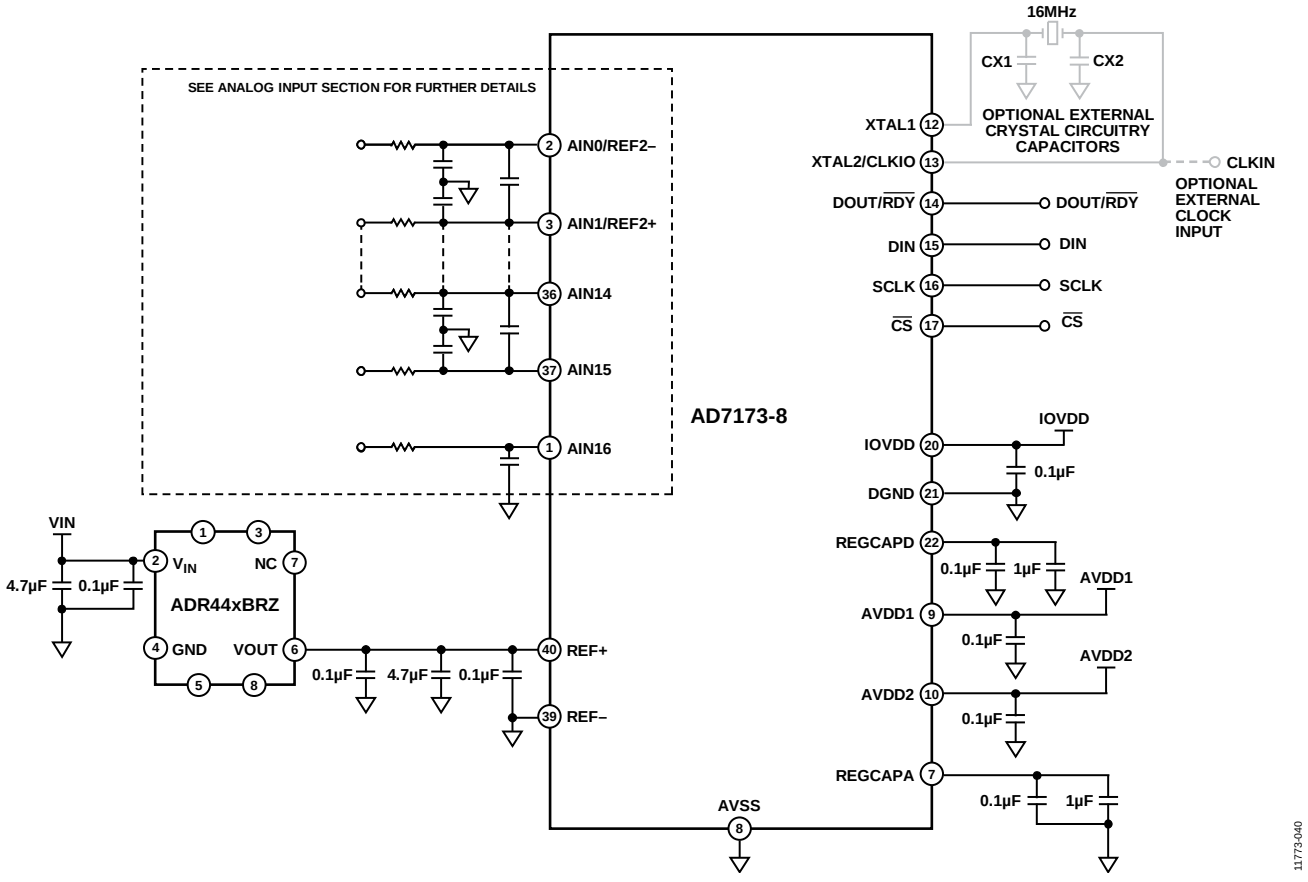


Figure 40. Typical Connection Diagram

The linear regulator for the digital IOVDD supply performs a similar function, regulating the input voltage applied at the IOVDD pin to 1.8 V for the internal digital filtering. The serial interface signals always operate from the IOVDD supply seen at the pin. This means that if 3.3 V is applied to the IOVDD pin, the interface logic inputs and outputs operate at this level.

The AD7173-8 can be used across a wide variety of applications, providing high resolution and accuracy. A sample of these scenarios follows:

- Fast scanning of analog input channels using the internal mux
- Fast scanning of analog input channels using an external mux
- High resolution at lower speeds in either multichannel or ADC per channel applications
- Single ADC per channel; the fast low latency output allows further application specific filtering in an external microcontroller, DSP, or FPGA

POWER SUPPLIES

The AD7173-8 has three independent power supply pins: AVDD1, AVDD2, and IOVDD. The AD7173-8 has no specific requirements for a power supply sequence. When all power supplies are stable, a device reset is required; see the AD7173-8 Reset section for details on how to reset the device.

AVDD1 powers the crosspoint multiplexer and integrated analog and reference input buffers. AVDD1 is referenced to AVSS, and AVDD1 − AVSS = 3.3 V or 5 V. AVDD1 and AVSS can be a single 3.3 V or 5 V supply, or a ±1.65 V or ±2.5 V split supply. The split supply operation allows true bipolar inputs. When using split supplies, consider the absolute maximum ratings (see the Absolute Maximum Ratings section).

AVDD2 powers the internal 1.8 V analog LDO regulator. This regulator powers the ADC core. AVDD2 is referenced to AVSS, and AVDD2 to AVSS can range from 2 V (minimum) to 5.5 V (maximum).

IOVDD powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. IOVDD sets the voltage levels for the serial peripheral interface (SPI) of the ADC. IOVDD is referenced to DGND, and IOVDD to DGND can vary from 2 V (minimum) to 5.5 V (maximum).

Single Supply Operation (AVSS = DGND)

When the AD7173-8 is powered from a single supply that is connected to AVDD1, the supply can be either 3.3 V or 5 V. In this configuration, AVSS and DGND can be shorted together on one single ground plane. With this setup, an external level shifting circuit is required to use fully differential inputs to shift the common-mode voltage.

AVDD2 is the input to the internal voltage regulator. Connect AVDD2 to AVDD1 for convenience. Otherwise, if a separate supply is available in the system, a voltage from 2 V to 5.5 V can be applied. IOVDD can range from 2 V to 5.5 V in this unipolar input configuration.

Split Supply Operation (AVSS ≠ DGND)

The AD7173-8 device has the ability to operate with AVSS set to a negative voltage, allowing true bipolar inputs to be applied. This allows for a fully differential input signal centered around 0 V and eliminates the need for an external level shifting circuit. For example, with a 5 V split supply, AVDD1 = 2.5 V and AVSS = −2.5 V. In this use case, the AD7173-8 internally level shifts the signals, allowing the digital output to function between DGND (nominally 0 V) and IOVDD.

When using a split supply for AVDD1 and AVSS, the absolute maximum ratings must be considered (refer to the Absolute Maximum Ratings section). Ensure that IOVDD is set below 3.6 V to stay within the absolute maximum rating for the device.

DIGITAL COMMUNICATION

The AD7173-8 has a 3-wire or 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

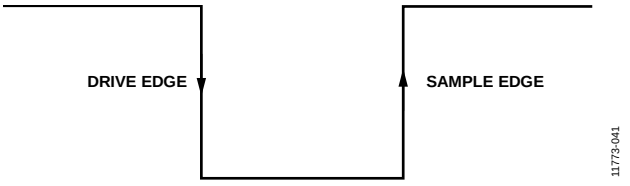


Figure 41. SPI Mode 3 SCLK Edges

Accessing the ADC Register Map

The communications register controls access to the full register map of the ADC. This register is an 8-bit write only register. On power-up or after a reset, the digital interface defaults to a state where it is expecting a write to the communications register; therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is being accessed and if the next operation is a read or write. The register address bits (RA[5:0]) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to its default state, where it expects a write operation to the communications register.

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire part, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high resets the digital interface to its default state and aborts any current operation.

Figure 42 and Figure 43 illustrate writing to and reading from a register by first writing the 8-bit command to the communications register followed by the data for the addressed register.

Reading the ID register is the recommended method for verifying correct communication with the part. The ID register is a read only register and contains the value 0x30DX for the AD7173-8. The communication register and ID register details are described in Table 8 and Table 9.

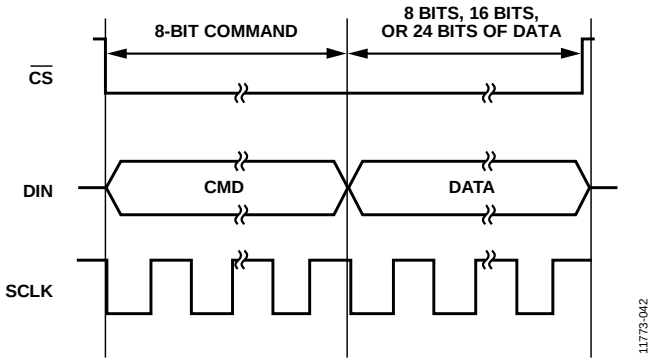


Figure 42. Writing to a Register (8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length Is Dependent on the Register Selected)

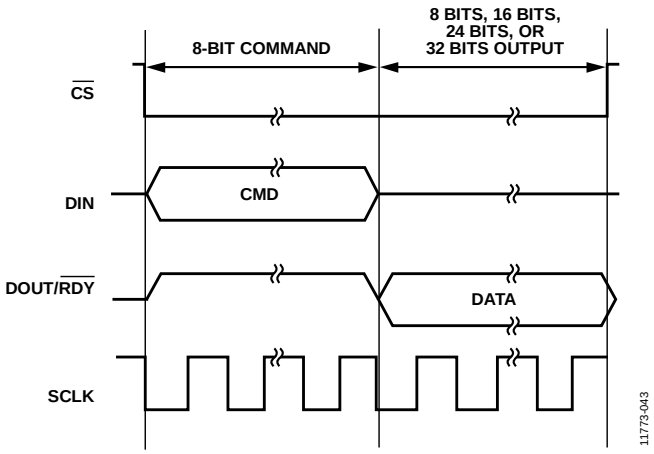


Figure 43. Reading from a Register (8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length on DOUT Is Dependent on the Register Selected)

AD7173-8 RESET

After a power-up cycle and when the power supplies are stable, a device reset is required. In situations where interface synchronization is lost, a device reset is also required. A write operation of at least 64 serial clock cycles with DIN high returns the ADC to the default state by resetting the entire device, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high sets the digital interface to the default state and halts any serial interface operation.

Table 8. Communications Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W

Table 9. ID Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x07	ID	[15:8]	ID[15:8]								0x30DX[1]	R
		[7:0]	ID[7:0]									

[1] X = don't care.

CONFIGURATION OVERVIEW

After power on-or reset, the AD7173-8 default configuration is as follows:

- Channel configuration. CH0 is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. Setup 0 is selected.
- Setup configuration. The input buffers are disabled, and the external reference is selected.
- ADC mode. Continuous conversion mode, the internal oscillator, and single cycle settling are enabled.
- Interface mode. CRC is disabled, and data + status output is disabled.

Note that only a few of the register setting options are shown; this list is just an example. For full register information, see the Register Details section.

Figure 44 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration (see Box A in Figure 44)
- Setup configuration (see Box B in Figure 44)
- ADC mode and interface mode configuration (see Box C in Figure 44)

Channel Configuration

The AD7173-8 has 16 independent channels and eight independent setups. The user can select any of the analog input pairs on any channel, as well as any of the eight setups for any channel, giving the user full flexibility in the channel configuration. This also allows per channel configuration when using eight differential inputs because each channel can have its own dedicated setup.

Channel Registers

The channel registers are used to select which of the 17 analog input pins (AIN0 to AIN16) are used as either the positive analog input or the negative analog input for that channel. This register also contains a channel enable/disable bit and the setup selection bits, which are used to pick which of the eight available setups are used for this channel.

When the AD7173-8 is operating with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 15. If a channel is disabled, it is skipped by the sequencer. Details of the channel register for Channel 0 are shown in Table 10.

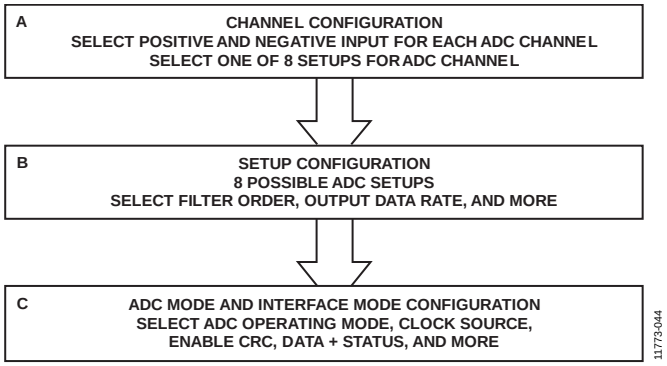


Figure 44. Suggested ADC Configuration Flow

Table 10. Channel 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL[2:0]			RESERVED		AINPOS0[4:3]		0x8001	RW
		[7:0]	AINPOS0[2:0]			AINNEG0						

ADC Setups

The AD7173-8 has eight independent setups. Each setup consists of the following four registers:

- Setup configuration register
- Filter configuration register
- Offset register
- Gain register

For example, Setup 0 consists of Setup Configuration Register 0, Filter Configuration Register 0, Offset Register 0, and Gain Register 0. Figure 45 shows the grouping of these registers The setup is selectable from the channel registers detailed in the Channel Configuration section. This allows each channel to be assigned to one of 8 separate setups. Table 11 through Table 14 show the four registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 7.

Setup Configuration Registers

The setup configuration registers allow the user to select the output coding of the ADC by selecting between bipolar and unipolar. In bipolar mode, the ADC accepts negative differential input voltages, and the output coding is offset binary. In unipolar mode, the ADC accepts only positive differential voltages, and the coding is straight binary. In either case, the input voltage must be within the AVDD1/AVSS supply voltages. The user can also select the reference source using this register. Four options are available: an internal 2.5 V reference, an external reference connected between the REF+ and REF− pins, an external reference connected between AIN0/REF2− and AIN1/REF2+, or AVDD1 − AVSS. The analog input buffers and reference input buffers for the setup can also be enabled using this register.

Filter Configuration Registers

The filter configuration register selects which digital filter is used at the output of the ADC modulator. The order of the filter and the output data rate is selected by setting the bits in this register. For more information, see the Digital Filters section.

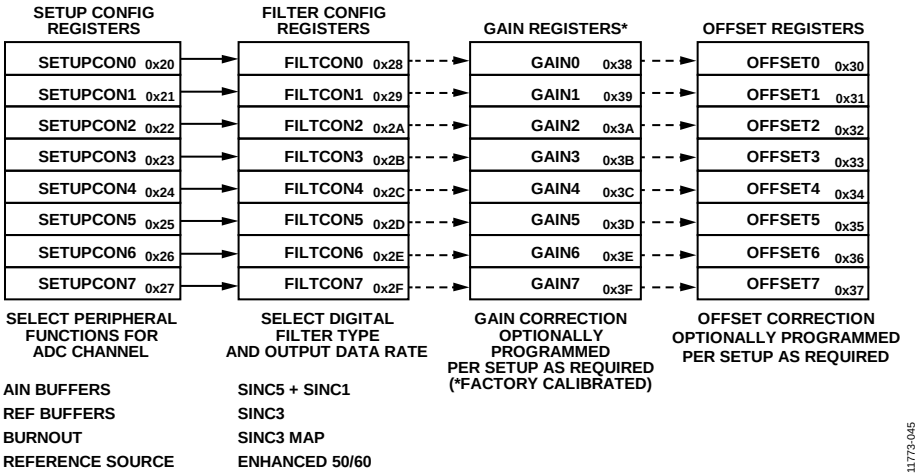


Figure 45. ADC Setup Register Grouping

Table 11. Setup Configuration 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x20	SETUPCON0	[15:8]	RESERVED			BI_UNIPOLAR0	REF_BUF 0[1:0]		AIN_BUF 0[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN0	BUFCHOPMAX0	REF_SEL0		RESERVED					

Table 12. Filter Configuration 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x28	FILTCON0		SINC3_MAP0	RESERVED			ENHFILTEN0	ENHFILT0			0x0000	RW
				ORDER0		ODR0						

Table 13. Offset Configuration 0 Register Bit Map

Reg	Name	Bits	Bit[23:0]	Reset	RW
0x30	OFFSET0	[23:0]	OFFSET0[23:0]	0x800000	RW

Table 14. Gain Configuration 0 Register Bit Map

Reg	Name	Bits	Bit[23:0]	Reset	RW
0x38	GAIN0	[23:0]	GAIN0[23:0]	0x5XXXX0	RW

Offset Registers

The offset register holds the offset calibration coefficient for the ADC. The power-on reset value of the offset register is 0x800000. The offset register is a 24-bit read/write register. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user or if the offset register is written to by the user.

Gain Registers

The gain register is a 24-bit register that holds the gain calibration coefficient for the ADC. The gain registers are read/write registers. These registers are configured at power-on with factory calibrated coefficients. Therefore, every device has different default coefficients. The default value is automatically overwritten if a system full-scale calibration is initiated by the user or if the gain register is written to by the user. For more information on calibration, see the Operating Modes section.

ADC Mode and Interface Mode Configuration

The ADC mode register and the interface mode register configure the core peripherals for use by the AD7173-8 and the mode for the digital interface.

ADC Mode Register

The ADC mode register is used primarily to set the conversion mode of the ADC to either continuous or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes. In addition, this register contains the clock source select bits and the internal reference enable bits. The reference select bits are contained in the setup configuration registers (see the ADC Setups section for more information).

Interface Mode Register

The interface mode register configures the digital interface operation. This register allows the user to control data-word length, CRC enable, data + status read and continuous read mode.

The details of both registers are shown in Table 15 and Table 16. For more information, see the Digital Interface section.

Table 15. ADC Mode Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADCMODE	[15:8]	REF_EN	RESERVED	SING_CYC	RESERVED		DELAY			0x2000	RW
		[7:0]	RESERVED	MODE			CLOCKSEL		RESERVED			

Table 16. Interface Mode Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x02	IFMODE	[15:8]	RESERVED			ALT_SYNC	IOSTRENGTH	$\overline{\text{HIDE\_DELAY}}$	RESERVED	DOUT_RESET	0x0000	RW
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	RESERVED	CRC_EN		RESERVED	WL16		

Understanding Configuration Flexibility

The most straightforward implementation of the AD7173-8 is to use eight differential inputs with adjacent analog inputs and run all of them with the same setup, gain correction, and offset correction register. In this case, the user selects the following differential inputs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, AIN8/AIN9. AIN10/AIN11, AIN12/AIN13, AIN14/AIN15. In Figure 46, the registers shown in black font must be programmed for such a configuration. The registers that are shown in gray font are redundant in this configuration.

Programming the gain and offset registers is optional for any use case, as indicated by the dashed lines between the register blocks.

An alternative way to implement these eight fully differential inputs is by taking advantage of the eight available setups. Motivation for doing this includes having is a different speed/noise requirement on some of the eight differential inputs vs. other inputs, or there may be a specific offset or gain correction for particular channels. Figure 47 shows how each of the differential inputs may use a separate setup, allowing full flexibility in the configuration of each channel.

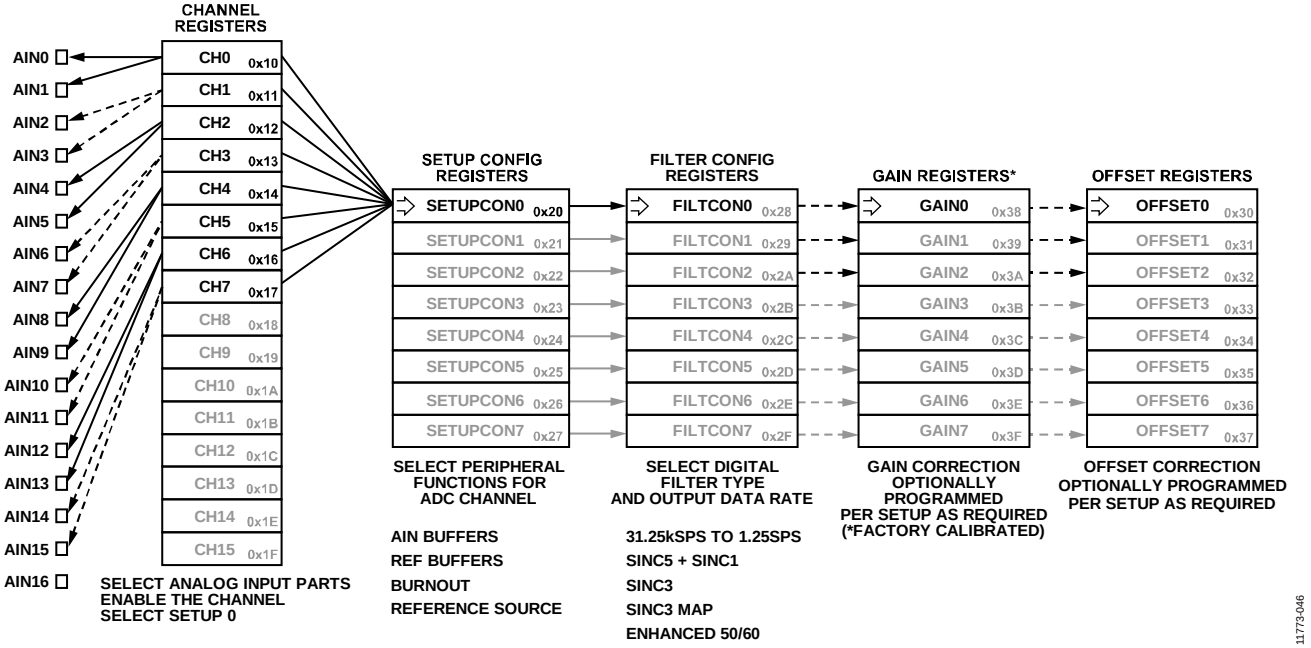


Figure 46. Eight Fully Differential Inputs, All Using a Single Setup (SETUPCON0; FILTCON0; GAIN0; OFFSET0)

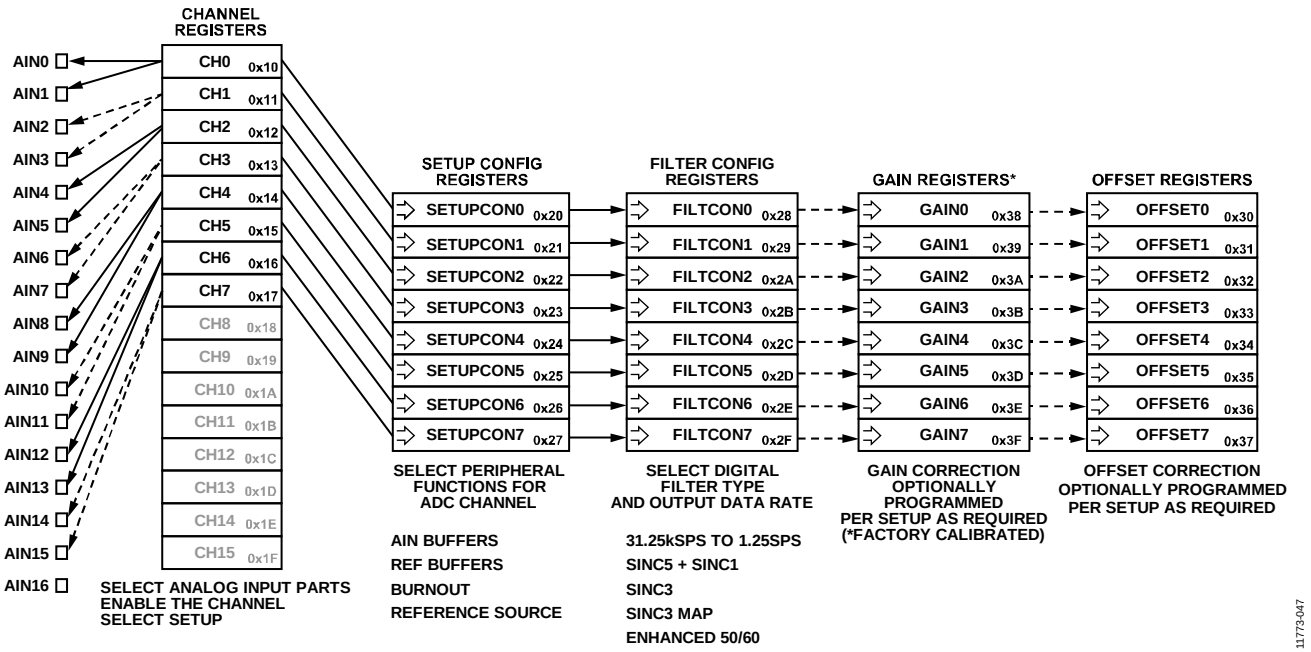


Figure 47. Eight Fully Differential Inputs with a Setup per Channel

Figure 48 shows an example of how the channel registers span between the analog input pins and the setup configurations downstream. In this random example, seven differential inputs and two single-ended inputs are required. The single-ended inputs are the AIN8/AIN16 and AIN15/AIN16 combinations. The first five differential input pairs (AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, AIN9/AIN10) use the same setup: SETUPCON0. The two single-ended input pairs (AIN8/AIN16 and AIN15/AIN16) are set up as a diagnostics; therefore, use a separate setup: SETUPCON1. The final two differential inputs (AIN11/AIN12 and AIN13/AIN14) also use a separate setup: SETUPCON2. Given that three setups are selected for use, the SETUPCON0, SETUPCON1, and SETUPCON2 registers are programmed as required, and the FILTCON0, FILTCON1, and FILTCON2 registers are also programmed as desired. Optional gain and offset correction can be employed on a per setup basis by programming the GAIN0, GAIN1, and GAIN2 registers and the OFFSET0, OFFSET1, and OFFSET2 registers.

In the example shown in Figure 48, the CH0 to CH8 registers are used. Setting the MSB in each of these registers, the CH_EN0 to CH_EN8 bits enable the nine combinations via the cross point mux. When the AD7173-8 converts, the sequencer transitions in ascending sequential order from CH0 to CH1 to CH2, and then on to CH8 before looping back to CH0 to repeat the sequence.

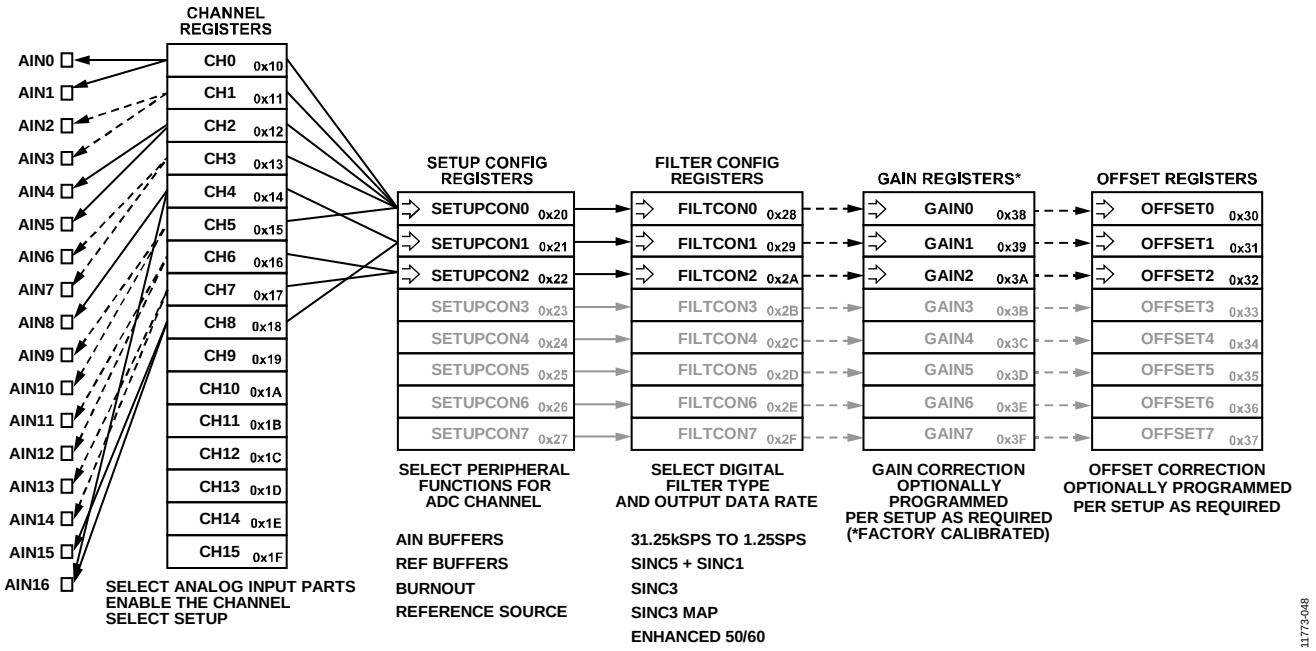


Figure 48. Mixed Differential and Single-Ended Configuration Using Multiple Shared Setups

CIRCUIT DESCRIPTION

ANALOG INPUT

Buffered Analog Input

The AD7173-8 integrates precision unity gain buffers on the ADC inputs. The output of the integrated cross point mux is connected to the ADC via these precision buffers. The buffers provide the benefit of giving the user high input impedance and fully drive the internal ADC switch capacitor sampling network.

There is a buffer on both the positive and negative analog inputs to the ADC. The input signals of the AIN pair that is selected via control of the cross point mux (BUF+, BUF−) pass to the buffer inputs, which drive the ADC sampling capacitor circuitry. Each analog input buffer has an input voltage range as shown in Figure 49. Each buffer can operate with an input signal down to AVSS (analog ground) or up to an input voltage of 1.1 V from the AVDD1 supply.

Fully Differential Inputs

The AIN0 to AIN16 analog inputs are connected to a cross point mux. Any combination of signals can be used to create an analog input pair. This allows the user to select eight fully differential inputs or 16 single-ended inputs. If all signals to the AD7173-8 are fully differential, it is recommended that the traces of the inputs be of the same length. The most reliable and efficient way to do this is by using adjacent input pins as the differential pair. All analog inputs decoupling capacitors connect to AVSS.

Single-Ended Inputs

The user can also choose to measure 16 different single-ended analog inputs. In this case, each of the analog inputs is converted as being the difference between the single-ended input to be measured and a set analog input common pin. Because there is a cross point mux, the user can set any of the analog inputs as the common pin. An example of such a scenario is to connect the AIN16 pin to AVSS or to the REFOUT voltage (that is, AVSS + 2.5 V) and select this input when configuring the cross point mux. When using the AD7173-8 with single-ended inputs, the INL specification is degraded.

When the user requires a buffered input in either the fully differential or single-ended case, the user is required to turn on the analog input buffers as a pair. This means that, even where an input pin is connected to AVSS, the input buffer of this channel is turned on if the other pin making up the differential input is going to be buffered.

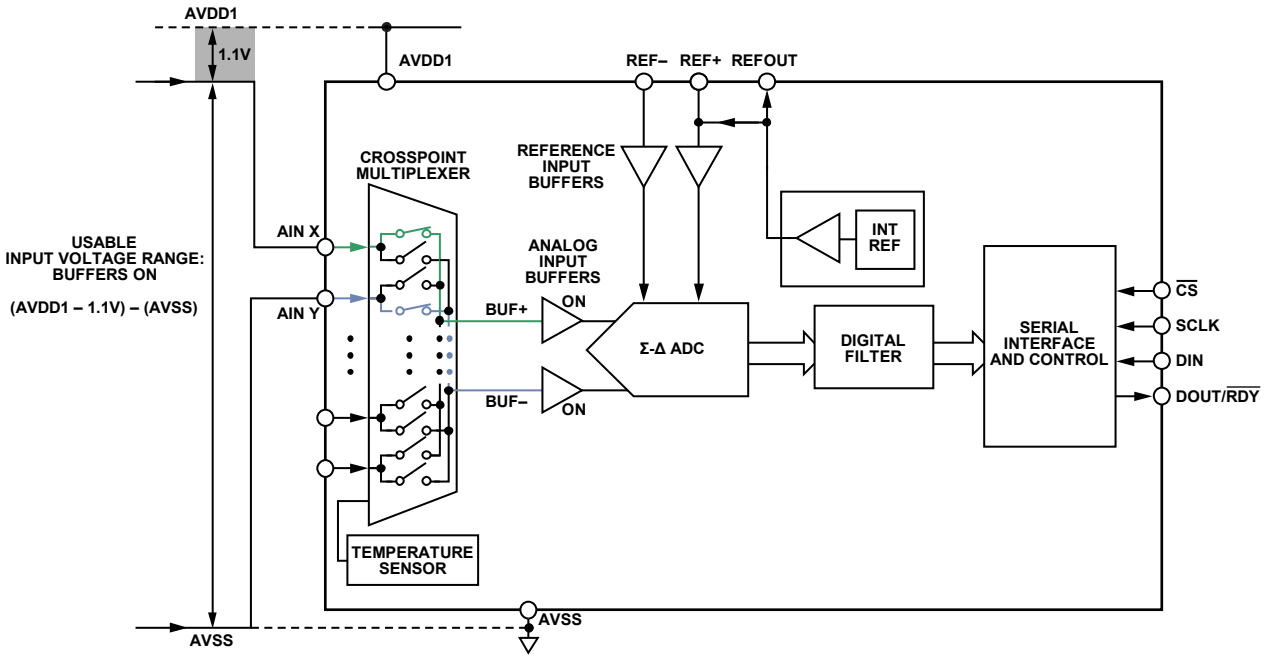


Figure 49. Analog Input Voltage Range with Analog Input Buffers Enabled

Buffer Chopping, Noise, and Input Current

Each analog input buffer amplifier is fully chopped, meaning that it minimizes the offset error drift and 1/f noise of the signal chain. The 1/f noise profile is shown in Figure 51.

The noise performance of the buffer at certain output data rates can be improved by increasing the chopping rate of the buffer, giving a corresponding increase in input current. This is done by setting the BUFCHOPMAXx bit in the setup configuration register of the selected setup.

Running with Single Cycle = 0

The output data rate can be maximized when using only a single channel by setting the SING_CYC bit to 0. However, the analog input current changes in magnitude, depending on the output data rate selected. In this condition, the input current increases by approximately 32× for output data rates selected at >2.6 kSPS. Set the SING_CYC bit to 0 only in this specific use case. Figure 52 and Figure 53 show rms noise and input current vs. output data rate for various conditions.

Using External Buffers

The analog input buffers can be disabled. When they are disabled, the input voltage range on the analog inputs is AVDD1 – AVSS. The analog input switched capacitor input is then exposed to the user. A suitable external amplifier is required to sufficiently drive and settle the analog input in such cases. The CS1 and CS2 capacitors each have a magnitude in the order of a number of picofarads (pF). This capacitance is the combination of both the sampling capacitance and the parasitic capacitance.

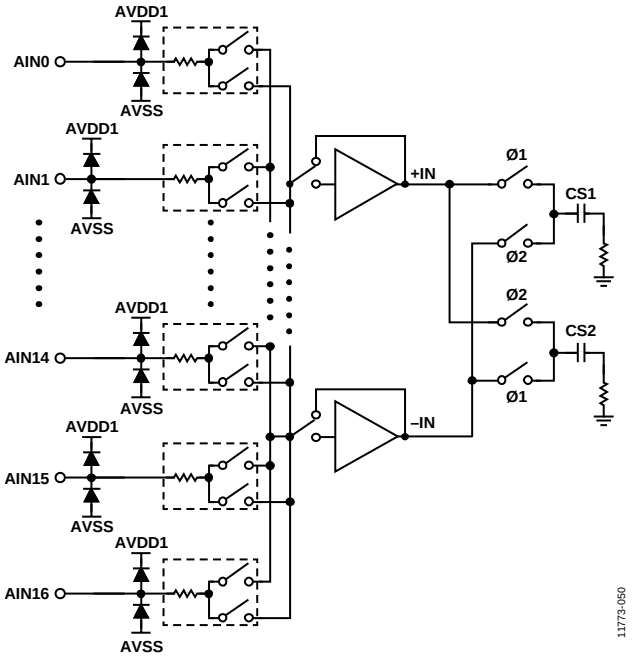


Figure 50. Simplfied Analog Input Circuit

The average input current to the AD7173-8 changes linearly with the differential input voltage at a rate of 6 µA/V. Each analog input must be buffered externally, not only to provide the varying input current with differential input amplitude, but also to settle the switched capacitor input to allow accurate sampling. The simplified analog input circuit for this situation is shown in Figure 50.

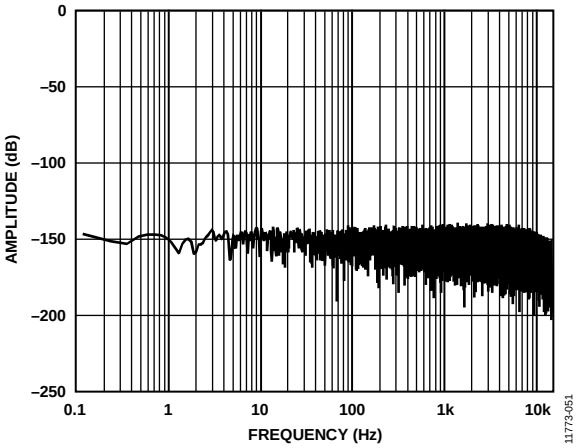


Figure 51. Shorted Input FFT

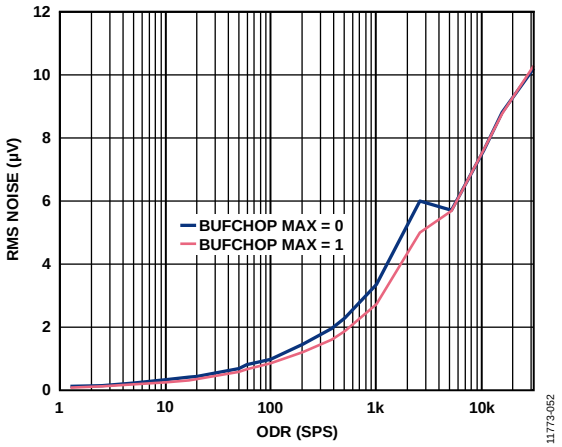


Figure 52. RMS Noise vs. Output Data Rate (Sinc5 + Sinc1 Filter)

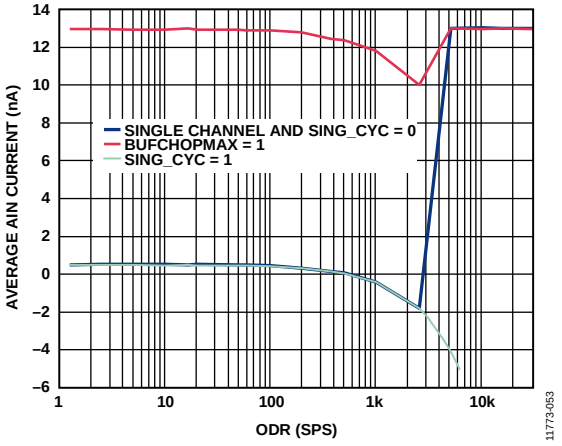


Figure 53. Typical Analog Input Current vs. Output Data Rate (2.5 V Common Mode)

REFERENCE OPTIONS

The AD7173-8 offers the user the option of either supplying an external reference to the REF+ and REF− pins of the device or allowing the use of the internal 2.5 V, low noise, low drift reference. Select the reference source to be used by the analog input by setting the REF_SELx bits (Bits[5:4]) in the setup configuration registers appropriately. The structure of the Setup Configuration 0 register is shown in Table 17. The AD7173-8 defaults on power-up to use of an external reference.

External Reference

The AD7173-8 has a fully differential reference input applied through the REF+ and REF− pins. Standard low noise, low drift voltage references, such as the ADR445, ADR444, and ADR441, are recommended for use. Apply the external reference to the AD7173-8 reference pins as shown in Figure 54. Decouple the output of any external reference is to AVSS. As shown in Figure 54, the ADR441 output is decoupled with a 0.1 µF capacitor at its output for stability purposes. The output is then connected to a 4.7 µF capacitor, which acts as a reservoir for any dynamic charge required by the ADC, and followed by a 0.1 µF decoupling capacitor at the REF+ input. This capacitor is placed as close as possible to the REF+ and REF− pins. The REF− pin is connected directly to the AVSS potential.

Internal Reference

The AD7173-8 includes its own low noise, low drift voltage reference. On power-up, the internal reference is disabled by default and a register write is required to select it as the reference source for the ADC. Write to the REF_EN bit (Bit 15) in the ADC mode register to enable it (see Table 18). The internal reference has a 2.5 V output and is output on the REFOUT pin after the REF_EN bit is set in the ADC mode register. Decouple the internal reference to AVSS with a 0.1 µF capacitor.

The REFOUT signal is buffered prior to being output to the pin. The signal can be used externally in the circuit as a common-mode source for external amplifier configurations.

CLOCK SOURCE

The AD7173-8 requires a master clock of 2 MHz. The AD7173-8 can use one of the following sources as its sampling clock:

- Internal oscillator
- External crystal (use a 16 MHz crystal, automatically divided internally to set the 2 MHz clock)
- External clock source

All output data rates listed in the data sheet relate to a master clock rate of 2 MHz. Using a lower clock frequency from, for example, an external source proportionally scales any listed data rate. To achieve the specified data rates, particularly rates for rejection of 50 Hz and 60 Hz, a use a 2 MHz clock. The source of the master clock is selected by setting the CLOCKSEL bits in the ADCMODE register, as shown in Table 25. The default, on power-up and reset, is to operate with the internal oscillator.

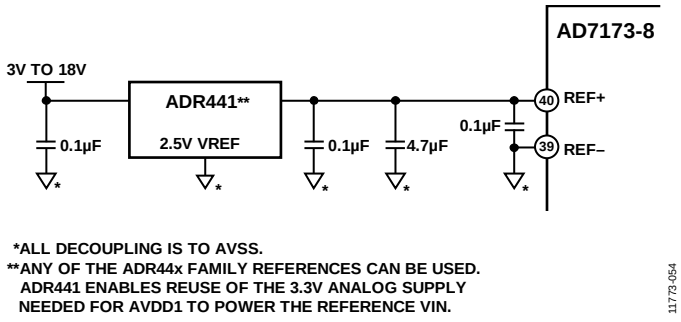


Figure 54. External Reference ADR441 Connected to AD7173-8 Reference Pins

Table 17. Setup Configuration 0 Register

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x20	SETUPCON0	[15:8]	RESERVED		RESERVED	BI_UNIPOLAR	REF_BUF 0[1:0]		AIN_BUF 0[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN	BUFCHOPMAX0	REF_SEL0		RESERVED					0

Table 18. ADC Mode Register

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADCMODE	[15:8]	INT_REF_EN	RESERVED	SING_CYC	RESERVED		DELAY			0x2000	RW
		[7:0]	RESERVED	MODE			CLOCKSEL		RESERVED			

Internal Oscillator

The internal oscillator is used as the ADC master clock by default. The clock used for the ADC sampling is 2 MHz (this is divided down from a higher frequency in the case of the internal oscillator use). It is the default clock source for the AD7173-8 and is specified with an accuracy of ±2.5%.

There is an option to allow the internal clock oscillator to be output on the XTAL2/CLKIO pin. The clock output is driven to the IOVDD logic level. Use of this option may affect the dc performance of the AD7173-8 due to a disturbance that may be introduced by the output driver. The extent to which the performance is affected depends on the IOVDD voltage supply. Higher IOVDD voltages create a wider logic output swing from the driver and may affect performance to a greater extent. This effect may be further exaggerated if the IOSTRENGTH bit (Register 0x02, Bit 11) is set at higher IOVDD levels (see Table 26 for more information).

External Crystal

If higher precision, lower jitter clock sources are required, the AD7173-8 has the ability to use an external crystal to generate the master clock. For the AD7173-8 the required crystal frequency is 16 MHz. Internally this is automatically divided to create the 2 MHz needed for sampling the ADC input.

The crystal is connected to the XTAL1 and XTAL2/CLKIO pins. A recommended crystal for use is the FA-20H: a 16 MHz, 10 ppm, 9 pF crystal from Epson-Toyocom, which is available in a surface-mounted package.

As shown in Figure 55, allow two capacitors to be inserted from the traces connecting the crystal to the XTAL1 and XTAL2/CLKIO pins. These capacitors enable circuit tuning. Connect these capacitors to the DGND pin. The value for these capacitors depends on the length and capacitance of the trace connections between the crystal and the XTAL1 and XTAL2/CLKIO pins. Therefore, the values of these capacitors differ depending on the PCB layout and the crystal employed. As a result, empirical testing of the circuit is required.

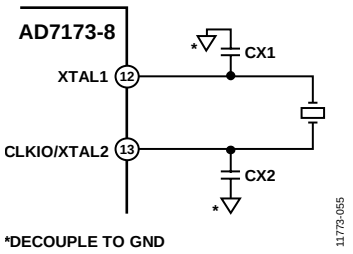


Figure 55. External Crystal Connections

External Clock

The AD7173-8 can also use an externally supplied clock. In systems where this is desirable, the external clock is routed to the XTAL2/CLKIO pin. In this configuration, the XTAL2/CLKIO pin accepts the externally sourced clock and routes it to the modulator. The logic level of this clock input is defined by the voltage applied to the IOVDD pin.

DIGITAL FILTERS

The AD7173-8 provides the following three flexible filter options to allow optimization of settling time, noise, and rejection:

- Sinc5 + sinc1 filter
- Sinc3 filter
- Enhanced 50 Hz and 60 Hz rejection filters

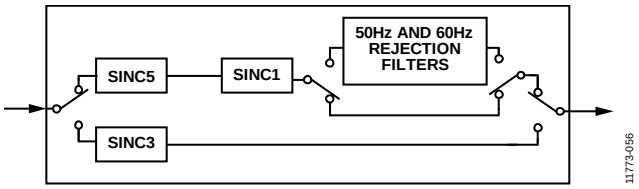


Figure 56. Digital Filter Block Diagram

The filter and output data rate are configured by setting the appropriate bits in the filter configuration register for the selected setup. When using the sinc5 + sinc1 filter, it is possible to select different output data rates per channel. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels. See the Register Details section for more information.

SINC5 + SINC1 FILTER

The sinc5 + sinc1 filter is targeted at fast switching multiplexed applications and achieves single cycle settling at output data rates of 2.6 kSPS and lower. The sinc5 block output is fixed at the maximum rate of 31.25 kSPS, and the sinc1 block output data rate can be varied to control the final ADC output data rate. Figure 57 shows the frequency domain response of the sinc5 + sinc1 filter at a 50 SPS output data rate. The sinc5 + sinc1 filter has a slow roll-off over frequency and narrow notches.

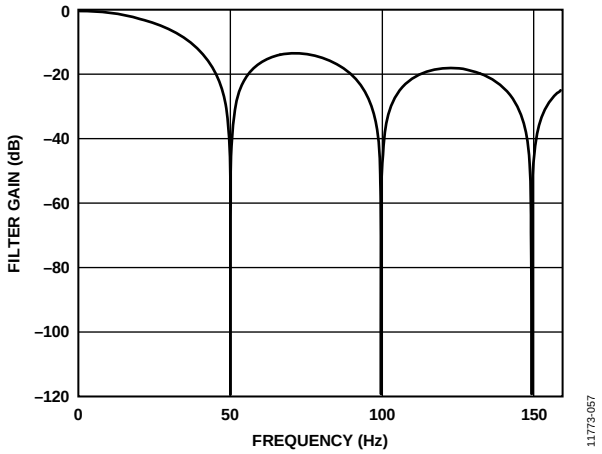


Figure 57. Sinc5 + Sinc1 Filter Response at 50 SPS ODR

The output data rates with the accompanying settling time and rms noise for the sinc5 + sinc1 filter are listed in Table 19.

Table 19. Output Data Rate (ODR), Settling Time (t_{SETTLE}), and Noise Using the Sinc5 + Sinc1 Filter

Default Output Data Rate (SPS/Channel);[1] SING_CYC = 1 or with Multiple Channels Enabled	Output Data Rate (SPS);[1] SING_CYC = 0 and Single Channel Enabled	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)	Noise (µV p-p)[2]	Effective Resolution with 5 V Reference (Bits)	Peak-to-Peak Resolution with 5 V Reference (Bits)
6211	31,250	161 µs	31250	8.0	67	20.2	17.5
5181	15,625	193 µs	15625	6.9	52	20.4	17.7
4444	10,417	225 µs	10417	6.0	40	20.7	17.9
3115	5208	321 µs	5208	4.5	30	21.1	18.3
2597	2597	385 µs	3890	3.9	27	21.3	18.5
1007	1007	993 µs	1156	2.2	15	22.2	19.3
503.8	503.8	1.99 ms	539	1.5	11	22.7	19.9
381	381	2.63 ms	401	1.3	8.9	22.9	20.1
200.3	200.3	4.99 ms	206	0.99	6.6	23.3	20.5
100.5	100.5	9.95 ms	102	0.71	5.1	23.8	21
59.52	59.52	16.8 ms	60	0.57	3.3	24	21.4
49.68	49.68	20.13 ms	50	0.52	3	24	21.4
20.01	20.01	49.98 ms	20	0.32	1.7	24	22.2
16.63	16.63	60.13 ms	16.67	0.3	1.6	24	22.4
10	10	100 ms	10	0.22	1.1	24	22.7
5	5	200 ms	5	0.15	0.75	24	23.4
2.5	2.5	400 ms	2.5	0.08	0.32	24	24
1.25	1.25	800 ms	1.25	0.07	0.32	24	24

[1] The settling time (t_{SETTLE}) is rounded to the nearest microsecond (µs). This is reflected in the output data rate and switching rate. Switching rate = 1 ÷ t_{SETTLE}.
[2] 1000 samples.

SINC3 FILTER

The sinc3 filter achieves the best single-channel noise performance at lower rates and is, therefore, most suitable for single-channel applications. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels. The sinc3 filter always has a settling time equal to

$$t_{SETTLE} = 3/Output\ Data\ Rate$$

Figure 58 shows the frequency domain filter response for the sinc3 filter. The sinc3 filter has good roll-off over frequency and has wide notches for good notch frequency rejection.

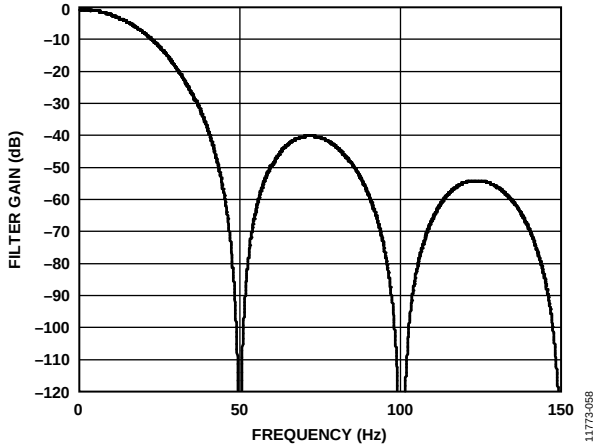


Figure 58. Sinc3 Filter Response

The output data rates with the accompanying settling time and rms noise for the sinc3 filter are shown in Table 20.

It is possible to fine-tune the output data rate for the sinc3 filter by setting the SINC3_MAPx bit in the Filter Configuration x register. If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the sinc3 filter. All other options are eliminated. The data rate, when on a single channel, can be calculated using the following equation:

$$Output\ Data\ Rate = \frac{f_{MOD}}{32 \times FILTCONx[14:0]}$$

where:

f_{MOD} is the modulator rate and is equal to 1 MHz.
FILTCONx[14:0] is the contents of the filter configuration register, excluding the MSB.

For example, an output data rate of 50 SPS can be achieved with SINC3_MAPx enabled by setting the FILTCONx[14:0] bits to a value of 625.

Table 20. Output Data Rate (ODR), Settling Time (t_{SETTLE}), and Noise Using the Sinc3 Filter

Default Output Data Rate (SPS/Channel);[1] SING_CYC = 1 or with Multiple Channels Enabled	Output Data Rate (SPS);[1] SING_CYC = 0 and Single Channel Enabled	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)	Noise (µV p-p)	Effective Resolution with 5 V Reference (Bits)	Peak-to-Peak Resolution with 5 V Reference (Bits)
10417	31,250	96 µs	31,250	210	1665	15.5	12.8
5208	15,625	192 µs	15,625	27	206	18.5	15.7
3472	10,417	288 µs	10,417	7.8	63	20.3	17.5
1736	5208	576 µs	5208	3.6	28	21.4	18.7
868	2,604	1.15 ms	2,604	2.4	20	22	19.2
336	1,008	2.98 ms	1,008	1.5	12	22.7	19.9
168	504	5.95 ms	504	1.1	8	23.1	20.4
133.53	400.6	7.49 ms	400.6	1	7.6	23.3	20.5
67.76	200.3	14.99 ms	200.3	0.73	5.1	23.8	21.2
33.5	100.5	29.85 ms	100.5	0.55	3.5	24	21.4
19.99	59.98	50.02 ms	59.98	0.44	2.5	24	21.6
16.67	50	60 ms	50	0.42	2.3	24	21.7
6.67	20.01	149.93 ms	20.01	0.25	1.2	24	22.4
5.56	16.67	179.96 ms	16.67	0.21	1.1	24	22.6
3.33	10	300 ms	10	0.16	0.83	24	22.9
1.67	5	600 ms	5	0.11	0.56	24	23.4
0.83	2.5	1.2 sec	2.5	0.08	0.41	24	24
0.42	1.25	2.4 sec	1.25	0.07	0.27	24	24

[1] The settling time (t_{SETTLE}) is rounded to the nearest microsecond (µs). This settling time is reflected in the output data rate and switching rate. Switching rate = 1 ÷ t_{SETTLE}.

SINGLE CYCLE SETTLING

By default, the AD7173-8 is configured with the SING_CYC bit in the ADC Mode Register. This means that only fully settled data is output, thus putting the ADC into a single cycle settling mode. This mode achieves single cycle settling by reducing the output data rate to be equal to the settling time of the ADC for the selected output data rate. This bit has no effect with the sinc5 + sinc1 at output data rates of 2.6 kSPS and lower or when multiple channels are enabled.

Figure 59 shows the same step on the analog input but with single cycle settling enabled. At least a single cycle is required for the output to be fully settled. The output data rate is equal to the settling time of the filter at the selected output data rate.

Figure 59. Step Input with Single Cycle Settling

Figure 60 shows a step on the analog input with this mode disabled, one channel enabled and the Sinc3 filter selected. At least three cycles are required after the step change for the output to reach the final settled value. However, the ADC can then output a new conversion result at the higher rate of 1/ODR.

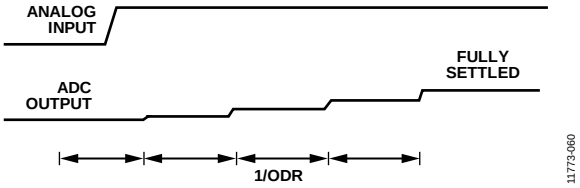


Figure 60. Step Input Without Single Cycle Settling

ENHANCED 50 Hz AND 60 Hz REJECTION FILTERS

The enhanced filters are designed to provide rejection of 50 Hz and 60 Hz simultaneously and to allow the user to trade off settling time and rejection. These filters can operate up to 27.27 SPS or can reject up to 90 dB of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz interference. These filters are realized by post filtering the output of the sinc5 + sinc1 filter. For this reason, the sinc5 + sinc1 filter must be selected when using the enhanced filters. Table 21 shows the output data rates with the accompanying settling time, rejection, and rms noise. Figure 61 to Figure 68 show the frequency domain plots of the responses from the enhanced filters.

Table 21. Enhanced Filter Output Data Rate (ODR), Noise, Settling Time (t_{SETTLE}), and Rejection Using the Enhanced Filters

Output Data Rate (SPS)	Settling Time (ms)	Simultaneous Rejection of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz (dB)[1]	Noise (µV rms)	Noise (µV p-p)	Effective Resolution (Bits)	Peak-to-Peak Resolution (Bits)	Reference
27.27	36.67	47	0.45	3.6	24.4	21.4	See Figure 61 and Figure 64
25	40.0	62	0.44	3.6	24.4	21.4	See Figure 62 and Figure 65
20	50.0	85	0.41	3.0	24.5	21.7	See Figure 63 and Figure 66
16.67	60.0	90	0.41	3.0	24.5	21.7	See Figure 67 and Figure 68

[1] Master clock = 2 MHz.

50 Hz and 60 Hz Rejection Filter Frequency Domain Plots

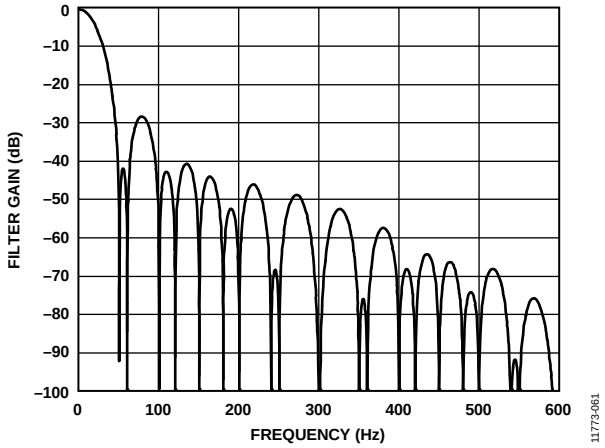


Figure 61. 27.27 SPS ODR, 36.67 ms Settling Time

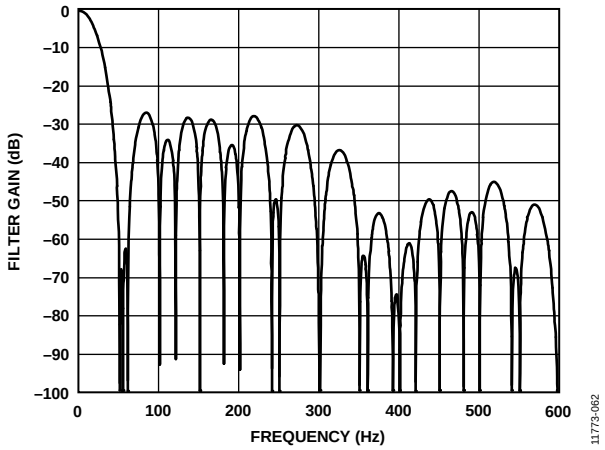


Figure 62. 25 SPS ODR, 40 ms Settling Time

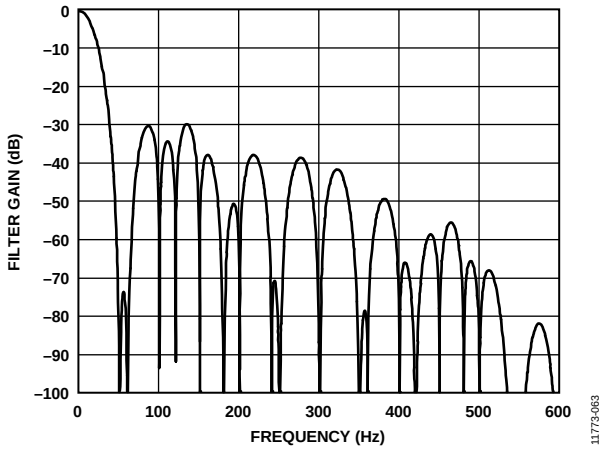


Figure 63. 20 SPS ODR, 50 ms Settling Time

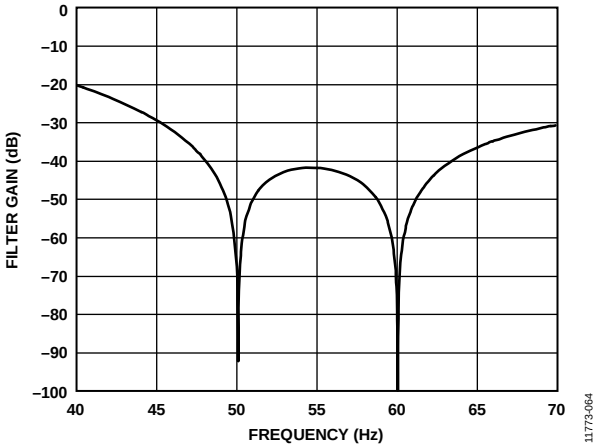


Figure 64. 27.27 SPS ODR, 36.67 ms Settling Time

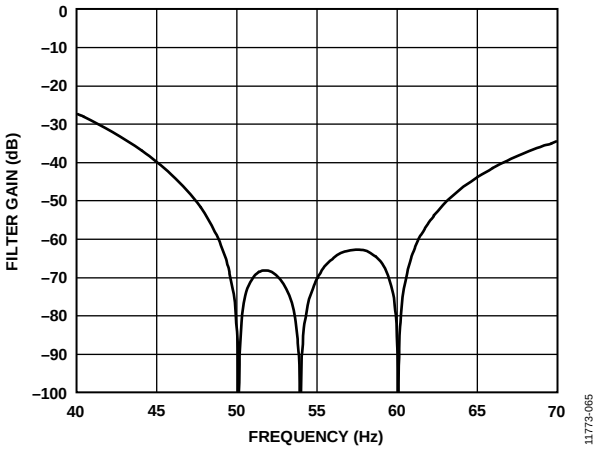


Figure 65. 25 SPS ODR, 40 ms Settling Time

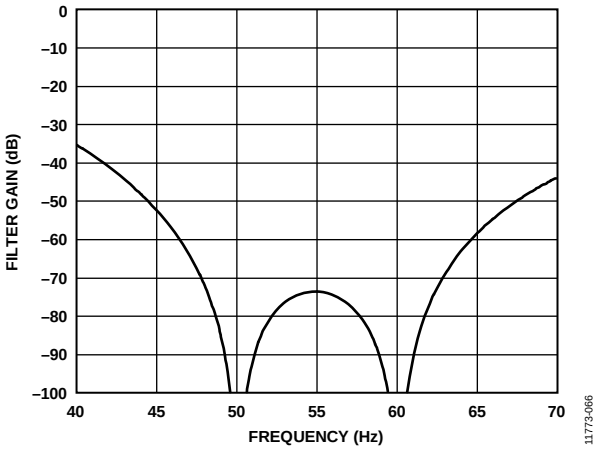


Figure 66. 20 SPS ODR, 50 ms Settling Time

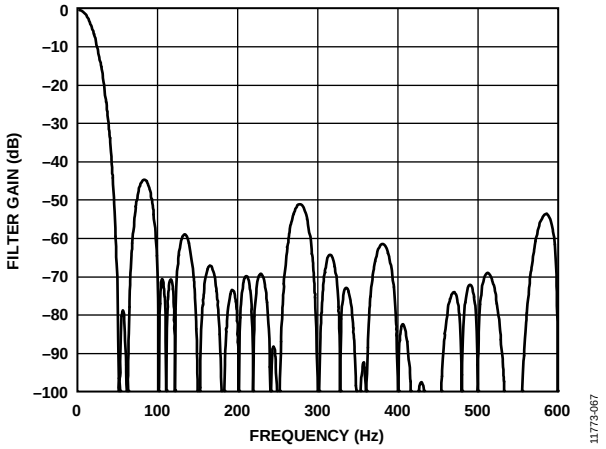


Figure 67. 16.667 SPS ODR, 60 ms Settling Time

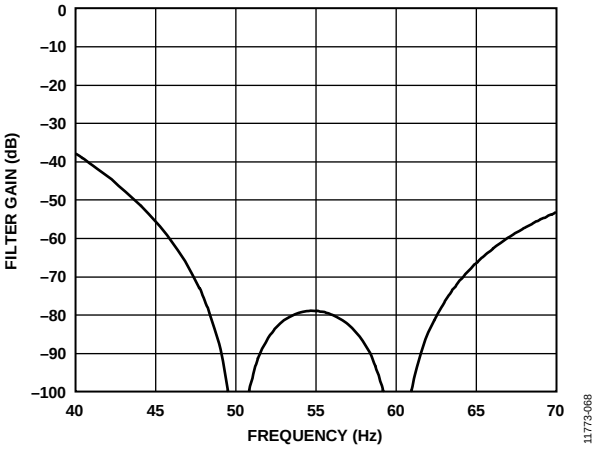


Figure 68. 16.667 SPS ODR, 60 ms Settling Time

OPERATING MODES

CONTINUOUS CONVERSION MODE

Continuous conversion (see Figure 69) is the default power-up mode. The AD7173-8 converts continuously, and the RDY bit in the status register goes low each time a conversion is complete. If CS is low, the DOUT/RDY line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. When the data-word has been read from the data register, DOUT/RDY goes high. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion.

When several channels are enabled, the ADC automatically sequences through the enabled channels, performing one conversion on each channel. When all channels are converted, the sequence starts again with the first channel. The channels are converted, in order, from lowest enabled channel to highest enabled channel. The data register is updated as soon as each conversion is available. The DOUT/RDY pin pulses low each time a conversion is available. The user must then read the conversion result while the ADC converts the next enabled channel; otherwise, the new conversion result is lost.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion data, are output each time the data register is read. The status register indicates the channel to which the conversion corresponds.

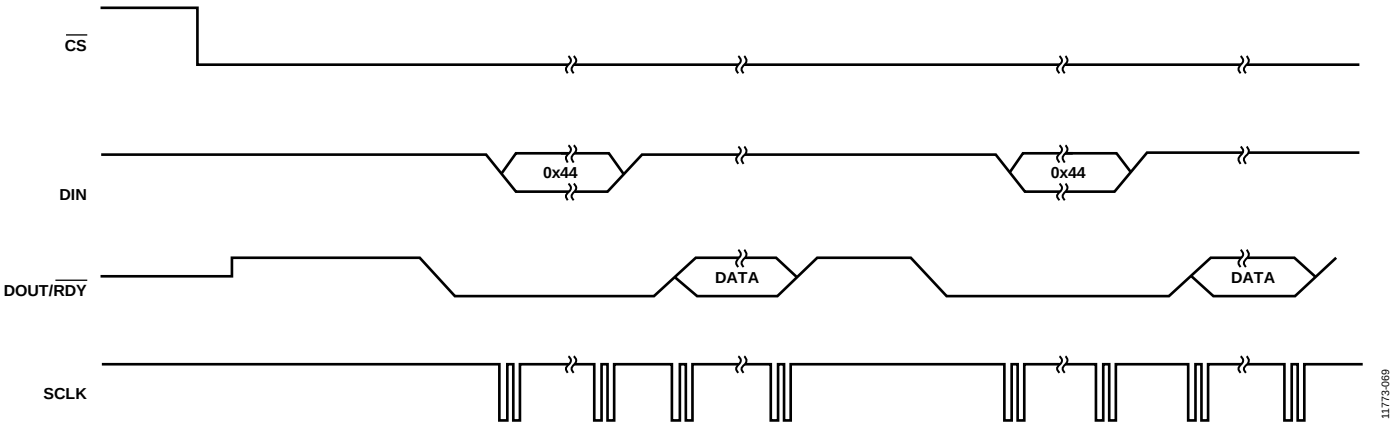


Figure 69. Continuous Conversion Mode

CONTINUOUS READ MODE

In continuous read mode (see Figure 70), it is not required that the communications register be written to before the ADC data is read. Instead, apply the required number of SCLKs after DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion. When the conversion is read, DOUT/$\overline{\text{RDY}}$ returns high until the next conversion is available. In this mode, the data can be read only once. The user must also ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion or if insufficient serial clocks are applied to the AD7173-8 to read the word, the serial output register is reset shortly before the next conversion is complete, and the new conversion is placed in the output serial register. To use continuous read mode, the ADC must be configured for continuous conversion mode.

To enable continuous read mode, set the CONTREAD bit in the interface mode register. When this bit is set, the only serial interface operations possible are reads from the data register. To exit continuous read mode, issue a dummy read of the ADC data register command (0x44) while $\overline{\text{RDY}}$ is low. Alternatively, apply a software reset, that is, 64 SCLKs with $\overline{\text{CS}}$ = 0 and DIN = 1. This resets the ADC and all register contents. These are the only commands that the interface recognizes after it is placed in continuous read mode. Hold DIN low in continuous read mode until an instruction is to be written to the device.

If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if the DATA_STAT bit is set in the interface mode register. The status register indicates the channel to which the conversion corresponds.

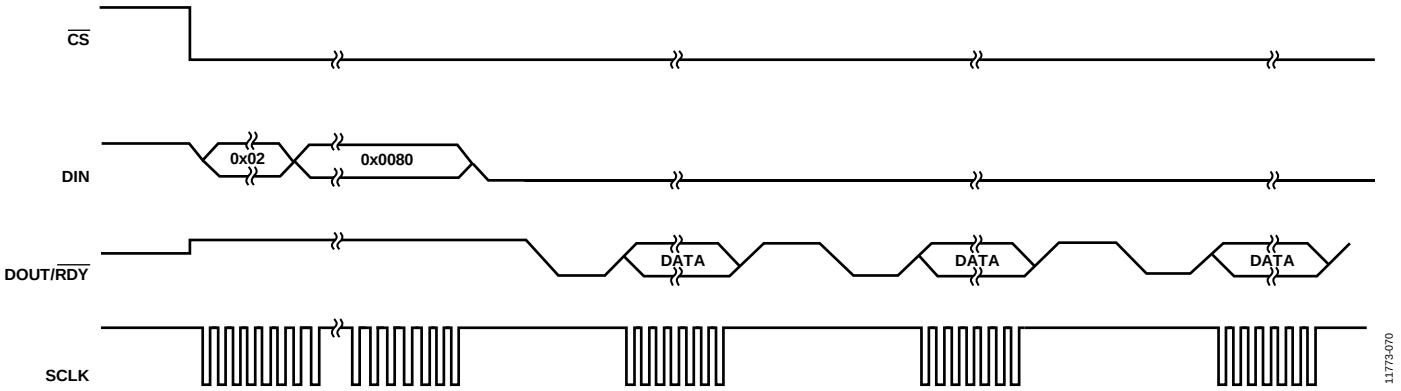


Figure 70. Continuous Read Mode

SINGLE CONVERSION MODE

In single conversion mode (see Figure 71), the AD7173-8 performs a single conversion and is placed in standby mode after the conversion is complete. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. After the data-word is read from the data register, DOUT/$\overline{RDY}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ is high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, DOUT/$\overline{RDY}$ goes high and remains high until a valid conversion is available and $\overline{CS}$ is low. As soon as the conversion is available, DOUT/$\overline{RDY}$ goes low. The ADC then selects the next channel and begins a conversion. The user must read the present conversion while the next conversion is being performed. As soon as the next conversion is complete, the data register is updated; therefore, the period in which to read the conversion is limited. After the ADC performs a single conversion on each of the selected channels, it returns to standby mode.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion, are output each time the data register is read. The four LSBs of the status register indicate the channel to which the conversion corresponds.

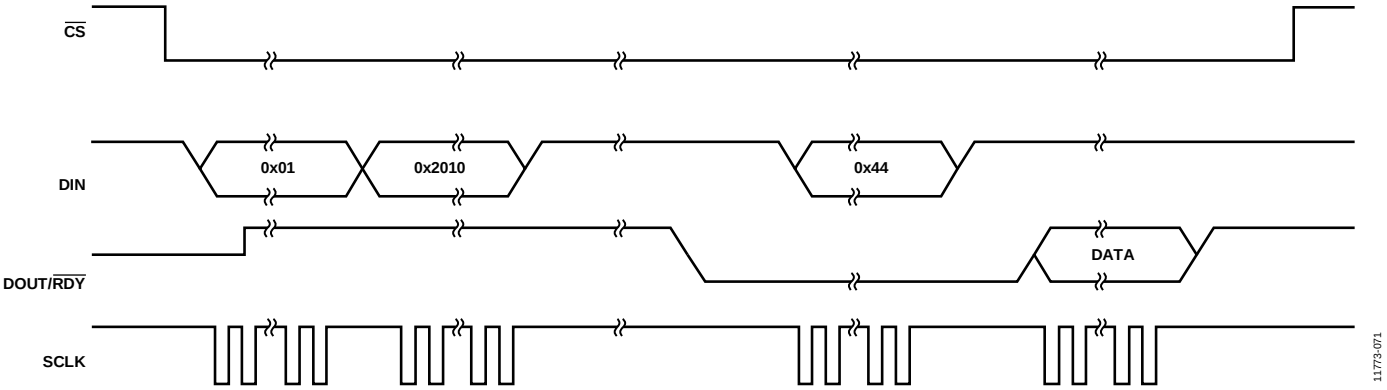


Figure 71. Single Conversion Mode

STANDBY AND POWER-DOWN MODES

In standby mode, most blocks are powered down. The LDOs remain active such that the registers maintain their contents. The internal reference remains active, if enabled; and the crystal oscillator remains active, if selected. To power down the reference in standby mode, set the REF_EN bit in the ADC mode register to 0. To power down the clock in standby mode, set the CLOCKSEL bits in the ADC mode register to 00 (internal oscillator).

In power-down mode, all blocks are powered down, including the LDOs. All registers lose their contents, and the GPIO outputs are placed in tristate. To prevent accidental entry to power-down mode, the ADC must first be placed into standby mode. Exiting power-down mode requires 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1, that is, a serial interface reset. A delay of 500 µs is recommended before issuing a subsequent serial interface command to allow the LDO to power up.

CALIBRATION MODES

The AD7173-8 provides three calibration modes that can be used to eliminate the offset and gain errors on a per setup basis:

- Internal zero-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

Only one channel can be active during calibration. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register.

The default value of the offset register is 0x800000, and the nominal value of the gain register is 0x555555. The calibration range of the ADC gain is from 0.4 × V_{REF} to 1.05 × V_{REF}. The following equations show the calculations that are used. In unipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left[\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right] \times \frac{Gain}{0x400000} \times 2$$

In bipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left[\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right] \times \frac{Gain}{0x400000} + 0x800000$$

To start a calibration, write the relevant value to the MODE bits in the ADC mode register. The DOUT/$\overline{RDY}$ pin and the RDY bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register are updated, the $\overline{RDY}$ bit in the status register is set, the DOUT/$\overline{RDY}$ pin returns low (if $\overline{CS}$ is low), and the AD7173-8 reverts to standby mode.

During an internal offset calibration, the selected positive analog input pin is disconnected, and both modulator inputs are connected internally to the selected negative analog input pin. For this reason, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference.

System calibrations, however, expect the system zero-scale (offset) and system full-scale (gain) voltages to be applied to the ADC pins before initiating the calibration modes. As a result, errors external to the ADC are removed.

From an operational point of view, treat a calibration like another ADC conversion. An offset calibration, if required, must always be performed before a full-scale calibration. Set the system software to monitor the $\overline{RDY}$ bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of a calibration via a polling sequence or an interrupt-driven routine. All calibrations require a time that is equal to the settling time of the selected filter and the output data rate to be completed.

An internal offset calibration, system zero-scale calibration, and system full-scale calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy and is accurate for all output data rates. A new calibration is required for a given channel if the reference source for that channel is changed.

The offset error is typically ±40 µV, and an offset calibration reduces the offset error to the order of the noise. The gain error is factory calibrated at ambient temperature. Following this calibration, the gain error is typically ±0.001%.

The AD7173-8 provides the user with access to the on-chip calibration registers, allowing the microprocessor to read the calibration coefficients of the device and to write its own calibration coefficients. A read or write of the offset and gain registers can be performed at any time except during an internal or self calibration.

DIGITAL INTERFACE

The programmable functions of the AD7173-8 are via the SPI serial interface. The serial interface of the AD7173-8 consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers, and DOUT/$\overline{RDY}$ is used to access data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or on DOUT/$\overline{RDY}$) occur with respect to the SCLK signal.

The DOUT/$\overline{RDY}$ pin also functions as a data-ready signal, with the line going low if $\overline{CS}$ is low when a new data-word is available in the data register. The pin is reset high when a read operation from the data register is complete. The DOUT/$\overline{RDY}$ pin also goes high before updating the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. Take care to avoid reading from the data register when DOUT/$\overline{RDY}$ is about to go low. The best method to ensure that no data read occurs is to always monitor the DOUT/$\overline{RDY}$ line; start reading the data register as soon as DOUT/$\overline{RDY}$ goes low; and ensure a sufficient SCLK rate, such that the read is completed before the next conversion result. $\overline{CS}$ is used to select a device. It can be used to decode the AD7173-8 in systems where several components are connected to the serial bus.

Figure 2 and Figure 3 show timing diagrams for interfacing to the AD7173-8 using $\overline{CS}$ to decode the part. Figure 2 shows the timing for a read operation from the AD7173-8, and Figure 3 shows the timing for a write operation to the AD7173-8. It is possible to read from the data register several times, even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, take care to ensure that the read operations are completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7173-8. The end of the conversion can also be monitored using the $\overline{RDY}$ bit in the status register.

The serial interface can be reset by writing 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1. A reset returns the interface to the state in which it expects a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, allow a period of 500 µs before addressing the serial interface.

CHECKSUM PROTECTION

The AD7173-8 has a checksum mode that can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERROR bit is set in the status register. However, to ensure that the register write was successful, it is important to read back the register and verify the checksum.

For CRC checksum calculations during a write operation, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

During read operations, the user can select between this polynomial and a similar XOR function. The XOR function requires less time to process on the host microcontroller than the polynomial-based checksum. The CRC_EN bits in the interface mode register enable and disable the checksum and allow the user to select between the polynomial check and the simple XOR check.

The checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8- to 24-bit data. For a read transaction, the checksum is calculated using the command word and the 8- to 32-bit data output. Figure 72 and Figure 73 show SPI write and read transactions, respectively.

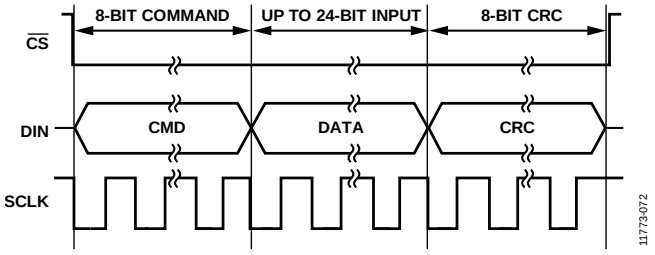


Figure 72. SPI Write Transaction with CRC

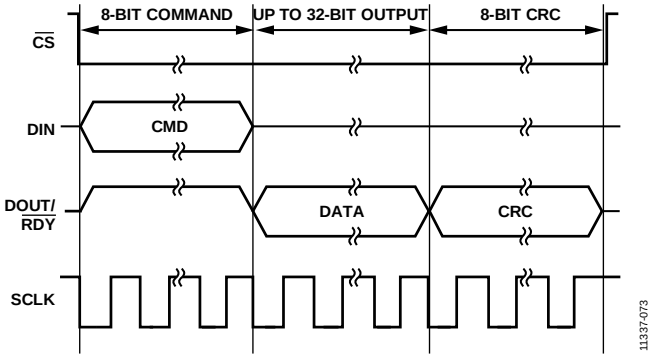


Figure 73. SPI Read Transaction with CRC

If checksum protection is enabled when continuous read mode is active, there is an implied read data command of 0x44 before every data transmission that must be accounted for when calculating the checksum value. This ensures a nonzero checksum value even if the ADC data equals 0x000000.

CRC CALCULATION

Polynomial

The checksum, which is eight bits wide, is generated using the following polynomial:

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

Example of a Polynomial CRC Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

```
Initial value          011001010100001100100001
                       011001010100001100100001000000000        left shifted eight bits
x^8 + x^2 + x + 1  =       100000111                            polynomial
   100100100000110010000100000000          XOR result
   100000111                               polynomial
      100011000110010000100000000          XOR result
      100000111                            polynomial
         111111100100001000000000          XOR result
         100000111                         polynomial value
          111110111000010000000 0          XOR result
          100000111                         polynomial value
           11111000000010000000 0          XOR result
           100000111                        polynomial value
            1110011100010000000 0          XOR result
            100000111                        polynomial value
             110010010010000000 0          XOR result
             100000111                       polynomial value
              10010101010000000 0          XOR result
              100000111                       polynomial value
                 1011011000000 0           XOR result
                 100000111                 polynomial value
                  101010110000 0           XOR result
                  100000111                polynomial value
                    1010001000 0           XOR result
                    100000111              polynomial value
                      10000110             checksum = 0x86.
```

XOR Calculation

The checksum, which is 8-bits wide, is generated by splitting the data into bytes and then performing an XOR of the bytes.

Example of an XOR Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

Using the previous example,

Divide into three bytes: 0x65, 0x43, and 0x21

01100101	0x65
01000011	0x43
00100110	XOR result
00100001	0x21
00000111	CRC

INTEGRATED FUNCTIONS

The AD7173-8 has a number of integrated functions that can be used to improve usefulness in a number of applications, as well as for diagnostic purposes in safety conscious applications.

GENERAL-PURPOSE I/O

The AD7173-8 has two general-purpose digital input/output pins (GPIO0, GPIO1) and two general-purpose digital output pins (GPO2, GPO3). As the naming convention suggests, the GPIO0 and GPIO1 pins can be configured as inputs or outputs, but GPO2 and GPO3 are outputs only. The GPIO and GPO pins are enabled using the following bits in the GPIOCON register: IP_EN0, IP_EN1 (or OP_EN0, OP_EN1) for GPIO0 and GPIO1, and OP_EN2_3 for GPO2 and GPO3.

When the GPIO0 or GPIO1 pin is enabled as an input, the logic level at the pin is contained in the GP_DATA0 or GP_DATA1 bit, respectively. When the GPIO0, GPIO1, GPO2, or GPO3 pin is enabled as an output, the GP_DATA0, GP_DATA1, GP_DATA2, or GP_DATA3 bit, respectively, determines the logic level output at the pin. The logic levels for these pins are referenced to AVDD1 and AVSS; therefore, outputs have an amplitude of either 5 V or 3.3 V depending on the AVDD1 − AVSS voltage.

The $\overline{\text{ERROR}}$ pin can also be used as a general-purpose output if the ERR_EN bits in the GPIOCON register are set to 11. In this configuration, the ERR_DAT bit in the GPIOCON register determines the logic level output at the $\overline{\text{ERROR}}$ pin. The logic level for the pin is referenced to IOVDD and DGND, and the $\overline{\text{ERROR}}$ pin has an active pull-up.

EXTERNAL MULTIPLEXER CONTROL

If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled using the AD7173-8 GPIO and GPO pins. When the MUX_IO bit is set in the GPIOCON register (Address 0x06, Bit 12), the timing of the GPIO pins is controlled by the ADC; therefore, the channel change is synchronized with the ADC, eliminating any need for external synchronization.

DELAY

It is possible to insert a programmable delay before the AD7173-8 begins taking samples when using the sinc5 + sinc1 filter. This allows for an external amplifier or multiplexer to settle and can also relax the specification requirements for the external amplifier or multiplexer. There are 8 programmable settings ranging from 0 µs to 8 ms which can be set using the DELAY bits in the ADC Mode Register (Address 0x01, Bits[10:8]).

If a delay greater than 0 µs is selected and $\overline{\text{HIDE\_DELAY}}$ in the Interface Mode Register (Address 0x02, Bit 10) is set to 1, then this delay is added to the conversion time for each sample regardless of selected output data rate.

If $\overline{\text{HIDE\_DELAY}}$ is set to 0 and the selected delay is less than half of the conversion time, then the delay can be absorbed by reducing the number of averages performed. This keeps the conversion time the same but may affect the noise performance, depending on the length of the delay compared to the conversion time. It is only possible to absorb the delay for output data rates less than 2.6 kSPS, with the exception of four rates which cannot absorb any delay: 381 SPS, 59.52 SPS, 49.68 SPS and 16.63 SPS.

16-BIT/24-BIT CONVERSIONS

By default, the AD7173-8 generates 24-bit conversions. However, the width of the conversions can be reduced to 16 bits. Setting Bit WL16 in the interface mode register to 1 rounds all data conversions to 16 bits. Clearing this bit sets the width of the data conversions to 24 bits.

SERIAL INTERFACE RESET (DOUT_RESET)

The serial interface is reset when each read operation is complete. The instant at which the serial interface is reset is programmable. By default, the serial interface is reset after a short period of time following the last SCLK rising edge, the SCLK edge on which the LSB is read by the processor. By setting the DOUT_RESET bit to 1 in the interface mode register, the instant at which the interface is reset is controlled by the $\overline{\text{CS}}$ rising edge. In this case, the DOUT/$\overline{\text{RDY}}$ pin continues to output the LSB of the register being read until $\overline{\text{CS}}$ is taken high. Only on the $\overline{\text{CS}}$ rising edge is the interface reset. This configuration is useful if the $\overline{\text{CS}}$ signal is used to frame all read operations. If $\overline{\text{CS}}$ is not used to frame all read operations, DOUT_RESET must be set to 0 so that the interface is reset following the last SCLK edge in the read operation.

SYNCHRONIZATION

Normal Synchronization

When the SYNC_EN bit in the GPIOCON register is set to 1, the $\overline{\text{SYNC}}$ pin functions as a synchronization pin. The $\overline{\text{SYNC}}$ input allows the user to reset the modulator and the digital filter without affecting any of the setup conditions on the part. This allows the user to start gathering samples of the analog input from a known point in time, that is, the rising edge of $\overline{\text{SYNC}}$. This pin must be low for at least one master clock cycle to ensure that synchronization occurs. If multiple channels are enabled, the sequencer is reset to the first enabled channel.

If multiple AD7173-8 devices are operated from a common master clock, they can be synchronized so that their data registers are updated simultaneously. This is normally done after each AD7173-8 has performed its own calibration or has calibration coefficients loaded into its calibration registers. A falling edge on the $\overline{\text{SYNC}}$ pin resets the digital filter and the analog modulator and places the AD7173-8 into a consistent known state. While the $\overline{\text{SYNC}}$ pin is low, the AD7173-8 is maintained in this state. On the $\overline{\text{SYNC}}$ rising edge, the modulator and filter are taken out of this reset state, and on the next master clock edge, the part starts to gather input samples again.

The part is taken out of reset on the master clock falling edge following the $\overline{\text{SYNC}}$ low-to-high transition. Therefore, when

multiple devices are being synchronized, take the SYNC pin high on the master clock rising edge to ensure that all devices begin sampling on the master clock falling edge. If the SYNC pin is not taken high in sufficient time, it is possible to have a difference of one master clock cycle between the devices; that is, the instant at which conversions are available differs from part to part by a maximum of one master clock cycle.

The SYNC pin can also be used as a start conversion command. In this mode, the rising edge of SYNC starts a conversion, and the falling edge of RDY indicates when the conversion is complete. The settling time of the filter must be allowed for each data register update.

Alternate Synchronization

Setting Bit ALT_SYNC in the interface mode register to 1 enables an alternate synchronization scheme. The SYNC_EN bit in the GPIOCON register must be set to 1 to enable this alternate scheme. In this mode, the SYNC pin operates as a start conversion command when several channels of the AD7173-8 are enabled. When SYNC is taken low, the ADC completes the conversion on the current channel, selects the next channel in the sequence, and then waits until SYNC is taken high to commence the conversion. The RDY pin goes low when the conversion is complete on
the current channel, and the data register is updated with the corresponding conversion. Therefore, the SYNC command does not interfere with the sampling on the currently selected channel but allows the user to control the instant at which the conversion begins on the next channel in the sequence.

This mode can be used only when several channels are enabled. It is not recommended to use this mode when a single channel is enabled.

ERROR FLAGS

The status register contains three error bits—ADC_ERROR, CRC_ERROR, and REG_ERROR—that flag errors with the ADC conversion, errors with the CRC check, and errors due to changes in the registers, respectively. In addition, the ERROR pin can indicate that an error has occurred.

ADC_ERROR

The ADC_ERROR bit in the status register flags any errors that occur during the conversion process. The flag is set when an overrange or underrange occurs at the output of the ADC. When an underrange or overrange occurs, the ADC also outputs all 0s or all 1s, respectively. This flag is reset only when the underrange or overrange is removed. It is not reset by a read of the data register.

CRC_ERROR

If the CRC value that accompanies a write operation does not correspond with the information sent, the CRC_ERROR flag is set. The flag is reset as soon as the status register is explicitly read.

REG_ERROR

This flag is used in conjunction with the REG_CHECK bit in the interface mode register. When the REG_CHECK bit is set, the AD7173-8 monitors the values in the on-chip registers. If a bit changes, the REG_ERROR bit is set. Therefore, for writes to the on-chip registers, ensure that REG_CHECK is set to 0. When the registers have been updated, the REF_CHK bit can be set to 1. The AD7173-8 calculates a checksum of the on-chip registers. If one of the register values has changed, the REG_ERROR bit is set. If an error is flagged, the REG_CHECK bit must be set to 0 to clear the REG_ERROR bit in the status register. The register check function does not monitor the data register, status register, or interface mode register.

ERROR Pin

The ERROR pin functions as an error input/output pin or a general-purpose output pin. The ERR_EN bits in the GPIOCON register determine the function of the pin.

When the ERR_EN bits are set to 10, the pin functions as an open-drain error output pin. The three error bits in the status register (ADC_ERROR, CRC_ERROR, and REG_ERROR) are OR'ed, inverted, and mapped to the ERROR pin. Therefore, the ERROR pin indicates that an error has occurred. To identify the error source, read the status register.

When ERR_EN bits are set to 01, the ERROR pin functions as an error input pin. The error pin of another component can be connected to the AD7173-8 ERROR pin so that the AD7173-8 indicates when an error occurs on either itself or the external component. The value on the ERROR pin is inverted and OR'ed with the errors from the ADC conversion, and the result is indicated via the ADC_ERROR bit in the status register. The value of the ERROR pin is reflected in the ERR_DAT bit in the status register.

The ERROR pin is disabled when the ERR_EN bits are set to 00. When the ERR_EN1 bits are set to 11, the ERROR pin operates as a general-purpose output.

DATA_STAT

The contents of the status register can be appended to each conversion on the AD7173-8. This is a useful function if several channels are enabled. Each time a conversion is output, the contents of the status register are appended. The four LSBs of the status register indicate to which channel the conversion corresponds. In addition, the user can determine if any errors are being flagged by the error bits.

IOSTRENGTH BIT

The serial interface can operate with a power supply as low as 2 V. At higher speeds (from 10 MHz to 15 MHz upward), the DOUT/RDY pin may not have sufficient drive strength if there is moderate parasitic capacitance on the board. The IOSTRENGTH bit in the interface mode register increases the drive strength of the DOUT/RDY pin. It is recommended that this bit be kept to its default value unless a high frequency SPI SCLK (that is, ~15 MHz upward) is being used.

GROUNDING AND LAYOUT

The analog inputs and reference inputs are differential and, therefore, most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the part removes common-mode noise on these inputs. The analog and digital supplies to the AD7173-8 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the master clock frequency.

The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7173-8 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7173-8 is high and the noise levels from the converter are so low, take care with regard to grounding and layout.

The printed circuit board (PCB) that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it results in the best shielding.

In any layout, the user must keep in mind the flow of currents in the system, ensuring that the paths for all return currents are as close as possible to the paths the currents took to reach their destinations.

Avoid running digital lines under the device because this couples noise onto the die and allows the analog ground plane to run under the AD7173-8 to prevent noise coupling. The power supply lines to the AD7173-8 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, whereas signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. The AD7173-8 has three power supply pins: AVDD1, AVDD2, and IOVDD. The AVDD1 and AVDD2 pins are referenced to AVSS, and the IOVDD pin is referenced to DGND. Decouple AVDD1 and AVDD2 with a 10 µF tantalum capacitor in parallel with a 0.1 µF capacitor to AVSS on each pin. Place the 0.1 µF capacitor as near as possible to the device on each supply, ideally right up against the device. Decouple IOVDD with a 10 µF tantalum capacitor, in parallel with a 0.1 µF capacitor to DGND. Decouple all analog inputs to AVSS. If an external reference is used, decouple the REF+ and REF− pins to AVSS.

The AD7173-8 also has two on-board LDO regulators—one that regulates the AVDD2 supply and one that regulates the IOVDD supply. For the REGCAPA pin, it is recommended that 1 µF and 0.1 µF capacitors to AVSS be used. Similarly, for the REGCAPD pin, it is recommended that 1 µF and 0.1 µF capacitors to DGND be used.

If using the AD7173-8 for split supply operation, a separate plane must be used for AVSS. As an example, the EVAL-AD7173-8SDZ customer evaluation board uses a 4-layer PCB, with the largest central section of Layer 3 used as the AVSS plane. Figure 74 shows the PCB layout of this layer.

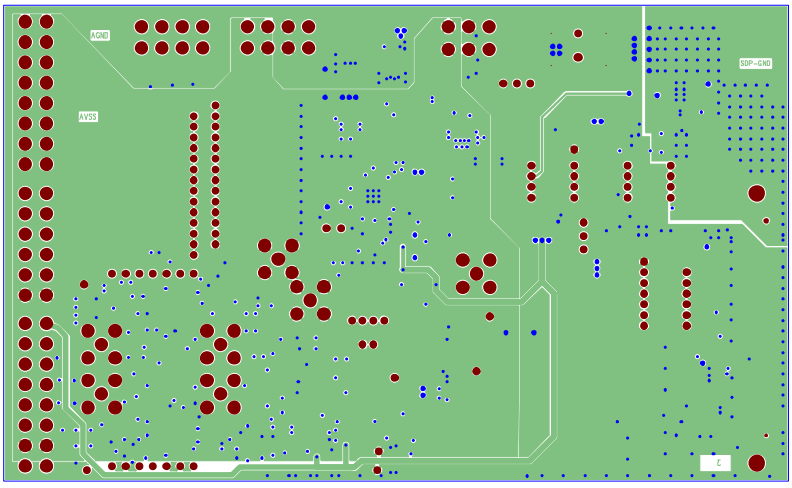


Figure 74. EVAL-AD7173-8SDZ, PCB Layer 3

REGISTER SUMMARY

Table 22. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{\text{WEN}}$	R/$\overline{\text{W}}$	RA						0x00	W
0x00	STATUS	[7:0]	$\overline{\text{RDY}}$	ADC_ERROR	CRC_ERROR	REG_ERROR	CHANNEL				0x80	R
0x01	ADCMODE	[15:8]	REF_EN	RESERVED	SING_CYC	RESERVED		DELAY			0x2000	RW
		[7:0]	RESERVED	MODE			CLOCKSEL		RESERVED			
0x02	IFMODE	[15:8]	RESERVED			ALT_SYNC	IOSTRENGTH	$\overline{\text{HIDE\_DELAY}}$	RESERVED	DOUT_RESET	0x0000	RW
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	RESERVED	CRC_EN		RESERVED	WL16		
0x03	REGCHECK	[23:16]	REGISTER_CHECK[23:16]								0x000000	R
		[15:8]	REGISTER_CHECK[15:8]									
		[7:0]	REGISTER_CHECK[7:0]									
0x04	DATA	[23:0]	DATA[23:0]								0x000000	R
0x06	GPIOCON	[15:8]	RESERVED	PDSW	OP_EN2_3	MUX_IO	SYNC_EN	ERR_EN		ERR_DAT	0x0800	RW
		[7:0]	GP_DATA3	GP_DATA2	IP_EN1	IP_EN0	OP_EN1	OP_EN0	GP_DATA1	GP_DATA0		
0x07	ID	[15:8]	ID[15:8]								0x30DX[1]	R
		[7:0]	ID[7:0]									
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL0			RESERVED		AINPOS0[4:3]		0x8001	RW
		[7:0]	AINPOS0[2:0]			AINNEG0						
0x11	CH1	[15:8]	CH_EN1	SETUP_SEL1			RESERVED		AINPOS1[4:3]		0x0001	RW
		[7:0]	AINPOS1[2:0]			AINNEG1						
0x12	CH2	[15:8]	CH_EN2	SETUP_SEL2			RESERVED		AINPOS2[4:3]		0x0001	RW
		[7:0]	AINPOS2[2:0]			AINNEG2						
0x13	CH3	[15:8]	CH_EN3	SETUP_SEL3			RESERVED		AINPOS3[4:3]		0x0001	RW
		[7:0]	AINPOS3[2:0]			AINNEG3						
0x14	CH4	[15:8]	CH_EN4	SETUP_SEL4			RESERVED		AINPOS4[4:3]		0x0001	RW
		[7:0]	AINPOS4[2:0]			AINNEG4						
0x15	CH5	[15:8]	CH_EN5	SETUP_SEL5			RESERVED		AINPOS5[4:3]		0x0001	RW
		[7:0]	AINPOS5[2:0]			AINNEG5						
0x16	CH6	[15:8]	CH_EN6	SETUP_SEL6			RESERVED		AINPOS6[4:3]		0x0001	RW
		[7:0]	AINPOS6[2:0]			AINNEG6						
0x17	CH7	[15:8]	CH_EN7	SETUP_SEL7			RESERVED		AINPOS7[4:3]		0x0001	RW
		[7:0]	AINPOS7[2:0]			AINNEG7						
0x18	CH8	[15:8]	CH_EN8	SETUP_SEL8			RESERVED		AINPOS8[4:3]		0x0001	RW
		[7:0]	AINPOS8[2:0]			AINNEG8						
0x19	CH9	[15:8]	CH_EN9	SETUP_SEL9			RESERVED		AINPOS9[4:3]		0x0001	RW
		[7:0]	AINPOS9[2:0]			AINNEG9						
0x1A	CH10	[15:8]	CH_EN10	SETUP_SEL10			RESERVED		AINPOS10[4:3]		0x0001	RW
		[7:0]	AINPOS10[2:0]			AINNEG10						
0x1B	CH11	[15:8]	CH_EN11	SETUP_SEL11			RESERVED		AINPOS11[4:3]		0x0001	RW
		[7:0]	AINPOS11[2:0]			AINNEG11						
0x1C	CH12	[15:8]	CH_EN12	SETUP_SEL12			RESERVED		AINPOS12[4:3]		0x0001	RW
		[7:0]	AINPOS12[2:0]			AINNEG12						
0x1D	CH13	[15:8]	CH_EN13	SETUP_SEL13			RESERVED		AINPOS13[4:3]		0x0001	RW
		[7:0]	AINPOS13[2:0]			AINNEG13						
0x1E	CH14	[15:8]	CH_EN14	SETUP_SEL14			RESERVED		AINPOS14[4:3]		0x0001	RW
		[7:0]	AINPOS14[2:0]			AINNEG14						
0x1F	CH15	[15:8]	CH_EN15	SETUP_SEL15			RESERVED		AINPOS15[4:3]		0x0001	RW
		[7:0]	AINPOS15[2:0]			AINNEG15						
0x20	SETUPCON0	[15:8]	RESERVED			BI_ UNIPOLAR0	REF_BUF 0[1:0]		AIN_BUF 0[1:0]		0x1000	RW
		[7:0]	BURNOUT_ EN0	BUFCHOPMAX0	REF_SEL0		RESERVED					
0x21	SETUPCON1	[15:8]	RESERVED			BI_UNIPOLAR1	REF_BUF 1[1:0]		AIN_BUF 1[1:0]		0x1000	RW
		[7:0]	BURNOUT_ EN1	BUFCHOPMAX1	REFSEL1		RESERVED					
0x22	SETUPCON2	[15:8]	RESERVED			BI_UNIPOLAR2	REF_BUF 2[1:0]		AIN_BUF 2[1:0]		0x1000	RW
		[7:0]	BURNOUT_ EN2	BUFCHOPMAX2	REFSEL2		RESERVED					

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x23	SETUPCON3	[15:8]	RESERVED			BI_UNIPOLAR3	REF_BUF 3[1:0]		AIN_BUF 3[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN3	BUFCHOPMAX 3	REFSEL3		RESERVED					
0x24	SETUPCON4	[15:8]	RESERVED			BI_UNIPOLAR4	REF_BUF 4[1:0]		AIN_BUF 4[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN4	BUFCHOPMAX 4	REFSEL4		RESERVED					
0x25	SETUPCON5	[15:8]	RESERVED			BI_UNIPOLAR5	REF_BUF 5[1:0]		AIN_BUF 5[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN5	BUFCHOPMAX 5	REFSEL5		RESERVED					
0x26	SETUPCON6	[15:8]	RESERVED			BI_UNIPOLAR6	REF_BUF 6[1:0]		AIN_BUF 6[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN6	BUFCHOPMAX 6	REFSEL6		RESERVED					
0x27	SETUPCON7	[15:8]	RESERVED			BI_UNIPOLAR7	REF_BUF 7[1:0]		AIN_BUF 7[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN7	BUFCHOPMAX 7	REFSEL7		RESERVED					
0x28	FILTCON0	[15:8]	SINC3_MAP0	RESERVED			ENHFILTEN0	ENHFILT0			0x0000	RW
		[7:0]	RESERVED	ORDER0		ODR0						
0x29	FILTCON1	[15:8]	SINC3_MAP1	RESERVED			ENHFILTEN1	ENHFILT1			0x0000	RW
		[7:0]	RESERVED	ORDER1		ODR1						
0x2A	FILTCON2	[15:8]	SINC3_MAP2	RESERVED			ENHFILTEN2	ENHFILT2			0x0000	RW
		[7:0]	RESERVED	ORDER2		ODR2						
0x2B	FILTCON3	[15:8]	SINC3_MAP3	RESERVED			ENHFILTEN3	ENHFILT3			0x0000	RW
		[7:0]	RESERVED	ORDER3		ODR3						
0x2C	FILTCON4	[15:8]	SINC3_MAP4	RESERVED			ENHFILTEN4	ENHFILT4			0x0000	RW
		[7:0]	RESERVED	ORDER4		ODR4						
0x2D	FILTCON5	[15:8]	SINC3_MAP5	RESERVED			ENHFILTEN5	ENHFILT5			0x0000	RW
		[7:0]	RESERVED	ORDER5		ODR5						
0x2E	FILTCON6	[15:8]	SINC3_MAP6	RESERVED			ENHFILTEN6	ENHFILT6			0x0000	RW
		[7:0]	RESERVED	ORDER6		ODR6						
0x2F	FILTCON7	[15:8]	SINC3_MAP7	RESERVED			ENHFILTEN7	ENHFILT7			0x0000	RW
		[7:0]	RESERVED	ORDER7		ODR7						
0x30	OFFSET0	[23:0]	OFFSET0[23:0]								0x800000	RW
0x31	OFFSET1	[23:0]	OFFSET1[23:0]								0x800000	RW
0x32	OFFSET2	[23:0]	OFFSET2[23:0]								0x800000	RW
0x33	OFFSET3	[23:0]	OFFSET3[23:0]								0x800000	RW
0x34	OFFSET4	[23:0]	OFFSET4[23:0]								0x800000	RW
0x35	OFFSET5	[23:0]	OFFSET5[23:0]								0x800000	RW
0x36	OFFSET6	[23:0]	OFFSET6[23:0]								0x800000	RW
0x37	OFFSET7	[23:0]	OFFSET7[23:0]								0x800000	RW
0x38	GAIN0	[23:0]	GAIN0[23:0]								0x5XXXX0[2]	RW
0x39	GAIN1	[23:0]	GAIN1[23:0]								0x5XXXX0[2]	RW
0x3A	GAIN2	[23:0]	GAIN2[23:0]								0x5XXXX0[2]	RW
0x3B	GAIN3	[23:0]	GAIN3[23:0]								0x5XXXX0[2]	RW
0x3C	GAIN4	[23:0]	GAIN4[23:0]								0x5XXXX0[2]	RW
0x3D	GAIN5	[23:0]	GAIN5[23:0]								0x5XXXX0[2]	RW
0x3E	GAIN6	[23:0]	GAIN6[23:0]								0x5XXXX0[2]	RW
0x3F	GAIN7	[23:0]	GAIN7[23:0]								0x5XXXX0[2]	RW

[1] X = don't care. The value of X is specific to the ADC.
[2] The value of X varies, depending on the IC that is used.

REGISTER DETAILS

COMMUNICATIONS REGISTER

Address: 0x00, Reset: 0x00, Name: COMMS

Table 23. Bit Descriptions for COMMS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{WEN}$		This bit must be low to begin communications with the ADC.	0x0	W
6	R/$\overline{W}$		This bit determines if the command is a read or write operation.	0x0	W
		0	Write command		
		1	Read command		
[5:0]	RA		The register address bits determine which register is to be read from or written to as part of the current communication.	0x00	W
		000000	Status register		
		000001	ADC mode register		
		000010	Interface mode register		
		000011	Register checksum register		
		000100	Data register		
		000110	GPIO configuration register		
		000111	ID register		
		010000	Channel 0 register		
		010001	Channel 1 register		
		010010	Channel 2 register		
		010011	Channel 3 register		
		010100	Channel 4 register		
		010101	Channel 5 register		
		010110	Channel 6 register		
		010111	Channel 7 register		
		011000	Channel 8 register		
		011001	Channel 9 register		
		011010	Channel 10 register		
		011011	Channel 11 register		
		011100	Channel 12 register		
		011101	Channel 13 register		
		011110	Channel 14 register		
		011111	Channel 15 register		
		100000	Setup Configuration 0 register		
		100001	Setup Configuration 1 register		
		100010	Setup Configuration 2 register		
		100011	Setup Configuration 3 register		
		100100	Setup Configuration 4 register		
		100101	Setup Configuration 5 register		
		100110	Setup Configuration 6 register		
		100111	Setup Configuration 7 register		
		101000	Filter Configuration 0 register		
		101001	Filter Configuration 1 register		
		101010	Filter Configuration 2 register		
		101011	Filter Configuration 3 register		
		101100	Filter Configuration 4 register		
		101101	Filter Configuration 5 register		
		101110	Filter Configuration 6 register		
		101111	Filter Configuration 7 register		
		110000	Offset 0 register		
		110001	Offset 1 register		

Bits	Bit Name	Settings	Description	Reset	Access
		110010	Offset 2 register		
		110011	Offset 3 register		
		110100	Offset 4 register		
		110101	Offset 5 register		
		110110	Offset 6 register		
		110111	Offset 7 register		
		111000	Gain 0 register		
		111001	Gain 1 register		
		111010	Gain 2 register		
		111011	Gain 3 register		
		111100	Gain 4 register		
		111101	Gain 5 register		
		111110	Gain 6 register		
		111111	Gain 7 register		

STATUS REGISTER

Address: 0x00, Reset: 0x80, Name: STATUS

The status register is an 8-bit register that contains ADC and serial interface status information. It can optionally be appended to the data register by setting the DATA_STAT bit in the interface mode register (Bit 6, Register 0x02).

Table 24. Bit Descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{\text{RDY}}$		The status of $\overline{\text{RDY}}$ is output to the DOUT/$\overline{\text{RDY}}$ pin whenever $\overline{\text{CS}}$ is low and a register is not being read. This bit goes low when the ADC has written a new result to the data register. In ADC calibration modes, this bit goes low when the ADC has written the calibration result. $\overline{\text{RDY}}$ is brought high automatically by a read of the data register.	0x1	R
		0	New data result available		
		1	Awaiting new data result		
6	ADC_ERROR		This bit, by default, indicates if an ADC overrange or underrange has occurred. The ADC result is clamped to ± full scale if an overrange or underrange occurs. This bit is updated when the ADC result is written and is cleared by removing the overrange or underrange condition on the analog inputs.	0x0	R
		0	No error		
		1	Error		
5	CRC_ERROR		This bit indicates if a CRC error has occurred during a register write. For register reads, the host microcontroller determines if a CRC error has occurred. This bit is cleared by a read of this register.	0x0	R
		0	No error		
		1	CRC error		
4	REG_ERROR		This bit indicates if the content of one of the internal registers has changed from the value calculated when the register integrity check was activated. The check is activated by setting the REG_CHECK bit in the interface mode register. This bit is cleared by clearing the REG_CHECK bit.	0x0	R
		0	No error		
		1	Error		
[3:0]	CHANNEL		These bits indicate which channel was active for the ADC conversion whose result is currently in the data register. This may be different from the channel currently being converted. The bits are a direct mapping from the Channel x registers; therefore, Channel 0 results in 0x0 and Channel 15 results in 0x1F.	0x0	R
		0000	Channel 0		
		0001	Channel 1		
		0010	Channel 2		
		0011	Channel 3		
		0100	Channel 4		
		0101	Channel 5		
		0110	Channel 6		
		0111	Channel 7		
		1000	Channel 8		
		1001	Channel 9		
		1010	Channel 10		
		1011	Channel 11		
		1100	Channel 12		
		1101	Channel 13		
		1110	Channel 14		
		1111	Channel 15		

ADC MODE REGISTER

Address: 0x01, Reset: 0x2000, Name: ADCMODE

The ADC mode register controls the operating mode of the ADC and the master clock selection. A write to the ADC mode register resets the filter and the $\overline{RDY}$ bits and starts a new conversion or calibration.

Table 25. Bit Descriptions for ADCMODE

Bits	Bit Name	Settings	Description	Reset	Access
15	REF_EN		Enables internal reference and outputs a buffered 2.5 V to the REFOUT pin.	0x0	RW
		0	Disabled		
		1	Enabled		
14	RESERVED		This bit is reserved. Set to 0.	0x0	R
13	SING_CYC		This bit can be used when only a single channel is active to set the ADC to output only at the settled filter data rate.	0x1	RW
		0	Disabled		
		1	Enabled		
[12:11]	RESERVED		These bits are reserved. Set to 0.	0x0	R
[10:8]	DELAY		These bits allow a programmable delay to be added after a channel switch to allow settling of external circuitry before the ADC starts processing its input.	0x0	RW
		000	0 µs		
		001	32 µs		
		010	128 µs		
		011	320 µs		
		100	800 µs		
		101	1.6 ms		
		110	4 ms		
		111	8 ms		
7	RESERVED		This bit is reserved. Set to 0.	0x0	R
[6:4]	MODE		These bits control the operating mode of the ADC. Details can be found in the Operating Modes section.	0x0	RW
		000	Continuous conversion mode		
		001	Single conversion mode		
		010	Standby mode		
		011	Power-down mode		
		100	Internal offset calibration		
		110	System offset calibration		
		111	System gain calibration		
[3:2]	CLOCKSEL		This bit is used to select the ADC clock source. Selecting the internal oscillator also enables the internal oscillator.	0x0	RW
		00	Internal oscillator		
		01	Internal oscillator output on XTAL2/CLKIO pin		
		10	External clock input on XTAL2/CLKIO pin		
		11	External crystal on XTAL1 and XTAL2/CLKIO pins		
[1:0]	RESERVED		These bits are reserved. Set to 0.	0x0	R

INTERFACE MODE REGISTER

Address: 0x02, Reset: 0x0000, Name: IFMODE

The interface mode register configures various serial interface options.

Table 26. Bit Descriptions for IFMODE

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved. Set to 0.	0x0	R
12	ALT_SYNC		This bit enables a different behavior of the $\overline{\text{SYNC}}$ pin to allow the use of $\overline{\text{SYNC}}$ as a control for conversions when cycling channels. (For details, see the description of the SYNC_EN bit in the GPIO Configuration Register.)	0x0	RW
		0	Disabled		
		1	Enabled		
11	IOSTRENGTH		This bit controls the drive strength of the DOUT (DOUT/$\overline{\text{RDY}}$) pin and the XTAL2/CLKIO pin. Set this bit to 1 when reading from the serial interface at high speed with low IOVDD supply and moderate capacitance.	0x0	RW
		0	Disabled (default)		
		1	Enabled		
10	$\overline{\text{HIDE\_DELAY}}$		If a programmable delay is set using the DELAY bits in the ADC mode register, then this bit allows for the delay to be hidden by absorbing the delay into the conversion time for selected data rates. See the Delay section for more details.	0x0	RW
		0	Enabled		
		1	Disabled		
9	RESERVED		These bits are reserved. Set to 0.	0x0	R
8	DOUT_RESET		This bit prevents the DOUT/$\overline{\text{RDY}}$ pin from switching from outputting DOUT to outputting $\overline{\text{RDY}}$ soon after the last rising edge of SCLK during a read operation. Instead, the DOUT/$\overline{\text{RDY}}$ pin continues to output the LSB of the data until $\overline{\text{CS}}$ goes high, providing longer hold times for the SPI master to sample the LSB of the data. When this bit is set, $\overline{\text{CS}}$ must not be tied low.	0x0	RW
		0	Disabled		
		1	Enabled		
7	CONTREAD		This bit enables continuous read of the ADC data register. To use continuous read, configure the ADC in continuous conversion mode. For more details, see the Operating Modes section.	0x0	RW
		0	Disabled		
		1	Enabled		
6	DATA_STAT		This bit enables the status register to be appended to the data register when read so that channel and status information is transmitted with the data. This is the only way to ensure that the channel bits read from the status register correspond to the data in the data register.	0x0	RW
		0	Disabled		
		1	Enabled		
5	REG_CHECK		This bit enables a register integrity checker that can be used to monitor any change in the value of the user registers. To use this feature, configure all other registers as desired, with this bit cleared. Then write to this register to set the REG_CHECK bit to 1. If the contents of any of the registers change, the REG_ERROR bit is set in the status register. To clear the error, set the REG_CHECK bit to 0. Neither the interface mode register nor the ADC data or status register is included in the registers that are checked. If a register must have a new value written, clear this bit first; otherwise, an error is flagged when the new register contents are written.	0x0	RW
		0	Disabled		
		1	Enabled		
4	RESERVED		This bit is reserved. Set to 0.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	CRC_EN		Enables CRC protection of register reads/writes. CRC increases the number of bytes in a serial interface transfer by one. See the CRC Calculation section for more details.	0x00	RW
		00	Disabled.		
		01	XOR checksum enabled for register read transactions. Register writes still use CRC with these bits set.		
		10	CRC checksum enabled for read and write transactions.		
1	RESERVED		This bit is reserved. Set to 0.	0x0	R
0	WL16		Changes the ADC data register to 16 bits. The ADC is not reset by a write to the interface mode register; therefore, the ADC result is not rounded to the correct word length immediately after writing to these bits. The first new ADC result is correct.	0x0	RW
		0	24-bit data		
		1	16-bit data		

REGISTER CHECK

Address: 0x03, Reset: 0x000000, Name: REGCHECK

The register check register is a 24-bit checksum calculated by XOR'ing the contents of the user registers and some nonaccessible registers. The REG_CHECK bit in the interface mode register must be set for this to operate; otherwise, the register reads 0.

Table 27. Bit Descriptions for REGCHECK

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	REGISTER_CHECK		This register contains the 24-bit checksum of user registers when the REG_CHECK bit is set in the interface mode register.	0x000000	R

DATA REGISTER

Address: 0x04, Reset: 0x000000, Name: DATA

The data register contains the ADC conversion result. The encoding is offset binary; however, it can be changed to unipolar by the BI_UNIPOLAR bit in the setup configuration register. Reading the data register brings the $\overline{\text{RDY}}$ bit and pin high if they are low. The ADC result can be read multiple times; however, because $\overline{\text{RDY}}$ has been brought high, it is not possible to know if another ADC result is imminent. The ADC does not write a new result into the data register if the register is currently being read.

Table 28. Bit Descriptions for DATA

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	DATA		This register contains the ADC conversion result. If the DATA_STAT bit is set in the interface mode register, the status register is appended to this register when read, making this a 32-bit register. If WL16 is set in the interface mode register, this register is set to a length of 16 bits.	0x000000	R

GPIO CONFIGURATION REGISTER

Address: 0x06, Reset: 0x0800, Name: GPIOCON

The GPIO configuration register controls the general-purpose I/O pins of the ADC.

Table 29. Bit Descriptions for GPIOCON

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		This bit is reserved. Set to 0.	0x0	R
14	PDSW		This bit enables/disables the power-down switch function. Setting the bit allows the pin to sink current. This function can be used for bridge sensor applications where the switch controls the power-up/power-down of the bridge.	0x0	RW
13	OP_EN2_3		This bit enables the GPO2 and GPO3 pins. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
12	MUX_IO		This bit allows the ADC to control an external multiplexer, using GPIO0/GPIO1/GPO2/GPO3 in sync with the internal channel sequencing. The analog input pins used for a channel can still be selected on a per channel basis. Therefore, it is possible to have a 16-channel multiplexer in front of each analog input pair (AIN0/AIN1 to AIN14/AIN15), giving a total of 128 differential channels. However, only 16 channels at a time can be automatically sequenced. Following the sequence of 16 channels, the user changes the analog input to the next pair of input channels, and it sequences through the next 16 channels. There is a delay function that allows extra time for the analog input to settle, in conjunction with any switching an external multiplexer (see the delay bits in the ADC Mode Register).	0x0	RW
11	SYNC_EN		This bit enables the $\overline{\text{SYNC}}$ pin as a sync input. When set low, the $\overline{\text{SYNC}}$ pin holds the ADC and filter in reset until $\overline{\text{SYNC}}$ goes high. An alternative operation of the $\overline{\text{SYNC}}$ pin is available when the ALT_SYNC bit in the interface mode register is set. This mode works only when multiple channels are enabled. In such cases, a low on the $\overline{\text{SYNC}}$ pin does not immediately reset the filter/modulator. Instead, if the $\overline{\text{SYNC}}$ pin is low when the channel is due to be switched, the modulator and filter are prevented from starting a new conversion. Bringing $\overline{\text{SYNC}}$ high begins the next conversion. This alternative sync mode allows $\overline{\text{SYNC}}$ to be used while cycling through channels.	0x1	RW
		0	Disabled		
		1	Enabled		
[10:9]	ERR_EN		These bits enable the $\overline{\text{ERROR}}$ pin as an error input/output.	0x0	RW
		00	Disabled		
		01	$\overline{\text{ERROR}}$ is an error input. The (inverted) readback state is OR'ed with other error sources and is available in the ADC_ERROR bit in the status register. The $\overline{\text{ERROR}}$ pin state can also be read from the ERR_DAT bit in this register.		
		10	$\overline{\text{ERROR}}$ is an open-drain error output. The status register error bits are OR'ed, inverted, and mapped to the $\overline{\text{ERROR}}$ pin. $\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.		
		11	$\overline{\text{ERROR}}$ is a general-purpose output. The status of the pin is controlled by the ERR_DAT bit in this register. This is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the general-purpose I/O pins. It has an active pull-up in this case.		
8	ERR_DAT		This bit determines the logic level at the $\overline{\text{ERROR}}$ pin if the pin is enabled as a general-purpose output. It reflects the readback status of the pin if the pin is enabled as an input.	0x0	RW
7	GP_DATA3		This bit is the write data for GPO3.	0x0	W
6	GP_DATA2		This bit is the write data for GPO2.	0x0	W
5	IP_EN1		This bit turns GPIO1 into an input. Input should equal AVDD1 or AVSS.	0x0	RW
		0	Disabled		
		1	Enabled		

Bits	Bit Name	Settings	Description	Reset	Access
4	IP_EN0		This bit turns GPIO0 into an input. Input should equal AVDD1 or AVSS.	0x0	RW
		0	Disabled		
		1	Enabled		
3	OP_EN1		This bit turns GPIO1 into an output. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
		0	Disabled		
		1	Enabled		
2	OP_EN0		This bit turns GPIO0 into an output. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
		0	Disabled		
		1	Enabled		
1	GP_DATA1		This bit is the readback or write data for GPIO1.	0x0	RW
0	GP_DATA0		This bit is the readback or write data for GPIO0.	0x0	RW

ID REGISTER

Address: 0x07, Reset: 0x30DX, Name: ID

The ID register returns a 16-bit ID. For the AD7173-8, this is 0x30DX.

Table 30. Bit Descriptions for ID

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	ID		The ID register returns a 16-bit ID code that is specific to the ADC.	0x30DX[1]	R
		0x30DX	AD7173-8		

[1] X = don't care.

CHANNEL REGISTER 0

Address: 0x10, Reset: 0x8001, Name: CH0

The channel registers are 16-bit registers that are used to select which channels are currently active, which inputs are selected for each channel, and which setup should be used to configure the ADC for that channel.

Table 31. Bit Descriptions for CH0

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_EN0		This bit enables Channel 0. If more than one channel is enabled, the ADC automatically sequences between them.	0x1	RW
		0	Disabled		
		1	Enabled (default)		
[14:12]	SETUP_SEL0		These bits identify which of the eight setups are used to configure the ADC for this channel. A setup comprises a set of four registers: the setup configuration register, the filter configuration register, the offset register, and the gain register. All channels can use the same setup, in which case the same 3-bit value is written to these bits on all active channels; alternatively, up to eight channels can be configured differently.	0x0	RW
		000	Setup 0		
		001	Setup 1		
		010	Setup 2		
		011	Setup 3		
		100	Setup 4		
		101	Setup 5		
		110	Setup 6		
		111	Setup 7		
[11:10]	RESERVED		These bits are reserved. Set to 0.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
[9:5]	AINPOS0		These bits select which of the analog inputs is connected to the positive input of the ADC for this channel. TEMP SENSOR ± is an internal temperature sensor.	0x0	RW
		00000	AIN0 (default)		
		00001	AIN1		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		00101	AIN5		
		00110	AIN6		
		00111	AIN7		
		01000	AIN8		
		01001	AIN9		
		01010	AIN10		
		01011	AIN11		
		01100	AIN12		
		01101	AIN13		
		01110	AIN14		
		01111	AIN15		
		10000	AIN16		
		10001	TEMP SENSOR +		
		10010	TEMP SENSOR −		
		10101	REF+		
		10110	REF−		
[4:0]	AINNEG0		These bits select which of the analog inputs is connected to the negative input of the ADC for this channel.	0x1	RW
		00000	AIN0		
		00001	AIN1(default)		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		00101	AIN5		
		00110	AIN6		
		00111	AIN7		
		01000	AIN8		
		01001	AIN9		
		01010	AIN10		
		01011	AIN11		
		01100	AIN12		
		01101	AIN13		
		01110	AIN14		
		01111	AIN15		
		10000	AIN16		
		10001	TEMP SENSOR +		
		10010	TEMP SENSOR −		
		10101	REF+		
		10110	REF−		

CHANNEL REGISTER 1 TO CHANNEL REGISTER 15

Address Range: 0x11 to 0x1F, Reset: 0x0001, Name: CH1 to CH15

Subsequent channel registers, CH1 to CH15, use the same structure as the CH0 register. They are disabled by default (MSB = 0). Each channel created can be referred to one of eight setups. The sequencer progresses through each of the enabled channels in order.

Table 32 shows the summary of these registers, their addresses, and their reset values.

Table 32. Summary of CH1 to CH15

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x11	CH1	[15:8]	CH_EN1	SETUP_SEL1			RESERVED		AINPOS1[4:3]		0x0001	RW
		[7:0]	AINPOS1[2:0]			AINNEG1						
0x12	CH2	[15:8]	CH_EN2	SETUP_SEL2			RESERVED		AINPOS2[4:3]		0x0001	RW
		[7:0]	AINPOS2[2:0]			AINNEG2						
0x13	CH3	[15:8]	CH_EN3	SETUP_SEL3			RESERVED		AINPOS3[4:3]		0x0001	RW
		[7:0]	AINPOS3[2:0]			AINNEG3						
0x14	CH4	[15:8]	CH_EN4	SETUP_SEL4			RESERVED		AINPOS4[4:3]		0x0001	RW
		[7:0]	AINPOS4[2:0]			AINNEG4						
0x15	CH5	[15:8]	CH_EN5	SETUP_SEL5			RESERVED		AINPOS5[4:3]		0x0001	RW
		[7:0]	AINPOS5[2:0]			AINNEG5						
0x16	CH6	[15:8]	CH_EN6	SETUP_SEL6			RESERVED		AINPOS6[4:3]		0x0001	RW
		[7:0]	AINPOS6[2:0]			AINNEG6						
0x17	CH7	[15:8]	CH_EN7	SETUP_SEL7			RESERVED		AINPOS7[4:3]		0x0001	RW
		[7:0]	AINPOS7[2:0]			AINNEG7						
0x18	CH8	[15:8]	CH_EN8	SETUP_SEL8			RESERVED		AINPOS8[4:3]		0x0001	RW
		[7:0]	AINPOS8[2:0]			AINNEG8						
0x19	CH9	[15:8]	CH_EN9	SETUP_SEL9			RESERVED		AINPOS9[4:3]		0x0001	RW
		[7:0]	AINPOS9[2:0]			AINNEG9						
0x1A	CH10	[15:8]	CH_EN10	SETUP_SEL10			RESERVED		AINPOS10[4:3]		0x0001	RW
		[7:0]	AINPOS10[2:0]			AINNEG10						
0x1B	CH11	[15:8]	CH_EN11	SETUP_SEL11			RESERVED		AINPOS11[4:3]		0x0001	RW
		[7:0]	AINPOS11[2:0]			AINNEG11						
0x1C	CH12	[15:8]	CH_EN12	SETUP_SEL12			RESERVED		AINPOS12[4:3]		0x0001	RW
		[7:0]	AINPOS12[2:0]			AINNEG12						
0x1D	CH13	[15:8]	CH_EN13	SETUP_SEL13			RESERVED		AINPOS13[4:3]		0x0001	RW
		[7:0]	AINPOS13[2:0]			AINNEG13						
0x1E	CH14	[15:8]	CH_EN14	SETUP_SEL14			RESERVED		AINPOS14[4:3]		0x0001	RW
		[7:0]	AINPOS14[2:0]			AINNEG14						
0x1F	CH15	[15:8]	CH_EN15	SETUP_SEL15			RESERVED		AINPOS15[4:3]		0x0001	RW
		[7:0]	AINPOS15[2:0]			AINNEG15						

SETUP CONFIGURATION REGISTER 0

Address: 0x20, Reset: 0x1000, Name: SETUPCON0

The setup configuration registers are 16-bit registers that configure the reference selection, input buffers, burnout currents, and output coding of the ADC.

Table 33. Bit Descriptions for SETUPCON0

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved. Set to 0.	0x0	R
12	BI_UNIPOLAR0		This bit sets the output coding of the ADC for Setup 0.	0x1	RW
		0	Unipolar coded output		
		1	Offset binary coded output		
[11:10]	REF_BUF_0[1:0]		Reference input buffer enable. These bits turn on the buffers of the positive and negative reference inputs. This offers a high impedance input for an external reference source and isolates it from the switch capacitor reference sampling input of the ADC. Use both reference buffers together.	0x0	RW
		00	Reference input buffers disabled		
		11	Reference input buffers enabled		
[9:8]	AIN_BUF_0[1:0]		Analog input buffer enable. These bits turn on the buffers of the positive and negative analog inputs. This offers a high impedance input to the device and isolates the sensor/signal for measurement from the switch capacitor sampling input of the ADC. Use both analog input buffers together.	0x0	RW
		00	Analog input buffers disabled		
		11	Analog input buffers enabled		
7	BURNOUT_EN0		This bit enables a 10 µA current source on the positive analog input selected and a 10 µA current sink on the negative analog input selected. The burnout currents are useful in diagnosis of an open wire, whereby the ADC result goes to full scale. Enabling the BURNOUT currents during measurement results in an offset voltage on the ADC reading of approximately 1 µV. This means the strategy for diagnosing an open wire operates best by turning on the BURNOUT currents at intervals, before or after precision measurements.	0x0	RW
6	BUFCHOPMAX0		This bit enables the maximum buffer chop frequency, increasing AIN input current and reducing buffer noise.	0x0	RW
[5:4]	REF_SEL0		These bits allow selection of the reference source for ADC conversion on Setup 0.	0x0	RW
		00	External reference supplied to REF+ and REF− pins		
		01	External Reference 2 supplied to AIN1/REF2+ and AIN0/REF2− pins		
		10	Internal 2.5 V reference; this reference must also be enabled in the ADC mode register		
		11	AVDD1 − AVSS; this setting can be used to as a diagnostic to validate other reference values		
[3:0]	RESERVED		These bits are reserved. Set to 0.	0x0	R

SETUP CONFIGURATION REGISTER 1 TO SETUP CONFIGURATION REGISTER 7

Address: 0x21 to 0x27, Reset: 0x1000, Name: SETUPCON1 to SETUPCON7

The remaining seven setup configuration registers share the same 16-bit register layout as SETUPCON0. They configure the reference selection, input buffers, burnout currents, and output coding of the ADC.

Table 34. Summary of SETUPCON1 to SETUPCON7

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x21	SETUPCON1	[15:8]	RESERVED			BI_UNIPOLAR1	REF_BUF 1[1:0]		AIN_BUF 1[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN1	BUFCHOPMAX1		REFSEL1	RESERVED					
0x22	SETUPCON2	[15:8]	RESERVED			BI_UNIPOLAR2	REF_BUF 2[1:0]		AIN_BUF 2[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN2	BUFCHOPMAX2		REFSEL2	RESERVED					
0x23	SETUPCON3	[15:8]	RESERVED			BI_UNIPOLAR3	REF_BUF 3[1:0]		AIN_BUF 3[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN3	BUFCHOPMAX3		REFSEL3	RESERVED					
0x24	SETUPCON4	[15:8]	RESERVED			BI_UNIPOLAR4	REF_BUF 4[1:0]		AIN_BUF 4[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN4	BUFCHOPMAX4		REFSEL4	RESERVED					
0x25	SETUPCON5	[15:8]	RESERVED			BI_UNIPOLAR5	REF_BUF 5[1:0]		AIN_BUF 5[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN5	BUFCHOPMAX5		REFSEL5	RESERVED					
0x26	SETUPCON6	[15:8]	RESERVED			BI_UNIPOLAR6	REF_BUF 6[1:0]		AIN_BUF 6[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN6	BUFCHOPMAX6		REFSEL6	RESERVED					
0x27	SETUPCON7	[15:8]	RESERVED			BI_UNIPOLAR7	REF_BUF 7[1:0]		AIN_BUF 7[1:0]		0x1000	RW
		[7:0]	BURNOUT_EN7	BUFCHOPMAX7		REFSEL7	RESERVED					

FILTER CONFIGURATION REGISTER 0

Address: 0x28, Reset: 0x0000, Name: FILTCON0

The filter configuration registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Table 35. Bit Descriptions for FILTCON0

Bits	Bit Name	Settings	Description	Reset	Access
15	SINC3_MAP0		If this bit is set, the mapping of the filter configuration register changes to directly program the decimation rate of the sinc3 filter for Setup 0. All other options are eliminated. This allows fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel, with single cycle settling disabled, equals FMOD/(32 × FILTCON0[14:0]).	0x0	RW
[14:12]	RESERVED		These bits are reserved. Set to 0.	0x0	R
11	ENHFILTEN0		This bit enables various post filters for enhanced 50 Hz/60 Hz rejection for Setup 0. For this setting to function, the ORDERx bits must also be set to 00 to select the sinc5 + sinc1 filter.	0x0	RW
		0	Disabled		
		1	Enabled		
[10:8]	ENHFILT0		These bits select between various post filters for enhanced 50 Hz/60 Hz rejection for Setup 0.	0x0	RW
		010	27.27 SPS, 47 dB rejection, 36.67 ms settling		
		011	25 SPS, 62 dB rejection, 40 ms settling		
		101	20 SPS, 86 dB rejection, 50 ms settling		
		110	16.67 SPS, 92 dB rejection, 60 ms settling		
7	RESERVED		This bit is reserved. Set to 0.	0x0	R
[6:5]	ORDER0		These bits control the order of the digital filter that processes the modulator data for Setup 0.	0x0	RW
		00	Sinc5 + sinc1 (default)		
		11	Sinc3. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels.		
[4:0]	ODR0		These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup 0.	0x0	RW
		00000	31,250 SPS		
		00001	31,250 SPS		
		00010	31,250 SPS		
		00011	31,250 SPS		
		00100	31,250 SPS		
		00101	31,250 SPS		
		00110	15,625 SPS		
		00111	10,417 SPS		
		01000	5208 SPS		
		01001	2597 SPS (2604 SPS for sinc3)		
		01010	1007 SPS (1008 SPS for sinc3)		
		01011	503.8 SPS (504 SPS for sinc3)		
		01100	381 SPS (400.6 SPS for sinc3)		
		01101	200.3 SPS		
		01110	100.5 SPS		
		01111	59.52 SPS (59.98 SPS for sinc3)		
		10000	49.68 SPS (50 SPS for sinc3)		
		10001	20.01 SPS		
		10010	16.63 SPS (16.67 SPS for sinc3)		
		10011	10 SPS		
		10100	5 SPS		
		10101	2.5 SPS		
		10110	1.25 SPS		

FILTER CONFIGURATION REGISTER 1 TO FILTER CONFIGURATION REGISTER 7

Address Range: 0x29 to 0x2F, Reset: 0x0000, Name: FILTCON1 to FILTCON7

The remaining seven filter configuration registers share the same 16-bit register layout as FILTCON0. They configure the ADC data rate and filter options and map as per their number. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Table 36. Summary of FILTCON1 to FILTCON7

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x29	FILTCON1	[15:8]	SINC3_MAP1	RESERVED			ENHFILTEN1	ENHFILT1			0x0000	RW
		[7:0]	RESERVED	ORDER1		ODR1						
0x2A	FILTCON2	[15:8]	SINC3_MAP2	RESERVED			ENHFILTEN2	ENHFILT2			0x0000	RW
		[7:0]	RESERVED	ORDER2		ODR2						
0x2B	FILTCON3	[15:8]	SINC3_MAP3	RESERVED			ENHFILTEN3	ENHFILT3			0x0000	RW
		[7:0]	RESERVED	ORDER3		ODR3						
0x2C	FILTCON4	[15:8]	SINC3_MAP4	RESERVED			ENHFILTEN4	ENHFILT4			0x0000	RW
		[7:0]	RESERVED	ORDER4		ODR4						
0x2D	FILTCON5	[15:8]	SINC3_MAP5	RESERVED			ENHFILTEN5	ENHFILT5			0x0000	RW
		[7:0]	RESERVED	ORDER5		ODR5						
0x2E	FILTCON6	[15:8]	SINC3_MAP6	RESERVED			ENHFILTEN6	ENHFILT6			0x0000	RW
		[7:0]	RESERVED	ORDER6		ODR6						
0x2F	FILTCON7	[15:8]	SINC3_MAP7	RESERVED			ENHFILTEN7	ENHFILT7			0x0000	RW
		[7:0]	RESERVED	ORDER7		ODR7						

OFFSET REGISTER 0

Address: 0x30, Reset: 0x800000, Name: OFFSET0

The offset (zero-scale) registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

Table 37. Bit Descriptions for OFFSET0

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET0		Offset calibration coefficient for Setup 0.	0x800000	RW

OFFSET REGISTER 1 TO OFFSET REGISTER 7

Address Range: 0x31to 0x37, Reset: 0x800000, Name: OFFSET1 to OFFSET7

The offset (zero-scale) registers, OFFSET1 to OFFSET7, share the same structure (24-bit) as OFFSET0. They can be used individually to compensate for any offset error in the ADC or in the system.

Table 38. Summary of OFFSET1 to OFFSET7

Reg	Name	Bits	Bit[23:0]	Reset	RW
0x31	OFFSET1	[23:0]	OFFSET1[23:0]	0x800000	RW
0x32	OFFSET2	[23:0]	OFFSET2[23:0]	0x800000	RW
0x33	OFFSET3	[23:0]	OFFSET3[23:0]	0x800000	RW
0x34	OFFSET4	[23:0]	OFFSET4[23:0]	0x800000	RW
0x35	OFFSET5	[23:0]	OFFSET5[23:0]	0x800000	RW
0x36	OFFSET6	[23:0]	OFFSET6[23:0]	0x800000	RW
0x37	OFFSET7	[23:0]	OFFSET7[23:0]	0x800000	RW

GAIN REGISTER 0

Address: 0x38, Reset: 0x5XXXX0, Name: GAIN0

The gain (full-scale) registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

Table 39. Bit Descriptions for GAIN0

Bits	Bit Name	Settings	Description	Reset[1]	Access
[23:0]	GAIN0		Gain calibration coefficient for Setup 0.	0x5XXXX0	RW

[1] The value of X varies, depending on the IC that is used.

GAIN REGISTER 1 TO GAIN REGISTER 7

Address Range: 0x39 to 0x3F, Reset: 0x5XXXX0, Name: GAIN1 to GAIN7

The gain (full-scale) registers for GAIN1 to GAIN7 share the same 24-bit structure as that shown by GAIN0 register. They can be used to compensate for any gain error in the ADC or in the system and are assigned as per their number to a given setup.

Table 40. Summary of GAIN1 to GAIN7

Reg	Name	Bits	Bit[23:0]	Reset[1]	RW
0x39	GAIN1	[23:0]	GAIN1[23:0]	0x5XXXX0	RW
0x3A	GAIN2	[23:0]	GAIN2[23:0]	0x5XXXX0	RW
0x3B	GAIN3	[23:0]	GAIN3[[23:0]	0x5XXXX0	RW
0x3C	GAIN4	[23:0]	GAIN4[23:0]	0x5XXXX0	RW
0x3D	GAIN5	[23:0]	GAIN5[23:0]	0x5XXXX0	RW
0x3E	GAIN6	[23:0]	GAIN6[23:0]	0x5XXXX0	RW
0x3F	GAIN7	[23:0]	GAIN7[23:0]	0x5XXXX0	RW

[1] The value of X varies, depending on the IC that is used.

OUTLINE DIMENSIONS

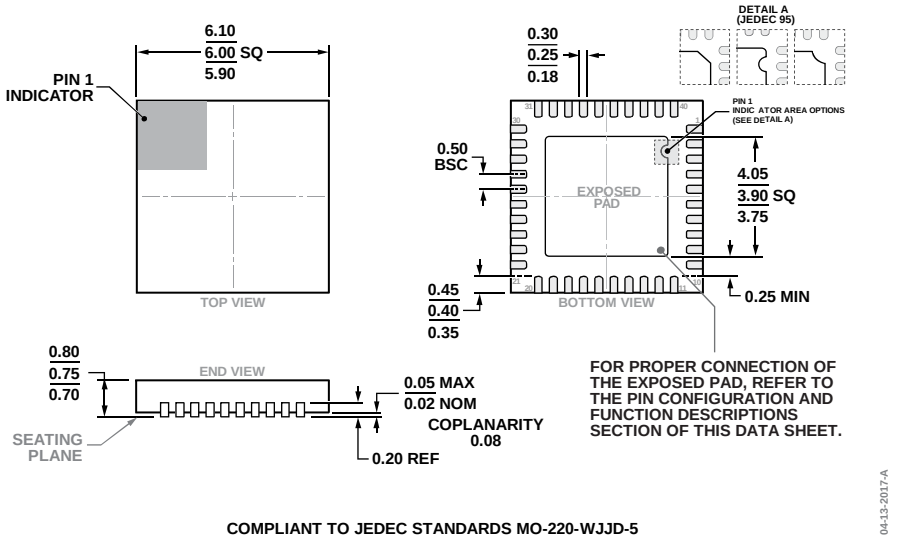


Figure 75. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7173-8BCPZ	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-14
AD7173-8BCPZ-RL	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-14
EVAL-AD7173-8SDZ		Evaluation Board	
EVAL-SDP-CB1Z		Evaluation Controller Board	

[1] Z = RoHS Compliant Part.

NOTES

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