



**THE DATASHEET OF  
SI2302ADS-T1**



## N-Channel 2.5-V (G-S) MOSFET

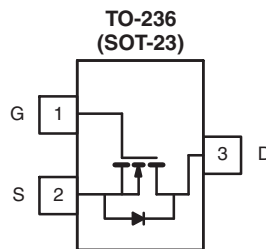
PRODUCT SUMMARY		
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
20	0.060 at $V_{GS} = 4.5$ V	2.4
	0.115 at $V_{GS} = 2.5$ V	2.0

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- 100 %  $R_g$  Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



Top View  
Si2302ADS (2A)\*  
\* Marking Code

**Ordering Information:** Si2302ADS-T1-E3 (Lead (Pb)-free)  
Si2302ADS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	20		V	
Gate-Source Voltage	$V_{GS}$	$\pm 8$			
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	$T_A = 25$ °C	2.4	2.1	A
		$T_A = 70$ °C	1.9	1.7	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	10			
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	0.94	0.6		
Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25$ °C	0.9	0.7	W
		$T_A = 70$ °C	0.57	0.46	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 5$ s	115	140	°C/W
		Steady State	140	175	

Notes:

a. Surface mounted on FR4 board.

For SPICE model information via the Worldwide Web: [www.vishay.com/www/product/spice.htm](http://www.vishay.com/www/product/spice.htm)

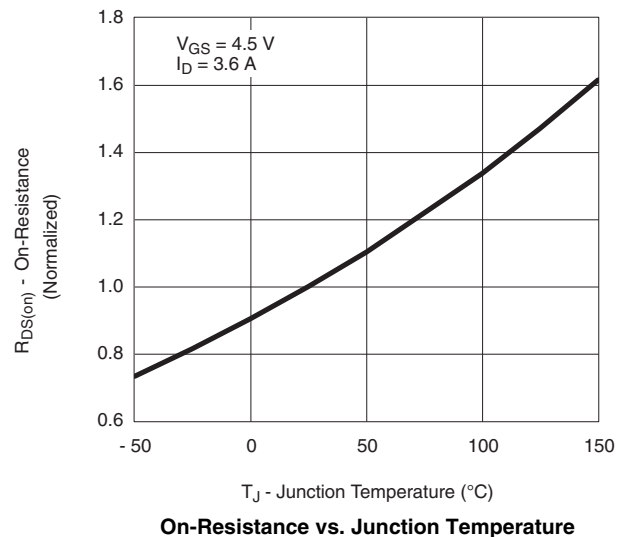
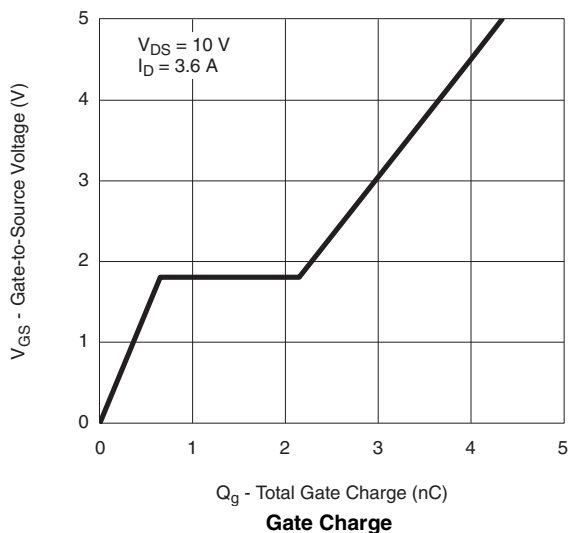
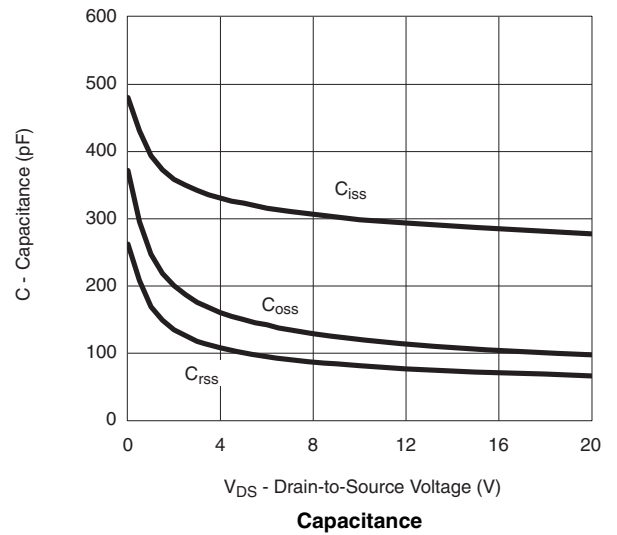
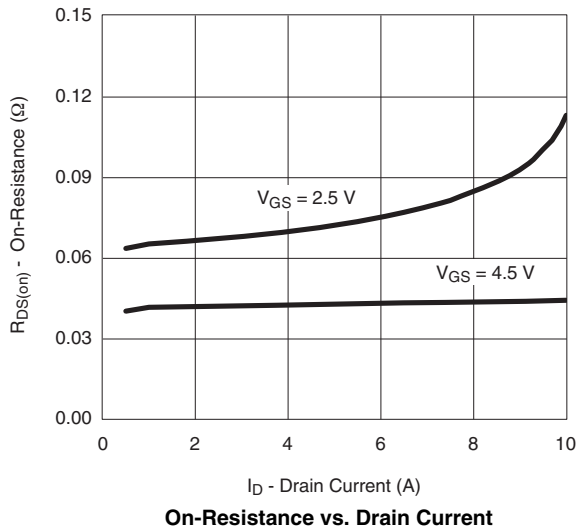
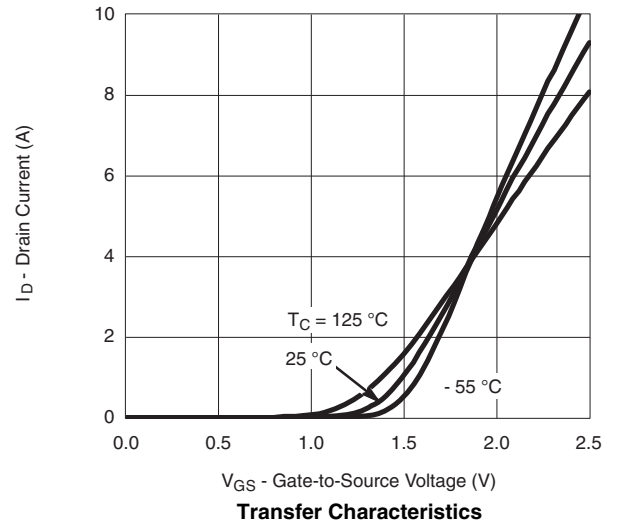
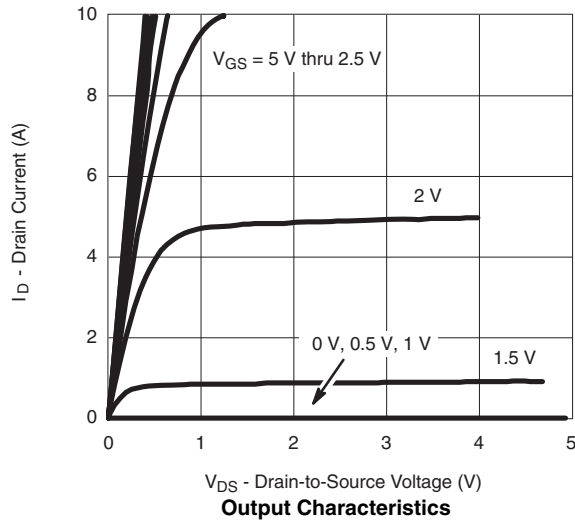
<b>SPECIFICATIONS</b> ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 10\text{ }\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	0.65	0.95	1.2	
Gate Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			0.1	$\mu\text{A}$
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			2.0	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	6			A
		$V_{DS} \geq 5\text{ V}, V_{GS} = 2.5\text{ V}$	4			
Drain-Source On-Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 3.6\text{ A}$		0.045	0.060 <sup>b</sup>	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 3.1\text{ A}$		0.070	0.115	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 5\text{ V}, I_D = 3.6\text{ A}$		8		S
Diode Forward Voltage	$V_{SD}$	$I_S = 0.94\text{ A}, V_{GS} = 0\text{ V}$		0.76	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 3.6\text{ A}$		4.0	10	nC
Gate-Source Charge	$Q_{gs}$			0.65		
Gate-Drain Charge	$Q_{gd}$			1.5		
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		300		pF
Output Capacitance	$C_{oss}$			120		
Reverse Transfer Capacitance	$C_{rss}$			80		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.5	1	2	$\Omega$
<b>Switching</b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 2.8\text{ }\Omega$ $I_D \cong 3.6\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 6\text{ }\Omega$		7	15	ns
Rise Time	$t_r$			55	80	
Turn-Off Delay Time	$t_{d(off)}$			16	60	
Fall Time	$t_f$			10	25	

Notes:

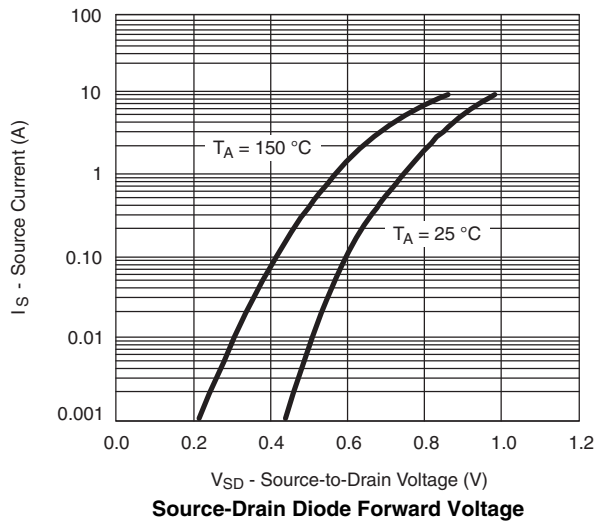
- a. Pulse test;  $PW \leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Effective for production 10/04.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

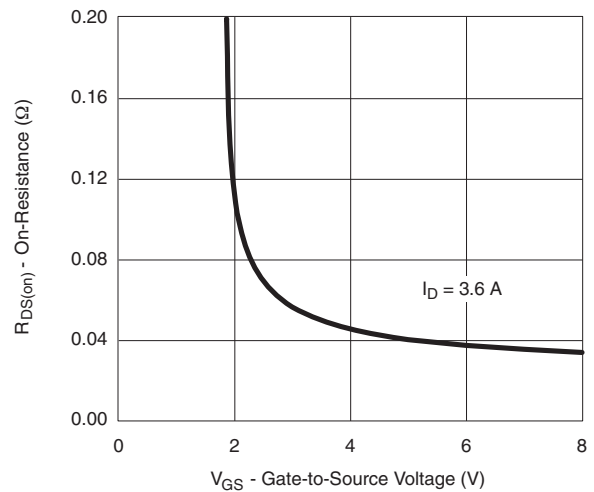
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



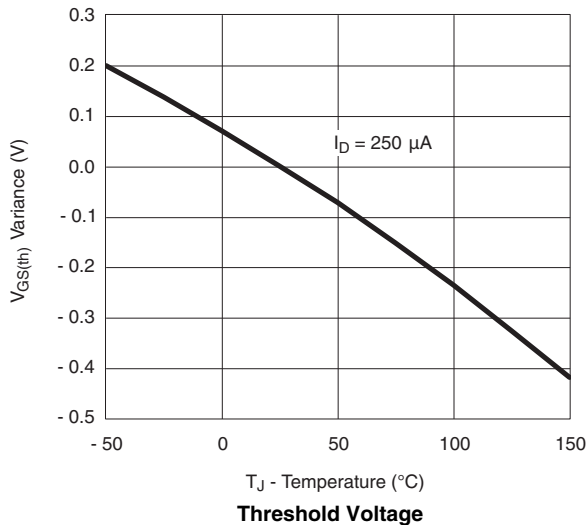
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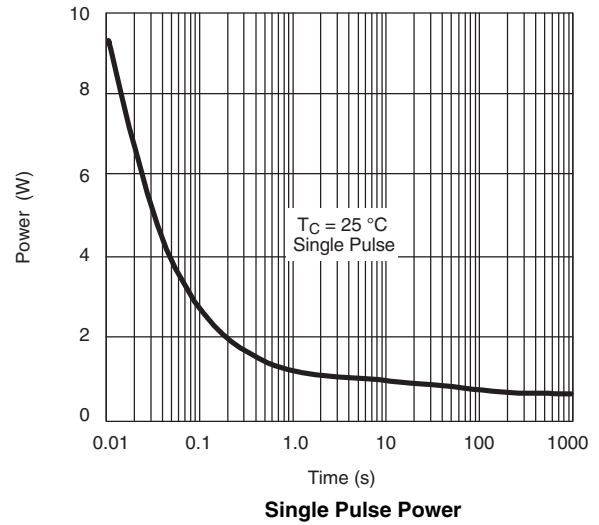
Source-Drain Diode Forward Voltage



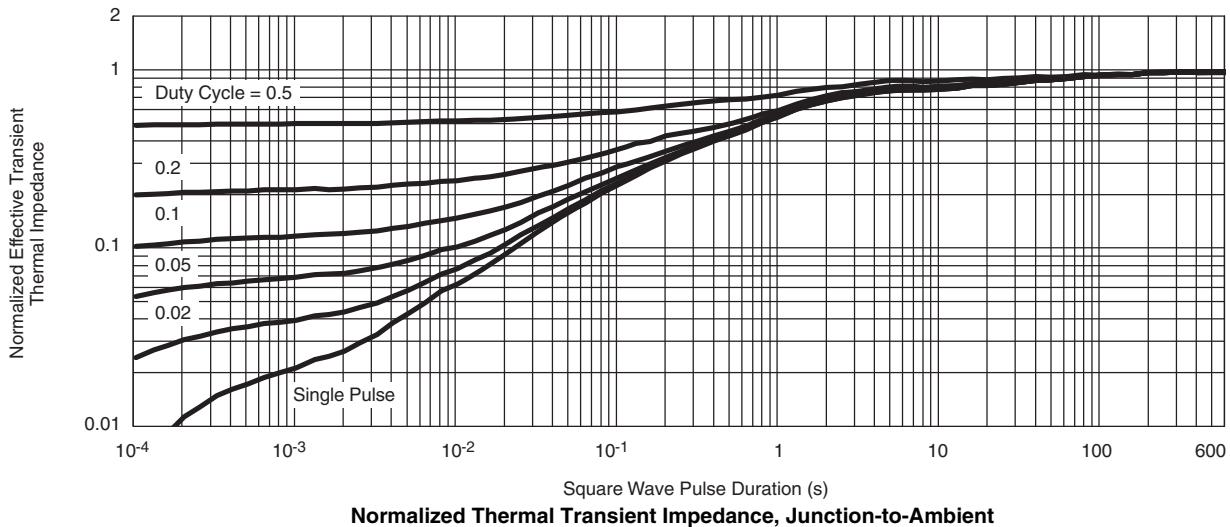
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



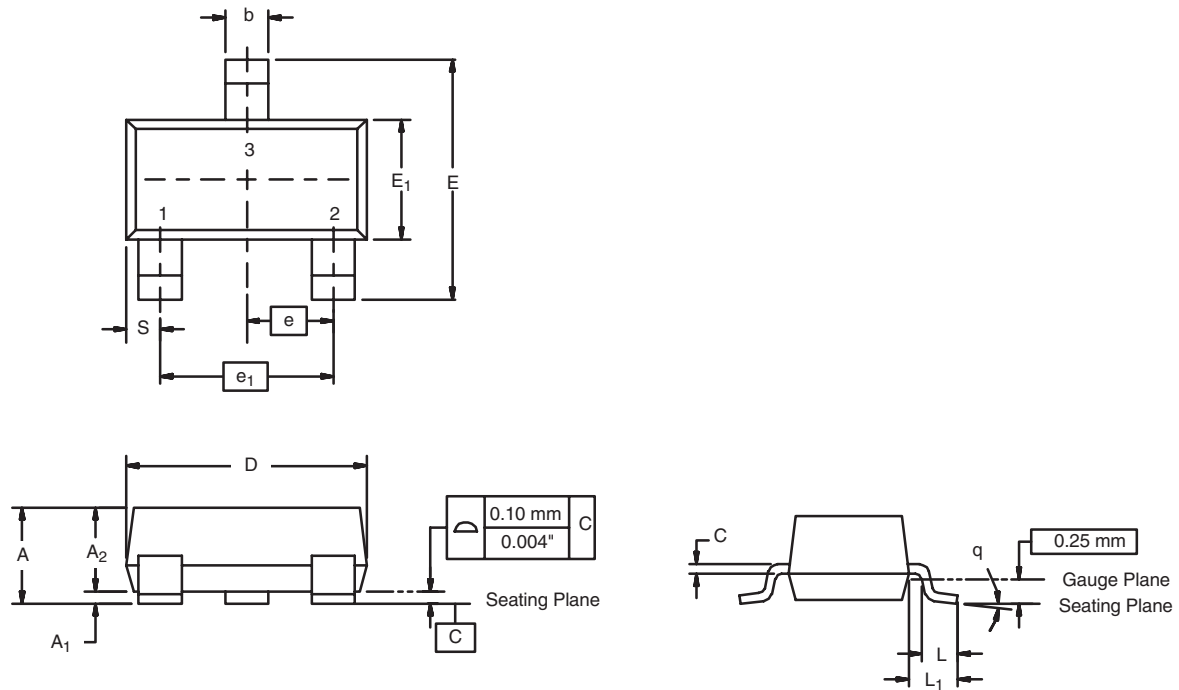
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?71831](http://www.vishay.com/ppg?71831).

## SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A <sub>1</sub>	0.01	0.10	0.0004	0.004
A <sub>2</sub>	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E <sub>1</sub>	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e <sub>1</sub>	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L <sub>1</sub>	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°

ECN: S-03946-Rev. K, 09-Jul-01  
 DWG: 5479

## RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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