



**THE DATASHEET OF
MC74HC164ADR2**



8-Bit Serial-Input/Parallel-Output Shift Register

High-Performance Silicon-Gate CMOS

MC74HC164A

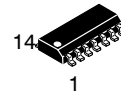
The MC74HC164A is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC74HC164A is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

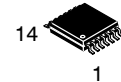
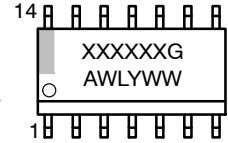
Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 V to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 244 FETs or 61 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

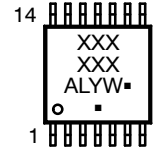
MARKING DIAGRAMS



SOIC-14
D SUFFIX
CASE 751A



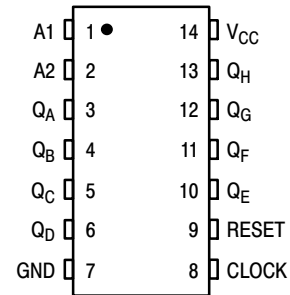
TSSOP-14
DT SUFFIX
CASE 948G



XXX = Specific Device Code
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or \blacksquare = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

MC74HC164A

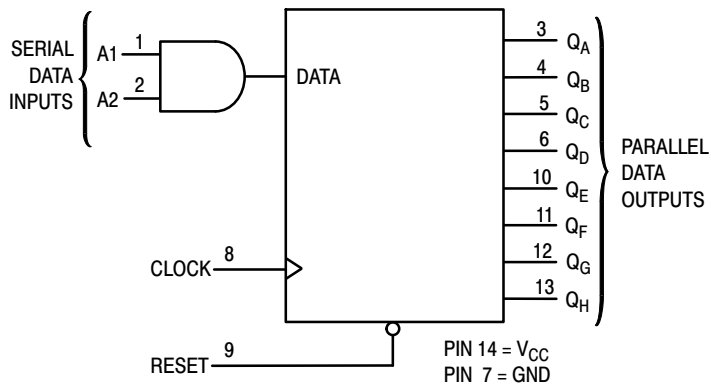


Figure 1. Logic Diagram

FUNCTION TABLE

| Reset | Inputs | | Outputs | | | | |
|-------|--------|----|---------|----------------|-----------------|-----|-----------------|
| | Clock | A1 | A2 | Q _A | Q _B | ... | Q _H |
| L | X | X | X | L | L | ... | L |
| H | | X | X | No Change | | | |
| H | | H | D | D | Q _{An} | ... | Q _{Gn} |
| H | | D | H | D | Q _{An} | ... | Q _{Gn} |

D = data input

Q_{An} - Q_{Gn} = data shifted from the preceding stage on a rising edge at the clock input.

MC74HC164A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit | |
|------------------|--|--|-----------------------|------|
| V _{CC} | DC Supply Voltage | -0.5 to +6.5 | V | |
| V _{IN} | DC Input Voltage | -0.5 to V _{CC} +0.5 | V | |
| V _{OUT} | DC Output Voltage | -0.5 to V _{CC} +0.5 | V | |
| I _{IN} | DC Input Diode Current, per Pin | ±20 | mA | |
| I _{OUT} | DC Output Diode Current, per Pin | ±25 | mA | |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±50 | mA | |
| I _{IK} | Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC}) | ±20 | mA | |
| I _{OK} | Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC}) | ±20 | mA | |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C | |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C | |
| T _J | Junction Temperature Under Bias | +150 | °C | |
| θ _{JA} | Thermal Resistance (Note 1) | SOIC-14 TSSOP-14 | 116 150 | °C/W |
| P _D | Power Dissipation in Still Air at 25°C | SOIC-14 TSSOP-14 | 1077 833 | mW |
| MSL | Moisture Sensitivity | Level 1 | - | |
| F _R | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in. | - |
| V _{ESD} | ESD Withstand Voltage (Note 2) | Human Body Model Charged Device Model | 2000 N/A | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|---|---|-------------------------|------|
| V _{CC} | DC Supply Voltage | 2.0 | 6.0 | V |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Note 3) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 3) | V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V | 0 1000 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|----------------------------------|--|----------------------|------------------|--------|---------|------|
| | | | | -55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |

MC74HC164A

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|--|----------------------|------------------|--------|---------|------|
| | | | | -55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 3.0 | 2.48 | 2.34 | 2.20 | |
| | | | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | | 6.0 | 5.48 | 5.34 | 5.20 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | | 6.0 | 0.26 | 0.33 | 0.40 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 4 | 40 | 160 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|--|---|------------------|--------|---------|------|
| | | | -55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| f _{max} | Maximum Clock Frequency (50% Duty Cycle) (Figures 2, 3) | 2.0 | 10 | 10 | 10 | MHz |
| | | 3.0 | 20 | 20 | 20 | |
| | | 4.5 | 40 | 35 | 30 | |
| | | 6.0 | 50 | 45 | 40 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Clock to Q (Figures 2, 3) | 2.0 | 160 | 200 | 250 | ns |
| | | 3.0 | 100 | 150 | 200 | |
| | | 4.5 | 32 | 40 | 48 | |
| | | 6.0 | 27 | 34 | 42 | |
| t _{PHL} | Maximum Propagation Delay, Reset to Q (Figures 2, 4) | 2.0 | 175 | 220 | 260 | ns |
| | | 3.0 | 100 | 150 | 200 | |
| | | 4.5 | 35 | 44 | 53 | |
| | | 6.0 | 30 | 37 | 45 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 2, 3) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{in} | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Package)* | Typical @ 25°C, V _{CC} = 5.0 V | | | pF | |
| | | 180 | | | | |

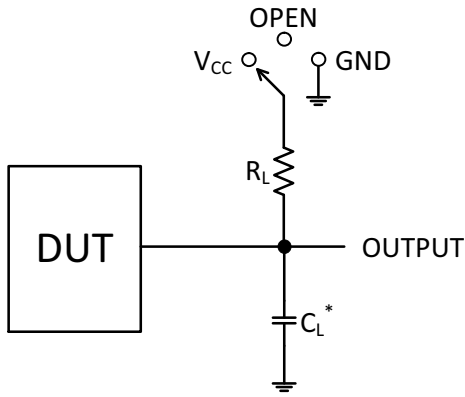
* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

MC74HC164A

TIMING REQUIREMENTS

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|---------------------------------|--|----------------------|------------------|--------|---------|------|
| | | | -55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{su} | Minimum Setup Time, A1 or A2 to Clock (Figure 5) | 2.0 | 25 | 35 | 40 | ns |
| | | 3.0 | 15 | 20 | 25 | |
| | | 4.5 | 7 | 8 | 9 | |
| | | 6.0 | 5 | 6 | 6 | |
| t _h | Minimum Hold Time, Clock to A1 or A2 (Figure 5) | 2.0 | 3 | 3 | 3 | ns |
| | | 3.0 | 3 | 3 | 3 | |
| | | 4.5 | 3 | 3 | 3 | |
| | | 6.0 | 3 | 3 | 3 | |
| t _{rec} | Minimum Recovery Time, Reset Inactive to Clock (Figure 4) | 2.0 | 3 | 3 | 3 | ns |
| | | 3.0 | 3 | 3 | 3 | |
| | | 4.5 | 3 | 3 | 3 | |
| | | 6.0 | 3 | 3 | 3 | |
| t _w | Minimum Pulse Width, Clock (Figure 3) | 2.0 | 50 | 60 | 75 | ns |
| | | 3.0 | 26 | 35 | 45 | |
| | | 4.5 | 12 | 15 | 20 | |
| | | 6.0 | 10 | 12 | 15 | |
| t _w | Minimum Pulse Width, Reset (Figure 4) | 2.0 | 50 | 60 | 75 | ns |
| | | 3.0 | 26 | 35 | 45 | |
| | | 4.5 | 12 | 15 | 20 | |
| | | 6.0 | 10 | 12 | 15 | |
| t _r , t _f | Maximum Input Rise and Fall Times (Figure 3) | 2.0 | 1000 | 1000 | 1000 | ns |
| | | 3.0 | 800 | 800 | 800 | |
| | | 4.5 | 500 | 500 | 500 | |
| | | 6.0 | 400 | 400 | 400 | |

MC74HC164A



| Test | Switch Position | C _L | R _L |
|-------------------------------------|-----------------|----------------|----------------|
| t _{PLH} / t _{PHL} | Open | 50 pF | 1 kΩ |
| t _{PLZ} / t _{PZL} | V _{CC} | | |
| t _{PHZ} / t _{PZH} | GND | | |

*C_L Includes probe and jig capacitance

Figure 2. Test Circuit

SWITCHING WAVEFORMS

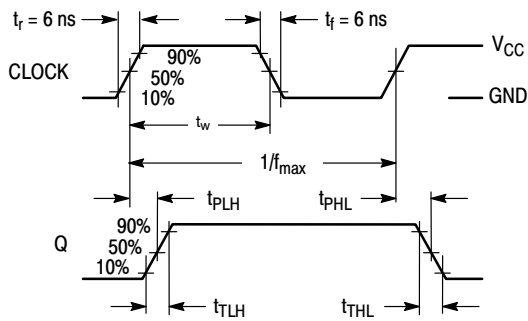


Figure 3.

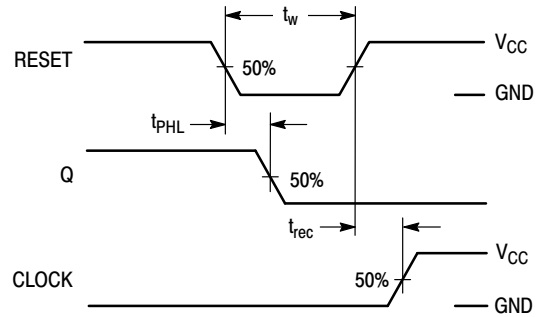


Figure 4.

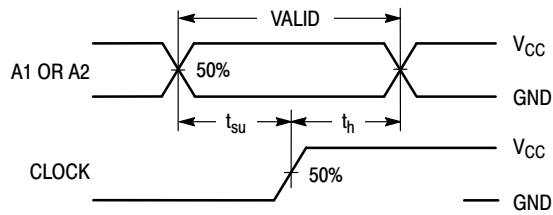


Figure 5.

MC74HC164A

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 1, 2)

Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data-enable input. When only one serial input is used, the other must be connected to V_{CC} .

Clock (Pin 8)

Shift Register Clock. A positive-going transition on this pin shifts the data at each stage to the next stage. The shift

register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

$Q_A - Q_H$ (Pins 3, 4, 5, 6, 10, 11, 12, 13)

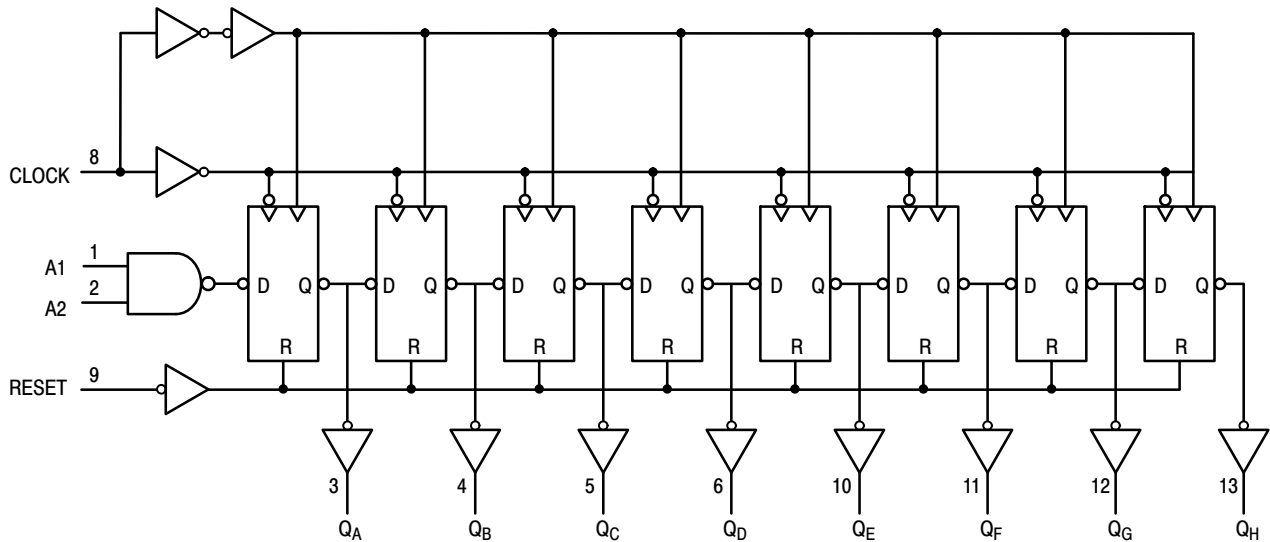
Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

CONTROL INPUT

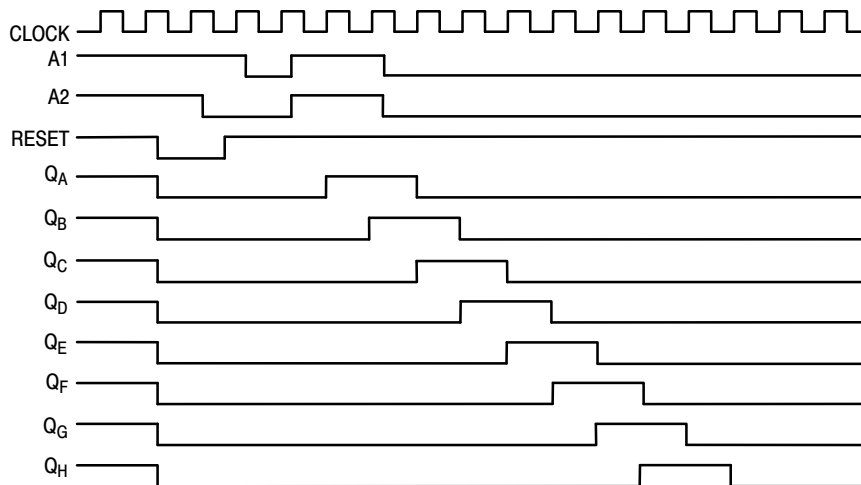
Reset (Pin 9)

Active-Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip-flops and sets Outputs $Q_A - Q_H$ to the low level state.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



MC74HC164A

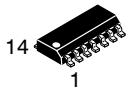
ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|--------------------|------------|----------|--------------------------|
| MC74HC164ADR2G | HC164AG | SOIC-14 | 2500 Units / Tape & Reel |
| MC74HC164ADTR2G | HC 164A | TSSOP-14 | 2500 Units / Tape & Reel |
| MC74HC164ADTR2G-Q* | HC 164A | TSSOP-14 | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

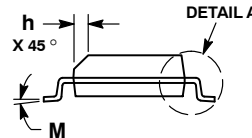
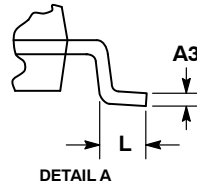
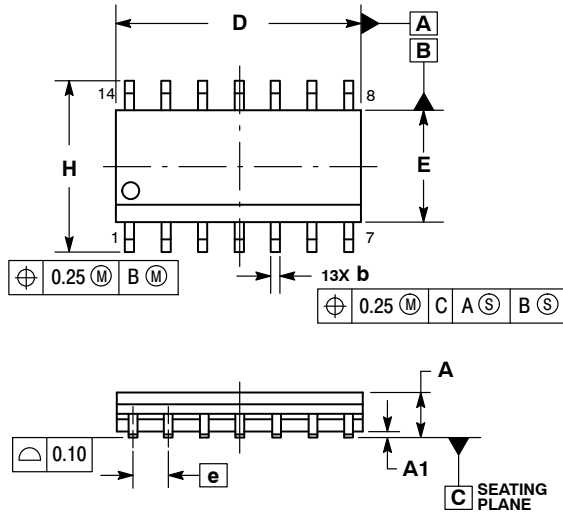
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

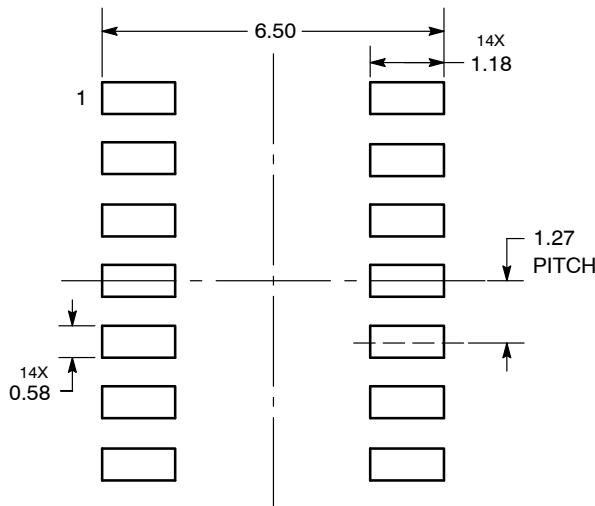


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

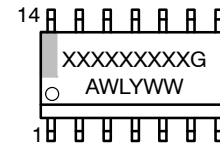
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

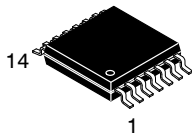
STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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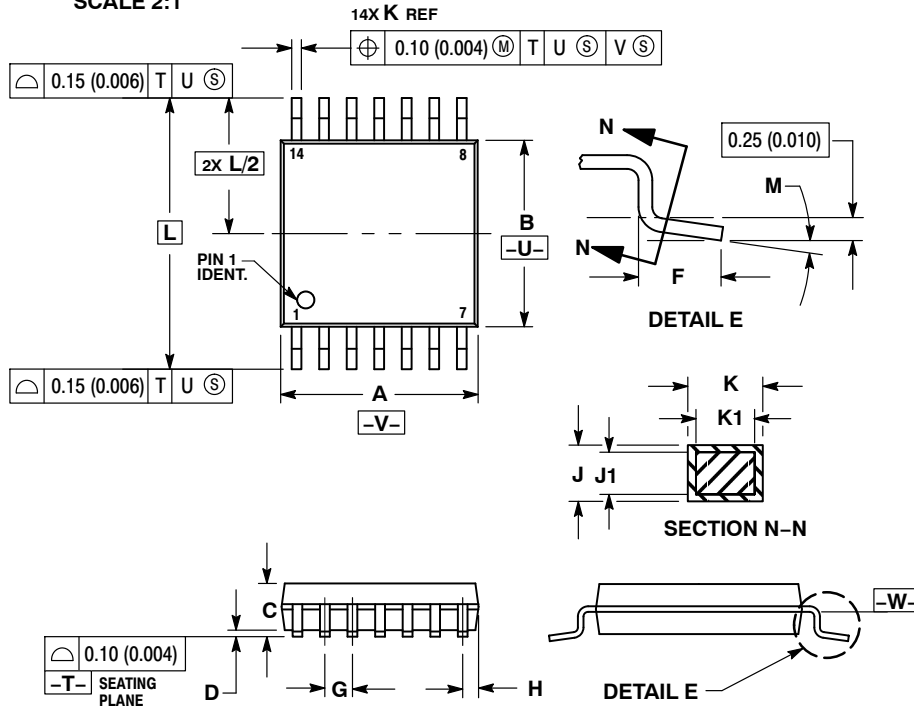
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

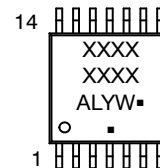


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*

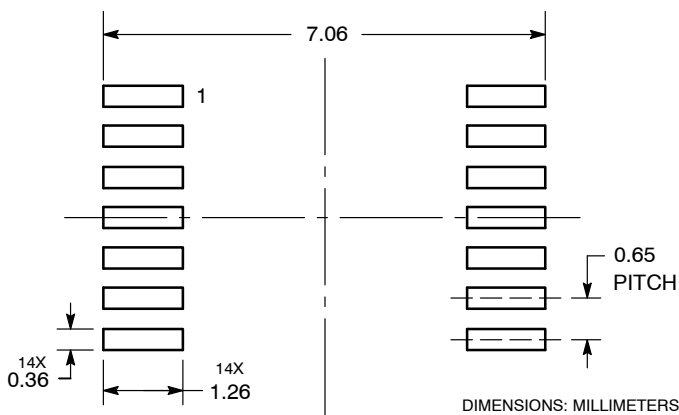


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



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|-------------------------|--------------------|--|
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