THE DATASHEET OF

AD8390AACPZ-R7

Low Power, High Output Current Differential Amplifier

Data Sheet

AD8390A

FEATURES

- Voltage feedback amplifier
  - Ideal for ADSL and ADSL2+ central office (CO) and customer premises equipment (CPE) applications
  - Enables high current differential applications
- Low power operation
  - Single- or dual-supply operation from 10 V (± 5 V) up to 24 V (± 12 V)
  - 5.5 mA total quiescent supply current for full power ADSL and ADSL2+ CO applications
  - Adjustable supply current to minimize power consumption
- High output voltage and current drive
  - 400 mA peak output drive current
  - 44 V p-p differential output voltage
- Low distortion
  - −70 dBc MTPR, 26 kHz to 1.1 MHz
  - −65 dBc MTPR, 1.1 MHz to 2.2 MHz
- High speed: 260 V/µs differential slew rate

FUNCTIONAL BLOCK DIAGRAM

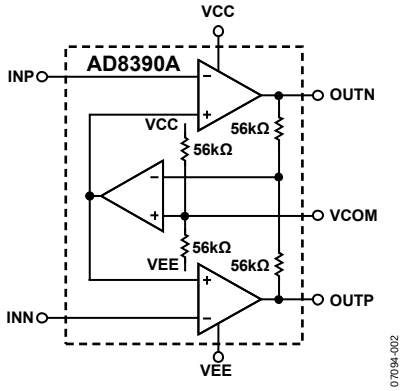

Figure 1.

APPLICATIONS

- ADSL/ADSL2+ CO and CPE line drivers
- xDSL line drivers
- High current differential amplifiers

GENERAL DESCRIPTION

The AD8390A is a high output current, low power consumption differential amplifier. It is particularly well suited for the central office (CO) driver interface in digital subscriber line systems such as ADSL and ADSL2+. In full bias operation, the driver delivers 20.4 dBm output power into low resistance loads while compensating for hybrid and transformer insertion losses and back termination resistors.

The AD8390A is available in a thermally enhanced LFCSP package (16-lead LFCSP). Significant control and flexibility in bias current have been designed into the AD8390A. Four power modes are selectable via two digital inputs, PD0 and PD1, providing three levels of driver bias and one power-down state. In addition, the I_{ADJ} pin is available for fine quiescent current trimming to tailor the performance of the AD8390A.

The low power consumption, high output current, high output voltage swing, and robust thermal packaging enable the AD8390A to be used as the central office line driver in ADSL, ADSL2+, and proprietary xDSL systems, as well as in other high current applications requiring a differential amplifier.

Rev. C

Document Feedback

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REVISION HISTORY

5/2016—Rev. B to Rev. C

Changed CP-16-4 to CP-16-23 ... Throughout
Change to Table 3 ... 4
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Updated Outline Dimensions ... 12
Changes to Ordering Guide ... 12

2/2013—Revision B: Initial Version

SPECIFICATIONS

V_S = ±12 V or V_S = 24 V, R_L = 100 Ω, G = 10, PD(1:0) = (1,1), I_{ADJ} = NC, VCOM = NC (bypassed with 0.1 µF capacitor), T_A = 25°C, unless otherwise noted. Refer to the basic test circuit in Figure 14.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p, R_F = 10 kΩ	38	45		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p	35	38		MHz
Peaking	V_{OUT} = 0.2 V p-p		0.1		dB
Slew Rate	V_{OUT} = 4 V p-p		260		V/µs
NOISE/DISTORTION PERFORMANCE					
Multitone Power Ratio (26 kHz to 1.1 MHz)	Z_{LINE} = 100 Ω, P_{LINE} = 20.4 dBm, crest factor (CF) = 5.4		−70		dBc
Multitone Power Ratio (1.1 MHz to 2.2 MHz)	Z_{LINE} = 100 Ω, P_{LINE} = 20.4 dBm, crest factor (CF) = 5.4		−65		dBc
Voltage Noise (RTI)	f = 10 kHz		5		nV/√Hz
INPUT CHARACTERISTICS					
RTI Offset Voltage ($V_{OS,DM(RTI)}$)	V_{INP} − V_{INN}, VCOM = midsupply	−3.0	±1.0	+3.0	mV
	V_{INP} − V_{INN}, VCOM = NC	−3.0	±1.0	+3.0	mV
±Input Bias Current			−4.0	−7.0	µA
Input Offset Current		−0.35	±0.05	+0.35	µA
Input Resistance			400		kΩ
Input Capacitance			2		pF
Common-Mode Rejection Ratio	$(\Delta V_{OS,DM(RTI)})/(\Delta V_{IN,CM})$	58	69		dB
OUTPUT CHARACTERISTICS					
Differential Output Voltage Swing	ΔV_{OUT}	42.8	44	44.6	V
Output Balance Error	$(\Delta V_{OS,CM})/\Delta V_{OUT}$		60		dB
Linear Output Current	R_L = 10 Ω, f_C = 100 kHz		400		mA
Output Impedance	f_C = 2 MHz		0.1		Ω
Output Common-Mode Offset	$(V_{OUTP} + V_{OUTN})/2$, VCOM = midsupply	−75	±35	+75	mV
	$(V_{OUTP} + V_{OUTN})/2$, VCOM = NC	−75	±35	+75	mV
POWER SUPPLY					
Operating Range (Dual Supply)		±5		±12	V
Operating Range (Single Supply)		10		24	V
Total Quiescent Current, I_{ADJ} = VEE	PD(1:0) = (1,1)		5.5	6.5	mA
	PD(1:0) = (1,0)		4.0	5.0	mA
	PD(1:0) = (0,1)		2.6	3.5	mA
	PD(1:0) = (0,0)		0.56	1.0	mA
Total Quiescent Current, I_{ADJ} = NC	PD(1:0) = (1,1)		10.0	11.0	mA
	PD(1:0) = (1,0)		6.7	8.0	mA
	PD(1:0) = (0,1)		3.8	5.0	mA
	PD(1:0) = (0,0)		0.67	1.0	mA
Power Supply Rejection Ratio (PSRR)	$\Delta V_{OS,DM}/\Delta V_S$, ΔV_S = ±1 V, VCOM = midsupply	72	94		dB
PD(1:0) = 0 (Low Logic State)				0.8	V
PD(1:0) = 1 (High Logic State)		1.6			V
VCOM					
Input Voltage Range		−11.0		+10.0	V
Input Resistance			28		kΩ
VCOM Accuracy	$\Delta V_{OUT,CM}/\Delta VCOM$	0.995	1.0	1.005	V/V

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VCC – VEE)	26 V
VCOM	VEE < VCOM < VCC
Package Power Dissipation	See Figure 2
Maximum Junction Temperature ($T_{J\ MAX}$)	150°C
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified in still air with exposed pad soldered to 4-layer JEDEC test board. θ_{JC} is specified at the exposed pad.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead LFCSP (CP-16-23)	30.4	16	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8390A is limited by its junction temperature on the die.

The maximum safe junction temperature of plastic encapsulated devices, as determined by the glass transition temperature of the plastic, is 150°C. Exceeding this limit temporarily may cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding this limit for an extended period can result in device failure.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature. θ_{JA} values are approximations.

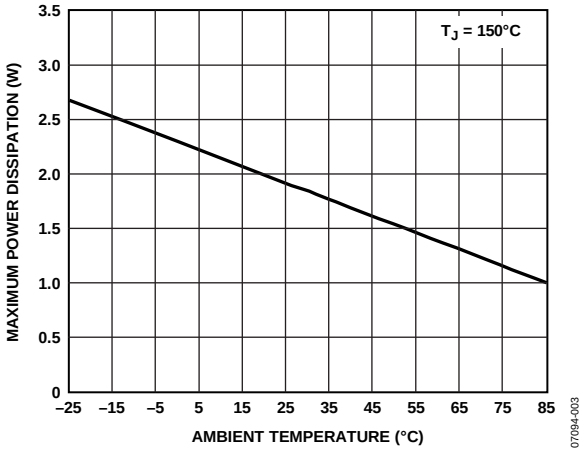

Figure 2. Maximum Power Dissipation vs. Temperature

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming that the load R_L is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, part of which is dissipated in the package and part in the load ($V_{OUT} \times I_{OUT}$).

RMS output voltages must be considered. If R_L is referenced to VEE as in single-supply operation, the total power is $V_S \times I_{OUT}$.

In single-supply operation with R_L referenced to VEE, the worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more copper in direct contact with the package leads from PCB traces, through holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

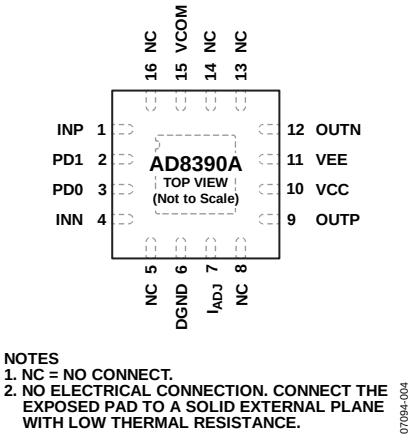

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INP	Amplifier Noninverting Input.
2	PD1	Power Mode Control.
3	PD0	Power Mode Control.
4	INN	Amplifier Inverting Input.
5	NC	No Connection.
6	DGND	Ground.
7	I_{ADJ}	Bias Current Adjustment.
8	NC	No Connection.
9	OUTP	Amplifier Noninverting Output.
10	VCC	Positive Power Supply.
11	VEE	Negative Power Supply.
12	OUTN	Amplifier Inverting Output.
13	NC	No Connection.
14	NC	No Connection.
15	VCOM	Common-Mode Voltage.
16	NC	No Connection.
	EPAD	Exposed pad. No electrical connection. Connect the exposed pad to a solid external plane with low thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±12 V, R_L = 100 Ω, G = 10, PD(1:0) = (1,1), I_{ADJ} = NC, VCOM = NC (bypassed with 0.1 µF capacitor), T_A = 25°C, unless otherwise noted. Refer to the basic test circuit in Figure 14.

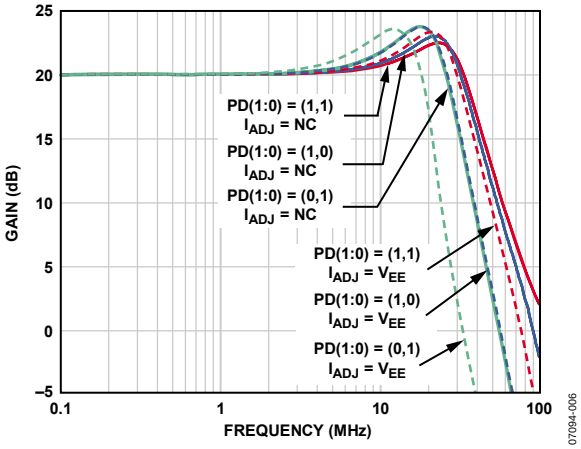

Figure 4. Differential Small Signal Frequency Response; V_S = ±12 V, Gain = 10, V_{OUT} = 200 mV p-p

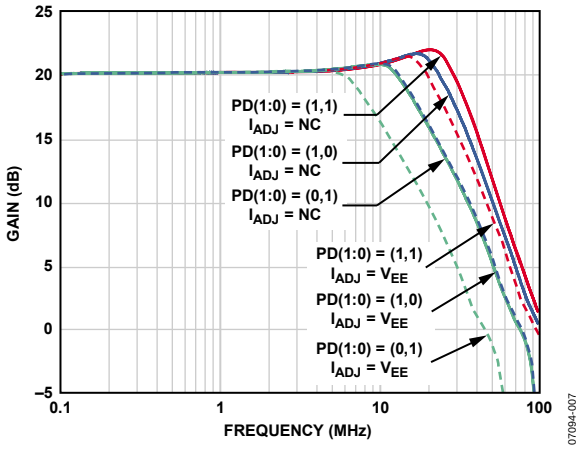

Figure 5. Differential Large Signal Frequency Response; V_S = ±12 V, Gain = 10, V_{OUT} = 4 V p-p

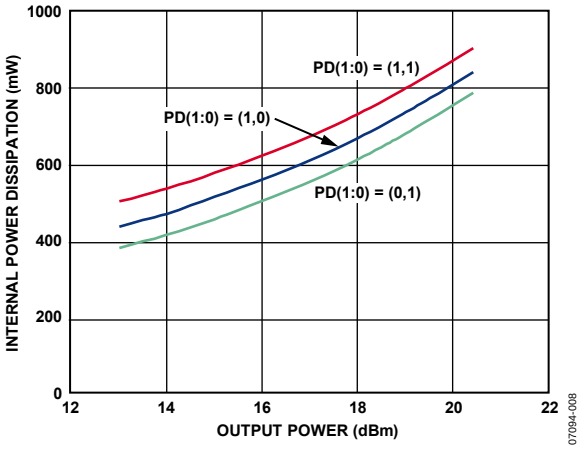

Figure 6. Internal Power Dissipation vs. Output Power; Transformer Turns Ratio = 1:1.4

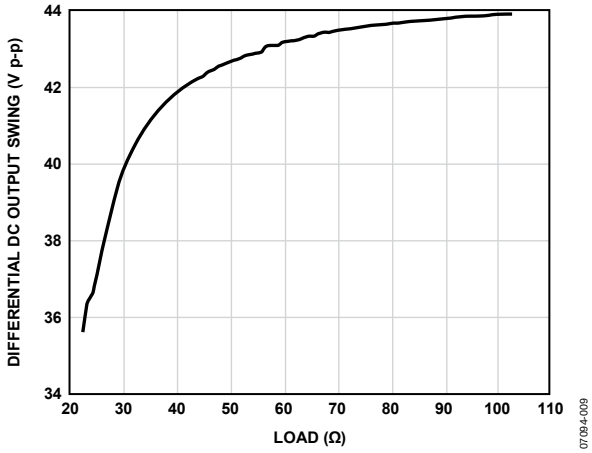

Figure 7. Differential DC Output Swing vs. R_L; V_S = ±12 V, PD(1:0) = (1,1), R_{IADJ} = NC

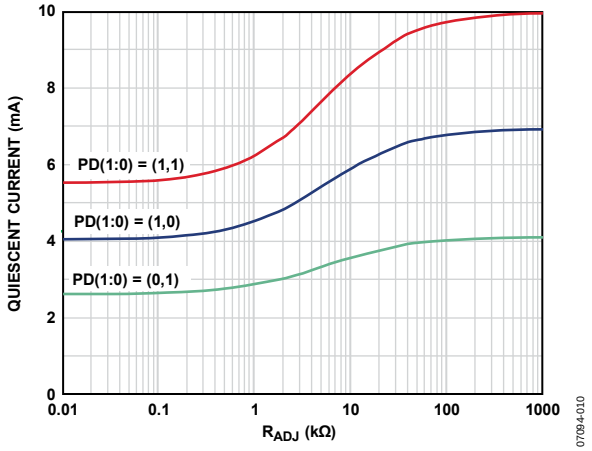

Figure 8. Quiescent Current vs. I_{ADJ} Resistor; V_S = ±12 V

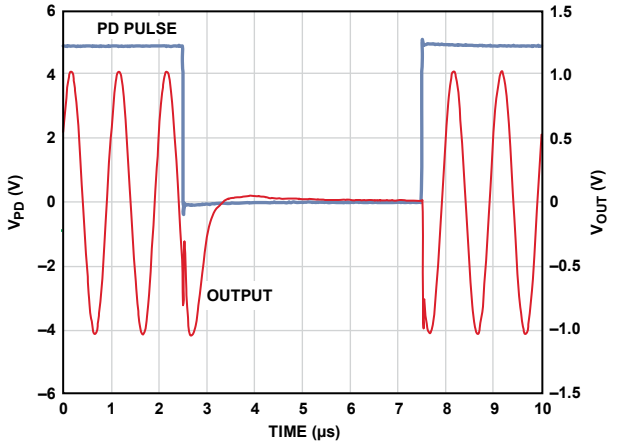

Figure 9. Power-Down to Power-Up Time; PD(1:0) = (1,1) to PD(1:0) = (0,0) to PD(1:0) = (1,1)

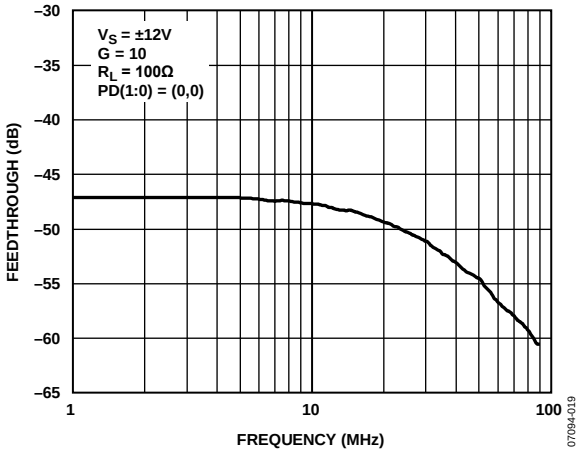

Figure 10. Signal Feedthrough

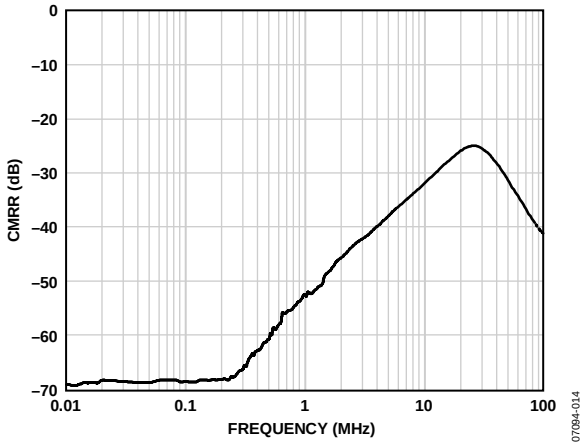

Figure 12. CMRR vs. Frequency; V_{IN} = 200 mV p-p, Gain = 10, I_{ADJ} = NC

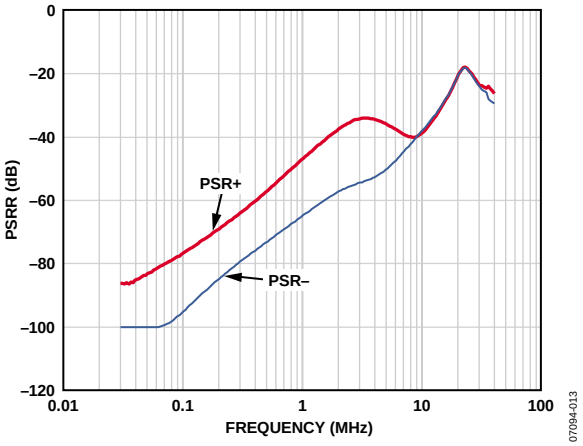

Figure 11. PSRR vs. Frequency; PD(1:0) = (1,1)

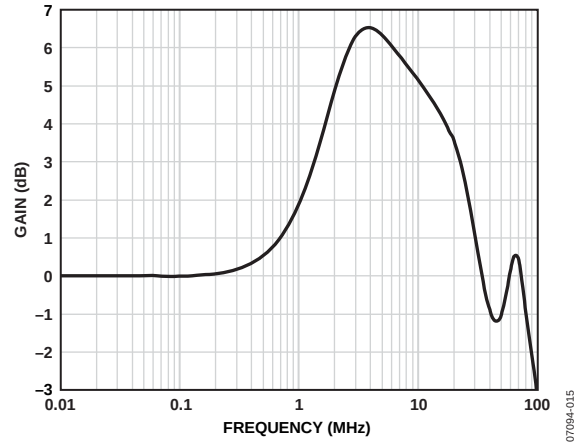

Figure 13. Gain with VCOM Driven vs. Frequency; VCOM = 200 mV p-p

TEST CIRCUITS

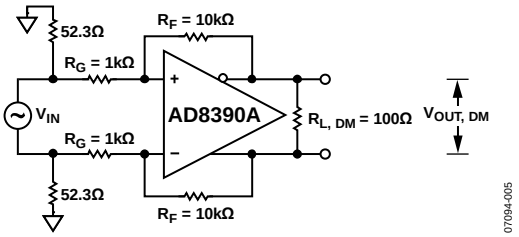

Figure 14. Basic Test Circuit

THEORY OF OPERATION

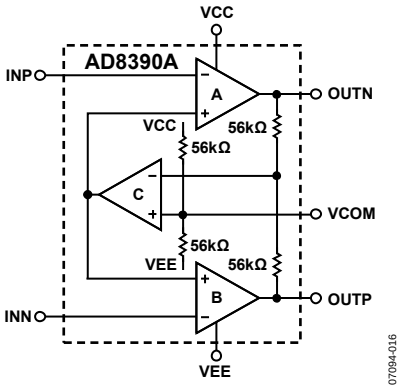

Figure 15. Functional Block Diagram

The AD8390A is a true differential amplifier with common-mode feedback. The AD8390A is functionally equivalent to three amplifiers, as shown in Figure 15. Amplifier A and Amplifier B form a standard dual amplifier in an inverting configuration. Amplifier C maintains the common-mode voltage VCOM at the output.

With VCOM left unconnected, the outputs are internally biased to midsupply. VCOM can be driven externally to set the dc output common-mode voltage.

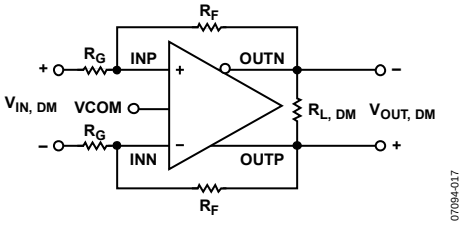

Figure 16. Basic Application Circuit

The high open-loop gain of the AD8390A and the negative feedback minimize the differential and common-mode error voltages.

With the differential and common-mode error voltages assumed to be 0, the differential-mode gain and input impedance of the basic application circuit shown in Figure 16 are as follows:

$$\frac{V_{OUT,DM}}{V_{IN,DM}} = \frac{R_F}{R_G}$$

$$R_{IN,DM} = 2 \times R_G$$

APPLICATIONS INFORMATION

SUPPLIES, GROUNDING, AND LAYOUT

The AD8390A can be powered from either single or dual supplies, with the total supply voltage ranging from 10 V to 24 V. For optimum performance, use well-regulated low ripple supplies.

As with all high speed amplifiers, pay close attention to supply decoupling, grounding, and overall board layout. Provide low frequency supply decoupling with 10 µF tantalum capacitors from each supply to ground. In addition, decouple all supply pins with 0.1 µF quality ceramic chip capacitors placed as close as possible to the driver. Use an internal low impedance ground plane to provide a common ground point for all driver and decoupling capacitor ground requirements. Whenever possible, use separate ground planes for analog and digital circuitry.

Follow high speed layout techniques to minimize parasitic capacitance around the inverting inputs. Some practical examples of these techniques are keeping feedback traces as short as possible and clearing away ground plane in the area of the inverting inputs.

Keep input and output traces as short as possible and as far apart from each other as practical to minimize crosstalk. Keep all differential signal traces as symmetrical as possible.

VCOM PIN

By design, the VCOM pin is internally biased at midsupply, eliminating the need for external resistors. However, the designer may set VCOM to other voltage levels with an external low impedance source.

When the VCOM pin is left unconnected, decouple it with a 0.1 µF capacitor to ground, placed in close proximity to the AD8390A.

With dual equal supplies, connect the VCOM pin directly to ground to bias the outputs at midsupply, eliminating the need for the external decoupling capacitor.

POWER MANAGEMENT

The AD8390A offers significant versatility for maximizing efficiency while maintaining optimal levels of performance.

Optimizing driver efficiency while delivering the required signal level is accomplished with two on-chip power management features: two PD pins to select one of four bias modes and an I_{ADJ} pin for fine bias adjustments.

PD(1:0) Pins

Two CMOS-compatible logic pins, PD1 and PD0, select one of three active power levels and a power-down mode.

The digital ground pin (DGND) is the logic ground reference for the PD(1:0) pins. PD(1:0) = (0,0) is the power-down mode.

The PD pins are internally connected to DGND via termination resistors. When the PD pins are left unconnected, the AD8390A is in power-down mode.

The AD8390A exhibits a low output impedance in the three active modes. The output impedance in the power-down mode is high but undefined and may not be suitable for systems that rely on a high impedance OFF state, such as multiplexing.

I_{ADJ} Pin

The I_{ADJ} pin provides bias current fine-tuning.

With the I_{ADJ} pin unconnected, the bias currents are internally set to 10 mA, 6.7 mA, and 3.8 mA for the three active modes.

With the I_{ADJ} pin connected to the negative supply (VEE), the bias currents are reduced by approximately 50%.

A resistor, R_{ADJ}, connected between the I_{ADJ} pin and the negative supply, provides fine bias adjustment as shown in Figure 8.

Table 5. PD and I_{ADJ} Selection Guide

PD1	PD0	R_{ADJ} (Ω)	I_Q (mA)
1	1	∞	10.0
1	0	∞	6.7
0	1	∞	3.8
0	0	∞	0.67
1	1	0	5.5
1	0	0	4.0
0	1	0	2.6
0	0	0	0.56

ADSL AND ADSL2+ APPLICATIONS

In a typical ADSL/ADSL2+ application, a differential line driver drives the signal from the analog front end (AFE) onto the twisted pair telephone line. Referring to the typical circuit representation in Figure 17, the differential input appears at V_{IN+} and V_{IN-} from the AFE. The differential output is transformer-coupled to the telephone line at tip and ring. The common-mode operating point, generally midway between the supplies, is set through VCOM.

In ADSL/ADSL2+ applications, it is common practice to conserve power by using positive feedback (R3 in Figure 17) to synthesize the output resistance, lowering the required value of the line matching resistors, R_M.

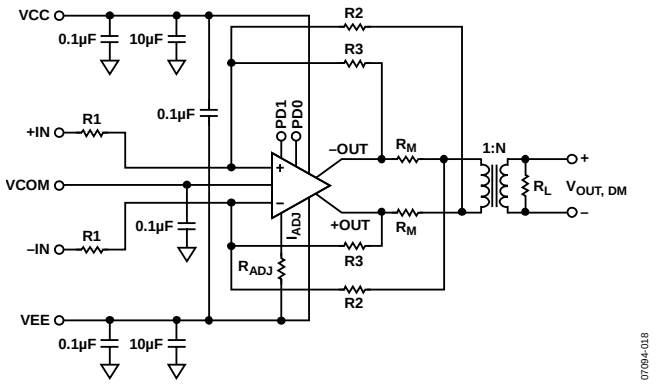

Figure 17. ADSL/ADSL2+ Application Circuit

The differential input impedance to the circuit is 2 × R1. R1 is chosen by the designer to match system requirements.

The synthesized value of the back termination resistor is given by the following equation.

$$R_M = k \times \frac{R_L}{2 \times N^2}$$

where R_L is the line impedance, and N is the turns ratio of the transformer.

The factor k defines the relationship between the negative and positive feedback resistors and is given by

$$k = 1 - \frac{R3}{R2}$$

Commonly used values for k are between 0.1 and 0.25. Values less than 0.1 can lead to instability and are not recommended.

Assuming low values for back termination resistor R_M, R3 is approximated as

$$R3 \cong R1 \times 2 \times k \times A_V$$

where A_V is the voltage gain.

R2 is given by

$$R2 = \frac{R3}{1-k}$$

With R_M, R3, and R2 calculated, the closest 1% resistors are chosen and the gain rechecked with the following equation:

$$A_V = \frac{R2 \times R3}{R1\left[R_M + R2(k+1) - R3\right]}$$

Table 6 compares the results of the exact values, the simplified approximation, and the closest 1% resistor value calculations. In this example, R1 = 1.0 kΩ, A_V = 10, and k = 0.1.

Note that decreasing the value of the back termination resistors attenuates the receive signal by approximately 1/k. Advances in low noise receive amplifiers permit the use of k values as small as 0.1.

The line impedance, turns ratio, and k factor specify the output voltage and current required from the AD8390A. To accommodate higher crest factors or lower supply rails, the turns ratio, N, may need to be increased. Because higher turns ratios and smaller k factors both attenuate the receive signal, a large increase in N may require an increase in k to maintain the desired noise performance. Any particular design process requires that these trade-offs be addressed.

Table 6. Resistor Selection

Component	Exact Value	Approximate Calculation	Standard 1% Resistor Value
R1 (Ω)	1000	1000	1000
R2 (Ω)	2246.95	2222.22	2210
R3 (Ω)	2022.25	2000	2000
R_M (Ω)	5	5	4.99
Actual A_V	10.000	9.889	10.138
Actual k	0.1	0.1	0.095

LIGHTNING AND AC POWER FAULT

When the AD8390A is an ADSL/ADSL2+ line driver, it is transformer-coupled to the twisted pair telephone line. In this environment, the AD8390A is subject to large line transients resulting from events such as lightning strikes or downed power lines. Additional circuitry is required to protect the AD8390A from damage due to these events.

OUTLINE DIMENSIONS

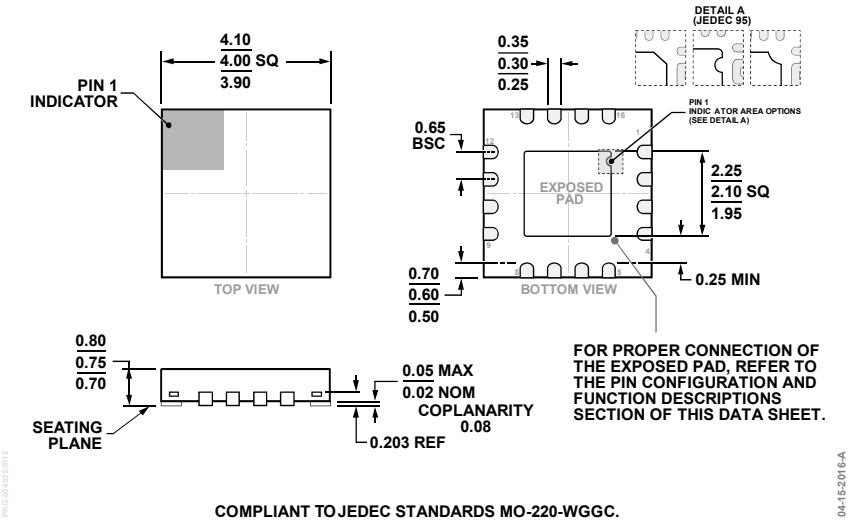

Figure 18. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8390AACPZ-R2	−40°C to +85°C	16-Lead LFCSP, 250 Piece Reel	CP-16-23
AD8390AACPZ-RL	−40°C to +85°C	16-Lead LFCSP, 13″ Tape and Reel	CP-16-23
AD8390AACPZ-R7	−40°C to +85°C	16-Lead LFCSP, 7″ Tape and Reel	CP-16-23

[1] Z = RoHS Compliant Part.

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- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management