# THE DATASHEET OF

# AD9600ABCPZ-105

# 10-Bit, 105 MSPS/125 MSPS/150 MSPS, 1.8 V Dual Analog-to-Digital Converter

# AD9600

## FEATURES

**SNR = 60.6 dBc (61.6 dBFS) to 70 MHz at 150 MSPS**
**SFDR = 81 dBc to 70 MHz at 150 MSPS**
**Low power: 825 mW at 150 MSPS**
**1.8 V analog supply operation**
**1.8 V to 3.3 V CMOS output supply or 1.8 V LVDS supply**
**Integer 1 to 8 input clock divider**
**Intermediate frequency (IF) sampling frequencies up to 450 MHz**
**Internal analog-to-digital converter (ADC) voltage reference**
**Integrated ADC sample-and-hold inputs**
**Flexible analog input: 1 V p-p to 2 V p-p range**
**Differential analog inputs with 650 MHz bandwidth**
**ADC clock duty cycle stabilizer**
**95 dB channel isolation/crosstalk**
**Serial port control**
**User-configurable built-in self-test (BIST) capability**
**Energy-saving power-down modes**
**Integrated receive features**
- **Fast detect/threshold bits**
- **Composite signal monitor**

## APPLICATIONS

**Point-to-point radio receivers (GPSK, QAM)**
**Diversity radio systems**
**I/Q demodulation systems**
**Smart antenna systems**
**Digital predistortion**
**General-purpose software radios**
**Broadband data applications**
**Data acquisition**
**Nondestructive testing**

## PRODUCT HIGHLIGHTS

1. Integrated dual, 10-bit, 150 MSPS/125 MSPS/105 MSPS ADC.
2. Fast overrange detect and signal monitor with serial output.
3. Signal monitor block with dedicated serial output mode.
4. Proprietary differential input maintains excellent SNR performance for input frequencies up to 450 MHz.
5. The AD9600 operates from a single 1.8 V supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
6. A standard serial port interface supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down mode, and voltage reference mode.
7. The AD9600 is pin compatible with the AD9627-11, AD9627, and AD9640, allowing a simple migration from 10 bits to 11 bits, 12 bits, or 14 bits.

## FUNCTIONAL BLOCK DIAGRAM

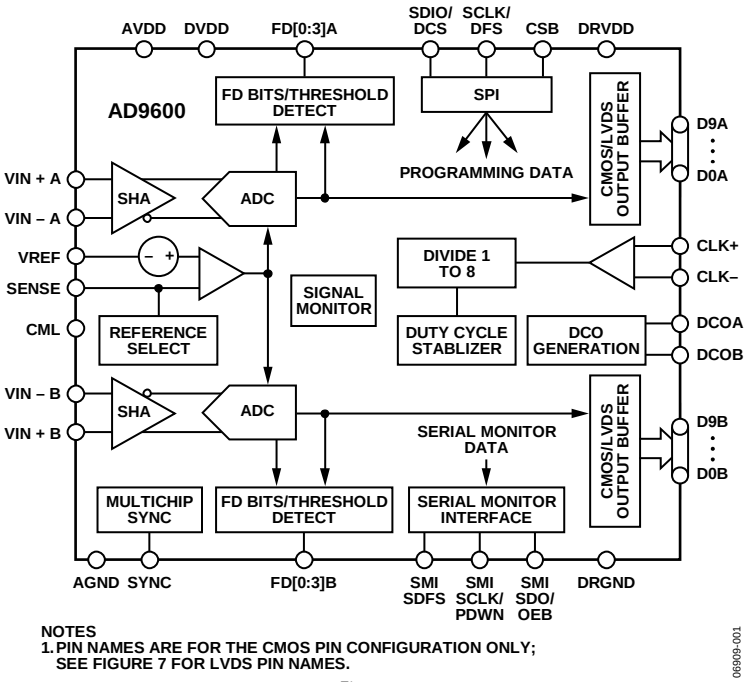


*Figure 1.*

**Rev. B**


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# GENERAL DESCRIPTION

The AD9600 is a dual, 10-bit, 105 MSPS/125 MSPS/150 MSPS ADC. It is designed to support communications applications where low cost, small size, and versatility are desired.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth, differential sample-and-hold analog input amplifiers supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The AD9600 has several functions that simplify the automated gain control (AGC) function in a communications receiver. For example, the fast detect feature allows fast overrange detection by outputting four bits of input level information with very short latency.

In addition, the programmable threshold detector allows monitoring the amplitude of the incoming signal with short latency, using the four fast detect bits of the ADC. If the input signal level exceeds the programmable threshold, the fine upper threshold indicator goes high. Because this threshold is set from the four MSBs, the user can quickly adjust the system gain to avoid an overrange condition.

Another AGC-related function of the AD9600 is the signal monitor. This block allows the user to monitor the composite magnitude of the incoming signal, which aids in setting the gain to optimize the dynamic range of the overall system.

The ADC output data can be routed directly to the two external 10-bit output ports. These outputs can be set from 1.8 V to 3.3 V CMOS or 1.8 V LVDS. In addition, flexible power-down options allow significant power savings.

# SPECIFICATIONS

## DC SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect output pins disabled, signal monitor disabled, unless otherwise noted.

**Table 1.**

| | | AD9600ABCPZ-105/ AD9600BCPZ-105 | | | AD9600ABCPZ-125/ AD9600BCPZ-125 | | | AD9600ABCPZ-150/ AD9600BCPZ-150 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Temp** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| RESOLUTION | Full | 10 | | | 10 | | | 10 | | | Bits |
| ACCURACY | | | | | | | | | | | |
| No Missing Codes | Full | | Guaranteed | | | Guaranteed | | | Guaranteed | | |
| Offset Error | Full | | ±0.3 | ±0.7 | | ±0.3 | ±0.7 | | ±0.3 | ±0.7 | % FSR |
| Gain Error | Full | −3.6 | −2.2 | −1.0 | −4.0 | −2.5 | −1.3 | −4.3 | −3.0 | −1.6 | % FSR |
| Differential Nonlinearity (DNL)[1] | Full | | | ±0.2 | | | ±0.2 | | | ±0.2 | LSB |
| | 25°C | | ±0.1 | | | ±0.1 | | | ±0.1 | | LSB |
| Integral Nonlinearity (INL)[1] | Full | | | ±0.3 | | | ±0.3 | | | ±0.4 | LSB |
| | 25°C | | ±0.1 | | | ±0.1 | | | ±0.1 | | LSB |
| MATCHING CHARACTERISTICS | | | | | | | | | | | |
| Offset Error | Full | | ±0.3 | ±0.7 | | ±0.3 | ±0.7 | | ±0.2 | ±0.7 | % FSR |
| Gain Error | Full | | ±0.2 | ±0.8 | | ±0.3 | ±0.8 | | ±0.2 | ±0.8 | % FSR |
| TEMPERATURE DRIFT | | | | | | | | | | | |
| Offset Error | Full | | ±15 | | | ±15 | | | ±15 | | ppm/°C |
| Gain Error | Full | | ±95 | | | ±95 | | | ±95 | | ppm/°C |
| INTERNAL VOLTAGE REFERENCE | | | | | | | | | | | |
| Output Voltage Error (1 V Mode) | Full | | ±5 | ±16 | | ±5 | ±16 | | ±5 | ±16 | mV |
| Load Regulation @ 1.0 mA | Full | | 7 | | | 7 | | | 7 | | mV |
| INPUT-REFERRED NOISE | | | | | | | | | | | |
| VREF = 1.0 V | 25°C | | 0.1 | | | 0.1 | | | 0.1 | | LSB rms |
| ANALOG INPUT | | | | | | | | | | | |
| Input Span, VREF = 1.0 V | Full | | 2 | | | 2 | | | 2 | | V p-p |
| Input Capacitance[2] | Full | | 8 | | | 8 | | | 8 | | pF |
| VREF INPUT RESISTANCE | Full | | 6 | | | 6 | | | 6 | | kΩ |
| POWER SUPPLIES | | | | | | | | | | | |
| Supply Voltage | | | | | | | | | | | |
| AVDD, DVDD | Full | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| DRVDD (CMOS Mode) | Full | 1.7 | 3.3 | 3.6 | 1.7 | 3.3 | 3.6 | 1.7 | 3.3 | 3.6 | V |
| Supply Current | | | | | | | | | | | |
| $I_{AVDD}$[1] | Full | | 310 | | | 385 | | | 419 | | mA |
| $I_{DVDD}$[1] | Full | | 34 | | | 42 | | | 50 | | mA |
| $I_{AVDD}$ and $I_{DVDD}$[1, 3] | | | | 365 | | | 455 | | | 495 | |
| $I_{DRVDD}$ (3.3 V CMOS) | Full | | 35 | | | 36 | | | 42 | | mA |
| $I_{DRVDD}$ (1.8 V CMOS) | Full | | 15 | | | 18 | | | 22 | | mA |
| $I_{DRVDD}$ (1.8 V LVDS) | | | 42 | | | 44 | | | 46 | | mA |
| POWER CONSUMPTION | | | | | | | | | | | |
| DC Input | Full | | 600 | 650 | | 750 | 800 | | 825 | 890 | mW |
| Sine Wave Input[1] | | | | | | | | | | | |
| DRVDD = 1.8 V | Full | | 645 | | | 813 | | | 892 | | mW |
| DRVDD = 3.3 V | Full | | 740 | | | 900 | | | 990 | | mW |
| Standby Power[3] | Full | | 68 | | | 77 | | | 77 | | mW |
| Power-Down Power | Full | | 2.5 | 6 | | 2.5 | 6 | | 2.5 | 6 | mW |

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 8 for the equivalent analog input structure.
[3] Standby power is measured with a dc input and the CLK+ and CLK− pins inactive )set to AVDD or AGND.

## AC SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect output pins disabled, signal monitor disabled, unless otherwise noted.

**Table 2.**

| | | AD9600ABCPZ-105/ AD9600BCPZ-105 | | | AD9600ABCPZ-125/ AD9600BCPZ-125 | | | AD9600ABCPZ-150/ AD9600BCPZ-150 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter[1]** | **Temp** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| SIGNAL-TO-NOISE RATIO (SNR) | | | | | | | | | | | |
| $f_{IN}$ = 2.3 MHz | 25°C | | 60.7 | | | 60.6 | | | 60.6 | | dB |
| $f_{IN}$ = 70 MHz | 25°C | | 60.6 | | | 60.6 | | | 60.6 | | dB |
| | Full | 60.3 | | | 60.3 | | | 60.3 | | | dB |
| $f_{IN}$ = 140 MHz | 25°C | | 60.6 | | | 60.6 | | | 60.5 | | dB |
| $f_{IN}$ = 220 MHz | 25°C | | 60.5 | | | 60.5 | | | 60.4 | | dB |
| SIGNAL-TO-NOISE AND DISTORTION (SINAD) | | | | | | | | | | | |
| $f_{IN}$ = 2.3 MHz | 25°C | | 60.6 | | | 60.5 | | | 60.5 | | dB |
| $f_{IN}$ = 70 MHz | 25°C | | 60.5 | | | 60.5 | | | 60.5 | | dB |
| | Full | 60.2 | | | 60.2 | | | 60.1 | | | dB |
| $f_{IN}$ = 140 MHz | 25°C | | 60.5 | | | 60.5 | | | 60.4 | | dB |
| $f_{IN}$ = 220 MHz | 25°C | | 60.4 | | | 60.4 | | | 60.3 | | dB |
| EFFECTIVE NUMBER OF BITS (ENOB) | | | | | | | | | | | |
| $f_{IN}$ = 2.3 MHz | 25°C | | 9.9 | | | 9.9 | | | 9.9 | | Bits |
| $f_{IN}$ = 70 MHz | 25°C | | 9.9 | | | 9.9 | | | 9.9 | | Bits |
| $f_{IN}$ = 140 MHz | 25°C | | 9.9 | | | 9.9 | | | 9.9 | | Bits |
| $f_{IN}$ = 220 MHz | 25°C | | 9.9 | | | 9.9 | | | 9.9 | | Bits |
| WORST SECOND OR THIRD HARMONIC | | | | | | | | | | | |
| $f_{IN}$ = 2.3 MHz | 25°C | | −87.0 | | | −86.5 | | | −88.5 | | dBc |
| $f_{IN}$ = 70 MHz | 25°C | | −85.0 | | | −85.0 | | | −84.0 | | dBc |
| | Full | | | −72.0 | | | −72.0 | | | −72.0 | dBc |
| $f_{IN}$ = 140 MHz | 25°C | | −84.0 | | | −84.0 | | | −83.5 | | dBc |
| $f_{IN}$ = 220 MHz | 25°C | | −83.0 | | | −83.0 | | | −77 | | dBc |
| SPURIOUS-FREE DYNAMIC RANGE (SFDR) | | | | | | | | | | | |
| $f_{IN}$ = 2.3 MHz | 25°C | | 85.5 | | | 85.5 | | | 85.5 | | dBc |
| $f_{IN}$ = 70 MHz | 25°C | | 85.0 | | | 85.0 | | | 84.0 | | dBc |
| | Full | 72.0 | | | 72.0 | | | 72.0 | | | dBc |
| $f_{IN}$ = 140 MHz | 25°C | | 83.0 | | | 84.0 | | | 83.5 | | dBc |
| $f_{IN}$ = 220 MHz | 25°C | | 81.0 | | | 81.0 | | | 77 | | dBc |
| WORST OTHER HARMONIC OR SPUR | | | | | | | | | | | |
| $f_{IN}$ = 2.3 MHz | 25°C | | −92 | | | −92 | | | −92 | | dBc |
| $f_{IN}$ = 70 MHz | 25°C | | −88 | | | -88 | | | −88 | | dBc |
| | Full | | | −81 | | | −81 | | | −80 | dBc |
| $f_{IN}$ = 140 MHz | 25°C | | −86 | | | −86 | | | −86 | | dBc |
| $f_{IN}$ = 220 MHz | 25°C | | −86 | | | −86 | | | −86 | | dBc |
| TWO-TONE SFDR | | | | | | | | | | | |
| $f_{IN}$ = 29.1 MHz, 32.1 MHz (−7 dBFS ) | 25°C | | 84 | | | 84 | | | 84 | | dBc |
| $f_{IN}$ = 169.1 MHz, 172.1 MHz (−7 dBFS ) | 25°C | | 82 | | | 82 | | | 82 | | dBc |
| CROSSTALK[2] | Full | | 95 | | | 95 | | | 95 | | dB |
| ANALOG INPUT BANDWIDTH | 25°C | | 650 | | | 650 | | | 650 | | MHz |

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation,* for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and no input on the alternate channel.

## DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

**Table 3.**

| Parameter | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–) | | | | | |
| Logic Compliance | | | CMOS/LVDS/LVPECL | | |
| Internal Common-Mode Bias | Full | | 1.2 | | V |
| Differential Input Voltage | Full | 0.2 | | 6 | V p-p |
| Input Voltage Range | Full | GND – 0.3 | | AVDD + 1.6 | V |
| Input Common-Mode Range | Full | 1.1 | | AVDD | V |
| High Level Input Voltage | Full | 1.2 | | 3.6 | V |
| Low Level Input Voltage | Full | 0 | | 0.8 | V |
| High Level Input Current | Full | −10 | | +10 | µA |
| Low Level Input Current | Full | −10 | | +10 | µA |
| Input Capacitance | Full | | 4 | | pF |
| Input Resistance | Full | 8 | 10 | 12 | kΩ |
| SYNC INPUT | | | | | |
| Logic Compliance | | | CMOS | | |
| Internal Bias | Full | | 1.2 | | V |
| Input Voltage Range | Full | GND – 0.3 | | AVDD + 1.6 | V |
| High Level Input Voltage | Full | 1.2 | | 3.6 | V |
| Low Level Input Voltage | Full | 0 | | 0.8 | V |
| High Level Input Current | Full | −10 | | +10 | µA |
| Low Level Input Current | Full | −10 | | +10 | µA |
| Input Capacitance | Full | | 4 | | pF |
| Input Resistance | Full | 8 | 10 | 12 | kΩ |
| LOGIC INPUT (CSB)[1] | | | | | |
| High Level Input Voltage | Full | 1.22 | | 3.6 | V |
| Low Level Input Voltage | Full | 0 | | 0.6 | V |
| High Level Input Current | Full | −10 | | +10 | µA |
| Low Level Input Current | Full | 40 | | 132 | µA |
| Input Resistance | Full | | 26 | | kΩ |
| Input Capacitance | Full | | 2 | | pF |
| LOGIC INPUT (SCLK/DFS)[2] | | | | | |
| High Level Input Voltage | Full | 1.22 | | 3.6 | V |
| Low Level Input Voltage | Full | 0 | | 0.6 | V |
| High Level Input Current (VIN = 3.3 V) | Full | −92 | | −135 | µA |
| Low Level Input Current | Full | −10 | | +10 | µA |
| Input Resistance | Full | | 26 | | kΩ |
| Input Capacitance | Full | | 2 | | pF |
| LOGIC INPUTS/OUTPUTS (SDIO/DCS, SMI SDFS)[1] | | | | | |
| High Level Input Voltage | Full | 1.22 | | 3.6 | V |
| Low Level Input Voltage | Full | 0 | | 0.6 | V |
| High Level Input Current | Full | −10 | | +10 | µA |
| Low Level Input Current | Full | 38 | | 128 | µA |
| Input Resistance | Full | | 26 | | kΩ |
| Input Capacitance | Full | | 5 | | pF |

| Parameter | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LOGIC INPUTS/OUTPUTS (SMI SDO/OEB, SMI SCLK/PDWN)[2] | | | | | |
| High Level Input Voltage | Full | 1.22 | | 3.6 | V |
| Low Level Input Voltage | Full | 0 | | 0.6 | V |
| High Level Input Current (VIN = 3.3 V) | Full | −90 | | −134 | µA |
| Low Level Input Current | Full | −10 | | +10 | µA |
| Input Resistance | Full | | 26 | | kΩ |
| Input Capacitance | Full | | 5 | | pF |
| DIGITAL OUTPUTS | | | | | |
| CMOS Mode—DRVDD = 3.3 V | | | | | |
| High Level Output Voltage ($I_{OH}$ = 50 µA) | Full | 3.29 | | | V |
| High Level Output Voltage ($I_{OH}$ = 0.5 mA) | Full | 3.25 | | | V |
| Low Level Output Voltage ($I_{OL}$ = 1.6 mA) | Full | | | 0.2 | V |
| Low Level Output Voltage ($I_{OL}$ = 50 µA) | Full | | | 0.05 | V |
| CMOS Mode—DRVDD = 1.8 V | | | | | |
| High Level Output Voltage ($I_{OH}$ = 50 µA) | Full | 1.79 | | | V |
| High Level Output Voltage ($I_{OH}$ = 0.5 mA) | Full | 1.75 | | | V |
| Low Level Output Voltage ($I_{OL}$ = 1.6 mA) | Full | | | 0.2 | V |
| Low Level Output Voltage ($I_{OL}$ = 50 µA) | Full | | | 0.05 | V |
| LVDS Mode—DRVDD = 1.8 V | | | | | |
| Differential Output Voltage ($V_{OD}$), ANSI Mode | Full | 250 | 350 | 450 | mV |
| Output Offset Voltage ($V_{OS}$), ANSI Mode | Full | 1.15 | 1.25 | 1.35 | V |
| Differential Output Voltage ($V_{OD}$), Reduced Swing Mode | Full | 150 | 200 | 280 | mV |
| Output Offset Voltage ($V_{OS}$), Reduced Swing Mode | Full | 1.15 | 1.25 | 1.35 | V |

[1] Pull up.
[2] Pull down.

## SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

**Table 4.**

| Parameter | Temp | AD9600ABCPZ-105/ AD9600BCPZ-105 | | | AD9600ABCPZ-125/ AD9600BCPZ-125 | | | AD9600ABCPZ-150/ AD9600BCPZ-150 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| CLOCK INPUT PARAMETERS | | | | | | | | | | | |
| Input Clock Rate | Full | | | 625 | | | 625 | | | 625 | MHz |
| Conversion Rate | | | | | | | | | | | |
| DCS Enabled | Full | 20 | | 105 | 20 | | 125 | 20 | | 150 | MSPS |
| DCS Disabled | Full | 10 | | 105 | 10 | | 125 | 10 | | 150 | MSPS |
| CLK Period ($t_{CLK}$) | Full | 9.5 | | | 8 | | | 6.66 | | | ns |
| CLK Pulse Width High | | | | | | | | | | | |
| Divide-by-1 Mode, DCS Enabled | Full | 2.85 | 4.75 | 6.65 | 2.4 | 4 | 5.6 | 2.0 | 3.33 | 4.66 | ns |
| Divide-by-1 Mode, DCS Disabled | Full | 4.28 | 4.75 | 5.23 | 3.6 | 4 | 4.4 | 3.0 | 3.33 | 3.66 | ns |
| Divide-by-2 Mode, DCS Enabled | Full | 1.6 | | | 1.6 | | | 1.6 | | | ns |
| Divide-by-3 Through Divide-by-8 Modes, DCS Enabled | Full | 0.8 | | | 0.8 | | | 0.8 | | | ns |
| DATA OUTPUT PARAMETERS | | | | | | | | | | | |
| CMOS Mode—DRVDD = 3.3 V | | | | | | | | | | | |
| Data Propagation Delay ($t_{PD}$)[1] | Full | 2.2 | 4.5 | 6.4 | 2.2 | 4.5 | 6.4 | 2.2 | 4.5 | 6.4 | ns |
| DCO Propagation Delay ($t_{DCO}$) | Full | 3.8 | 5.0 | 6.8 | 3.8 | 5.0 | 6.8 | 3.8 | 5.0 | 6.8 | ns |
| Setup Time ($t_S$) | Full | | 5.25 | | | 4.5 | | | 3.83 | | ns |
| Hold Time ($t_H$) | Full | | 4.25 | | | 3.5 | | | 2.83 | | ns |
| CMOS Mode—DRVDD = 1.8 V | | | | | | | | | | | |
| Data Propagation Delay ($t_{PD}$)[1] | Full | 2.4 | 5.2 | 6.9 | 2.4 | 5.2 | 6.9 | 2.4 | 5.2 | 6.9 | ns |
| DCO Propagation Delay ($t_{DCO}$) | Full | 4.0 | 5.6 | 7.3 | 4.0 | 5.6 | 7.3 | 4.0 | 5.6 | 7.3 | ns |
| Setup Time ($t_S$) | Full | | 5.25 | | | 4.5 | | | 3.83 | | ns |
| Hold Time ($t_H$) | Full | | 4.25 | | | 3.5 | | | 2.83 | | ns |
| LVDS Mode—DRVDD = 1.8 V | | | | | | | | | | | |
| Data Propagation Delay ($t_{PD}$)[1] | Full | 3.0 | 3.7 | 4.4 | 3.0 | 3.8 | 4.5 | 3.0 | 3.8 | 4.5 | ns |
| DCO Propagation Delay ($t_{DCO}$) | Full | 5.2 | 6.4 | 7.6 | 5.0 | 6.2 | 7.4 | 4.8 | 5.9 | 7.3 | ns |
| CMOS Mode Pipeline Delay (Latency) | Full | | 12 | | | 12 | | | 12 | | Cycles |
| LVDS Mode Pipeline Delay (Latency) Channel A/Channel B | Full | | 12/12.5 | | | 12/12.5 | | | 12/12.5 | | Cycles |
| Aperture Delay ($t_A$) | Full | | 1.0 | | | 1.0 | | | 1.0 | | ns |
| Aperture Uncertainty (Jitter, $t_J$) | Full | | 0.1 | | | 0.1 | | | 0.1 | | ps rms |
| Wake-Up Time[2] | Full | | 350 | | | 350 | | | 350 | | µs |
| OUT-OF-RANGE RECOVERY TIME | Full | | 2 | | | 3 | | | 3 | | Cycles |

[1] Output propagation delay is measured from the CLK+ and CLK− pins 50% transition to the output data pins 50% transition, with 5 pF load.
[2] Wake-up time is dependent on the value of the decoupling capacitors.

## TIMING CHARACTERISTICS

**Table 5.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SYNC TIMING REQUIREMENTS | | | | | |
| $t_{SSYNC}$ | Setup time between SYNC and the rising edge of CLK+ | | 0.24 | | ns |
| $t_{HSYNC}$ | Hold time between SYNC and the rising edge of CLK+ | | 0.40 | | ns |
| SPI TIMING REQUIREMENTS | | | | | |
| $t_{DS}$ | Setup time between the data and the rising edge of SCLK | 2 | | | ns |
| $t_{DH}$ | Hold time between the data and the rising edge of SCLK | 2 | | | ns |
| $t_{CLK}$ | Period of the SCLK | 40 | | | ns |
| $t_S$ | Setup time between CSB and SCLK | 2 | | | ns |
| $t_H$ | Hold time between CSB and SCLK | 2 | | | ns |
| $t_{HIGH}$ | SCLK pulse width high | 10 | | | ns |
| $t_{LOW}$ | SCLK pulse width low | 10 | | | ns |
| $t_{EN\_SDIO}$ | Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge | 10 | | | ns |
| $t_{DIS\_SDIO}$ | Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge | 10 | | | ns |
| SPORT TIMING REQUIREMENTS | | | | | |
| $t_{CSSCLK}$ | Delay from the rising edge of CLK+ to the rising edge of SMI SCLK | 3.2 | 4.5 | 6.2 | ns |
| $t_{SSCLKSDO}$ | Delay from the rising edge of SMI SCLK to SMI SDO | −0.4 | 0 | 0.4 | ns |
| $t_{SSCLKSDFS}$ | Delay from the rising edge of SMI SCLK to SMI SDFS | −0.4 | 0 | 0.4 | ns |

## TIMING DIAGRAMS

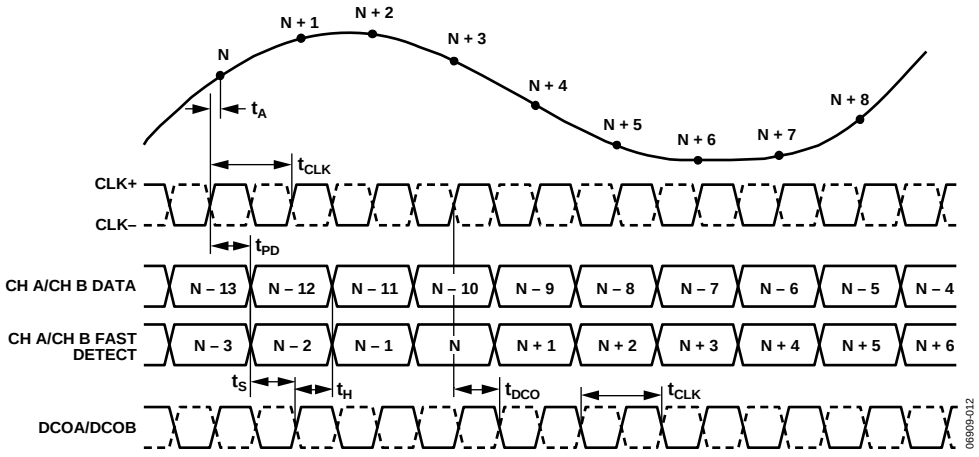



*Figure 2. CMOS Output Mode Data and Fast Detect Output Timing*

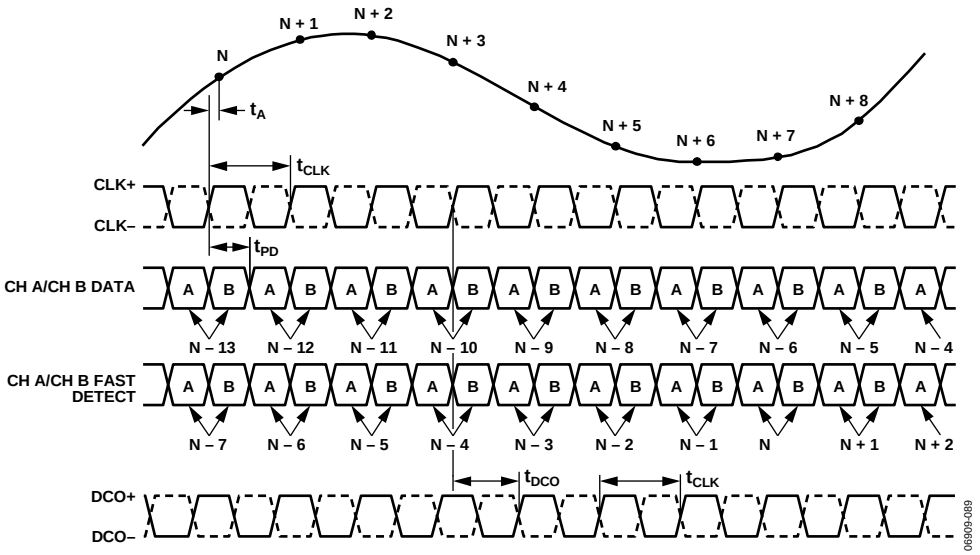



*Figure 3. LVDS Mode Data and Fast Detect Output Timing (Fast Detect Mode Select Bits = 000)*

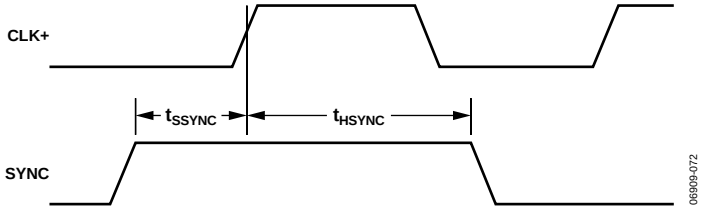



*Figure 4. SYNC Input Timing Requirements*

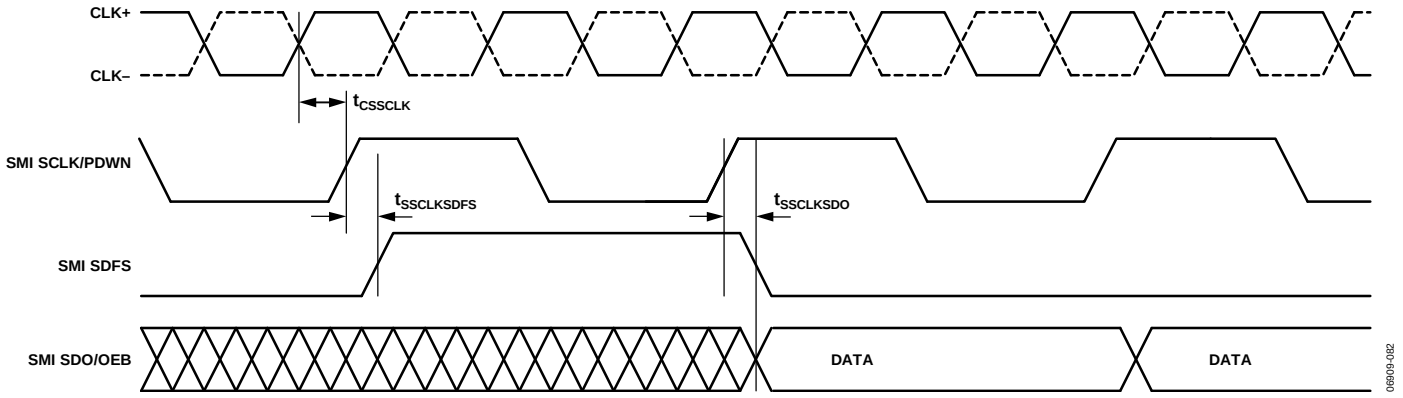



*Figure 5. Signal Monitor SPORT Output Timing (Divide-by-2 Mode)*

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Rating |
|---|---|
| ELECTRICAL | |
| AVDD, DVDD to AGND | −0.3 V to +2.0 V |
| DRVDD to DRGND | −0.3 V to +3.9 V |
| AGND to DRGND | −0.3 V to +0.3 V |
| AVDD to DRVDD | −3.9 V to +2.0 V |
| VIN + A/VIN + B, VIN − A/VIN − B to AGND | −0.3 V to AVDD + 0.2 V |
| CLK+, CLK− to AGND | −0.3 V to +3.9 V |
| SYNC to AGND | −0.3 V to +3.9 V |
| VREF to AGND | −0.3 V to AVDD + 0.2 V |
| SENSE to AGND | −0.3 V to AVDD + 0.2 V |
| CML to AGND | −0.3 V to AVDD + 0.2 V |
| RBIAS to AGND | −0.3 V to AVDD + 0.2 V |
| CSB to AGND | −0.3 V to +3.9 V |
| SCLK/DFS to DRGND | −0.3 V to +3.9 V |
| SDIO/DCS to DRGND | −0.3 V to DRVDD + 0.3 V |
| SMI SDO/OEB | −0.3 V to DRVDD + 0.3 V |
| SMI SCLK/PDWN | −0.3 V to DRVDD + 0.3 V |
| SMI SDFS | −0.3 V to DRVDD + 0.3 V |
| Output Data Pins to DRGND[1] | −0.3 V to DRVDD + 0.3 V |
| Fast Detect Output Pins to DRGND[2] | −0.3 V to DRVDD + 0.3 V |
| Data Clock Output Pins to DRGND[3] | −0.3 V to DRVDD + 0.3 V |
| ENVIRONMENTAL | |
| Operating Temperature Range (Ambient) | −40°C to +85°C |
| Maximum Junction Temperature Under Bias | 150°C |
| Storage Temperature Range (Ambient) | −65°C to +150°C |

[1] The output data pins are D0A/D0B to D9A/D9B for the CMOS configuration and D0+/D0− to D9+/D9− for the LVDS configuration.
[2] The fast detect output pins are FD0A/FD0B to FD3A/FD3B for the CMOS configuration and FD0+/FD0− to FD3+/FD3−.
[3] The data clock output pins are DCOA and DCOB for the CMOS configuration and DCO+ and DCO− for the LVDS configuration.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

**Table 7. Thermal Resistance**

| Package Type | Airflow Velocity (m/s) | $\theta_{JA}$[1, 2] | $\theta_{JC}$[1, 3] | $\theta_{JB}$[1, 4] | Unit |
|---|---|---|---|---|---|
| 64-Lead, 9 mm × 9 mm LFCSP (CP-64-3, CP-64-6) | 0 | 18.8 | 0.6 | 6.0 | °C/W |
| | 1.0 | 16.5 | | | °C/W |
| | 2.0 | 15.8 | | | °C/W |

[1] Per JEDEC 51-7 standard and JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical $\theta_{JA}$ and $\theta_{JC}$ are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing $\theta_{JA}$. In addition, metal (such as metal traces through holes, ground, and power planes) that is in direct contact with the package leads reduces the $\theta_{JA}$.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

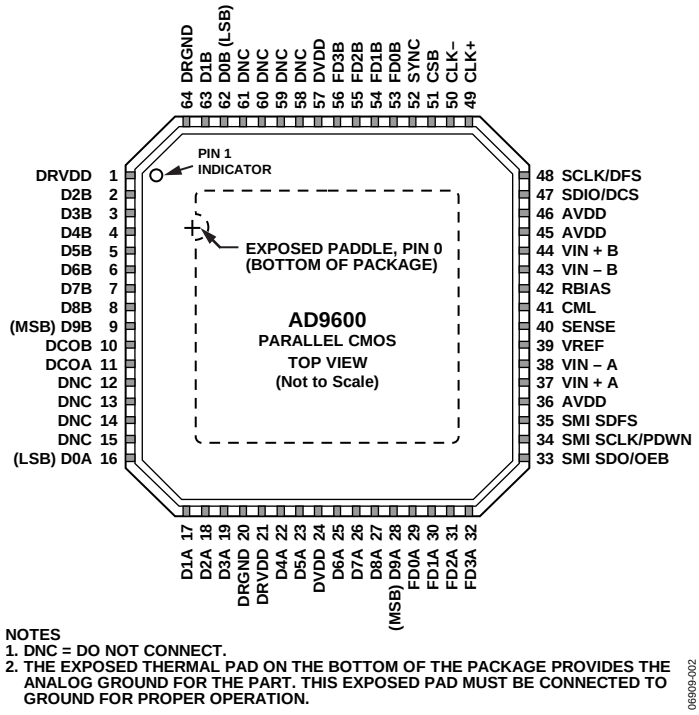



*Figure 6. Parallel CMOS Mode Pin Configuration (Top View)*

**Table 8. Parallel CMOS Mode Pin Function Descriptions**

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| ADC Power Supplies | | | |
| 20, 64 | DRGND | Ground | Digital Output Ground. |
| 1, 21 | DRVDD | Supply | Digital Output Driver Supply (1.8 V to 3.3 V). |
| 24, 57 | DVDD | Supply | Digital Power Supply (1.8 V Nominal). |
| 36, 45, 46 | AVDD | Supply | Analog Power Supply (1.8 V Nominal). |
| 0 | AGND | Ground | Analog Ground. Pin 0 is the exposed thermal pad on the bottom of the package. |
| ADC Inputs | | | |
| 37 | VIN + A | Input | Differential Analog Input Pin (+) for Channel A. |
| 38 | VIN − A | Input | Differential Analog Input Pin (−) for Channel A. |
| 44 | VIN + B | Input | Differential Analog Input Pin (+) for Channel B. |
| 43 | VIN − B | Input | Differential Analog Input Pin (−) for Channel B. |
| 39 | VREF | I/O | Voltage Reference Input/Output. |
| 40 | SENSE | Input | Voltage Reference Mode Select (see Table 11 for details). |
| 42 | RBIAS | Input | External Reference Bias Resistor. |
| 41 | CML | Output | Common-Mode Level Bias Output for Analog Inputs. |
| 49 | CLK+ | Input | ADC Master Clock True. The ADC clock can be driven using a single-ended CMOS (see Figure 60 and Figure 61 for the recommended connection). |
| 50 | CLK− | Input | ADC Master Clock Complement. The ADC clock can be driven using a single-ended CMOS (see Figure 60 and Figure 61 for the recommended connection). |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| ADC Fast Detect Outputs | | | |
| 29 | FD0A | Output | Channel A Fast Detect Indicator (see Table 14 for details). |
| 30 | FD1A | Output | Channel A Fast Detect Indicator (see Table 14 for details). |
| 31 | FD2A | Output | Channel A Fast Detect Indicator (see Table 14 for details). |
| 32 | FD3A | Output | Channel A Fast Detect Indicator (see Table 14 for details). |
| 53 | FD0B | Output | Channel B Fast Detect Indicator (see Table 14 for details). |
| 54 | FD1B | Output | Channel B Fast Detect Indicator (see Table 14 for details). |
| 55 | FD2B | Output | Channel B Fast Detect Indicator (see Table 14 for details). |
| 56 | FD3B | Output | Channel B Fast Detect Indicator (see Table 14 for details). |
| Digital Inputs | | | |
| 52 | SYNC | Input | Digital Synchronization Pin (Slave Mode Only). |
| Digital Outputs | | | |
| 16 to 19, 22, 23, 25 to 28 | D0A to D9A | Output | Channel A CMOS Output Data. |
| 62, 63, 2 to 9 | D0B to D9B | Output | Channel B CMOS Output Data. |
| 11 | DCOA | Output | Channel A Data Clock Output. |
| 10 | DCOB | Output | Channel B Data Clock Output. |
| SPI Control | | | |
| 48 | SCLK/DFS | Input | SPI Serial Clock/Data Format Select Pin in External Pin Mode. |
| 47 | SDIO/DCS | I/O | SPI Serial Data Input and Output/Duty Cycle Stabilizer in External Pin Mode. |
| 51 | CSB | Input | SPI Chip Select (Active Low). |
| Signal Monitor Port | | | |
| 33 | SMI SDO/OEB | I/O | Signal Monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode. |
| 35 | SMI SDFS | Output | Signal Monitor Serial Data Frame Sync. |
| 34 | SMI SCLK/PDWN | I/O | Signal Monitor Serial Clock Output/Power-Down Input in External Pin Mode. |
| Do Not Connect | | | |
| 12 to 15, 58 to 61 | DNC | N/A | Do Not Connect. |

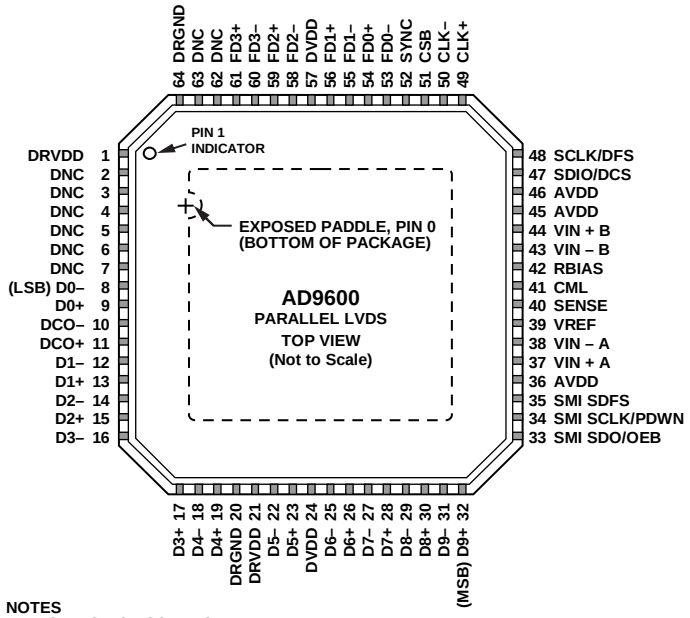



*Figure 7. Interleaved Parallel LVDS Mode Pin Configuration (Top View)*

**Table 9. Interleaved Parallel LVDS Mode Pin Function Descriptions**

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| ADC Power Supplies | | | |
| 20, 64 | DRGND | Ground | Digital Output Ground. |
| 1, 21 | DRVDD | Supply | Digital Output Driver Supply (1.8 V to 3.3 V). |
| 24, 57 | DVDD | Supply | Digital Power Supply (1.8 V Nominal). |
| 36, 45, 46 | AVDD | Supply | Analog Power Supply (1.8 V Nominal). |
| 0 | AGND | Ground | Analog Ground. Pin 0 is the exposed thermal pad on the bottom of the package. |
| ADC Inputs | | | |
| 37 | VIN + A | Input | Differential Analog Input Pin (+) for Channel A. |
| 38 | VIN − A | Input | Differential Analog Input Pin (−) for Channel A. |
| 44 | VIN + B | Input | Differential Analog Input Pin (+) for Channel B. |
| 43 | VIN − B | Input | Differential Analog Input Pin (−) for Channel B. |
| 39 | VREF | I/O | Voltage Reference Input/Output. |
| 40 | SENSE | Input | Voltage Reference Mode Select (see Table 11 for details). |
| 42 | RBIAS | Input | External Reference Bias Resistor. |
| 41 | CML | Output | Common-Mode Level Bias Output for Analog Inputs. |
| 49 | CLK+ | Input | ADC Master Clock True. The ADC clock can be driven using a single-ended CMOS (see Figure 60 and Figure 61 for the recommended connection). |
| 50 | CLK− | Input | ADC Master Clock Complement. The ADC clock can be driven using a single-ended CMOS (see Figure 60 and Figure 61 for the recommended connection). |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| ADC Fast Detect Outputs | | | |
| 54 | FD0+ | Output | Channel A/Channel B LVDS Fast Detect Indicator 0 True (see Table 14 for full details). |
| 53 | FD0− | Output | Channel A/Channel B LVDS Fast Detect Indicator 0 Complement (see Table 14 for details). |
| 56 | FD1+ | Output | Channel A/Channel B LVDS Fast Detect Indicator 1 True (see Table 14 for details). |
| 55 | FD1− | Output | Channel A/Channel B LVDS Fast Detect Indicator 1 Complement (see Table 14 for details). |
| 59 | FD2+ | Output | Channel A/Channel B LVDS Fast Detect Indicator 2 True (see Table 14 for details). |
| 58 | FD2− | Output | Channel A/Channel B LVDS Fast Detect Indicator 2 Complement (see Table 14 for details). |
| 61 | FD3+ | Output | Channel A/Channel B LVDS Fast Detect Indicator 3 True (see Table 14 for details). |
| 60 | FD3− | Output | Channel A/Channel B LVDS Fast Detect Indicator 3 Complement (see Table 14 for details). |
| Digital Inputs | | | |
| 52 | SYNC | Input | Digital Synchronization Pin (Slave Mode Only). |
| Digital Outputs | | | |
| 9 | D0+ | Output | Channel A/Channel B LVDS Output Data 0 True. |
| 8 | D0− | Output | Channel A/Channel B LVDS Output Data 0 Complement. |
| 13 | D1+ | Output | Channel A/Channel B LVDS Output Data 1 True. |
| 12 | D1− | Output | Channel A/Channel B LVDS Output Data 1 Complement. |
| 15 | D2+ | Output | Channel A/Channel B LVDS Output Data 2 True. |
| 14 | D2− | Output | Channel A/Channel B LVDS Output Data 2 Complement. |
| 17 | D3+ | Output | Channel A/Channel B LVDS Output Data 3 True. |
| 16 | D3− | Output | Channel A/Channel B LVDS Output Data 3 Complement. |
| 19 | D4+ | Output | Channel A/Channel B LVDS Output Data 4 True. |
| 18 | D4− | Output | Channel A/Channel B LVDS Output Data 4 Complement. |
| 23 | D5+ | Output | Channel A/Channel B LVDS Output Data 5 True. |
| 22 | D5− | Output | Channel A/Channel B LVDS Output Data 5 Complement. |
| 26 | D6+ | Output | Channel A/Channel B LVDS Output Data 6 True. |
| 25 | D6− | Output | Channel A/Channel B LVDS Output Data 6 Complement. |
| 28 | D7+ | Output | Channel A/Channel B LVDS Output Data 7 True. |
| 27 | D7− | Output | Channel A/Channel B LVDS Output Data 7 Complement. |
| 30 | D8+ | Output | Channel A/Channel B LVDS Output Data 8 True. |
| 29 | D8− | Output | Channel A/Channel B LVDS Output Data 8 Complement. |
| 32 | D9+ | Output | Channel A/Channel B LVDS Output Data 9 True. |
| 31 | D9− | Output | Channel A/Channel B LVDS Output Data 9 Complement. |
| 11 | DCO+ | Output | Channel A/Channel B LVDS Data Clock Output True. |
| 10 | DCO− | Output | Channel A/Channel B LVDS Data Clock Output Complement. |
| SPI Control | | | |
| 48 | SCLK/DFS | Input | SPI Serial Clock/Data Format Select Pin in External Pin Mode. |
| 47 | SDIO/DCS | I/O | SPI Serial Data Input and Output/Duty Cycle Stabilizer in External Pin Mode. |
| 51 | CSB | Input | SPI Chip Select (Active Low). |
| Signal Monitor Port | | | |
| 33 | SMI SDO/OEB | I/O | Signal Monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode. |
| 35 | SMI SDFS | Output | Signal Monitor Serial Data Frame Sync. |
| 34 | SMI SCLK/PDWN | I/O | Signal Monitor Serial Clock Output/Power-Down Input in External Pin Mode. |
| Do Not Connect | | | |
| 2 to 7, 62, 63 | DNC | N/A | Do Not Connect. |

# EQUIVALENT CIRCUITS

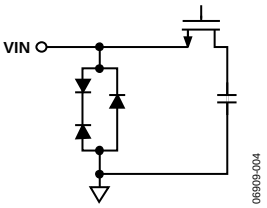



Figure 8. Analog Input Circuit

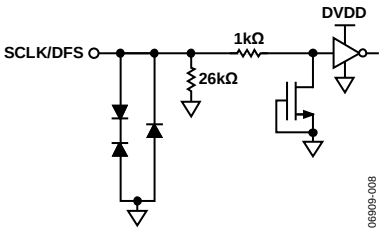



Figure 12. Equivalent SCLK/DFS Input Circuit

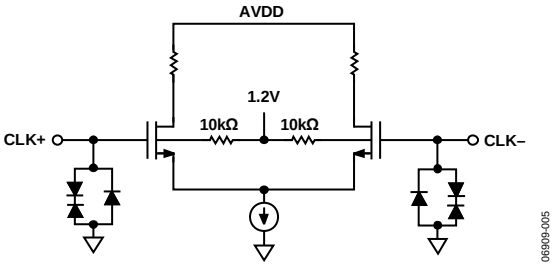



Figure 9. Equivalent Clock Input Circuit

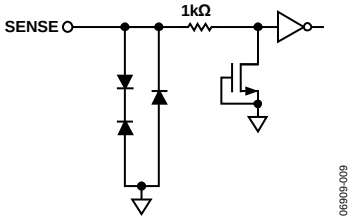



Figure 13. Equivalent SENSE Circuit

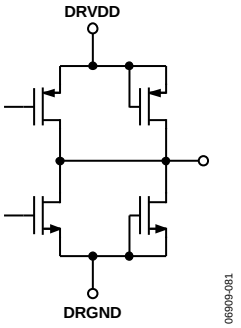



Figure 10. Digital Output

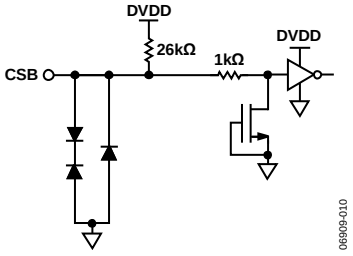



Figure 14. Equivalent CSB Input Circuit

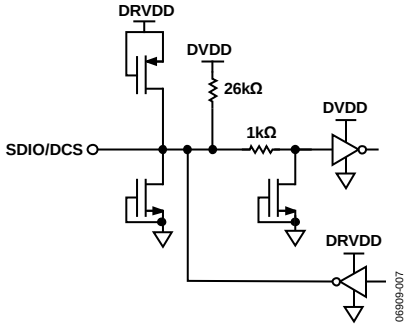



Figure 11. Equivalent SDIO/DCS Input Circuit

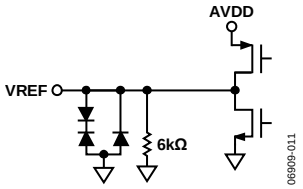



Figure 15. Equivalent VREF Circuit

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, sample rate = 150 MSPS, DCS enabled, 1 V internal reference, 2 V p-p differential input, VIN = −1.0 dBFS, 64k sample, and $T_A$ = 25°C, unless otherwise noted.

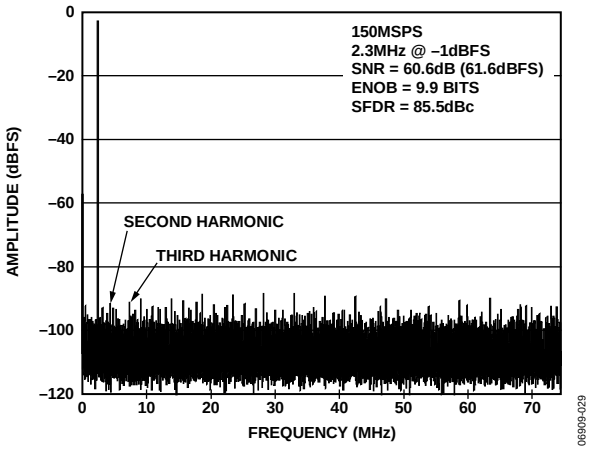



Figure 16. AD9600-150 Single-Tone FFT with $f_{IN}$ = 2.3 MHz

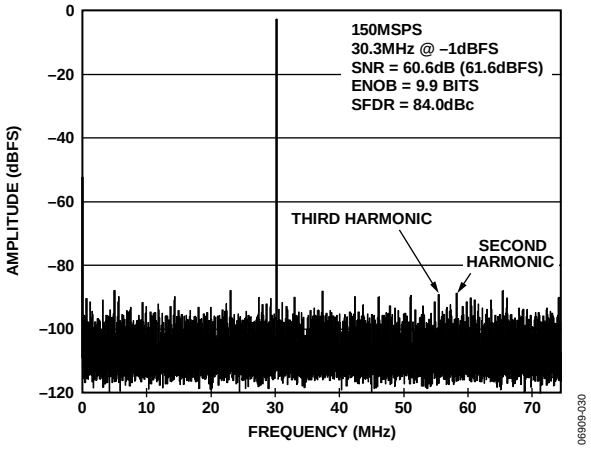



Figure 17. AD9600-150 Single-Tone FFT with $f_{IN}$ = 30.3 MHz

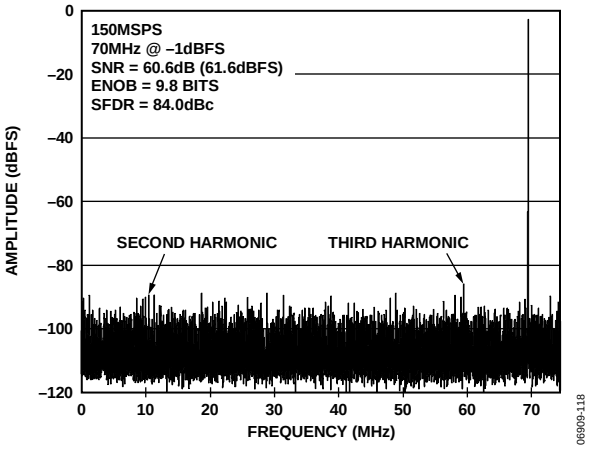



Figure 18. AD9600-150 Single-Tone FFT with $f_{IN}$ = 70 MHz

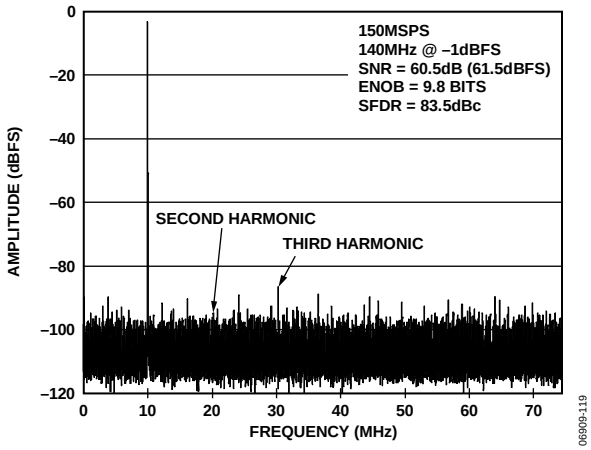



Figure 19. AD9600-150 Single-Tone FFT with $f_{IN}$ = 140 MHz

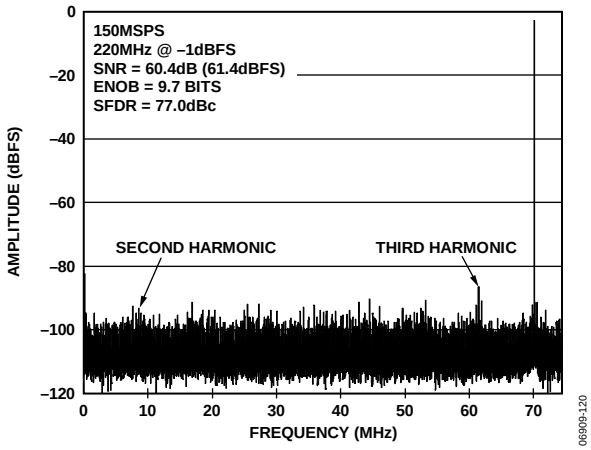



Figure 20. AD9600-150 Single-Tone FFT with $f_{IN}$ = 220 MHz

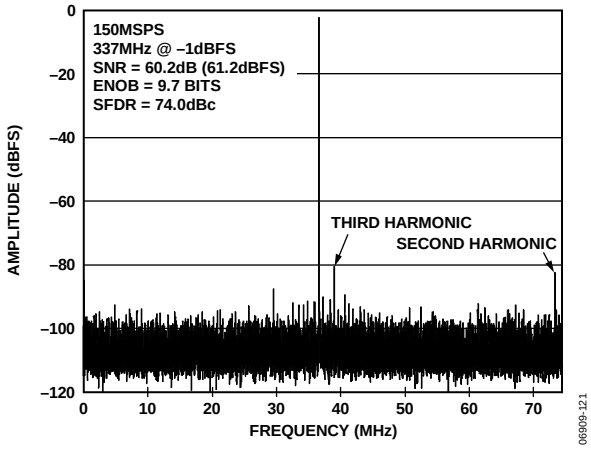



Figure 21. AD9600-150 Single-Tone FFT with $f_{IN}$ = 337 MHz

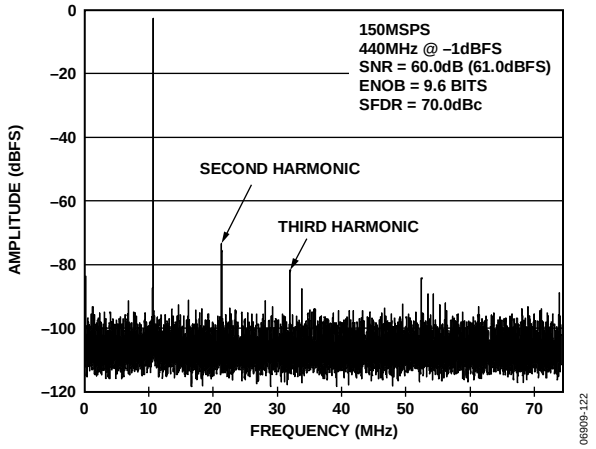



Figure 22. AD9600-150 Single-Tone FFT with $f_{IN}$ = 440 MHz

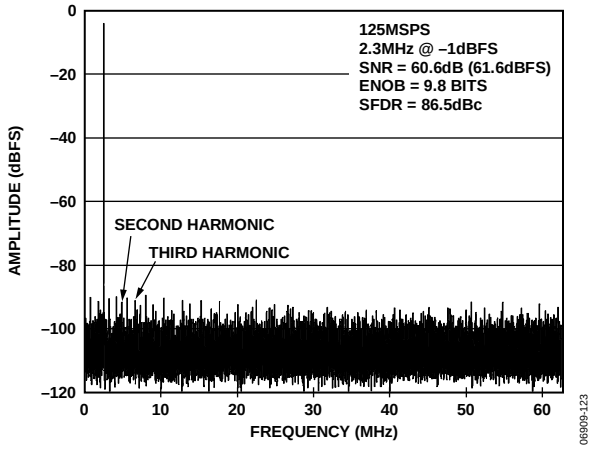



Figure 23. AD9600-125 Single-Tone FFT with $f_{IN}$ = 2.3 MHz

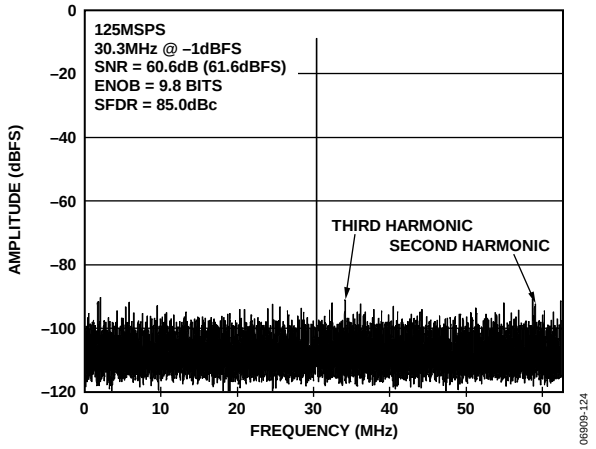



Figure 24. AD9600-125 Single-Tone FFT with $f_{IN}$ = 30.3 MHz

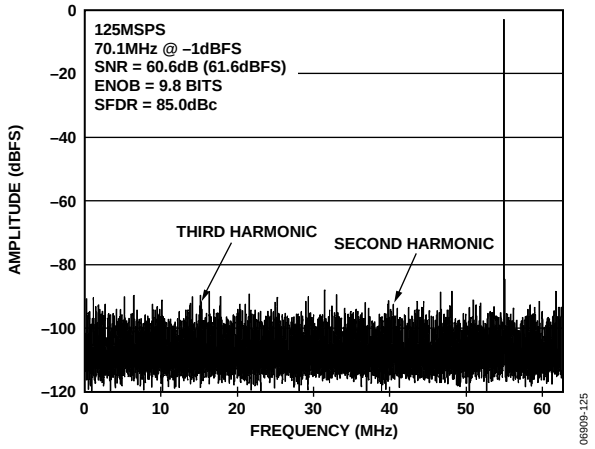



Figure 25. AD9600-125 Single-Tone FFT with $f_{IN}$ = 70.1 MHz

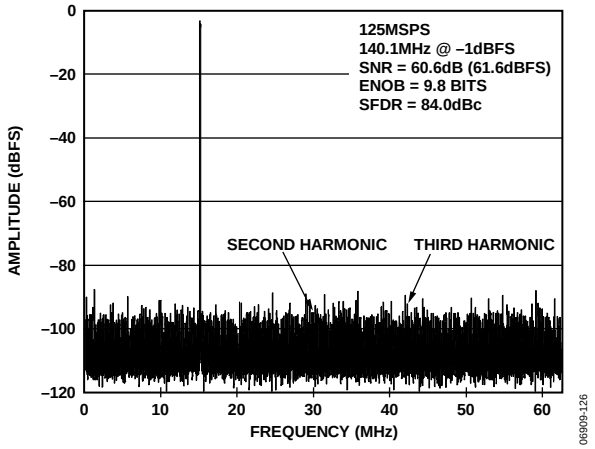



Figure 26. AD9600-125 Single-Tone FFT with $f_{IN}$ = 140.1 MHz

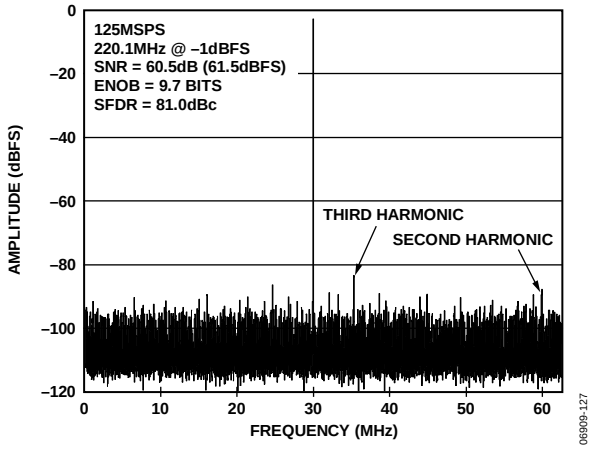



Figure 27. AD9600-125 Single-Tone FFT with $f_{IN}$ = 220.1 MHz

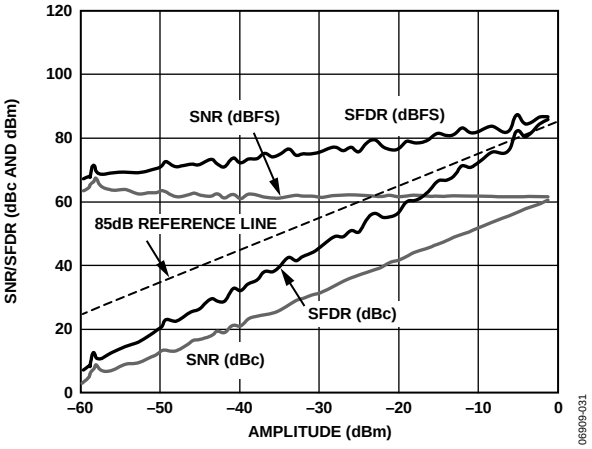



Figure 28. AD9600-150 Single-Tone SNR/SFDR vs. Input Amplitude ($A_{IN}$) with $f_{IN}$ = 2.4 MHz

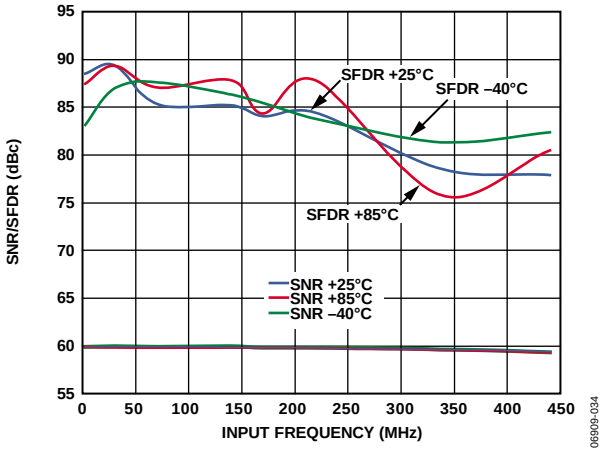



Figure 31. AD9600-150 Single-Tone SNR/SFDR vs. Input Frequency ($f_{IN}$) and Temperature with12 V p-p Full Scale

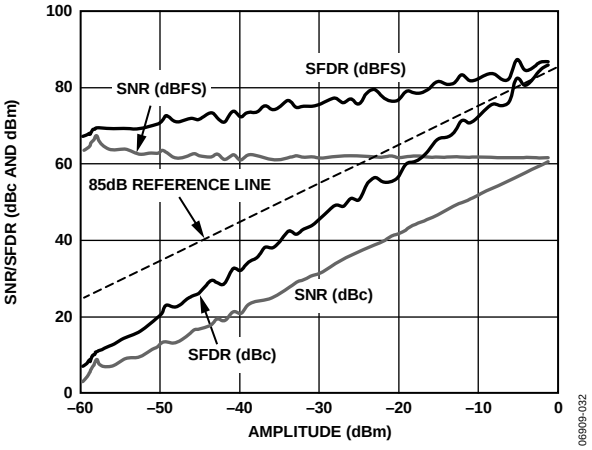



Figure 29. AD9600-150 Single-Tone SNR/SFDR vs. Input Amplitude ($A_{IN}$) with $f_{IN}$ = 98.12 MHz

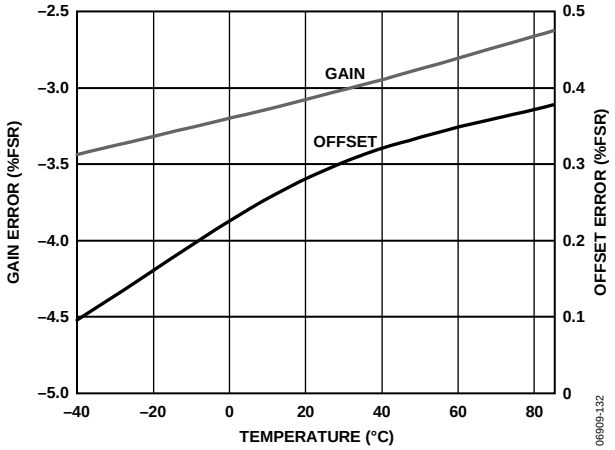



Figure 32. AD9600-150 Gain and Offset vs. Temperature

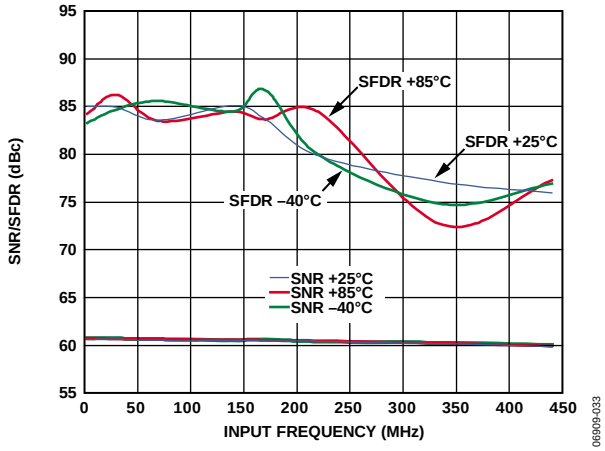



Figure 30. AD9600-150 Single-Tone SNR/SFDR vs. Input Frequency ($f_{IN}$) and Temperature with 2 V p-p Full Scale

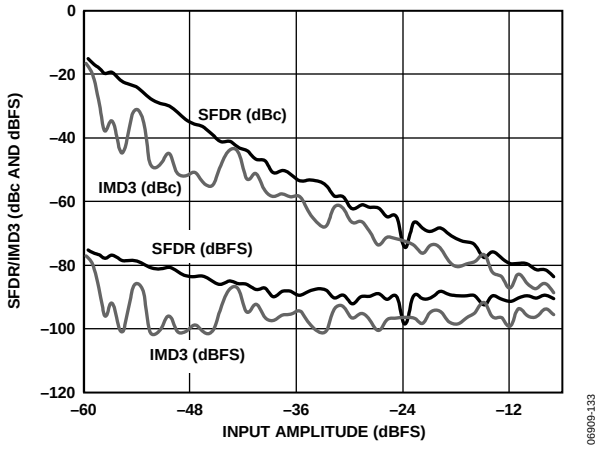



Figure 33. AD9600-150 Two-Tone SFDR/IMD3 vs. Input Amplitude ($A_{IN}$) with $f_{IN1}$ = 29.1 MHz, $f_{IN2}$ = 32.1 MHz, $f_S$ = 150 MSPS

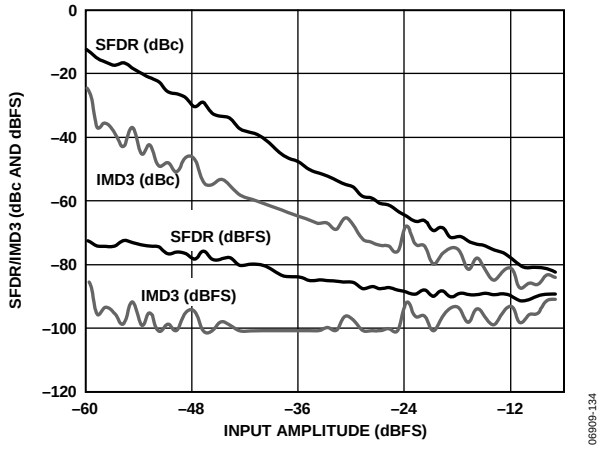



Figure 34. AD9600-150 Two-Tone SFDR/IMD3 vs. Input Amplitude ($A_{IN}$) with $f_{IN1}$ = 169.1 MHz, $f_{IN2}$ = 172.1 MHz, $f_S$ = 150 MSPS

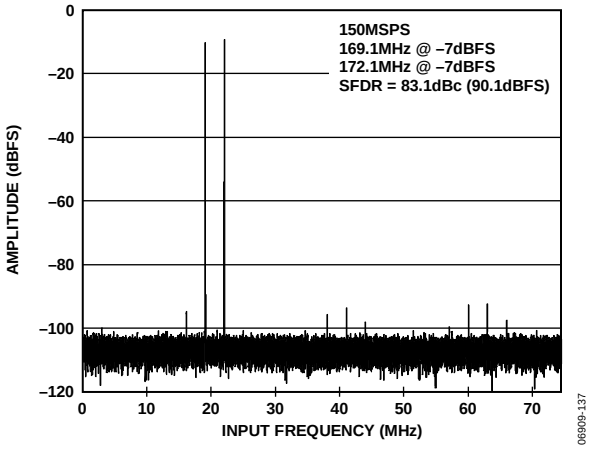



Figure 37. AD9600-150 Two-Tone SFDR/IMD3 vs. Input Frequency ($f_{IN}$) with $f_{IN1}$ = 169.1 MHz, $f_{IN2}$ = 172.1 MHz, $f_S$ = 150 MSPS

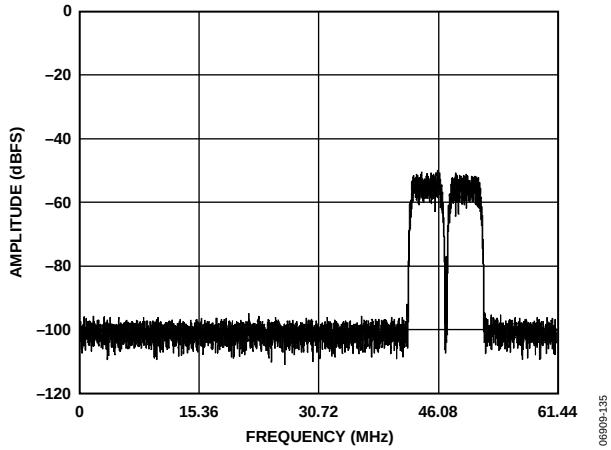



Figure 35. AD9600-125 Two 64k WCDMA Carriers with $f_{IN}$ = 170 MHz, $f_S$ = 125 MSPS

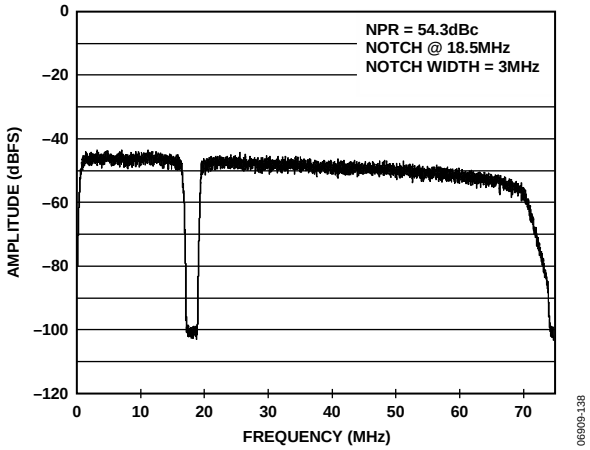



Figure 38. AD9600-150 Noise Power Ratio (NPR)

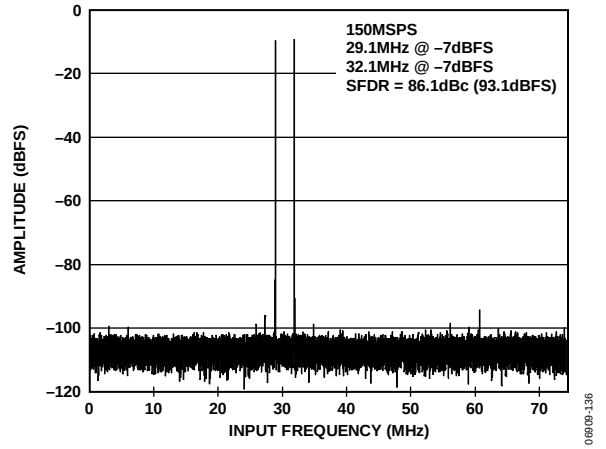



Figure 36. AD9600-150 Two-Tone SFDR/IMD3 vs. Input Frequency ($f_{IN}$) with $f_{IN1}$ = 29.1 MHz, $f_{IN2}$ = 32.1 MHz, $f_S$ = 150 MSPS

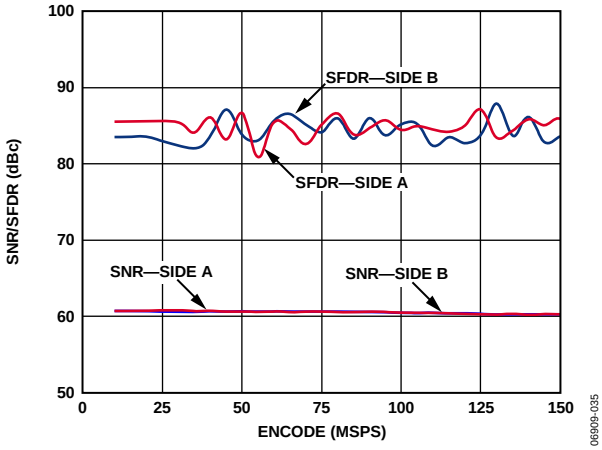



Figure 39. AD9600-150 Single-Tone SNR/SFDR vs. Clock Frequency ($f_S$) with $f_{IN1}$ = 2.3 MHz

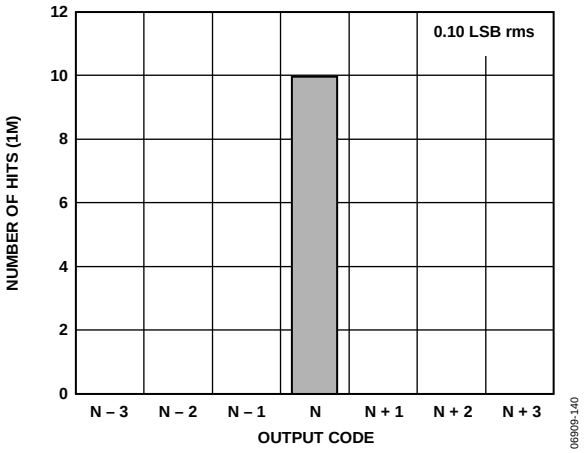



Figure 40. AD9600 Grounded Input Histogram

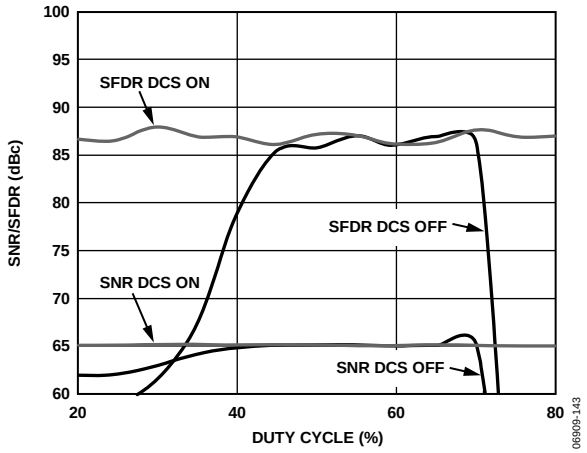



Figure 43. AD9600-150 SNR/SFDR vs. Duty Cycle with $f_{IN1}$ = 10.3 MHz

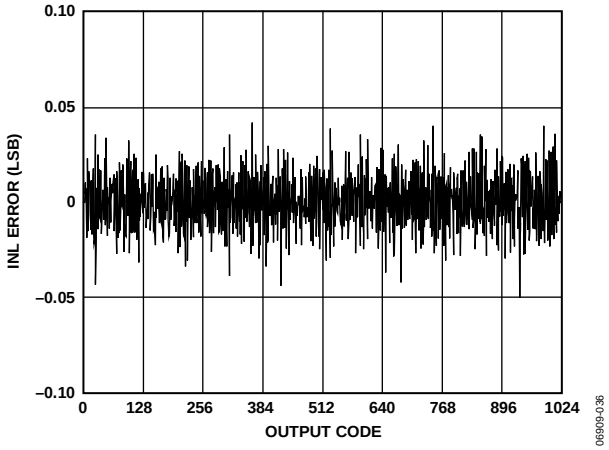



Figure 41. AD9600 INL with $f_{IN1}$ = 10.3 MHz

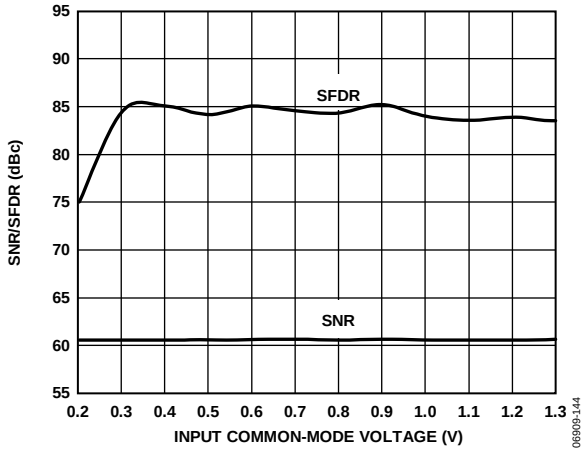



Figure 44. AD9600-150 SNR/SFDR vs. Input Common-Mode Voltage ($V_{CM}$) with $f_{IN1}$ = 30 MHz

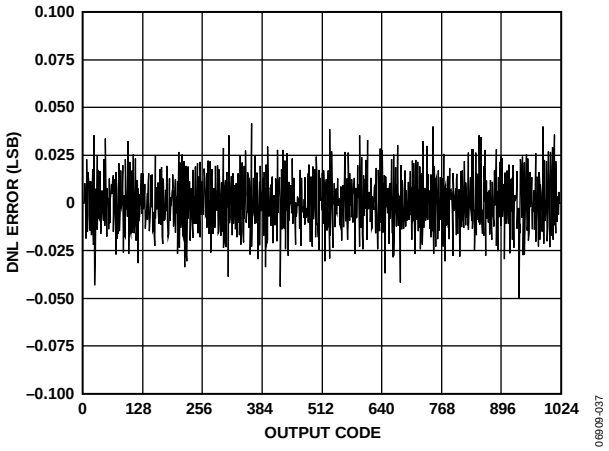



Figure 42. AD9600 DNL with $f_{IN1}$ = 10.3 MHz

# THEORY OF OPERATION

The AD9600 dual ADC design can be used for diversity reception of signals, where the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any $f_S/2$ frequency segment from dc to 200 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Although operation of up to 450 MHz analog input is permitted, ADC distortion increases at frequencies toward the higher end of this range.

In nondiversity applications, the AD9600 can be used as a baseband receiver where one ADC is used for I input data and the other used for Q input data.

Synchronization capability is provided to allow synchronized timing among multiple channels or multiple devices.

Programming and control of the AD9600 is accomplished using a 3-bit SPI-compatible serial interface.

## ADC ARCHITECTURE

The AD9600 architecture consists of a dual front-end sample-and-hold amplifier (SHA) followed by a pipelined switched-capacitor ADC. The quantized outputs from each stage are combined into a final 10-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline excluding the last consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

## ANALOG INPUT CONSIDERATIONS

The analog input to the AD9600 is a differential switched-capacitor SHA that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the SHA between sample mode and hold mode (see Figure 45). When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent on the application.

In undersampling (IF sampling) applications, any shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. See the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values are dependent on the application.

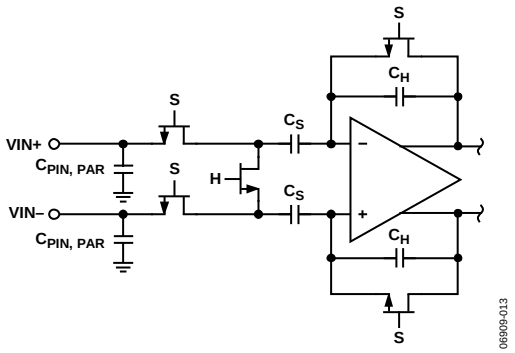



*Figure 45. Switched-Capacitor SHA Input*

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched.

An internal differential reference buffer creates positive and negative reference voltages that define the input span of the ADC core. The span of the ADC core is set by the buffer to 2 × VREF.

### *Input Common Mode*

The analog inputs of the AD9600 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM}$ = 0.55 × AVDD is recommended for optimum performance, but the device can function over a wider range with reasonable performance (see Figure 44). An on-board common-mode voltage reference is included in the design and is available from the CML pin. Optimum performance is achieved when the common-mode voltage of the analog input is set by the CML pin voltage (typically 0.55 × AVDD). The CML pin must be decoupled to ground by a 0.1 µF capacitor as described in the Applications Information section.

### *Differential Input Configurations*

Optimum performance is achieved while driving the AD9600 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the

ADC. The output common-mode voltage of the AD8138 is easily set with the CML pin of the AD9600 (see Figure 46), and the driver can be configured in a Sallen-Key filter topology to band limit the input signal.

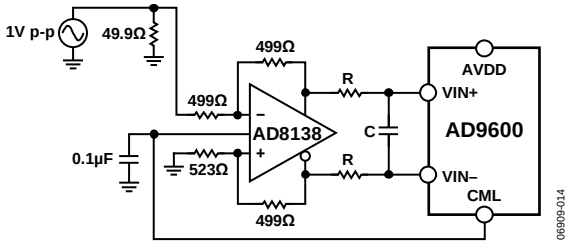



*Figure 46. Differential Input Configuration Using the AD8138*

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 47. The CML voltage can be connected to the center tap of the transformer's secondary winding to bias the analog input.

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can cause core saturation, which leads to distortion.

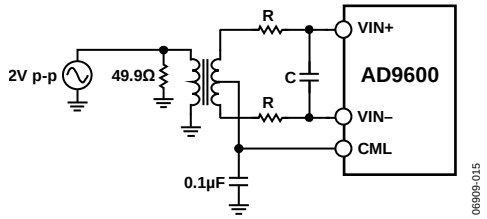



*Figure 47. Differential Transformer-Coupled Configuration*

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9600. For applications where SNR is a key parameter, differential double-balun coupling is the recommended input configuration. An example is shown in Figure 49.

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver. An example is shown in Figure 50. See the AD8352 data sheet for more information.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 10 lists the recommended values to set the RC network. However, the actual values are dependent on the input signal; therefore, Table 10 should only be used as a starting guide.

**Table 10. Example RC Network**

| Frequency Range (MHz) | R Series (Ω, Each) | C Differential (pF) |
|---|---|---|
| 0 to 70 | 33 | 15 |
| 70 to 200 | 33 | 5 |
| 200 to 300 | 15 | 5 |
| >300 | 15 | Open |

### *Single-Ended Input Configuration*

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance. Figure 48 details a typical single-ended input configuration.

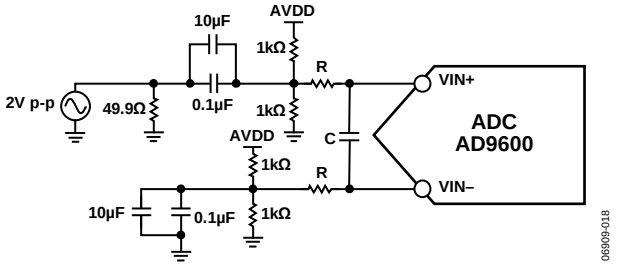



*Figure 48. Single-Ended Input Configuration*

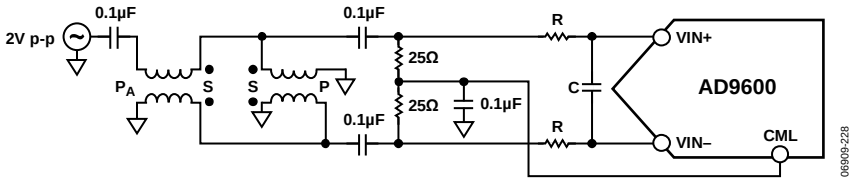



*Figure 49. Differential Double-Balun Input Configuration*

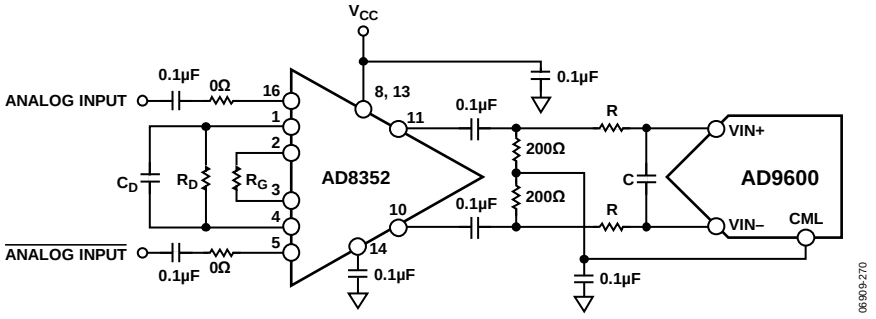



*Figure 50. Differential Input Configuration Using the AD8352*

## VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9600. The input range can be adjusted by varying the reference voltage applied to the AD9600, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. The various reference modes are summarized in this section. The Reference Decoupling section describes the best PCB layout practices for the reference.

### *Internal Reference Connection*

A comparator within the AD9600 detects the potential at the SENSE pin and configures the reference into four possible modes, which are summarized in Table 11. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 51), setting VREF to 1.0 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected external to the chip as shown in Figure 52, the switch again selects the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

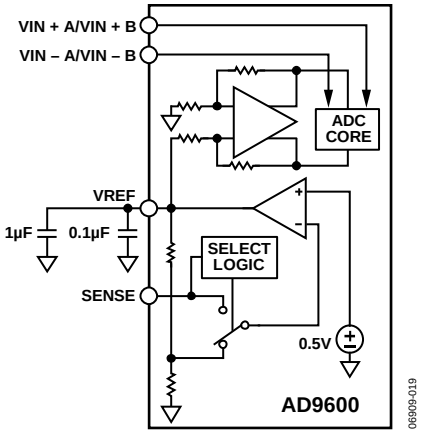



*Figure 51. Internal Reference Configuration*

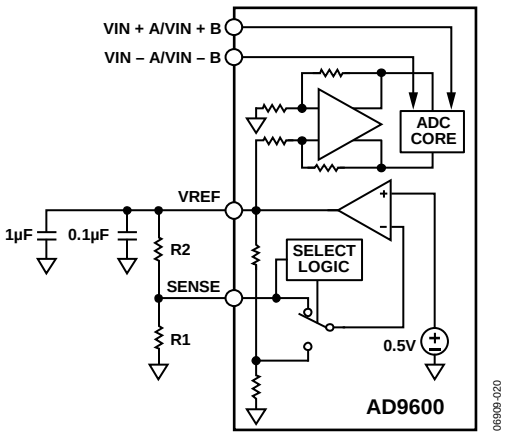



*Figure 52. Programmable Reference Configuration*

If the internal reference of the AD9600 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 53 depicts how the internal reference voltage is affected by loading.

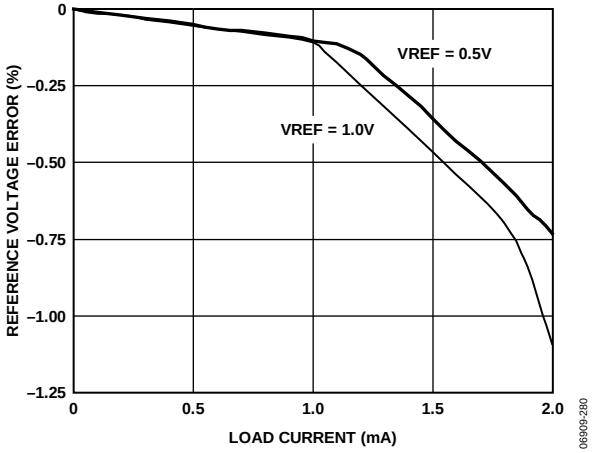



*Figure 53. VREF Accuracy vs. Load*

**Table 11. Reference Configuration Summary**

| Selected Mode | SENSE Voltage | Resulting VREF (V) | Resulting Differential Span (V p-p) |
|---|---|---|---|
| External Reference | AVDD | N/A | 2 × external reference |
| Internal Fixed Reference | VREF | 0.5 | 1.0 |
| Programmable Reference | 0.2 V to VREF | $0.5 \times \left(1 + \frac{R2}{R1}\right)$ (see Figure 52) | 2 × VREF |
| Internal Fixed Reference | AGND to 0.2 V | 1.0 | 2.0 |

### External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve the thermal drift characteristics. Figure 54 shows the typical drift characteristics of the internal reference in 1.0 V mode.

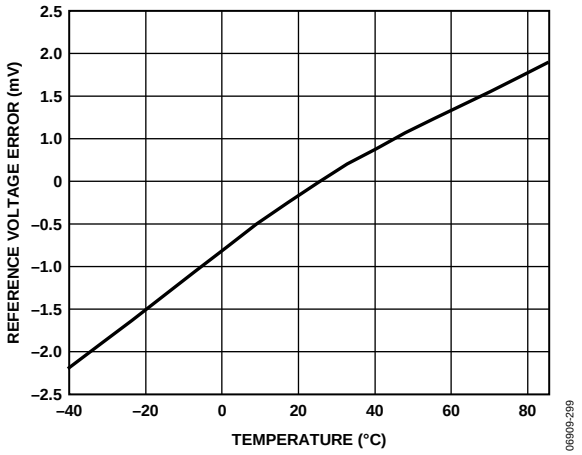



Figure 54. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 6 kΩ load (see Figure 15). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

## CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9600 sample clock inputs (CLK+ and CLK–) should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally (see Figure 55) and require no external bias.

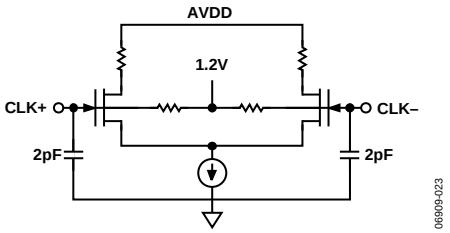



Figure 55. Equivalent Clock Input Circuit

### Clock Input Options

The AD9600 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, the jitter of the clock source is of the most concern, as described in the Jitter Considerations section.

Figure 56 and Figure 57 show preferred methods for clocking the AD9600 (at clock rates of up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF balun or an RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the secondary transformer or balun limit clock excursions into the AD9600 to approximately 0.8 V p-p differential.

This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9600 while preserving the fast rise and fall times of the signal that are critical to low jitter performance.

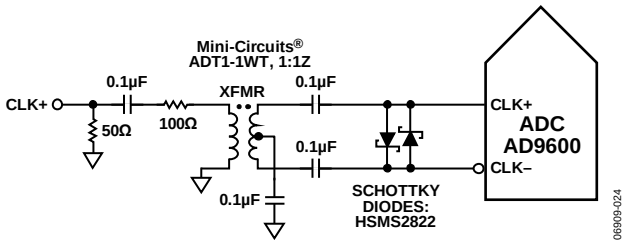



Figure 56. Transformer-Coupled Differential Clock (up to 200 MHz)

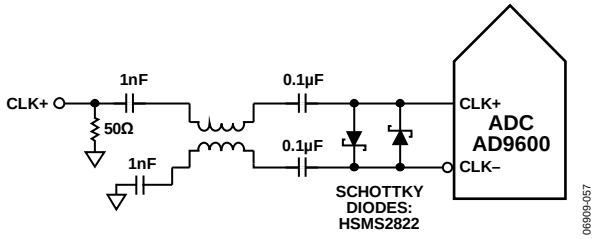



Figure 57. Balun-Coupled Differential Clock (up to 625 MHz)

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 58. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

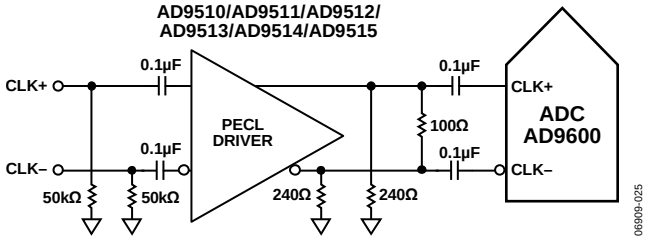



Figure 58. Differential PECL Sample Clock (up to 150 MSPS)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins as shown in Figure 59. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offer excellent jitter performance.

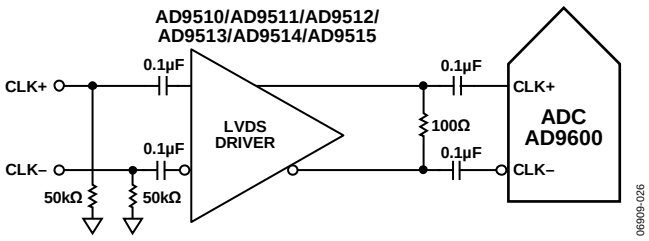



Figure 59. Differential LVDS Sample Clock (up to 150 MSPS)

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK− pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 60). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.6 V and therefore offers several selections for the drive logic voltage.

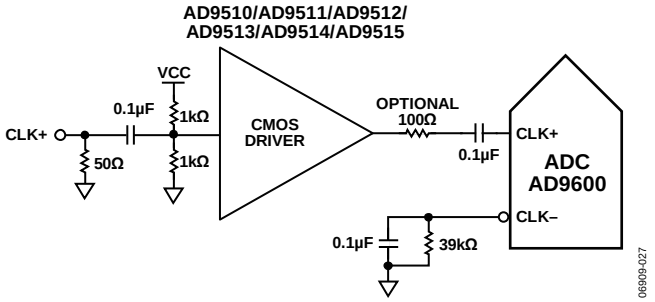



*Figure 60. Single-Ended 1.8 V CMOS Sample Clock (up to 150 MSPS)*

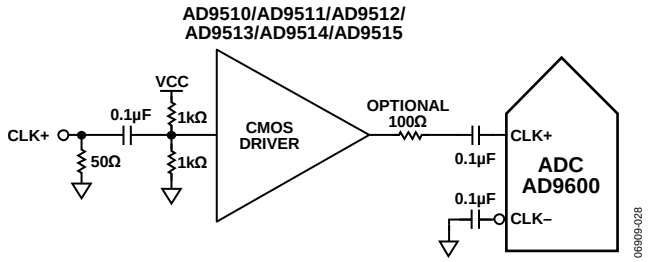



*Figure 61. Single-Ended 3.3 V CMOS Sample Clock (up to 150 MSPS)*

### Input Clock Divider

The AD9600 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. If a divide ratio other than 1 is selected, the duty cycle stabilizer is automatically enabled.

The AD9600 clock divider can be synchronized by using the external SYNC input. Bit 1 and Bit 2 of Register 0x100 allow the clock divider to be resynchronized either on every SYNC signal or on only the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows aligning the clock dividers of multiple devices to guarantee simultaneous input sampling.

### Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9600 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (or falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9600. When the SDIO/DCS pin functions as DCS, noise and distortion performance are nearly flat for a wide range of duty cycles, as shown in Figure 43.

Jitter in the rising edge of the input is an important concern, and it is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz nominally. The loop has a time constant associated with it that needs to be considered if the clock rate may change dynamically. This requires a wait time of 1.5 µs to 5 µs after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During this time, the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty clock stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

### Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency ($f_{IN}$) due to jitter ($t_J$) can be calculated as

$$SNR = -20\log\left(2\pi f_{IN} \times t_J\right)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 62).

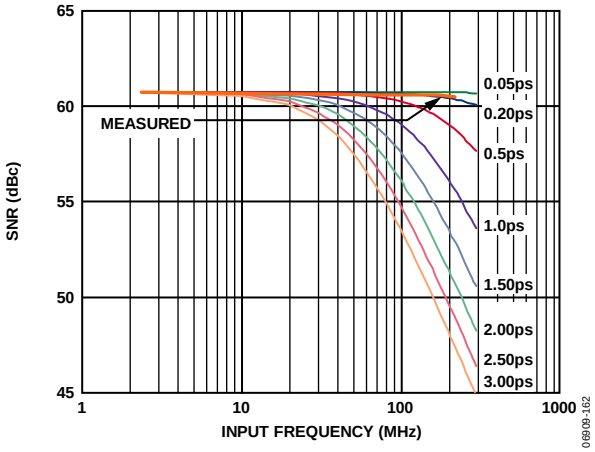



*Figure 62. SNR vs. Input Frequency and Jitter*

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9600. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

## POWER DISSIPATION AND STANDBY MODE

As shown in Figure 63, the power dissipated by the AD9600 is proportional to its sample rate. In CMOS output mode, the digital power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current ($I_{DRVDD}$) can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where $N$ is the number of output bits (22 in the case of AD9600 with the fast detect output pins disabled).

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency, $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal. Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 63 was taken with the same operating conditions as the Typical Performance Characteristics, with a 5 pF load on each output driver.

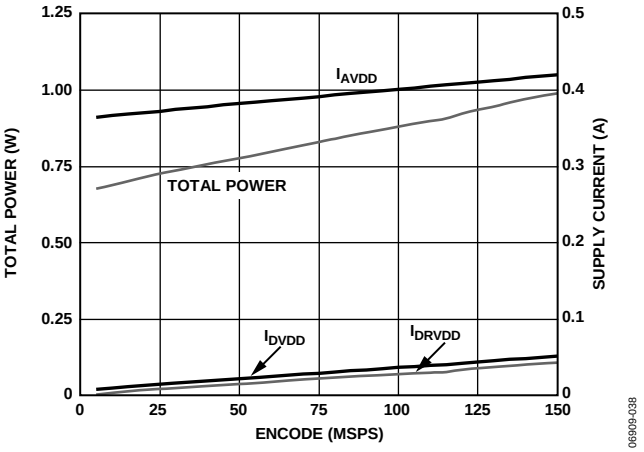



Figure 63. AD9600-150 Power and Current vs. Sample Rate

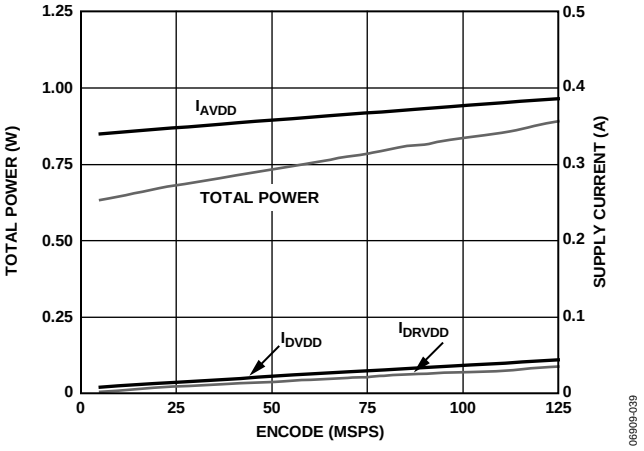



Figure 64. AD9600-125 Power and Current vs. Sample Rate

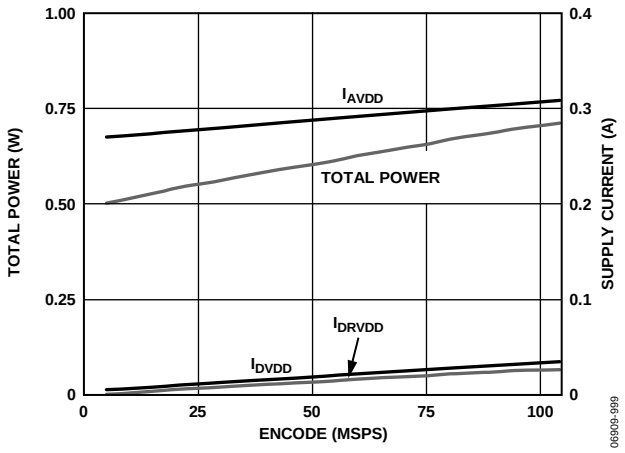



Figure 65. AD9600-105 Power and Current vs. Sample Rate

By asserting the PDWN mode (either through the SPI port or by asserting the PDWN pin high), the AD9600 is placed into power-down mode. In this state, the ADC typically dissipates 2.5 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9600 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in power-down mode: shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC into power-down or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Description section for more details.

## DIGITAL OUTPUTS

The AD9600 output drivers can be configured to interface with 1.8 V to 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic.

In CMOS output mode, the output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies and may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The output data format can be selected for either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 12). As detailed in the Memory Map Register Description section, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

**Table 12. SCLK/DFS Mode Selection (External Pin Mode)**

| Voltage at Pin | SCLK/DFS | SDIO/DCS |
|---|---|---|
| AGND | Offset binary (default) | DCS disabled |
| AVDD | Twos complement | DCS enabled (default) |

### *Digital Output Enable Function (OEB)*

The AD9600 has a flexible three-state ability for the digital output pins. The three-state mode can be enabled by using the SMI SDO/OEB pin or the SPI interface. If the SMI SDO/OEB pin is low, the output data drivers are enabled. If the SMI SDO/OEB pin is high, the output data drivers are placed into a high impedance state. This output enable function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

When the device uses the SPI interface, each channel's data and fast detect output pins can be independently three-stated by using the output enable bar bit in Register 0x14.

## TIMING

The AD9600 provides latched data with a pipeline delay of 12 clock cycles. Data outputs are available one propagation delay ($t_{PD}$) after the rising edge of the clock signal.

The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9600. These transients can degrade the dynamic performance of the converter. The lowest typical conversion rate of the AD9600 is typically 10 MSPS. At clock rates below 10 MSPS, dynamic performance may degrade.

### *Data Clock Output (DCO)*

The AD9600 provides two data clock output (DCO) signals intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO, unless the polarity has been changed via the SPI. See the timing diagrams shown in Figure 2 and Figure 3 for more information.

**Table 13. Output Data Format**

| Input (V) | Condition (V) | Binary Output Mode | Twos Complement Mode | Overrange |
|---|---|---|---|---|
| (VIN+) – (VIN–) | < –VREF – 0.5 LSB | 00 0000 0000 | 10 0000 0000 | 1 |
| (VIN+) – (VIN–) | = –VREF | 00 0000 0000 | 10 0000 0000 | 0 |
| (VIN+) – (VIN–) | = 0 | 10 0000 0000 | 00 0000 0000 | 0 |
| (VIN+) – (VIN–) | = +VREF – 1.0 LSB | 11 1111 1111 | 01 1111 1111 | 0 |
| (VIN+) – (VIN–) | > +VREF – 0.5 LSB | 11 1111 1111 | 01 1111 1111 | 1 |

# ADC OVERRANGE AND GAIN CONTROL

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overflow indicator provides after-the-fact information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, latency of this function is of major concern. Highly pipelined converters can have significant latency. A good compromise is to use the output bits from the first stage of the ADC for this function. Latency for these output bits is very low, and overall resolution is not highly significant. Peak input signals are typically between full scale and 6 dB to 10 dB below full scale. A 3-bit or 4-bit output provides adequate range and resolution for this function.

Via the SPI port, the user can provide a threshold above which an overrange output would be active. As long as the signal is below that threshold, the output should remain low. The fast detect output pins can also be programmed via the SPI port so that one of the pins functions as a traditional overrange pin for customers who currently use this feature. In this mode, all 12 bits of the converter are examined in the traditional manner, and the output is high for the condition normally defined as overflow. In either mode, the magnitude of the data is considered in the calculation of the condition (but the sign of the data is not considered). The threshold detection responds identically to positive and negative signals outside the desired magnitude range.

## FAST DETECT OVERVIEW

The AD9600 contains circuitry to facilitate fast overrange detection, allowing very flexible external gain control implementations. Each ADC has four fast detect output pins that are used to output information about the current state of the ADC input level. The function of these pins is programmable via the fast detect mode select bits and the fast detect enable bit in Register 0x104, allowing range information to be output from several points in the internal datapath. These pins can also be set up to indicate the presence of overrange or underrange conditions, according to programmable threshold levels. Table 14 shows the six configurations available for the fast detect pins.

**Table 14. Fast Detect Mode Select Bits Settings**

| Fast Detect Mode Select Bits (Register 0x104 [3:1]) | Information Presented on Fast Detect (FD) Pins of Each ADC[1, 2] | | | |
|---|---|---|---|---|
| | FD [3] | FD [2] | FD [1] | FD [0] |
| 000 | ADC fast magnitude (see Table 15) | | | |
| 001 | ADC fast magnitude (see Table 16) | | | OR |
| 010 | ADC fast magnitude (see Table 17) | | OR | F_LT |
| 011 | ADC fast magnitude (see Table 17) | | C_UT | F_LT |
| 100 | OR | C_UT | F_UT | F_LT |
| 101 | OR | F_UT | IG | DG |

[1] The fast detect pins are FD0A/FD0B to FD9A/FD9B for the CMOS mode configuration and FD0+/FD0– to FD9+/FD9– for the LVDS mode configuration.
[2] See the ADC Overrange (OR) and Gain Switching sections for more information about OR, C_UT, F_UT, F_LT, IG, and DG.

## ADC FAST MAGNITUDE

When the fast detect output pins are configured to output the ADC fast magnitude (that is, when the fast detect mode select bits are set to 0b000), the information presented is the ADC level from an early converter stage with only a two-clock-cycle latency (when in CMOS output mode). Using the fast detect output pins in this configuration provides the earliest possible level indication information. Because this information is provided early in the datapath, there is a significant uncertainty in the level indicated. The nominal levels, along with the uncertainty indicated by the ADC fast magnitude, are shown in Table 15.

**Table 15. ADC Fast Magnitude Nominal Levels with Fast Detect Mode Select Bits = 000**

| ADC Fast Magnitude on FD [3:0] Pins | Nominal Input Magnitude Below FS (dB) | Nominal Input Magnitude Uncertainty (dB) |
|---|---|---|
| 0000 | <–24 | Minimum to –18.07 |
| 0001 | –24 to –14.5 | –30.14 to –12.04 |
| 0010 | –14.5 to –10 | –18.07 to –8.52 |
| 0011 | –10 to –7 | –12.04 to –6.02 |
| 0100 | –7 to –5 | –8.52 to –4.08 |
| 0101 | –5 to –3.25 | –6.02 to –2.5 |
| 0110 | –3.25 to –1.8 | –4.08 to –1.16 |
| 0111 | –1.8 to –0.56 | –2.5 to FS |
| 1000 | –0.56 to 0 | –1.16 to 0 |

When the fast detect mode select bits are set to 0b001, 0b010, or 0b011, a subset of the fast detect output pins is available. In these modes, the fast detect output pins have a latency of six clock cycles. Table 16 shows the corresponding ADC input levels when the fast detect mode select bits are set to 0b001 (that is, when ADC fast magnitude is presented on the FD [3:1] pins).

**Table 16. ADC Fast Magnitude Nominal Levels with Fast Detect Mode Select Bits = 001**

| ADC Fast Magnitude on FD [3:1] Pins | Nominal Input Magnitude Below FS (dB) | Nominal Input Magnitude Uncertainty (dB) |
|---|---|---|
| 000 | <−24 | Minimum to −18.07 |
| 001 | −24 to −14.5 | −30.14 to −12.04 |
| 010 | −14.5 to −10 | −18.07 to −8.52 |
| 011 | −10 to −7 | −12.04 to −6.02 |
| 100 | −7 to −5 | −8.52 to −4.08 |
| 101 | −5 to −3.25 | −6.02 to −2.5 |
| 110 | −3.25 to −1.8 | −4.08 to −1.16 |
| 111 | −1.8 to 0 | −2.5 to 0 |

When the fast detect mode select bits are set to 0b010 or 0b011 (that is, when ADC fast magnitude is presented on the FD [3:2] pins), the LSB is not provided. The input ranges for this mode are shown in Table 17.

**Table 17. ADC Fast Magnitude Nominal Levels with Fast Detect Mode Select Bits = 010 or 011**

| ADC Fast Magnitude on FD [3:2] Pins | Nominal Input Magnitude Below FS (dB) | Nominal Input Magnitude Uncertainty (dB) |
|---|---|---|
| 00 | <−14.5 | Minimum to −12.04 |
| 01 | −14.5 to −7 | −18.07 to −6.02 |
| 10 | −7 to −3.25 | −8.52 to −2.5 |
| 11 | −3.25 to 0 | −4.08 to 0 |

## ADC OVERRANGE (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and therefore is subject to the 12-clock-cycle latency. An overrange at the input would be indicated by this bit 12 clock cycles after it occurred.

## GAIN SWITCHING

The AD9600 includes circuitry that is useful in applications either where large dynamic ranges exist or where gain ranging converters are employed. This circuitry allows digital thresholds to be set such that an upper threshold and a lower threshold can be programmed. Fast detect mode select bit = 010 through fast detect mode select bit = 101 support various combinations of the gain switching options.

One such use is to detect when an ADC is about to reach full scale with a particular input condition. The result is to provide an indicator that can be used to quickly insert an attenuator that prevents ADC overdrive.

### *Coarse Upper Threshold (C_UT)*

The coarse upper threshold indicator is asserted if the ADC fast magnitude input level is greater than the level programmed in the coarse upper threshold register at Address 0x105 [2:0]. The coarse upper threshold output is output two clock cycles after the level is exceeded at the input and therefore provides a fast indication of the input signal level. The coarse upper threshold levels are shown in Table 18. This indicator remains asserted for a minimum of two ADC clock cycles or until the signal drops below the threshold level.

**Table 18. Coarse Upper Threshold Levels**

| Coarse Upper Threshold (Register 0x105 [2:0]) | C_UT Is Active When Signal Magnitude Below FS Is Greater Than (dB) |
|---|---|
| 000 | <−24 |
| 001 | −24 |
| 010 | −14.5 |
| 011 | −10 |
| 100 | −7 |
| 101 | −5 |
| 110 | −3.25 |
| 111 | −1.8 |

### *Fine Upper Threshold (F_UT)*

The fine upper threshold indicator is asserted if the input magnitude exceeds the value programmed in the fine upper threshold register located at Address 0x106 and Address 0x107. The 13-bit threshold register is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC clock latency but is accurate in terms of the converter resolution. The fine threshold magnitude is defined by the following equation:

$$dBFS = 20 \log(Threshold\ Magnitude/2^{13}) \quad (1)$$

### *Fine Lower Threshold (F_LT)*

The fine lower threshold indicator is asserted if the input magnitude is less than the value programmed in the fine lower threshold register located at Address 0x108 and Address 0x109. The fine lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC clock latency but provides a comparison accurate to the converter resolution. The fine threshold magnitude is defined in Equation 1.

The operation of the F_UT and F_LT indicators is shown in Figure 66.

### *Increment Gain (IG) and Decrement Gain (DG)*

The increment gain and decrement gain indicators are intended to be used together to provide information to enable external gain control. The decrement gain indicator works in conjunction with the coarse upper threshold bits, asserting when the input magnitude is greater than the 3-bit value in the coarse upper threshold register (Address 0x105). The increment gain indicator, similarly, corresponds with the fine lower threshold bits, except that it is asserted only if the input magnitude is less than the value programmed in the fine lower threshold register after the dwell time elapses. This dwell time is set by the 16-bit increase gain dwell time register (Address 0x10A and Address 0x10B) and is in units of ADC input clock cycles ranging from 1 to 65,535. The fine lower threshold register is a 13-bit register that is compared with the magnitude at the output of the ADC. This comparison is subject to the ADC clock latency but allows a finer, more accurate comparison. The fine threshold magnitude is defined in Equation 1 (see the Fine Upper Threshold (F_UT) section).

The decrement gain output is influenced by the fast detect output pins, which provide a fast indication of potential overrange conditions. Assertion of the increment gain indicator is based on the comparison at the output of the ADC, requiring the input magnitude to remain below an accurate, programmable level for a predefined period before signaling external circuitry to increase the gain.

The operation of the IG and DG indicators is shown in Figure 66.

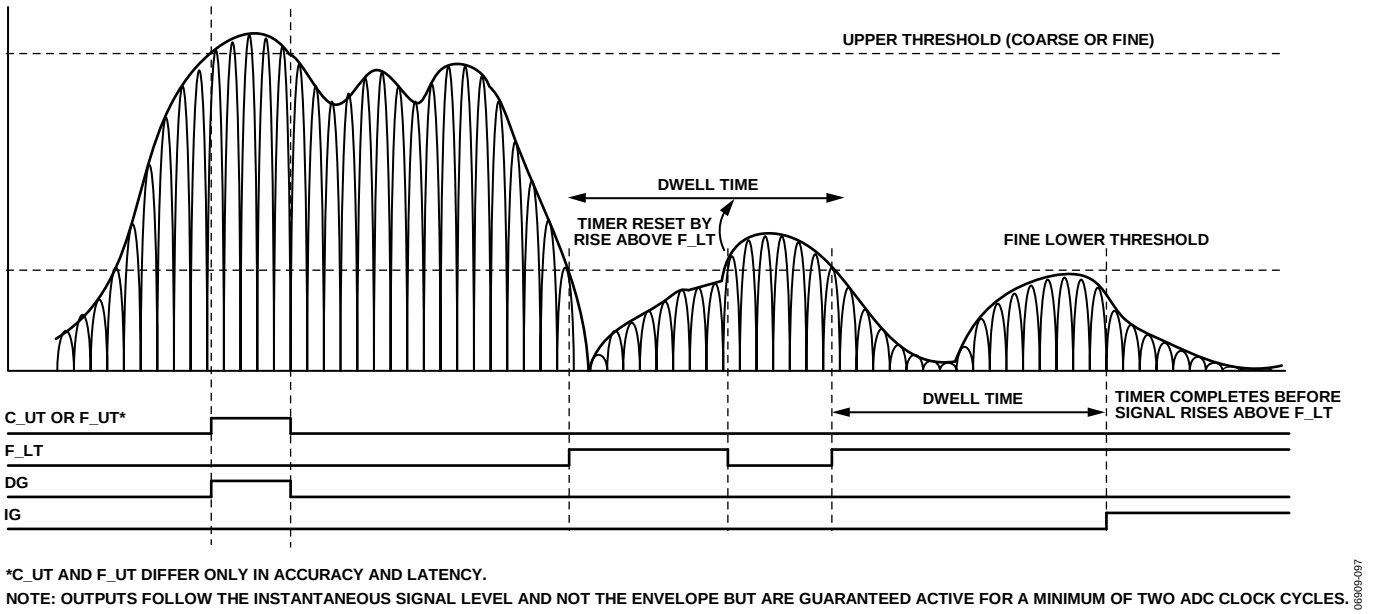



*Figure 66. Threshold Settings for C_UT, F_UT, F_LT, IG, and DG*

# SIGNAL MONITOR

The signal monitoring block provides additional information about the signal being digitized by the ADC. The signal monitor computes the rms input magnitude, the peak magnitude, and/or the number of samples by which the magnitude exceeds a particular threshold. Together, these functions can be used to gain insight into the signal characteristics and to estimate the peak/average ratio or even the shape of the complementary cumulative distribution function (CCDF) curve of the input signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The signal monitor result values can be obtained from the part by reading back Register 0x116 to Register 0x11B, using the SPI port or the signal monitor SPORT output. The output contents of the SPI-accessible signal monitor registers are set via the two signal monitor mode bits of the signal monitor control register (Address 0x112). Both ADC channels must be configured for the same signal monitor mode. Separate SPI-accessible, 20-bit signal monitor result (SMR) registers (Address 0x116 to Address 0x11B) are provided for each ADC channel. Any combination of the signal monitor functions can also be output to the user via the serial SPORT interface. These outputs are enabled using the peak detector output enable, rms magnitude output enable, and threshold crossing output enable bits in the signal monitor SPORT control register (Address 0x111).

For each of the signal monitor measurements, a programmable signal monitor period register (SMPR) controls the duration of the measurement. This period is programmed as the number of input clock cycles in the 24-bit signal monitor period register located at Address 0x113, Address 0x114, and Address 0x115. This register can be programmed with a period from 128 samples to 16.78 ($2^{24}$) million samples.

Because the dc offset of the ADC can be significantly larger than the signal of interest (affecting the results from the signal monitor), a dc correction circuit is included as part of the signal monitor block to null the dc offset before measuring the power.

## PEAK DETECTOR MODE

The magnitude of the input port signal is monitored over a programmable period (determined by SMPR) to give the peak value detected. This function is enabled by programming a Logic 1 in the signal monitor mode bits of the signal monitor control register (Address 0x112) or by setting the peak detector output enable bit in the signal monitor SPORT control register (Address 0x111). The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer and the countdown is started. The magnitude of the input signal is compared with the value in the internal peak level holding register (not accessible to the user), and the greater of the two values is updated as the current peak level. The initial value in the peak level holding register is set to the current ADC input signal magnitude, and the comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit value in the peak level holding register is transferred to the signal monitor holding register (not accessible to the user) and can be read through the SPI port or output through the SPORT serial interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the value in the peak level holding register is reset to the magnitude of the first input sample, and the previously explained comparison and update procedure continues.

Figure 67 is a block diagram of the peak detector logic. The SMR register contains the absolute magnitude of the peak detected by the peak detector logic.

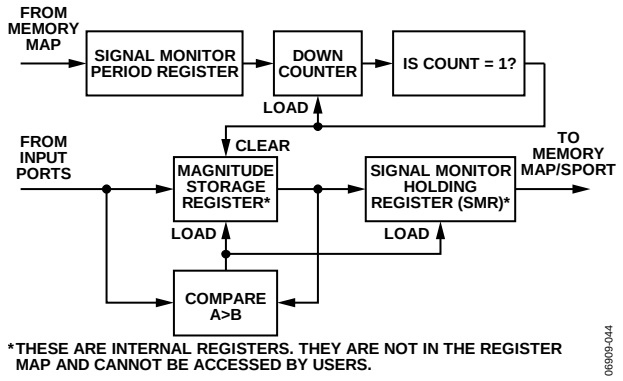



*Figure 67. ADC Input Peak Detector Block Diagram*

## RMS/MS MAGNITUDE MODE

In this mode, the root-mean-square (rms) or mean-square (ms) magnitude of the input port signal is integrated (by adding an accumulator) over a programmable period (determined by SMPR) to give the rms or ms magnitude of the input signal. This mode is set by programming Logic 0 in the signal monitor mode bits of the signal monitor control register (Address 0x112) or by setting the rms magnitude output enable bit in the signal monitor SPORT control register (Address 0x111). The 24-bit SMPR, representing the period over which integration is performed, must be programmed before activating this mode.

After enabling the rms/ms magnitude mode, the value in the SMPR is loaded into a monitor period timer, and the countdown is started immediately. Each input sample is converted to floating-point format and squared. It is then converted to an 11-bit fixed-point format and added to the contents of the 24-bit accumulator. The integration continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the square root of the value in the accumulator is taken and transferred (after some formatting) to the signal monitor holding register, which can be read through the SPI port or output through the SPORT serial port. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition,

the value of the accumulator is reset to the first input sample signal power, and the accumulation continues with the subsequent input samples.

Figure 68 illustrates the rms magnitude monitoring logic.

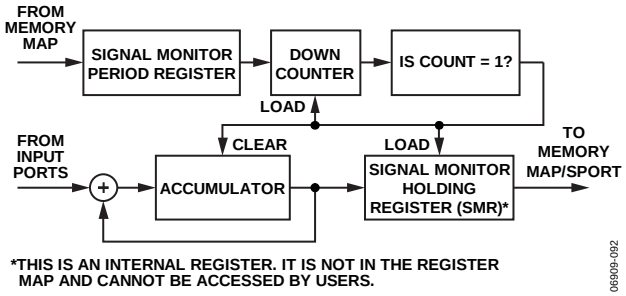



*Figure 68. ADC Input RMS Magnitude Monitoring Block Diagram*

For rms magnitude mode, the value in the signal monitor result (SMR) register is a 20-bit fixed-point number. The following equation can be used to determine the rms magnitude in decibels full scale (dBFS) from the MAG value in the register:

$$RMS\ Magnitude = 20\log\left(\frac{MAG}{2^{20}}\right) - 10\log\left[\frac{SMP}{2^{ceil[\log_2(SMP)]}}\right]$$

where if the signal monitor period (SMP) is a power of 2, the second term in the equation becomes 0.

For ms magnitude mode, the value in the SMR is a 20-bit fixed-point number. The following equation can be used to determine the ms magnitude in decibels full scale (dBFS) from the MAG value in the register:

$$MS\ Magnitude = 10\log\left(\frac{MAG}{2^{20}}\right) - 10\log\left[\frac{SMP}{2^{ceil[\log_2(SMP)]}}\right]$$

where if the SMP is a power of 2, the second term in the equation becomes 0.

## THRESHOLD CROSSING MODE

In the threshold crossing mode of operation, the magnitude of the input port signal is monitored over a programmable period (determined by SMPR) to count the number of times it crosses a certain programmable threshold value. This mode is set by programming Logic 1x (where x is a don't care bit) in the signal monitor mode bits of the signal monitor control register (Address 0x112) or by setting the threshold crossing output enable bit in the signal monitor SPORT control register (Address 0x111). Before activating this mode, the user needs to program the 24-bit signal monitor period register (Address 0x113 to Address 0x115) and the 13-bit fine upper threshold register (Address 0x106 and Address 0x107) for each individual input port. The same fine upper threshold register is used for both signal monitoring and gain control (see the ADC Overrange and Gain Control section).

After entering this mode, the value in the SMPR is loaded into a monitor period timer and the countdown is started. The magnitude of the input signal is compared with the previously programmed fine upper threshold register on each input clock cycle. If the input signal has a magnitude greater than the value set in the fine upper threshold register, the value in the internal count register (not accessible to the user) is incremented by 1.

The initial value of the internal count register is set to 0. The comparison and incrementing of this value continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the value in the internal count register is transferred to the signal monitor holding register (not accessible to the user), which can be read through the SPI port or output through the SPORT serial port.

The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. The internal count register is also cleared to a value of 0. Figure 69 illustrates the threshold crossing logic. The value in the SMR register is the number of samples that have a magnitude greater than the fine upper threshold register.

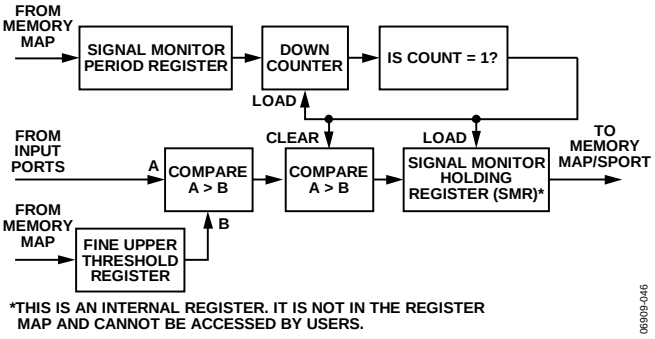



*Figure 69. ADC Input Threshold Crossing Block Diagram*

## ADDITIONAL CONTROL BITS

For additional flexibility in the signal monitoring process, two control bits are provided in the signal monitor control register (Address 0x112). They are the signal monitor enable bit and the complex power calculation mode enable bit.

### *Signal Monitor Enable Bit*

The signal monitor enable bit, located in Bit 0 of Register 0x112, enables operation of the signal monitor block. If the signal monitor function is not needed in a particular application, this bit should be cleared (default) to conserve power.

### *Complex Power Calculation Mode Enable Bit*

When this bit is set, the part assumes that Channel A is digitizing the I data and Channel B is digitizing the Q data for a complex input signal (or vice versa). In this mode, the power reported is equal to

$$\sqrt{I^2 + Q^2}$$

This result is presented in the signal monitor DC value Channel A register (Address 0x10D and Address 0x10E) if the signal monitor mode bits are set to 00. The signal monitor DC value Channel B register (Address 0x10F and Address 0x110) continues to compute the Channel B value.

## DC CORRECTION

Because the dc offset of the ADC may be significantly larger than the signal being measured, a dc correction circuit is included to null the dc offset before measuring the power. The dc correction circuit can also be switched into the main signal path, but this may not be appropriate if the ADC is digitizing a time-varying signal with significant dc content, such as GSM.

### *DC Correction Bandwidth*

The dc correction circuit is a high-pass filter with a programmable bandwidth (ranging between 0.15 Hz and 1.2 kHz at 125 MSPS). The bandwidth is controlled by writing the 4-bit dc correction bandwidth register located at Register 0x10C, Bits [5:2].

The following equation can be used to compute the bandwidth value for the dc correction circuit:

$$DC\_Corr\_BW = 2^{-k-14} \times \frac{f_{CLK}}{2 \times \pi}$$

where:
$k$ is the 4-bit value programmed in Register 0x10C, Bits [5:2] (values between 0 and 13 are valid for k; programming 14 or 15 provides the same result as programming 13).
$f_{CLK}$ is the AD9600 ADC sample rate in hertz.

### *DC Correction Readback*

The current dc correction value can be read back in Register 0x10D and Register 0x10E for Channel A and Register 0x10F and Register 0x110 for Channel B. The dc correction value is a 10-bit value that can span the entire input range of the ADC.

### *DC Correction Freeze*

Setting the dc correction freeze bit (Bit 6 of Register 0x10C) halts the dc correction at its current state and continues to use the last updated value as the dc correction value. Clearing this bit restarts dc correction and adds the currently calculated value to the data.

### *DC Correction Enable Bits*

Setting Bit 0 (the dc correction for SM enable bit) of Register 0x10C enables the dc correction for use in the signal monitor calculations. Setting Bit 1 (the dc correction for signal path enable bit) of Register 0x10C enables the calculated dc correction value to be added to the output data signal path.

## SIGNAL MONITOR SPORT OUTPUT

The SPORT is a serial interface with three output pins: SMI SCLK (SPORT clock), SMI SDFS (SPORT frame sync), and SMI SDO (SPORT data). The SPORT is the master and drives all three SPORT output pins on the chip.

### *SMI SCLK*

The data and frame sync are driven on the positive edge of the SMI SCLK. The SMI SCLK has three possible baud rates: 1/2, 1/4, or 1/8 the ADC clock rate, based on the SPORT controls. In addition, by using the SPORT SMI SCLK sleep bit, the SMI SCLK can be gated to remain low when the signal monitor block is not sending any data. Using this bit to disable the SMI SCLK when it is not needed can reduce coupling errors in the return signal path. Doing so, however, has the disadvantage of spreading the frequency content of the clock; if desired, the SMI SCLK can be left enabled to ease frequency planning.

### *SMI SDFS*

The SMI SDFS is the serial data frame sync. It defines the start of a frame. One SPORT frame includes data from both datapaths. The data from Datapath A is sent just after the frame sync, followed by data from Datapath B.

### *SMI SDO*

The SMI SDO is the serial data output of the block. The data is sent MSB first on the first positive edge after the SMI SDFS. Each data output block includes one or more rms magnitude value, peak level value, and threshold crossing value from each datapath in the stated order. If enabled, the data is sent, rms first, followed by the peak value and the threshold crossing value, as shown in Figure 70.

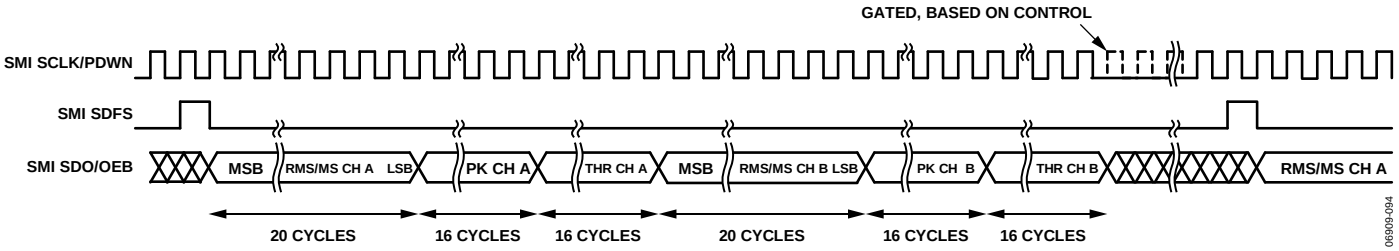



*Figure 70. Signal Monitor SPORT Output Timing (RMS, Peak, and Threshold Enabled)*

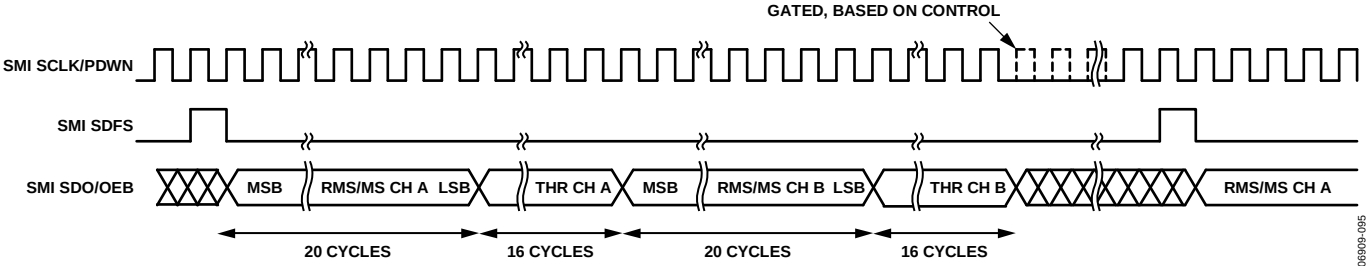



*Figure 71. Signal Monitor SPORT Output Timing (RMS and Threshold Enabled)*

# BUILT-IN SELF-TEST (BIST) AND OUTPUT TEST

The AD9600 includes built-in test features to enable verification of the integrity of each channel as well as to facilitate board level debugging. A BIST feature is included that verifies the integrity of the digital datapath of the AD9600. Various output test options are also provided to place predictable values on the outputs of the AD9600.

## BUILT-IN SELF-TEST (BIST)

The BIST is a thorough test of the digital portion of the selected AD9600 signal path. When enabled, the test runs from an internal pseudorandom noise (PN) source through the digital datapath, starting at the ADC block output. The BIST sequence runs for 512 cycles and then stops. The BIST signature value for Channel A or Channel B is placed in Register 0x24 and Register 0x25. If one channel is chosen, its BIST signature is written to the two registers. If both channels are chosen, the results of the two channels are XOR'ed and placed in the BIST signature registers. The outputs are not disconnected during this test; therefore, the PN sequence can be observed as it runs. The PN sequence can be continued from its last value or started from the beginning, based on the value programmed in Bit 2 of Register 0x0E. The BIST signature result varies depending on the channel configuration.

## OUTPUT TEST MODES

The output test options are shown in Table 22. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks, and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The seed value for the PN sequence tests can be forced by setting Bit 4 or Bit 5 of the test mode register (Address 0x0D) to hold the generator in reset mode. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

# CHANNEL/CHIP SYNCHRONIZATION

The AD9600 has a SYNC input that offers the user flexible synchronization options for synchronizing the internal blocks. The clock divider sync feature is useful to guarantee synchronized sample clocks across multiple ADCs. The signal monitor block can also be synchronized using the SYNC input, allowing properties of the input signal to be measured during a specific period. The input clock divider can be enabled to synchronize on a single occurrence of the sync signal or on every occurrence. The signal monitor block is synchronized on every SYNC input signal.

The SYNC input is internally synchronized to the sample clock; however, to ensure there is no timing uncertainty between multiple parts, the SYNC input signal should be externally synchronized to the input clock signal, meeting the setup and hold times shown in Table 5. The SYNC input should be driven using a single-ended CMOS-type signal.

# SERIAL PORT INTERFACE (SPI)

The AD9600 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This may provide the user with additional flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For detailed operational information, see AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

## CONFIGURATION USING THE SPI

There are three pins that define the SPI: SCLK, SDIO, and CSB (see Table 19). The SCLK pin is used to synchronize the read and write data presented from and to the ADC. The SDIO pin is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB pin is an active-low control that enables or disables the read and write cycles.

**Table 19. Serial Port Interface Pins**

| Pin | Function |
|---|---|
| SCLK | Serial Clock. The serial shift clock input, which is used to synchronize serial interface reads and writes. |
| SDIO | Serial Data Input/Output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame. |
| CSB | Chip Select Bar. An active-low control that gates the read and write cycles. |

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 72 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any secondary functions of the SPI pin.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits. W0 and W1 represent the number of data bytes to transfer for either a read or a write. The value represented by W1:W0 + 1 is the number of bytes to transfer.

All data is composed of 8-bit words. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB-first mode or LSB-first mode. MSB-first mode is the default on power-up and can be changed via the SPI port configuration register (Address 0x00). For more information about this and other features, see AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

## HARDWARE INTERFACE

The pins described in Table 19 constitute the physical interface between the user programming device and the serial port of the AD9600. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9600 to keep these signals from transitioning at the converter inputs during critical sampling periods.

Some pins serve a dual function when the SPI interface is not being used. When the pins are strapped to AVDD or ground during device power-on, they are associated with a specific function. The Theory of Operation section describes the strappable functions supported on the AD9600.

## CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/DCS pin, the SCLK/DFS pin, the SMI SDO/OEB pin, and the SMI SCLK/PDWN pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer, output data format, output enable, and power-down feature control. In this mode, the CSB chip select should be connected to AVDD, which disables the serial port interface.

**Table 20. Mode Selection**

| Pin | External Voltage | Configuration |
|---|---|---|
| SDIO/DCS | AVDD (default) | Duty cycle stabilizer enabled |
| | AGND | Duty cycle stabilizer disabled |
| SCLK/DFS | AVDD | Twos complement enabled |
| | AGND (default) | Offset binary enabled |
| SMI SDO/OEB | AVDD | Outputs in high impedance |
| | AGND (default) | Outputs enabled |
| SMI SCLK/PDWN | AVDD | Chip in power-down or standby |
| | AGND (default) | Normal operation |

## SPI ACCESSIBLE FEATURES

Brief descriptions of the general features available on many Analog Devices, Inc., high speed ADCs, including the AD9600, that are accessible via the SPI are included in Table 21. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9600 part-specific features are described in the Memory Map Register Description section.

**Table 21. Features Accessible Using the SPI**

| Feature Name | Description |
|---|---|
| Modes | Allows the user to set either the power-down mode or the standby mode |
| Clock | Allows the user to access the DCS via the SPI |
| Offset | Allows the user to digitally adjust the converter offset |
| Test I/O | Allows the user to set the test modes to have known data on the output bits |
| Output Mode | Allows the user to set up the outputs |
| Output Phase | Allows the user to set the output clock polarity |
| Output Delay | Allows the user to vary the DCO delay |
| VREF | Allows the user to set the reference voltage |

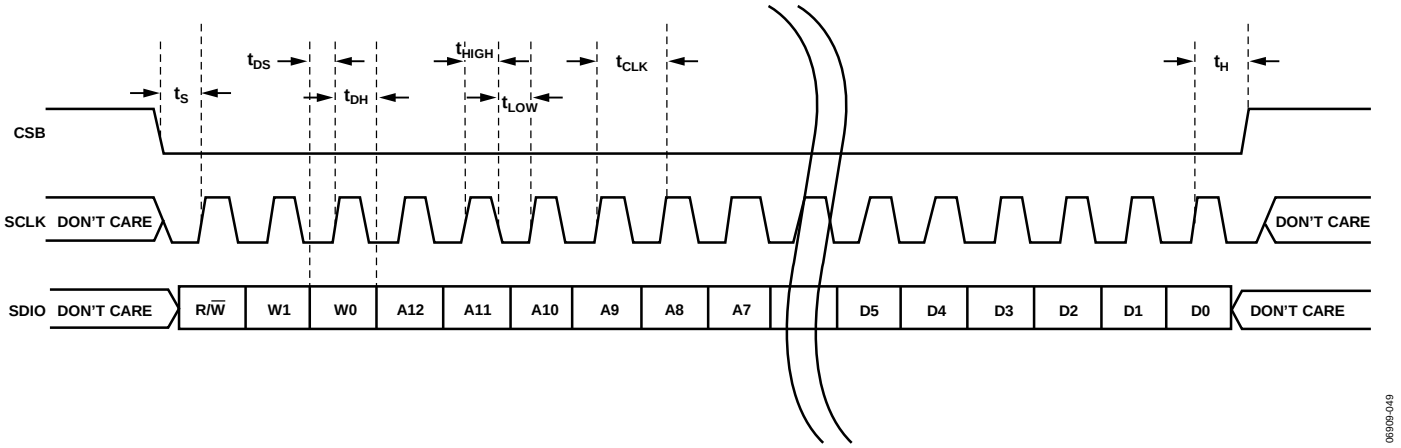



*Figure 72. Serial Port Interface Timing Diagram*

# MEMORY MAP

## READING THE MEMORY MAP TABLE

Each row in the memory map registers table (Table 22) has eight bit locations. The memory map is divided into four sections: the chip configuration registers (Address 0x00 to Address 0x02), the channel index and transfer registers (Address 0x05 and Address 0xFF), the ADC functions registers (Address 0x08 to Address 0x25), and the digital feature control registers (Address 0x100 to Address 0x11B).

The leftmost column of the memory map indicates the register address number, and the default value is shown in the second rightmost column. The (MSB) Bit 7 column is the start of the default hexadecimal value given. For example, Address 0x18, the VREF select register, has a default value of 0xC0, meaning that Bit 7 = 1, Bit 6 = 1, and the remaining bits are 0s. This setting is the default reference selection setting. The default value uses a 2.0 V peak-to-peak reference. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This application note details the functions controlled by Register 0x00 to Register 0xFF. The remaining registers (from Register 0x100 to Register 0x11B) are documented in the Memory Map Register Description section.

### *Open Locations*

All address and bit locations that are not included in Table 22 are currently not supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), this address location should not be written.

### *Default Values*

When the AD9600 comes out of a reset, critical registers are loaded with default values. The default values for the registers are given in the memory map registers table (Table 22).

### *Logic Levels*

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

### *Transfer Register Map*

Address 0x08 to Address 0x18 are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit (Bit 0 of Register 0xFF) is set. The internal update takes place when the transfer bit is set, and the bit autoclears.

### *Channel-Specific Registers*

Some channel setup functions, such as the signal monitor thresholds, can be individually programmed for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers are designated as local registers in Table 22 and can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x05. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, only Channel A or Channel B should be set to read one of the two registers. If both bits are set during an SPI read cycle, the part returns the value for Channel A.

On the other hand, registers that are designated as global registers in Table 22 affect the entire part or the channel features for which independent settings are not allowed between the channels. The settings in Register 0x05 do not affect the global registers.

## MEMORY MAP

All address and bit locations that are not included in Table 22 are currently not supported for this device.

**Table 22. Memory Map Registers**

| Addr (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | Default Notes/ Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Chip Configuration Registers** | | | | | | | | | | | |
| 0x00 | SPI Port Configuration (Global) | 0 | LSB first | Soft reset | 1 | 1 | Soft reset | LSB first | 0 | 0x18 | The nibbles are mirrored so that LSB- or MSB-first mode is set correctly, regardless of shift mode. |
| 0x01 | Chip ID (Global) | 8-bit Chip ID [7:0] (AD9600 = 0x21) (default) | | | | | | | | 0x21 Read only | Read only. |
| 0x02 | Chip Grade (Global) | Open | Open | Speed grade ID<br>00 = 150 MSPS<br>01 = 125 MSPS<br>10 = 105 MSPS<br>11 = 80 MSPS | | Open | Open | Open | Open | Read only | Speed grade ID used to differentiate devices. |
| **Channel Index and Transfer Registers** | | | | | | | | | | | |
| 0x05 | Channel Index | Open | Open | Open | Open | Open | Open | Data Channel B (default) | Data Channel A (default) | 0x03 | Bits are set to determine which on-chip device receives the next write command; applies to local registers. |
| 0xFF | Transfer | Open | Open | Open | Open | Open | Open | Open | Transfer | 0x00 | Synchronously transfers data from the master shift register to the slave. |
| **ADC Functions Registers** | | | | | | | | | | | |
| 0x08 | Power Modes | Open | Open | External power-down pin function (global)<br>0 = power-down<br>1 = standby | Open | Open | Open | Internal power-down mode (local)<br>00 = normal operation<br>01 = full power-down<br>10 = standby<br>11 = normal operation | | 0x00 | Determines various generic modes of chip operation. |
| 0x09 | Global Clock (Global) | Open | Open | Open | Open | Open | Open | Open | Duty cycle stabilizer (default) | 0x01 | |
| 0x0B | Clock Divide (Global) | Open | Open | Open | Open | Open | Clock divide ratio<br>000 = divide by 1<br>001 = divide by 2<br>010 = divide by 3<br>011 = divide by 4<br>100 = divide by 5<br>101 = divide by 6<br>110 = divide by 7<br>111 = divide by 8 | | | 0x00 | Clock divide values other than 000 automatically cause the duty cycle stabilizer to become active. |
| 0x0D | Test Mode (Local) | Open | Open | Reset PN23 gen | Reset PN9 gen | Open | Output test mode<br>000 = off (default)<br>001 = midscale short<br>010 = positive FS<br>011 = negative FS<br>100 = alternating checkerboard<br>101 = PN 23 sequence<br>110 = PN 9 sequence<br>111 = one/zero word toggle | | | 0x00 | When this register is set, the test data is placed on the output pins in place of normal data. |

| Addr (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | Default Notes/ Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0E | BIST Enable (Local) | Open | Open | Open | Open | Open | Reset BIST sequence | Open | BIST enable | 0x00 | |
| 0x10 | Offset Adjust (Local) | Open | Open | Offset adjust in LSBs from +31 to −32 (twos complement format) | | | | | | 0x00 | |
| 0x14 | Output Mode | Drive strength<br>0 V to 3.3 V CMOS or ANSI LVDS:<br>1 V to 1.8 V CMOS or reduced: LVDS (global) | Output type<br>0 = CMOS<br>1 = LVDS<br>(global) | Open | Output enable bar (local) | Open | Output invert (local) | 00 = offset binary<br>01 = twos complement<br>01 = gray code<br>11 = offset binary<br>(local) | | 0x00 | Configures the outputs and the format of the data. |
| 0x16 | Clock Phase Control (Global) | Invert DCO clock | Open | Open | Open | Open | Input clock divider phase adjust<br>000 = no delay<br>001 = 1 input clock cycle<br>010 = 2 input clock cycles<br>011 = 3 input clock cycles<br>100 = 4 input clock cycles<br>101 = 5 input clock cycles<br>110 = 6 input clock cycles<br>111 = 7 input clock cycles | | | 0x00 | Allows selection of clock delays into the input clock divider. |
| 0x17 | DCO Output Delay (Global) | Open | Open | Open | DCO clock delay<br>(delay = 2500 ps × register value/31)<br>00000 = 0 ps<br>00001 = 81 ps<br>00010 = 161 ps<br>…<br>11110 = 2419 ps<br>11111 = 2500 ps | | | | | 0x00 | |
| 0x18 | VREF Select (Global) | Reference voltage selection<br>00 = 1.25 V p-p<br>01 = 1.5 V p-p<br>10 = 1.75 V p-p<br>11 = 2.0 V p-p (default) | | Open | Open | Open | Open | Open | Open | 0xC0 | |
| 0x24 | BIST Signature LSB (Local) | BIST signature [7:0] | | | | | | | | 0x00 | Read only. |
| 0x25 | BIST Signature MSB (Local) | BIST signature [15:8] | | | | | | | | 0x00 | Read only. |
| **Digital Feature Control Registers** | | | | | | | | | | | |
| 0x100 | Sync Control (Global) | Signal monitor sync enable | Open | Open | Open | Open | Clock divider next sync only | Clock divider sync enable | Master sync enable | 0x00 | |
| 0x104 | Fast Detect Control (Local) | Open | Open | Open | Open | Fast Detect Mode Select [2:0] | | | Fast detect enable | 0x00 | |
| 0x105 | Coarse Upper Threshold (Local) | Open | Open | Open | Open | Open | Coarse Upper Threshold [2:0] | | | 0x00 | |
| 0x106 | Fine Upper Threshold Register 0 (Local) | Fine Upper Threshold [7:0] | | | | | | | | 0x00 | |
| 0x107 | Fine Upper Threshold Register 1 (Local) | Open | Open | Open | Fine Upper Threshold [12:8] | | | | | 0x00 | |
| 0x108 | Fine Lower Threshold Register 0 (Local) | Fine Lower Threshold [7:0] | | | | | | | | 0x00 | |
| 0x109 | Fine Lower Threshold Register 1 (Local) | Open | Open | Open | Fine Lower Threshold [12:8] | | | | | 0x00 | |

| Addr (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | Default Notes/ Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x10A | Increase Gain Dwell Time Register 0 (Local) | Increase Gain Dwell Time [7:0] | | | | | | | | 0x00 | In ADC clock cycles. |
| 0x10B | Increase Gain Dwell Time Register 1 (Local) | Increase Gain Dwell Time [15:8] | | | | | | | | 0x00 | In ADC clock cycles. |
| 0x10C | Signal Monitor DC Correction Control (Global) | Open | DC correction freeze | DC Correction Bandwidth [3:0] | | | | DC correction for signal path enable | DC correction for signal monitor enable | 0x00 | |
| 0x10D | Signal Monitor DC Value Channel A Register 0 (Global) | DC Value Channel A [7:0] | | | | | | | | | Read only. |
| 0x10E | Signal Monitor DC Value Channel A Register 1 (Global) | Open | Open | DC Value Channel A [13:8] | | | | | | | Read only. |
| 0x10F | Signal Monitor DC Value Channel B Register 0 (Global) | DC Value Channel B [7:0] | | | | | | | | | Read only. |
| 0x110 | Signal Monitor DC Value Channel B Register 1 (Global) | Open | Open | DC Value Channel B [13:8] | | | | | | | Read only |
| 0x111 | Signal Monitor SPORT Control (Global) | Open | RMS/MS magnitude output enable | Peak detector output enable | Threshold crossing output enable | SPORT SMI SCLK divide<br>00 = undefined<br>01 = divide by 2<br>10 = divide by 4<br>11 = divide by 8 | | SPORT SMI SCLK sleep | Signal monitor SPORT output enable | 0x04 | |
| 0x112 | Signal Monitor Control (Global) | Complex power calculation mode enable | Open | Open | Open | Signal monitor rms/ms select<br>0 = rms<br>1 = ms | Signal monitor mode<br>00 = rms/ms magnitude<br>01 = peak power<br>10 = threshold crossing<br>11 = threshold crossing | | Signal monitor enable | 0x00 | |
| 0x113 | Signal Monitor Period Register 0 (Global) | Signal Monitor Period [7:0] | | | | | | | | 0x40 | In ADC clock cycles. |
| 0x114 | Signal Monitor Period Register 1 (Global) | Signal Monitor Period [15:8] | | | | | | | | 0x00 | In ADC clock cycles. |
| 0x115 | Signal Monitor Period Register 2 (Global) | Signal Monitor Period [23:16] | | | | | | | | 0x00 | In ADC clock cycles. |
| 0x116 | Signal Monitor Result Channel A Register 0 (Global) | Signal Monitor Result Channel A [7:0] | | | | | | | | | Read only. |
| 0x117 | Signal Monitor Result Channel A Register 1 (Global) | Signal Monitor Result Channel A [15:8] | | | | | | | | | Read only. |

| Addr (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | Default Notes/ Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x118 | Signal Monitor Result Channel A Register 2 (Global) | Open | Open | Open | Open | Signal Monitor Value Channel A [19:16] | | | | | Read only. |
| 0x119 | Signal Monitor Result Channel B Register 0 (Global) | Signal Monitor Result Channel B [7:0] | | | | | | | | | Read only. |
| 0x11A | Signal Monitor Result Channel B Register 1 (Global) | Signal Monitor Result Channel B [15:8] | | | | | | | | | Read only. |
| 0x11B | Signal Monitor Result Channel B Register 2 (Global) | Open | Open | Open | Open | Signal Monitor Result Channel B [19:16] | | | | | Read only. |

## MEMORY MAP REGISTER DESCRIPTION

For information about functions controlled in Register 0x00 to Register 0xFF, see Application Note AN-877, *Interfacing to High Speed ADCs via SPI*.

### *Sync Control (Register 0x100)*

**Bit 7—Signal Monitor Sync Enable**

Bit 7 enables the sync pulse from the external sync input to the signal monitor block. The sync signal is passed when both Bit 7 and Bit 0 are high. This is continuous sync mode.

**Bits [6:3]—Reserved**

**Bit 2—Clock Divider Next Sync Only**

If the master sync enable bit (Address 0x100 [0]) is high and the clock divider sync enable bit (Address 0x100 [1]) is high, the clock divider next sync only bit (Address 0x100 [2]) allows the clock divider to sync to the first sync pulse it receives and ignore the rest. The clock divider sync enable bit (Address 0x100 [1]) resets after it syncs.

**Bit 1—Clock Divider Sync Enable**

Bit 1 gates the sync pulse to the clock divider. The sync signal is passed when both Bit 1 and Bit 0 are high. This is continuous sync mode.

**Bit 0—Master Sync Enable**

Bit 0 must be high to enable the sync functions.

### *Fast Detect Control (Register 0x104)*

**Bits [7:4]—Reserved**

**Bits [3:1]—Fast Detect Mode Select**

These bits set the mode of the fast detect output pins according to Table 14.

**Bit 0—Fast Detect Enable**

Bit 0 is used to enable the fast detect output pins. When the fast detect output pins are disabled, the outputs go into a high impedance state. In LVDS mode, when the fast detect output pins are interleaved, the outputs go high-Z only if both channels are turned off (power-down/standby/output disabled). If only one channel is turned off (power-down/standby/output disabled), the fast detect output pins repeat the data of the active channel.

### *Coarse Upper Threshold (Register 0x105)*

**Bits [7:3]—Reserved**

**Bits [2:0]—Coarse Upper Threshold**

These bits set the level required to assert the coarse upper threshold indication (see Table 18).

### *Fine Upper Threshold (Register 0x106 and Register 0x107)*

**Register 0x106, Bits [7:0]—Fine Upper Threshold [7:0]**

**Register 0x107, Bits [7:5]—Reserved**

**Register 0x107, Bits [4:0]—Fine Upper Threshold [12:8]**

These registers provide the fine upper limit threshold. This 13-bit value is compared with the 10-bit magnitude from the ADC block. If the ADC magnitude exceeds this threshold value, the F_UT indicator is set.

### *Fine Lower Threshold (Register 0x108 and Register 0x109)*

**Register 0x108, Bits [7:0]—Fine Lower Threshold [7:0]**
**Register 0x109, Bits [7:5]—Reserved**
**Register 0x109, Bits [4:0]—Fine Lower Threshold [12:8]**

These registers provide a fine lower limit threshold. This 13-bit value is compared with the 10-bit magnitude from the ADC block. If the ADC magnitude is less than this threshold value, the F_LT indicator is set.

### *Increase Gain Dwell Time (Register 0x10A and Register 0x10B)*

**Register 0x10A, Bits [7:0]—Increase Gain Dwell Time [7:0]**
**Register 0x10B, Bits [7:0]—Increase Gain Dwell Time [15:8]**

These registers are programmed with the dwell time in ADC clock cycles. The signal must be below the fine lower threshold value before the increase gain (IG) indicator is asserted.

### *Signal Monitor DC Correction Control (Register 0x10C)*

**Bit 7—Reserved**

**Bit 6—DC Correction Freeze**

When Bit 6 is set high, the dc correction is not updated to the signal monitor block; therefore, the block continues to hold the last dc value that it calculated.

**Bits [5:2]—DC Correction Bandwidth**

These bits set the averaging time of the power monitor dc correction function. This 4-bit word sets the bandwidth of the correction block according to the following equation:

$$DC\_Corr\_BW = 2^{-k-14} \times \frac{f_{CLK}}{2 \times \pi}$$

where:
*k* is the 4-bit value programmed in Register 0x10C, Bits [5:2] (values between 0 and 13 are valid for k; programming 14 or 15 provides the same result as programming 13).
$f_{CLK}$ is the AD9600 ADC sample rate in hertz.

**Bit 1—DC Correction for Signal Path Enable**

Setting Bit 1 high causes the output of the dc measurement block to be summed with the data in the signal path to remove the dc offset from the signal path.

**Bit 0—DC Correction for Signal Monitor Enable**

Bit 0 enables the dc correction function in the signal monitor block. The dc correction is an averaging function that can be used by the signal monitor to remove dc offset in the signal. Removing this dc from the measurement allows a more accurate reading.

### *Signal Monitor DC Value Channel A (Register 0x10D and Register 0x10E)*

**Register 0x10D, Bits [7:0]—DC Value Channel A [7:0]**

**Register 0x10E, Bits [7:6]—Reserved**

**Register 0x10E, Bits [5:0]—DC Value Channel A [13:8]**

These read-only registers hold the latest dc offset value computed by the signal monitor for Channel A.

### *Signal Monitor DC Value Channel B (Register 0x10F and Register 0x110)*

**Register 0x10F Bits [7:0]—DC Value Channel B [7:0]**

**Register 0x110 Bits [7:6]—Reserved**

**Register 0x110 Bits [5:0]—DC Value Channel B [13:8]**

These read-only registers hold the latest dc offset value computed by the signal monitor for Channel B.

### *Signal Monitor SPORT Control (Register 0x111)*

**Bit 7—Reserved**

**Bit 6—RMS/MS Magnitude Output Enable**

These bits enable the 20-bit rms or ms magnitude measurement as output on the SPORT.

**Bit 5—Peak Detector Output Enable**

Bit 5 enables the 10-bit peak measurement as output on the SPORT.

**Bit 4—Threshold Crossing Output Enable**

Bit 4 enables the 10-bit threshold measurement as output on the SPORT.

**Bits [3:2]—SPORT SMI SCLK Divide**

The values of these bits set the SPORT SMI SCLK divide ratio from the input clock. A value of 0x01 sets divide by 2 (default), a value of 0x10 sets divide by 4, and a value of 0x11 sets divide by 8.

**Bit 1— SPORT SMI SCLK Sleep**

Setting Bit 1 high causes the SMI SCLK to remain low when the signal monitor block has no data to transfer.

**Bit 0—Signal Monitor SPORT Output Enable**

When set, Bit 0 enables the SPORT output of the signal monitor to begin shifting out the result data from the signal monitor block.

### *Signal Monitor Control (Register 0x112)*

**Bit 7—Complex Power Calculation Mode Enable**

This mode assumes that I data is present on one channel and Q data is present on the opposite channel. The result reported is the complex power, measured as

$$\sqrt{I^2 + Q^2}$$

**Bits [6:4]—Reserved**

**Bit 3—Signal Monitor RMS/MS Select**

Setting Bit 3 low selects rms power measurement mode. Setting Bit 3 high selects ms power measurement mode.

**Bits [2:1]—Signal Monitor Mode**

Bit 2 and Bit 1 set the mode of the signal monitor for the data output of Register 0x116 to Register 0x11B. Setting Bit 2 and Bit 1 to 00 selects rms/ms magnitude output, setting these bits to 01 selects peak power output, and setting to 10 or 11 selects threshold crossing output.

**Bit 0—Signal Monitor Enable**

Setting Bit 0 high enables the signal monitor block.

### *Signal Monitor Period (Register 0x113 to Register 0x115)*

**Register 0x113, Bits [7:0]—Signal Monitor Period [7:0]**

**Register 0x114, Bits [7:0]—Signal Monitor Period [15:8]**

**Register 0x115, Bits [7:0]—Signal Monitor Period [23:16]**

This 24-bit value sets the number of clock cycles over which the signal monitor performs its operation. Although this register defaults to 64 (0x40), the minimum value for this register is 128 (0x80) cycles—writing values less than 128 can cause inaccurate results.

### *Signal Monitor Result Channel A (Register 0x116 to Register 0x118)*

**Register 0x116, Bits [7:0]—Signal Monitor Result Channel A [7:0]**

**Register 0x117, Bits [7:0]—Signal Monitor Result Channel A [15:8]**

**Register 0x118, Bits [7:4]—Reserved**

**Register 0x118, Bits [3:0]—Signal Monitor Result Channel A [19:16]**

This 20-bit value contains the result calculated by the signal monitoring block for Channel A. The content is dependent on the settings in Bits [2:1] of Register 0x112.

### *Signal Monitor Result Channel B (Register 0x119 to Register 0x11B)*

**Register 0x119, Bits [7:0]— Signal Monitor Result Channel B [7:0]**

**Register 0x11A, Bits [7:0]—Signal Monitor Result Channel B [15:8]**

**Register 0x11B, Bits [7:4]—Reserved**

**Register 0x11B, Bits [3:0]—Signal Monitor Result Channel B [19:16]**

This 20-bit value contains the result calculated by the signal monitoring block for Channel B. The content is dependent on the settings in Bits [2:1] of Register 0x112.

# APPLICATIONS INFORMATION

## DESIGN GUIDELINES

When designing the AD9600 into a system, the designer should, before starting design and layout, become familiar with these guidelines, which discuss the special circuit connections and layout requirements for certain pins.

### *Power and Ground Recommendations*

When connecting power to the AD9600, the designer should use two separate 1.8 V supplies: one supply should be used for AVDD and DVDD and a separate supply for DRVDD. The AVDD and DVDD supplies, although derived from the same source, should be isolated with a ferrite bead or filter choke and have separate decoupling capacitors. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the part's pins with minimal trace length.

A single PC board ground plane should be sufficient when using the AD9600. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance can be easily achieved.

### *Exposed Paddle Thermal Heat Slug Recommendations*

To achieve the best electrical and thermal performance of the AD9600, the exposed paddle on the underside of the ADC must be connected to analog ground (AGND). A continuously exposed (no solder mask) copper plane on the PCB should mate to the exposed paddle, Pin 0, of the AD9600. In addition, the copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB, and these vias should be filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and PCB. See the evaluation board layout figures (Figure 84 to Figure 91) for an example of a PCB layout. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

### *CML*

The CML pin should be decoupled to ground with a 0.1 µF capacitor, as shown in Figure 47.

### *RBIAS*

The AD9600 requires the user to place a 10 kΩ resistor between the RBIAS pin and ground. This register sets the master current reference of the ADC core and should have at least a 1% tolerance.

### *Reference Decoupling*

The VREF pin should be externally decoupled to ground with a low-ESR 1.0 µF capacitor in parallel with a 0.1 µF ceramic low-ESR capacitor.

### *SPI Port*

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade the converter's performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9600 in order to keep these signals from transitioning at the converter inputs during critical sampling periods.

# EVALUATION BOARD

The AD9600 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially using the double-balun configuration (default) or an AD8352 differential driver. The ADC can also be driven in a single-ended fashion. Separate power pins are provided to isolate the DUT from the AD8352 drive circuitry. Each input configuration can be selected by properly connecting various components (see Figure 74 to Figure 83). Figure 73 shows the typical bench characterization setup used to evaluate the ac performance of the AD9600.

It is critical that the signal sources used for the analog input and clock have very low phase noise (<<1 ps rms jitter) to realize the optimum performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 74 to Figure 91 for the complete schematics and layout diagrams that demonstrate the routing and grounding techniques that should be applied at the system level.

## POWER SUPPLIES

The evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The output of the supply is a 2.1 mm inner diameter circular jack that connects to the PCB at J16. Once on the PC board, the 6 V supply is fused and conditioned before connecting to six low dropout linear regulators that supply the proper bias to each of the various sections of the board.

The evaluation board can be operated using external supplies by removing L1, L3, L4, and L13 to disconnect the voltage regulators supplied from the switching power supply. This enables the user to individually bias each section of the board. Use P3 and P4 to connect a different supply for each section. At least one 1.8 V supply is needed with a 1 A current capability for AVDD and DVDD; a separate 1.8 V to 3.3 V supply is recommended for DRVDD. To operate the evaluation board using the AD8352 driver, a separate 5.0 V supply (AMP VDD) with a 1 A current capability is needed. To operate the evaluation board using the alternative SPI options, a separate 3.3 V analog supply (VS) is needed in addition to the other supplies. The 3.3 V supply (VS) should also have a 1 A current capability. Using Solder Jumper SJ35 allows the user to separate AVDD and DVDD if desired.

## INPUT SIGNALS

When connecting the clock and analog sources to the evaluation board, use clean signal generators with low phase noise, such as Rohde & Schwarz SMA100A or Agilent HP8644 signal generators or the equivalent, as well as a 1 m, shielded, RG-58, 50 Ω coaxial cable. Enter the desired frequency and amplitude for the ADC. The AD9600 evaluation board from Analog Devices can accept a ~2.8 V p-p or a 13 dBm sine wave input for the clock. When connecting the analog input source, it is recommended to use a multipole, narrow-band, band-pass filter with 50 Ω terminations. Good choices of such band-pass filters are available from TTE, Allen Avionics, and K&L Microwave, Inc. Connect the filter directly to the evaluation board, if possible.

## OUTPUT SIGNALS

The parallel CMOS outputs interface directly with the Analog Devices standard ADC data capture board (HSC-ADC-EVALCZ). For more information on the ADC data capture boards and their optional settings, visit www.analog.com/FIFO.

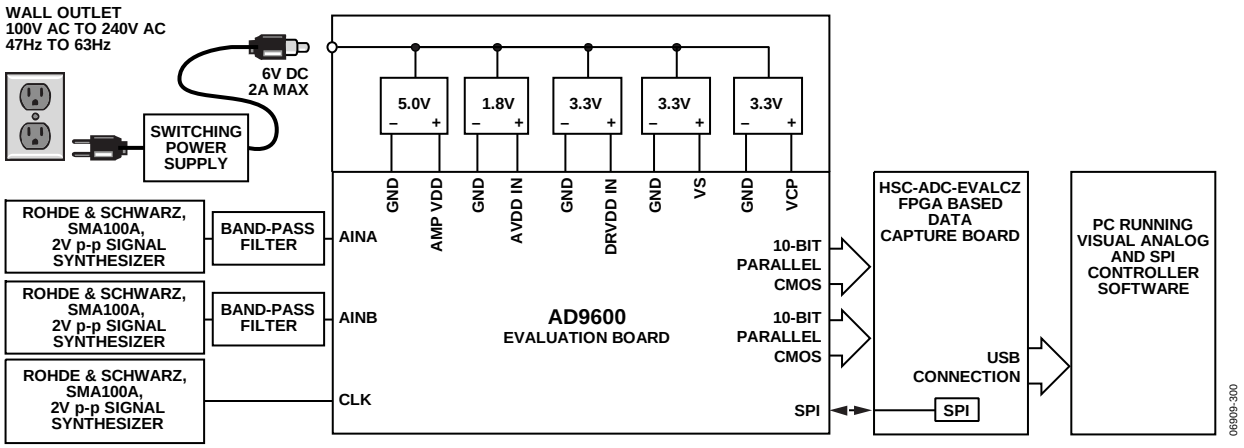



*Figure 73. Evaluation Board Connection*

## DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

The following is a list of the default and optional settings, or modes, allowed on the AD9600 evaluation board.

### *POWER*

Connect the switching power supply that is provided with the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P500.

### *VIN*

The evaluation board is set up for a double-balun configuration analog input with an optimum 50 Ω impedance matching from 70 MHz to 200 MHz. For more bandwidth response, the differential capacitor across the analog inputs can be changed or removed (see Table 10). The common mode of the analog inputs is developed from the center tap of the transformer via the CML pin of the ADC (see the Analog Input Considerations section).

### *VREF*

VREF is set to 1.0 V by tying the SENSE pin to ground and adding a jumper on Header J5 (Pin 1 to Pin 2). This causes the ADC to operate in the 2.0 V p-p full-scale range. To place the ADC in the 1.0 V p-p mode (VREF = 0.5 V), a jumper should be placed on Header J4. A separate external reference option is also included on the evaluation board. To use an external reference, connect Pin 1 of J6 to Pin 2 of J6 and provide an external reference at TP5. Proper use of the VREF options is detailed in the Voltage Reference section.

### *RBIAS*

RBIAS requires that a 10 kΩ resistor (R503) be connected to ground. This pin is used to set the ADC core bias current.

### *CLOCK*

The default clock input circuitry is derived from a simple balun-coupled circuit using a high bandwidth 1:1 impedance ratio balun (T5) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave inputs. The transformer converts the single-ended input to a differential signal that is clipped before entering the ADC clock inputs. When the AD9600 input clock divider is used, clock frequencies up to 625 MHz can be input into the evaluation board through Connector S5.

### *PDWN*

To enable the power-down feature, connect J7, shorting the PDWN pin to AVDD.

### *CSB*

The CSB pin is internally pulled up, setting the chip into external pin mode, to ignore the SDIO and SCLK information. To connect the control of the CSB pin to the SPI circuitry on the evaluation board, connect Pin 1 of J21 to Pin 2 of J21.

### *SCLK/DFS*

If the SPI port is in external pin mode, the SCLK/DFS pin sets the data format of the outputs. If the pin is left floating, the pin is internally pulled down, setting the default data format condition to offset binary. Connecting Pin 1 of J2 to Pin 2 of J2 sets the format to twos complement. If the SPI port is in serial pin mode, connecting Pin 2 of J2 to Pin 3 of J2 connects the SCLK pin to the on-board SPI circuitry (see the Serial Port Interface (SPI) section).

### *SDIO/DCS*

If the SPI port is in external pin mode, the SDIO/DCS pin acts to set the duty cycle stabilizer. If the pin is left floating, the pin is internally pulled up, setting the default condition to DCS enabled. To disable the DCS, connect Pin 1 of J1 to Pin 2 of J1. If the SPI port is in serial pin mode, connecting Pin 2 of J1 to Pin 3 of J1 connects the SDIO pin to the on-board SPI circuitry (see the Serial Port Interface (SPI) section).

## ALTERNATIVE CLOCK CONFIGURATIONS

Two clocking options are provided on the AD9600 evaluation board. The first option is to use the on-board crystal oscillator (Y1) to provide the clock input to the part. To enable this crystal, Resistors R8 (0 Ω) and R85 (10 kΩ) should be installed and Resistors R82 and R30 should be removed.

The second option is to use a differential LVPECL clock to drive the ADC input using the AD9516-4 (U2). When using this option, the AD9516-4 charge-pump filter components need to be populated (see Figure 78). Consult the AD9516-4 data sheet for more information.

To configure the clock input (from S5) to drive the AD9516 reference input instead of directly driving the ADC, the following components need to be added, removed, and/or changed.

1. Remove R32, R33, R99, and R101 in the default clock path.
2. Populate C78 and C79 with 0.001 µF capacitors and R78 and R79 with 0 Ω resistors in the clock path.

Additionally, unused AD9516 outputs (one LVDS and one LVPECL) are routed to optional Connectors S8 through S11 on the evaluation board.

## ALTERNATIVE ANALOG INPUT DRIVE CONFIGURATION

This section provides a brief description of the alternative analog input drive configuration using the AD8352. When using this drive option, some additional components need to be populated. For more details on the AD8352 differential driver, including how it works and its optional pin settings, consult the AD8352 data sheet.

To configure the analog input to drive the AD8352 instead of the default transformer option, the following components need to be added, removed, and/or changed for Channel A. In addition, the corresponding components for Channel B should be changed.

1. Remove C1, C17, C18, and C117 in the default analog input path.
2. Populate C8 and C9 with 0.1 µF capacitors in the analog input path. To drive the AD8352 in the differential input mode populate Transformer T10; Resistors R1, R37, R39, R126, and R127; and Capacitors C10, C11, and C125.
3. Populate the optional amplifier output path with the desired components, including an optional low-pass filter. Install 0 Ω Resistors R44 and R48. Resistors R43 and R47 should be increased (typically to 100 Ω) to increase the output impedance seen by the AD8352 to 200 Ω.

## SCHEMATICS

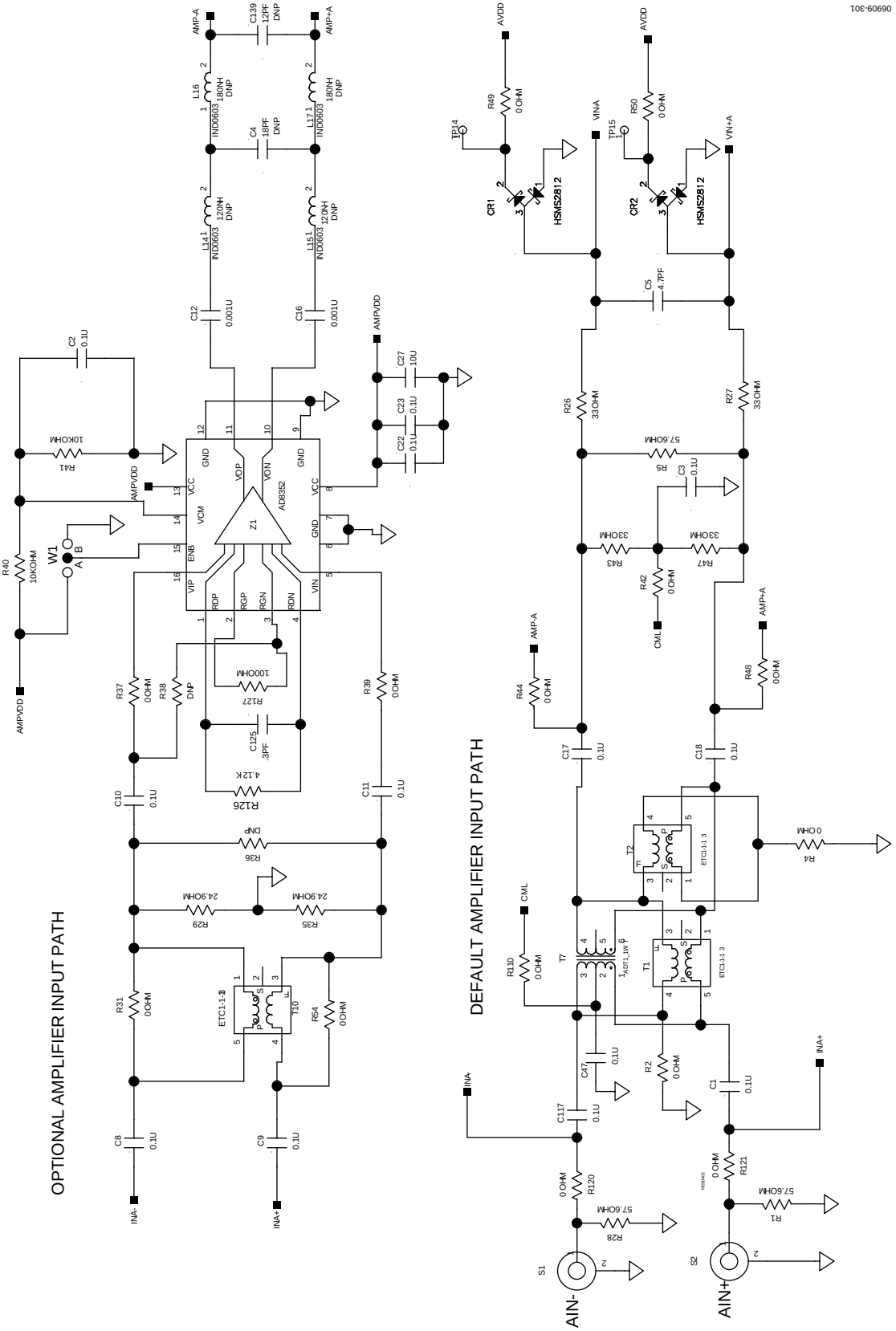



*Figure 74. Evaluation Board Schematic, Channel A Analog Inputs*

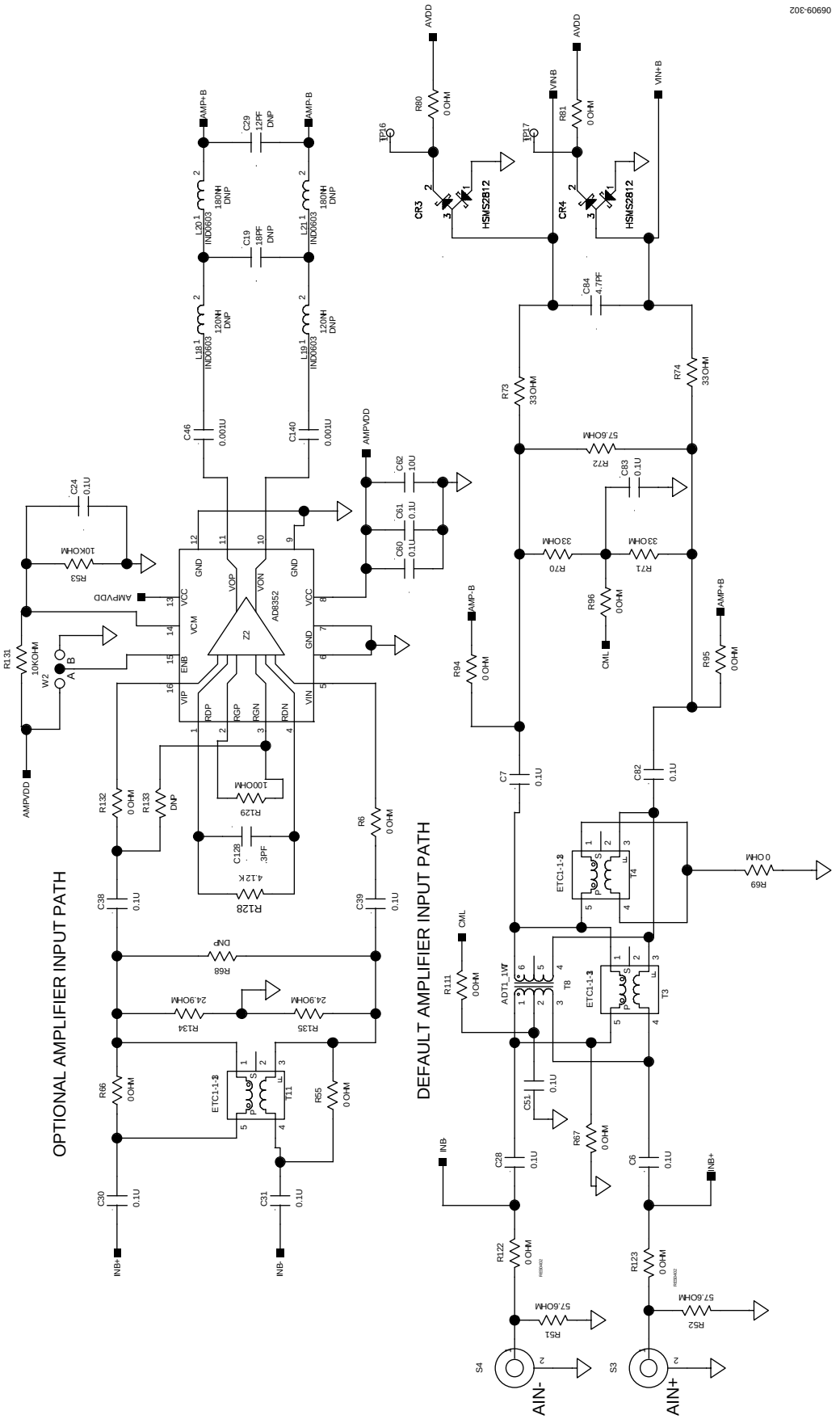



*Figure 75. Evaluation Board Schematic, Channel B Analog Inputs*

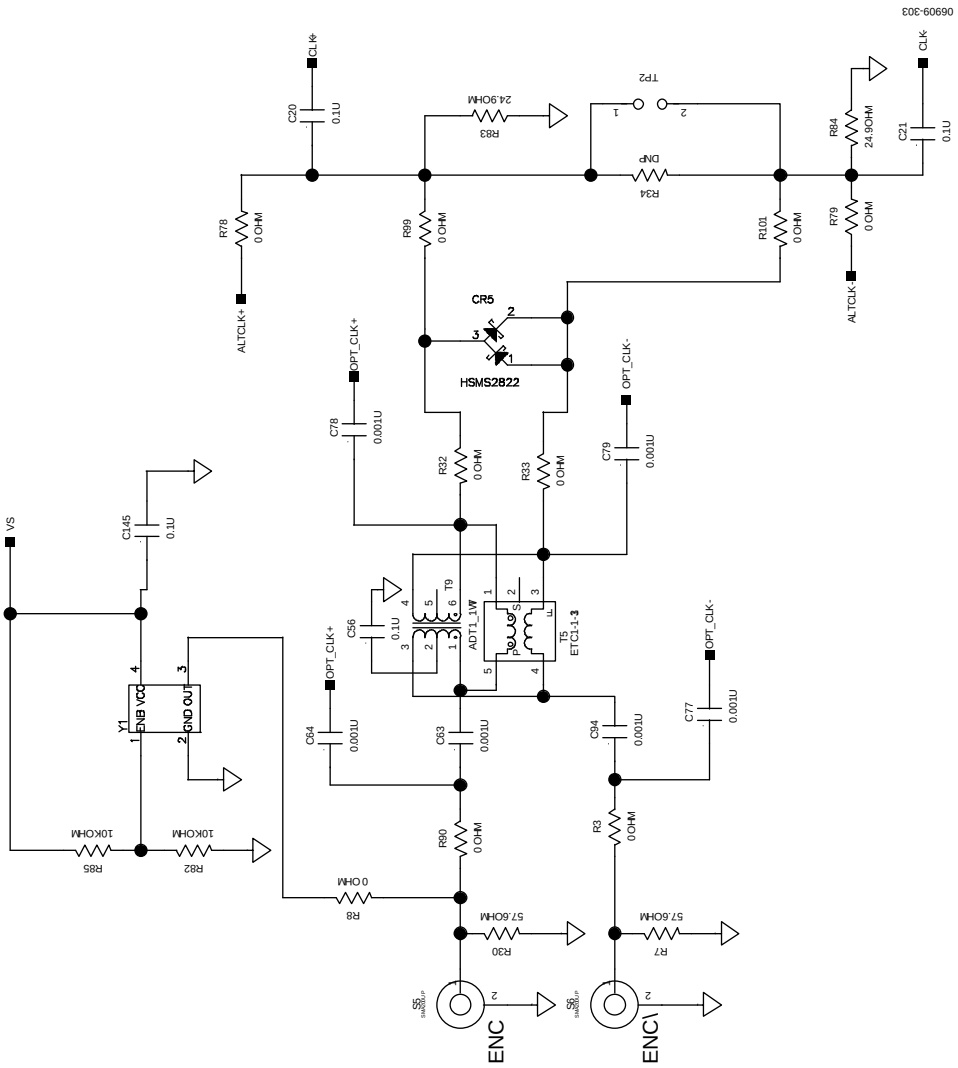



*Figure 76. Evaluation Board Schematic, DUT Clock Input*

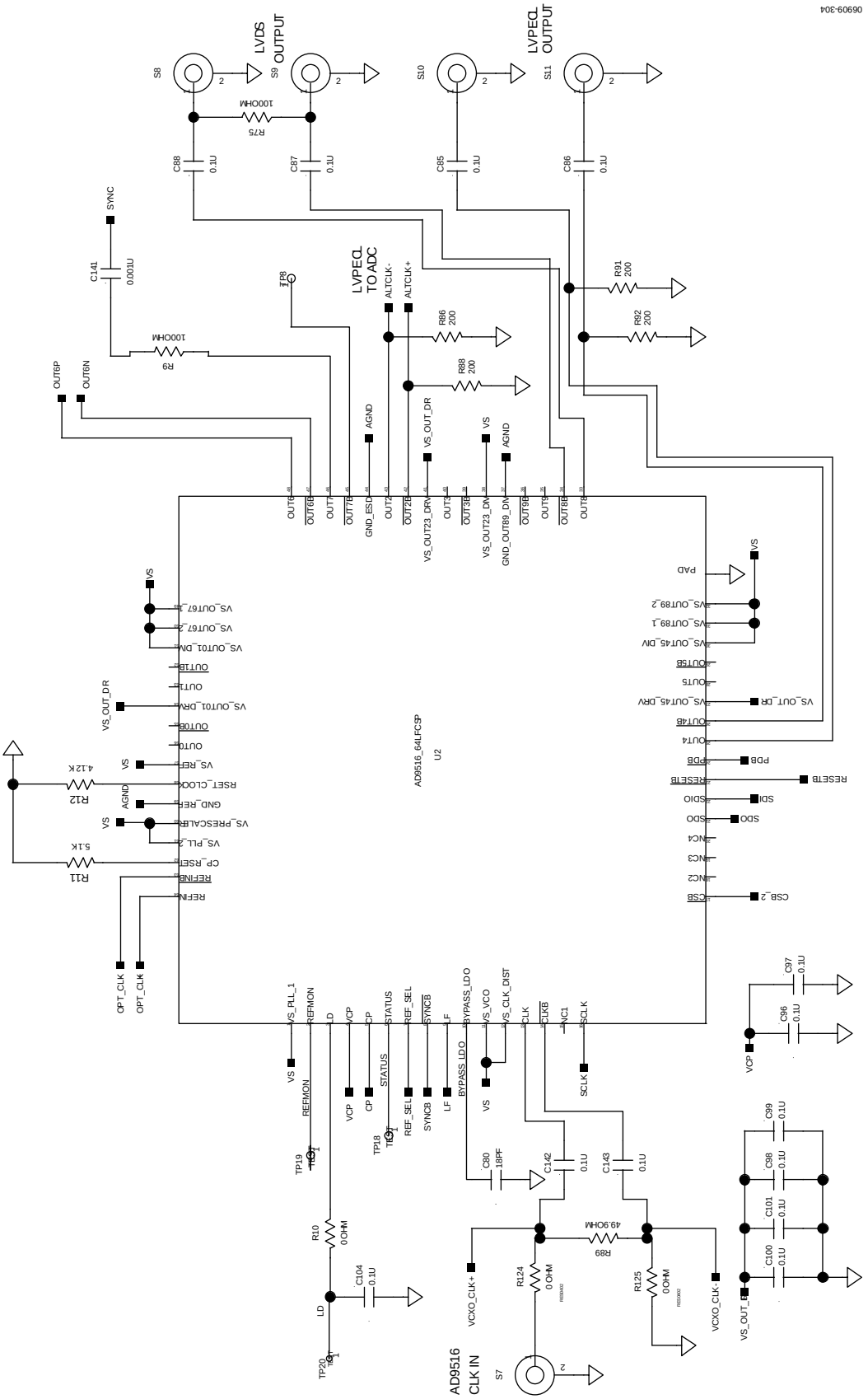



*Figure 77. Evaluation Board Schematic, Optional AD9516 Clock Circuit*

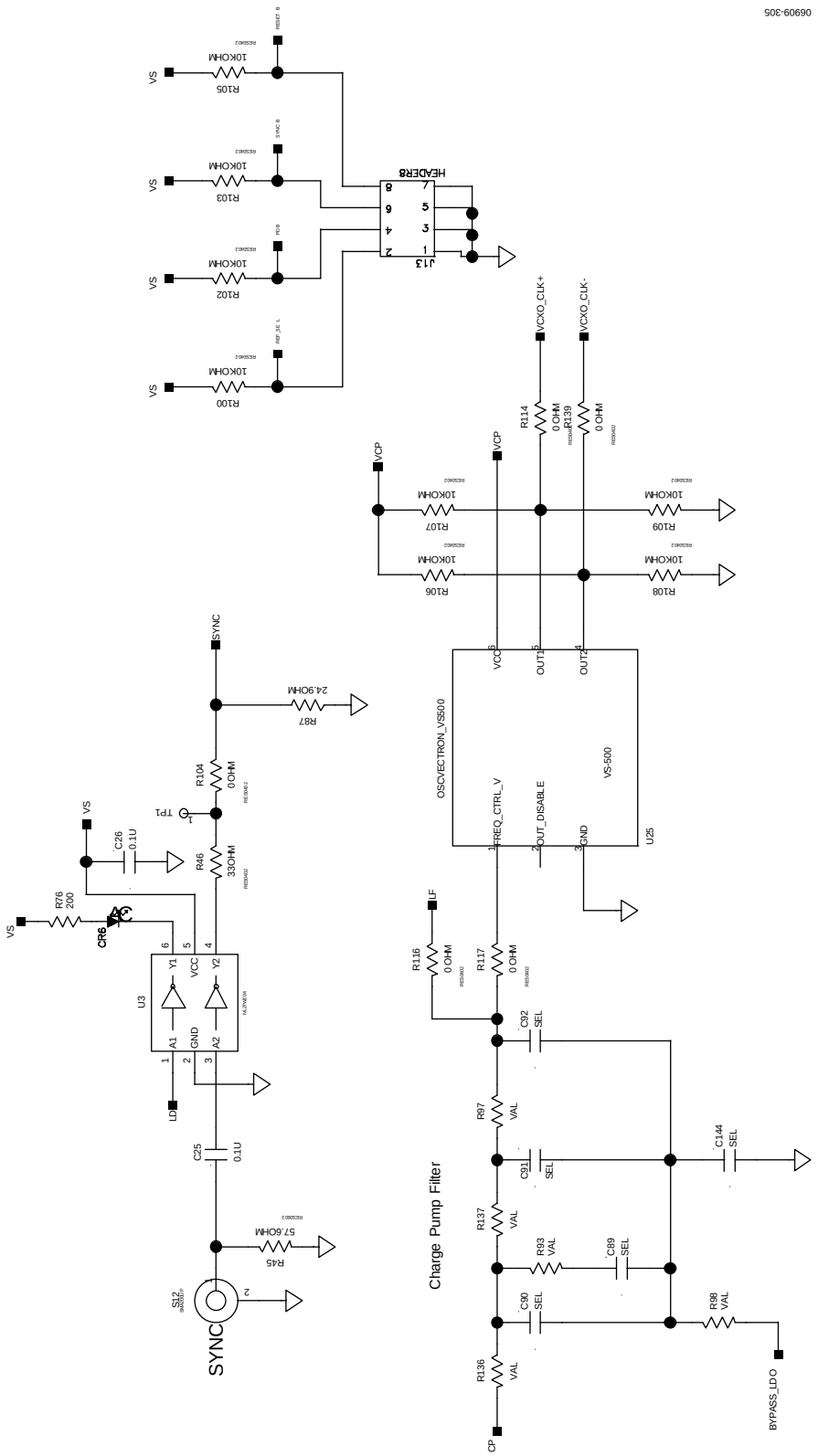



*Figure 78. Evaluation Board Schematic, Optional AD9516 Loop Filter/VCO and SYNC Input*

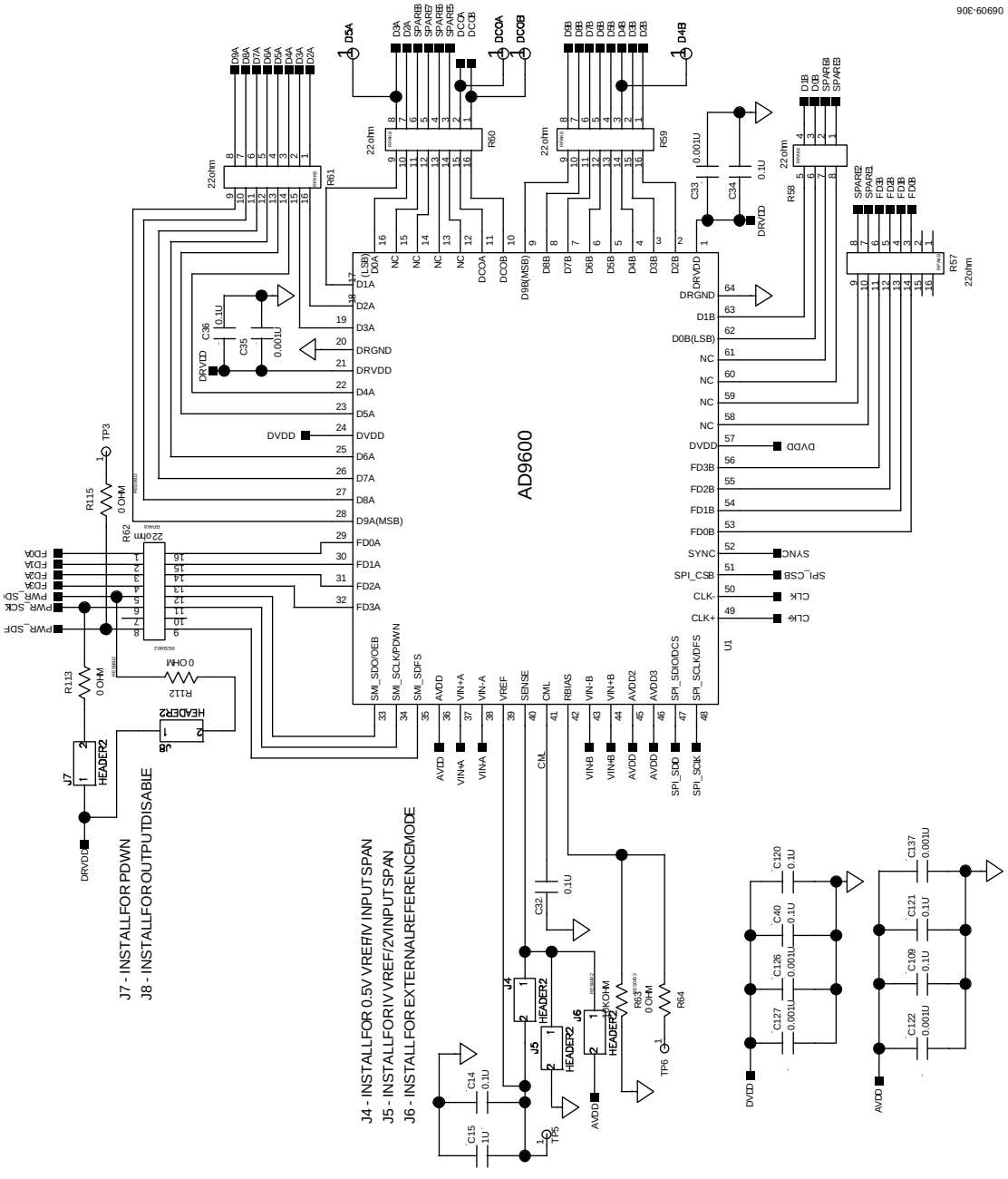



*Figure 79. Evaluation Board Schematic, DUT*

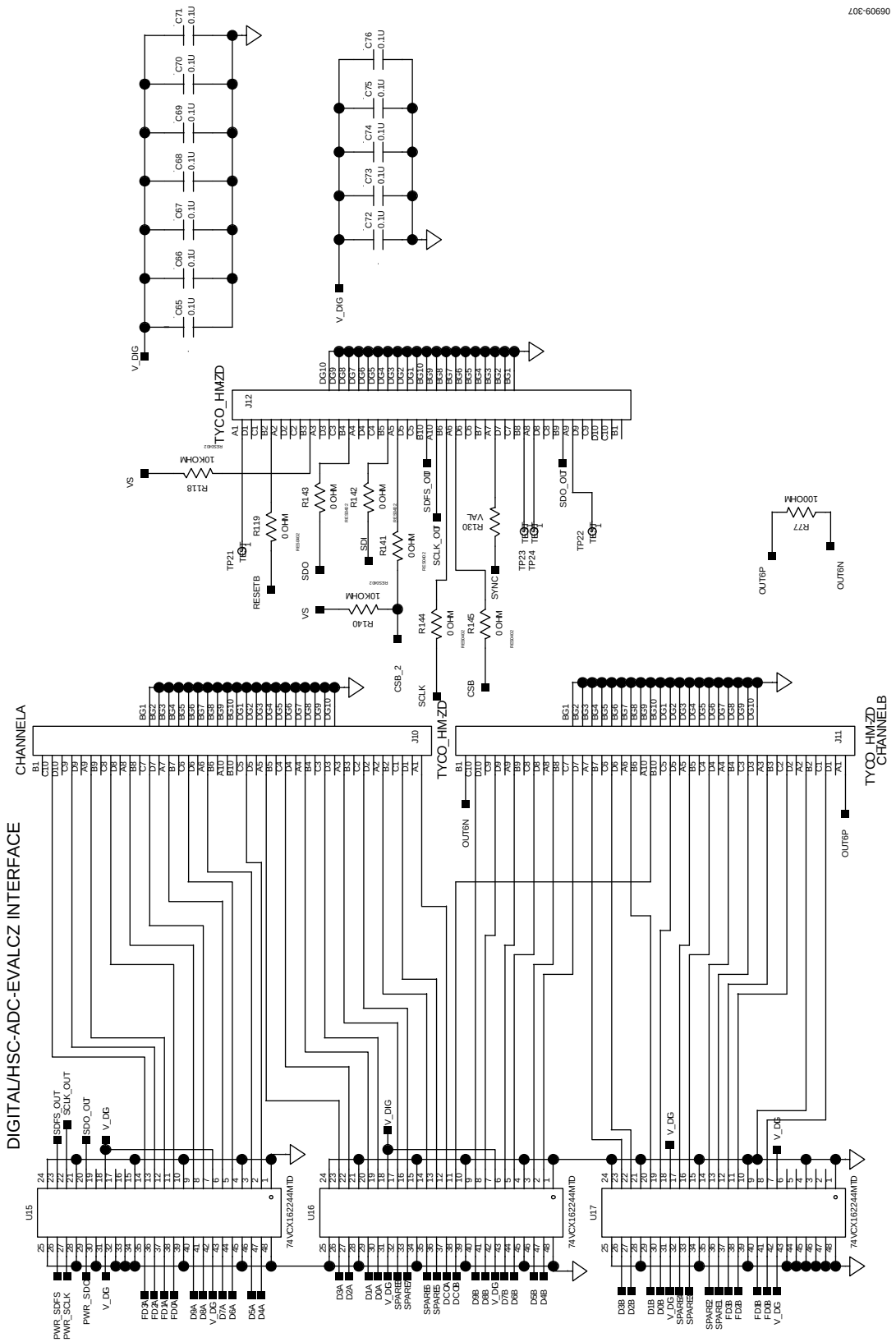



*Figure 80. Evaluation Board Schematic, Digital Output Interface*

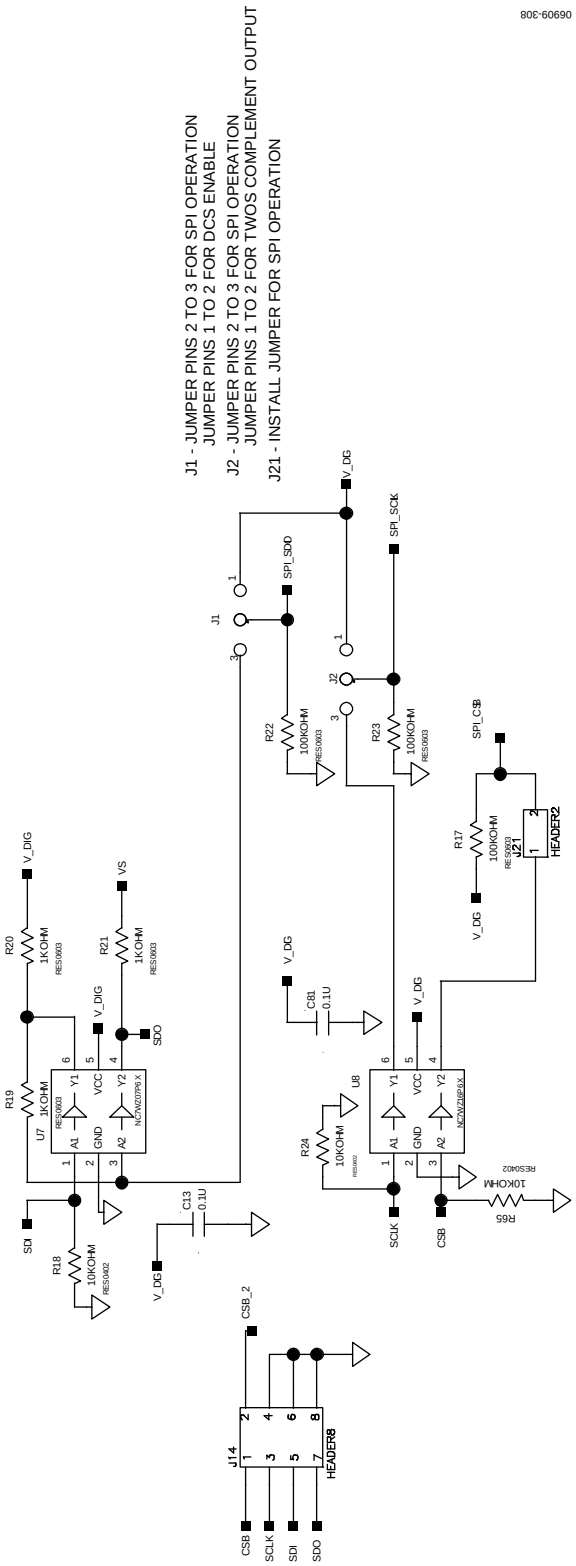



*Figure 81. Evaluation Board Schematic, SPI Circuitry*

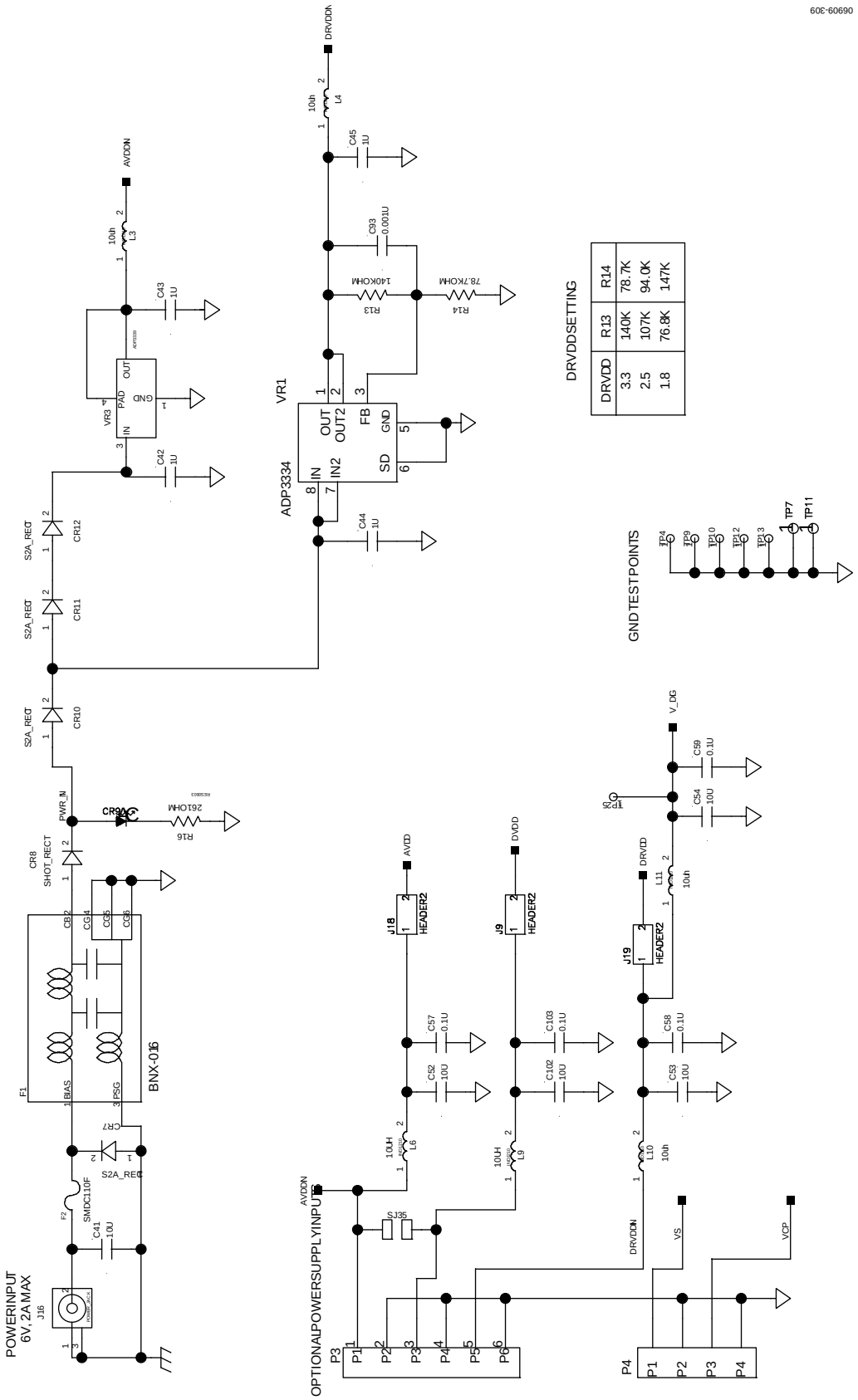



*Figure 82. Evaluation Board Schematic, Power Supply*

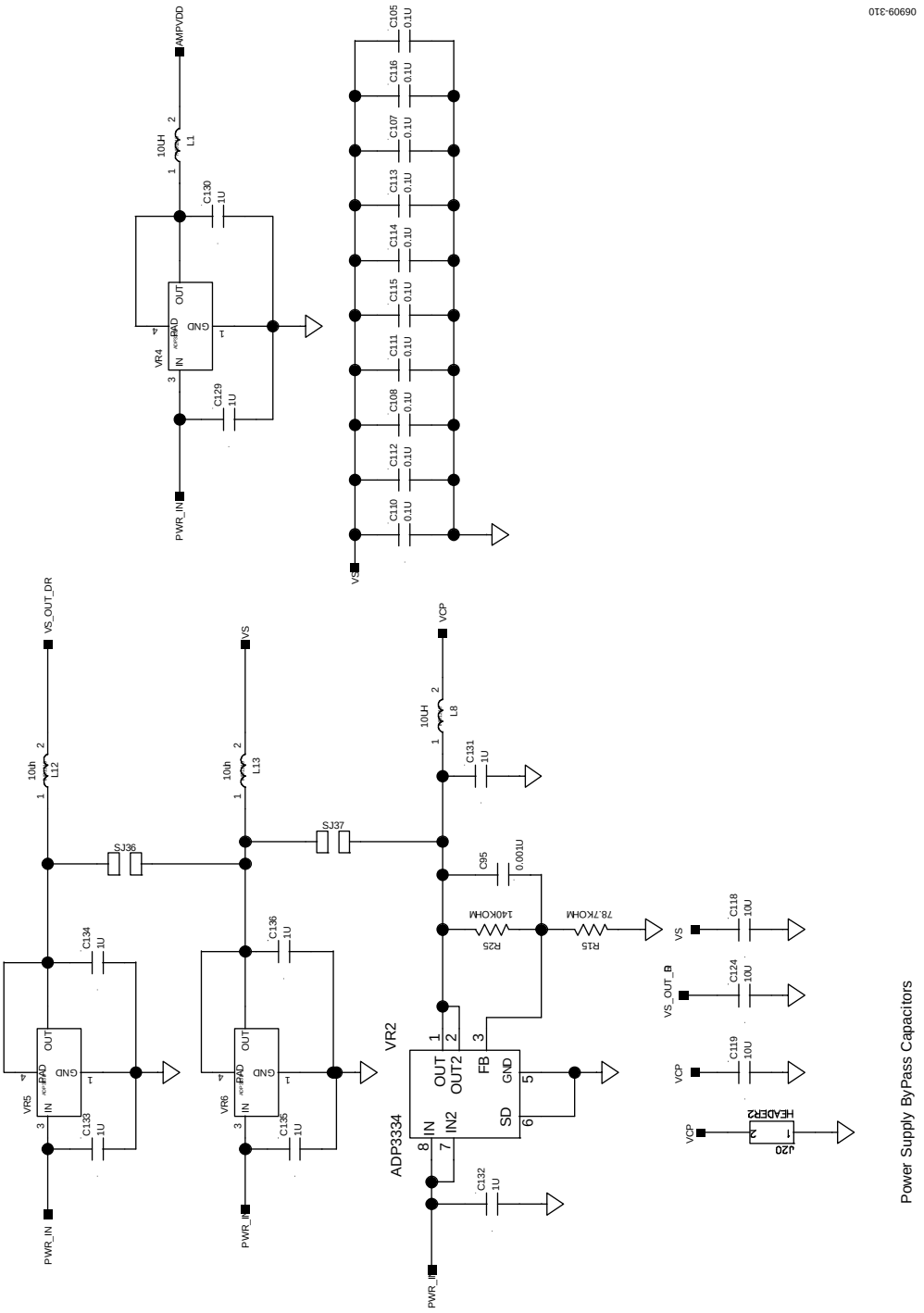



*Figure 83. Evaluation Board Schematic, Power Supply (Continued)*

## EVALUATION BOARD LAYOUTS

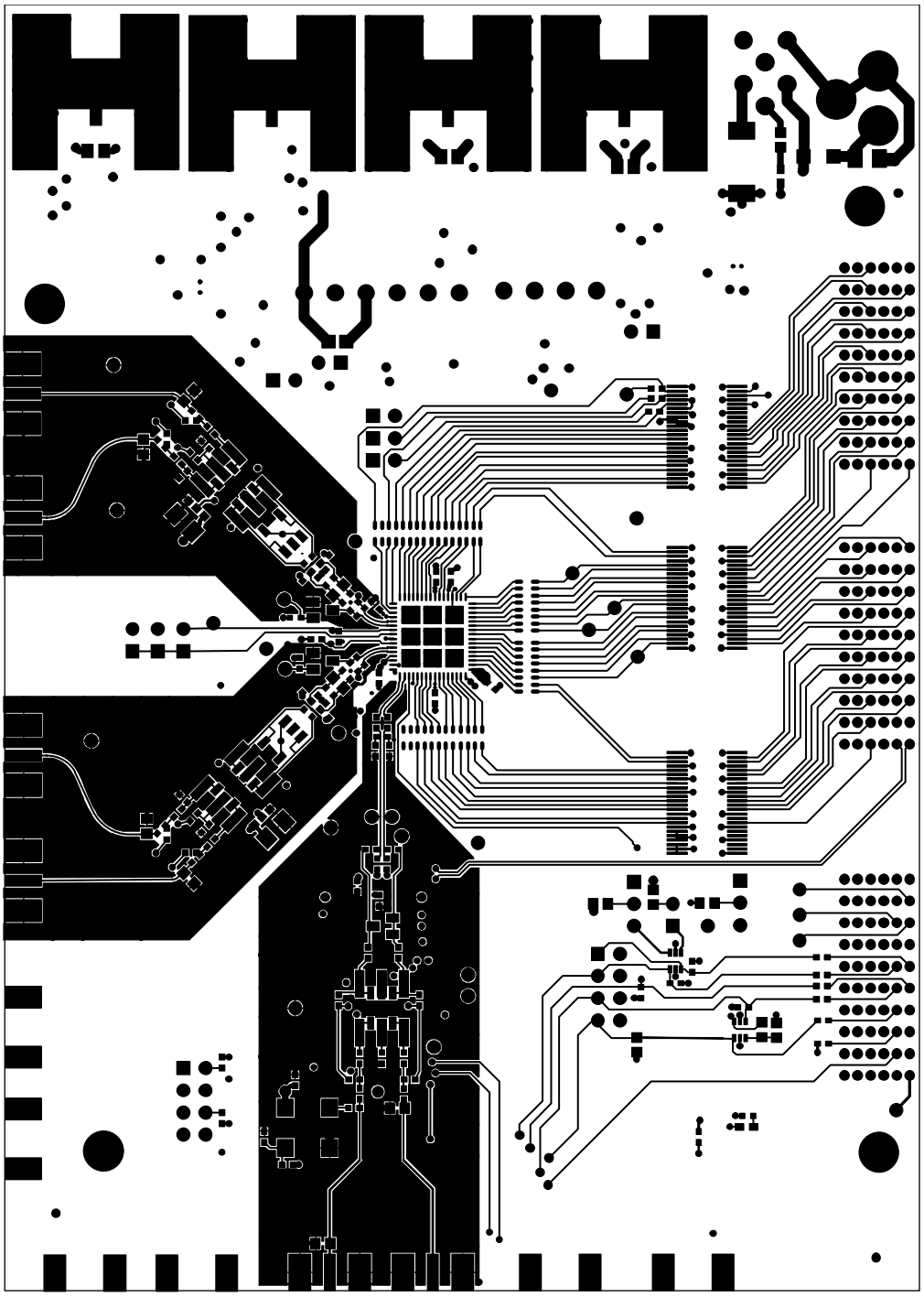



*Figure 84. Evaluation Board Layout, Primary Side*

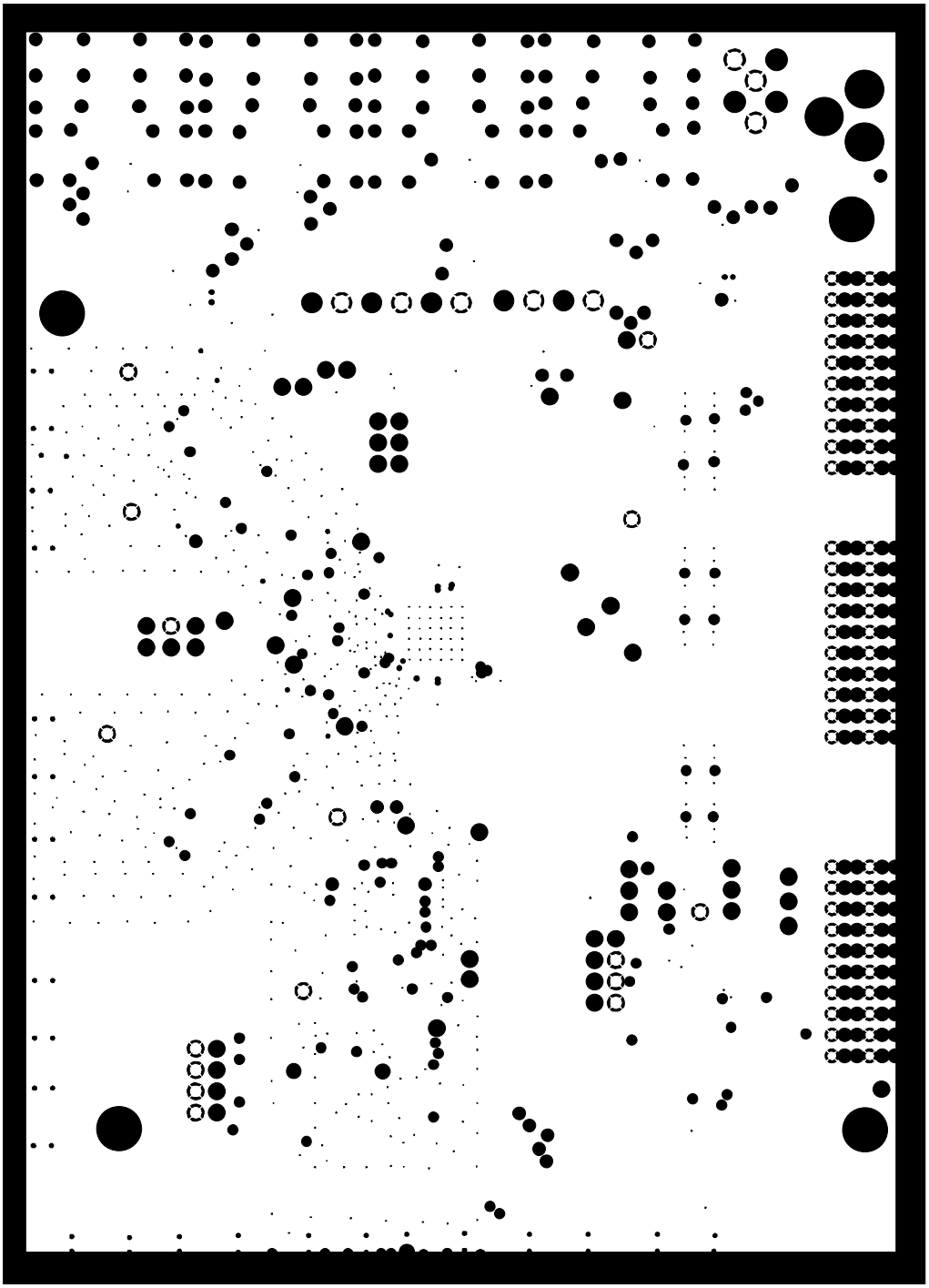



*Figure 85. Evaluation Board Layout, Ground Plane*

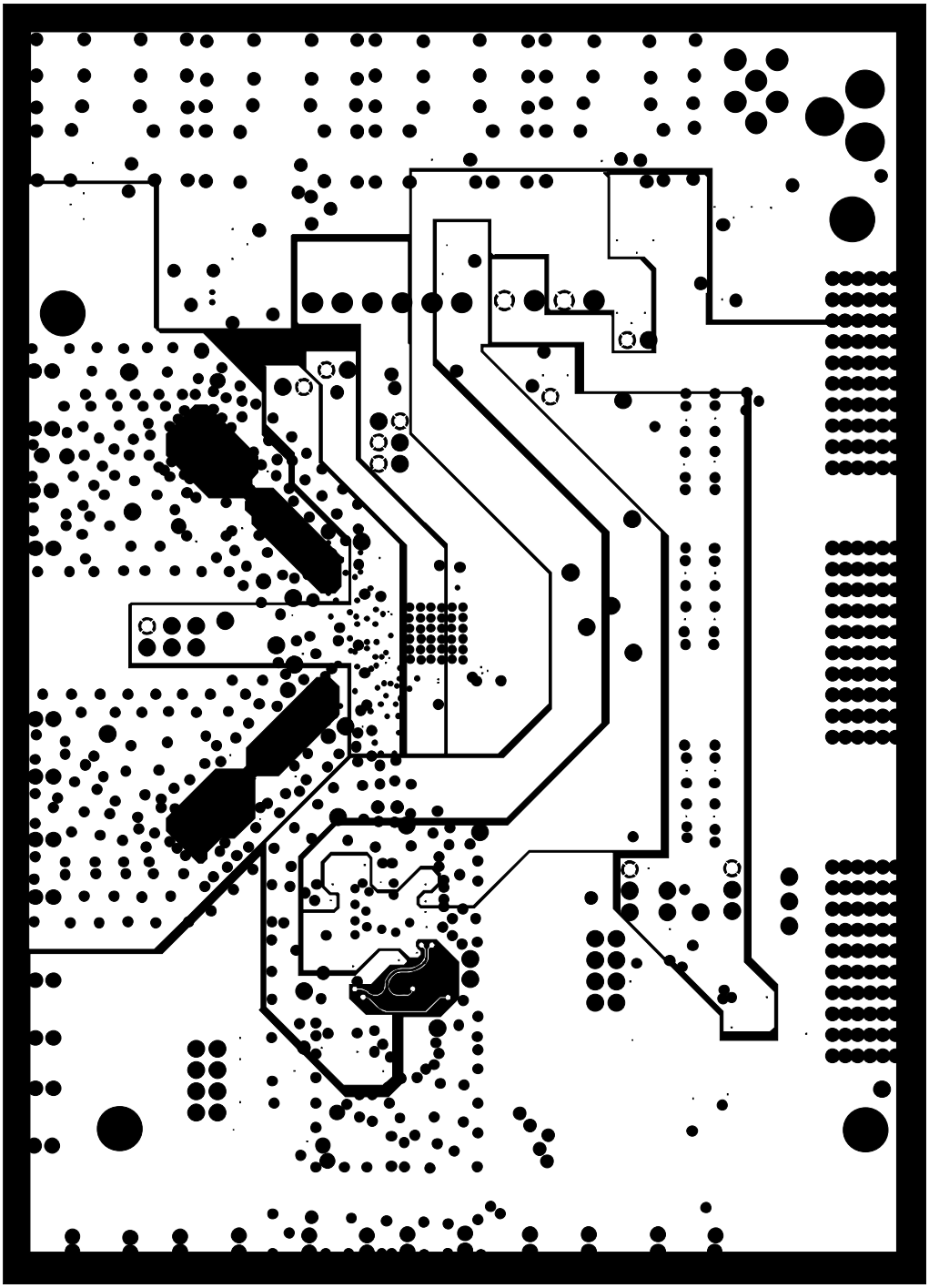



*Figure 86. Evaluation Board Layout, Power Plane*

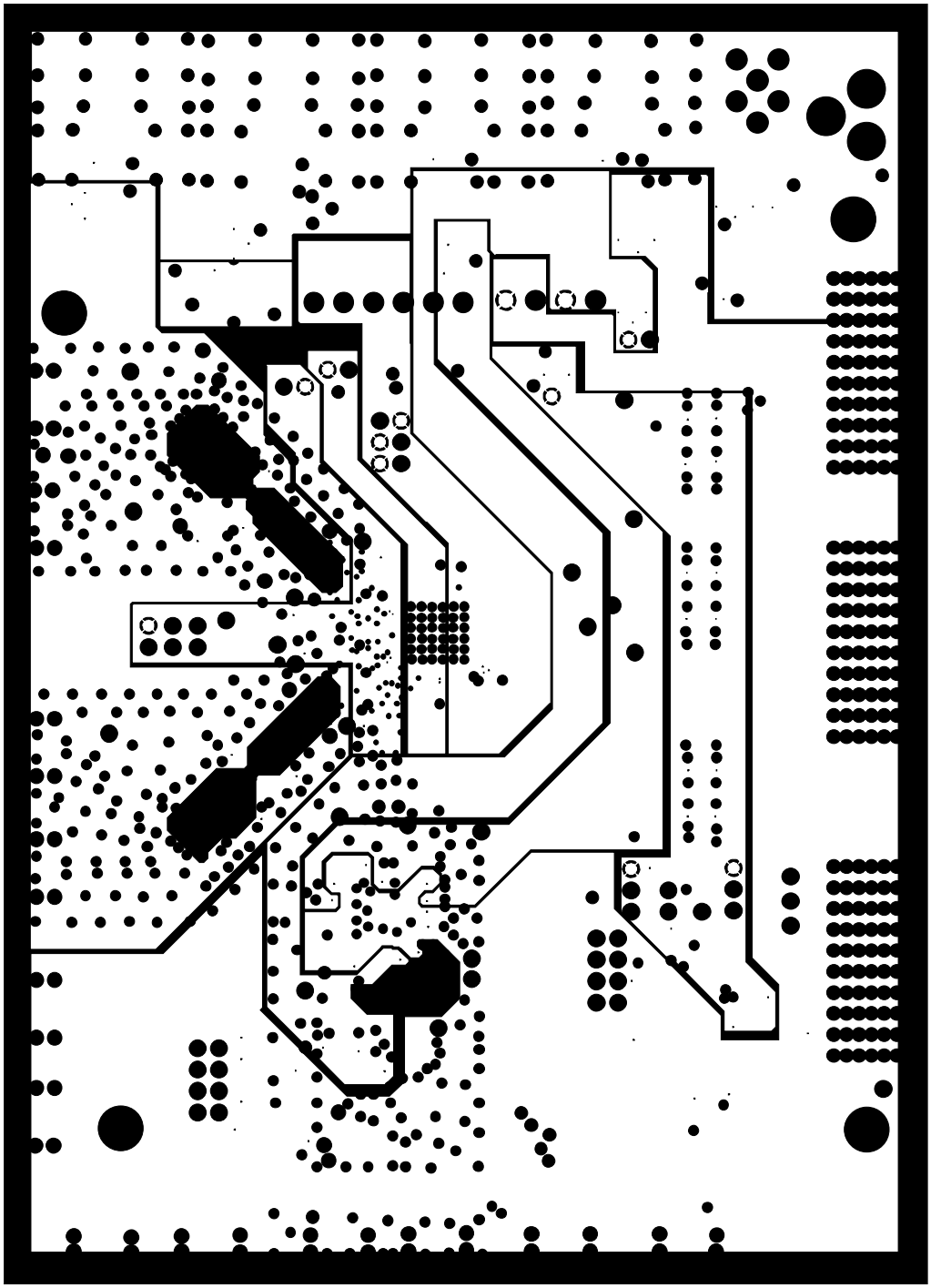



*Figure 87. Evaluation Board Layout, Power Plane*

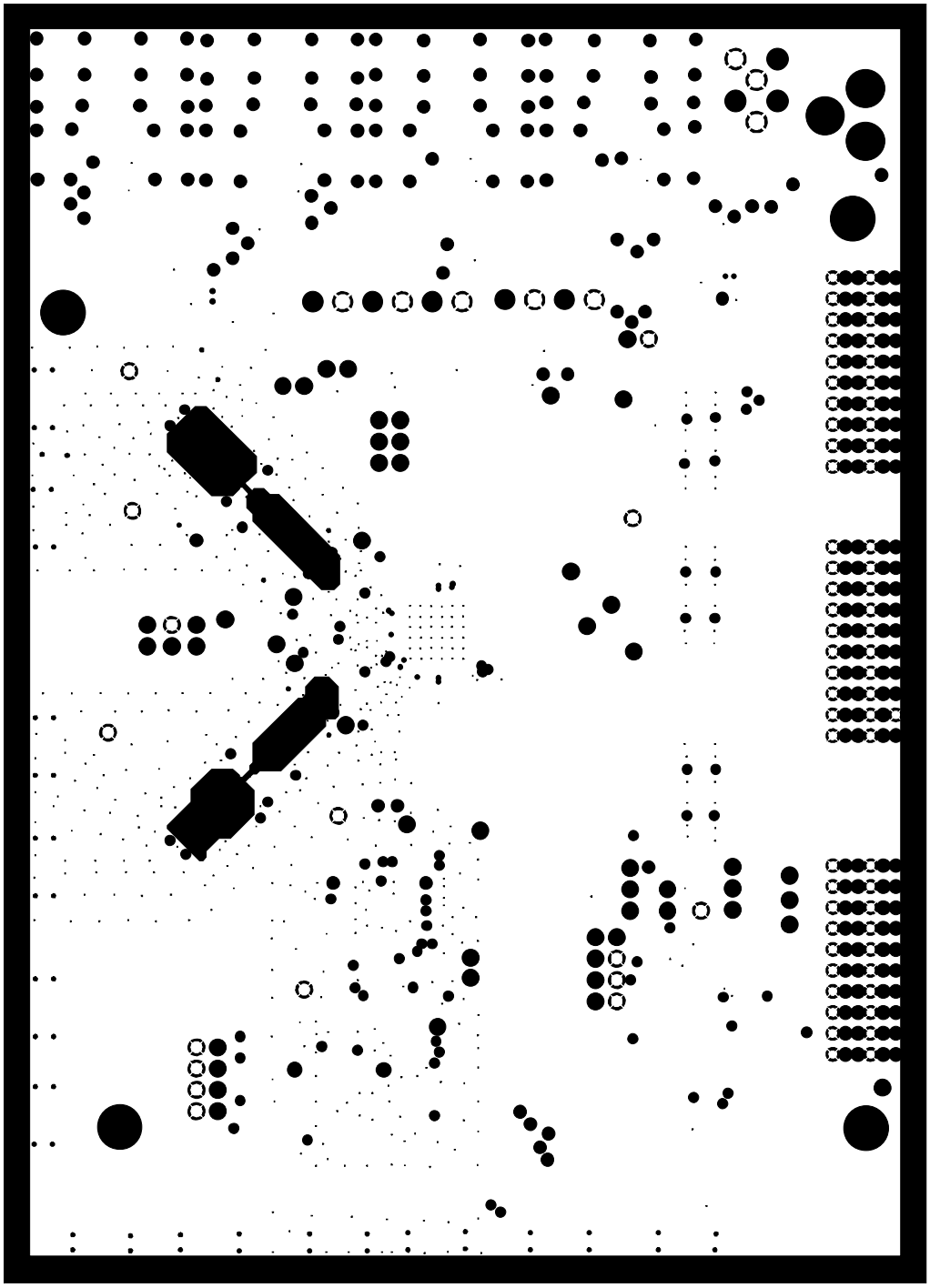



*Figure 88. Evaluation Board Layout, Ground Plane*

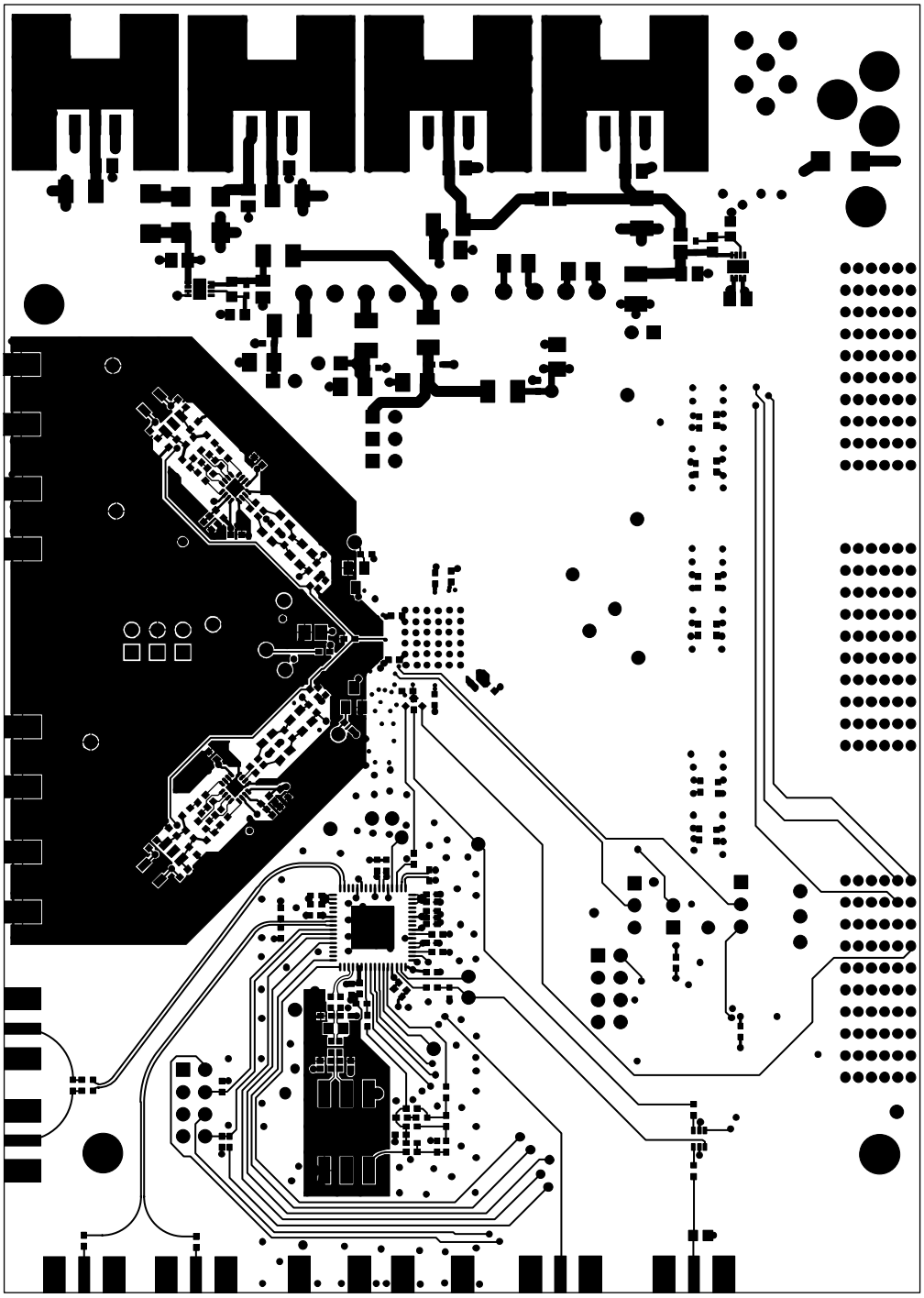


*Figure 89. Evaluation Board Layout, Secondary Side (Mirrored Image)*

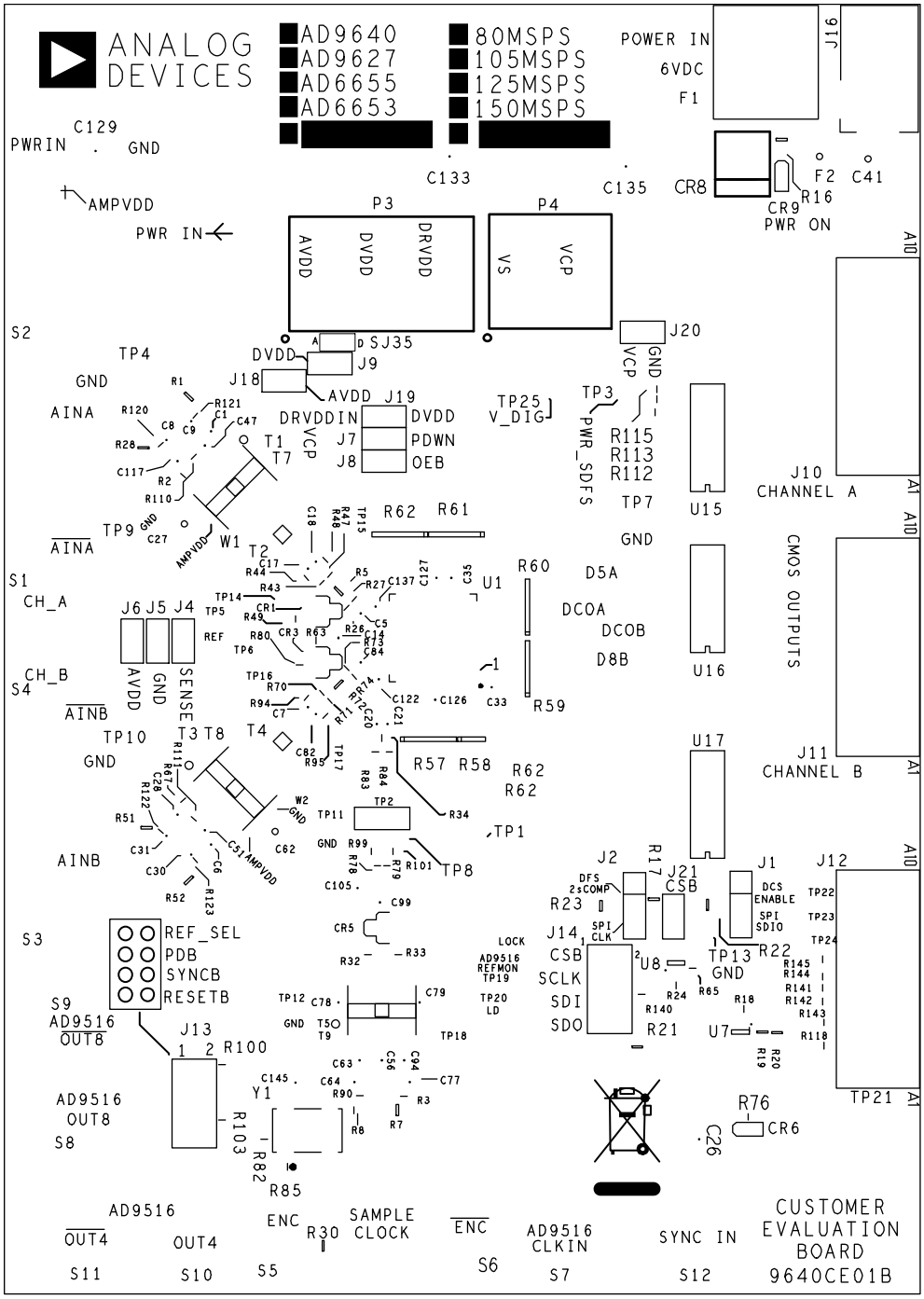



*Figure 90. Evaluation Board Layout, Silkscreen, Primary Side*

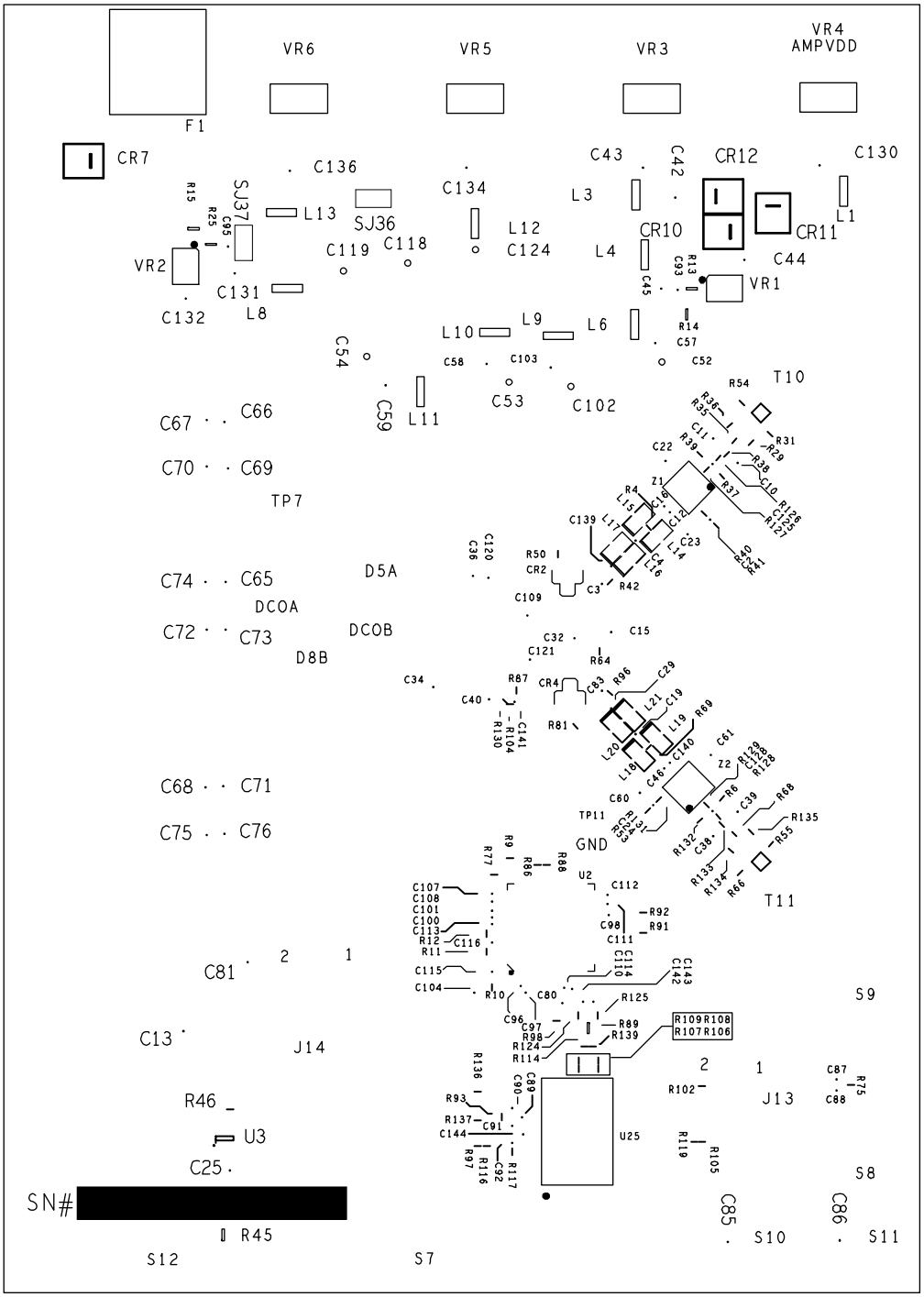



*Figure 91. Evaluation Board Layout, Silk Screen, Secondary Side*

## BILL OF MATERIALS

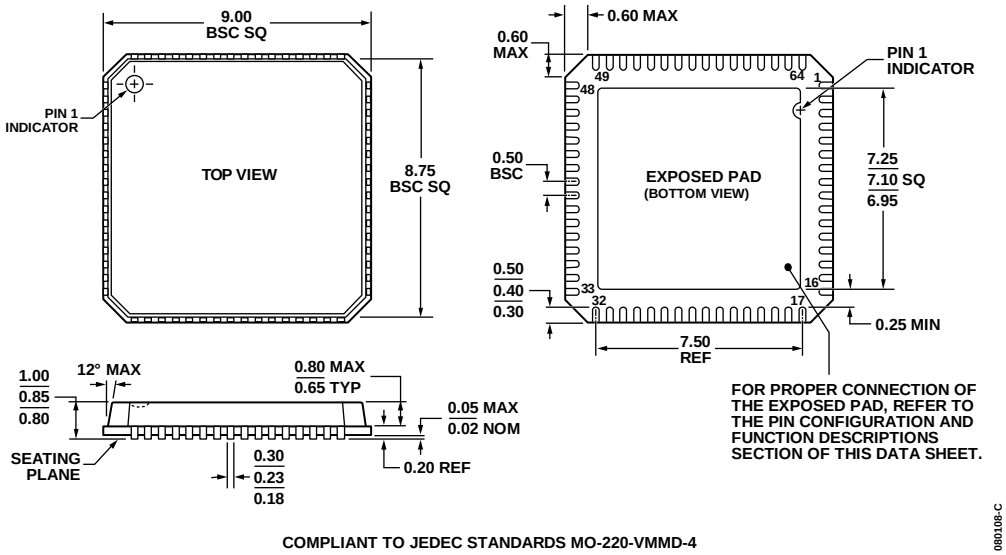
**Table 23. Evaluation Board Bill of Materials (BOM)[1, 2]**

| Item | Qty | Reference Designator | Description | Package | Manufacturer | Mfg. Part Number |
|---|---|---|---|---|---|---|
| 1 | 1 | AD9600CE_REVB | PCB | PCB | Analog Devices | |
| 2 | 55 | C1 to C3, C6, C7, C13, C14, C17, C18, C20 to C26, C32, C57 to C61, C65 to C76, C81 to C83, C96 to C101, C103, C105, C107, C108, C110 to C116, C145 | 0.1 µF, 16 V ceramic capacitor, SMT 0402 | C0402SM | Murata | GRM155R71C104KA88D |
| 3 | 1 | C80 | 18 pF, COG, 50 V, 5% ceramic capacitor, SMT 0402 | C0402SM | Murata | GJM1555C1H180JB01J |
| 4 | 2 | C5, C84 | 4.7 pF, COG, 50 V, 5% ceramic capacitor, SMT 0402 | C0402SM | Murata | GJM1555C1H4R7CB01J |
| 5 | 10 | C33, C35, C63, C93 to C95, C122, C126, C127, C137 | 0.001 µF, X7R, 25 V, 10% ceramic capacitor, SMT 0402 | C0402SM | Murata | GRM155R71H102KA01D |
| 6 | 13 | C15, C42 to C45, C129 to C136 | 1 µF, X5R, 25 V, 10% ceramic capacitor, SMT 0805 | C0805 | Murata | GR4M219R61A105KC01D |
| 7 | 10 | C27, C41, C52 to C54, C62, C102, C118, C119, C124 | 10 µF, X5R, 10 V, 10% ceramic capacitor, SMT 1206 | C1206 | Murata | GRM31CR61C106KC31L |
| 8 | 1 | CR5 | Schottky diode HSMS2822, SOT23 | SOT23 | Avago Technologies | HSMS-2822-BLKG |
| 9 | 2 | CR6, CR9 | LED RED, SMT, 0603, SS-type | LED0603 | Panasonic | LNJ208R8ARA |
| 10 | 4 | CR7, CR10 to CR12 | 50 V, 2 A diode | DO_214AA | Micro Commercial Components | S2A-TP |
| 11 | 1 | CR8 | 30 V, 3 A diode | DO_214AB | Micro Commercial Components | SK33-TP |
| 12 | 1 | F1 | EMI filter | FLTHMURATABNX01 | Murata | BNX016-01 |
| 13 | 1 | F2 | 6.0 V, 3.0 A, trip current resettable fuse | L1206 | Tyco Raychem | NANOSMDC150F-2 |
| 14 | 2 | J1 to J2 | 3-pin, male, single row, straight header | HDR3 | Samtec | TWS-1003-08-G-S |
| 15 | 9 | J4 to J9, J18, J19, J21 | 2-pin, male, straight header | HDR2 | Samtec | TWS-102-08-G-S |
| 16 | 3 | J10 to J12 | Interface connector | TYCO_HM_ZD | Tyco | 6469169-1 |
| 17 | 1 | J14 | 8-pin, male, double row, straight header | CNBERG2X4H350LD | Samtec | TSW-104-08-T-D |
| 18 | 1 | J16 | DC power jack connector | PWR_JACK1 | Cui Stack | PJ-002A |
| 19 | 10 | L1, L3, L4, L6, L8 to L13 | 10 µH, 2 A bead core, 1210 | 1210 | Panasonic | EXC-CL3225U1 |
| 20 | 1 | P3 | 6-terminal connector | PTMICRO6 | Weiland Electric, Inc. | Z5.531.3625.0 |
| 21 | 1 | P4 | 4-terminal connector | PTMICRO4 | Weiland Electric, Inc. | Z5.531.3425.0 |
| 22 | 3 | R7, R30, R45 | 57.6 Ω, 0603, 1/10 W, 1% resistor | R0603 | NIC Components | NRC06F57R6TRF |
| 23 | 27 | R2, R3, R4, R32, R33, R42, R64, R67, R69, R90, R96, R99, R101, R104, R110 to R113, R115, R119, R121, R123, R141 to R145 | 0 Ω, 1/16 W, 5% resistor | R0402SM | NIC Components | NRC04ZOTRF |
| 24 | 2 | R13, R25 | 140 kΩ, 0603, 1/10 W, 1% resistor | R0603 | NIC Components | NRC06F1403TRF |
| 25 | 2 | R14, R15 | 78.7 kΩ, 0603, 1/10 W, 1% resistor | R0603 | NIC Components | NRC06F7872TRF |

| Item | Qty | Reference Designator | Description | Package | Manufacturer | Mfg. Part Number |
|---|---|---|---|---|---|---|
| 26 | 1 | R16 | 261 Ω, 0603, 1/10 W, 1% resistor | R0603 | NIC Components | NRC06F2610TRF |
| 27 | 3 | R17, R22, R23 | 100 kΩ, 0603, 1/10 W, 1% resistor | R0603 | NIC Components | NRC06F1003TRF |
| 28 | 7 | R18, R24, R63, R65, R82, R118, R140 | 10 kΩ, 0402, 1/16 W, 1% resistor | R0402SM | NIC Components | NRC04F1002TRF |
| 29 | 3 | R19, R20, R21 | 1 kΩ, 0603, 1/10 W, 1% resistor | R0603 | NIC Components | NRC06F1001TRF |
| 30 | 9 | R26, R27, R43, R46, R47, R70, R71, R73, R74 | 33 Ω, 0402, 1/16 W, 5% resistor | R0402SM | NIC Components | NRC04J330TRF |
| 31 | 5 | R57, R59 to R62 | 22 Ω, 16-pin, 8-resistor, resistor array | R_742 | CTS Corporation | 742C163220JPTR |
| 32 | 1 | R58 | 22 Ω, 8-pin, 4-resistor, resistor array | RES_ARRY | CTS Corporation | 742C083220JPTR |
| 33 | 1 | R76 | 200 Ω, 0402, 1/16 W, 1% resistor | R0402SM | NIC Components | NCR04F2000TRF |
| 34 | 4 | S2, S3, S5 ,S12 | SMA, inline, male, coaxial connector | SMA_EDGE | Emerson Network Power | 142-0701-201 |
| 35 | 1 | SJ35 | 0 Ω, 1/8 W, 1% resistor | SLDR_PAD2MUYLAR | NIC Components | NRC10ZOTRF |
| 36 | 5 | T1 to T5 | Balun | TRAN6B | M/A-COM | MABA-007159-000000 |
| 37 | 1 | U1 | IC, AD9600 | LFCSP64-9X9-9E | Analog Devices | AD9600BCPZ/AD9600ABCPZ |
| 38 | 1 | U2 | Clock distribution, PLL IC | LFCSP64-9X9 | Analog Devices | AD9516-4BCPZ |
| 39 | 1 | U3 | Dual inverter IC | SC70_6 | Fairchild Semiconductor | NC7WZ04P6X_NL |
| 40 | 1 | U7 | Dual buffer IC, open-drain circuits | SC70_6 | Fairchild Semiconductor | NC7WZ07P6X_NL |
| 41 | 1 | U8 | UHS dual buffer IC | SC70_6 | Fairchild Semiconductor | NC7WZ16P6X_NL |
| 42 | 3 | U15 to U17 | 16-bit CMOS buffer IC | TSOP48_8_1MM | Fairchild Semiconductor | 74VCX16244MTDX_NL |
| 43 | 2 | VR1, VR2 | Adjustable regulator | LFCSP8-3X3 | Analog Devices | ADP3334ACPZ |
| 44 | 1 | VR3 | 1.8 V high accuracy regulator | SOT223-HS | Analog Devices | ADP3339AKCZ-1.8 |
| 45 | 1 | VR4 | 5.0 V high accuracy regulator | SOT223-HS | Analog Devices | ADP3339AKCZ-5.0 |
| 46 | 2 | VR5, VR6 | 3.3 V high accuracy regulator | SOT223-HS | Analog Devices | ADP3339AKCZ-3.3 |
| 47 | 1 | Y1 | Oscillator clock, VFAC3 | OSC-CTS-CB3 | Valpey Fisher | VFAC3-BHL |
| 48 | 2 | Z1, Z2 | High speed IC, op amp | LFCSP16-3X3-PAD | Analog Devices | AD8352ACPZ |

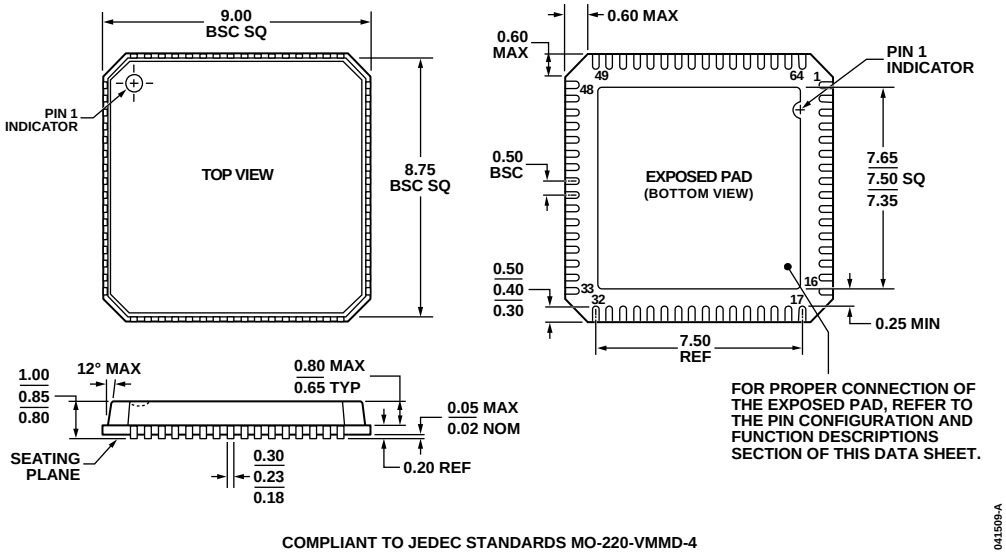
[1] This bill of materials is RoHS compliant.
[2] The bill of materials lists only those items that are normally installed in the default condition. Items that are not installed are not included in the BOM.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

*Figure 92. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*9 mm × 9 mm Body, Very Thin Quad*
*(CP-64-3)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

*Figure 93. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*9 mm × 9 mm Body, Very Thin Quad*
*(CP-64-6)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD9600ABCPZ-150[1,2] | −40°C to +85°C | 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-64-6 |
| AD9600ABCPZ-125[1,2] | −40°C to +85°C | 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-64-6 |
| AD9600ABCPZ-105[1,2] | −40°C to +85°C | 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-64-6 |
| AD9600BCPZ-150[1] | −40°C to +85°C | 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-64-3 |
| AD9600BCPZ-125[1] | −40°C to +85°C | 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-64-3 |
| AD9600BCPZ-105[1] | −40°C to +85°C | 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-64-3 |
| AD9600-150EBZ[1] | | Evaluation Board with AD9600 and Software | |

[1] Z = RoHS Compliant Part.
[2] Recommended for use in new designs; reference PCN 09_0156.


D06909-0-12/09(B)

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