THE DATASHEET OF

ADR439ARMZ-REEL7

Ultralow Noise XFET Voltage References with Current Sink and Source Capability

ADR430/ADR431/ADR433/ADR434/ADR435/ADR439

FEATURES

- Low noise (0.1 Hz to 10.0 Hz): 3.5 µV p-p @ 2.5 V output
- No external capacitor required
- Low temperature coefficient
  - A Grade: 10 ppm/°C maximum
  - B Grade: 3 ppm/°C maximum
- Load regulation: 15 ppm/mA
- Line regulation: 20 ppm/V
- Wide operating range
  - ADR430: 4.1 V to 18 V
  - ADR431: 4.5 V to 18 V
  - ADR433: 5.0 V to 18 V
  - ADR434: 6.1 V to 18 V
  - ADR435: 7.0 V to 18 V
  - ADR439: 6.5 V to 18 V
- High output source and sink current: +30 mA and −20 mA
- Wide temperature range: −40°C to +125°C

APPLICATIONS

- Precision data acquisition systems
- High resolution data converters
- Medical instruments
- Industrial process control systems
- Optical control circuits
- Precision instruments

PIN CONFIGURATIONS

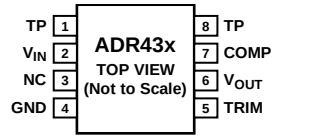

Figure 1. 8-Lead MSOP (RM-8)

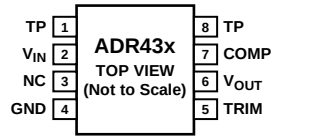

Figure 2. 8-Lead SOIC_N (R-8)

GENERAL DESCRIPTION

The ADR43x series is a family of XFET® voltage references featuring low noise, high accuracy, and low temperature drift performance. Using Analog Devices, Inc., patented temperature drift curvature correction and XFET (eXtra implanted junction FET) technology, voltage change vs. temperature nonlinearity in the ADR43x is minimized.

The XFET references operate at lower current (800 µA) and lower supply voltage headroom (2 V) than buried Zener references. Buried Zener references require more than 5 V headroom for operation. The ADR43x XFET references are the only low noise solutions for 5 V systems.

The ADR43x family has the capability to source up to 30 mA of output current and sink up to 20 mA. It also comes with a trim terminal to adjust the output voltage over a 0.5% range without compromising performance.

The ADR43x is available in 8-lead MSOP and 8-lead narrow SOIC packages. All versions are specified over the extended industrial temperature range of −40°C to +125°C.

Table 1. Selection Guide

Model	Output Voltage (V)	Accuracy (mV)	Temperature Coefficient (ppm/°C)
ADR430A	2.048	±3	10
ADR430B	2.048	±1	3
ADR431A	2.500	±3	10
ADR431B	2.500	±1	3
ADR433A	3.000	±4	10
ADR433B	3.000	±1.5	3
ADR434A	4.096	±5	10
ADR434B	4.096	±1.5	3
ADR435A	5.000	±6	10
ADR435B	5.000	±2	3
ADR439A	4.500	±5.5	10
ADR439B	4.500	±2	3

Rev. F

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1/09—Rev. D to Rev. E

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Inserted Figure 31, Figure 32, and Figure 33; Renumbered Sequentially ... 16
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12/03—Revision 0: Initial Version

SPECIFICATIONS

ADR430 ELECTRICAL CHARACTERISTICS

V_{IN} = 4.1 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O					
A Grade			2.045	2.048	2.051	V
B Grade			2.047	2.048	2.049	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±3	mV
					±0.15	%
B Grade					±1	mV
					±0.05	%
TEMPERATURE COEFFICIENT	TCV_O					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 4.1 V to 18 V, −40°C < T_A < +125°C		5	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 5.0 V, −40°C < T_A < +125°C			15	ppm/mA
	$\Delta V_O/\Delta I_L$	I_L = −10 mA to 0 mA, V_{IN} = 5.0 V, −40°C < T_A < +125°C			15	ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		560	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		3.5		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		60		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[1]	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		4.1		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR431 ELECTRICAL CHARACTERISTICS

V_{IN} = 4.5 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O					
A Grade			2.497	2.500	2.503	V
B Grade			2.499	2.500	2.501	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±3	mV
					±0.12	%
B Grade					±1	mV
					±0.04	%
TEMPERATURE COEFFICIENT	TCV_O					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 4.5 V to 18 V, −40°C < T_A < +125°C		5	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 5.0 V, −40°C < T_A < +125°C			15	ppm/mA
	$\Delta V_O/\Delta I_L$	I_L = −10 mA to 0 mA, V_{IN} = 5.0 V, −40°C < T_A < +125°C			15	ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		580	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		3.5		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		80		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[1]	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		4.5		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR433 ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O					
A Grade			2.996	3.000	3.004	V
B Grade			2.9985	3.000	3.0015	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±4	mV
					±0.13	%
B Grade					±1.5	mV
					±0.05	%
TEMPERATURE COEFFICIENT	TCV_O					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 5 V to 18 V, −40°C < T_A < +125°C		5	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 6 V, −40°C < T_A < +125°C			15	ppm/mA
	$\Delta V_O/\Delta I_L$	I_L = −10 mA to 0 mA, V_{IN} = 6 V, −40°C < T_A < +125°C			15	ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		590	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		3.75		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		90		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[1]	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		5.0		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR434 ELECTRICAL CHARACTERISTICS

V_{IN} = 6.1 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O					
A Grade			4.091	4.096	4.101	V
B Grade			4.0945	4.096	4.0975	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±5	mV
					±0.12	%
B Grade					±1.5	mV
					±0.04	%
TEMPERATURE COEFFICIENT	TCV_O					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 6.1 V to 18 V, −40°C < T_A < +125°C		5	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 7 V, −40°C < T_A < +125°C			15	ppm/mA
	$\Delta V_O/\Delta I_L$	I_L = −10 mA to 0 mA, V_{IN} = 7 V, −40°C < T_A < +125°C			15	ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		595	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		6.25		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		100		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[1]	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		6.1		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR435 ELECTRICAL CHARACTERISTICS

V_{IN} = 7.0 V to 18 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O					
A Grade			4.994	5.000	5.006	V
B Grade			4.998	5.000	5.002	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±6	mV
					±0.12	%
B Grade					±2	mV
					±0.04	%
TEMPERATURE COEFFICIENT	TCV_O					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 7 V to 18 V, −40°C < T_A < +125°C		5	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 8 V, −40°C < T_A < +125°C			15	ppm/mA
	$\Delta V_O/\Delta I_L$	I_L = −10 mA to 0 mA, V_{IN} = 8 V, −40°C < T_A < +125°C			15	ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		620	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10 Hz		8		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		115		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[1]	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		7.0		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ADR439 ELECTRICAL CHARACTERISTICS

V_{IN} = 6.5 V to 18 V, I_L = 0 mV, T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_O					
A Grade			4.4946	4.500	4.5054	V
B Grade			4.498	4.500	4.502	V
INITIAL ACCURACY	V_{OERR}					
A Grade					±5.5	mV
					±0.12	%
B Grade					±2	mV
					±0.04	%
TEMPERATURE COEFFICIENT	TCV_O					
A Grade		−40°C < T_A < +125°C		2	10	ppm/°C
B Grade		−40°C < T_A < +125°C		1	3	ppm/°C
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 6.5 V to 18 V, −40°C < T_A < +125°C		5	20	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$	I_L = 0 mA to 10 mA, V_{IN} = 6.5 V, −40°C < T_A < +125°C			15	ppm/mA
	$\Delta V_O/\Delta I_L$	I_L = −10 mA to 0 mA, V_{IN} = 6.5 V, −40°C < T_A < +125°C			15	ppm/mA
QUIESCENT CURRENT	I_{IN}	No load, −40°C < T_A < +125°C		600	800	µA
VOLTAGE NOISE	e_N p-p	0.1 Hz to 10.0 Hz		7.5		µV p-p
VOLTAGE NOISE DENSITY	e_N	1 kHz		110		nV/√Hz
TURN-ON SETTLING TIME	t_R	C_L = 0 µF		10		µs
LONG-TERM STABILITY[1]	ΔV_O	1000 hours		40		ppm
OUTPUT VOLTAGE HYSTERESIS	V_{O_HYS}			20		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 1 kHz		−70		dB
SHORT CIRCUIT TO GND	I_{SC}			40		mA
SUPPLY VOLTAGE OPERATING RANGE	V_{IN}		6.5		18	V
SUPPLY VOLTAGE HEADROOM	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Supply Voltage	20 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R)	130	43	°C/W
8-Lead MSOP (RM)	142	44	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

Default conditions: ±5 V, C_L = 5 pF, G = 2, R_G = R_F = 1 kΩ, R_L = 2 kΩ, V_O = 2 V p-p, f = 1 MHz, T_A = 25°C, unless otherwise noted.

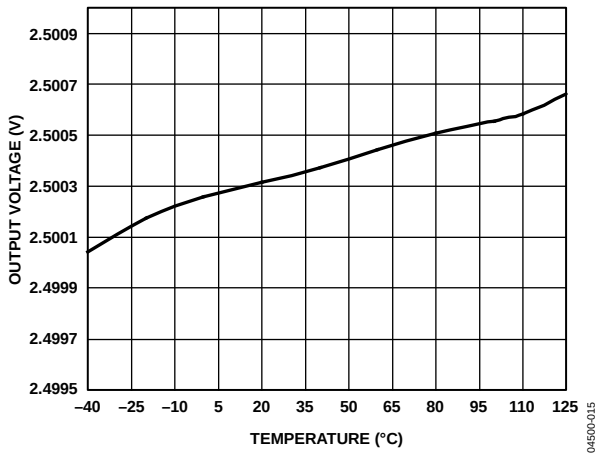


Figure 3. ADR431 Output Voltage vs. Temperature

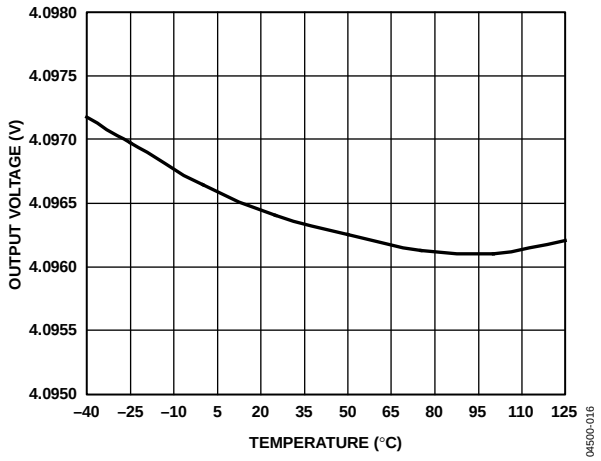


Figure 4. ADR434 Output Voltage vs. Temperature

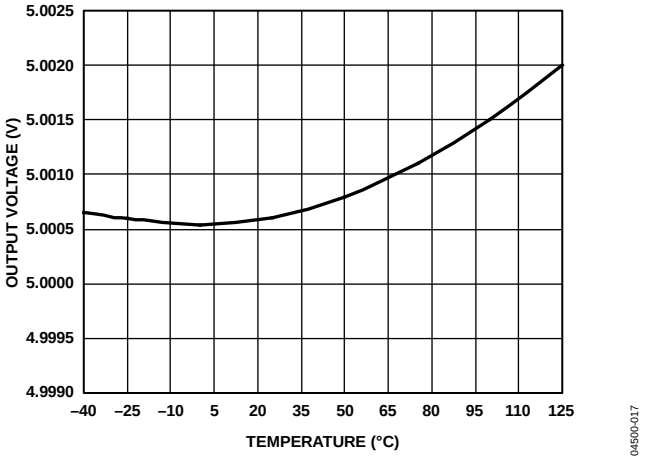


Figure 5. ADR435 Output Voltage vs. Temperature

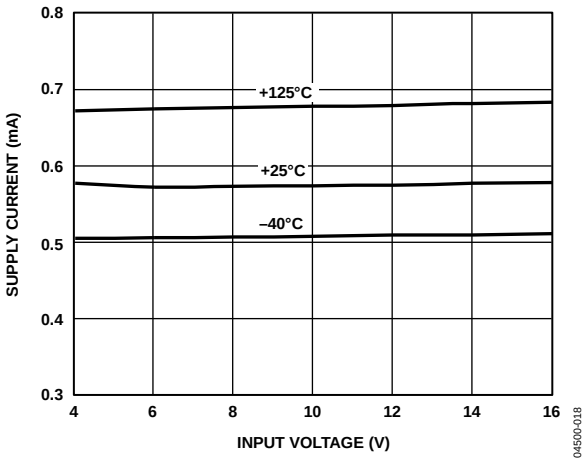


Figure 6. ADR435 Supply Current vs. Input Voltage

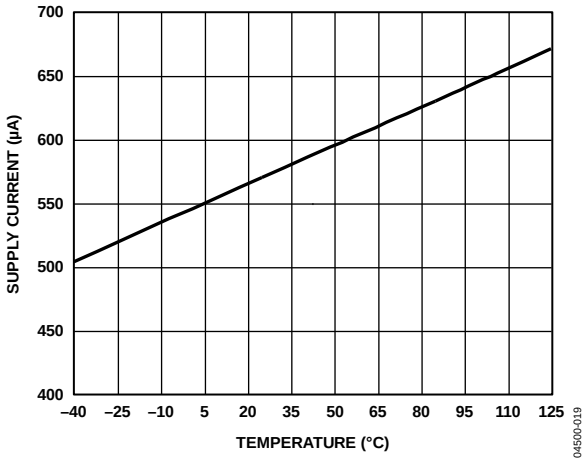


Figure 7. ADR435 Supply Current vs. Temperature

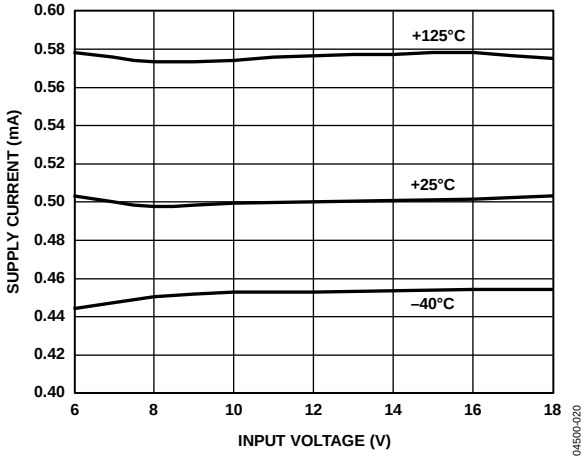


Figure 8. ADR431 Supply Current vs. Input Voltage

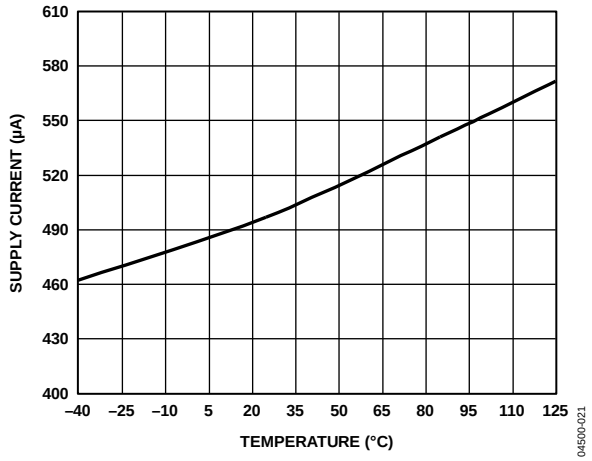


Figure 9. ADR431 Supply Current vs. Temperature

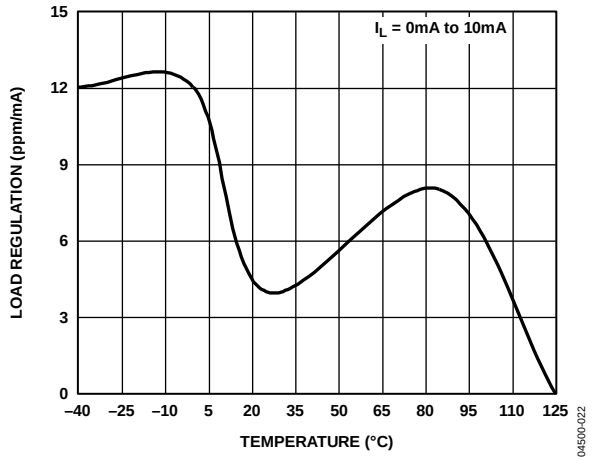


Figure 10. ADR431 Load Regulation vs. Temperature

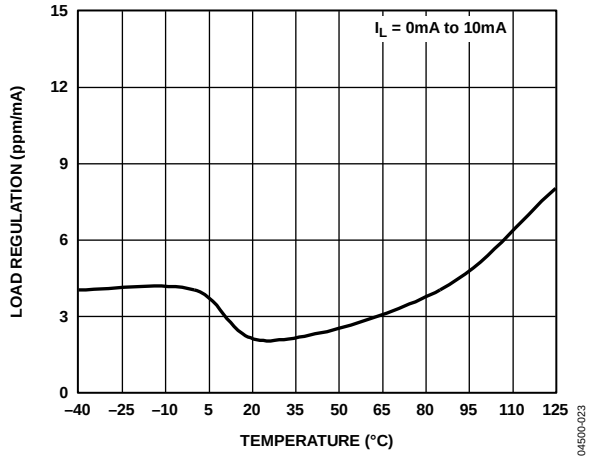


Figure 11. ADR435 Load Regulation vs. Temperature

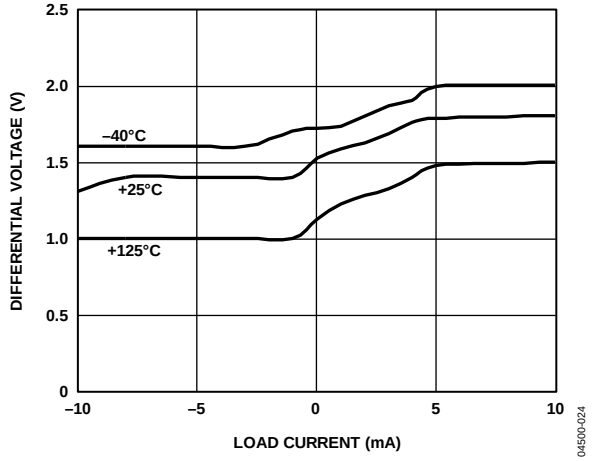


Figure 12. ADR431 Minimum Input/Output Differential Voltage vs. Load Current

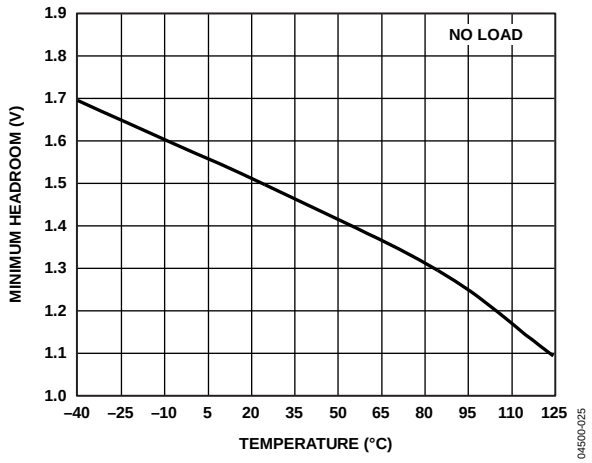


Figure 13. ADR431 Minimum Headroom vs. Temperature

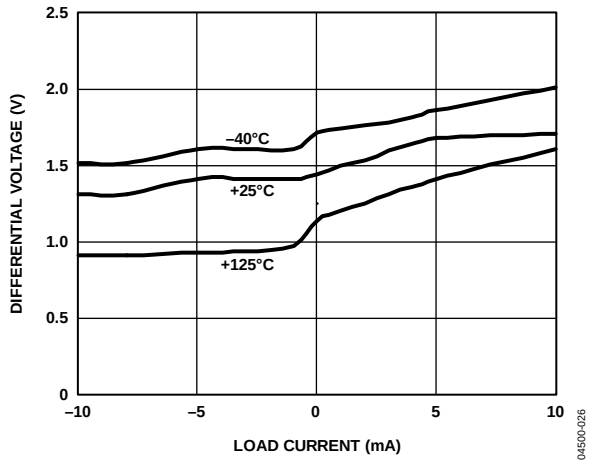


Figure 14. ADR435 Minimum Input/Output Differential Voltage vs. Load Current

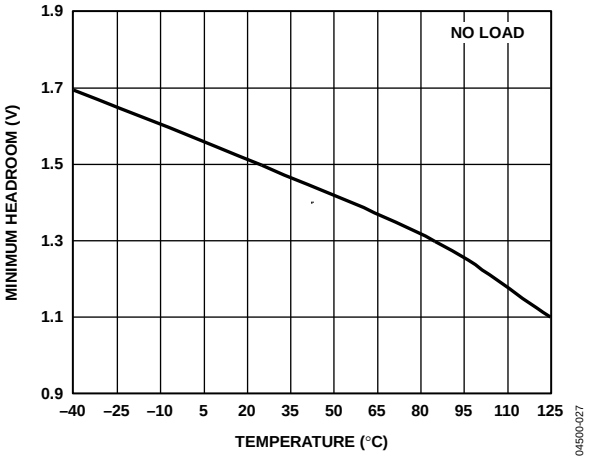


Figure 15. ADR435 Minimum Headroom vs. Temperature

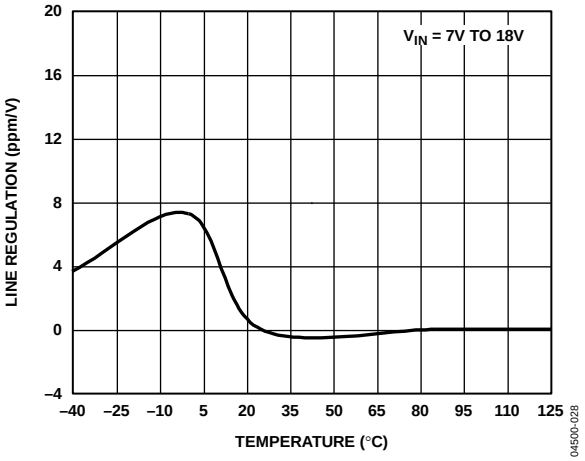


Figure 16. ADR435 Line Regulation vs. Temperature

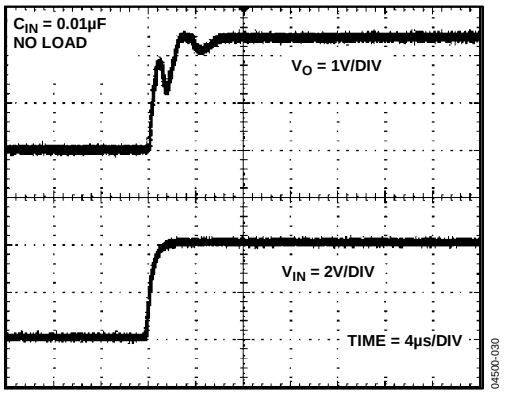


Figure 17. ADR431 Turn-On Response

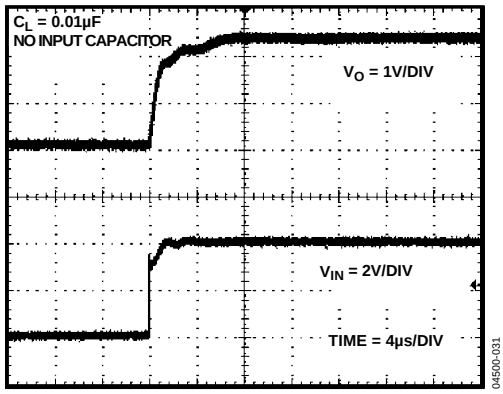


Figure 18. ADR431 Turn-On Response, 0.01 µF Load Capacitor

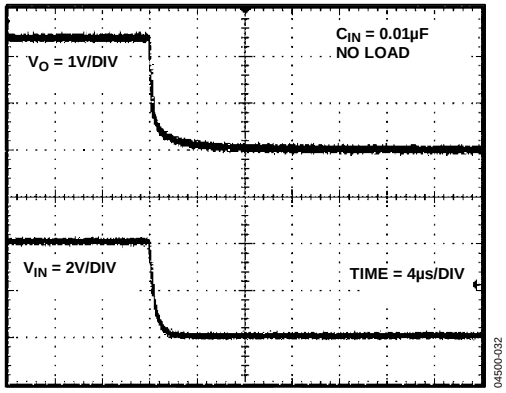


Figure 19. ADR431 Turn-Off Response

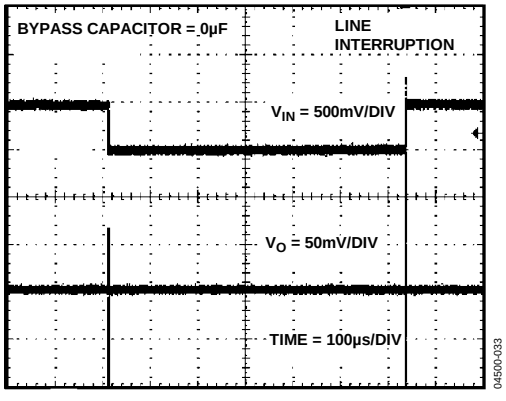


Figure 20. ADR431 Line Transient Response

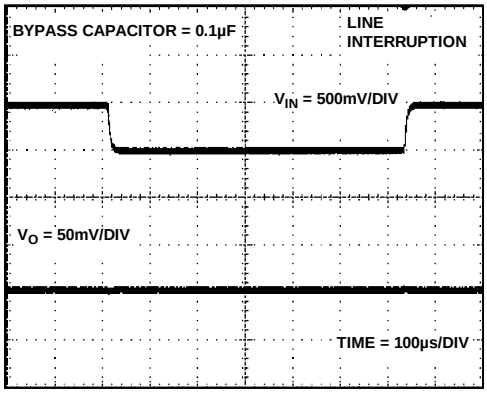


Figure 21. ADR431 Line Transient Response, 0.1 µF Bypass Capacitor

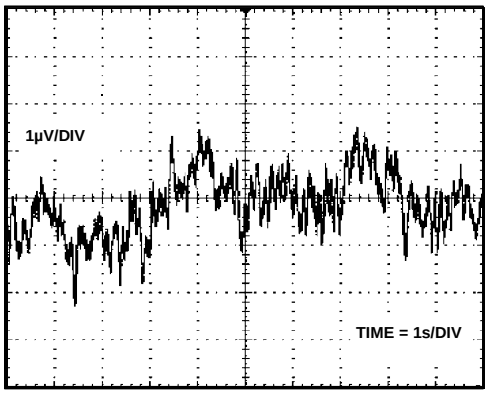


Figure 22. ADR431 0.1 Hz to 10.0 Hz Voltage Noise

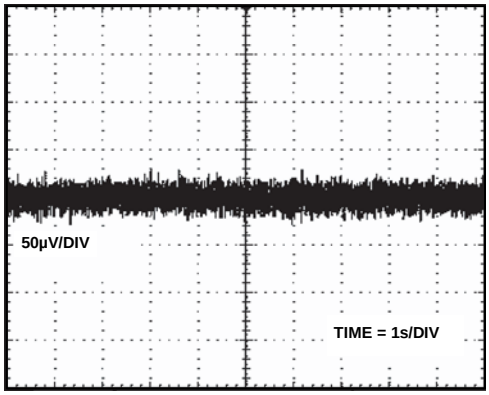


Figure 23. ADR431 10 Hz to 10 kHz Voltage Noise

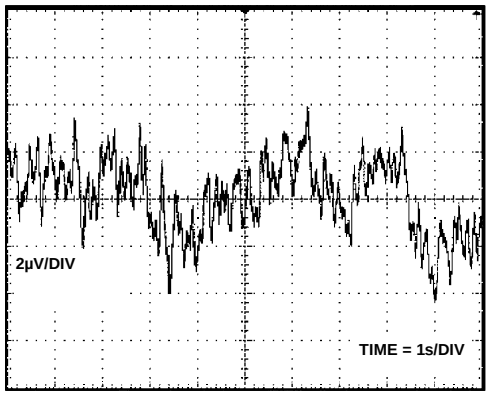


Figure 24. ADR435 0.1 Hz to 10.0 Hz Voltage Noise

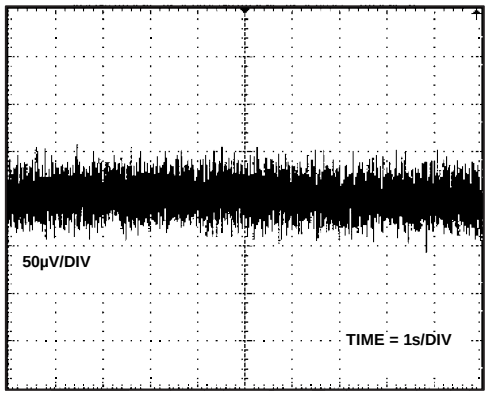


Figure 25. ADR435 10 Hz to 10 kHz Voltage Noise

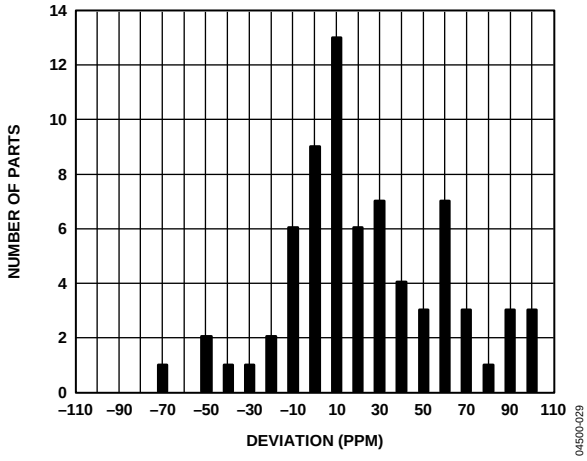


Figure 26. ADR431 Typical Hysteresis

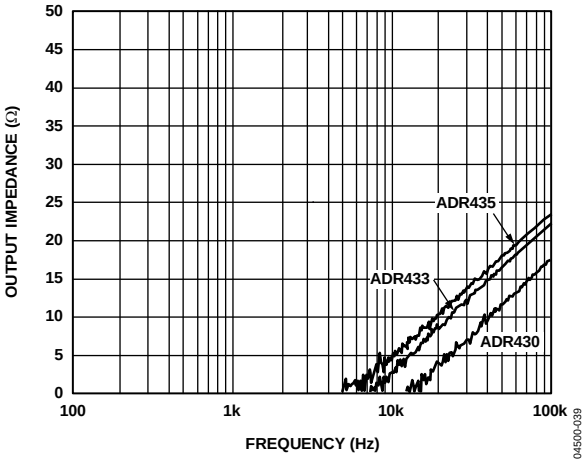


Figure 27. Output Impedance vs. Frequency

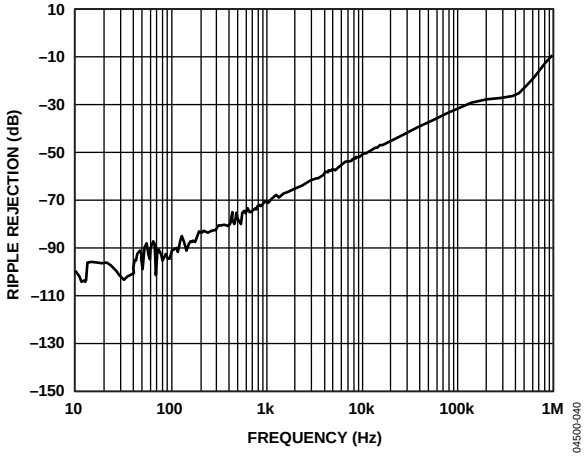


Figure 28. Ripple Rejection

THEORY OF OPERATION

The ADR43x series of references uses a reference generation technique known as XFET (eXtra implanted junction FET). This technique yields a reference with low supply current, good thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field-effect transistors (JFETs), one of which has an extra channel implant to raise its pinch-off voltage. By running the two JFETs at the same drain current, the difference in pinch-off voltage can be amplified and used to form a highly stable voltage reference.

The intrinsic reference voltage is around 0.5 V with a negative temperature coefficient of about −120 ppm/°C. This slope is essentially constant to the dielectric constant of silicon and can be compensated closely by adding a correction term generated in the same fashion as the proportional-to-temperature (PTAT) term used to compensate band gap references. The primary advantage of an XFET reference is its correction term, which is ~30 times lower and requires less correction than that of a band gap reference. Because most of the noise of a band gap reference comes from the temperature compensation circuitry, the XFET results in much lower noise.

Figure 29 shows the basic topology of the ADR43x series. The temperature correction term is provided by a current source with a value designed to be proportional to absolute temperature. The general equation is

$$V_{OUT} = G\,(\Delta V_P - R1 \times I_{PTAT}) \quad (1)$$

where:
G is the gain of the reciprocal of the divider ratio.
ΔV_P is the difference in pinch-off voltage between the two JFETs.
I_{PTAT} is the positive temperature coefficient correction current.

ADR43x devices are created by on-chip adjustment of R2 and R3 to achieve 2.048 V or 2.500 V, respectively, at the reference output.

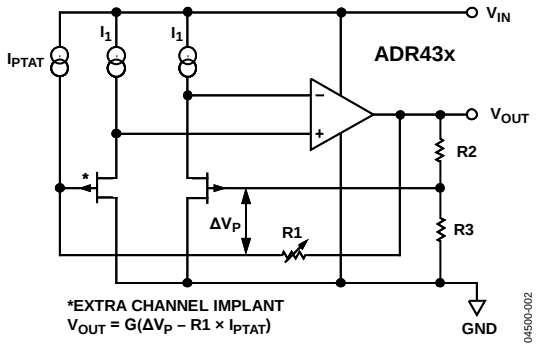


Figure 29. Simplified Schematic Device Power Dissipation Considerations

The ADR43x family of references is guaranteed to deliver load currents to 10 mA with an input voltage that ranges from 4.1 V to 18 V. When these devices are used in applications at higher currents, use the following equation to account for the temperature effects due to the power dissipation increases:

$$T_J = P_D \times \theta_{JA} + T_A \quad (2)$$

where:
T_J and T_A are the junction and ambient temperatures, respectively.
P_D is the device power dissipation.
θ_{JA} is the device package thermal resistance.

BASIC VOLTAGE REFERENCE CONNECTIONS

Voltage references, in general, require a bypass capacitor connected from V_{OUT} to GND. The circuit in Figure 30 illustrates the basic configuration for the ADR43x family of references. Other than a 0.1 µF capacitor at the output to help improve noise suppression, a large output capacitor at the output is not required for circuit stability.

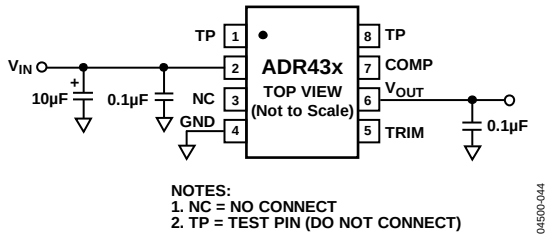


Figure 30. Basic Voltage Reference Configuration

NOISE PERFORMANCE

The noise generated by the ADR43x family of references is typically less than 3.75 µV p-p over the 0.1 Hz to 10.0 Hz band for ADR430, ADR431, and ADR433. Figure 22 shows the 0.1 Hz to 10.0 Hz noise of the ADR431, which is only 3.5 µV p-p. The noise measurement is made with a band-pass filter made of a 2-pole high-pass filter with a corner frequency at 0.1 Hz and a 2-pole low-pass filter with a corner frequency at 10.0 Hz.

HIGH FREQUENCY NOISE

The total noise generated by the ADR43x family of references is composed of the reference noise and the op amp noise. Figure 31 shows the wideband noise from 10 Hz to 25 kHz. An internal node of the op amp is brought out on Pin 7, and by overcompensating the op amp, the overall noise can be reduced.

This is understood by considering that in a closed-loop configuration, the effective output impedance of an op amp is

$$R_O = \frac{r_O}{1 + A_{VO}\beta} \quad (3)$$

where:
R_O is the apparent output impedance.
r_O is the output resistance of the op amp.
A_{VO} is the open-loop gain at the frequency of interest.
β is the feedback factor.

Equation 3 shows that the apparent output impedance is reduced by approximately the excess loop gain; therefore, as the frequency increases, the excess loop gain decreases, and the apparent output impedance increases. A passive element whose impedance increases as its frequency increases is an inductor. When a capacitor is added to the output of an op amp or a reference, it forms a tuned circuit that resonates at a certain frequency and results in gain peaking. This can be observed by using a model of a semiperfect op amp with a single-pole response and some pure resistance in series with the output. Changing capacitive loads results in peaking at different frequencies. For most normal op amp applications with low capacitive loading (<100 pF), this effect is usually not observed.

However, references are used increasingly to drive the reference input of an ADC that may present a dynamic, switching capacitive load. Large capacitors, in the microfarad range, are used to reduce the change in reference voltage to less than one-half LSB. Figure 31 shows the ADR431 noise spectrum with various capacitive values to 50 µF. With no capacitive load, the noise spectrum is relatively flat at approximately 60 nV/√Hz to 70 nV/√Hz. With various values of capacitive loading, the predicted noise peaking becomes evident.

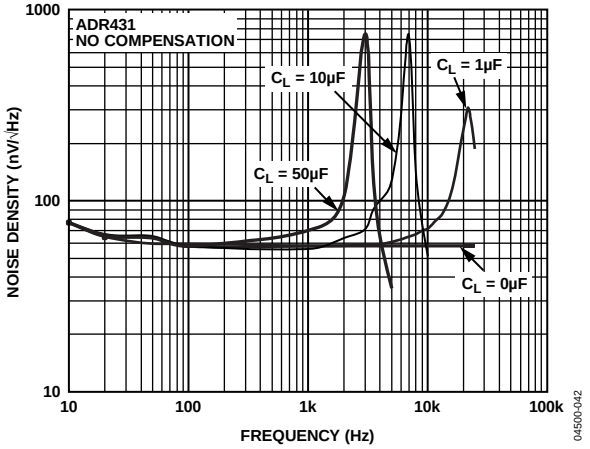


Figure 31. Noise vs. Capacitive Loading

The op amp within the ADR43x family uses the classic RC compensation technique. Monolithic capacitors in an IC are limited to tens of picofarads. With very large external capacitive loads, such as 50 µF, it is necessary to overcompensate the op amp. The internal compensation node is brought out on Pin 7, and an external series RC network can be added between Pin 7 and the output, Pin 6, as shown in Figure 32.

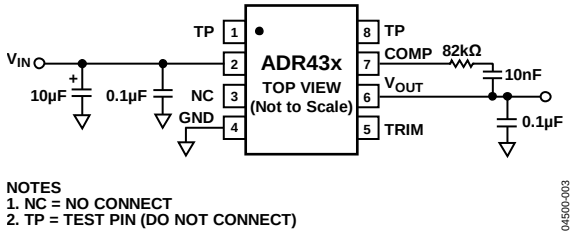


Figure 32. Compensated Reference

The 82 kΩ resistor and 10 nF capacitor can eliminate the noise peaking (see Figure 33). The COMP pin should be left unconnected if unused.

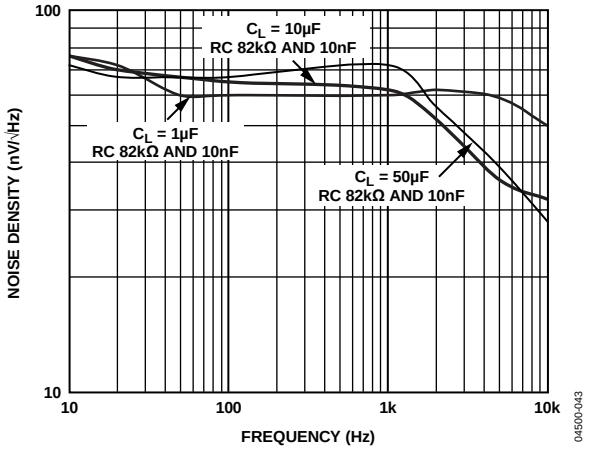


Figure 33. Noise with Compensation Network

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are the time for the active circuits to settle and the time for the thermal gradients on the chip to stabilize. Figure 17 and Figure 18 show the turn-on settling time for the ADR431.

APPLICATIONS INFORMATION

OUTPUT ADJUSTMENT

The ADR43x trim terminal can be used to adjust the output voltage over a ±0.5% range. This feature allows the system designer to trim system errors out by setting the reference to a voltage other than the nominal. This is also helpful if the part is used in a system at temperature to trim out any error. Adjustment of the output has negligible effect on the temperature performance of the device. To avoid degrading temperature coefficients, both the trimming potentiometer and the two resistors need to be low temperature coefficient types, preferably <100 ppm/°C.

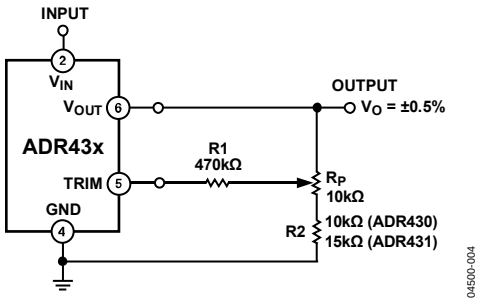


Figure 34. Output Trim Adjustment

REFERENCE FOR CONVERTERS IN OPTICAL NETWORK CONTROL CIRCUITS

In Figure 35, the high capacity, all optical router network employs arrays of micromirrors to direct and route optical signals from fiber to fiber without first converting them to electrical form, which reduces the communication speed. The tiny micromechanical mirrors are positioned so that each is illuminated by a single wavelength that carries unique information and can be passed to any desired input and output fiber. The mirrors are tilted by the dual-axis actuators, which are controlled by precision ADCs and DACs within the system. Due to the microscopic movement of the mirrors, not only is the precision of the converters important but the noise associated with these controlling converters is also extremely critical. Total noise within the system can be multiplied by the number of converters employed. Therefore, to maintain the stability of the control loop for this application, the ADR43x, with its exceptionally low noise, is necessary.

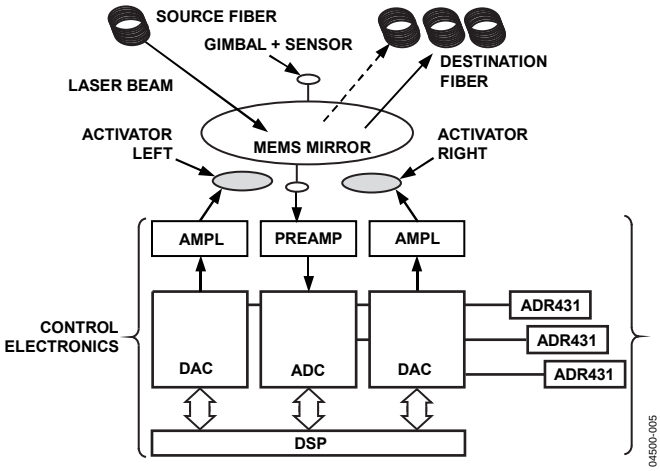


Figure 35. All Optical Router Network

NEGATIVE PRECISION REFERENCE WITHOUT PRECISION RESISTORS

In many current output CMOS DAC applications, where the output signal voltage must be of the same polarity as the reference voltage, it is required to reconfigure a current-switching DAC into a voltage-switching DAC by using a 1.25 V reference, an operational amplifier, and a pair of resistors. Using a current-switching DAC directly requires an additional operational amplifier at the output to reinvert the signal. A negative voltage reference is desirable because an additional operational amplifier is not required for either reinversion (current-switching mode) or amplification (voltage-switching mode) of the DAC output voltage. In general, any positive voltage reference can be converted to a negative voltage reference by using an operational amplifier and a pair of matched resistors in an inverting configuration. The disadvantage of this approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

A negative reference can easily be generated by adding a precision operational amplifier, such as the OP777 or the OP193, and configuring it as shown in Figure 36. V_{OUT} is at virtual ground; therefore, the negative reference can be taken directly from the output of the amplifier. The operational amplifier must be dual supply and have low offset and rail-to-rail capability if the negative supply voltage is close to the reference output.

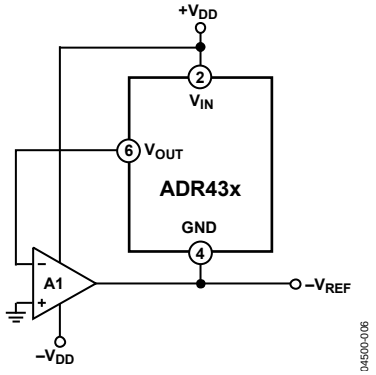


Figure 36. Negative Reference

HIGH VOLTAGE FLOATING CURRENT SOURCE

The circuit in Figure 37 can be used to generate a floating current source with minimal self heating. This particular configuration can operate on high supply voltages determined by the breakdown voltage of the N-channel JFET.

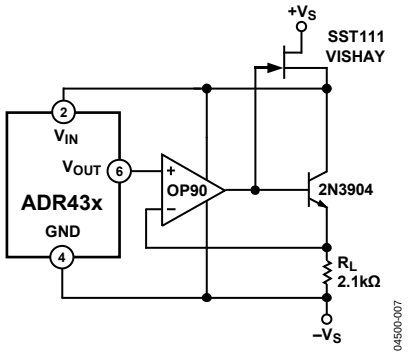


Figure 37. High Voltage Floating Current Source

KELVIN CONNECTION

In many portable instrumentation applications, where printed circuit board (PCB) cost and area go hand in hand, circuit interconnects are very often of dimensionally minimum width. These narrow lines can cause large voltage drops if the voltage reference is required to provide load currents to various functions. In fact, circuit interconnects can exhibit a typical line resistance of 0.45 mΩ/square (for example, 1 oz. Cu). Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. Load currents flowing through wiring resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. However, the Kelvin connection of Figure 38 overcomes the problem by including the wiring resistance within the forcing loop of the operational amplifier.

Because the amplifier senses the load voltage, the operational amplifier loop control forces the output to compensate for the wiring error and to produce the correct voltage at the load.

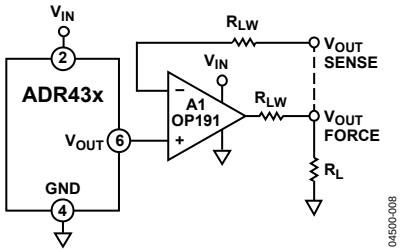


Figure 38. Advantage of Kelvin Connection

DUAL POLARITY REFERENCES

Dual polarity references can easily be made with an operational amplifier and a pair of resistors. To avoid defeating the accuracy obtained by the ADR43x, it is imperative to match the resistance tolerance as well as the temperature coefficient of all the components.

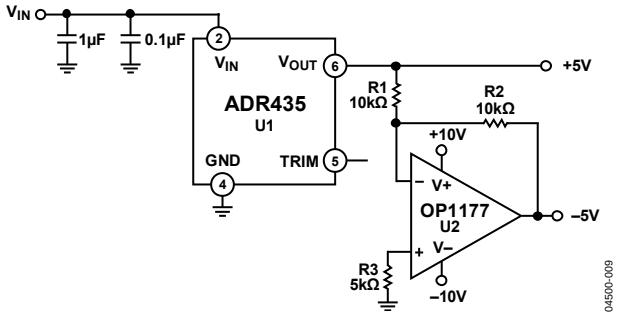


Figure 39. +5 V and –5 V References Using ADR435

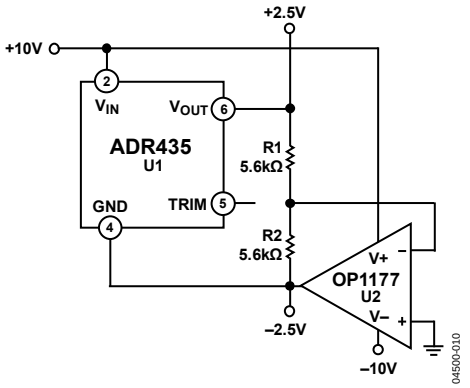


Figure 40. +2.5 V and –2.5 V References Using ADR435

PROGRAMMABLE CURRENT SOURCE

Together with a digital potentiometer and a Howland current pump, the ADR435 forms the reference source for a programmable current as

$$I_L = \left(\frac{R2_A + R2_B}{\frac{R1}{R2_B}} \right) \times V_W \quad (4)$$

and

$$V_W = \frac{D}{2^N} \times V_{REF} \quad (5)$$

where:
D is the decimal equivalent of the input code.
N is the number of bits.

In addition, R1' and R2' must be equal to R1 and ($R2_A$ + $R2_B$), respectively. In theory, $R2_B$ can be made as small as needed to achieve the necessary current within the A2 output current driving capability. In this example, the OP2177 can deliver a maximum output current of 10 mA. Because the current pump employs both positive and negative feedback, C1 and C2 capacitors are needed to ensure that the negative feedback prevails and, therefore, avoids oscillation. This circuit also allows bidirectional current flow if the V_A and V_B inputs of the digital potentiometer are supplied with the dual polarity references, as shown in Figure 41.

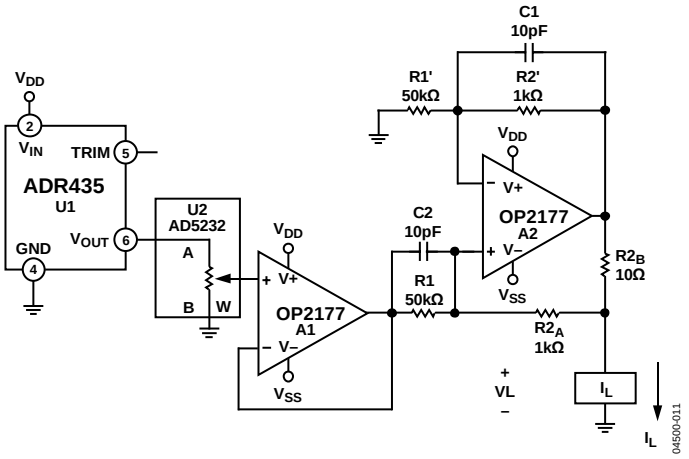


Figure 41. Programmable Current Source

PROGRAMMABLE DAC REFERENCE VOLTAGE

By employing a multichannel DAC, such as the AD7398, quad, 12-bit voltage output DAC, one of its internal DACs and an ADR43x voltage reference can be used as a common programmable V_{REFX} for the rest of the DACs. The circuit configuration is shown in Figure 42.

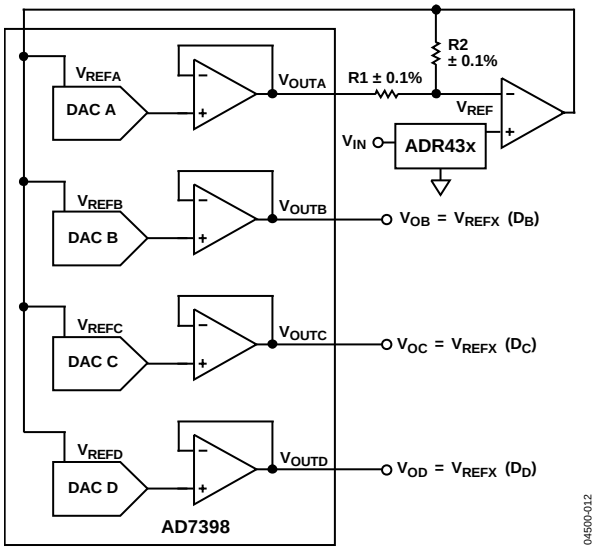


Figure 42. Programmable DAC Reference

The relationship of V_{REFX} to V_{REF} depends on the digital code and the ratio of R1 and R2, given by

$$V_{REFX} = \frac{V_{REF} \times \left(1 + \frac{R2}{R1}\right)}{\left(1 + \frac{D}{2^N} \times \frac{R2}{R1}\right)} \quad (6)$$

where:
D is the decimal equivalent of the input code.
N is the number of bits.
V_{REF} is the applied external reference.
V_{REFX} is the reference voltage for DAC A to DAC D.

Table 10. V_{REFX} vs. R1 and R2

R1, R2	Digital Code	V_{REF}
R1 = R2	0000 0000 0000	2 V_{REF}
R1 = R2	1000 0000 0000	1.3 V_{REF}
R1 = R2	1111 1111 1111	V_{REF}
R1 = 3R2	0000 0000 0000	4 V_{REF}
R1 = 3R2	1000 0000 0000	1.6 V_{REF}
R1 = 3R2	1111 1111 1111	V_{REF}

PRECISION VOLTAGE REFERENCE FOR DATA CONVERTERS

The ADR43x family has a number of features that make it ideal for use with ADCs and DACs. The exceptional low noise, tight temperature coefficient, and high accuracy characteristics make the ADR43x ideal for low noise applications, such as cellular base station applications.

Another example of an ADC for which the ADR431 is well suited is the AD7701. Figure 43 shows the ADR431 used as the precision reference for this converter. The AD7701 is a 16-bit ADC with on-chip digital filtering intended for the measurement of wide dynamic range and low frequency signals, such as those representing chemical, physical, or biological processes. It contains a charge-balancing Σ-Δ ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, and a serial communications port.

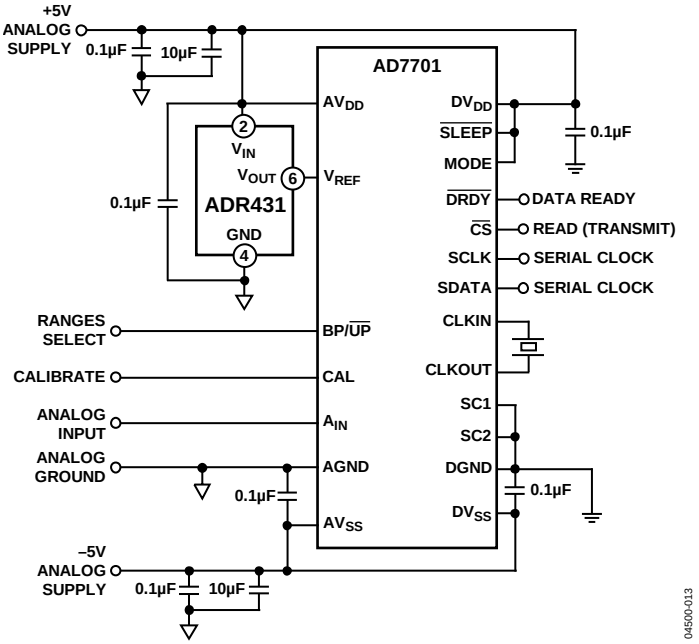


Figure 43. Voltage Reference for the AD7701 16-Bit ADC

PRECISION BOOSTED OUTPUT REGULATOR

A precision voltage output with boosted current capability can be realized with the circuit shown in Figure 44. In this circuit, U2 forces V_O to be equal to V_{REF} by regulating the turn-on of N1. Therefore, the load current is furnished by V_{IN}. In this configuration, a 50 mA load is achievable at a V_{IN} of 5 V. Moderate heat is generated on the MOSFET, and higher current can be achieved with a replacement of the larger device. In addition, for a heavy capacitive load with step input, a buffer can be added at the output to enhance the transient response.

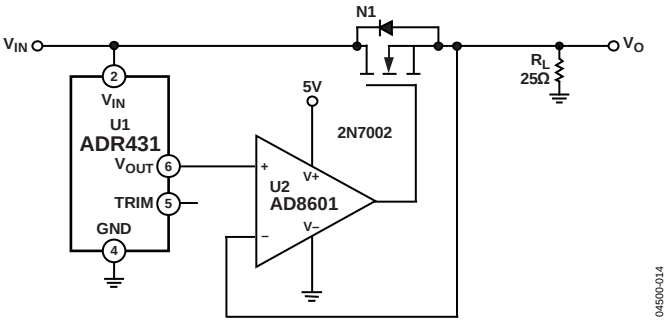
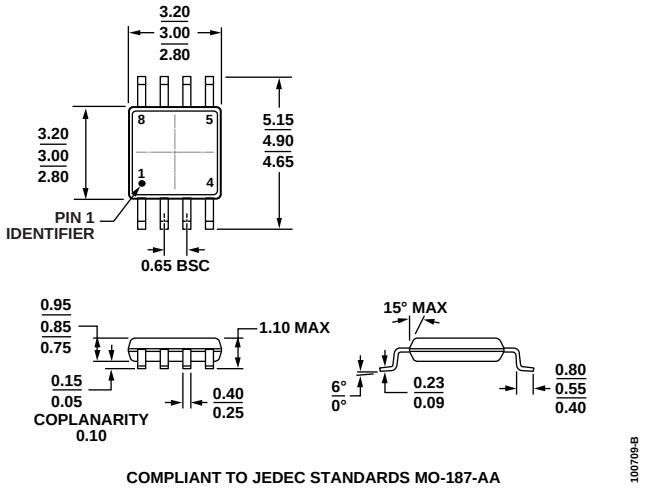


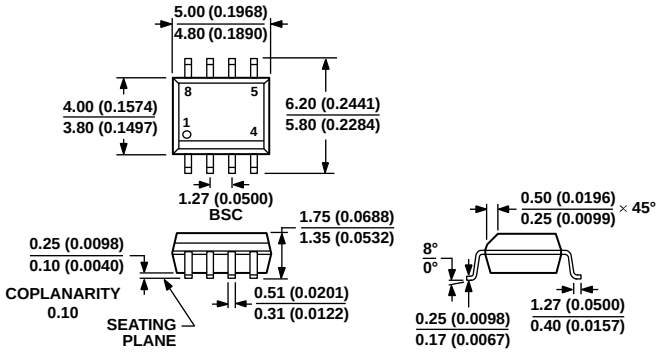
Figure 44. Precision Boosted Output Regulator

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 45. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 46. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Output Voltage (V)	Initial Accuracy, ± (mV)	Initial Accuracy, ± (%)	Temperature Coefficient Package (ppm/°C)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADR430ARZ	2.048	3	0.15	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR430ARZ-REEL7	2.048	3	0.15	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR430ARMZ	2.048	3	0.15	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R10
ADR430ARMZ-REEL7	2.048	3	0.15	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R10
ADR430BRZ	2.048	1	0.05	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR430BRZ-REEL7	2.048	1	0.05	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR431ARZ	2.500	3	0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR431ARZ-REEL7	2.500	3	0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR431ARMZ	2.500	3	0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R12
ADR431ARMZ-REEL7	2.500	3	0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R12
ADR431BR	2.500	1	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR431BR-REEL7	2.500	1	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR431BRZ	2.500	1	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR431BRZ-REEL7	2.500	1	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR433ARZ	3.000	4	0.13	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR433ARZ-REEL7	3.000	4	0.13	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR433ARMZ	3.000	4	0.13	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R14
ADR433ARMZ-REEL7	3.000	4	0.13	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R14
ADR433BRZ	3.000	1.5	0.05	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR433BRZ-REEL7	3.000	1.5	0.05	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR434ARZ	4.096	5	0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR434ARZ-REEL7	4.096	5	0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR434ARMZ	4.096	5	0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R16
ADR434ARMZ-REEL7	4.096	5	0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R16
ADR434BRZ	4.096	1.5	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR434BRZ-REEL7	4.096	1.5	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR435ARZ	5.000	6	0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR435ARZ-REEL7	5.000	6	0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR435ARMZ	5.000	6	0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	50	R18
ADR435ARMZ-REEL7	5.000	6	0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R18
ADR435BRZ	5.000	2	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADR435BRZ-REEL7	5.000	2	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR439ARZ-REEL7	4.500	5.5	0.12	10	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADR439ARMZ-REEL7	4.500	5.5	0.12	10	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	R1C
ADR439BRZ-REEL7	4.500	2	0.04	3	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	

[1] Z = RoHS Compliant Part.

NOTES

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