



**THE DATASHEET OF  
SN65EPT21DGKR**



## 3.3-V Differential PECL/LVDS to TTL Translator

Check for Samples: [SN65EPT21](#)

### FEATURES

- 1 ns Propagation Delay
- $F_{max} > 300\text{MHz}$
- Operating Range:  $V_{CC} = 3.0\text{ V to } 3.6\text{ V}$  with  $GND = 0\text{ V}$
- 24-mA TTL Output
- Built-In Temperature Compensation
- Drop-In Compatible to the MC10EPT21, MC100EPT21

### APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion for Clock or Data

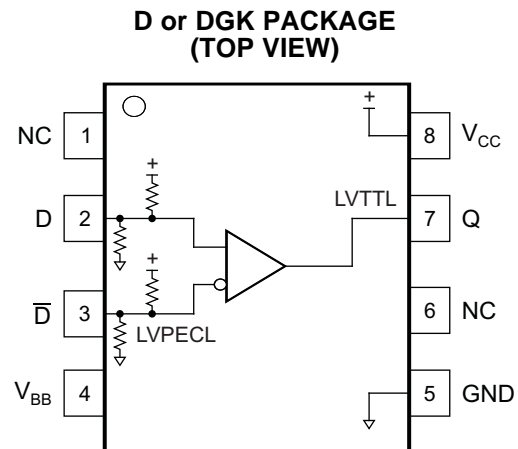
### DESCRIPTION

The SN65EPT21 is a differential PECL-to-TTL translator. It operates on +3.3 V supply and ground only. The device includes circuitry to maintain inputs at  $V_{CC}/2$  when left open.

The  $V_{BB}$  pin is a reference voltage output for the device. When the device is used in single-ended mode, the unused input should be tied to  $V_{BB}$ . This reference voltage can also be used to bias the input when it is ac coupled. When it is used, place a  $0.01\mu\text{F}$  decoupling capacitor between  $V_{CC}$  and  $V_{BB}$ . Also limit the sink/source current to  $< 0.5\text{ mA}$  to  $V_{BB}$ . Leave  $V_{BB}$  open when it is not used.

The SN65EPT21 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

### PIN ASSIGNMENT(Add pullup on BOTH inputs)


**Table 1. Pin Descriptions**

PIN	FUNCTION
Q	LVTTTL/LVCMOS Output
D, $\bar{D}$	Differential LVPECL/LVDS/CML Input
$V_{CC}$	Positive Supply
$V_{BB}$	Output Reference Voltage
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

### ORDERING INFORMATION<sup>(1)</sup>

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65EPT21D/DR	EPT21	SOIC	NiPdAu
SN65EPT21DGK/DGKR	SSSI	MSOP	NiPdAu

(1) Leaded device options are not initially available; contact a sales representative for further details.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL mode supply voltage	$V_{CC}$ (GND = 0 V)	3.8	V
Sink/source current, $V_{BB}$		$\pm 0.5$	mA
PECL input voltage	GND = 0 V, $V_I \leq V_{CC}$	0 to 3.8	V
Operating temperature range		-40 to 85	°C
Storage temperature range		-65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
MSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

## THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$\theta_{JB}$	Junction-to-board thermal resistance	SOIC	79		°C/W
		MSOP	120		
$\theta_{JC}$	Junction-to-case thermal resistance	SOIC	98		°C/W
		MSOP	74		

## KEY ATTRIBUTES

CHARACTERISTICS	VALUE	
Internal input pull-down resistor	50 k $\Omega$	
Internal input pull-up resistor	50 k $\Omega$	
Moisture sensitivity level	Level 1	
Flammability rating (oxygen index: 28 to 34)	UL 94 V-0 at 0.125 in	
Electrostatic discharge	Human body model	2 kV
	Charged-device model	2 kV
	Machine mode	200 V
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test		

## PECL DC CHARACTERISTICS

At  $V_{CC} = 3.3\text{ V}$ ,  $GND = 0.0\text{ V}$  (unless otherwise noted)<sup>(1) (2)</sup>

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ\text{C}$			$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IH}$	High-level input voltage, single-ended	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Low-level input voltage, single-ended	1355		1675	1355		1675	1355		1675	mV
$V_{BB}$	Output reference voltage	1910	2009	2160	1910	2034	2160	1910	2026	2160	mV
$V_{IHCMR}$	High-level input voltage, common-mode range, differential	See <sup>(3)</sup>			1.2		3.3	1.2		3.3	V
$I_{IH}$	High-level input current			150			150			150	$\mu\text{A}$
$I_{IL}$	Low-level input current	-150			-150			-150			$\mu\text{A}$

(1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

(2) Input parameters vary 1:1 with  $V_{CC}$ .

(3)  $V_{IHCMR(\min)}$  varies 1:1 with  $GND$ ,  $V_{IHCMR(\max)}$  varies 1:1 with  $V_{CC}$ .  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal

## TTL DC CHARACTERISTICS

At  $V_{CC} = 3.3\text{ V}$ ,  $GND = 0.0$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CCH}$	Power supply current Output is HIGH	5	9	20	mA
$I_{CCL}$	Power supply current Output is LOW	8	7.5	26	mA
$V_{OH}$	High-level output voltage $I_{OH} = -3.0\text{ mA}$	2.4	3.05		V
$V_{OL}$	Low-level output voltage $I_{OL} = 24\text{ mA}$		0.32	0.5	V
$I_{OS}$	Output short circuit current	-180	-100	-80	mA

(1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

## AC CHARACTERISTICS

At  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $GND = 0.0\text{ V}$  (unless otherwise noted)<sup>(1) (2)</sup>

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ\text{C}$			$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{MAX}$	Maximum switching frequency (Figure 1–Figure 3)	300			300			300			MHz
$t_{PLH}$	Propagation delay At 1.5 V	1000	1394	1800	1000	1444	1800	1000	1481	1800	ps
$t_{PHL}$	Propagation delay At 1.5 V	1000	1140	1900	1000	1280	1900	1000	1421	1900	ps
$t_{JITTER}$	Random clock jitter (RMS)		2.25	5		3.2	5		3.4	5	ps
$t_{SKEW}$	Duty Cycle Skew <sup>(3)</sup>		94	250		78	250		62	250	ps
$t_{SKPP}$	Part-to-Part Skew <sup>(3)</sup>			500			500			500	ps
$V_{PP}$	Input swing See <sup>(4)</sup>	150		1200	150		1200	150		1200	mV
$t_r/t_f$	Output rise/fall times $Q, \bar{Q}$ (0.8V - 2.0V))	250	500	900	250	500	900	250	500	900	ps

(1) The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

(2)  $R_L = 500\ \Omega$  to  $GND$  and  $C_L = 20\text{ pF}$  to  $GND$ . See Figure 4. Measured with 750mV, 50% duty cycle clock source

(3) Skews are measured between outputs under identical transitions

(4)  $V_{PP(\min)}$  is minimum input swing for which ac parameters are assured.

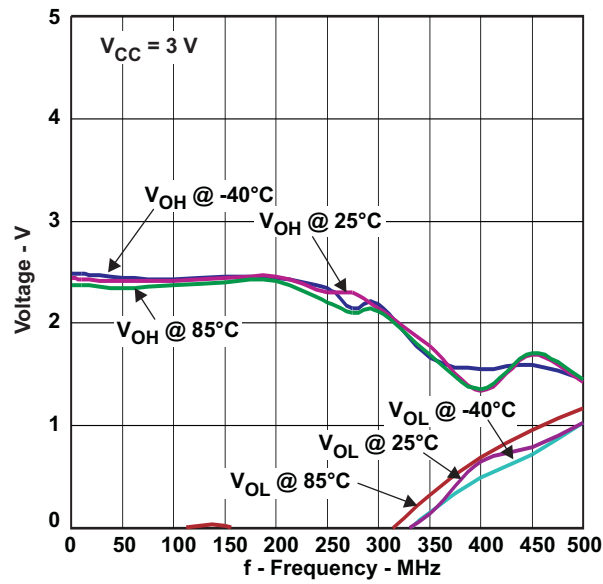


Figure 1. Maximum Switching Frequency  $V_{CC} = 3.0\text{ V}$

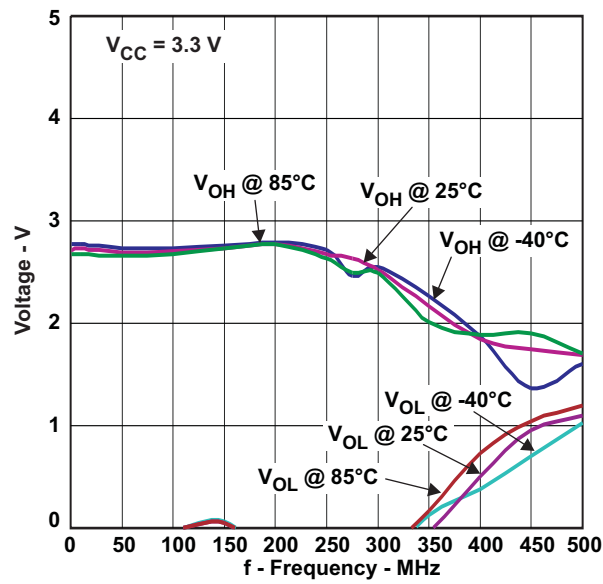


Figure 2. Maximum Switching Frequency  $V_{CC} = 3.3\text{ V}$

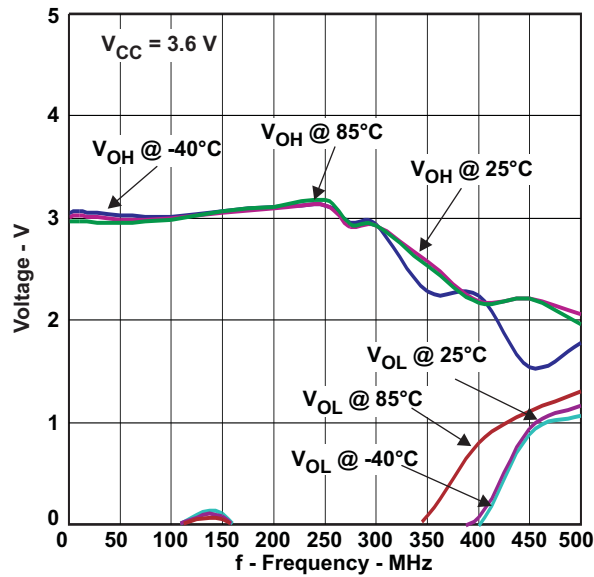


Figure 3. Maximum Switching Frequency  $V_{CC} = 3.6\text{ V}$

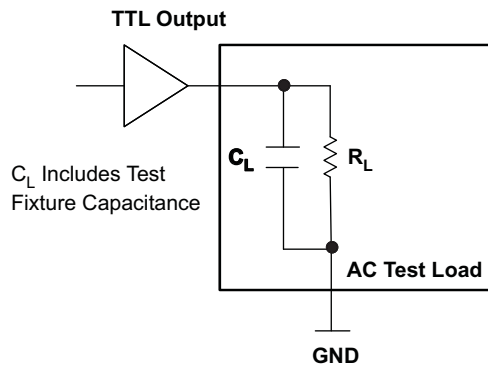


Figure 4. TTL Output AC Test Loading Condition

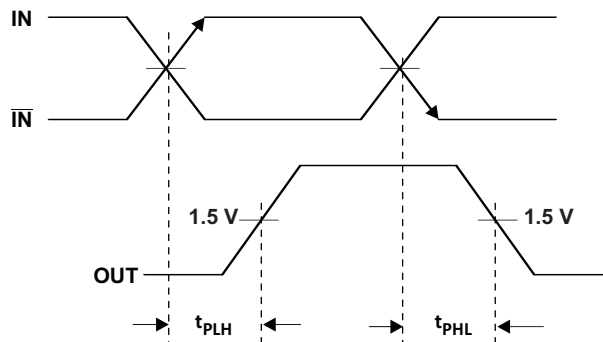
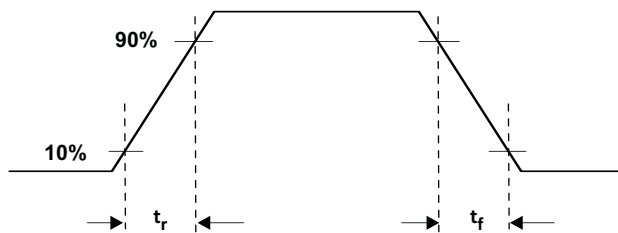


Figure 5. Output Propagation Delay



**Figure 6. Output Rise and Fall Times**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65EPT21D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT21	<a href="#">Samples</a>
SN65EPT21DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SSSI	<a href="#">Samples</a>
SN65EPT21DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   Call TI	Level-1-260C-UNLIM	-40 to 85	SSSI	<a href="#">Samples</a>
SN65EPT21DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT21	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65EPT21DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65EPT21DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65EPT21DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65EPT21DR	SOIC	D	8	2500	367.0	367.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

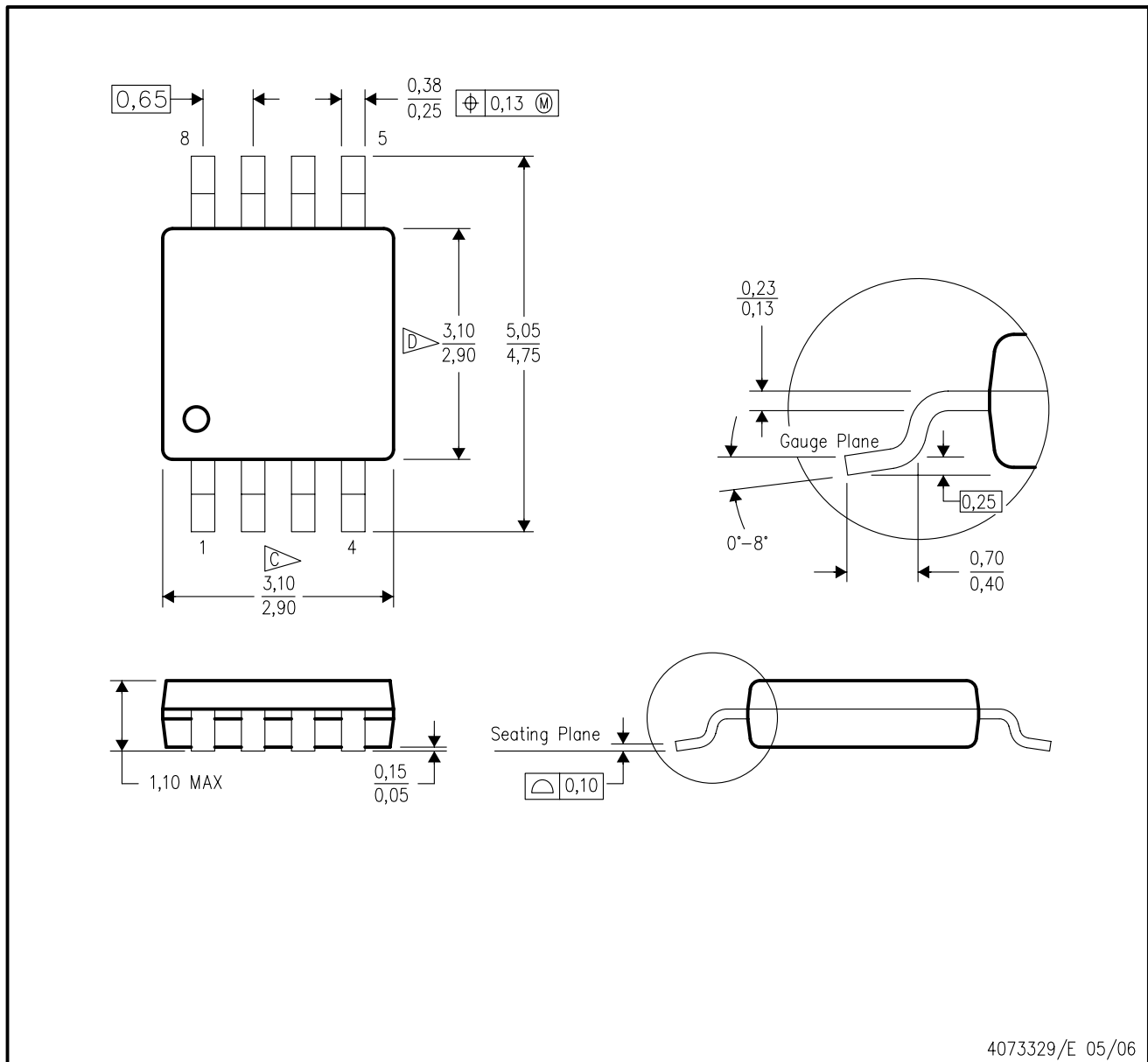
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

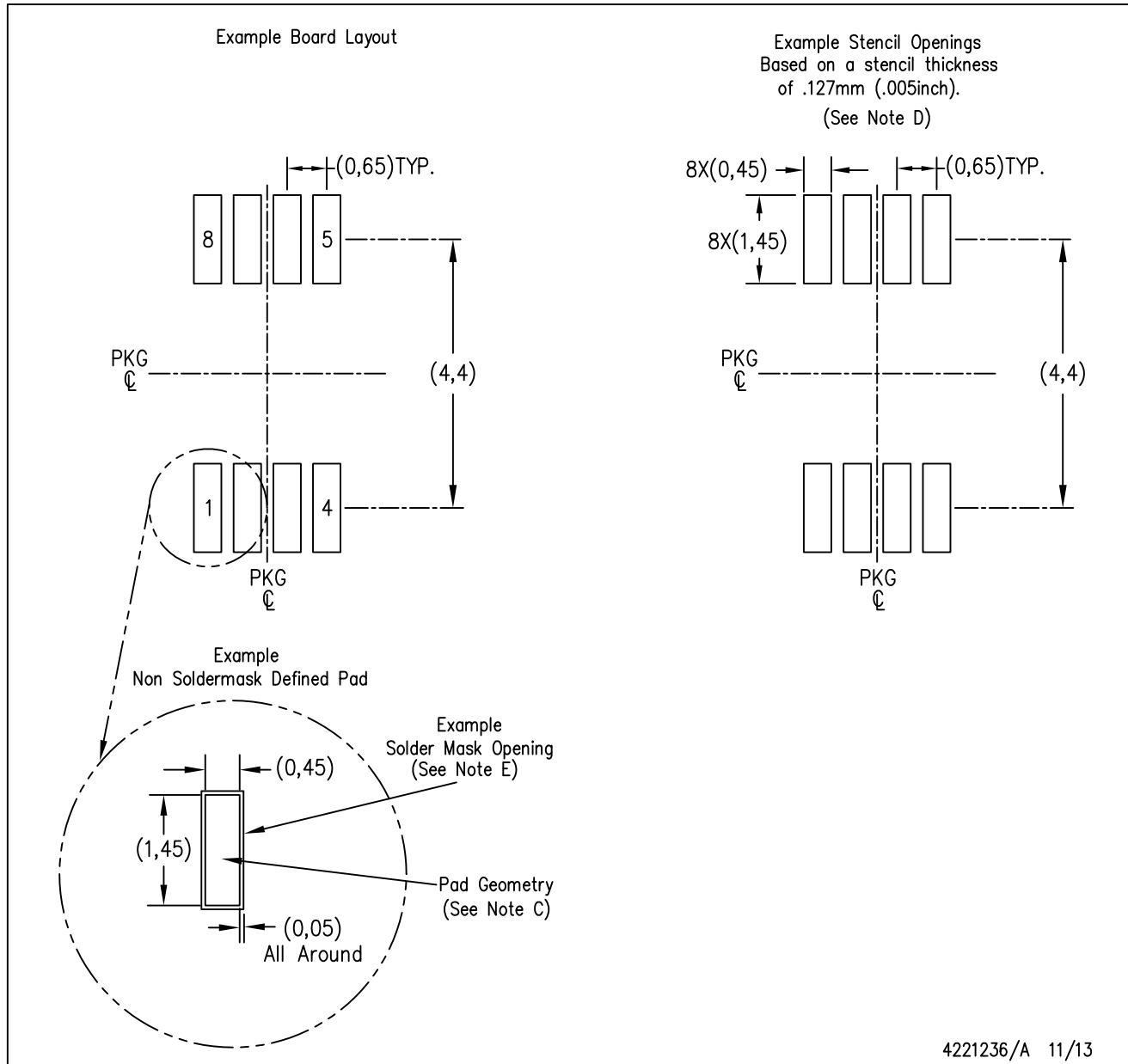
DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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