



**THE DATASHEET OF
IPW60R070P6**



MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ P6

600V CoolMOS™ P6 Power Transistor
IPW60R070P6

Data Sheet

Rev. 2.0
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ P6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

Features

- Increased MOSFET dv/dt ruggedness
- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

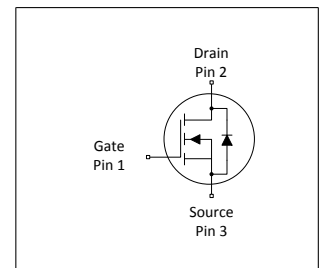
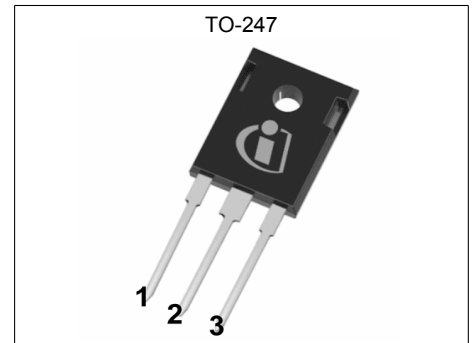


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	70	mΩ
$Q_{g,typ}$	100	nC
$I_{D,pulse}$	156	A
$E_{oss@400V}$	12.3	μJ
Body diode di/dt	300	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPW60R070P6	PG-TO 247	6R070P6	see Appendix A

Table of Contents

Description	2
Maximum ratings	4
Thermal characteristics	5
Electrical characteristics	6
Electrical characteristics diagrams	8
Test Circuits	12
Package Outlines	13
Appendix A	14
Revision History	15
Disclaimer	15

2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	53.5 33.8	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	156	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	1136	mJ	$I_D=9.3\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	1.72	mJ	$I_D=9.3\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, repetitive	I_{AR}	-	-	9.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation (Non FullPAK) TO-247	P_{tot}	-	-	391	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque (Non FullPAK) TO-247	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	46.3	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	156	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di_i/dt	-	-	300	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics (Non FullPAK) TO-247

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.32	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3.5	4.0	4.5	V	$V_{DS}=V_{GS}$, $I_D=1.72\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	5	μA	$V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.063 0.164	0.070 -	Ω	$V_{GS}=10\text{V}$, $I_D=20.6\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=20.6\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	1	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4750	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$
Output capacitance	C_{oss}	-	190	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	150	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	703	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=25.8\text{A}$, $R_G=1.7\Omega$; see table 9
Rise time	t_r	-	15	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=25.8\text{A}$, $R_G=1.7\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	64	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=25.8\text{A}$, $R_G=1.7\Omega$; see table 9
Fall time	t_f	-	4	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=25.8\text{A}$, $R_G=1.7\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	30	-	nC	$V_{DD}=400\text{V}$, $I_D=25.8\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	35	-	nC	$V_{DD}=400\text{V}$, $I_D=25.8\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	100	-	nC	$V_{DD}=400\text{V}$, $I_D=25.8\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	6.1	-	V	$V_{DD}=400\text{V}$, $I_D=25.8\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=25.8A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	520	-	ns	$V_R=400V, I_F=25.8A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	12	-	μC	$V_R=400V, I_F=25.8A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	44	-	A	$V_R=400V, I_F=25.8A, di_F/dt=100A/\mu s$; see table 8

5 Electrical characteristics diagrams

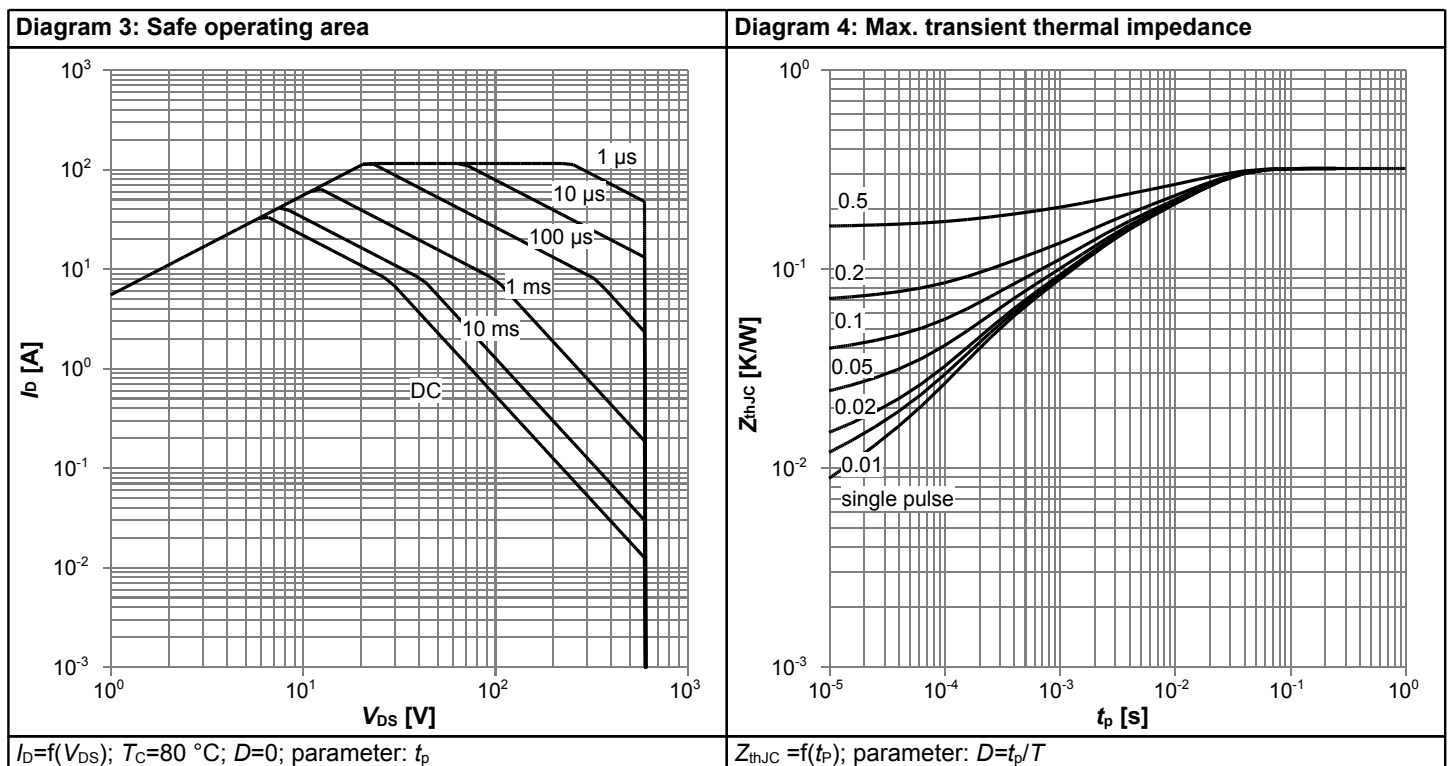
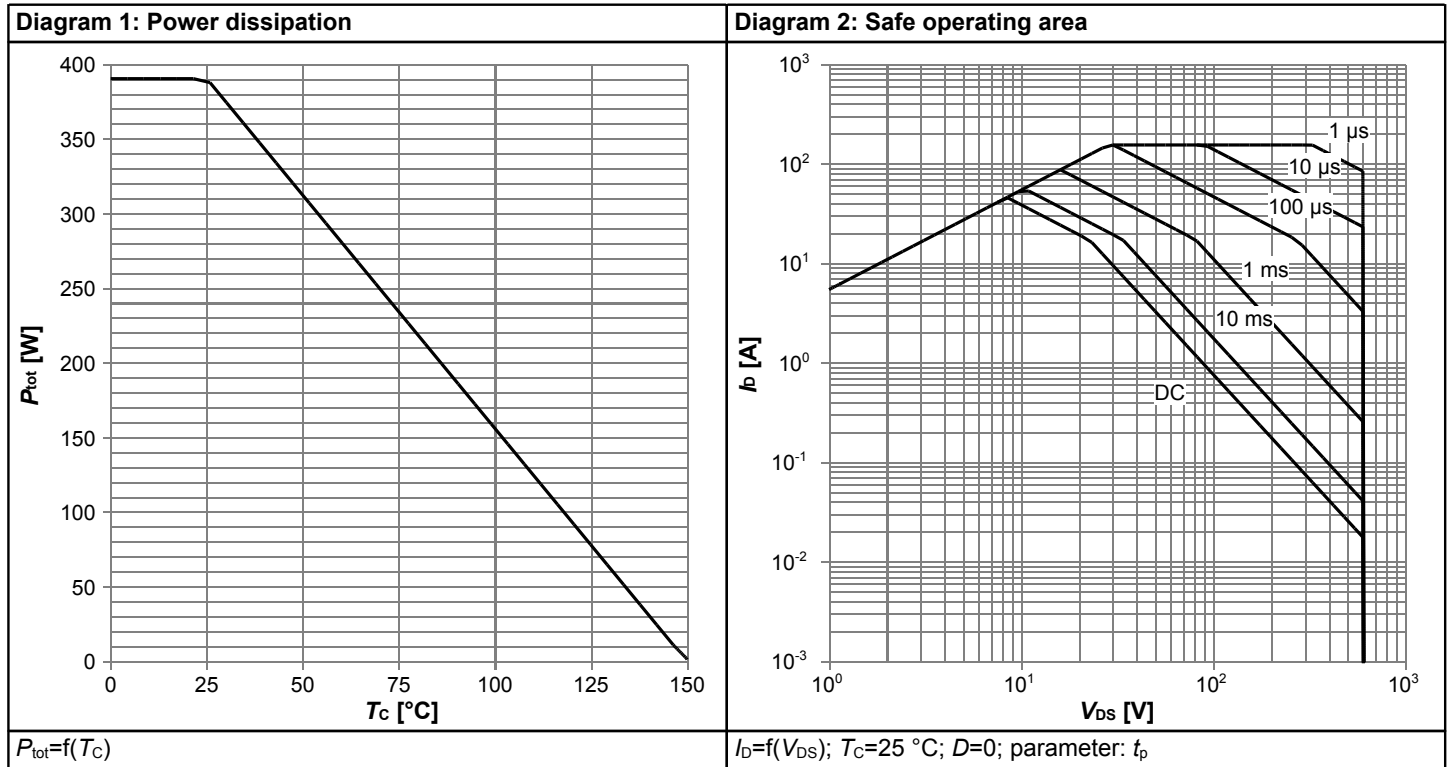
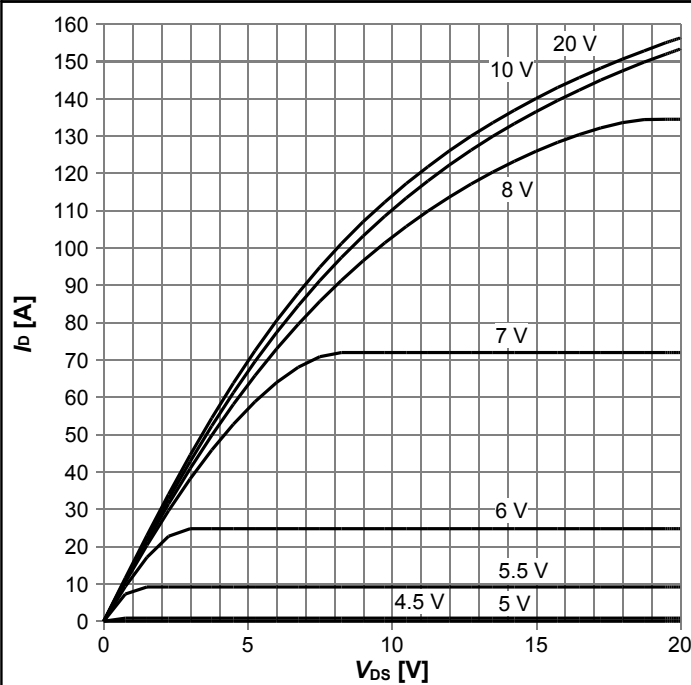
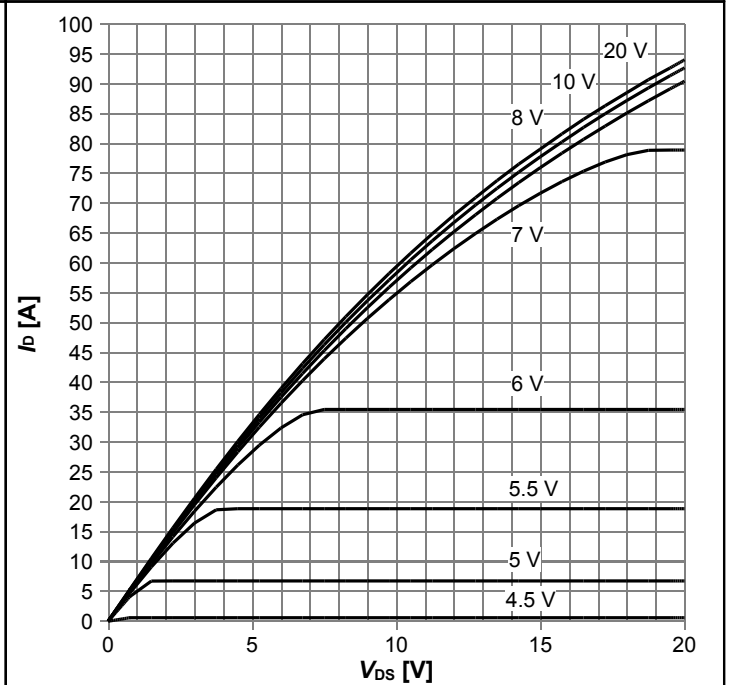


Diagram 5: Typ. output characteristics



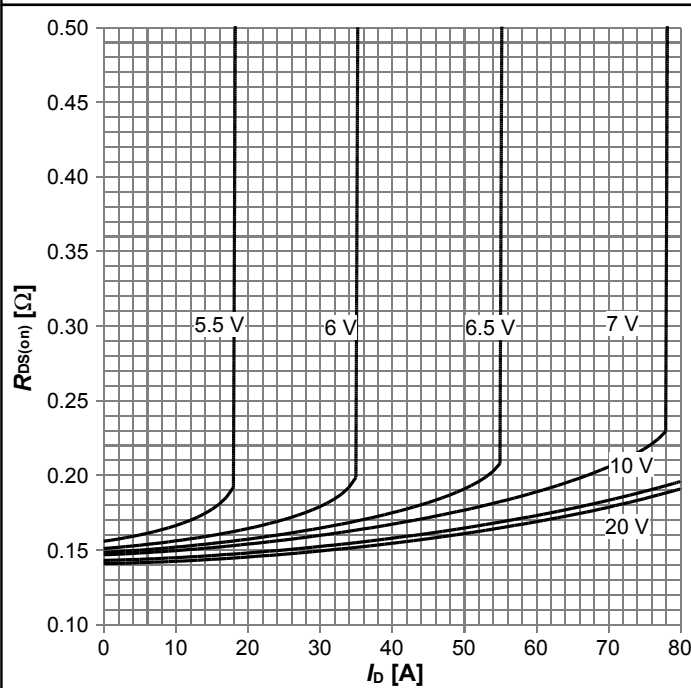
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 6: Typ. output characteristics



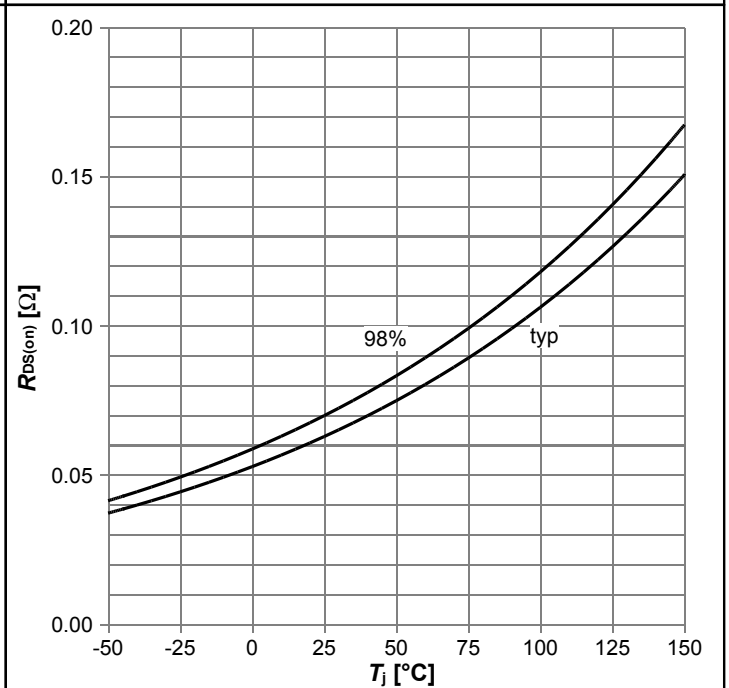
$I_D=f(V_{DS}); T_j=125\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



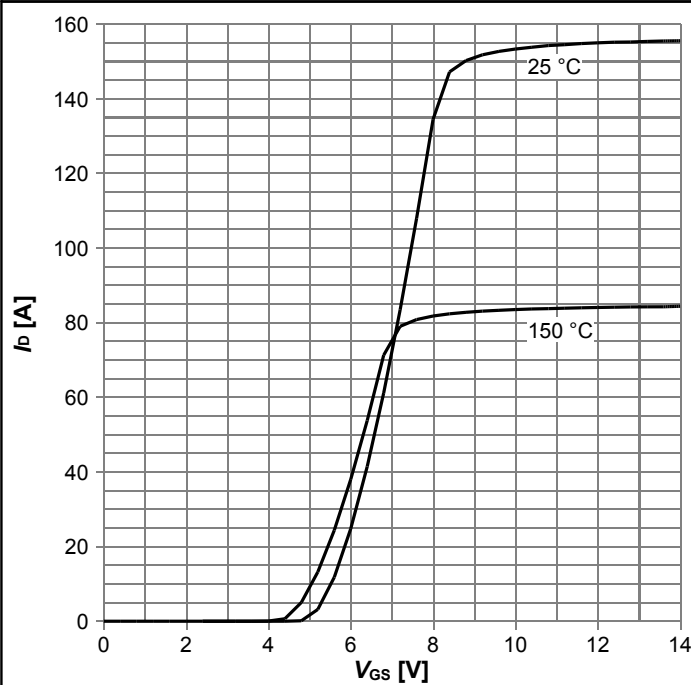
$R_{DS(on)}=f(I_D); T_j=125\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



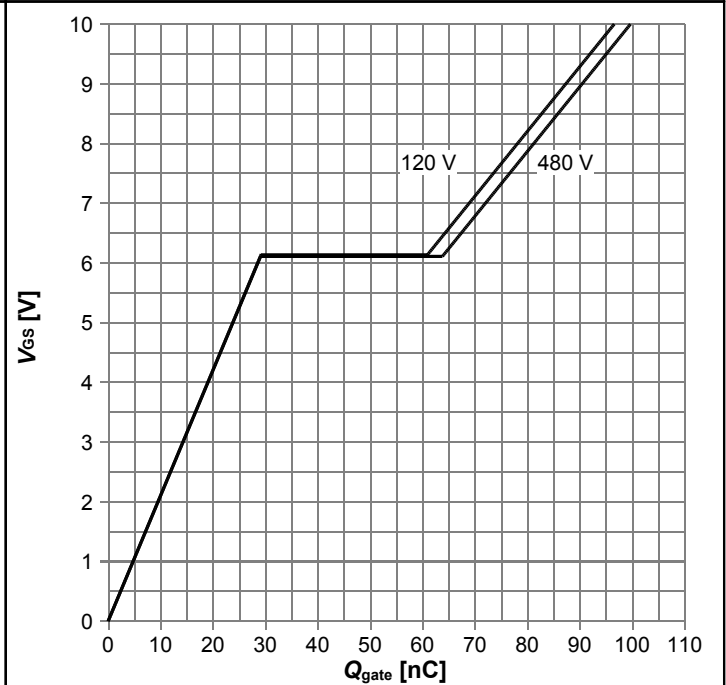
$R_{DS(on)}=f(T_j); I_D=20.6\text{ A}; V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



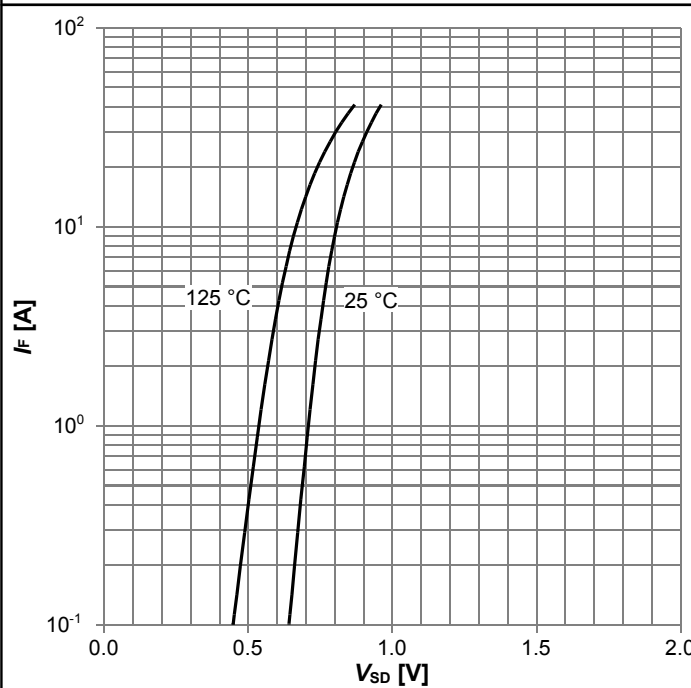
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



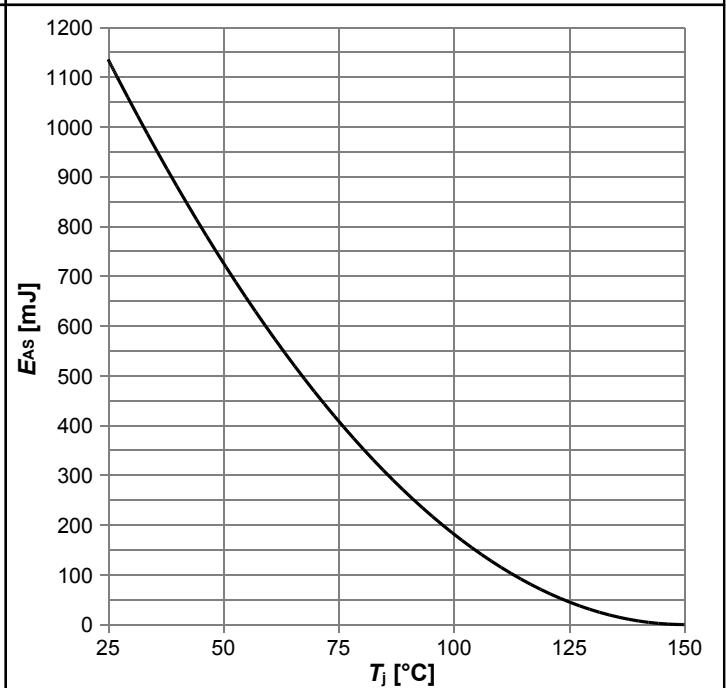
$V_{GS}=f(Q_{gate}); I_D=25.8 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



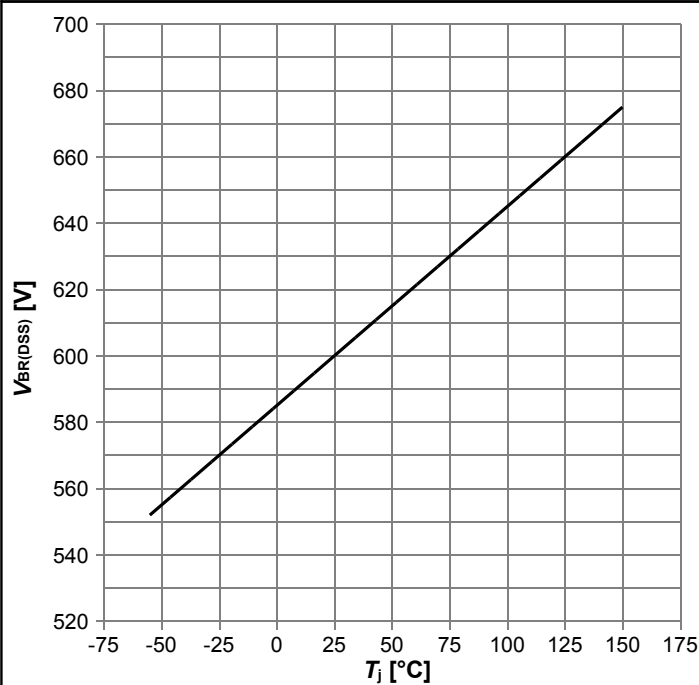
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



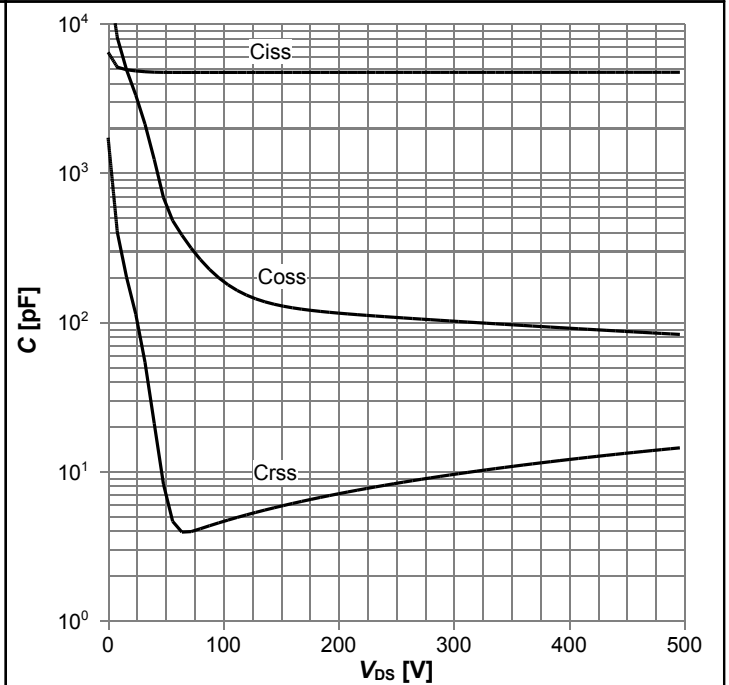
$E_{AS}=f(T_j); I_D=9.3 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



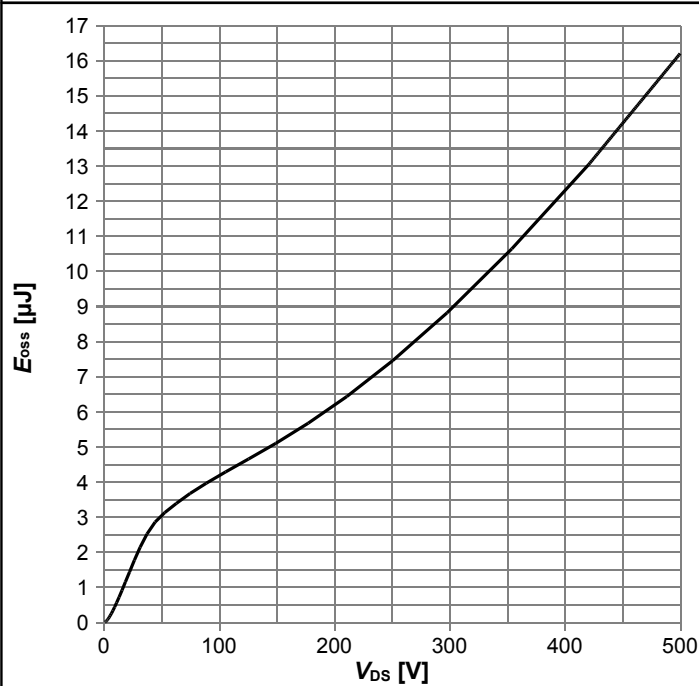
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

6 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform

Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

7 Package Outlines

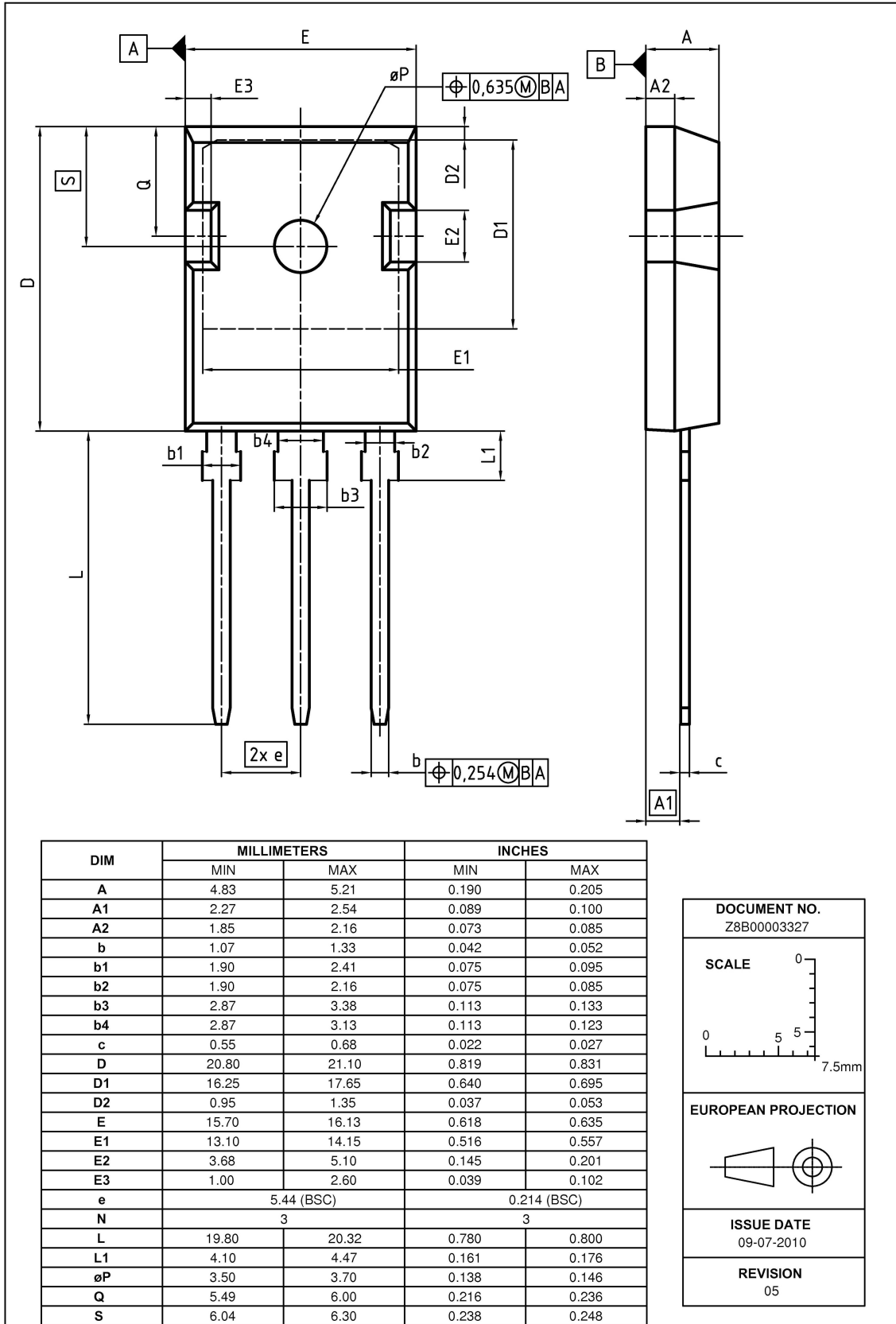


Figure 1 Outline PG-TO 247, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS™ P6 Webpage: www.infineon.com
- IFX CoolMOS™ P6 application note: www.infineon.com
- IFX CoolMOS™ P6 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPW60R070P6

Revision: 2014-03-07, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-03-07	Release of final version

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