



**THE DATASHEET OF
TLV2252AIDG4**



TLV225x, TLV225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

- Output Swing Includes Both Supply Rails
- Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Very Low Power . . . 34 μA Per Channel Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage
850 μV Max at T_A = 25°C
- Wide Supply Voltage Range
2.7 V to 8 V
- Macromodel Included
- Available in Q-Temp Automotive
HighRel Automotive Applications
Configuration Control / Print Support
Qualification to Automotive Standards

description

The TLV2252 and TLV2254 are dual and quadruple low-voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV225x family consumes only 34 μA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. The TLV225x has a noise level of 19 nV/√Hz at 1kHz, four times lower than competitive micropower solutions.

The TLV225x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV225xA family is available and has a maximum input offset voltage of 850 μV.

The TLV2252/4 also make great upgrades to the TLV2322/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

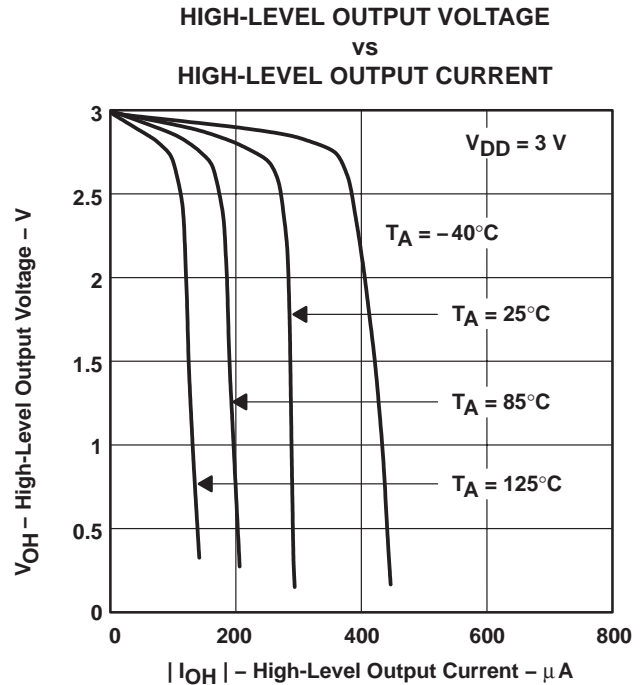


Figure 1



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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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TLV2252 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLATPACK (U)
-40°C to 125°C	850 µV 1500 µV	TLV2252AID TLV2252ID	— —	— —	TLV2252AIP TLV2252IP	TLV2252AIPWLE —	— —
-40°C to 125°C	850 µV 1500 µV	TLV2252AQD TLV2252QD	— —	— —	— —	— —	— —
-55°C to 125°C	850 µV 1500 µV	— —	TLV2252AMFK TLV2252MFK	TLV2252AMJG TLV2252MJG	— —	— —	TLV2252AMU TLV2252MU

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2252CDR).

‡ The PW package is available only left-end taped and reeled.

§ Chips are tested at 25°C.

TLV2254 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLATPACK (W)
-40°C to 125°C	850 µV 1500 µV	TLV2254AID TLV2254ID	— —	— —	TLV2254AIN TLV2254IN	TLV2254AIPWLE —	— —
-40°C to 125°C	850 µV 1500 µV	TLV2254AQD TLV2254QD	— —	— —	— —	— —	— —
-55°C to 125°C	850 µV 1500 µV	— —	TLV2254AMFK TLV2254MFK	TLV2254AMJ TLV2254MJ	— —	— —	TLV2254AMW TLV2254MW

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2254CDR).

‡ The PW package is available only left-end taped and reeled.

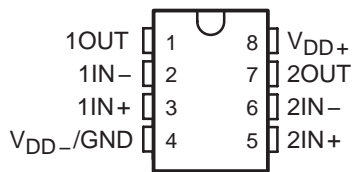
§ Chips are tested at 25°C.



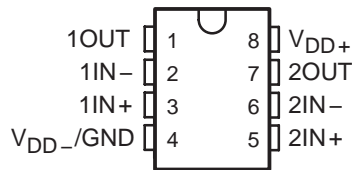
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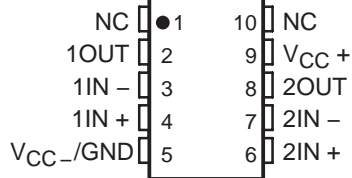
**TLV2252I, TLV2252AI
TLV2252Q, TLV2252AQ
D, P, OR PW PACKAGE
(TOP VIEW)**



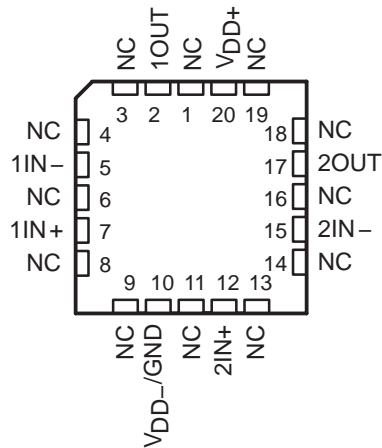
**TLV2252M, TLV2252AM . . . JG PACKAGE
(TOP VIEW)**



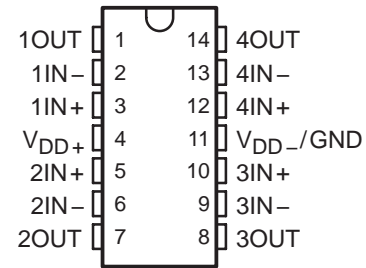
**TLV2252M, TLV2252AM . . . U PACKAGE
(TOP VIEW)**



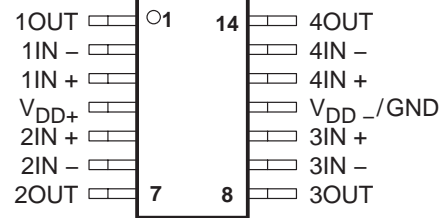
**TLV2252M, TLV2252AM . . . FK PACKAGE
(TOP VIEW)**



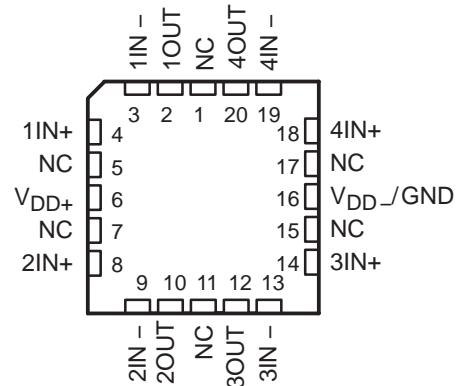
**TLV2254I, TLV2254AI, TLV2254Q, TLV2254AQ . . . D OR N PACKAGE
TLV2254M, TLV2254AM . . . J OR W PACKAGE
(TOP VIEW)**



**TLV2254I, TLV2254AI . . . PW PACKAGE
(TOP VIEW)**



**TLV2254M, TLV2254AM . . . FK PACKAGE
(TOP VIEW)**



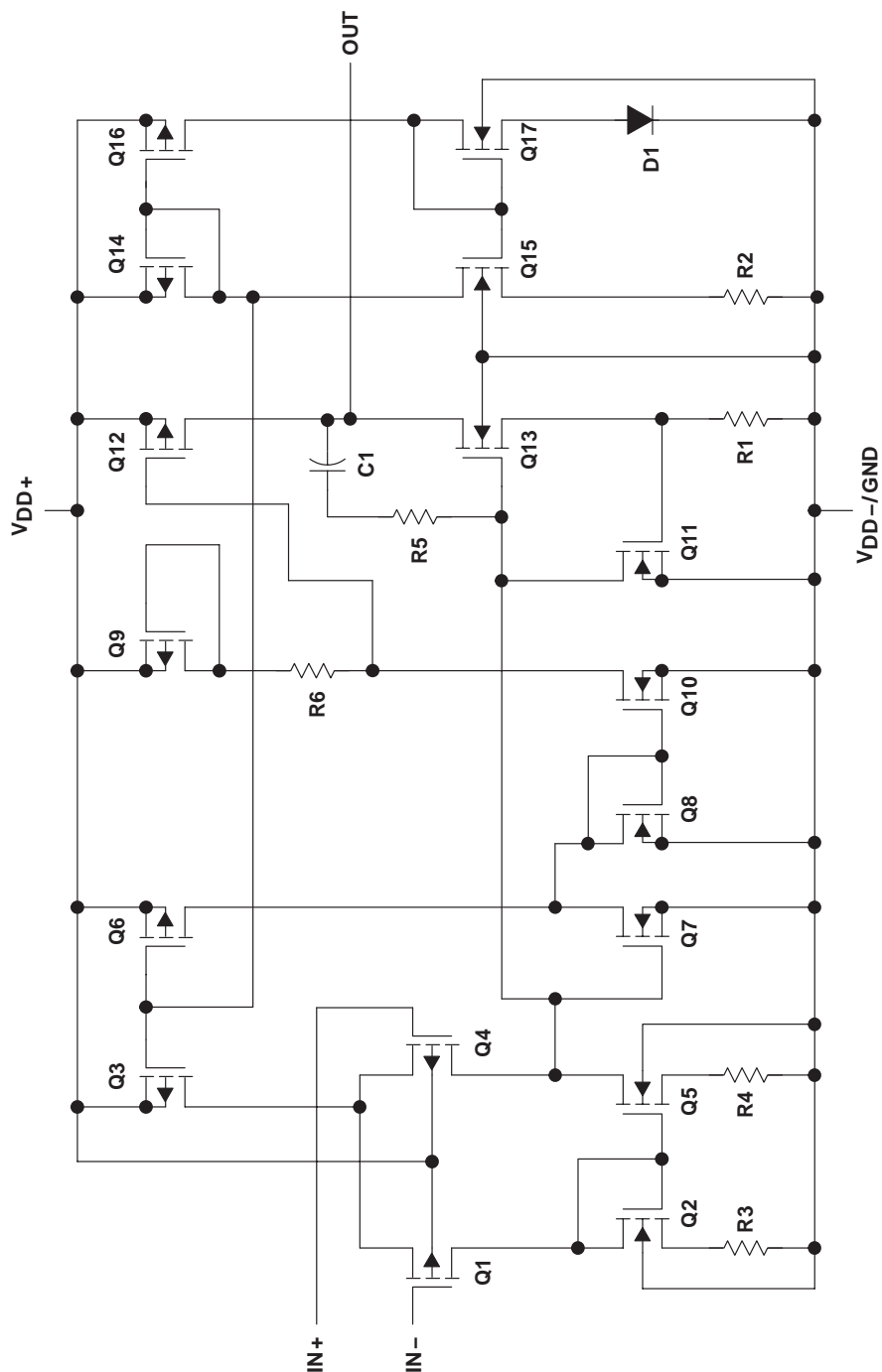
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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLV2252	TLV2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	16 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	$V_{DD-} - 0.3 \text{ V to } V_{DD+}$
Input current, I_I (each input)	$\pm 5 \text{ mA}$
Output current, I_O	$\pm 50 \text{ mA}$
Total current into V_{DD+}	$\pm 50 \text{ mA}$
Total current out of V_{DD-}	$\pm 50 \text{ mA}$
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : I Suffix	-40°C to 125°C
Q Suffix	-40°C to 125°C
M Suffix	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, and PW packages	260°C
J, JG, U, and W packages	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-} .
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3 \text{ V}$.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D-8	725 mW	5.8 mW/°C	377 mW	145 mW
D-14	950 mW	7.6 mW/°C	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
J	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
N	1150 mW	9.2 mW/°C	598 mW	230 mW
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW-8	525 mW	4.2 mW/°C	273 mW	105 mW
PW-14	700 mW	5.6 mW/°C	364 mW	140 mW
U	700 mW	5.5 mW/°C	370 mW	150 mW
W	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions

	TLV225xI		TLV225xQ		TLV225xM		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	8	2.7	8	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	-40	125	-40	125	-55	125	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-} .



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TLV2252I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage		25°C	200	1500		200	850	μV	
		Full range			1750		1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current	$V_{DD\pm} = \pm 1.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	0.5	60		0.5	60	pA	
		-40°C to 85°C			150		150		
		Full range			1000		1000		
I_{IB} Input bias current		25°C	1	60		1	60	pA	
		-40°C to 85°C			150		150		
		Full range			1000		1000		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2	V	
		Full range	0 to 1.7			0 to 1.7			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	2.98		2.98		V		
	$I_{OH} = -75\ \mu\text{A}$	25°C	2.9		2.9				
	$I_{OH} = -150\ \mu\text{A}$	Full range	2.8		2.8				
		25°C	2.8		2.8				
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	10		10		mV		
		Full range	80		80				
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	100		100				
		Full range	150		150				
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C	200		200				
		Full range	300		300				
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to } 2\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	250	100	250	V/mV	
			Full range	10		10			
		$R_L = 1\text{ M}\Omega$ ‡	25°C	800		800			
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²		10 ¹²		Ω		
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²		10 ¹²		Ω		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C	8		8		pF		
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	220		220		Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C	65	75	65	77	dB		
		Full range	60		60				

† Full range is -40°C to 125°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2252I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV2252I			TLV2252AI			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	100	dB	
			Full range	80			80			
I_{DD}	Supply current	$V_O = 1.5\text{ V}$, No load	25°C		68	125		68	125	μA
			Full range			150			150	

† Full range is –40°C to 125°C.

TLV2252I operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.1\text{ V to } 1.9\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.1		0.07	0.1	V/μs
			Full range	0.05			0.05		
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		35		35	nV/√Hz	
			25°C		19		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to } 1\text{ Hz}$ $f = 0.1\text{ Hz to } 10\text{ Hz}$	25°C		0.6		0.6	μV	
			25°C		1.1		1.1		
I_n	Equivalent input noise current		25°C		0.6		0.6	fA/√Hz	
	Gain-bandwidth product	$f = 1\text{ kHz}$, $C_L = 100\text{ pF}$ ‡, $R_L = 50\text{ k}\Omega$ ‡	25°C		0.187		0.187	MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C		60		60	kHz	
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		63°		63°		
	Gain margin		25°C		15		15	dB	

† Full range is –40°C to 125°C.

‡ Referenced to 1.5 V

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TLV2252I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage		25°C	200	1500		200	850	μV	
		Full range			1750		1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	0.5		60	0.5		60	pA
		-40°C to 85°C	150			150			
		Full range	1000			1000			
I_{IB} Input bias current		25°C	1		60	1		60	pA
		-40°C to 85°C	150			150			
		Full range	1000			1000			
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5		0 to 3.5				
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98		4.98		V		
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94	4.9	4.94			
	Full range	4.8		4.8					
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01		0.01		V		
		Full range	0.06		0.06				
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15	0.09	0.15			
		Full range	0.15		0.15				
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C	0.2	0.3	0.2	0.3			
		Full range	0.3		0.3				
AVD Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	350	100	350	V/mV	
		$R_L = 1\text{ M}\Omega$ ‡	Full range	10		10			
			25°C	1700		1700			
$r_{i(d)}$ Differential input resistance		25°C	10^{12}			10^{12}		Ω	
$r_{i(c)}$ Common-mode input resistance		25°C	10^{12}			10^{12}		Ω	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C	8			8		pF	
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	200			200		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70		70				

† Full range is -40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2252I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV2252I			TLV2252AI			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95	dB	
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5\text{ V}$, No load	25°C		70	125		70	125	μA
			Full range			150			150	

† Full range is – 40°C to 125°C.

TLV2252I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.12		0.07	0.12	$\text{V}/\mu\text{s}$
			Full range	0.05			0.05		
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		36			36	$\text{nV}/\sqrt{\text{Hz}}$
			25°C		19			19	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		0.7			0.7	μV
			25°C		1.1			1.1	
I_n	Equivalent input noise current		25°C		0.6			0.6	$\text{fA}/\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$	25°C		0.2%		0.2%	
			$A_V = 10$			1%		1%	
	Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡,	25°C		0.2		0.2	MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡,	$A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C		30		30	kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C		63°		63°	
				25°C		15		15	dB

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

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TLV2254I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2254I			TLV2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 1.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	200	1500		200	850	μV	
		Full range		1750		1000			
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		-40°C to 85°C		150		150			
		Full range		1000		1000			
I_{IB} Input bias current		25°C	1	60		1	60	pA	
		-40°C to 85°C		150		150			
		Full range		1000		1000			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2	V	
		Full range	0 to 1.7			0 to 1.7			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -75\ \mu\text{A}$ $I_{OH} = -150\ \mu\text{A}$	25°C		2.98		2.98		V	
		25°C	2.9			2.9			
		Full range	2.8			2.8			
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ $V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ $V_{IC} = 1.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C		10		10		mV	
		Full range		80		80			
		25°C	100			100			
		Full range	150			150			
		25°C	200			200			
		Full range	300			300			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to }2\text{ V}$	25°C	$R_L = 100\ \text{k}\Omega$ ‡		100	225	100	225	V/mV
			Full range		10		10		
		25°C	$R_L = 1\ \text{M}\Omega$ ‡		800		800		
$r_{i(d)}$ Differential input resistance		25°C		10 ¹²		10 ¹²	Ω		
$r_{i(c)}$ Common-mode input resistance		25°C		10 ¹²		10 ¹²	Ω		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}$, N package	25°C		8		8	pF		
Z_o Closed-loop output impedance	$f = 25\ \text{kHz}$, $A_V = 10$	25°C		220		220	Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C	65	75		65	77	dB	
		Full range	60			60			

† Full range is -40°C to 125°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2254I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV2254I			TLV2254AI			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	100	dB	
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 1.5\text{ V}$, No load	25°C		135	250		135	250	μA
			Full range			300			300	

† Full range is – 40°C to 125°C.

TLV2254I operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2254I			TLV2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 0.7\text{ V to } 1.7\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.1		0.07	0.1	V/μs
			Full range	0.05			0.05		
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		35		35	nV/√Hz	
			25°C		19		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to } 1\text{ Hz}$ $f = 0.1\text{ Hz to } 10\text{ Hz}$	25°C		0.6		0.6	μV	
			25°C		1.1		1.1		
I_n	Equivalent input noise current		25°C		0.6		0.6	fA/√Hz	
	Gain-bandwidth product	$f = 1\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		0.187		0.187	MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $A_V = 1$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		60		60	kHz	
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		63°		63°		
	Gain margin		25°C		15		15	dB	

† Full range is – 40°C to 85°C.

‡ Referenced to 1.5 V

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TLV2254I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2254I			TLV2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	200	1500		200	850	μV	
		Full range		1750		1000			
αV_{IO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		–40°C to 85°C		150		150			
		Full range		1000		1000			
I_{IB} Input bias current		25°C	1	60		1	60	pA	
	–40°C to 85°C		150		150				
	Full range		1000		1000				
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98			4.98	V		
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		4.9		4.94	
		Full range	4.8			4.8			
	$I_{OH} = -150\ \mu\text{A}$	25°C	4.8	4.88		4.8		4.88	
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01			0.01	V		
		Full range		0.06		0.06			
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		0.09		0.15	
		Full range		0.15		0.15			
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C	0.2	0.3		0.2		0.3	
		Full range		0.3		0.3			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	350		100	350	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega$ ‡	25°C	1700			1700		
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²	Ω		
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²	Ω		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C	8			8	pF		
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	200			200	Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70			70			

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2254I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV2254I			TLV2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C		140	250		140	250	μA
		Full range			300			300	

† Full range is – 40°C to 125°C.

TLV2254I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2254I			TLV2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.4\text{ V to }2.6\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.12		0.07	0.12		V/μs
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	f = 10 Hz f = 1 kHz	25°C		36			36		nV/√Hz
		25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz f = 0.1 Hz to 10 Hz	25°C		0.7			0.7		μV
		25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6	fA/√Hz	
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, f = 20 kHz, $R_L = 50\text{ k}\Omega$ ‡	25°C	$A_V = 1$		0.2%		0.2%		
			$A_V = 10$		1%		1%		
Gain-bandwidth product	f = 50 kHz, $C_L = 100\text{ pF}$ ‡	25°C		0.2			0.2	MHz	
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡	25°C		30			30	kHz	
ϕ_m Phase margin at unity gain Gain margin	$R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		63°			63°		
		25°C		15			15	dB	

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

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TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage		25°C	200	1500		200	850	μV	
		Full range		1750		1000			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)	$V_{DD} \pm = \pm 1.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		125°C	1000			1000			
I_{IB} Input bias current		25°C	1	60		1	60	pA	
	125°C	1000			1000				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2	V	
		Full range	0 to 1.7		0 to 1.7				
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	2.98			2.98			V
	$I_{OH} = -75\ \mu\text{A}$	25°C	2.9			2.9			
	$I_{OH} = -150\ \mu\text{A}$	Full range	2.8			2.8			
		25°C	2.8			2.8			
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	10			10			mV
		25°C	100	150		100	150		
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	Full range	165			165			
		25°C	200	300		200	300		
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 1\text{ mA}$	Full range	300			300			
25°C		100	250		100	250			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to }2\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	250		100	250	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega$ ‡	25°C	800			800		
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²			Ω
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²			Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	220			220			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C	65	75		65	77	dB	
		Full range	60			60			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	100	dB	
		Full range	80			80			
I_{DD} Supply current	$V_O = 1.5\text{ V}$, No load	25°C	68	125		68	125	μA	
		Full range	150			150			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2252Q, and TLV2252M operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain $V_O = 0.8\text{ V to }1.4\text{ V}, R_L = 100\text{ k}\Omega\ddagger,$ $C_L = 100\text{ pF}\ddagger$	25°C	0.07	0.1		0.07	0.1		V/ μs	
		Full range	0.05			0.05				
V_n	Equivalent input noise voltage	f = 10 Hz	25°C			35			nV/ $\sqrt{\text{Hz}}$	
		f = 1 kHz	25°C			19				
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C			0.6			μV	
		f = 0.1 Hz to 10 Hz	25°C			1.1				
I_n	Equivalent input noise current	25°C				0.6			fA/ $\sqrt{\text{Hz}}$	
	Gain-bandwidth product	f = 1 kHz, $R_L = 50\text{ k}\Omega\ddagger,$ $C_L = 100\text{ pF}\ddagger$	25°C			0.187			MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V},$ $R_L = 50\text{ k}\Omega\ddagger,$	$A_V = 1,$ $C_L = 100\text{ pF}\ddagger$	25°C			60			kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega\ddagger,$	$C_L = 100\text{ pF}\ddagger$	25°C			63°			
	Gain margin			25°C			15			dB

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

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TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 2.5\text{ V}, V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850	μV	
		Full range		1750		1000			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		125°C		1000		1000			
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	125°C		1000		1000				
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}, R_S = 50\ \Omega$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -75\ \mu\text{A}$ $I_{OH} = -150\ \mu\text{A}$	25°C	4.98			4.98		V	
		25°C	4.9	4.94		4.9	4.94		
		Full range	4.8			4.8			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$ $V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$ $V_{IC} = 2.5\text{ V}, I_{OL} = 1\text{ mA}$	25°C	0.01			0.01		V	
		25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
		25°C	0.2	0.3		0.2	0.3		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	350		100	350	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega$ ‡	25°C	1700			1700		
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²		Ω	
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²		Ω	
$C_{i(c)}$ Common-mode input capacitance	f = 10 kHz, P package	25°C	8			8		pF	
z_o Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C	200			200		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70			70			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95	dB	
		Full range	80			80			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		70	125		70	125	μA
		Full range			150			150	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2252Q, and TLV2252M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.25\text{ V}$ to 2.75 V , $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.12		0.07	0.12		$\text{V}/\mu\text{s}$
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		36			36		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz}$ to 1 Hz	25°C		0.7			0.7		μV
	$f = 0.1\text{ Hz}$ to 10 Hz	25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6	$\text{fA}/\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$		0.2%			0.2%		
		$A_V = 10$		1%			1%		
Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡, 25°C		0.2			0.2	MHz	
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$, $C_L = 100\text{ pF}$ ‡, 25°C		30			30	kHz	
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		63°			63°		
Gain margin		25°C		15			15	dB	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

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TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage		25°C	200	1500		200	850	μV	
		Full range		1750		1000			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 1.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		125°C	1000			1000			
I_{IB} Input bias current		25°C	1	60		1	60	pA	
		125°C	1000			1000			
V_{ICR} Common-mode input voltage range		$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2	V
	Full range		0 to 1.7		0 to 1.7				
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	2.98			2.98			V
	$I_{OH} = -75\ \mu\text{A}$	25°C	2.9			2.9			
	Full range	2.8			2.8				
V_{OL} Low-level output voltage	$I_{OH} = -150\ \mu\text{A}$	25°C	2.8			2.8			
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	10			10			
		Full range	100	150		100	150		
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	165			165			
		Full range	200	300		200	300		
$V_{IC} = 1.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C	300			300				
	Full range	300			300				
AVD Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to }2\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	225		100	225	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega$ ‡	25°C	800			800		
$r_{i(d)}$ Differential input resistance		25°C	10^{12}			10^{12}			Ω
$r_{i(c)}$ Common-mode input resistance		25°C	10^{12}			10^{12}			Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	220			220			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C	65	75		65	77	dB	
		Full range	60			60			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	100	dB	
		Full range	80			80			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current (four amplifiers)	$V_O = 1.5\text{ V}$, No load	25°C		135	250		135	250	μA
		Full range			300			300	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2254Q, and TLV2254M operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V}$ to 1.7 V , $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.1		0.07	0.1		$\text{V}/\mu\text{s}$
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		35			35		$\text{nV}/\sqrt{\text{Hz}}$
		25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz}$ to 1 Hz $f = 0.1\text{ Hz}$ to 10 Hz	25°C		0.6			0.6		μV
		25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6	$\text{fA}/\sqrt{\text{Hz}}$	
Gain-bandwidth product	$f = 1\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		0.187			0.187	MHz	
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $A_V = 1$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		60			60	kHz	
ϕ_m Phase margin at unity gain Gain margin	$R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		63°			63°		
		25°C		15			15	dB	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

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TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}, V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850	μV	
		Full range			1750		1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		125°C			1000		1000		
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	125°C			1000		1000			
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}, R_S = 50\ \Omega$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98		4.98		V		
		25°C	4.9	4.94	4.9	4.94			
		Full range	4.8		4.8				
		25°C	4.8	4.88	4.8	4.88			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C	0.01		0.01		V		
		25°C	0.09	0.15	0.09	0.15			
	Full range	0.15		0.15					
		25°C	0.2	0.3	0.2	0.3			
	Full range	0.3		0.3					
		25°C	100	350	100	350			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	10		10		V/mV		
		Full range	10		10				
		$R_L = 1\text{ M}\Omega$ ‡	1700		1700				
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²		10 ¹²		Ω		
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²		10 ¹²		Ω		
$c_{i(c)}$ Common-mode input capacitance	f = 10 kHz, N package	25°C	8		8		pF		
z_o Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C	200		200		Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C	70	83	70	83	dB		
		Full range	70		70				
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95	80	95	dB		
		Full range	80		80				

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C	140	250	140	250	μA	
			Full range	300			300		

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2254Q, and TLV2254M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain $V_O = 0.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.12		0.07	0.12	$\text{V}/\mu\text{s}$		
		Full range	0.05			0.05				
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	36			36			$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 1\text{ kHz}$	19			19				
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	0.7			0.7			μV	
		$f = 0.1\text{ Hz to }10\text{ Hz}$	1.1			1.1				
I_n	Equivalent input noise current	25°C	0.6			0.6			$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$	0.2%			0.2%				
		$A_V = 10$	1%			1%				
	Gain-bandwidth product $f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡, 25°C	0.2			0.2			MHz	
BOM	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C	30			30			kHz
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega$ ‡	$C_L = 100\text{ pF}$ ‡	25°C	63°			63°			
			Gain margin	25°C	15			15		

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

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TYPICAL CHARACTERISTICS

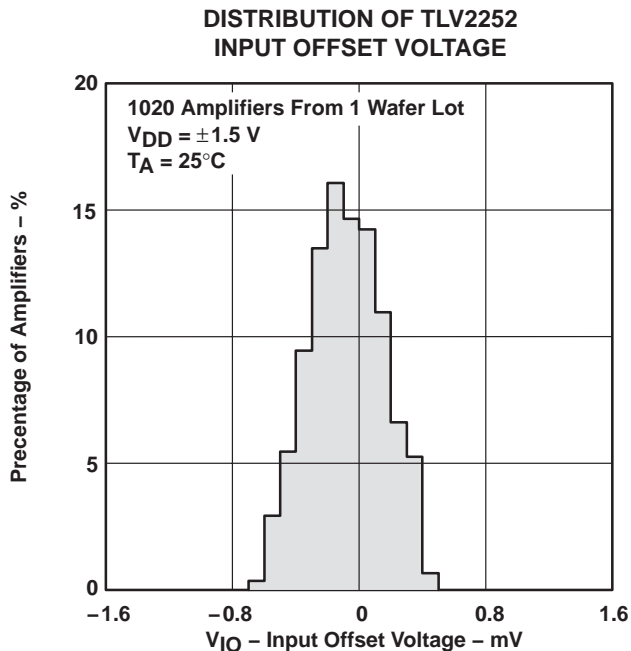


Figure 2

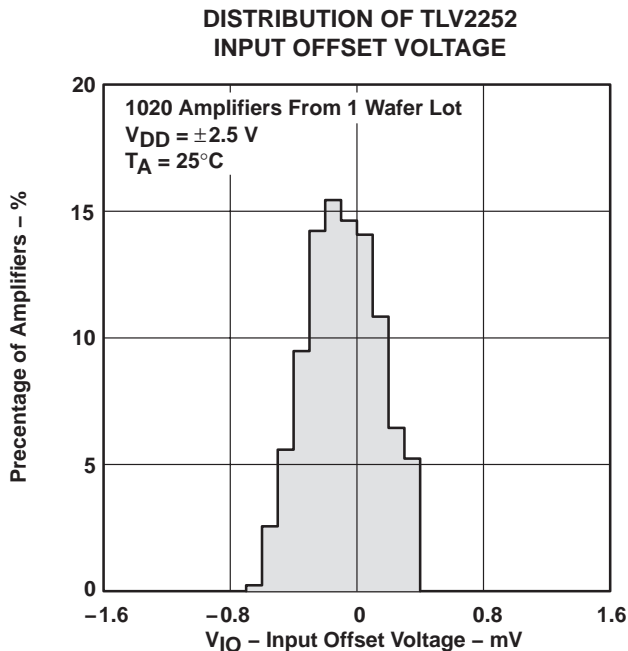


Figure 3

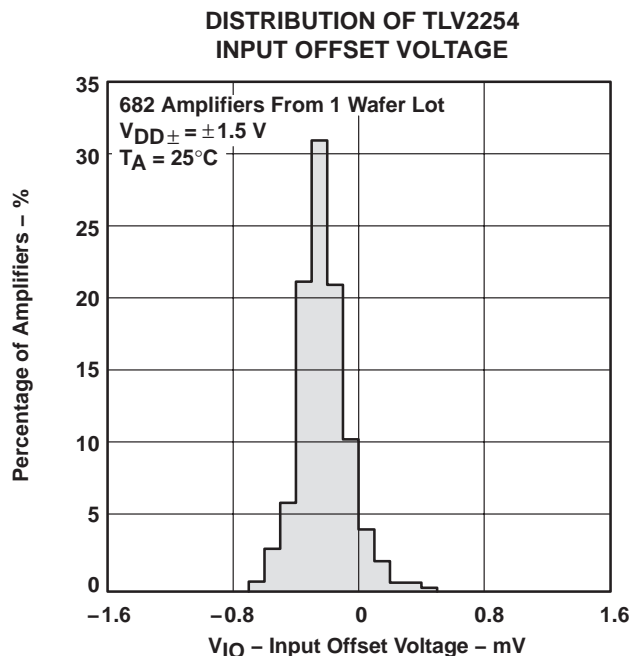


Figure 4

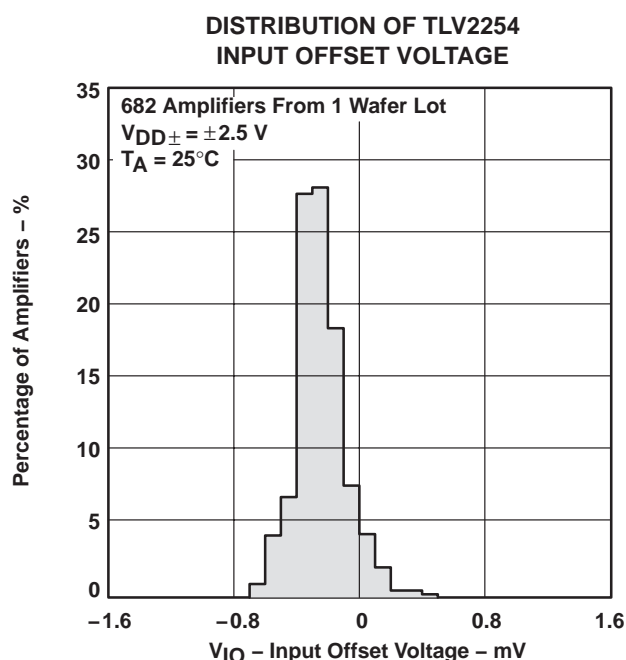


Figure 5

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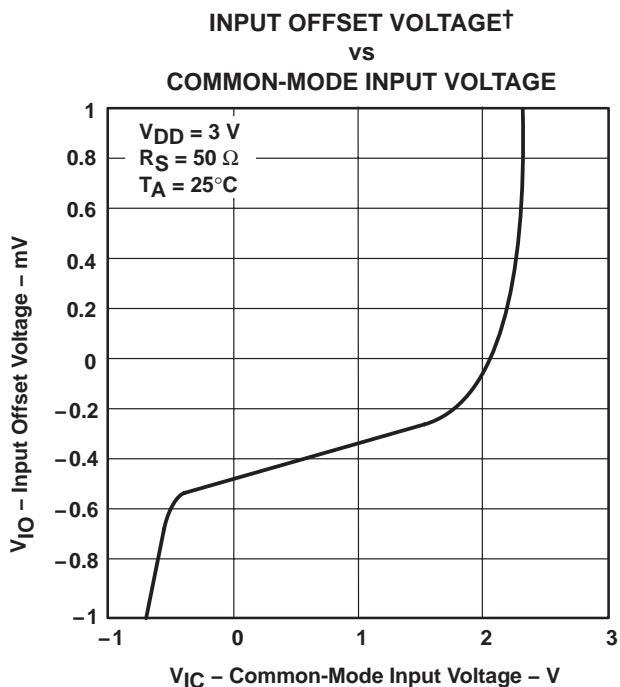


Figure 6

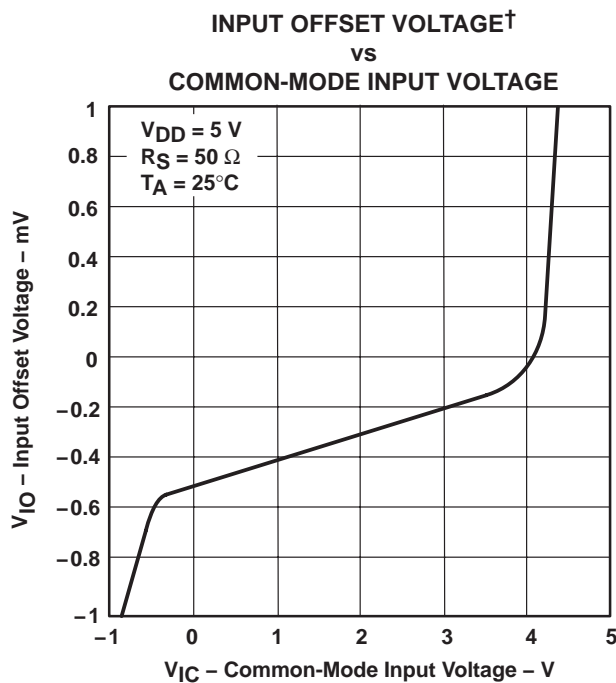


Figure 7

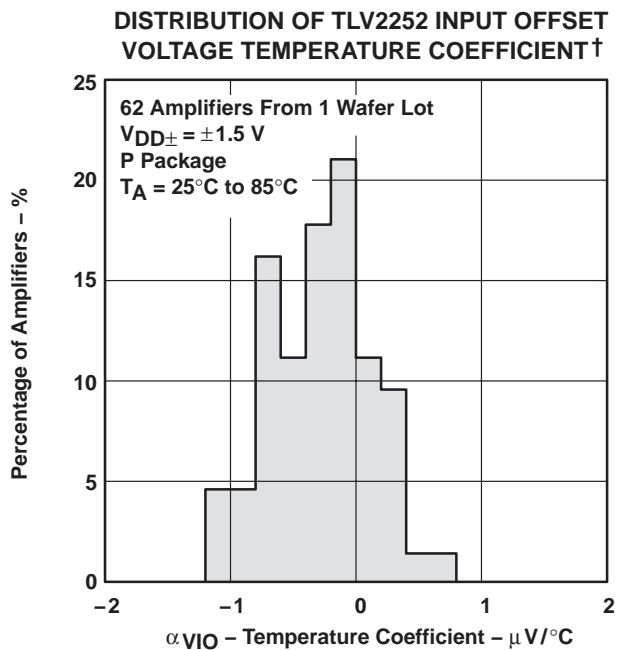


Figure 8

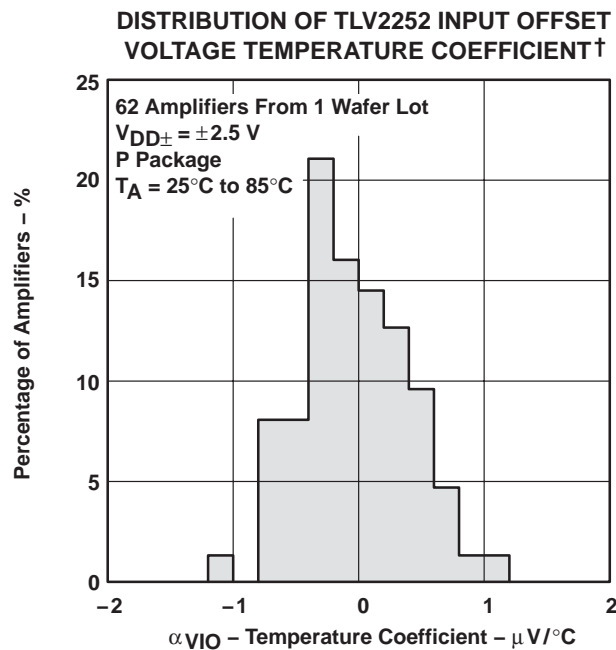


Figure 9

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.



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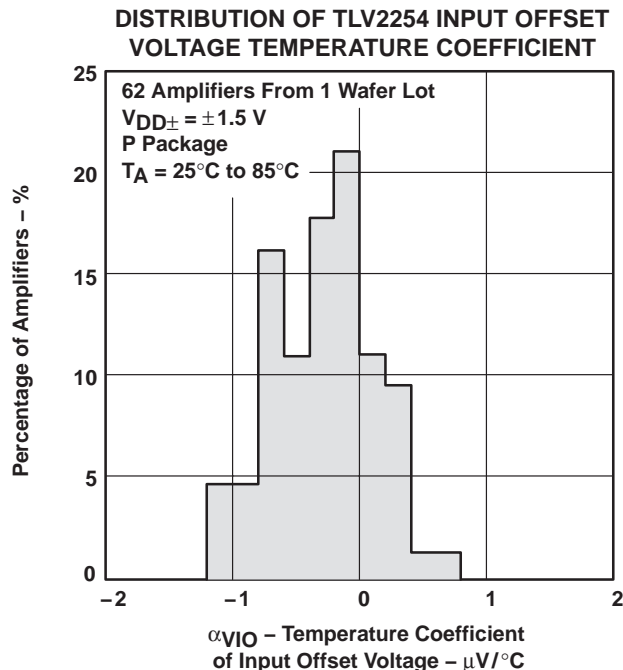


Figure 10

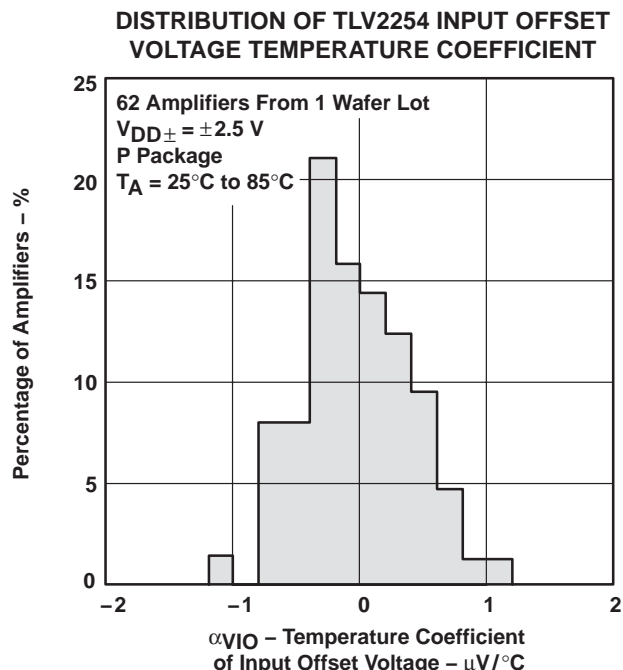


Figure 11

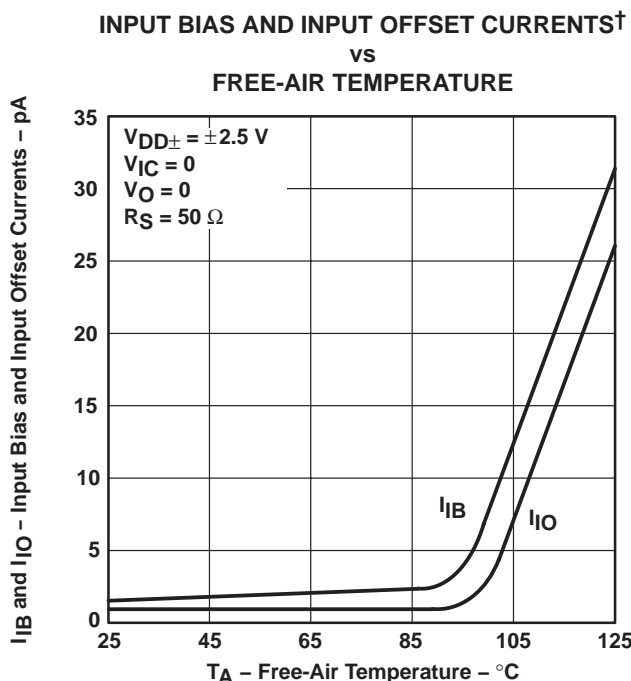


Figure 12

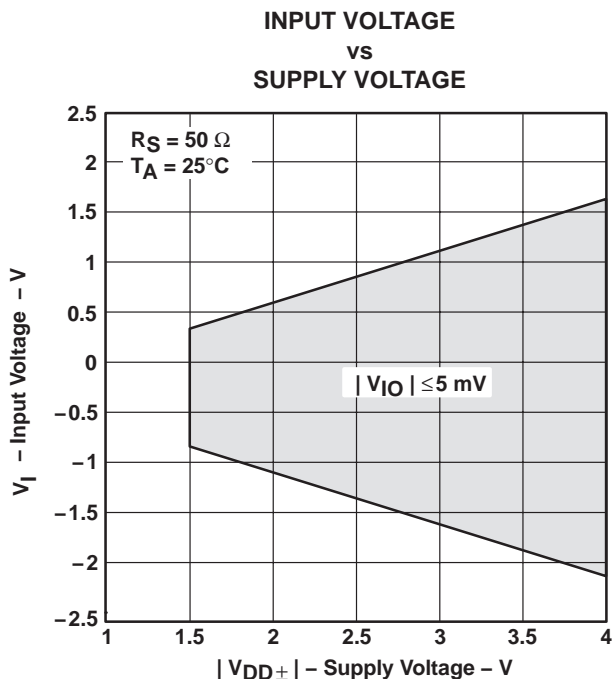


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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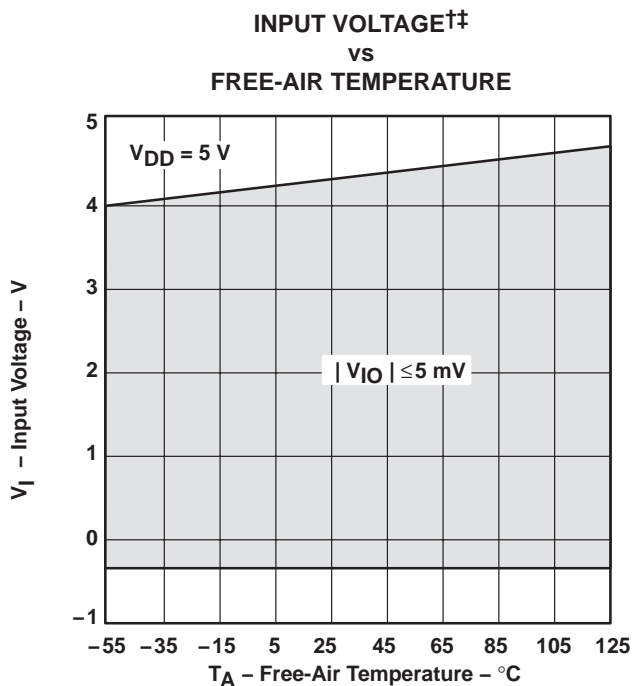


Figure 14

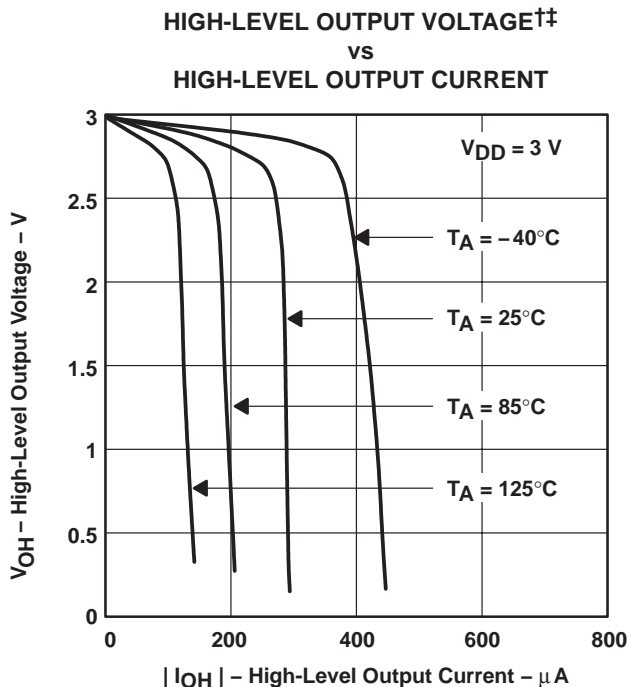


Figure 15

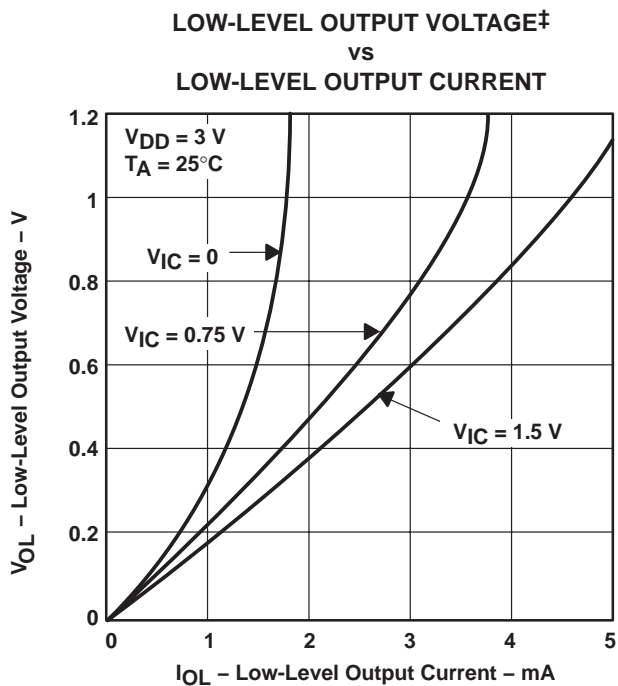


Figure 16

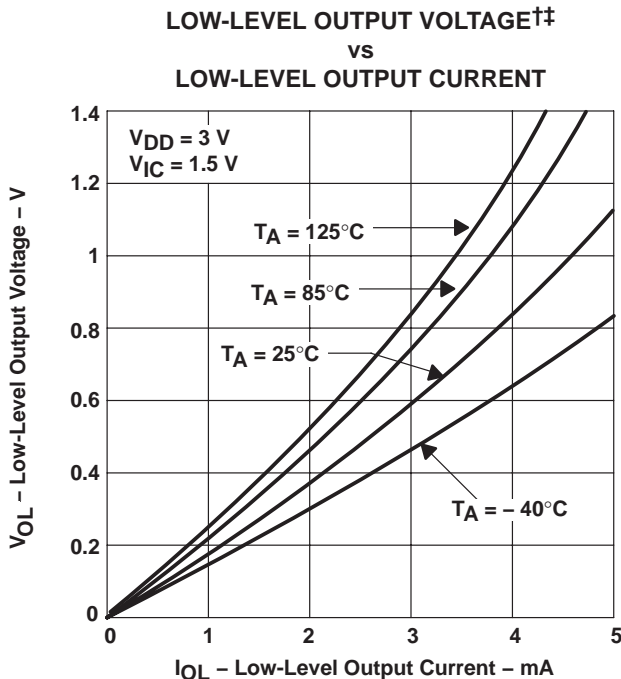


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

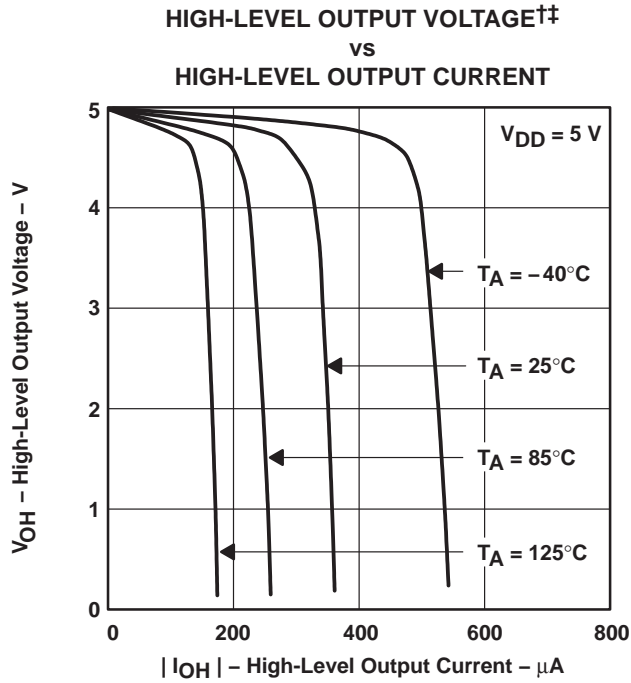


Figure 18

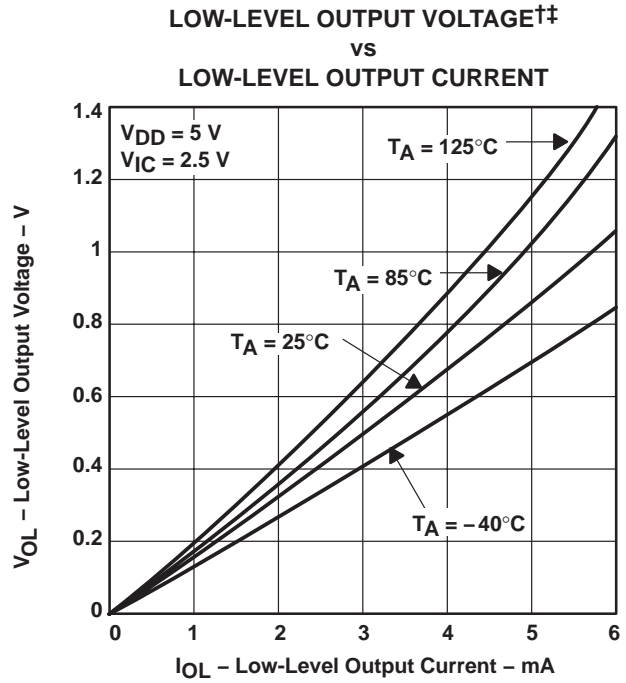


Figure 19

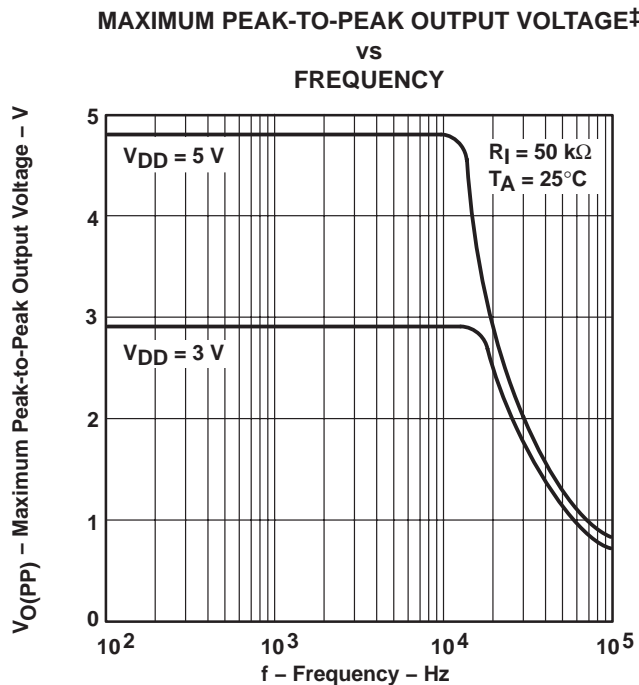


Figure 20

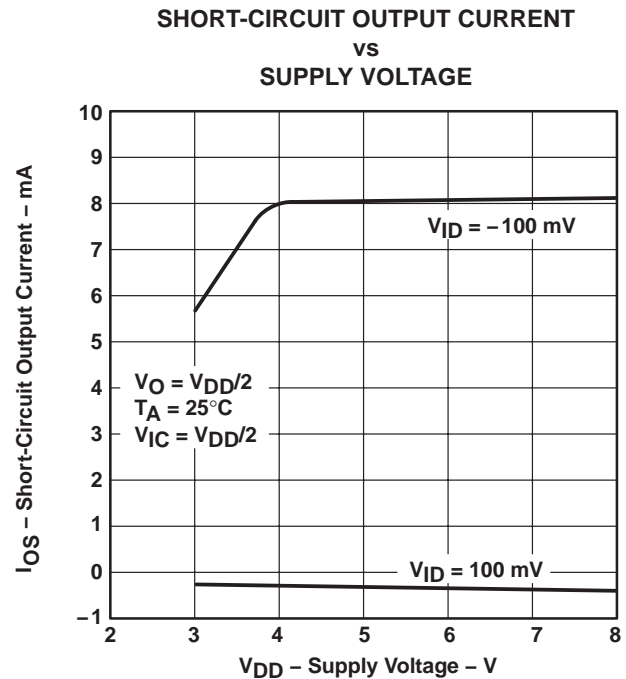


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TLV225x, TLV225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

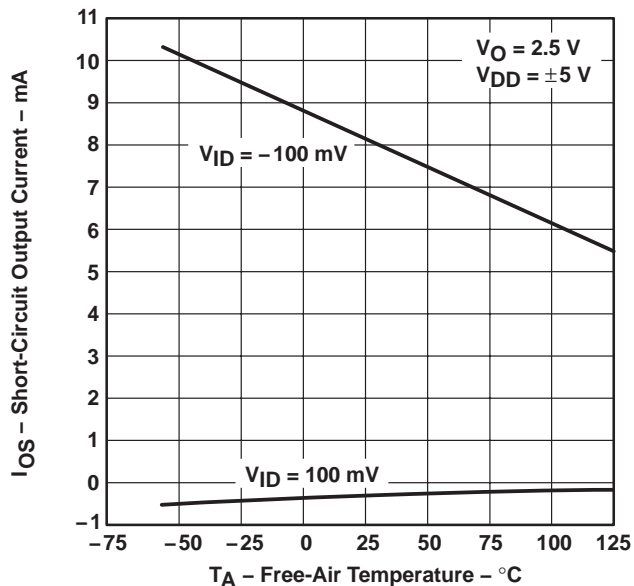


Figure 22

DIFFERENTIAL INPUT VOLTAGE‡
vs
OUTPUT VOLTAGE

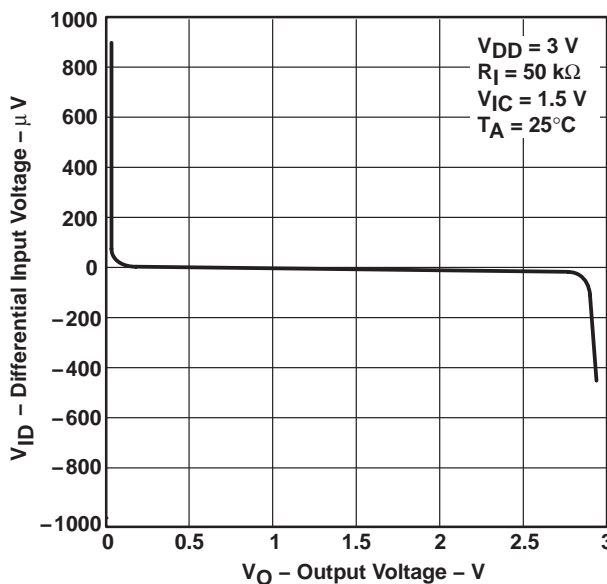


Figure 23

DIFFERENTIAL INPUT VOLTAGE‡
vs
OUTPUT VOLTAGE

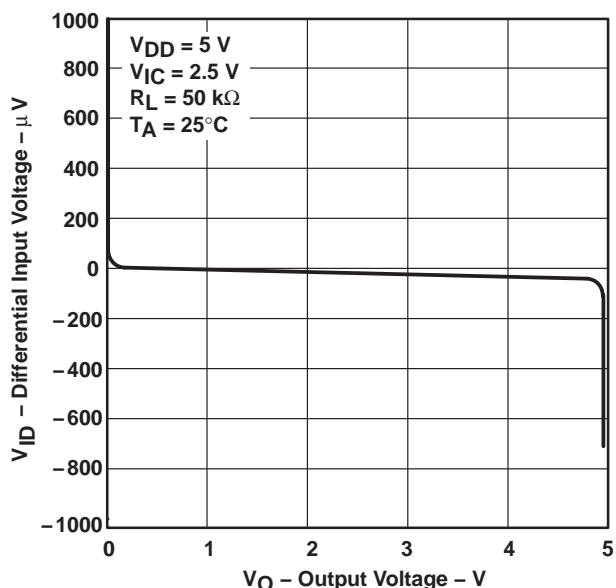


Figure 24

DIFFERENTIAL VOLTAGE AMPLIFICATION†‡
vs
LOAD RESISTANCE

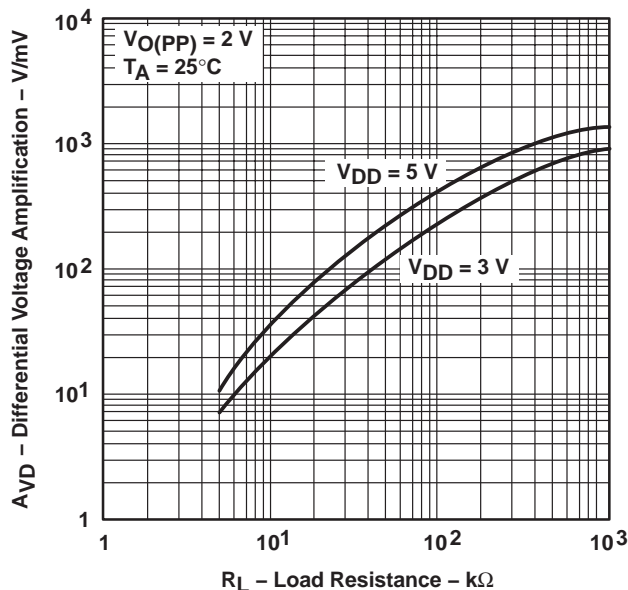


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE†
 AMPLIFICATION AND PHASE MARGIN
 vs
 FREQUENCY**

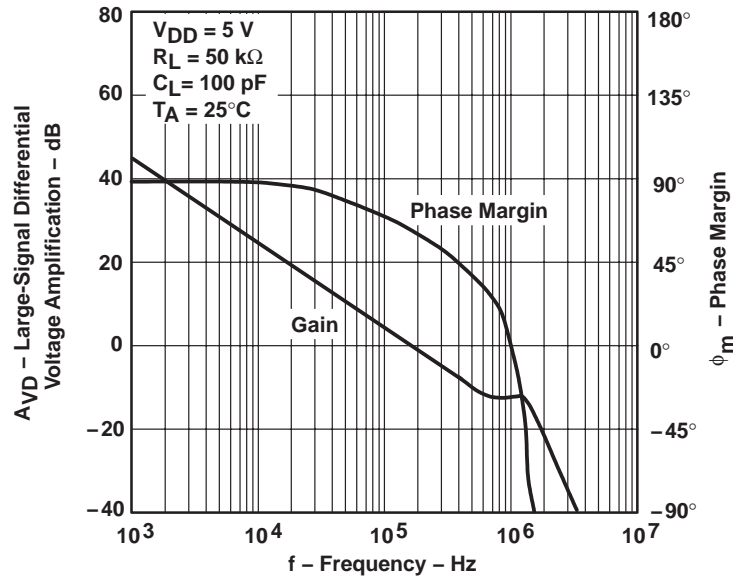


Figure 26

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE†
 AMPLIFICATION AND PHASE MARGIN
 vs
 FREQUENCY**

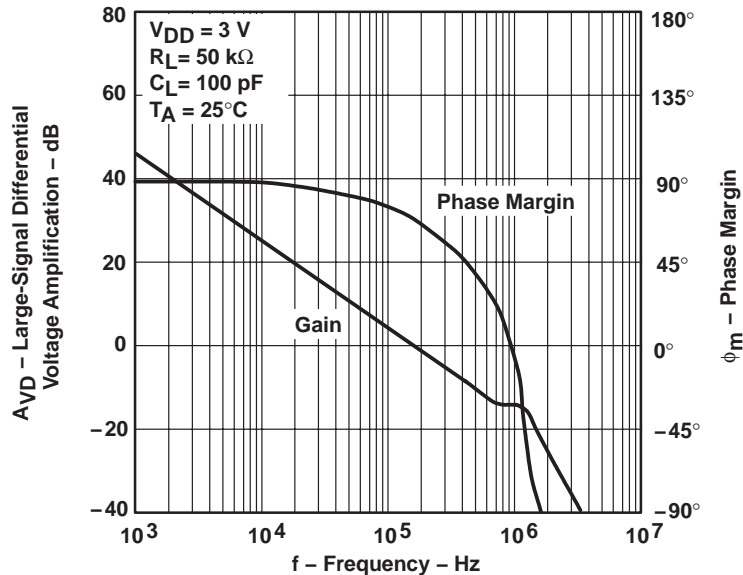


Figure 27

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL††
 VOLTAGE AMPLIFICATION**
 vs
FREE-AIR TEMPERATURE

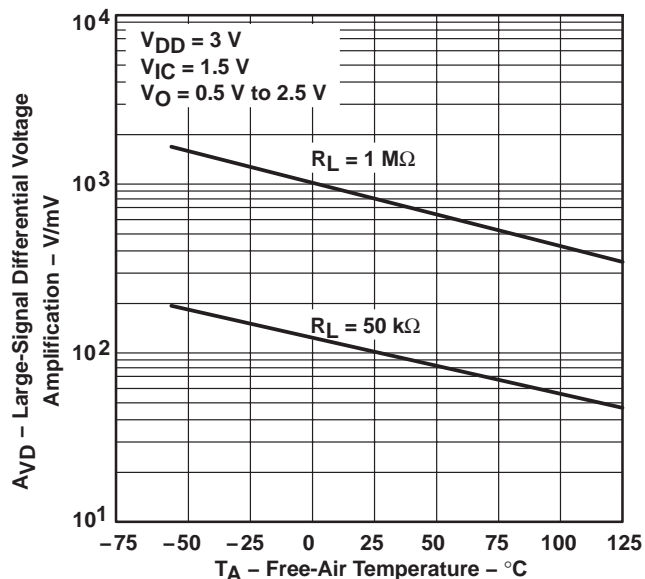


Figure 28

**LARGE-SIGNAL DIFFERENTIAL††
 VOLTAGE AMPLIFICATION**
 vs
FREE-AIR TEMPERATURE

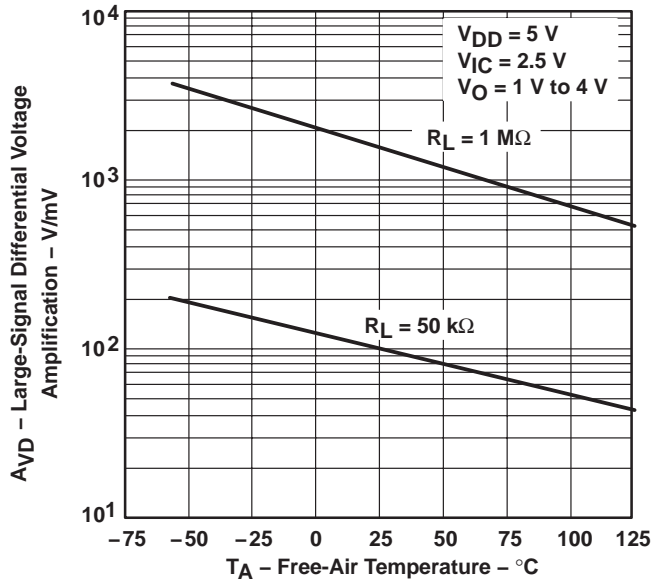


Figure 29

**OUTPUT IMPEDANCE†
 vs
 FREQUENCY**

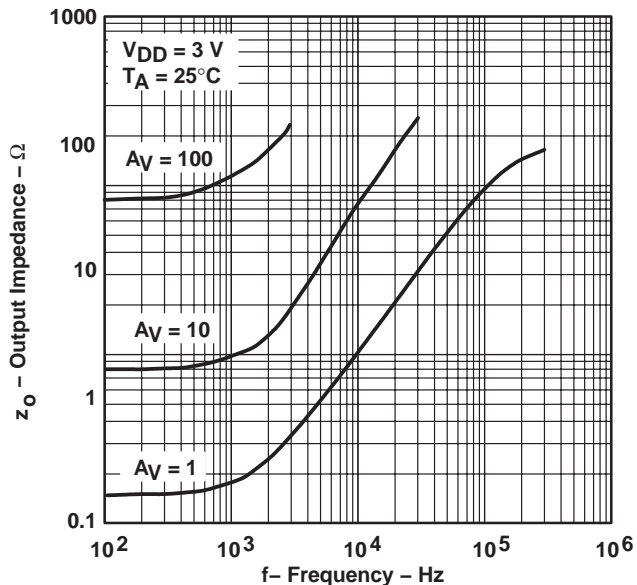


Figure 30

**OUTPUT IMPEDANCE†
 vs
 FREQUENCY**

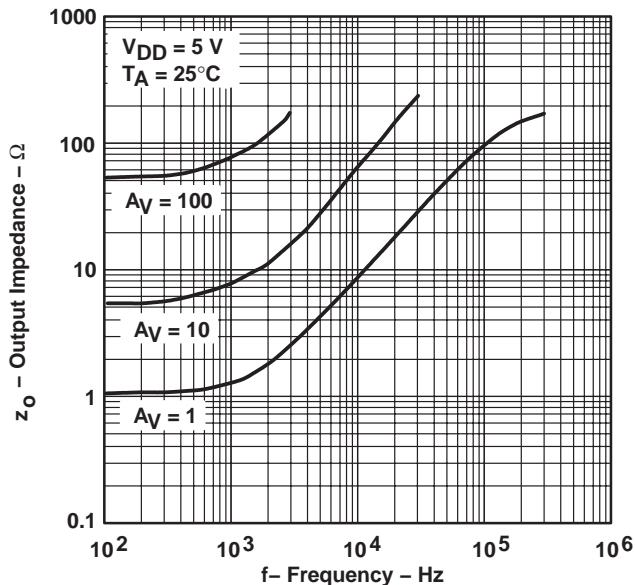


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.



TYPICAL CHARACTERISTICS

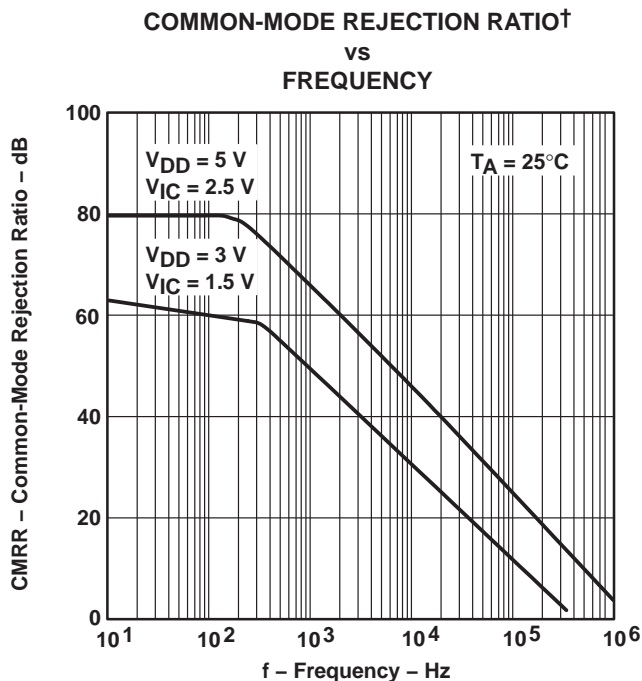


Figure 32

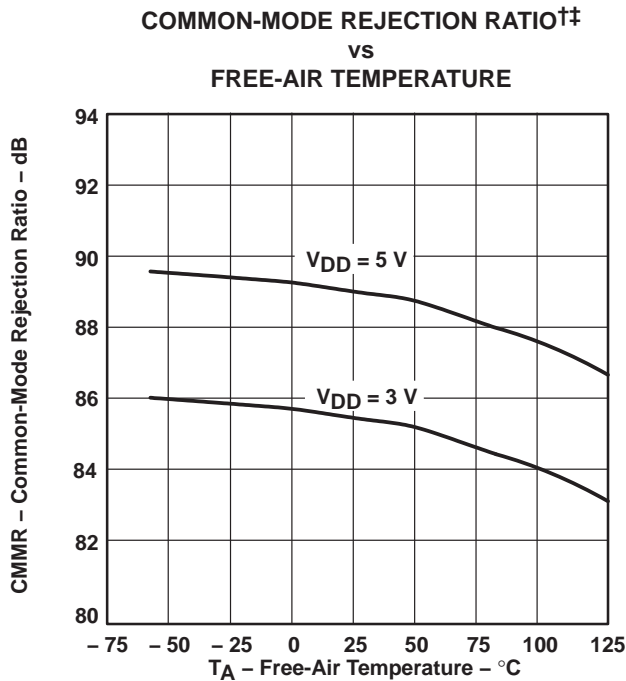


Figure 33

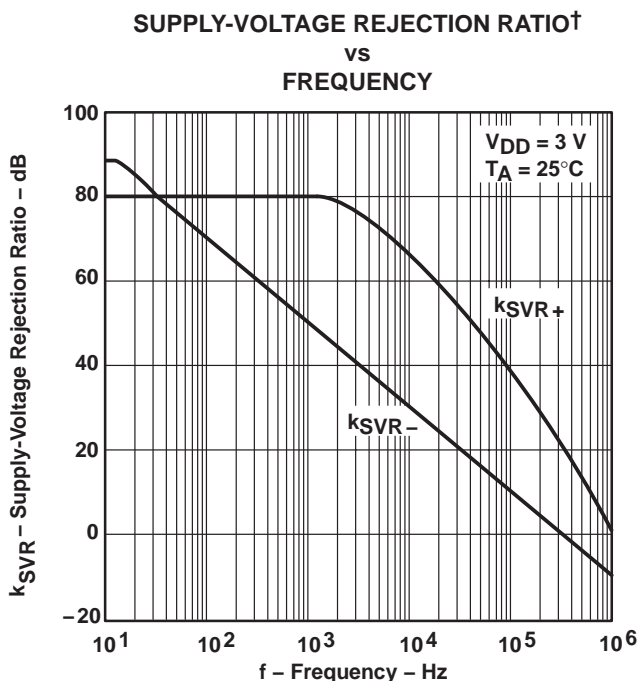


Figure 34

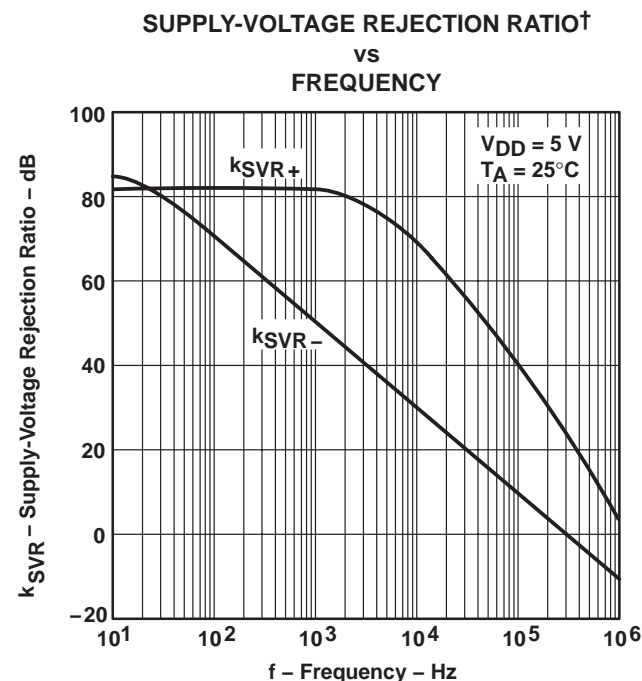


Figure 35

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.
 †† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

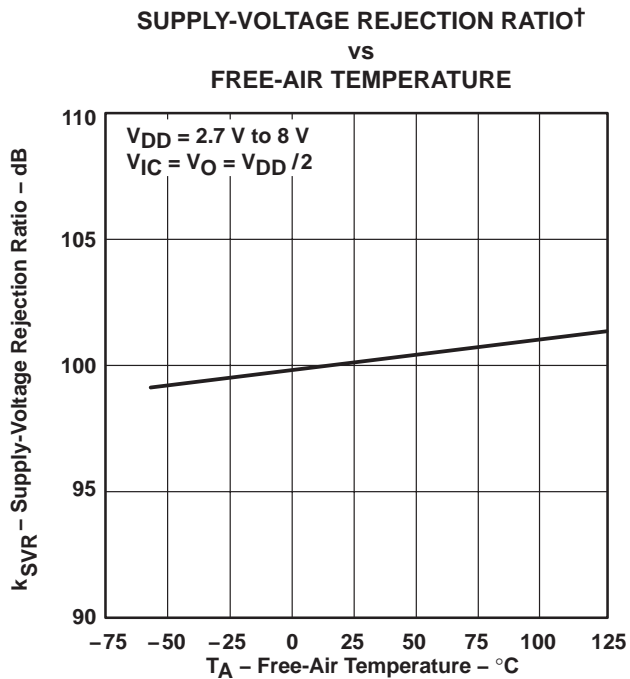


Figure 36

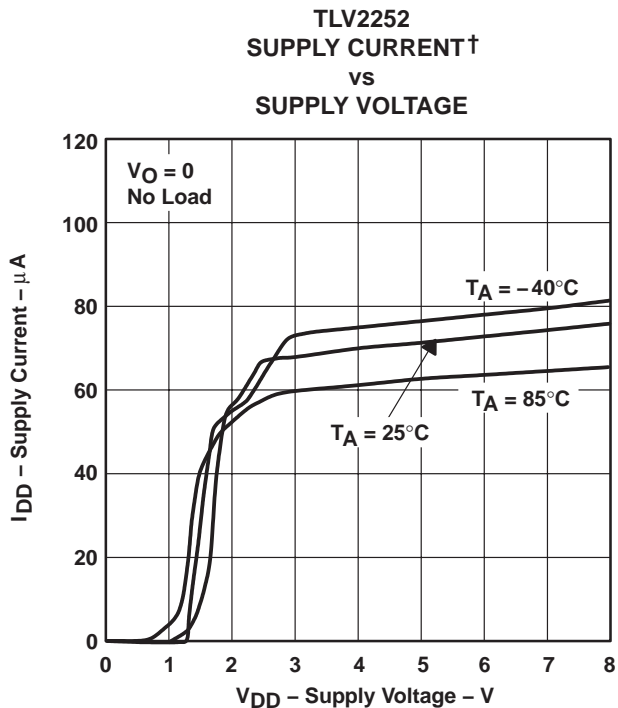


Figure 37

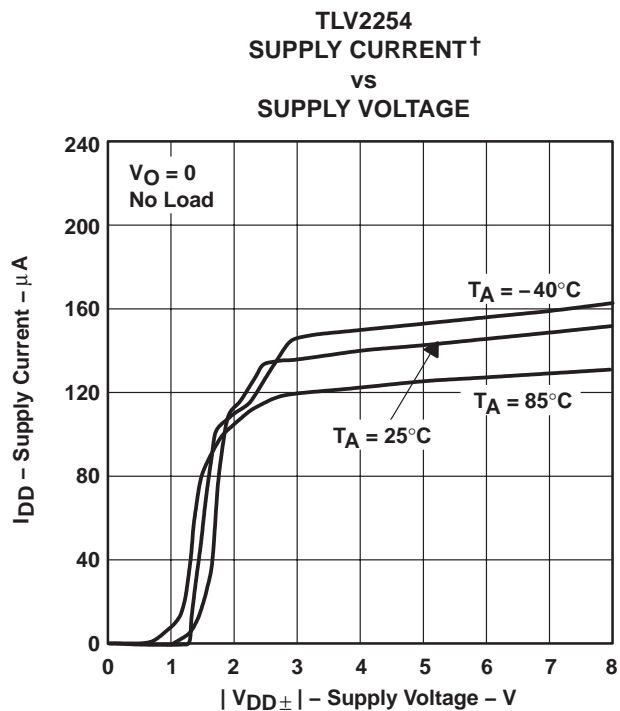


Figure 38

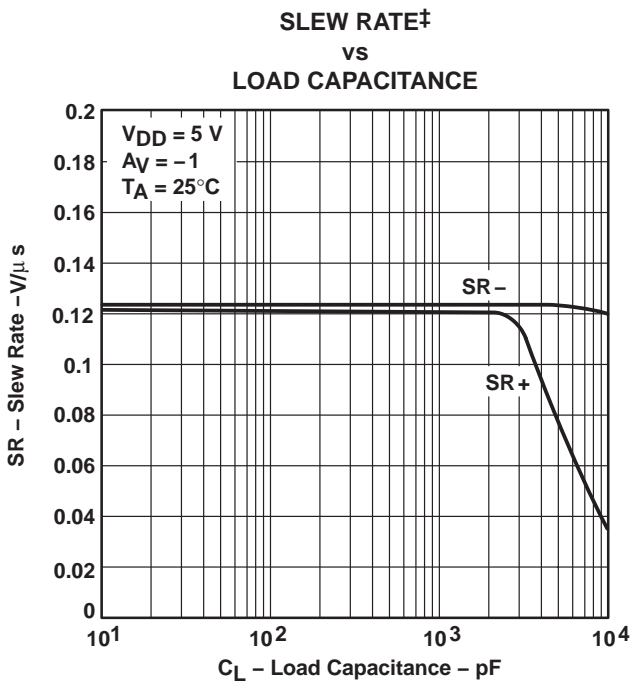
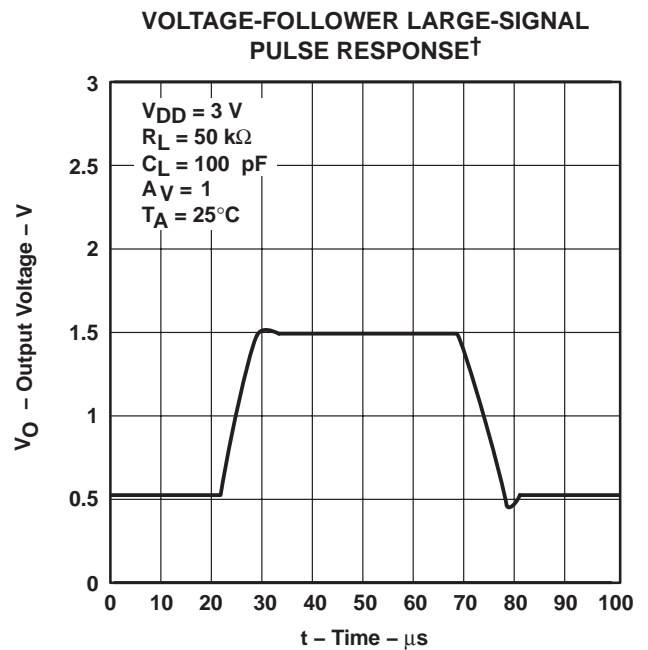
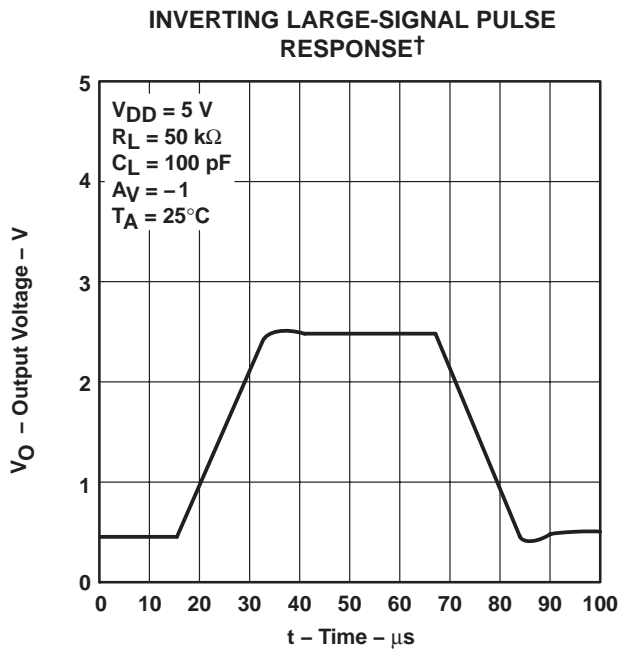
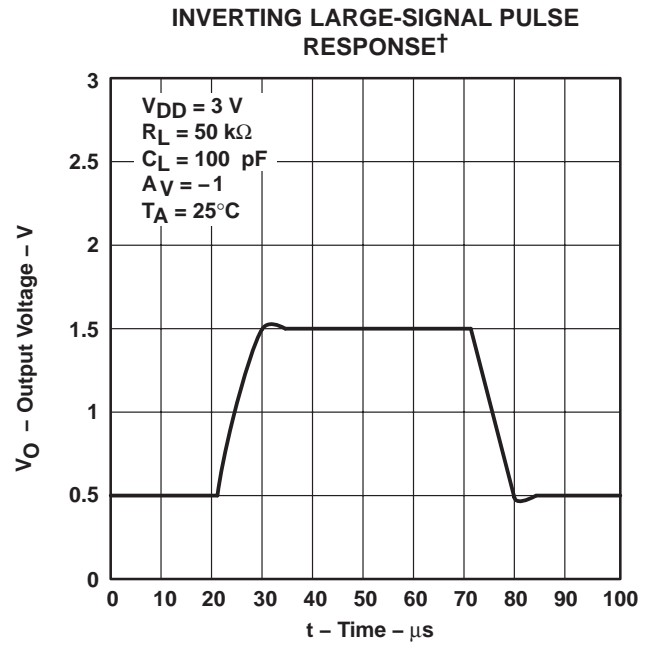
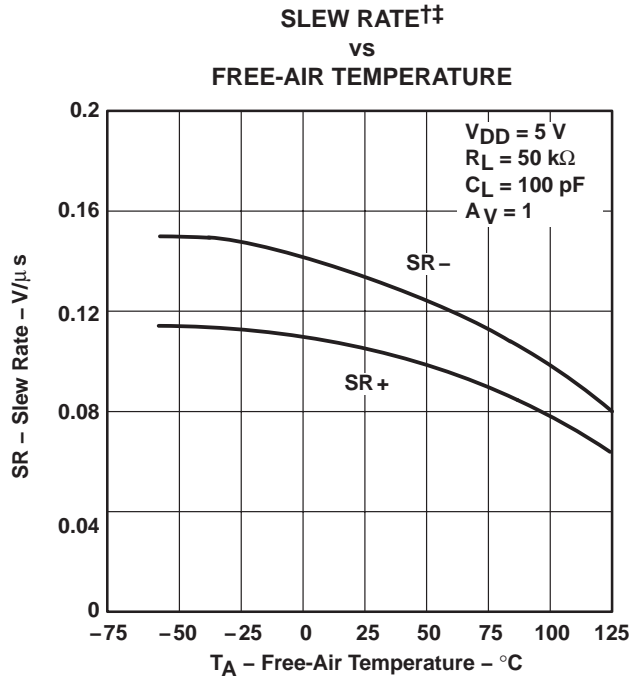


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

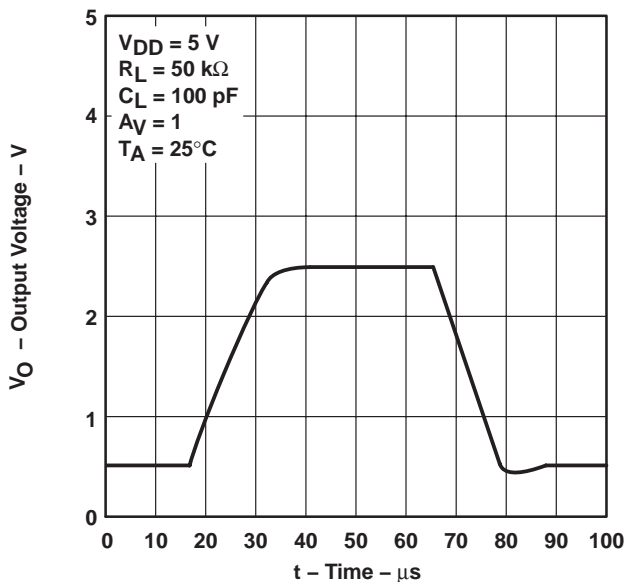


Figure 44

INVERTING SMALL-SIGNAL PULSE RESPONSE†

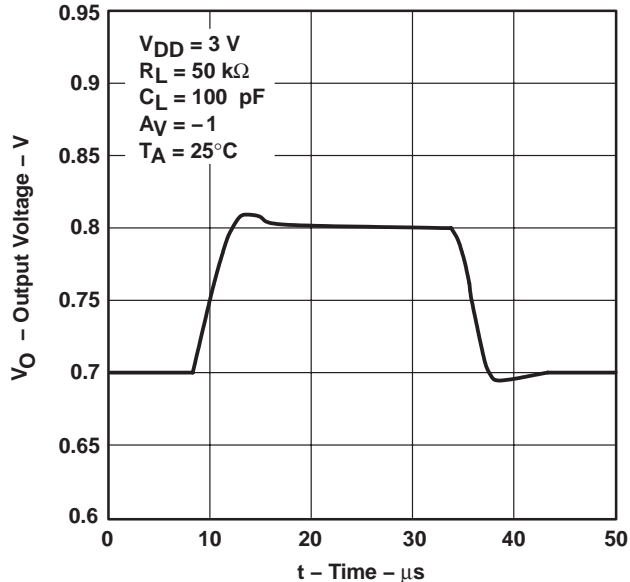


Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE†

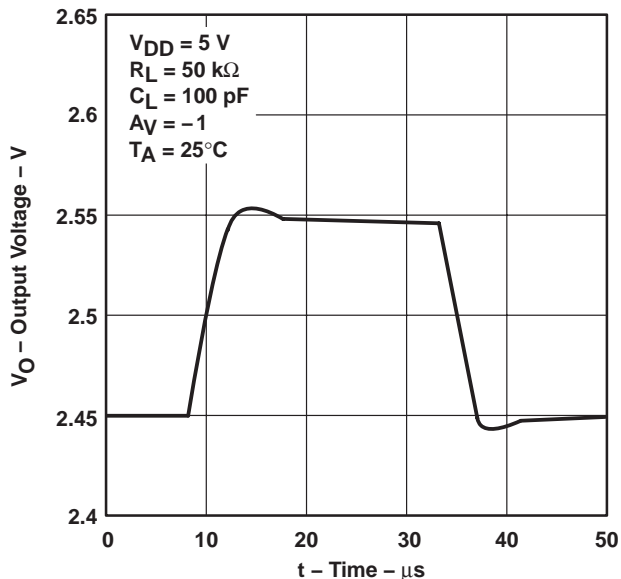


Figure 46

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

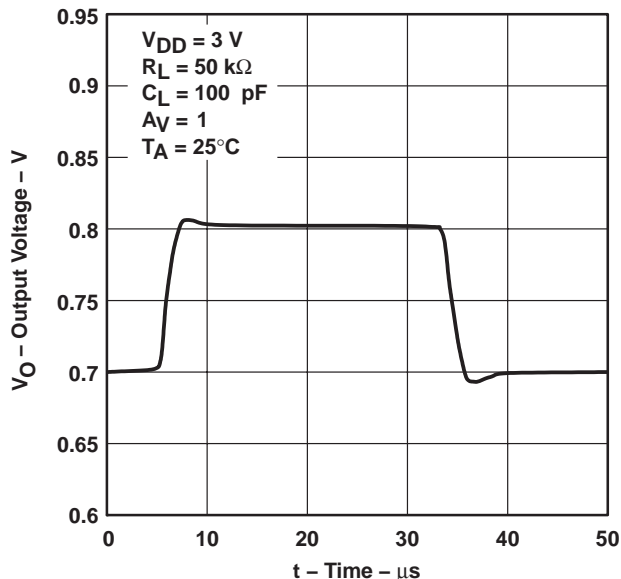


Figure 47

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

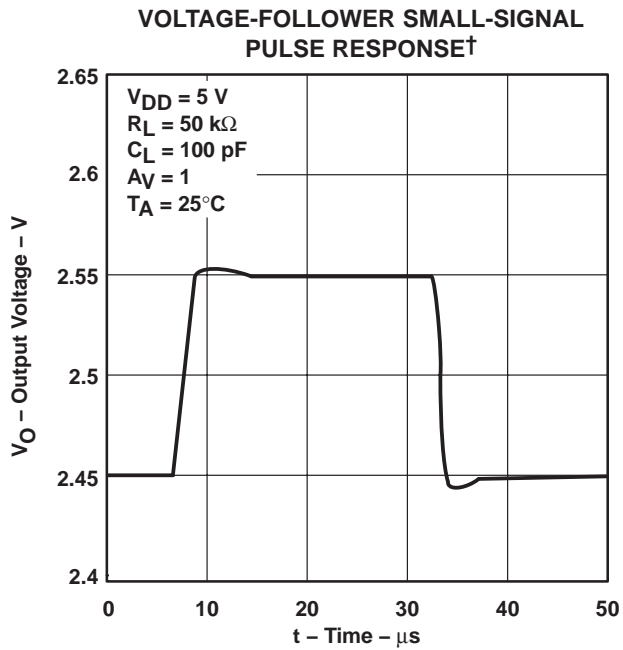


Figure 48

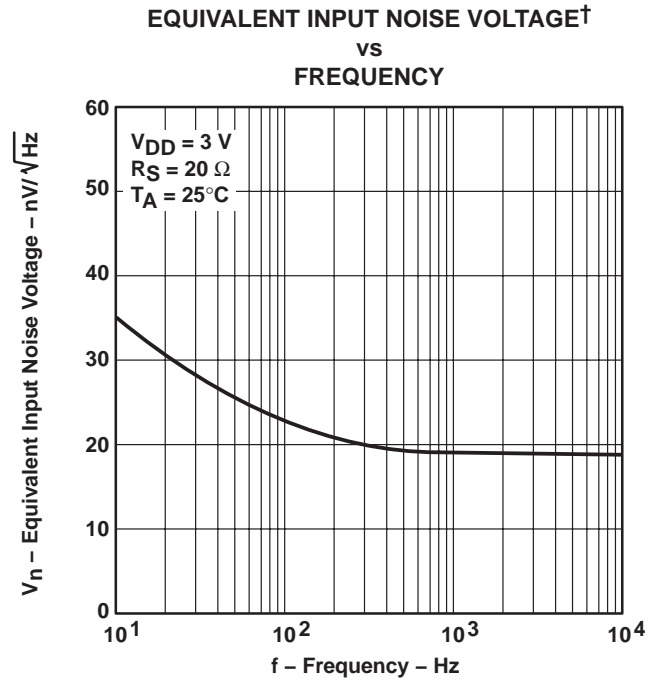


Figure 49

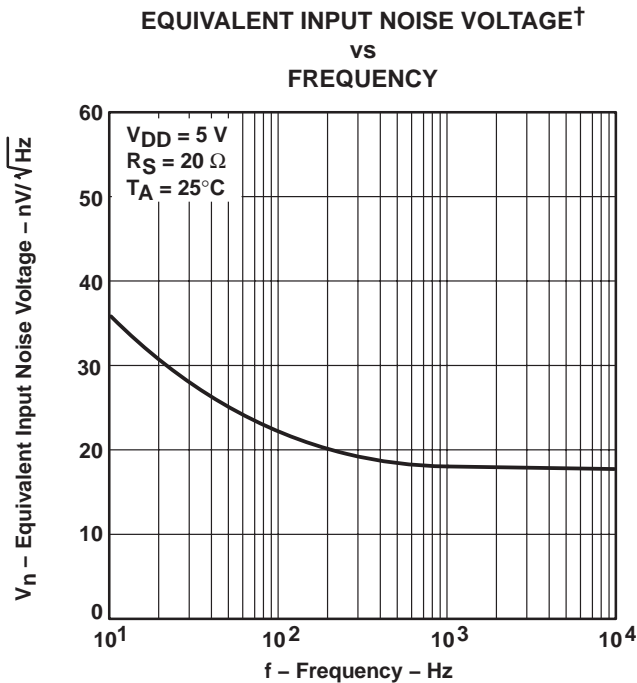


Figure 50

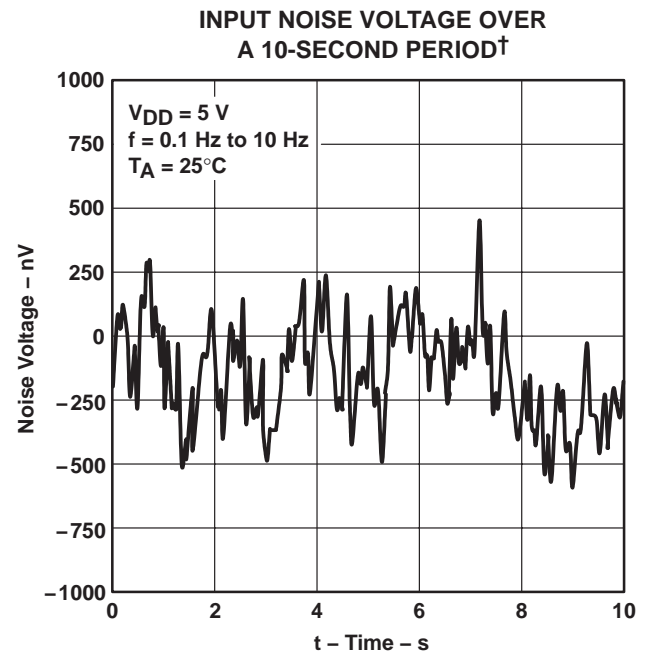


Figure 51

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INTEGRATED NOISE VOLTAGE†
vs
FREQUENCY

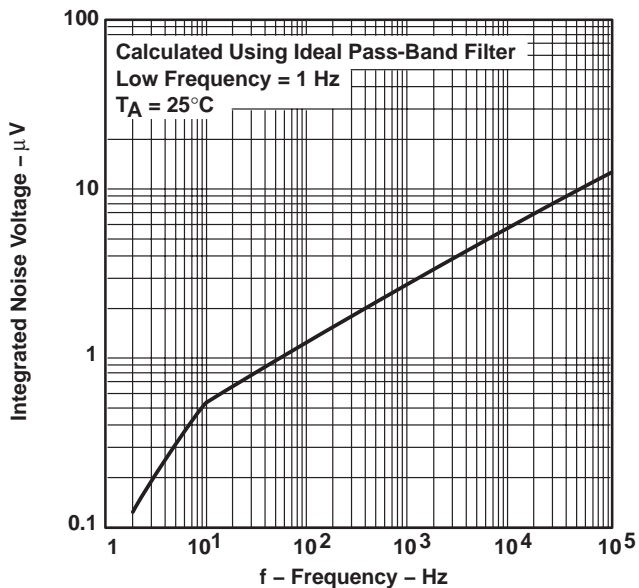


Figure 52

TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY

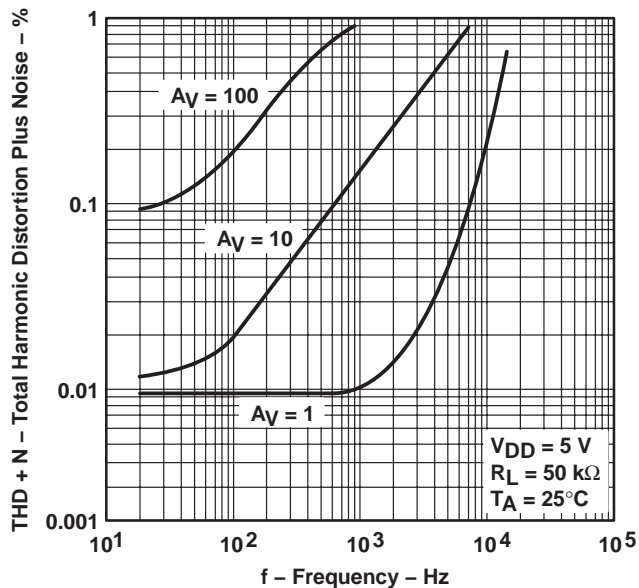


Figure 53

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

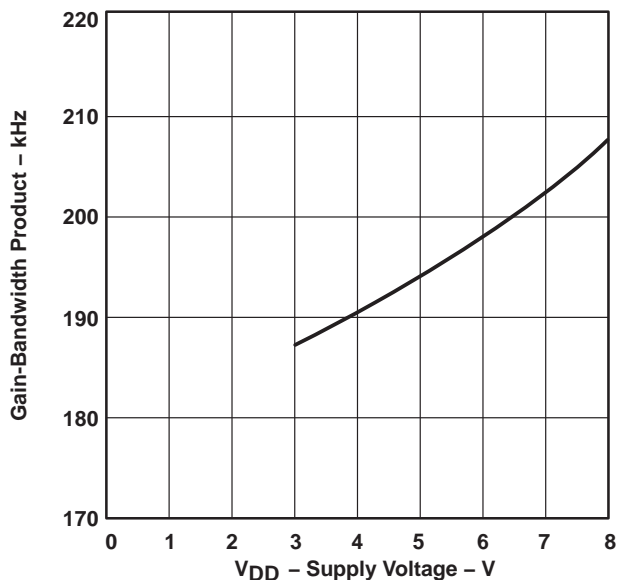


Figure 54

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

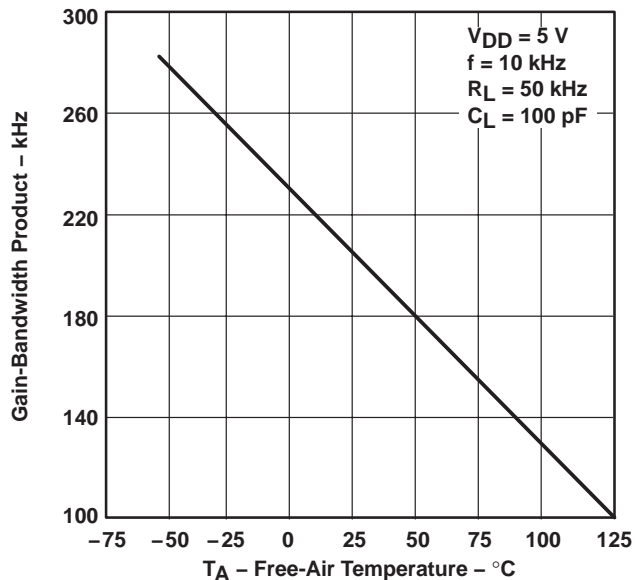


Figure 55

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

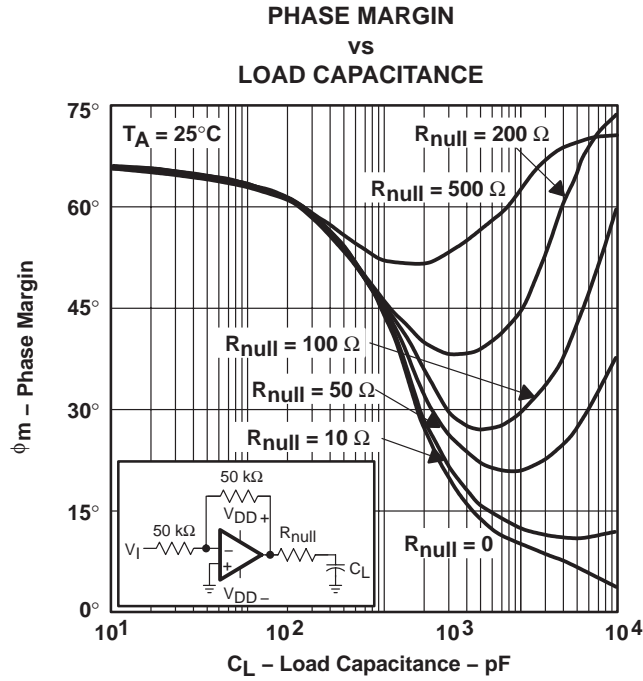


Figure 56

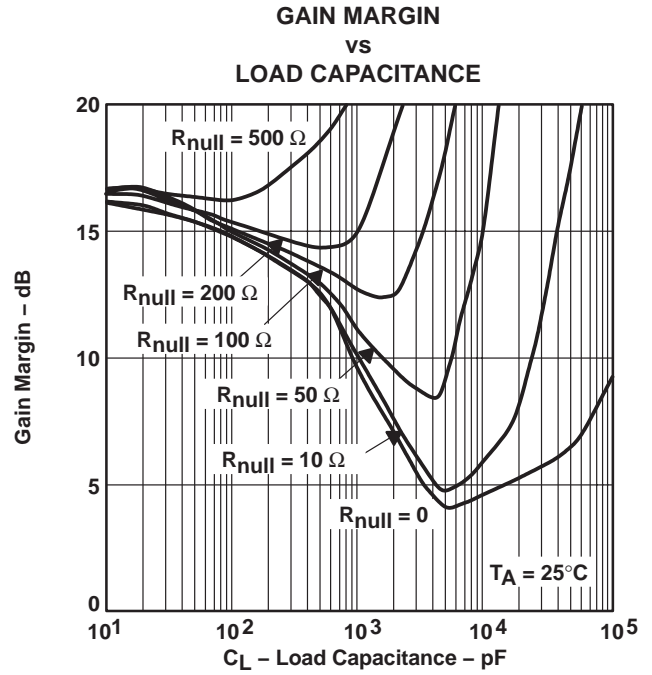


Figure 57

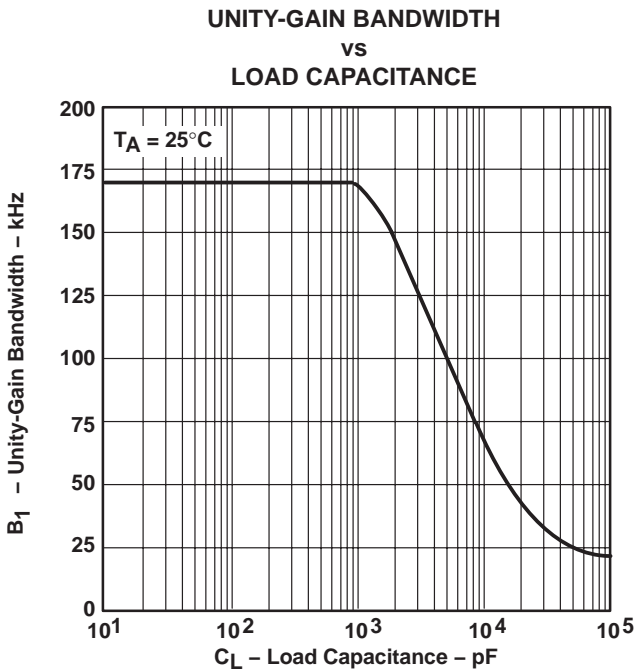
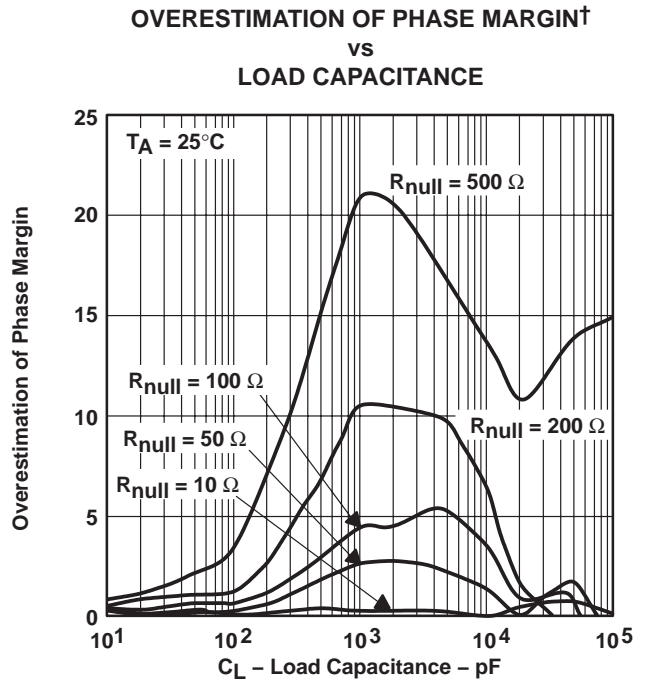


Figure 58



† See application information

Figure 59

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.
 ‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

driving large capacitive loads

The TLV2252 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 55 and Figure 56 show the effects of adding series resistances of 10 Ω , 50 Ω , 100 Ω , 200 Ω , and 500 Ω . The addition of this series resistor has two effects: the first adds a zero to the transfer function and the second reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \tag{1}$$

Where :

- $\Delta\phi_{m1}$ = improvement in phase margin
- UGBW = unity-gain bandwidth frequency
- R_{null} = output series resistance
- C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

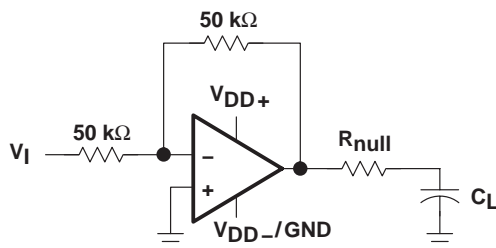


Figure 60. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts™*, the model generation software used with Microsim *PSpice™*. The Boyle macromodel (see Note 5) and subcircuit in Figure 61 are generated using the TLV2252 typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

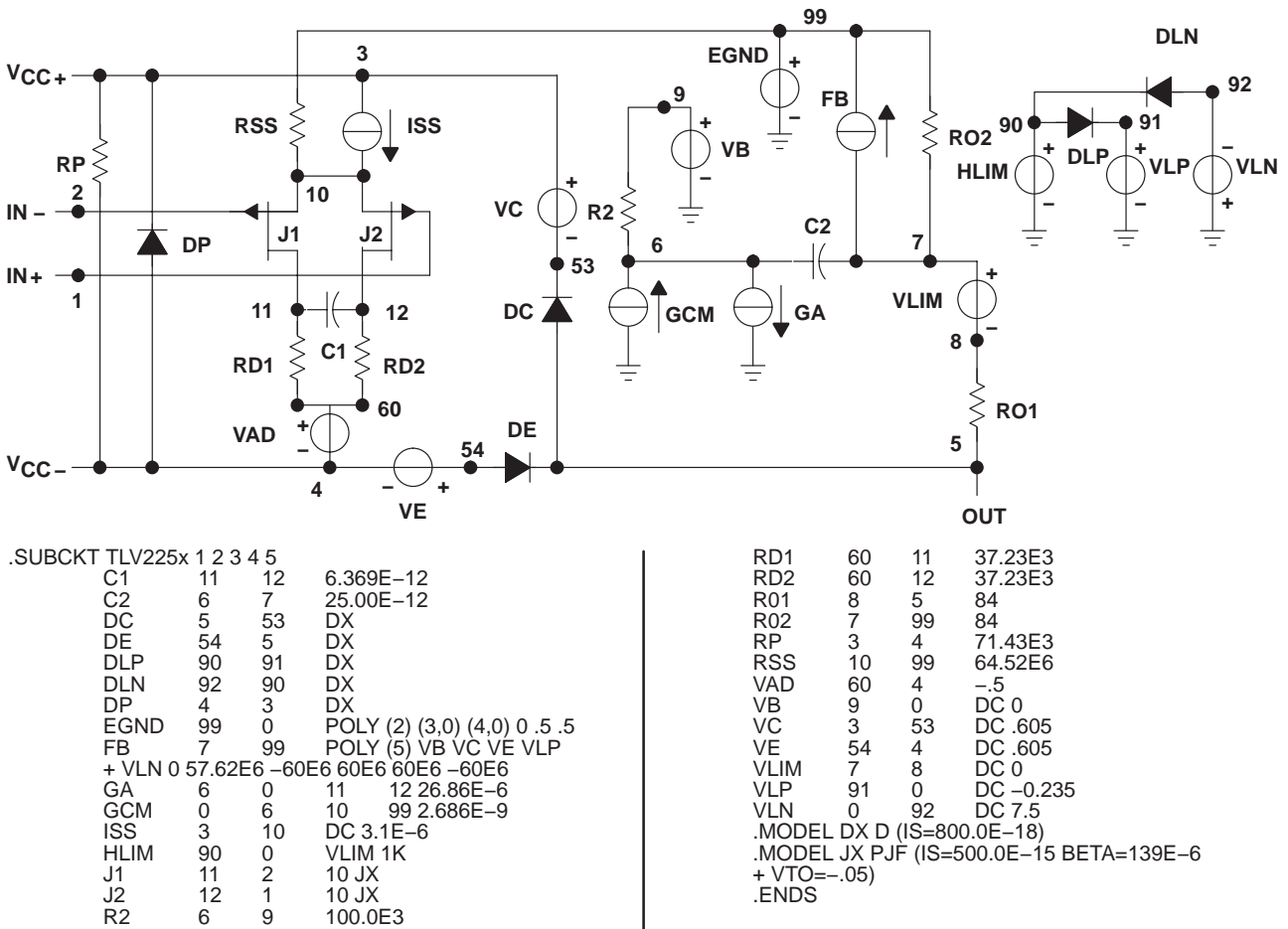


Figure 61. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9550401QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9550401QPA TLV2262M	Samples
5962-9550403QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9550403QHA TLV2262AM	Samples
5962-9550403QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9550403QPA TLV2262AM	Samples
5962-9566601QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9566601QPA TLV2252M	Samples
5962-9566603QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9566603QPA TLV2252AM	Samples
TLV2252AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252A	Samples
TLV2252AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252A	Samples
TLV2252AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252A	Samples
TLV2252AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252A	Samples
TLV2252AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2252AI	Samples
TLV2252AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY252A	Samples
TLV2252AIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY252A	Samples
TLV2252AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY252A	Samples
TLV2252AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9566603QPA TLV2252AM	Samples
TLV2252AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		V2252A	Samples
TLV2252ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252I	Samples
TLV2252IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2252IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252I	Samples
TLV2252IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2252IP	Samples
TLV2252MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9566601QPA TLV2252M	Samples
TLV2254AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2254AI	Samples
TLV2254AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2254AI	Samples
TLV2254AIN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2254AIN	Samples
TLV2254AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2254A	Samples
TLV2254AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2254A	Samples
TLV2254AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2254A	Samples
TLV2254AQD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254A	Samples
TLV2254ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254I	Samples
TLV2254IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254I	Samples
TLV2254IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254I	Samples
TLV2254IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV2254IN	Samples
TLV2262AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9550403QPA TLV2262AM	Samples
TLV2262AMUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9550403QHA TLV2262AM	Samples
TLV2262MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9550401QPA TLV2262M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV2252, TLV2252A, TLV2252AM, TLV2252M, TLV2254A, TLV2262AM, TLV2262M :

- Catalog: [TLV2252A](#), [TLV2252](#), [TLV2262A](#), [TLV2262](#)
- Automotive: [TLV2252-Q1](#), [TLV2252A-Q1](#), [TLV2252A-Q1](#), [TLV2252-Q1](#), [TLV2254A-Q1](#), [TLV2262A-Q1](#)
- Enhanced Product: [TLV2252A-EP](#), [TLV2252A-EP](#), [TLV2254A-EP](#)
- Military: [TLV2252M](#), [TLV2252AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2252AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2252AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2252IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2254AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2254AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2254IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2252AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2252AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLV2252IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2254AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2254AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2254IDR	SOIC	D	14	2500	350.0	350.0	43.0

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK

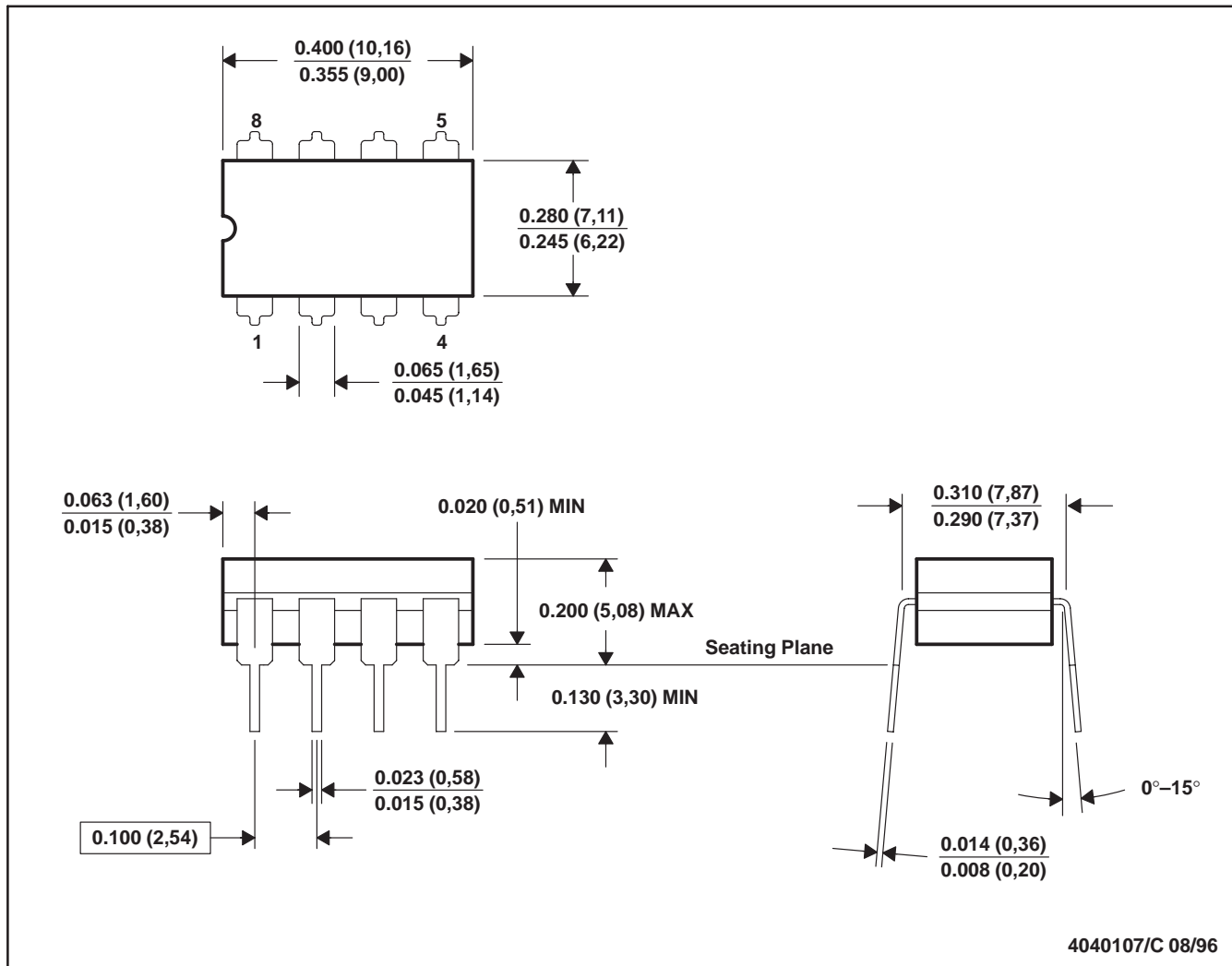


4040179/B 03/95

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

JG (R-GDIP-T8)

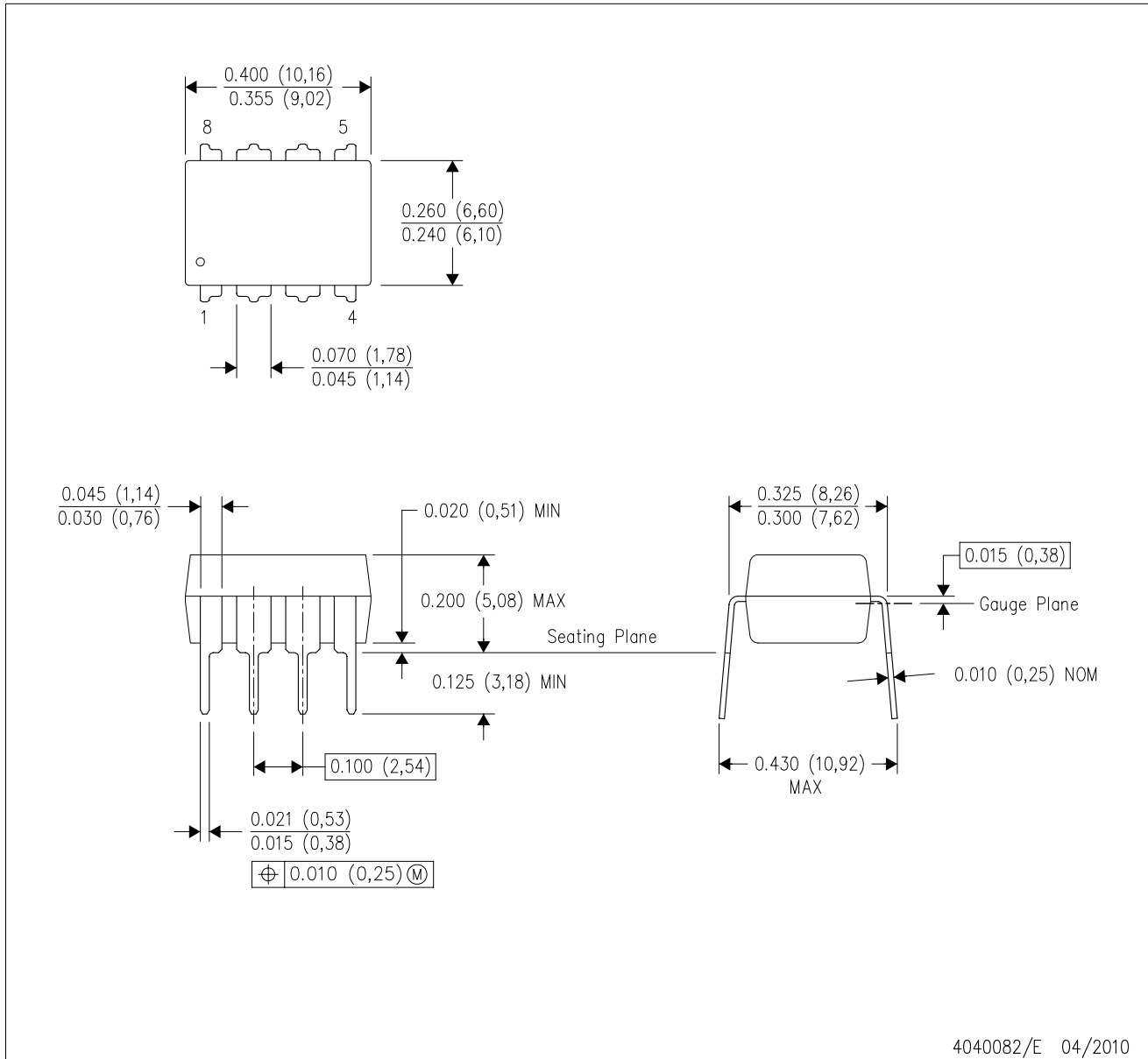
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

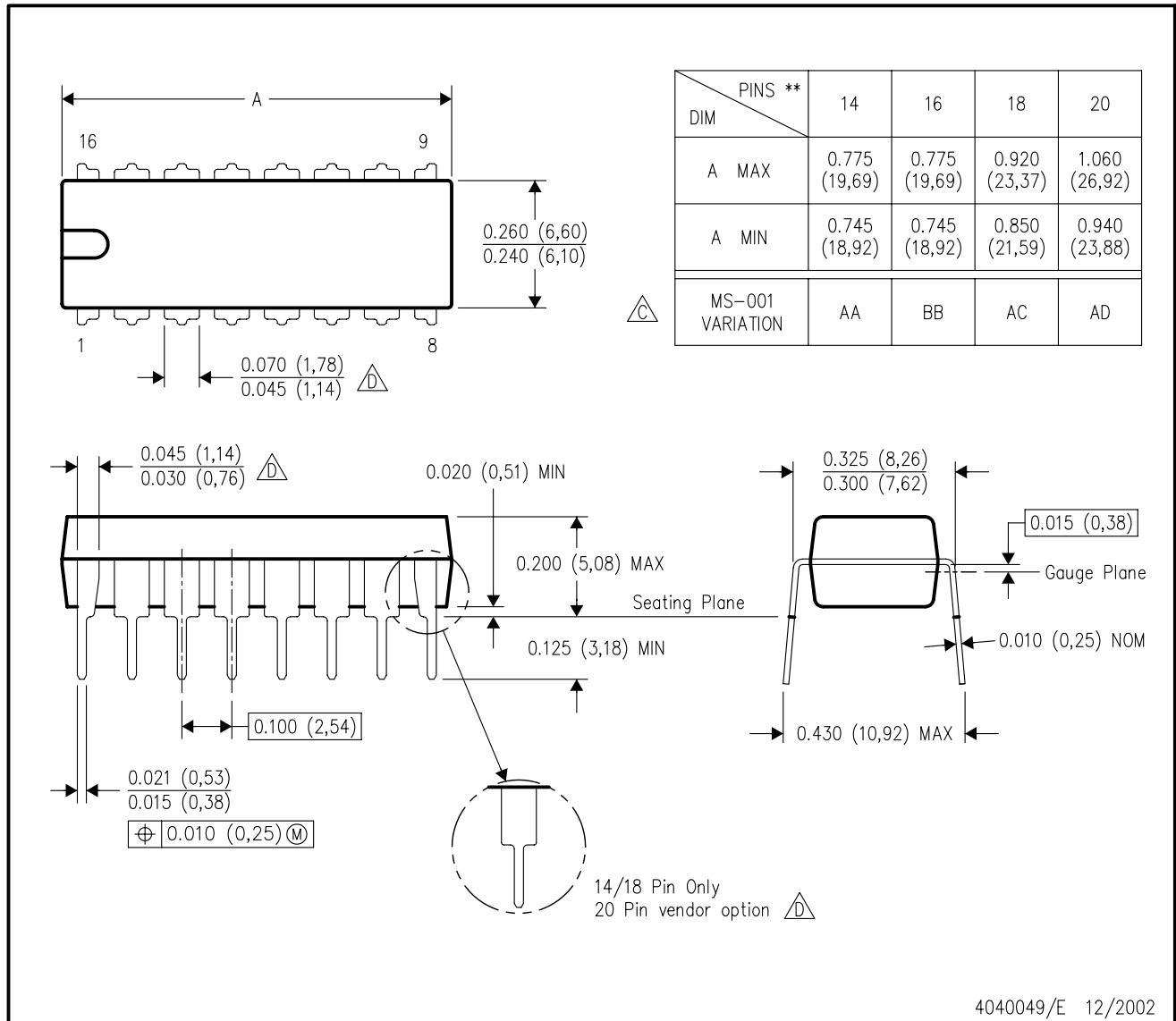


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

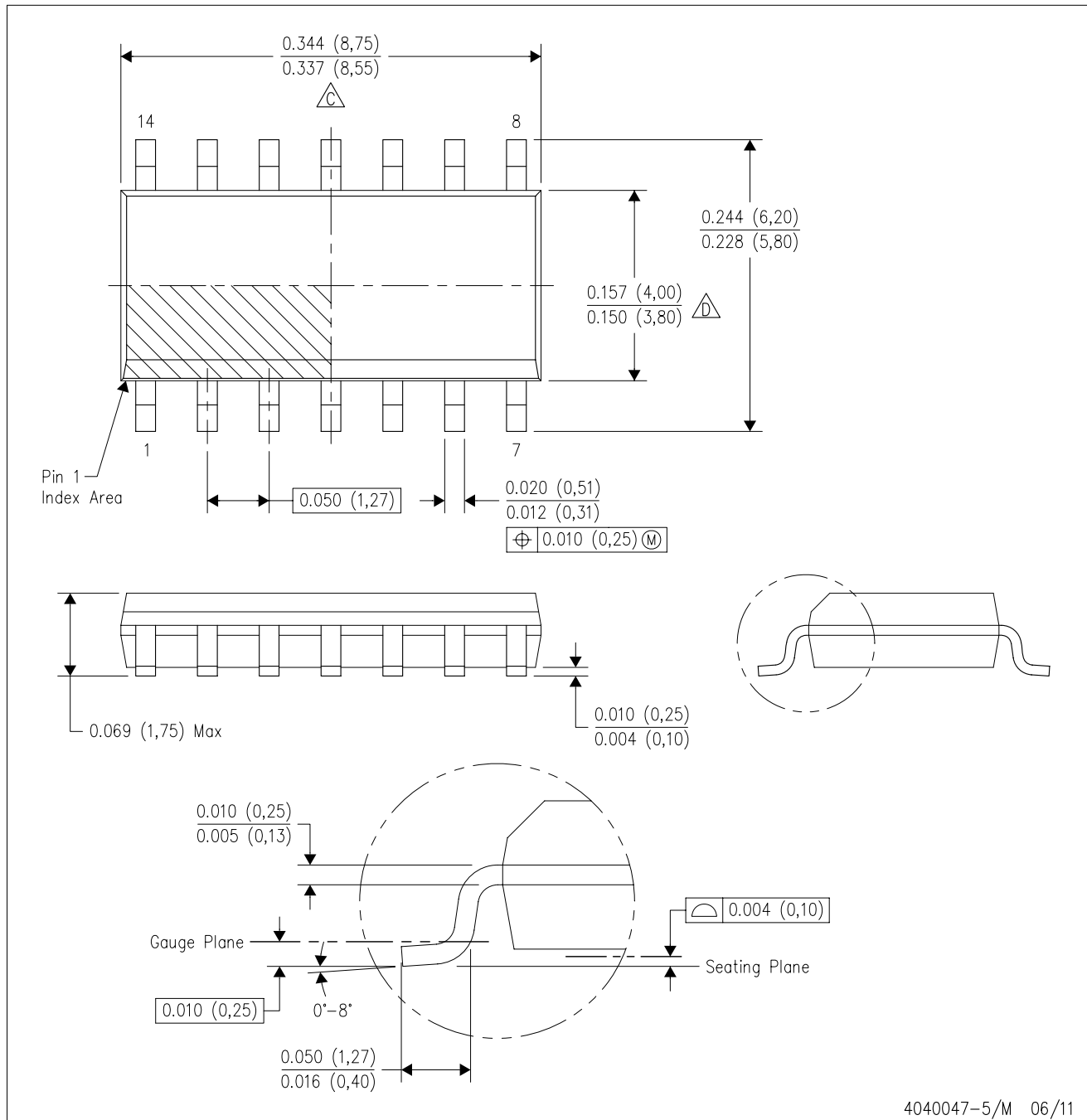
4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

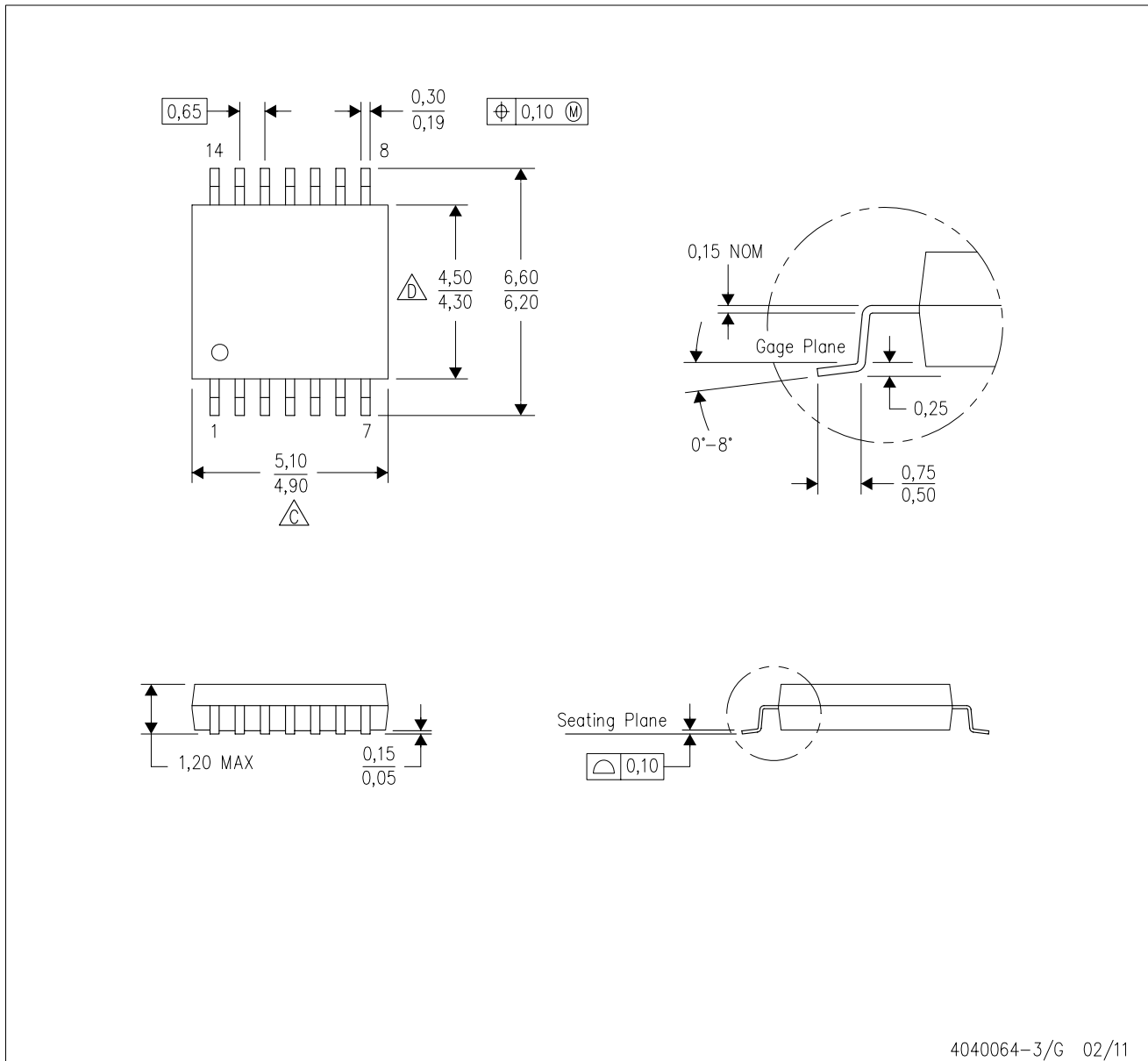
PLASTIC SMALL OUTLINE





- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

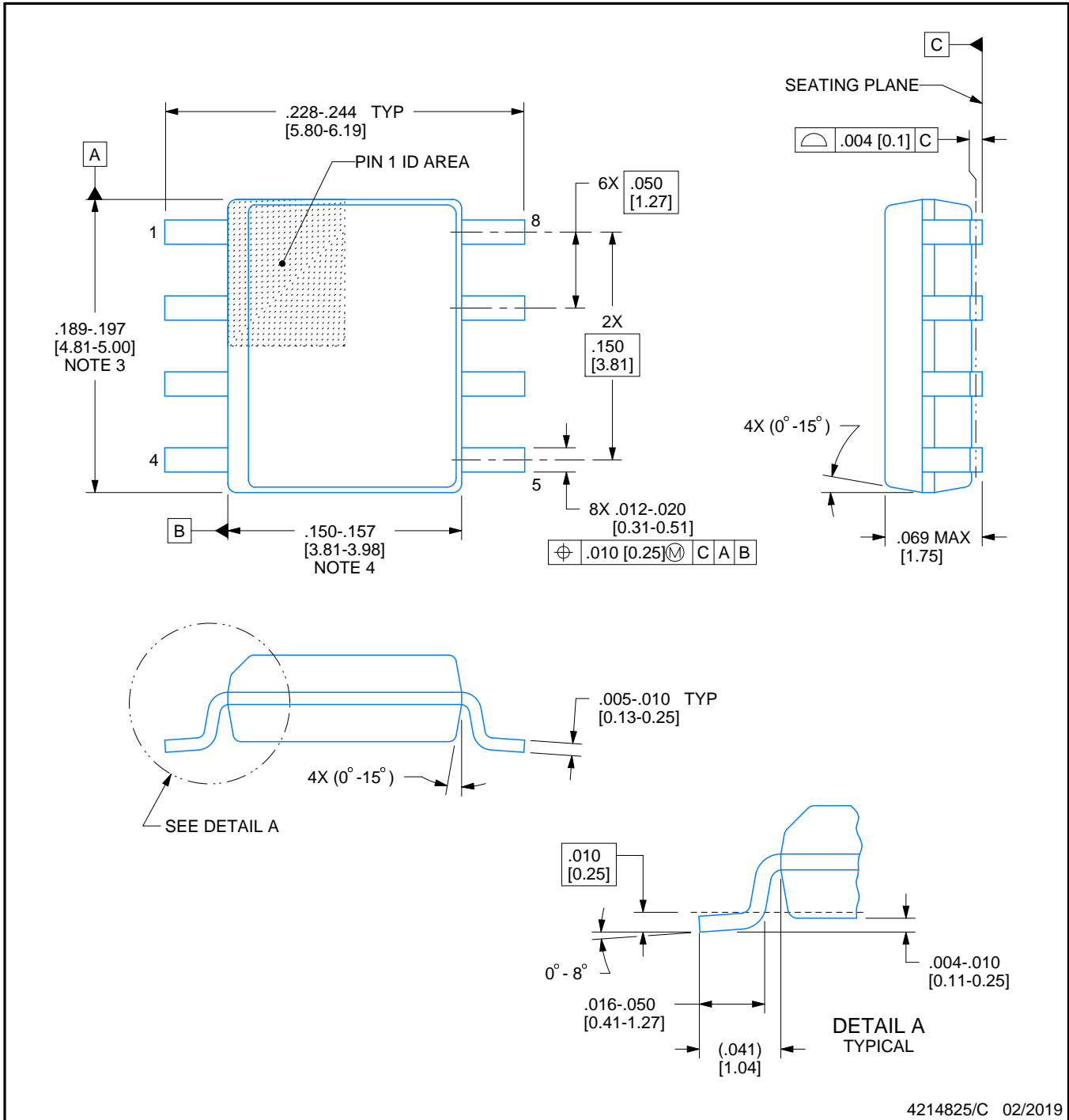


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

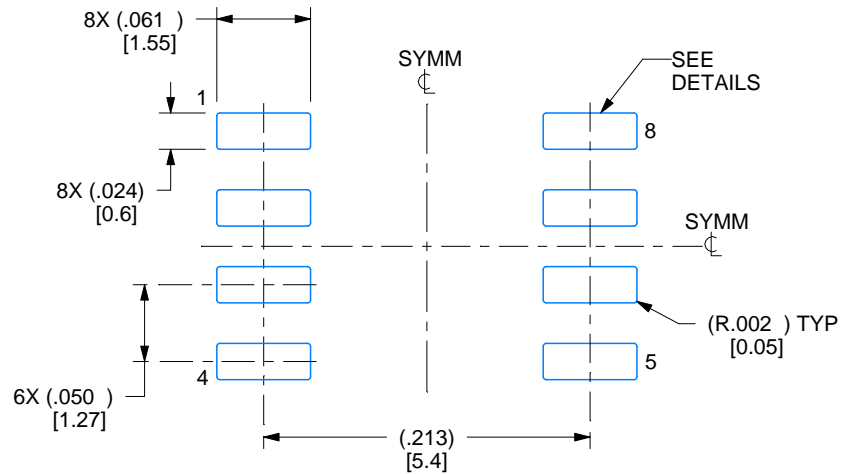
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

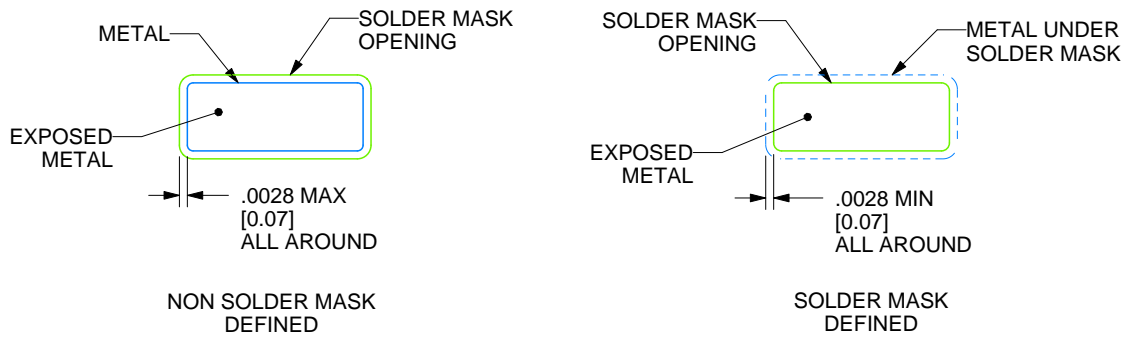
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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