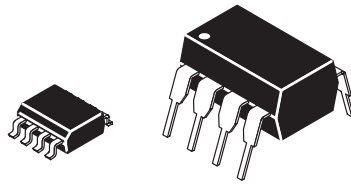




**THE DATASHEET OF
SN65LBC182P**





DIFFERENTIAL BUS TRANSCEIVER

FEATURES

- **One-Fourth Unit Load Allows up to 128 Devices on a Bus**
- **ESD Protection for Bus Terminals:**
 - ± 15 -kV Human Body Model
 - ± 8 -kV IEC61000-4-2, Contact Discharge
 - ± 15 -kV IEC61000-4-2, Air-Gap Discharge
- **Meets or Exceeds the Requirements of ANSI Standard TIA/EIA-485-A and ISO 8482: 1987(E)**
- **Controlled Driver Output-Voltage Slew Rates Allow Longer Cable Stub Lengths**
- **Designed for Signaling Rates† Up to 250-kbps**
- **Low Disabled Supply Current . . . 250 μ A Max**
- **Thermal Shutdown Protection**
- **Open-Circuit Fail-Safe Receiver Design**
- **Receiver Input Hysteresis . . . 70 mV Typ**
- **Glitch-Free Power-Up and Power-Down Protection**

APPLICATIONS

- **Utility Meters**
- **Industrial Process Control**
- **Building Automation**

DESCRIPTION

The SN65LBC182 and SN75LBC182 are differential data line transceivers with a high level of ESD protection in the trade-standard footprint of the SN75176. They are designed for balanced transmission lines and meet ANSI standard TIA/EIA-485-A and ISO 8482. The SN65LBC182 and SN75LBC182 combine a 3-state, differential line driver and differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control.

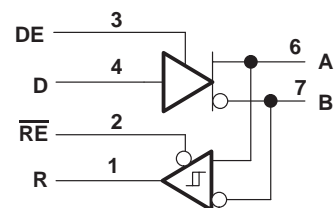
The driver outputs and the receiver inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus. This port operates over a wide range of common-mode voltage, making the device suitable for party-line applications. The device also includes additional features for party-line data buses in electrically noisy environment applications such as industrial process control or power inverters.

The SN75LBC182 and SN65LBC182 bus pins also exhibit a high input resistance equivalent to one-fourth unit load allowing connection of up to 128 similar devices on the bus. The high ESD tolerance protects the device for cabled connections. (For an even higher level of protection, see the SN65/75LBC184, literature number SLLS236.)

The differential driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled voltage transitions. The receiver design provides a fail-safe output of a high level when the inputs are left floating (open circuit). Very low device supply current can be achieved by disabling the driver and the receiver.

The SN65LBC182 is characterized for operation from -40°C to 85°C , and the SN75LBC182 is characterized for operation from 0°C to 70°C .

functional block diagram



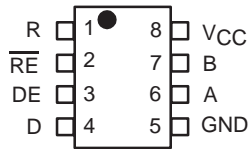
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

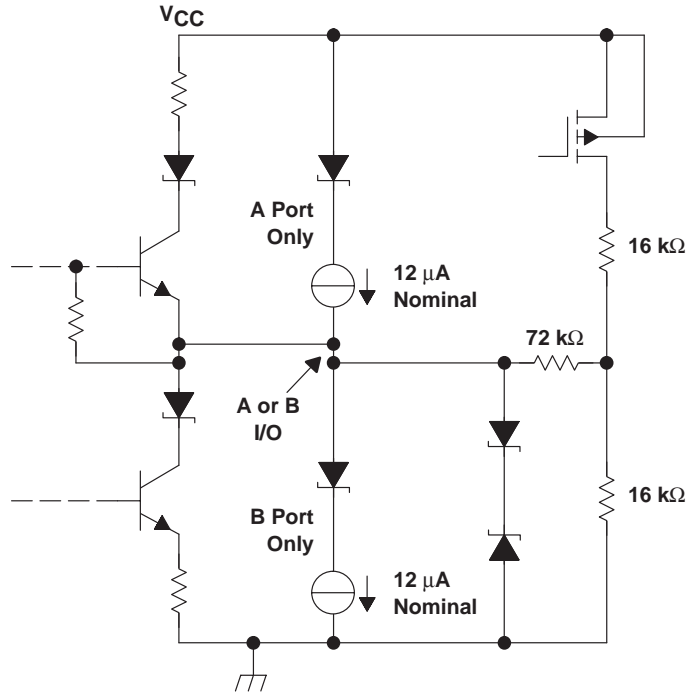
SN65LBC182 SN75LBC182

SLLS500A – MAY 2001 – REVISED MARCH 2005

SN65LBC182D (Marked as 6LB182)
 SN75LBC182D (Marked as 7LB182)
 SN65LBC182P (Marked as 65LBC182)
 SN75LBC182P (Marked as 75LBC182)
 (TOP VIEW)



schematic of inputs and outputs



Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H

AVAILABLE OPTIONS

T _A	PACKAGE	
	PLASTIC SMALL-OUTLINE† (JEDEC MS-012)	PLASTIC DUAL-IN-LINE PACKAGE (JEDEC MS-001)
0°C to 70°C	SN75LBC182D	SN75LBC182P
-40°C to 85°C	SN65LBC182D	SN65LBC182P

† Add R suffix for taped and reel.

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

driver electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = -18 mA	-1.5			V
V _O	Output voltage	I _O = 0	0		V _{CC}	V
V _{OD}	Differential output voltage	R _L = 54 Ω, See Figure 1	1.5	2.2	V _{CC}	V
		V _{test} = -7 V to 12 V, See Figure 2	1.5	2.2	V _{CC}	V
ΔV _{OD}	Change in magnitude of differential output voltage	See Figure 1	-0.2		0.2	V
V _{OC(SS)}	Steady-state common-mode output voltage		1		3	
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage	See Figures 1 and 4	-0.2		0.2	
V _{OC(PP)}	Peak-to-peak change in common-mode output voltage during state transitions		0.8			V
I _{OZ}	High-impedance output current	See receiver input currents				
I _{IH}	High-level input current (D, DE)	V _I = 2.4 V			50	μA
I _{IL}	Low-level input current (D, DE)	V _I = 0.4 V	-50			μA
I _{OS}	Short-circuit output current	V _O = -7 V to 12 V	-250		250	mA
I _{CC}	Supply current	SN75LBC182	No load, DE at V _{CC} , \overline{RE} at V _{CC}	12	25	mA
		SN65LBC182		12	30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _r	Differential output signal rise time	R _L = 54 Ω, C _L = 50 pF, See Figure 3	0.25	0.72	1.2	μs
t _f	Differential output signal fall time		0.25	0.73	1.2	
t _{PLH}	Propagation delay time, low-to-high-level output				1.3	
t _{PHL}	Propagation delay time, high-to-low-level output				1.3	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			0.075	0.15	
t _{PZH}	Output enable time to high level	R _L = 110 Ω, See Figure 5			3.5	μs
t _{PHZ}	Output disable time from high level				3.5	
t _{PZL}	Output enable time to low level	R _L = 110 Ω, See Figure 6			3.5	μs
t _{PLZ}	Output disable time from low level				3.5	

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

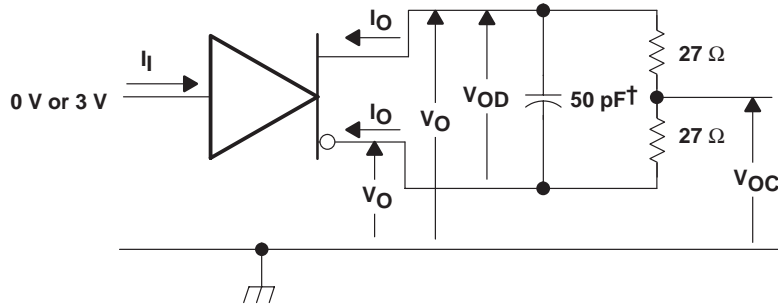
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage				0.2	V
V_{IT-}	Negative-going input threshold voltage		-0.2			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			70		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18$ mA	-1.5			V
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV, $I_O = -8$ mA, See Figure 7	2.8			V
V_{OL}	Low-level output voltage	$V_{ID} = 200$ mV, $I_O = 4$ mA, See Figure 7			0.4	V
I_{OZ}	High-impedance-state output current	$V_O = 0.4$ to 2.4 V			± 1	μ A
I_I	Bus input current	$V_{IH} = 12$ V, $V_{CC} = 5$ V	Other input at 0 V		250	μ A
		$V_{IH} = 12$ V, $V_{CC} = 0$ V			250	
		$V_{IH} = -7$ V, $V_{CC} = 5$ V			-200	
		$V_{IH} = -7$ V, $V_{CC} = 0$ V			-200	
I_{IH}	High-level input current (\overline{RE})	$V_{IH} = 2$ V			50	μ A
I_{IL}	Low-level input current (\overline{RE})	$V_{IL} = 0.8$ V	-50			μ A
I_{CC}	Supply current	No load	DE at 0 V, \overline{RE} at 0 V		3.5	mA
			DE at 0 V, \overline{RE} at V_{CC}		175 250	μ A

† All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	$C_L = 50$ pF, See Figure 7		20		ns
t_f	Differential output signal fall time			20		
t_{PLH}	Propagation delay time, low-to-high-level output				150	
t_{PHL}	Propagation delay time, high-to-low-level output				150	
t_{PZH}	Output enable time to high level	See Figure 8		100		ns
t_{PZL}	Output enable time to low level			100		
t_{PHZ}	Output disable time from high level				100	ns
t_{PLZ}	Output disable time from low level				100	
$t_{sk(p)}$	Pulse skew $ t_{PHL} - t_{PLH} $			50	ns	

PARAMETER MEASUREMENT INFORMATION



†Includes probe and jig capacitance

Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

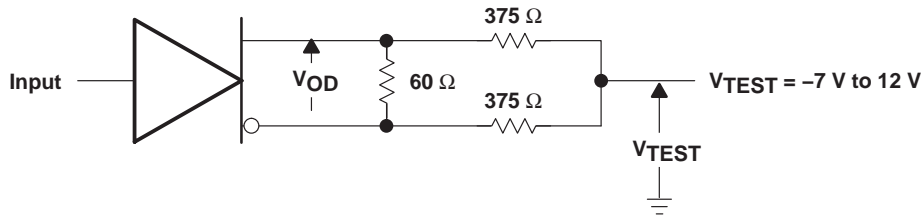
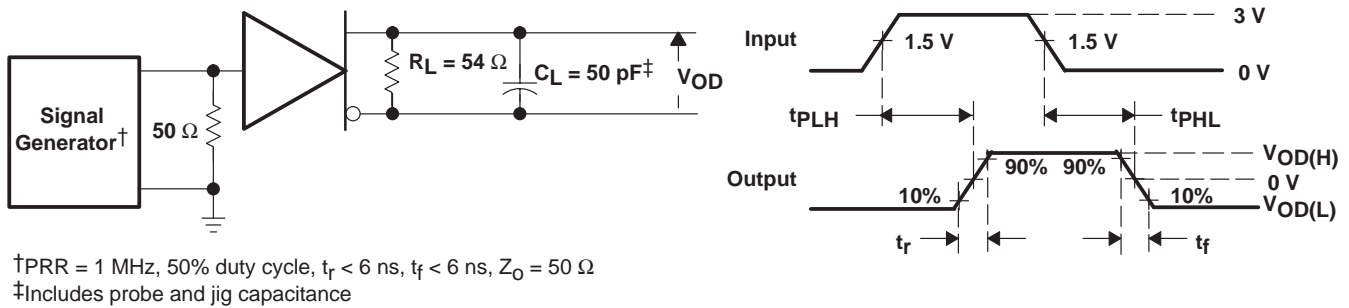


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading



†PRR = 1 MHz, 50% duty cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_0 = 50 \Omega$

‡Includes probe and jig capacitance

Figure 3. Driver Switching Test Circuit and Waveforms

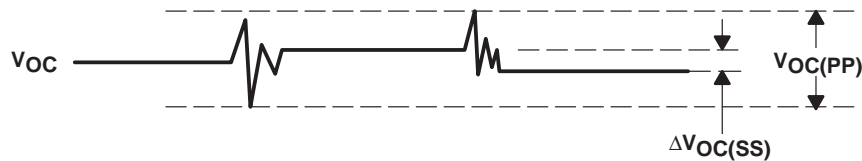
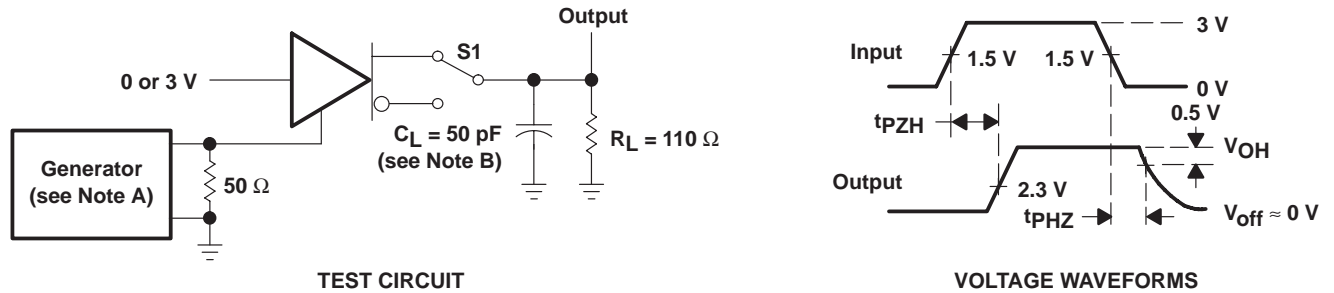


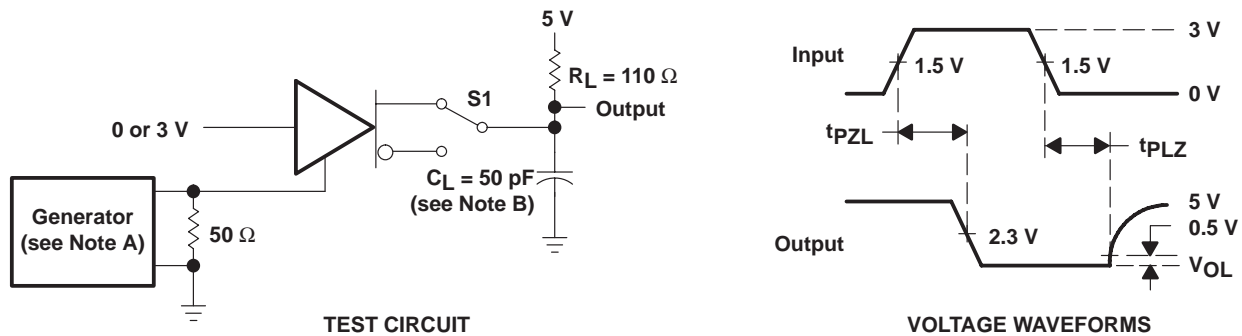
Figure 4. V_{OC} Definitions

PARAMETER MEASUREMENT INFORMATION



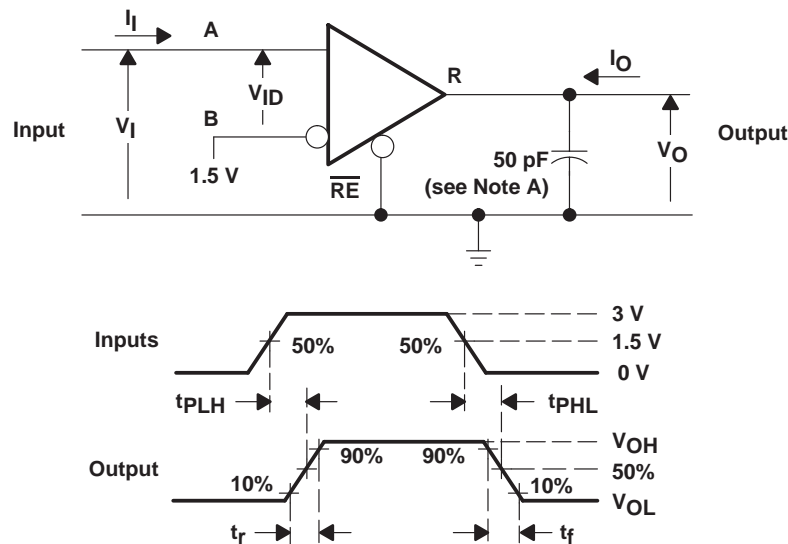
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 5. Driver t_{pZH} and t_{pHZ} Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

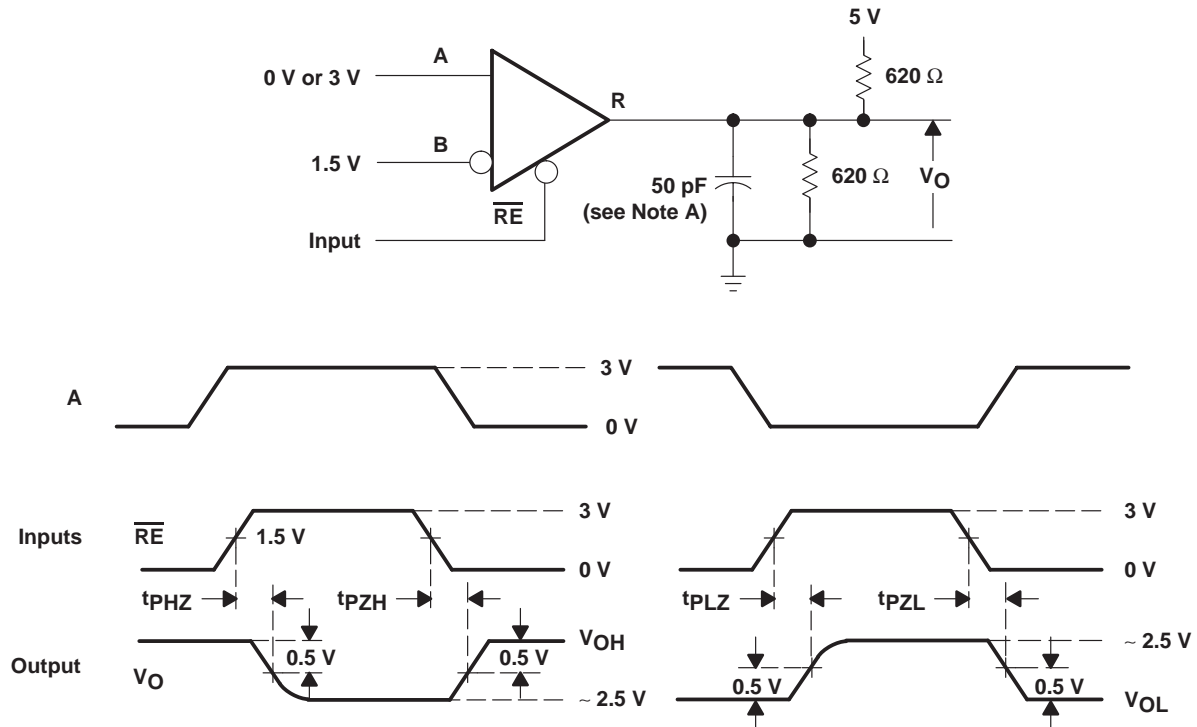
Figure 6. Driver t_{pZL} and t_{pLZ} Test Circuit and Voltage Waveforms



NOTE A: This value includes probe and jig capacitance ($\pm 10\%$).

Figure 7. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This value includes probe and jig capacitance ($\pm 10\%$).

Figure 8. Receiver t_{PZL} , t_{PLZ} , t_{PZH} , and t_{PHZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

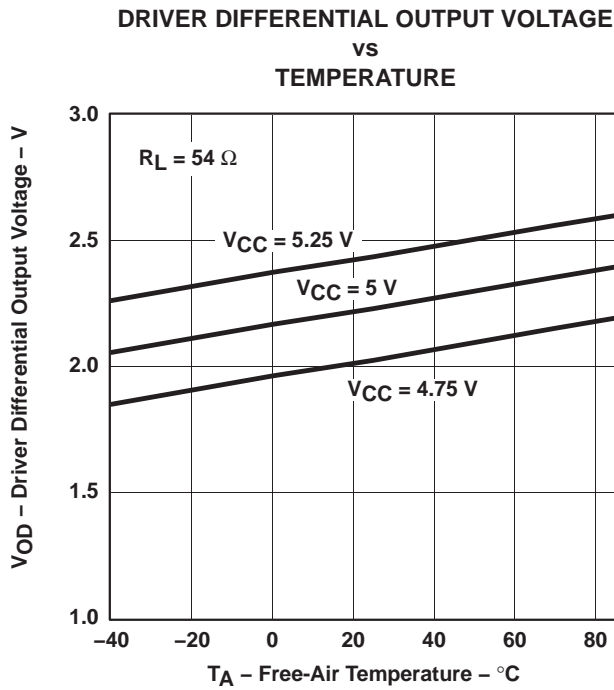


Figure 9

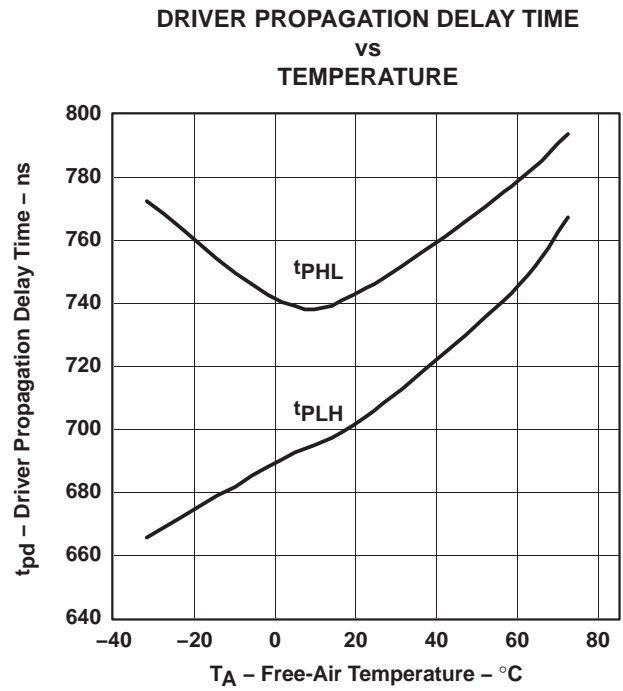


Figure 10

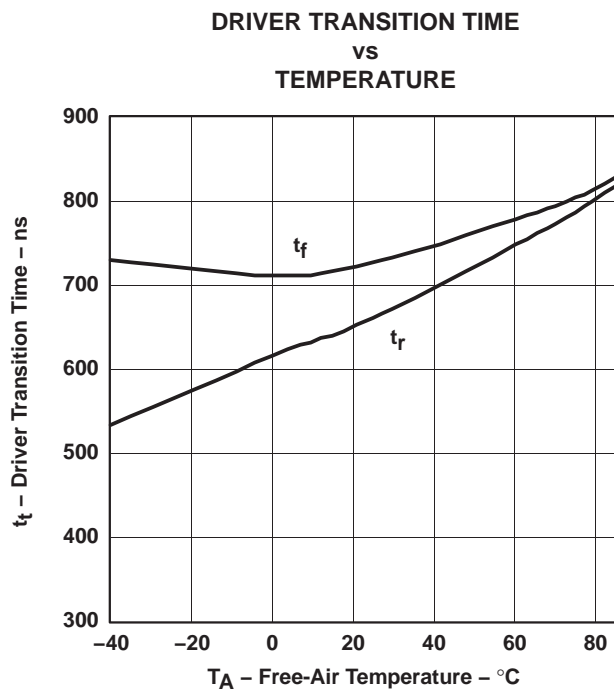


Figure 11

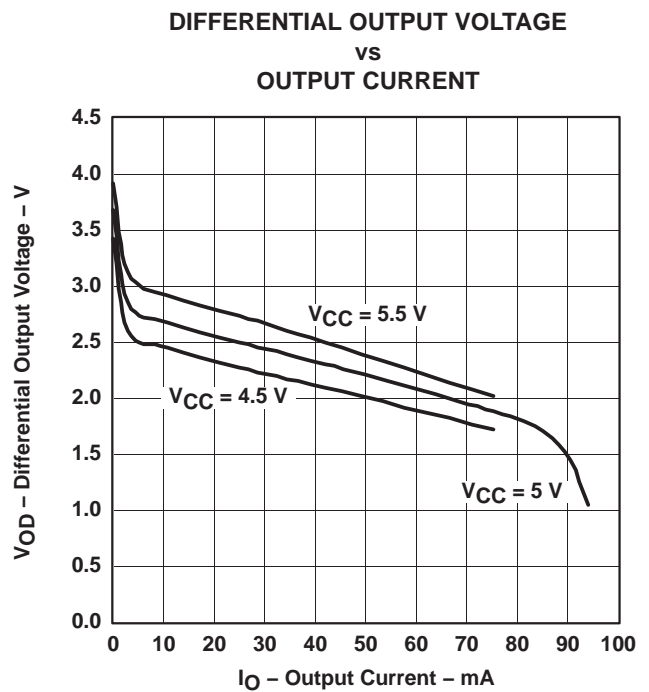


Figure 12

TYPICAL CHARACTERISTICS

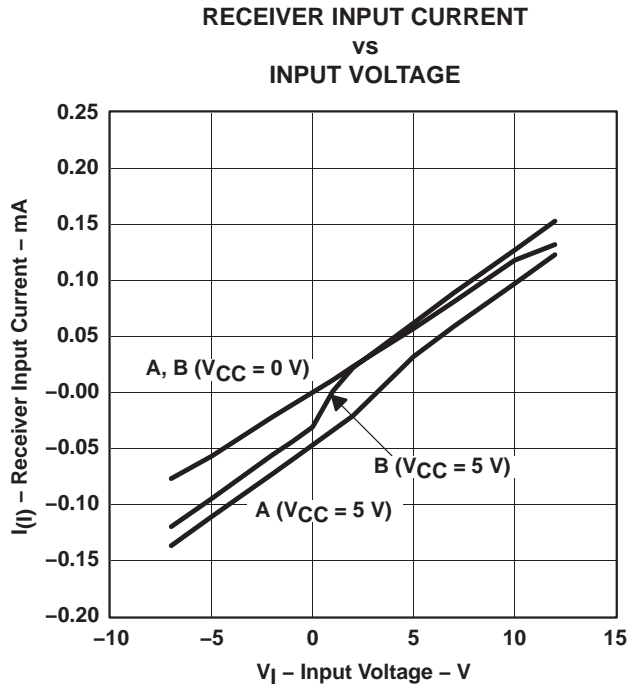
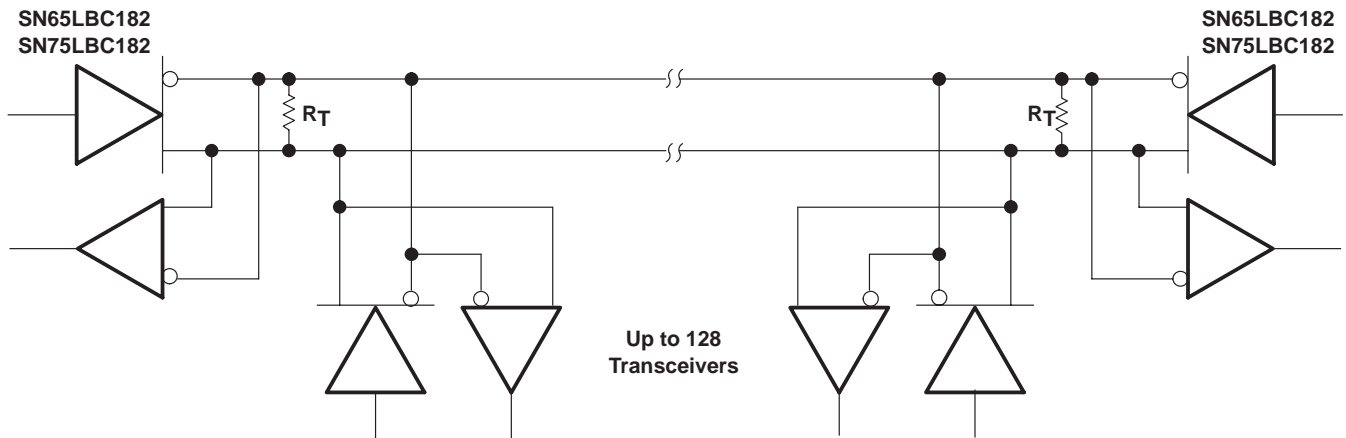


Figure 13

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 14. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC182D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65LBC182	Samples
SN75LBC182D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	75LBC182	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC182DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC182DR	SOIC	D	8	2500	340.5	338.1	20.6

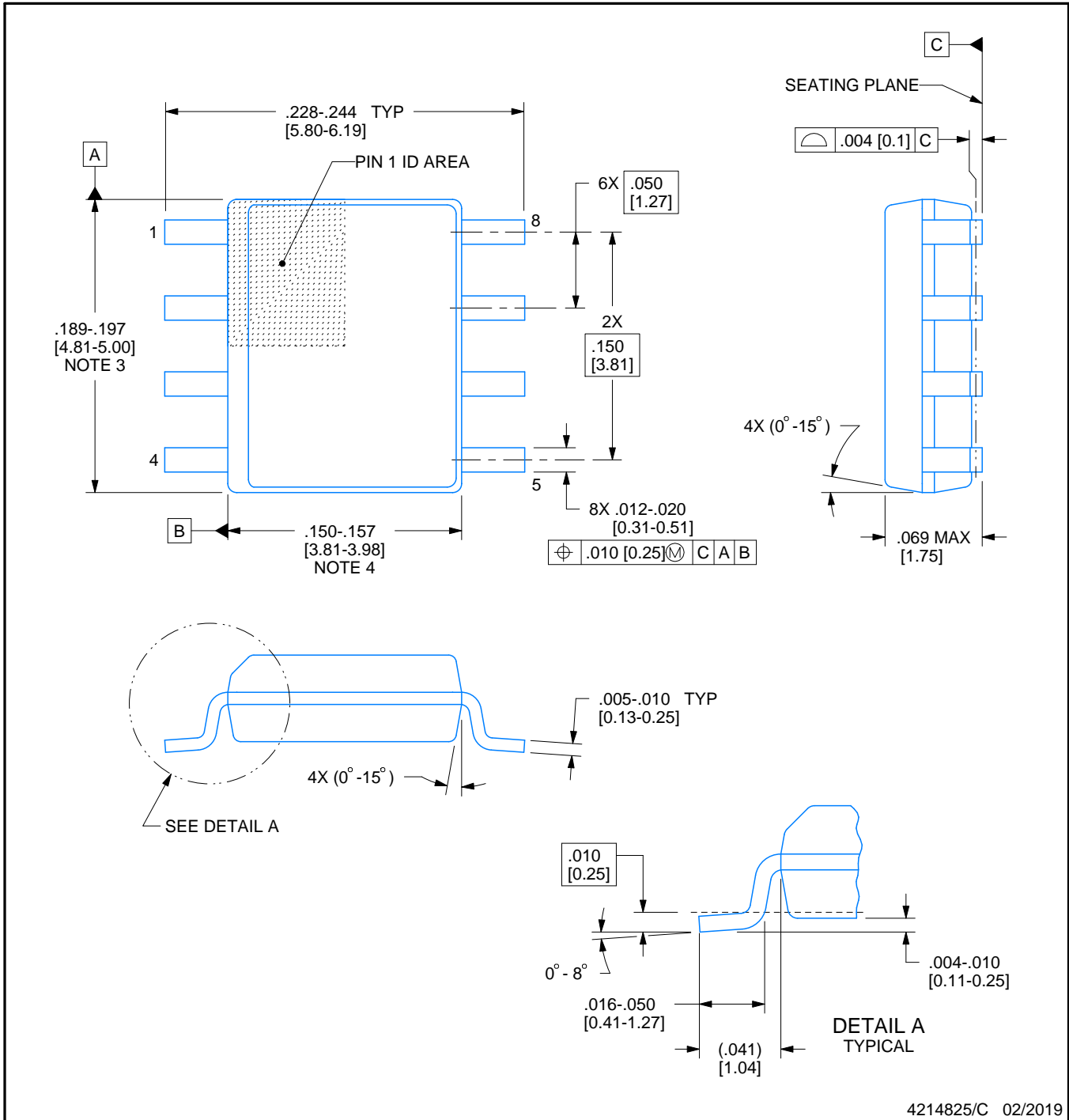


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

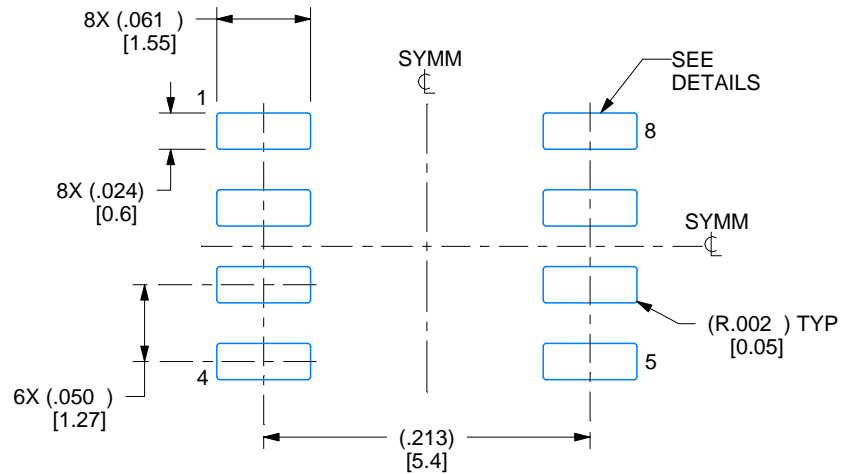
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

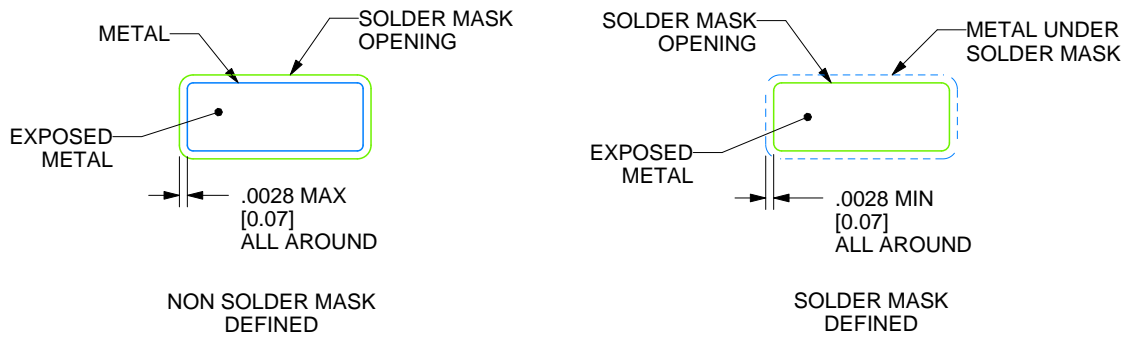
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

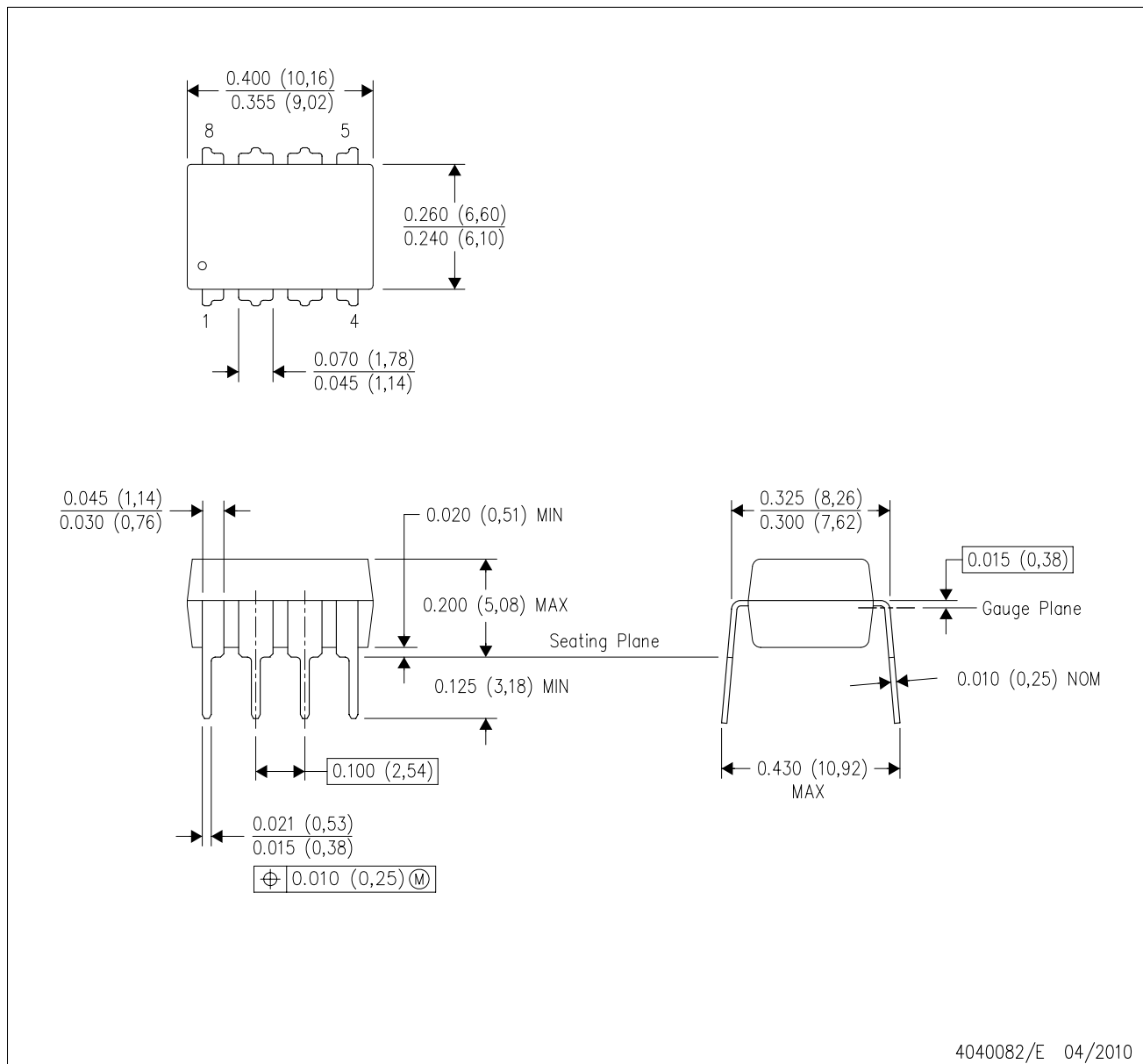
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management