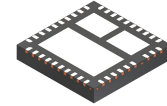




**THE DATASHEET OF
FDMF3030**



Extra-Small, High-Performance, High-Frequency, DrMOS Module



PQFN40 6x6, 0.5P
CASE 483AN

FDMF3030

Description

The DrMOS family is **onsemi**'s next-generation, fully optimized, ultra-compact, integrated MOSFET-plus-driver, power-stage solution for high-current, high-frequency, synchronous buck, DC-DC applications. The FDMF3030 integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra-compact, 6x6 mm package.

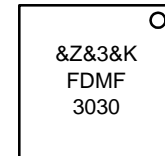
With an integrated approach, the complete switching power stage is optimized with regard to driver and MOSFET dynamic performance, system inductance, and power MOSFET $R_{DS(ON)}$. The FDMF3030 uses **onsemi**'s high-performance POWERTRENCH[®] MOSFET technology, which dramatically reduces switch ringing, eliminating the need for a snubber circuit in most buck converter applications.

A driver IC with reduced dead times and propagation delays further enhances performance. A thermal warning function indicates a potential over-temperature situation. The FDMF3030 also incorporates a Zero-Cross Detect (ZCD_EN# pin) for improved light-load efficiency and provides a 3-state 5 V PWM input for compatibility with a wide range of PWM controllers.

Features

- Over 93% Peak-Efficiency
- High-Current Handling: 50 A
- High-Performance PQFN Copper-Clip Package
- 3-State 5 V PWM Input Driver
- Automatic Diode Emulation (Skip Mode) Enabled through ZCD_EN# Input
- Thermal Warning Flag for Over-Temperature Condition
- Driver Output Disable Function (DISB# Pin)
- Internal Pull-Up and Pull-Down for ZCD_EN# and DISB# Inputs, Respectively
- **onsemi** POWERTRENCH Technology MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- **onsemi** SyncFET[™] Technology (Integrated Schottky Diode) in Low-Side MOSFET
- Integrated Bootstrap Schottky Diode
- Adaptive Gate-Drive Timing for Shoot-Through Protection
- Under-Voltage Lockout (UVLO)
- Optimized for Switching Frequencies up to 1 MHz
- Low-Profile SMD Package
- Based on the Intel[®] 4.0 DrMOS Standard
- This Device is Pb-Free, Halide Free and is RoHS Compliant

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code
- &K = 2-Digits Lot Run Traceability Code
- FDMF3030 = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

Benefits

- Ultra-Compact 6x6 mm PQFN, 72% Space-Saving Compared to Conventional Discrete Solutions
- Fully Optimized for System Efficiency
- Clean-Switching Waveforms with Minimal Ringing
- High-Current Handling

Applications

- Notebook Computers
- High-Performance Gaming Motherboards
- Compact Blade Servers & Workstations, V-Core and Non-V-Core DC-DC Converters
- Desktop Computers, V-Core and Non-V-Core DC-DC Converters
- High-Current DC-DC Point-of-Load Converters
- Networking and Telecom Microprocessor Voltage Regulators
- Small Form-Factor Voltage Regulator Modules

FDMF3030

TYPICAL APPLICATION CIRCUIT

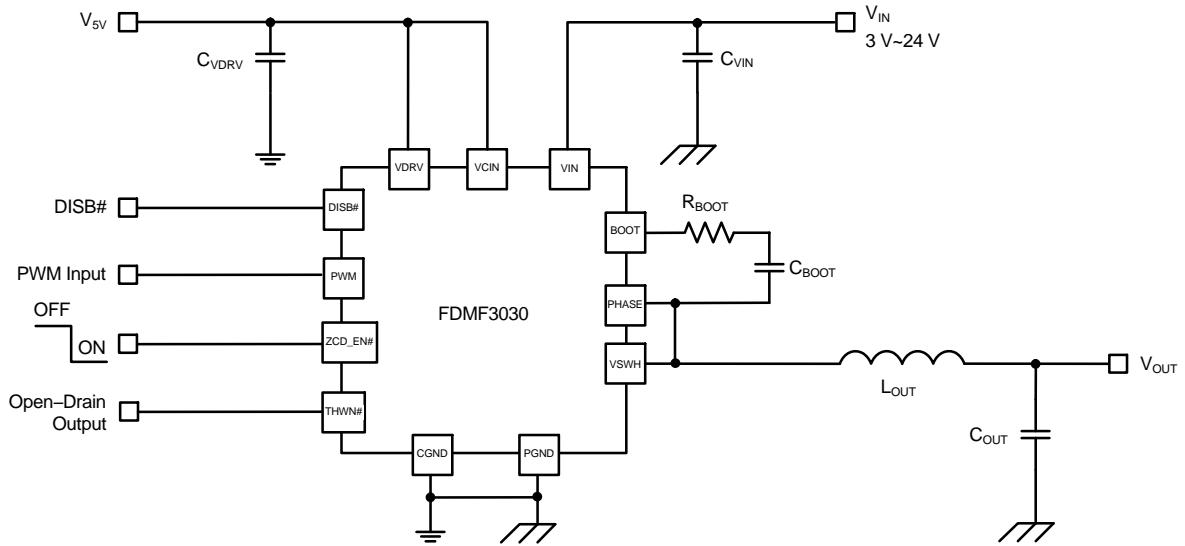


Figure 1. Typical Application Circuit

DrMOS BLOCK DIAGRAM

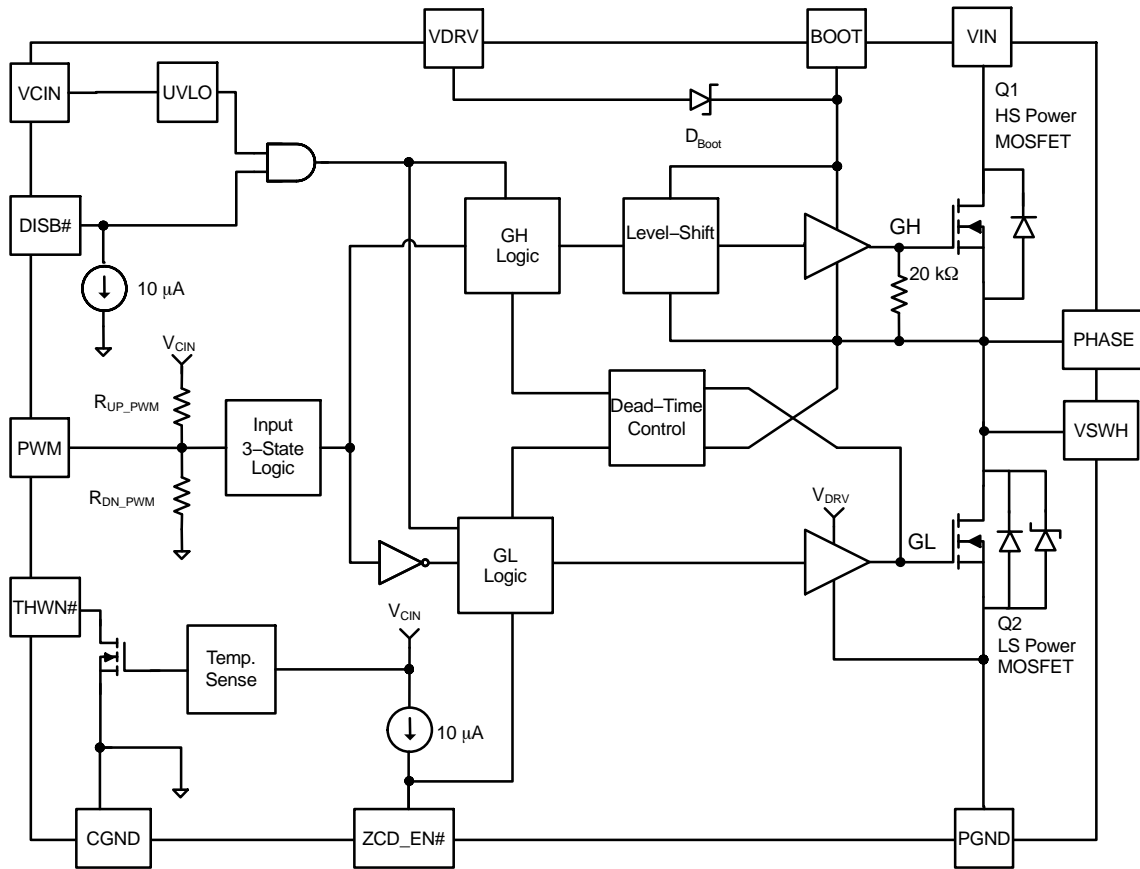


Figure 2. DrMOS Block Diagram

FDMF3030

PIN CONFIGURATION

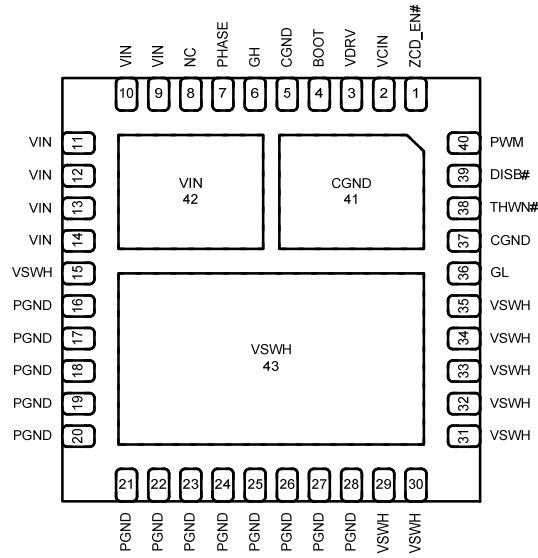


Figure 3. Top View

PIN DEFINITIONS

Pin #	Name	Description
1	ZCD_EN#	When ZCD_EN# = HIGH, the low-side driver is the inverse of the PWM input. When ZCD_EN# = LOW, diode emulation is enabled. This pin has a 10 μ A internal pull-up current source. Do not add a noise filter capacitor.
2	VCIN	IC bias supply. Minimum 1 μ F ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for the gate driver. Minimum 1 μ F ceramic capacitor is recommended to be connected as close as possible from this pin to CGND.
4	BOOT	Bootstrap supply input. Provides voltage supply to the high-side MOSFET driver. Connect a bootstrap capacitor from this pin to PHASE.
5, 37, 41	CGND	IC ground. Ground return for driver IC.
6	GH	For manufacturing test only. This pin must float; it must not be connected to any pin.
7	PHASE	Switch node pin for bootstrap capacitor routing. Electrically shorted to VSWH pin.
8	NC	No connect. The pin is not electrically connected internally, but can be connected to VIN for convenience.
9–14, 42	VIN	Power input. Output stage supply voltage.
15, 29–35, 43	VSWH	Switch node input. Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
16–28	PGND	Power ground. Output stage ground. Source pin of the low-side MOSFET.
36	GL	For manufacturing test only. This pin must float; it must not be connected to any pin.
38	THWN#	Thermal warning flag, open collector output. When temperature exceeds the trip limit, the output is pulled LOW. THWN# does not disable the module.
39	DISB#	Output disable. When LOW, this pin disables power MOSFET switching (GH and GL are held LOW). This pin has a 10 μ A internal pull-down current source. Do not add a noise filter capacitor.
40	PWM	PWM signal input. This pin accepts a three-state 5 V PWM signal from the controller.

FDMF3030

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V _{CIN}	Supply Voltage	Referenced to CGND	-0.3	7.0	V
V _{DRV}	Drive Voltage	Referenced to CGND	-0.3	7.0	V
V _{DISB#}	Output Disable	Referenced to CGND	-0.3	7.0	V
V _{PWM}	PWM Signal Input	Referenced to CGND	-0.3	7.0	V
V _{ZCD_EN#}	ZCD Enable Signal Input	Referenced to CGND	-0.3	7.0	V
V _{GL}	Low Gate Manufacturing Test Pin	Referenced to CGND	-0.3	7.0	V
V _{THWN#}	Thermal Warning Flag	Referenced to CGND	-0.3	7.0	V
V _{IN}	Power Input	Referenced to PGND, CGND	-0.3	30.0	V
V _{BOOT}	Bootstrap Supply	Referenced to VSWH, PHASE	-0.3	7.0	V
		Referenced to CGND	-0.3	30.0	V
V _{GH}	High Gate Manufacturing Test Pin	Referenced to VSWH, PHASE	-0.3	7.0	V
		Referenced to CGND	-0.3	30.0	V
V _{PHS}	PHASE	Referenced to CGND	-0.3	30.0	V
V _{SWH}	Switch Node Input	Referenced to PGND, CGND (DC Only)	-0.3	30.0	V
		Referenced to PGND, <20 ns	-8.0	33.0	V
V _{BOOT}	Bootstrap Supply	Referenced to VDRV	-	22.0	V
		Referenced to VDRV, <20 ns	-	25.0	V
I _{THWN#}	THWN# Sink Current		-0.1	7.0	mA
I _{O(AV)}	Output Current (Note 1)	f _{SW} = 300 kHz, V _{IN} = 12 V, V _O = 1.0 V	-	50	A
		f _{SW} = 1 MHz, V _{IN} = 12 V, V _O = 1.0 V	-	45	A
θ _{JPCB}	Junction-to-PCB Thermal Resistance (onsemi Evaluation Board)		-	3	°C/W
T _A	Ambient Temperature Range		-40	+125	°C
T _J	Maximum Junction Temperature		-	+150	°C
T _{STG}	Storage Temperature Range		-55	+150	°C
ESD	Electrostatic Discharge Protection	Human Body Model, JESD22-A114	2000	-	V
		Charged Device Model, JESD22-C101	2000	-	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{O(AV)} is rated using onsemi's DrMOS evaluation board, at T_A = 25°C, with natural convection cooling. This rating is limited by the peak DrMOS temperature, T_J = 150°C, and varies depending on operating conditions and PCB layout. This rating can be changed with different application settings.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CIN}	Control Circuit Supply Voltage	4.5	5.0	5.5	V
V _{DRV}	Gate Drive Circuit Supply Voltage	4.5	5.0	5.5	V
V _{IN}	Output Stage Supply Voltage	3.0	12.0	24.0 (Note 2)	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Operating at high V_{IN} can create excessive AC overshoots on the VSWH-to-GND and BOOT-to-GND nodes during MOSFET switching transients. For reliable DrMOS operation, VSWH-to-GND and BOOT-to-GND must remain at or below the Absolute Maximum Ratings shown in the table above. Refer to the ["Application Information"](#) and ["PCB Layout Guidelines"](#) sections of this datasheet for additional information.

FDMF3030

ELECTRICAL CHARACTERISTICS (Typical values are $V_{IN} = 12\text{ V}$, $V_{CIN} = 5\text{ V}$, $V_{DRV} = 5\text{ V}$, and $T_A = T_J = +25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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BASIC OPERATION

I_Q	Quiescent Current	$I_Q = I_{VCIN} + I_{VDRV}$, PWM = LOW or HIGH or Float	–	–	2	mA
V_{UVLO}	UVLO Threshold	V_{CIN} Rising	–	3.3	–	V
V_{UVLO_HYS}	UVLO Hysteresis		–	0.35	–	V

PWM INPUT ($V_{CIN} = V_{DRV} = 5\text{ V} \pm 10\%$)

R_{UP_PWM}	Pull-Up Impedance	$V_{PWM} = 5\text{ V}$	–	20	–	k Ω
R_{DN_PWM}	Pull-Down Impedance	$V_{PWM} = 0\text{ V}$	–	20	–	k Ω
V_{IH_PWM}	PWM High Level Voltage		3.15	3.80	4.45	V
V_{TRI_HI}	3-State Upper Threshold		3.10	3.75	4.40	V
V_{TRI_LO}	3-State Lower Threshold		1.05	1.40	1.90	V
V_{IL_PWM}	PWM Low Level Voltage		0.70	1.00	1.30	V
$t_{D_HOLD-OFF}$	3-State Shut-Off Time		–	150	–	ns
V_{HiZ_PWM}	3-State Open Voltage		2.20	2.50	2.80	V
$t_{PWM-OFF_MIN}$	PWM Minimum Off Time		70	–	–	ns

PWM INPUT ($V_{CIN} = V_{DRV} = 5\text{ V} \pm 5\%$)

R_{UP_PWM}	Pull-Up Impedance	$V_{PWM} = 5\text{ V}$	–	20	–	k Ω
R_{DN_PWM}	Pull-Down Impedance	$V_{PWM} = 0\text{ V}$	–	20	–	k Ω
V_{IH_PWM}	PWM High Level Voltage		3.35	3.80	4.25	V
V_{TRI_HI}	3-State Upper Threshold		3.30	3.75	4.20	V
V_{TRI_LO}	3-State Lower Threshold		1.10	1.40	1.75	V
V_{IL_PWM}	PWM Low Level Voltage		0.74	1.00	1.26	V
$t_{D_HOLD-OFF}$	3-State Shut-Off Time		–	150	–	ns
V_{HiZ_PWM}	3-State Open Voltage		2.30	2.50	2.70	V
$t_{PWM-OFF_MIN}$	PWM Minimum Off Time		70	–	–	ns

DISB# INPUT

V_{IH_DISB}	High-Level Input Voltage		2	–	–	V
V_{IL_DISB}	Low-Level Input Voltage		–	–	0.8	V
I_{PLD}	Pull-Down Current		–	10	–	μA
t_{PD_DISBL}	Propagation Delay	PWM = GND, Delay Between DISB# from HIGH to LOW to GL from HIGH to LOW	–	220	–	ns
t_{PD_DISBH}	Propagation Delay	PWM = GND, Delay Between DISB# from LOW to HIGH to GL from LOW to HIGH	–	520	–	ns

ZCD_EN# INPUT

$V_{IH_ZCD_EN}$	High-Level Input Voltage		2	–	–	V
$V_{IL_ZCD_EN}$	Low-Level Input Voltage		–	–	0.8	V
I_{PLU}	Pull-Up Current		–	10	–	μA
t_{PD_ZLGLL}	Propagation Delay	PWM = GND, Delay Between ZCD_EN# from HIGH to LOW to GL from HIGH to LOW	–	1800	–	ns
t_{PD_ZHGLH}	Propagation Delay	PWM = GND, Delay Between ZCD_EN# from LOW to HIGH to GL from LOW to HIGH	–	20	–	ns

FDMF3030

ELECTRICAL CHARACTERISTICS (Typical values are $V_{IN} = 12\text{ V}$, $V_{CIN} = 5\text{ V}$, $V_{DRV} = 5\text{ V}$, and $T_A = T_J = +25^\circ\text{C}$ unless otherwise noted.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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THERMAL WARNING FLAG

T_{ACT}	Activation Temperature		–	150	–	$^\circ\text{C}$
T_{RST}	Reset Temperature		–	135	–	$^\circ\text{C}$
R_{THWN}	Pull-Down Resistance	5 k Ω Resistor Pull-up to V_{CIN}	–	60	–	Ω

HIGH-SIDE DRIVER ($f_{SW} = 1000\text{ kHz}$, $I_{OUT} = 30\text{ A}$, $T_A = +25^\circ\text{C}$)

R_{SOURCE_GH}	Output Impedance, Sourcing	Source Current = 50 mA	–	0.8	–	Ω
R_{SINK_GH}	Output Impedance, Sinking	Sink Current = 50 mA	–	0.6	–	Ω
t_{R_GH}	Rise Time	GH = 10% to 90%	–	10	–	ns
t_{F_GH}	Fall Time	GH = 90% to 10%	–	10	–	ns
t_{D_DEADON}	LS to HS Deadband Time	GL Going LOW to GH Going HIGH, 1.7 V GL to 10% GH	–	20	–	ns
t_{PD_PLGHL}	PWM LOW Propagation Delay	PWM Going LOW to GH Going LOW, V_{IL_PWM} to 90% GH	–	20	–	ns
t_{PD_PHGHH}	PWM HIGH Propagation Delay (ZCD_EN# = 0)	PWM Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH (ZCD_EN# = 0, $I_{D_LS} > 0$)	–	25	–	ns
t_{PD_TSGHH}	Exiting 3-State Propagation Delay	PWM (From 3-State) Going HIGH to GH Going HIGH, V_{IH_PWM} to 10% GH	–	35	–	ns

LOW-SIDE DRIVER ($f_{SW} = 1000\text{ kHz}$, $I_{OUT} = 30\text{ A}$, $T_A = +25^\circ\text{C}$)

R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current = 50 mA	–	0.9	–	Ω
R_{SINK_GL}	Output Impedance, Sinking	Sink Current = 50 mA	–	0.4	–	Ω
t_{R_GL}	Rise Time	GL = 10% to 90%	–	15	–	ns
t_{F_GL}	Fall Time	GL = 90% to 10%	–	10	–	ns
$t_{D_DEADOFF}$	HS to LS Deadband Time	SW Going LOW to GL Going HIGH, 1.7 V SW to 10% GL	–	20	–	ns
t_{PD_PHGLL}	PWM-HIGH Propagation Delay	PWM Going HIGH to GL Going LOW, V_{IH_PWM} to 90% GL	–	20	–	ns
t_{PD_TSGLH}	Exiting 3-State Propagation Delay	PWM (From 3-State) Going LOW to GL Going HIGH, V_{IL_PWM} to 10% GL	–	30	–	ns
$t_{GL_ON_MIN}$	GL Minimum On Time in DCM	$V_{ZCD_EN\#} = 0\text{ V}$	–	350	–	ns

BOOT DIODE

V_F	Forward-Voltage Drop	$I_F = 1\text{ mA}$	–	0.6	–	V
V_R	Breakdown Voltage	$I_R = 1\text{ mA}$	22	–	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FDMF3030

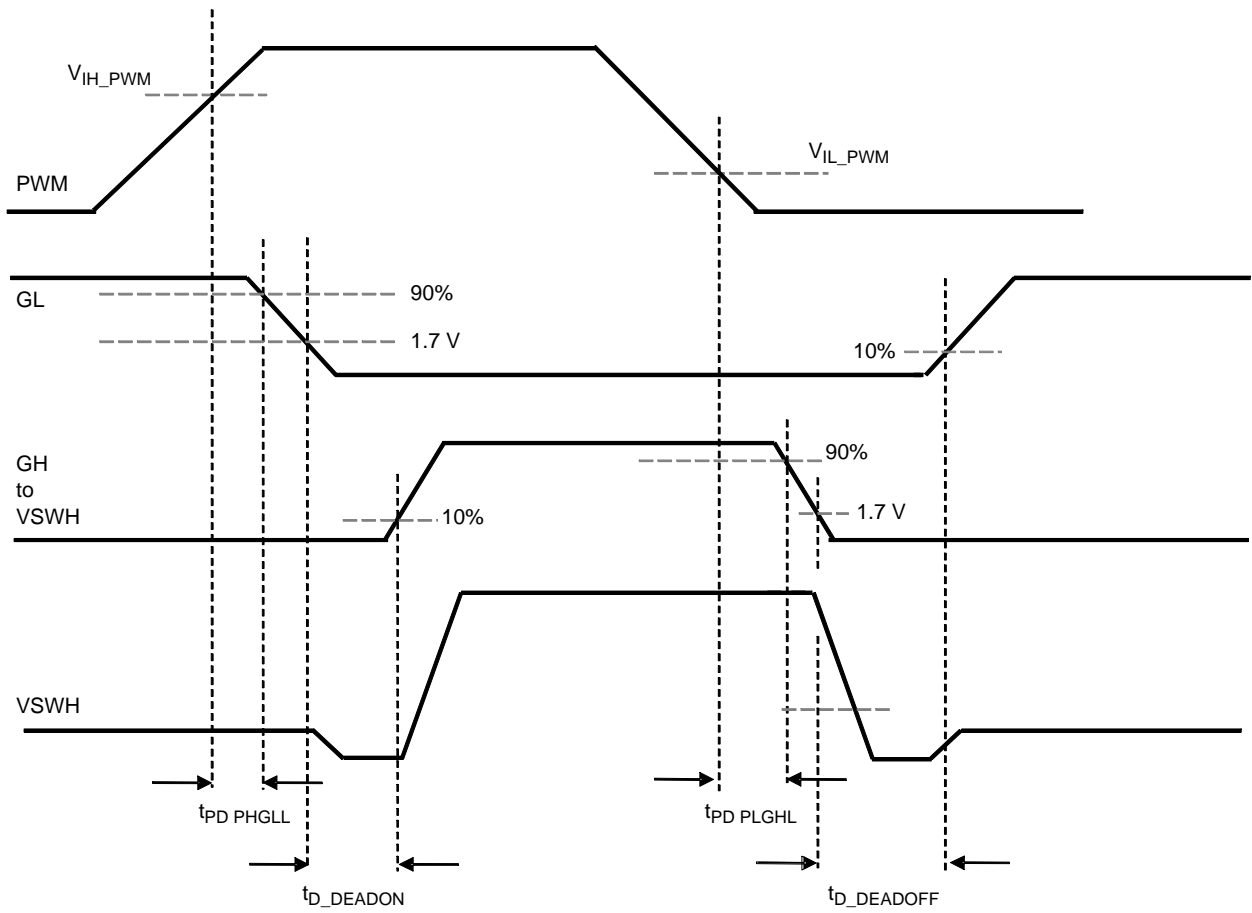


Figure 4. PWM Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: $V_{IN} = 12\text{ V}$ or 19 V , $V_{OUT} = 1\text{ V}$, $V_{CIN} = 5\text{ V}$, $V_{DRV} = 5\text{ V}$, $L_{OUT} = 250\text{ nH}$, $T_A = 25^\circ\text{C}$, and natural convection cooling, unless otherwise specified.)

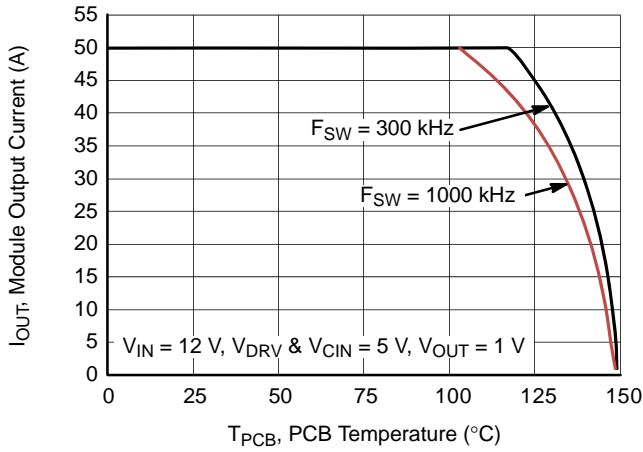


Figure 5. Safe Operating Area for 12 V_{IN}

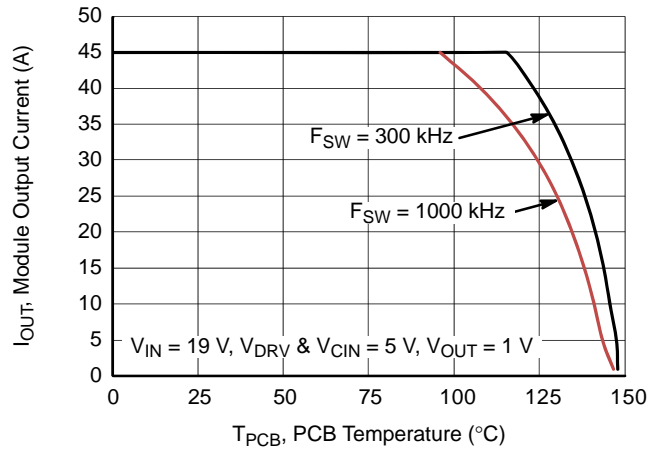


Figure 6. Safe Operating Area for 19 V_{IN}

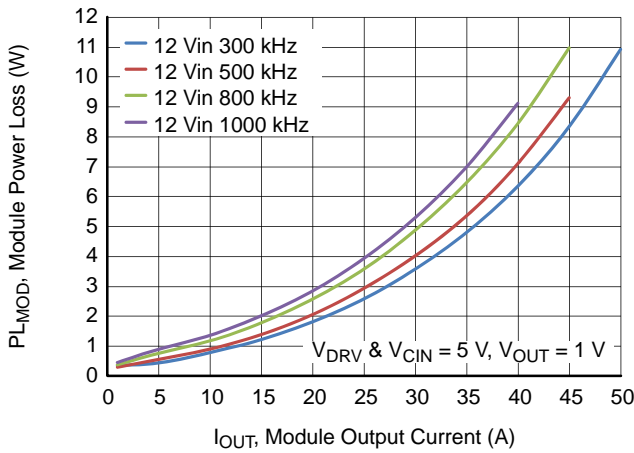


Figure 7. Power Loss vs. Output Current for 12 V_{IN}

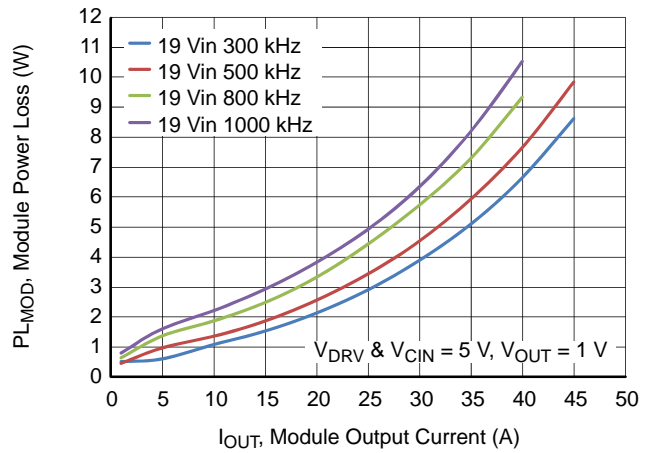


Figure 8. Power Loss vs. Output Current for 19 V_{IN}

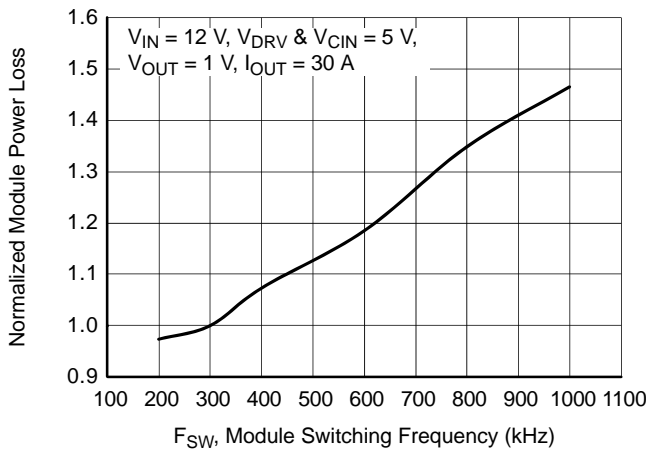


Figure 9. Power Loss vs. Switching Frequency

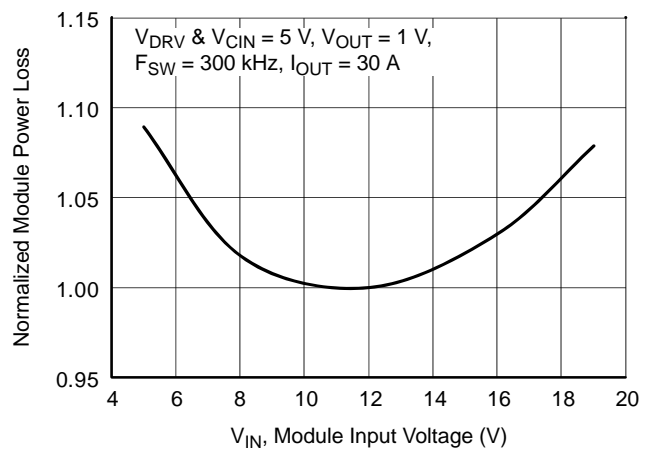


Figure 10. Power Loss vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: $V_{IN} = 12\text{ V}$ or 19 V , $V_{OUT} = 1\text{ V}$, $V_{CIN} = 5\text{ V}$, $V_{DRV} = 5\text{ V}$, $L_{OUT} = 250\text{ nH}$, $T_A = 25^\circ\text{C}$, and natural convection cooling, unless otherwise specified.)

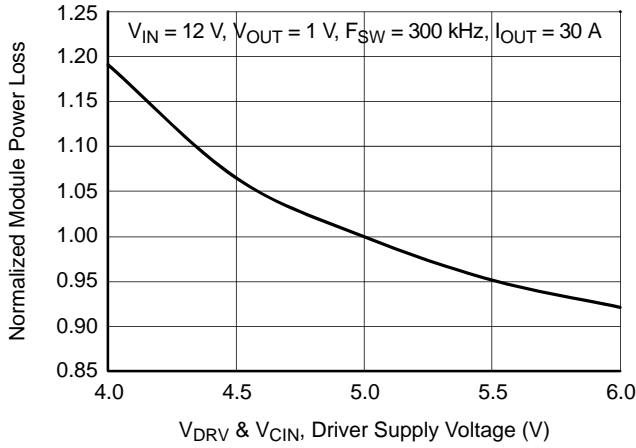


Figure 11. Power Loss vs. Driver Supply Voltage

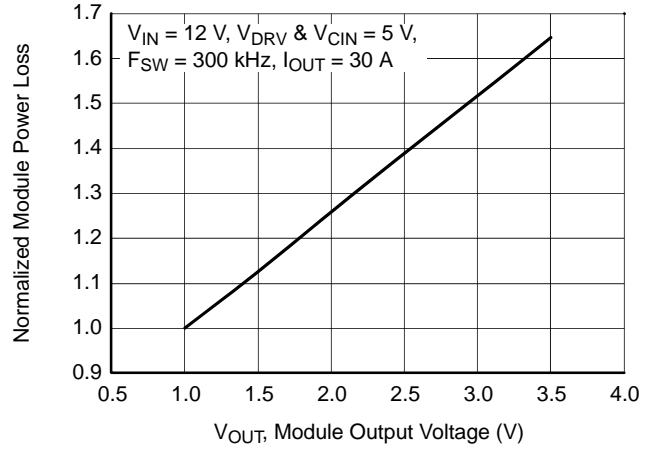


Figure 12. Power Loss vs. Output Voltage

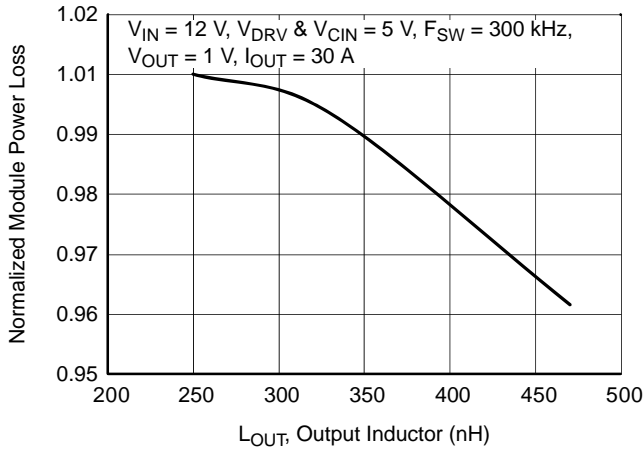


Figure 13. Power Loss vs. Output Inductor

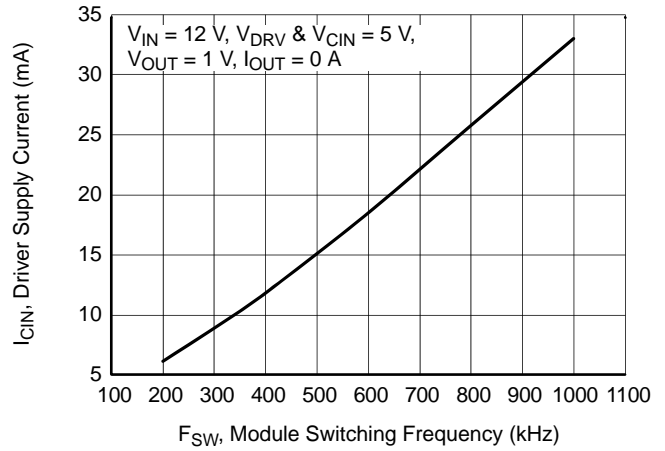


Figure 14. Driver Supply Current vs. Switching Frequency

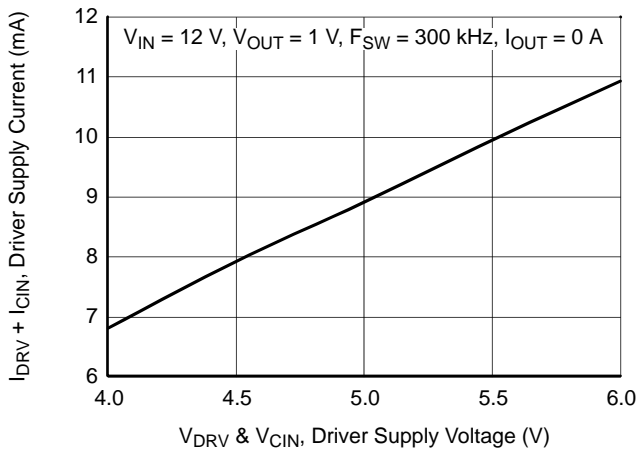


Figure 15. Driver Supply Current vs. Driver Supply Voltage

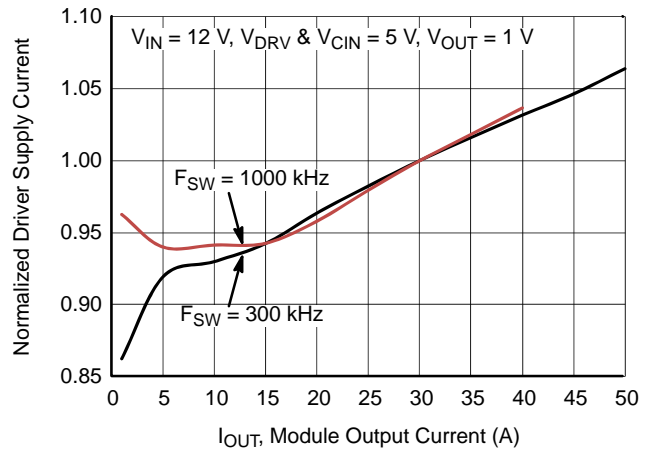


Figure 16. Driver Supply Current vs. Output Current

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: $V_{CIN} = 5\text{ V}$, $V_{DRV} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, and natural convection cooling, unless otherwise specified.)

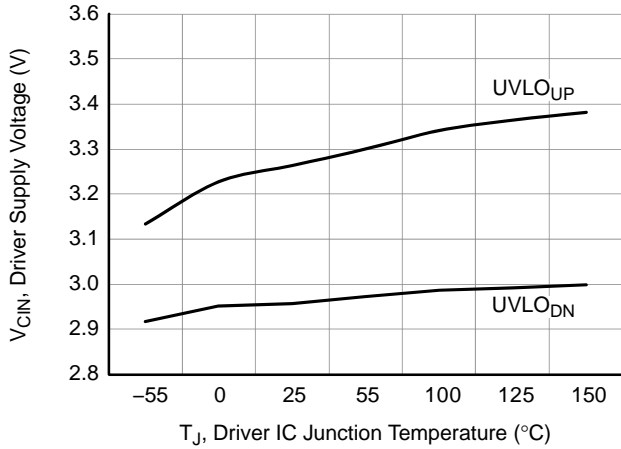


Figure 17. UVLO Threshold vs. Temperature

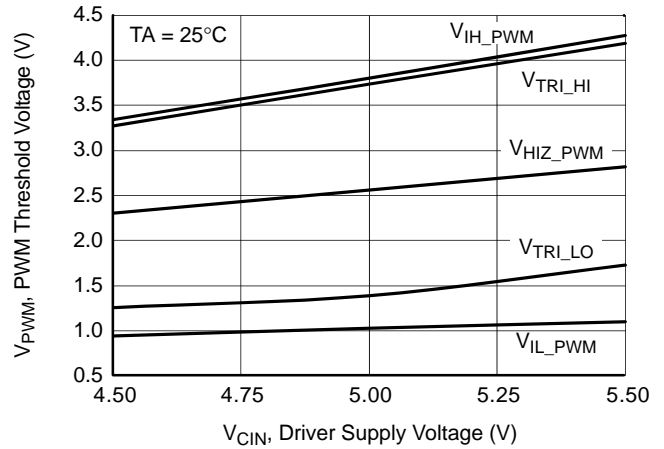


Figure 18. PWM Threshold vs. Driver Supply Voltage

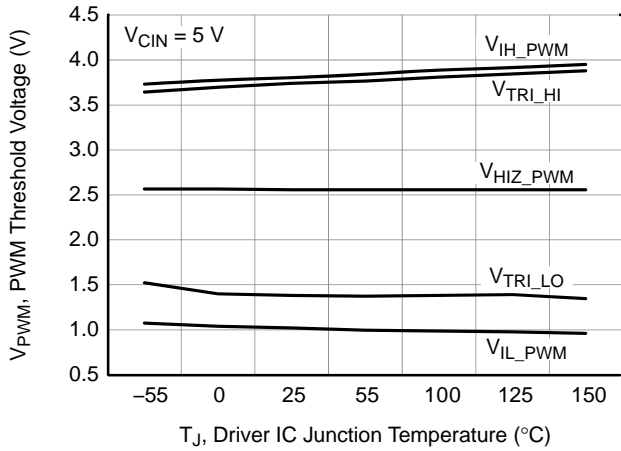


Figure 19. PWM Threshold vs. Temperature

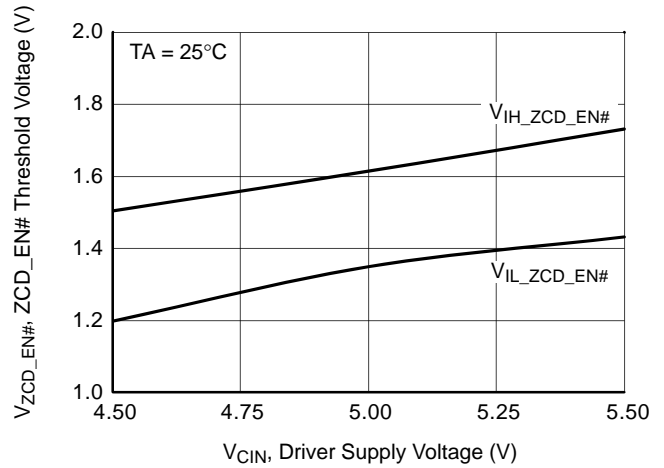


Figure 20. ZCD_EN# Threshold vs. Driver Supply Voltage

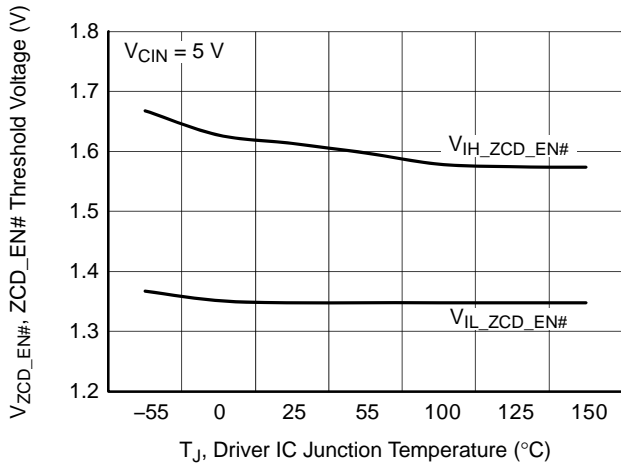


Figure 21. ZCD_EN# Threshold vs. Temperature

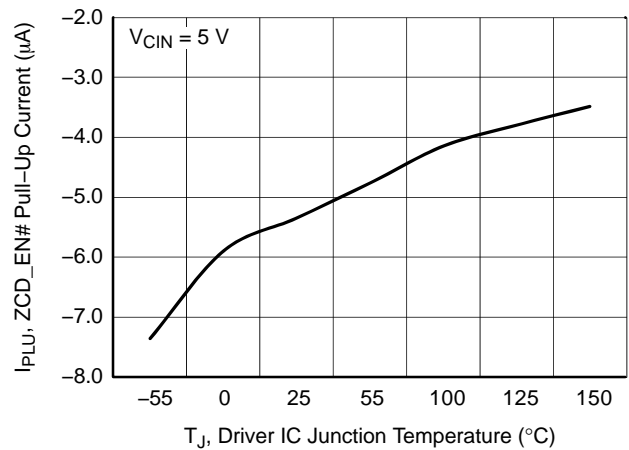


Figure 22. ZCD_EN# Pull-Up Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: $V_{CIN} = 5\text{ V}$, $V_{DRV} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, and natural convection cooling, unless otherwise specified.)

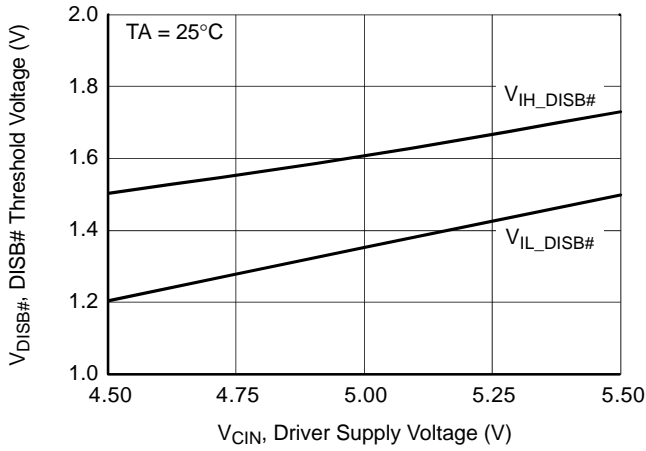


Figure 23. DISB# Threshold vs. Driver Supply Voltage

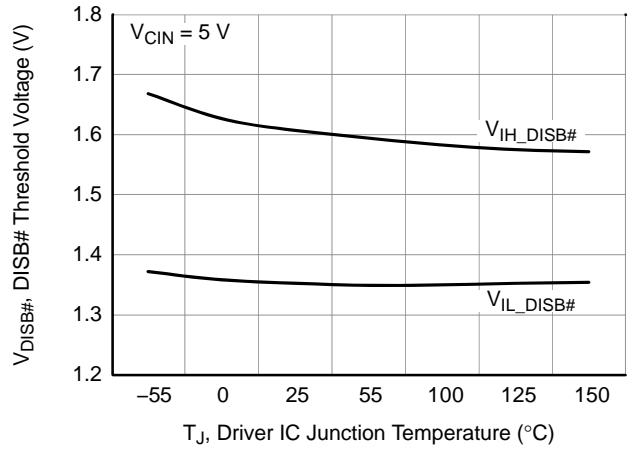


Figure 24. DISB# Threshold vs. Temperature

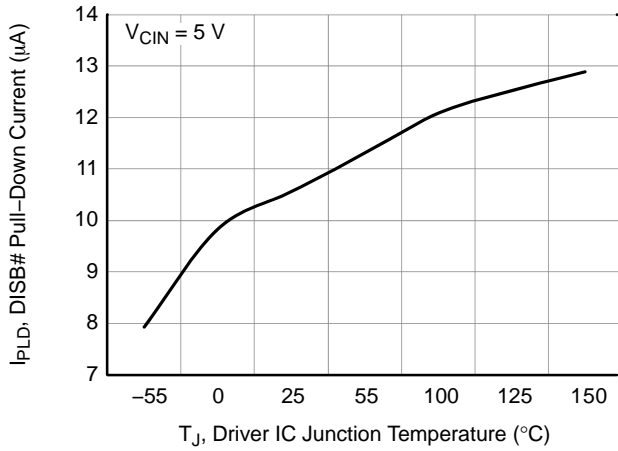


Figure 25. DISB# Pull-Down Current vs. Temperature

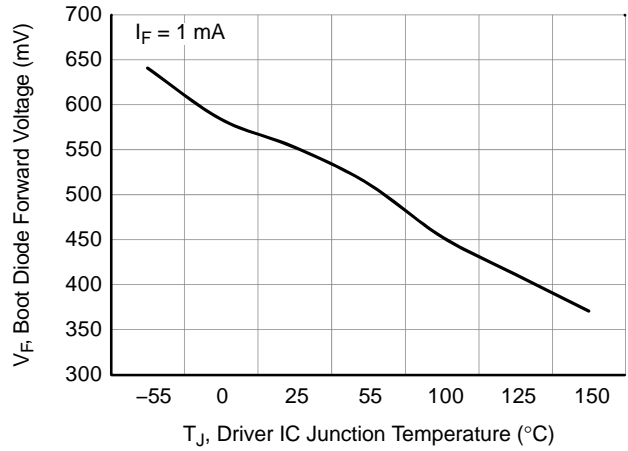


Figure 26. Boot Diode Forward Voltage vs. Temperature

FUNCTIONAL DESCRIPTION

The FDMF3030 is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 1 MHz.

VCIN and Disable (DISB#)

The VCIN pin is monitored by an Under-Voltage Lockout (UVLO) circuit. When VCIN rises above ~3.3 V, the driver is enabled. When VCIN falls below ~2.95 V, the driver is disabled (GH, GL = 0). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < VIL_DISB), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > VIH_DISB).

Table 1. UVLO AND DISABLE LOGIC

UVLO	DISB#	Driver State
0	X	Disabled (GH, GL=0)
1	0	Disabled (GH, GL=0)
1	1	Enabled (see Table 2)
1	Open	Disabled (GH, GL=0)

3. DISB# internal pull-down current source is 10 µA.

Thermal Warning Flag (THWN#)

The FDMF3030 provides a thermal warning flag (THWN#) to warn of over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN# output returns to a high-impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN# output requires a pull-up resistor, which can be connected to VCIN. THWN# does NOT disable the DrMOS module.

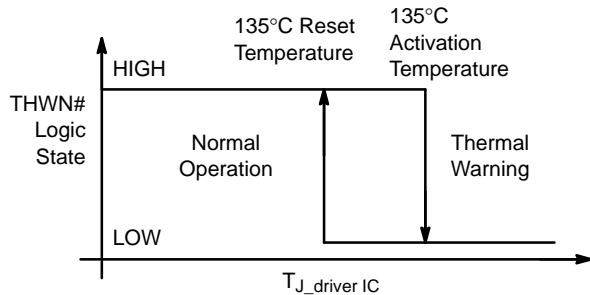


Figure 27. THWN Operation

Three-State PWM Input

The FDMF3030 incorporates a three-state 5 V PWM input gate drive design. The three-state gate drive has both logic HIGH level and LOW level, along with a three-state shutdown window. When the PWM input signal enters and remains within the three-state window for a defined hold-off time (t_{D_HOLD-OFF}), both GL and GH are pulled

LOW. This enables the gate drive to shut down both high-side and low-side MOSFETs to support features such as phase shedding, which is common on multi-phase voltage regulators.

Exiting Three-State Condition

When exiting a valid three-state condition, the FDMF3030 follows the PWM input command. If the PWM input goes from three-state to LOW, the low-side MOSFET is turned on. If the PWM input goes from three-state to HIGH, the high-side MOSFET is turned on. This is illustrated in Figure 28. The FDMF3030 design allows for short propagation delays when exiting the three-state window (see [Electrical Characteristics](#)).

Low-Side Driver

The low-side driver (GL) is designed to drive a ground-referenced, low-R_{DS(ON)}, N-channel MOSFET. The bias for GL is internally connected between the VDRV and CGND pins. When the driver is enabled, the driver’s output is 180° out of phase with the PWM input. When the driver is disabled (DISB# = 0 V), GL is held LOW.

High-Side Driver

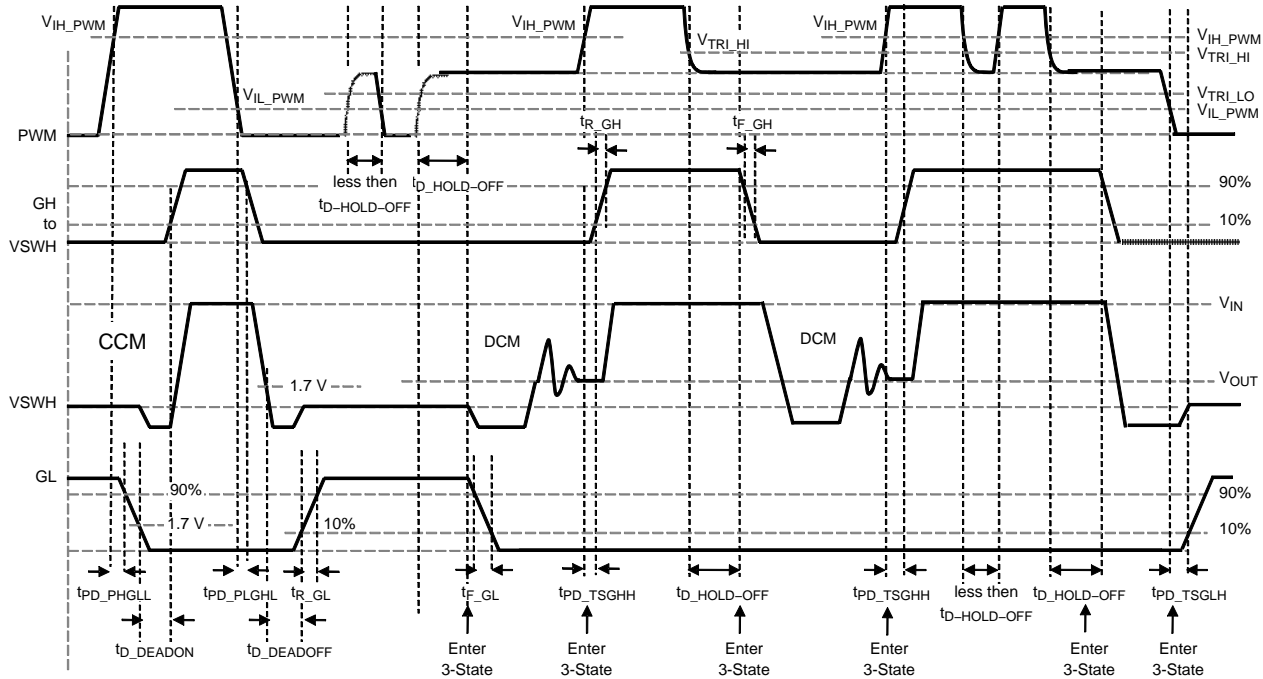
The high-side driver (GH) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, V_{SWH} is held at PGND, allowing C_{BOOT} to charge to V_{DRV} through the internal diode. When the PWM input goes HIGH, GH begins to charge the gate of the high-side MOSFET (Q1). During this transition, the charge is removed from C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, V_{SWH} rises to V_{IN}, forcing the BOOT pin to V_{IN} + V_{BOOT}, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling GH to V_{SWH}. C_{BOOT} is then recharged to V_{DRV} when V_{SWH} falls to PGND. GH output is in-phase with the PWM input. The high-side gate is held LOW when the driver is disabled or the PWM signal is held within the three-state window for longer than the three-state hold-off time, t_{D_HOLD-OFF}.

Adaptive Gate Drive Circuit

The driver IC advanced design ensures minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure they do not conduct simultaneously. Figure 28 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 begins to turn off after a propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below 1.7 V, Q1 begins to turn on after adaptive delay t_{D_DEADON}.

To prevent overlap during the HIGH-to-LOW transition (Q1 off to Q2 on), the adaptive circuitry monitors the voltage at the GH-to-PHASE pin pair. When the PWM signal goes LOW, Q1 begins to turn off after a propagation delay

(t_{PD_PLGHL}). Once the voltage across GH-to-PHASE falls below 1.7 V, Q2 begins to turn on after adaptive delay $t_{D_DEADOFF}$.



NOTES:

t_{PD_xxx} = propagation delay from external signal (PWM, ZCD_EN#, etc.) to IC generated signal. Example (t_{PD_PHGHL} – PWM going HIGH to LS Vgs (GL) going LOW)

t_{D_xxx} = delay from IC generated signal to IC generated signal. Example (t_{D_DEADON} – LS Vgs (GL) LOW to HS Vgs (GH) HIGH)

PWM

t_{PD_PHGHL} = PWM rise to LS V_{GS} fall, V_{IH_PWM} to 90% LS V_{GS} t_{PD_PLGHL} = PWM fall to HS V_{GS} fall, V_{IL_PWM} to 90% HS V_{GS}

t_{PD_PHGHH} = PWM rise to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS} (ZCD_EN# held LOW)

ZCD_EN#

t_{PD_ZLGLL} = ZCD_EN# fall to LS V_{GS} fall, $V_{IL_ZCD_EN}$ to 90% LS V_{GS}

t_{PD_ZHGLH} = ZCD_EN# rise to LS V_{GS} rise, $V_{IH_ZCD_EN}$ to 10% LS V_{GS}

Exiting 3-state

t_{PD_TSGHH} = PWM 3-state to HIGH to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS}

t_{PD_TSGLH} = PWM 3-state to LOW to LS V_{GS} rise, V_{IL_PWM} to 10% LS V_{GS}

Dead Times

t_{D_DEADON} = LS V_{GS} fall to HS V_{GS} rise, LS-comp trip value (~1.7 V GL) to 10% HS V_{GS}

$t_{D_DEADOFF}$ = VSWH fall to LS V_{GS} rise, SW-comp trip value (~1.7 V VSWH) to 10% LS V_{GS}

Figure 28. PWM and 3-State Timing Diagram

Zero Cross Detection Mode (ZCD_EN#)

The Zero Cross Detection Mode allows for higher converter efficiency when operating in light-load conditions. When ZCD_EN# is pulled LOW; the low-side MOSFET gate signal pulls LOW when internal circuitry detects positive LS MOSFET drain current, preventing discharge of the output capacitors as the filter inductor current attempts reverse current flow – known as “Diode Emulation” Mode.

When the ZCD_EN# pin is pulled HIGH, the synchronous buck converter works in Synchronous Mode, which allows for gating of the low-side MOSFET.

When the ZCD_EN# pin is pulled LOW, the low-side MOSFET is gated off automatically during positive LS MOSFET drain current. If the ZCD_EN# pin is pulled LOW by the PWM controller to support light-load Power-Saving Mode, FDMF3030 can actively turn off the low-side MOSFET when it detects the zero crossing of the inductor

FDMF3030

current. The low-side MOSFET turns on when inductor current is positive (LS MOSFET drain current is negative) and turns off when inductor current is negative (LS MOSFET drain current is positive). Zero-crossing

detection of the inductor current and low-side MOSFET on and off are automatically performed on a cycle-by-cycle basis. Normally this pin is active LOW. See Figure 29 for timing delays.

Table 2. ZCD_EN# LOGIC

DISB#	PWM	ZCD_EN#	GH	GL
0	X	X	0	0
1	3-State	X	0	0
1	0	0	0	0 ($I_L < 0$), 1 ($I_L > 0$) (Note 4)
1	1	0	1	0
1	0	1	0	1
1	1	1	1	0

4. GL = 0, when $I_L < 0$ (Inductor current is negative and flowing in to the DrMOS VSWH node). GL = 1 when $I_L > 0$ (Inductor current is positive and flowing out of the DrMOS VSWH node).

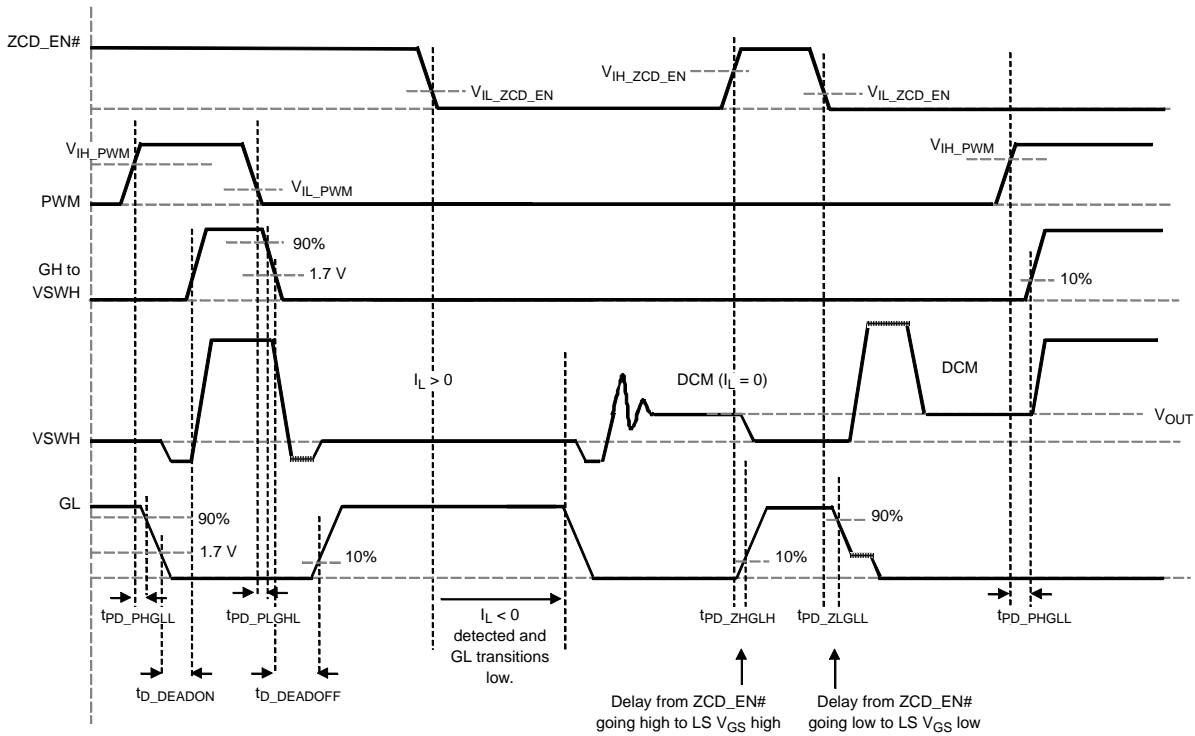


Figure 29. ZCD_EN# Timing Diagram

APPLICATION INFORMATION

Supply Capacitor Selection

For the supply inputs (V_{CIN}), a local ceramic bypass capacitor is recommended to reduce noise and to supply the peak current. Use at least a 1 μ F X7R or X5R capacitor. Keep this capacitor close to the VCIN pin and connect it to the GND plane with vias.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 30. A bootstrap capacitance of 100 nF X7R or X5R capacitor is usually adequate. A series bootstrap resistor may be needed for specific applications to improve switching noise immunity. The boot resistor may be required when operating above 15 V_{IN} and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SHW} overshoot. R_{BOOT} values from 0.5 Ω to 3.0 Ω are typically effective in reducing V_{SWH} overshoot.

VCIN Filter

The VDRV pin provides power to the gate drive of the high-side and low-side power MOSFET. In most cases, it can be connected directly to VCIN, the pin that provides

power to the logic section of the driver. For additional noise immunity, an RC filter can be inserted between the VDRV and VCIN pins. Recommended values would be 10 Ω and 1 μ F.

Power Loss and Efficiency

Measurement and Calculation

Refer to Figure 30 for power loss testing method. Power loss calculations are:

$$P_{IN} = (V_{IN} \times I_{IN}) + (V_{5V} \times I_{5V}) \text{ (W)} \tag{eq. 1}$$

$$P_{SW} = V_{SW} \times I_{OUT} \text{ (W)} \tag{eq. 2}$$

$$P_{OUT} = V_{OUT} \times I_{OUT} \text{ (W)} \tag{eq. 3}$$

$$P_{LOSS_MODULE} = P_{IN} - P_{SW} \text{ (W)} \tag{eq. 4}$$

$$P_{LOSS_BOARD} = P_{IN} - P_{OUT} \text{ (W)} \tag{eq. 5}$$

$$EFFI_{MODULE} = 100 \times P_{SW} / P_{IN} \text{ (\%)} \tag{eq. 6}$$

$$EFFI_{BOARD} = 100 \times P_{OUT} / P_{IN} \text{ (\%)} \tag{eq. 7}$$

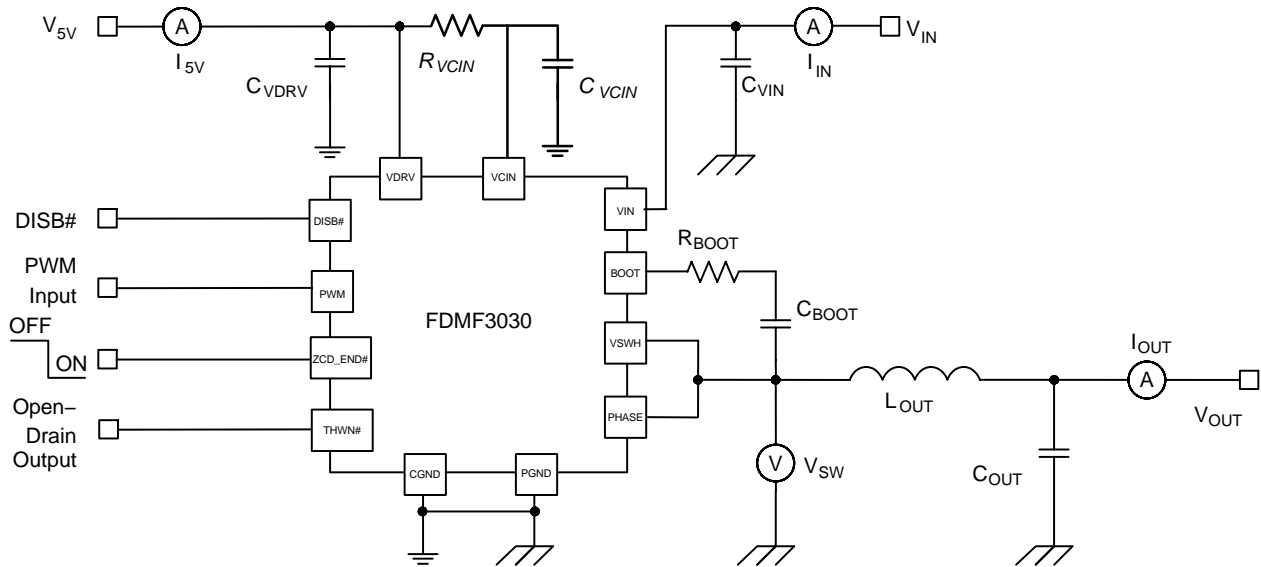


Figure 30. Circuit Diagram and Power Loss Measurement

PCB LAYOUT GUIDELINES

Figure 31 and Figure 32 provide an example of a proper layout for the FDMF3030 and critical components. All of the high-current paths; such as VIN, VSWH, VOUT, and GND copper; should be short and wide for low inductance and resistance. This aids in achieving a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Recommendations for PCB Designers

Input ceramic bypass capacitors must be placed close to the VIN and PGND pins. This reduces the high-current power loop inductance and the input current ripple induced by power MOSFET switching operation.

The V_{SWH} copper trace serves two purposes. In addition to being the high-frequency current path from the DrMOS package to the output inductor, it serves as a heat sink for the low-side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low-impedance path for the high-frequency, high-current flow between the DrMOS and inductor. The short and wide trace minimizes electrical losses as well as the DrMOS temperature rise. The V_{SWH} node is a high-voltage and high-frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace acts as a heat sink for the lower MOSFET, balance using the largest area possible to improve DrMOS cooling while maintaining acceptable noise emission.

An output inductor should be located close to the FDMF3030 to minimize the power loss due to the V_{SWH} copper trace. Care should also be taken so the inductor dissipation does not heat the DrMOS.

POWERTRENCH MOSFETs are used in the output stage and minimize ringing due to fast switching. In most cases, no VSWH snubber is required. If a snubber is used, it should be placed close to the VSWH and PGND pins. The selected resistor and capacitor need to be the proper size for power dissipation.

VCIN, VDRV, and BOOT capacitors should be placed as close as possible to the VCIN-to-CGND, VDRV-to-CGND, and BOOT-to-PHASE pin pairs to ensure clean and stable power. Routing width and length should be considered as well.

Include a trace from the PHASE pin to the VSWH pin to improve noise margin. Keep this trace as short as possible.

The layout should include the option to insert a small-value series boot resistor between the boot capacitor and BOOT pin. The boot-loop size, including R_{BOOT} and

C_{BOOT}, should be as small as possible. The boot resistor may be required when operating above 15 V_{IN} and is effective at controlling the high-side MOSFET turn-on slew rate and V_{SWH} overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative V_{SWH} ringing. Inserting a boot resistance lowers the DrMOS efficiency. Efficiency versus noise trade-offs must be considered. R_{BOOT} values from 0.5 Ω to 3.0 Ω are typically effective in reducing V_{SWH} overshoot.

The VIN and PGND pins handle large current transients with frequency components greater than 100 MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is discouraged since this adds inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SWH} ringing.

GND pad and PGND pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between CGND and PGND. This could lead to faulty operation of the gate driver and MOSFETs and should be avoided.

Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add an additional BOOT to the PGND capacitor. This may lead to excess current flow through the BOOT diode.

The ZCD_EN# and DISB# pins have weak internal pull-up and pull-down current sources, respectively. These pins should not have any noise filter capacitors. Do not float these pins unless absolutely necessary.

Use multiple vias on the VIN and VOUT copper areas to interconnect top, inner, and bottom layers to distribute current flow and heat conduction. Do not put many vias on the VSWH copper to avoid extra parasitic inductance and noise on the switching waveform. As long as efficiency and thermal performance are acceptable, place only one VSWH copper on the top layer and use no vias on the VSWH copper to minimize switch node parasitic noise. Vias should be relatively large and of reasonably low inductance. Critical high-frequency components, such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors; should be located as close to the respective DrMOS module pins as possible on the top layer of the PCB. If this is not feasible, they can be connected from the backside through a network of low-inductance vias.

PCB LAYOUT GUIDELINES (Continued)

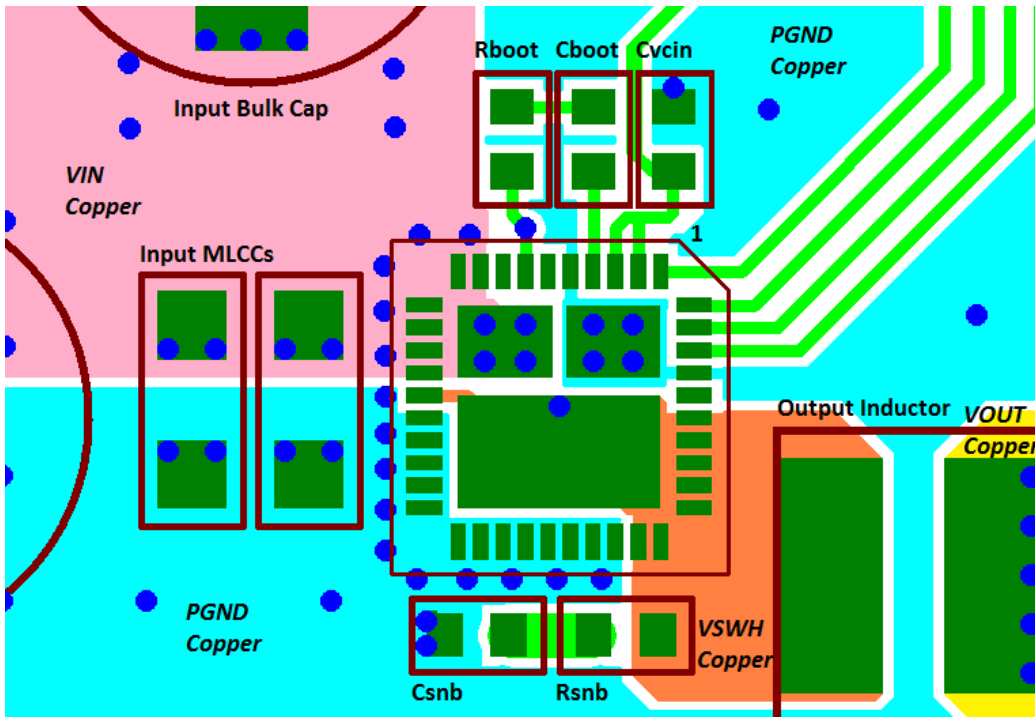


Figure 31. PCB Layout Example (Top View)

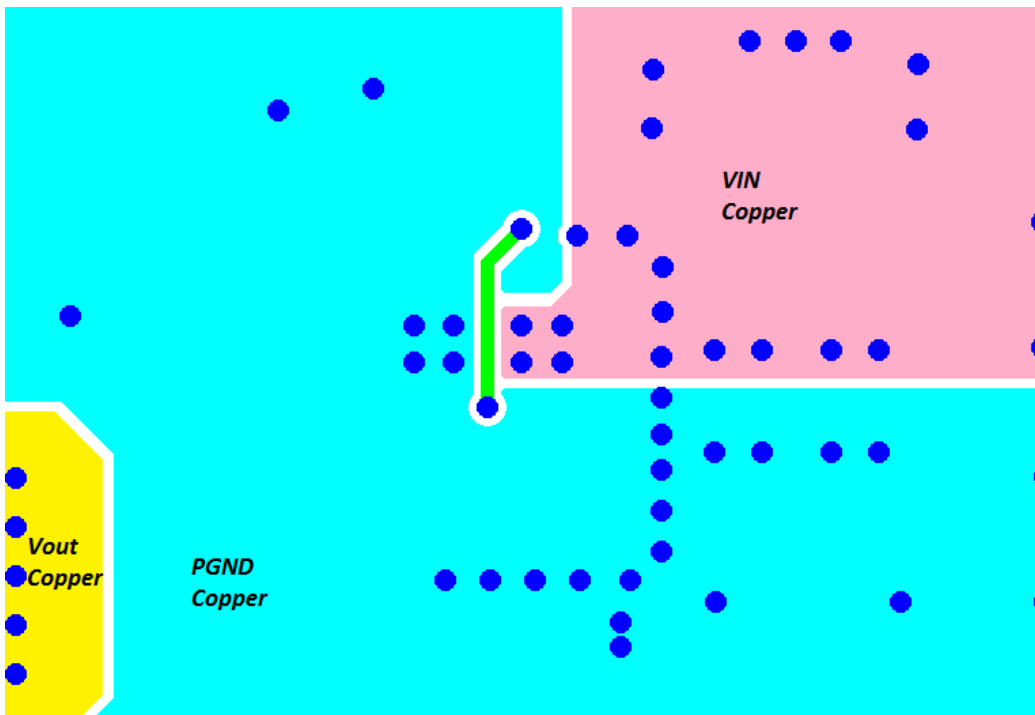


Figure 32. PCB Layout Example (Bottom View)

FDMF3030

ORDERING INFORMATION

Part Number	Top Mark	Current Rating	Package Type	Shipping†
FDMF3030	FDMF3030	50 A	40-Lead, Clipbond PQFN DrMOS, 6.0 mm x 6.0 mm Package (Pb-Free, Halide Free)	3000 / Tape & Reel

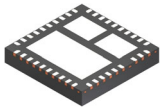
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

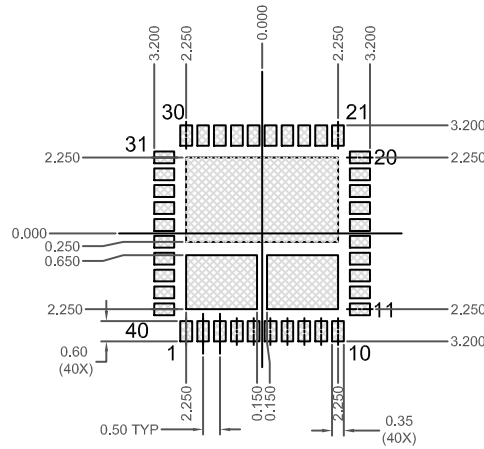
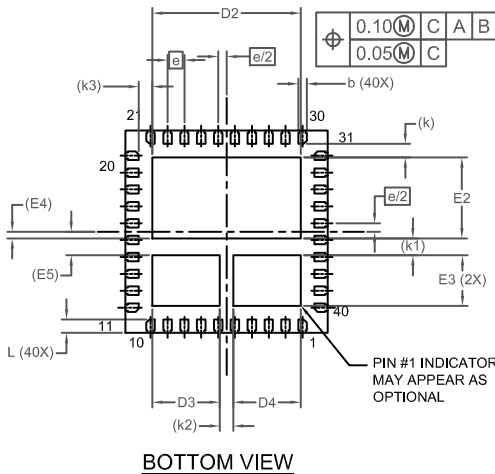
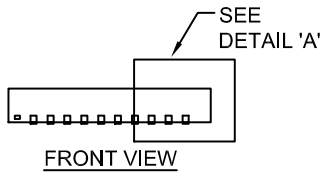
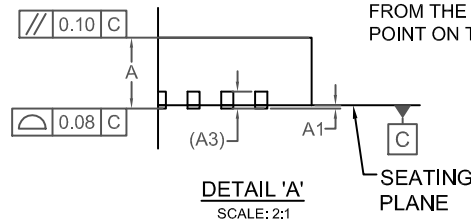
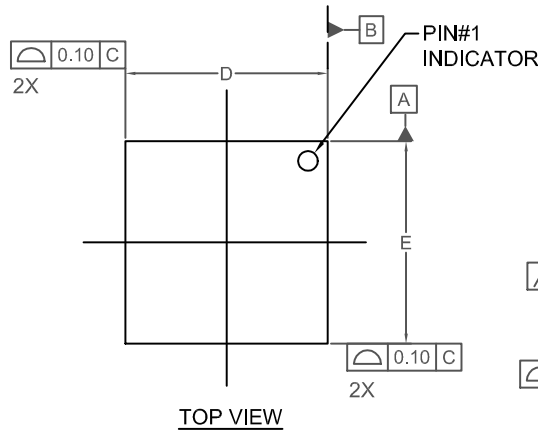
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PQFN40 6X6, 0.5P CASE 483AN ISSUE A

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5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.25 REF		
b	0.20	0.25	0.30
D	5.90	6.00	6.10
D2	4.30	4.40	4.50
D3	1.90	2.00	2.10
D4	1.90	2.00	2.10
E	5.90	6.00	6.10
E2	2.30	2.40	2.50
E3	1.40	1.50	1.60
E4	0.20 REF		
E5	0.70 REF		
e	0.50 BSC		
e/2	0.25 BSC		
k	0.40 REF		
k1	0.50 REF		
k2	0.40 REF		
k3	0.40 REF		
L	0.30	0.40	0.50

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