



**THE DATASHEET OF  
CLVTH16543MDLREP**



## FEATURES

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree <sup>(1)</sup>
- Member of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Supports Unregulated Battery Operation Down to 2.7 V
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DGG OR DL PACKAGE  
(TOP VIEW)

$\overline{1OEAB}$	1	56	$\overline{1OEBA}$
$\overline{1LEAB}$	2	55	$\overline{1LEBA}$
$\overline{1CEAB}$	3	54	$\overline{1CEBA}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
$V_{CC}$	7	50	$V_{CC}$
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
$V_{CC}$	22	35	$V_{CC}$
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2CEAB}$	26	31	$\overline{2CEBA}$
$\overline{2LEAB}$	27	30	$\overline{2LEBA}$
$\overline{2OEAB}$	28	29	$\overline{2OEBA}$

## DESCRIPTION/ORDERING INFORMATION

The SN74LVTH16543 is a 16-bit registered transceiver designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. This device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN74LVTH16543-EP

## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVER

### 3-STATE OUTPUTS

SCBS785B–NOVEMBER 2003–REVISED JUNE 2006

#### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The A-to-B enable ( $\overline{CEAB}$ ) input must be low to enter data from A or to output data from B. If  $\overline{CEAB}$  is low and  $\overline{LEAB}$  is low, the A-to-B latches are transparent; a subsequent low-to-high transition of  $\overline{LEAB}$  puts the A latches in the storage mode. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$  inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

#### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	CLVTH16543IDGGREP	LH16543EP
–55°C to 125°C	SSOP – DL	Tape and reel	CLVTH16543MDLREP	LH16543MEP

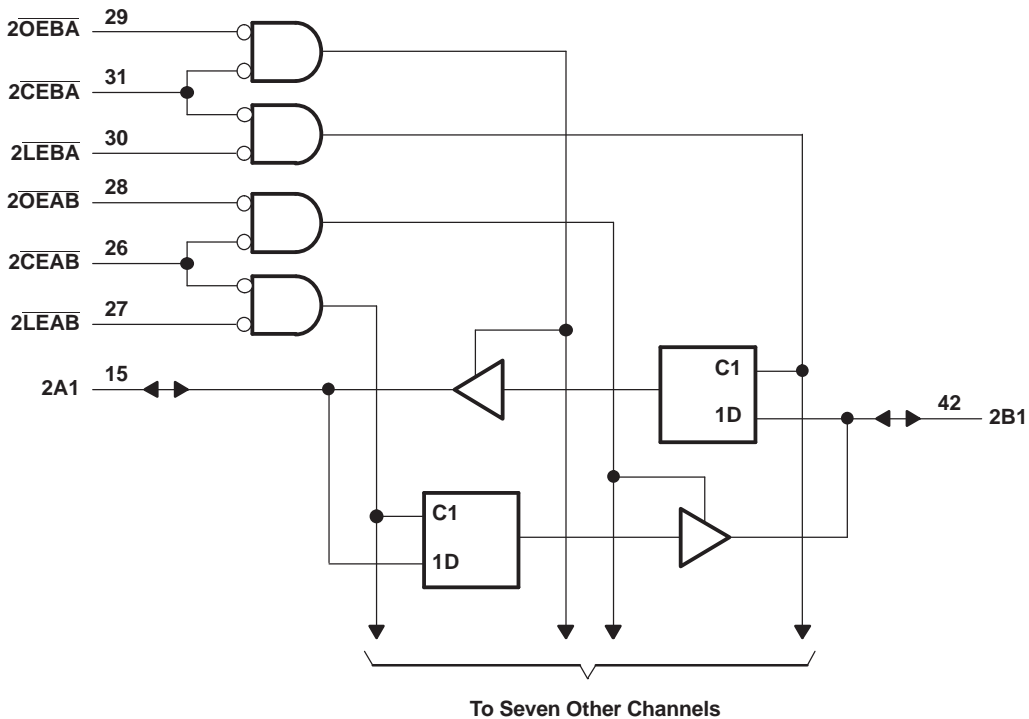
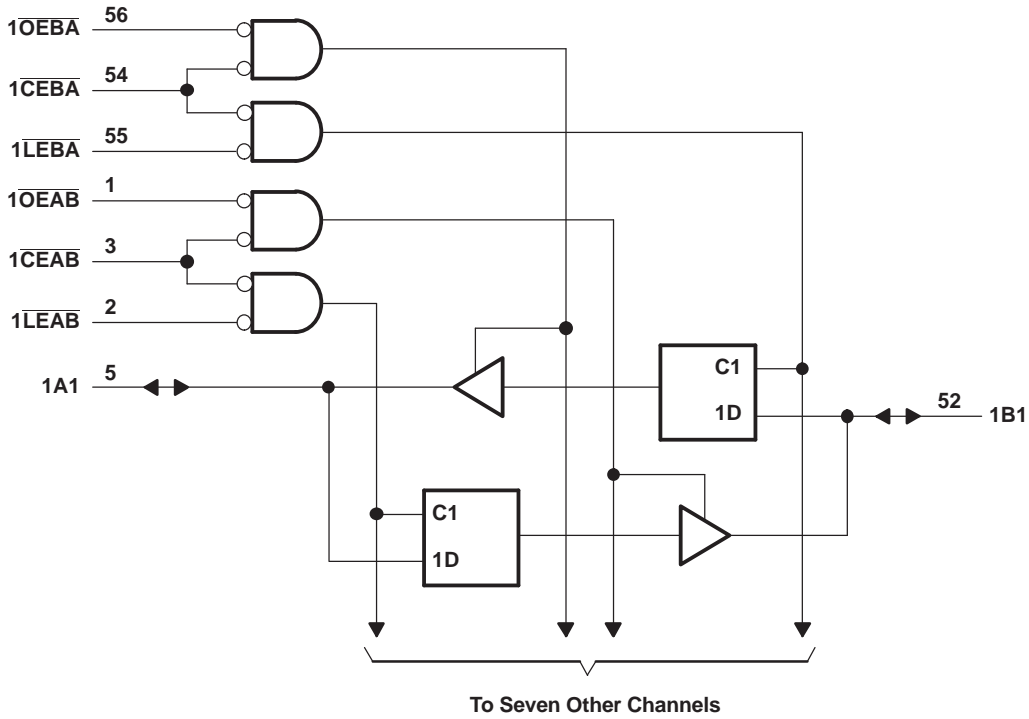
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE<sup>(1)</sup> (each 8-bit section)

INPUTS				A	OUTPUT B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$			
H	X	X	X	X	Z
X	X	H	X	X	Z
L	H	L	X	X	$B_0^{(2)}$
L	L	L	L	L	L
L	L	L	H	H	H

- (1) A-to-B data flow is shown; B-to-A flow control is the same, except that it uses  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .
- (2) Output level before the indicated steady-state input conditions were established

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# SN74LVTH16543-EP

## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVER

### 3-STATE OUTPUTS

SCBS785B–NOVEMBER 2003–REVISED JUNE 2006

#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high state <sup>(2)</sup>	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	Current into any output in the low state		128	mA
I <sub>O</sub>	Current into any output in the high state <sup>(3)</sup>		64	mA
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	–50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package	81	°C/W
		DL package	73.5	
T <sub>stg</sub>	Storage temperature range <sup>(5)</sup>	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and V<sub>O</sub> > V<sub>CC</sub>.
- (4) The package thermal impedance is calculated in accordance with JESD 51.
- (5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

#### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage		5.5	V
I <sub>OH</sub>	High-level output current		–32	mA
I <sub>OL</sub>	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200	μs/V
T <sub>A</sub>	Operating free-air temperature	I temp	–40	85
		M temp	–55	125

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 2.7\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$			V
		$V_{CC} = 2.7\text{ V}$ ,	$I_{OH} = -8\text{ mA}$	2.4			
		$V_{CC} = 3\text{ V}$ ,	$I_{OH} = -32\text{ mA}$	2			
$V_{OL}$		$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
			$I_{OL} = 24\text{ mA}$			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4		
		$I_{OL} = 32\text{ mA}$			0.5		
		$I_{OL} = 64\text{ mA (I temp)}$			0.55		
$I_I$	Control inputs	$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}\text{ or GND}$			$\pm 1$	$\mu\text{A}$
			$V_{CC} = 0\text{ or }3.6\text{ V}$ ,	$V_I = 5.5\text{ V}$			
	A or B port <sup>(2)</sup>	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V (I temp)}$			20	
			$V_I = 5.5\text{ V (M temp)}$			100	
			$V_I = V_{CC}$			1	
		$V_I = 0$			-5		
$I_{off}$		$V_{CC} = 0$	$V_I\text{ or }V_O = 0\text{ to }4.5\text{ V (I temp)}$			$\pm 100$	$\mu\text{A}$
			$V_I\text{ or }V_O = 0\text{ to }4.5\text{ V (M temp)}$			$\pm 550$	
$I_{I(\text{hold})}$	A or B port	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$		75		$\mu\text{A}$
			$V_I = 2\text{ V}$		-75		
		$V_{CC} = 3.6\text{ V}$ , <sup>(3)</sup>	$V_I = 0\text{ to }3.6\text{ V}$			$\pm 500$	
$I_{OZPU}$		$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $\overline{OE} = \text{don't care}$				$\pm 100$	$\mu\text{A}$
$I_{OZPD}$		$V_{CC} = 1.5\text{ to }0\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $\overline{OE} = \text{don't care}$				$\pm 100$	$\mu\text{A}$
$I_{CC}$ <sup>(4)</sup>		$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high			0.19	mA
			Outputs low			5	
			Outputs disabled			0.19	
$\Delta I_{CC}$		$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$				0.2	mA
$C_i$		$V_I = 3\text{ V or }0$			4		pF
$C_{io}$		$V_O = 3\text{ V or }0$			10		pF

 (1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

 (2) Unused pins at  $V_{CC}\text{ or GND}$ 

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}\text{ or GND}$ .

# SN74LVTH16543-EP

## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVER

### 3-STATE OUTPUTS

SCBS785B–NOVEMBER 2003–REVISED JUNE 2006

### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

			M TEMP				I TEMP				UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		3.3		3.3		3.3		3.3		ns
$t_{su}$	Setup time	A or B before $\overline{LEAB}\uparrow$ OR $\overline{LEBA}\uparrow$	Data high	0.7	0.9	0.5	0.5			ns	
			Data low	1.2	1.9	0.8	1.3				
	A or B before $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	Data high	0.5	0.8	0	0					
		Data low	1.1	1.9	0.6	1.1					
$t_h$	Hold time	A or B before $\overline{LEAB}\uparrow$ OR $\overline{LEBA}\uparrow$	Data high	1.5	1.0	1.5	0.7			ns	
			Data low	1.2	1.5	1.2	1.3				
	A or B before $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	Data high	1.7	1.1	1.7	0.9					
		Data low	1.6	1.9	1.6	1.8					

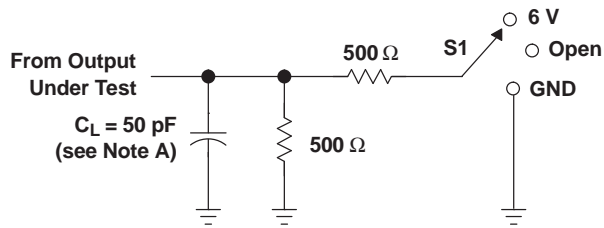
### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	M TEMP				I TEMP				UNIT	
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$			
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN		MAX
$t_{PLH}$	A or B	B or A	1.2	4.7	6.5		1.2	2.3	3.2	3.7		ns
$t_{PHL}$			1.2	5.4	6.5		1.2	2.1	3.2	3.7		
$t_{PLH}$	$\overline{LE}$	A or B	1.3	7.3	7.8		1.3	2.5	3.9	4.9		ns
$t_{PHL}$			1.3	6.9	7.8		1.3	2.3	3.9	4.9		
$t_{PZH}$	$\overline{OE}$	A or B	1.3	6.5	7.4		1.3	2.8	4.3	5.4		ns
$t_{PZL}$			1.3	6.7	7.4		1.3	2.8	4.3	5.4		
$t_{PHZ}$	$\overline{OE}$	A or B	2	5.7	7.2		2	3.5	4.7	5.2		ns
$t_{PLZ}$			2	5.1	6.9		2	3.3	4.4	4.5		
$t_{PZH}$	$\overline{CE}$	A or B	1.3	6.5	7.6		1.3	3	4.5	5.6		ns
$t_{PZL}$			1.3	6.4	7.6		1.3	3	4.5	5.6		
$t_{PHZ}$	$\overline{CE}$	A or B	2	5.3	7.4		2	3.6	4.9	5.4		ns
$t_{PLZ}$			2	5.1	6.9		2	3.5	4.7	4.9		

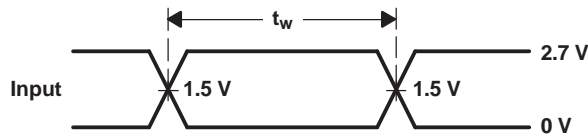
(1) All typical values are at  $V_{CC} = 3.3 V$ ,  $T_A = 25^\circ C$ .

PARAMETER MEASUREMENT INFORMATION

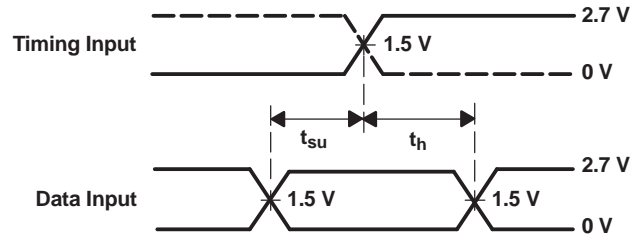


LOAD CIRCUIT

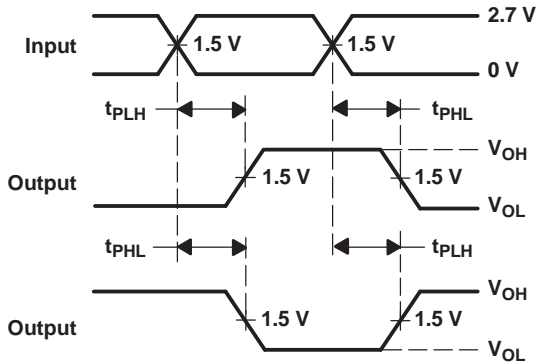
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



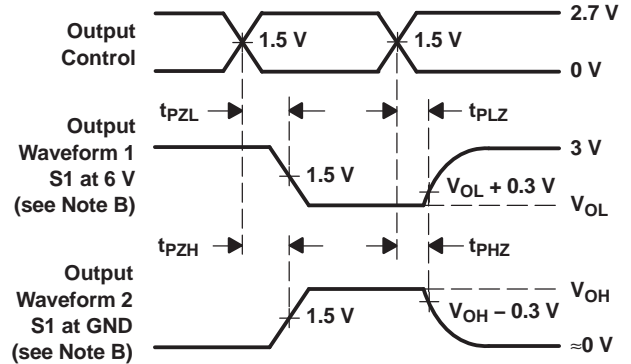
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CLVTH16543IDGGREP	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CLVTH16543MDLREP	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04715-01XE	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04715-02YE	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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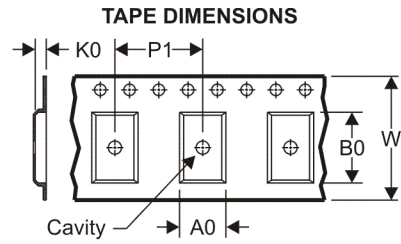
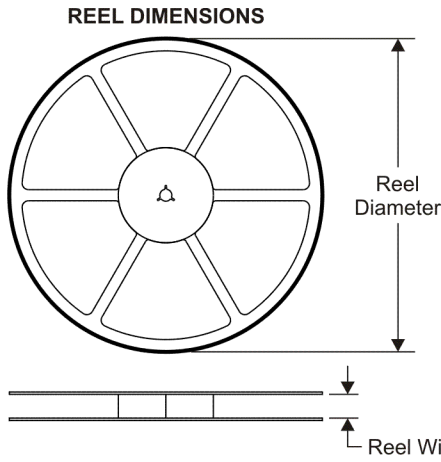
**OTHER QUALIFIED VERSIONS OF SN74LVTH16543-EP :**

- Catalog: [SN74LVTH16543](#)

NOTE: Qualified Version Definitions:

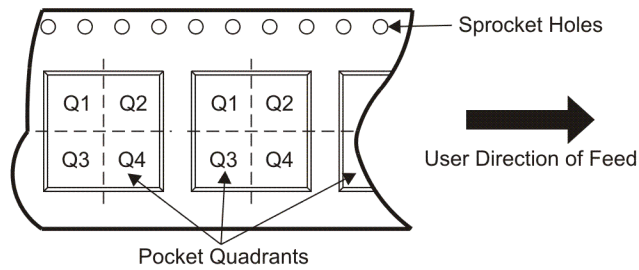
- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVTH16543IDGGREP	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CLVTH16543MDLREP	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVTH16543IDGGREP	TSSOP	DGG	56	2000	346.0	346.0	41.0
CLVTH16543MDLREP	SSOP	DL	56	1000	346.0	346.0	49.0

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

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