



THE DATASHEET OF TLE4270



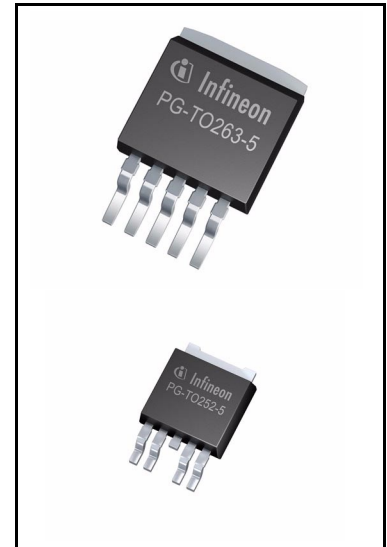
OPTIREG™ Linear TLE4270-2

5-V low drop fixed voltage regulator



Features

- Output voltage tolerance $\leq \pm 2\%$
- 650 mA output current capability
- Low-drop voltage
- Reset functionality
- Adjustable reset time
- Suitable for use in automotive electronics
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- Wide temperature range
- ESD protection: ± 2 kV HBM¹⁾
- Green Product (RoHS compliant)



Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ Linear TLE4270-2 is a 5-V low drop fixed-voltage regulator. The maximum input voltage is 42 V (65 V, ≤ 400 ms). Up to an input voltage of 26 V and for an output current up to 650 mA it regulates the output voltage within a 2% accuracy. The short circuit protection limits the output current of more than 650 mA. The device incorporates overvoltage protection and a temperature protection which turns off the device at high temperatures.

1) ESD susceptibility, Human Body Model (HBM) according to EIA/JESD 22-A114B.

OPTIREG™ Linear TLE4270-2
5-V low drop fixed voltage regulator



| Type | Package | Marking |
|-------------|----------------|----------------|
| TLE4270-2G | P-TO263-5 | 4270-2G |
| TLE4270-2D | P-TO252-5 | 4270-2D |

Table of contents

| | | |
|----------|--|-----------|
| | Features | 1 |
| | Potential applications | 1 |
| | Product validation | 1 |
| | Description | 1 |
| | Table of contents | 3 |
| 1 | Block diagram | 4 |
| 2 | Pin configuration | 5 |
| 2.1 | Pin assignment | 5 |
| 2.2 | Pin definitions and functions | 5 |
| 3 | General product characteristics | 6 |
| 3.1 | Absolute maximum ratings | 6 |
| 3.2 | Functional range | 6 |
| 3.3 | Thermal resistance | 7 |
| 4 | Functional description | 8 |
| 4.1 | Circuit description | 8 |
| 4.2 | Electrical characteristics | 8 |
| 4.3 | Typical performance graphs | 10 |
| 5 | Application information | 13 |
| 5.1 | Design notes for external components | 13 |
| 5.2 | Reset circuitry | 14 |
| 5.3 | Reset timing | 14 |
| 6 | Package information | 15 |
| 7 | Revision history | 16 |

Block diagram

1 Block diagram

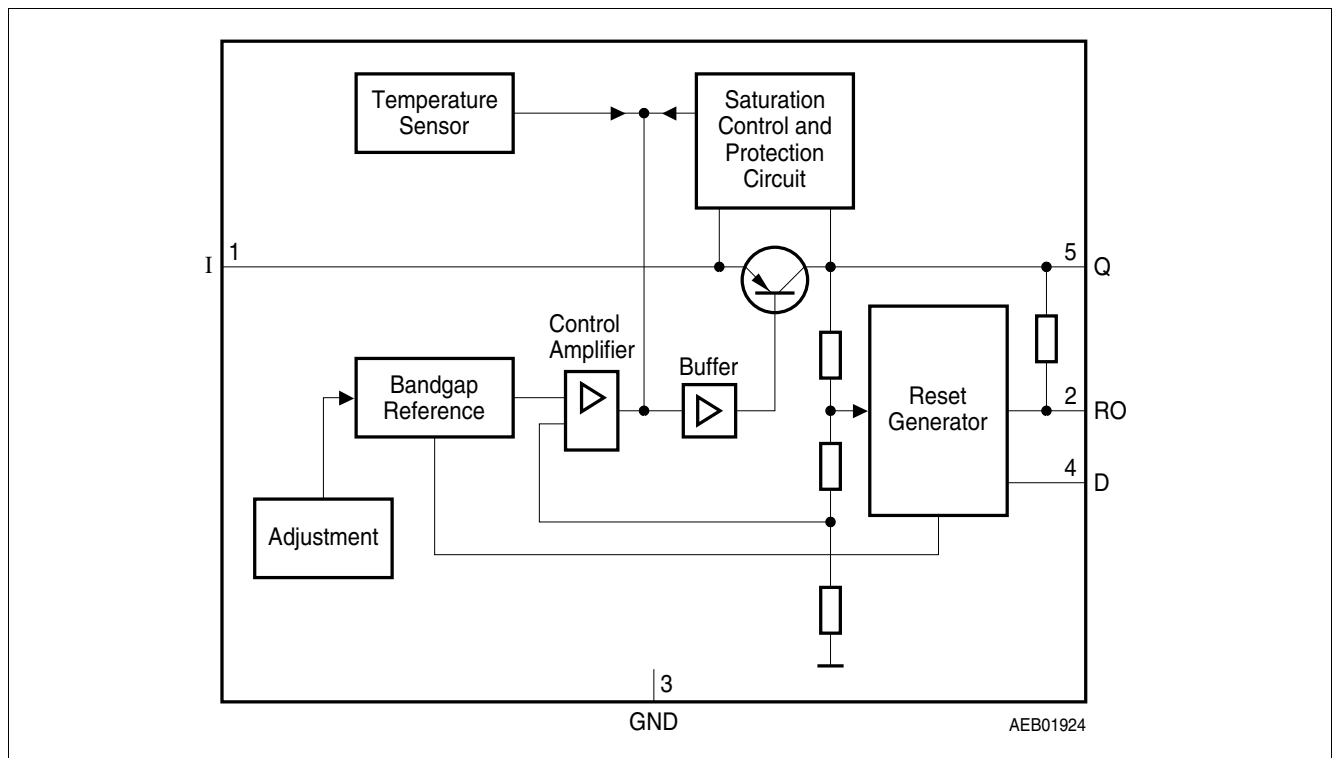


Figure 1 Block diagram

Pin configuration

2 Pin configuration

2.1 Pin assignment

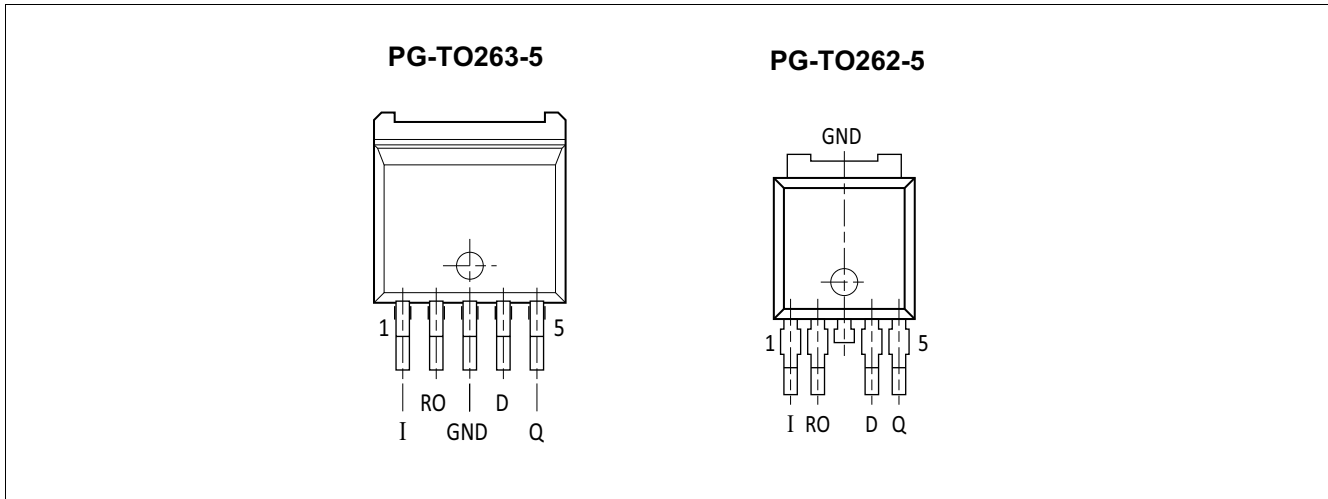


Figure 2 Pin configuration (top view)

2.2 Pin definitions and functions

| Pin | Symbol | Function |
|-----|--------|--|
| 1 | I | Input; block to ground directly at the IC with a ceramic capacitor. |
| 2 | RO | Reset output; the open collector output is connected to the 5-V output via an integrated resistor of 30 kΩ. |
| 3 | GND | Ground; internally connected to heatsink. |
| 4 | D | Reset delay; connect a capacitor to ground for delay time adjustment. |
| 5 | Q | 5-V output; block to ground with 22 μF capacitor, ESR < 3 Ω. |

General product characteristics

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings

$T_j = -40$ to 150°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------|-----------|--------|------|------|------------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Input I | | | | | | | |
| Voltage | V_I | -42 | - | 42 | V | - | P_3.1.1 |
| Voltage | V_I | - | - | 65 | V | $t \leq 400$ ms | P_3.1.2 |
| Current | I_I | - | - | - | - | Internally limited | P_3.1.3 |
| Reset output RO | | | | | | | |
| Voltage | V_{RO} | -0.3 | - | 7 | V | - | P_3.1.4 |
| Current | I_{RO} | - | - | - | - | Internally limited | P_3.1.5 |
| Reset delay D | | | | | | | |
| Voltage | V_D | -0.3 | - | 7 | V | - | P_3.1.6 |
| Current | I_D | - | - | - | - | Internally limited | P_3.1.7 |
| Output Q | | | | | | | |
| Voltage | V_Q | -1.0 | - | 16 | V | - | P_3.1.8 |
| Current | I_Q | - | - | - | - | Internally limited | P_3.1.9 |
| Ground GND | | | | | | | |
| Current | I_{GND} | -0.5 | - | - | A | - | P_3.1.10 |
| Temperatures | | | | | | | |
| Junction temperature | T_j | - | - | 150 | $^\circ\text{C}$ | - | P_3.1.11 |
| Storage temperature | T_{stg} | -50 | - | 150 | $^\circ\text{C}$ | - | P_3.1.12 |

3.2 Functional range

Table 2 Functional range

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|----------------------|--------|--------|------|------|------------------|------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Input voltage | V_I | 6 | - | 42 | V | - | P_3.2.1 |
| Junction temperature | T_j | -40 | - | 150 | $^\circ\text{C}$ | - | P_3.2.2 |

General product characteristics

3.3 Thermal resistance

Table 3 Thermal resistance

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---------------------------|------------|--------|------|------|------|------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Thermal resistance | | | | | | | |
| Junction ambient | R_{thJA} | – | – | 65 | K/W | TO263, ¹⁾ | P_3.3.1 |
| | | – | – | 79 | K/W | TO252 ¹⁾ | P_3.3.2 |
| Junction case | R_{thJC} | – | – | 3 | K/W | TO-263 Packages | P_3.3.3 |

1) Mounted on PCB, 80 × 80 × 1.5 mm³; 35 μ Cu; 5 μ Sn; footprint only; zero airflow.

Functional description

4 Functional description

4.1 Circuit description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

4.2 Electrical characteristics

Table 4 Electrical characteristics

$V_I = 13.5\text{ V}$; $T_j = -40\text{ to }125^\circ\text{C}$ (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------------|--------|------|------|------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Output voltage | V_Q | 4.90 | 5.00 | 5.10 | V | $5\text{ mA} \leq I_Q \leq 550\text{ mA}$; $6\text{ V} \leq V_I \leq 26\text{ V}$ | P_4.0.1 |
| | V_Q | 4.90 | 5.00 | 5.10 | V | $26\text{ V} \leq V_I \leq 36\text{ V}$; $I_Q \leq 300\text{ mA}$ | P_4.0.2 |
| Output current limiting | I_{Qmax} | 650 | 850 | – | mA | $V_Q = 0\text{ V}$ | P_4.0.3 |
| Current consumption $I_q = I_1 - I_Q$ | I_q | – | 1 | 1.5 | mA | $I_Q = 5\text{ mA}$ | P_4.0.4 |
| | I_q | – | 55 | 75 | mA | $I_Q = 550\text{ mA}$ | P_4.0.5 |
| | I_q | – | 70 | 90 | mA | $I_Q = 550\text{ mA}$; $V_I = 5\text{ V}$ | P_4.0.6 |
| Drop voltage | V_{DR} | – | 350 | 700 | mV | $I_Q = 550\text{ mA}^{(1)}$ | P_4.0.7 |
| Load regulation | $\Delta V_{Q,Lo}$ | – | 25 | 50 | mV | $I_Q = 5\text{ to }550\text{ mA}$; $V_I = 6\text{ V}$ | P_4.0.8 |
| Line regulation | $\Delta V_{Q,Li}$ | – | 12 | 25 | mV | $V_I = 6\text{ to }26\text{ V}$; $I_Q = 5\text{ mA}$ | P_4.0.9 |
| Power supply ripple rejection | $PSRR$ | – | 54 | – | dB | $f_r = 100\text{ Hz}$; $V_r = 0.5\text{ Vpp}$ | P_4.0.10 |
| Reset generator | | | | | | | |
| Switching threshold | V_{RT} | 4.5 | 4.65 | 4.8 | V | – | P_4.0.11 |
| Reset high voltage | V_{ROH} | 4.5 | – | – | V | – | P_4.0.12 |
| Reset low voltage | V_{ROL} | – | 60 | – | mV | $R_{int} = 30\text{ k}\Omega^{(2)}$; $1.0\text{ V} \leq V_Q \leq 4.5\text{ V}$ | P_4.0.13 |
| | V_{ROL} | – | 200 | 400 | mV | $I_R = 3\text{ mA}$, $V_Q = 4.4\text{ V}$ | P_4.0.14 |
| Reset pull-up | R_{int} | 18 | 30 | 46 | k Ω | Internally connected to Q | P_4.0.15 |

Functional description

Table 4 Electrical characteristics (cont'd)

$V_I = 13.5\text{ V}$; $T_j = -40\text{ to }125^\circ\text{C}$ (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------------|-----------|--------|------|------|---------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Charge current | $I_{D,c}$ | 8 | 14 | 25 | μA | $V_D = 1.0\text{ V}$ | P_4.0.16 |
| Upper reset timing threshold | V_{DU} | 1.4 | 1.8 | 2.3 | V | – | P_4.0.17 |
| Lower reset timing threshold | V_{DL} | 0.2 | 0.45 | 0.8 | V | $V_Q < V_{RT}$ | P_4.0.18 |
| Delay time | t_{rd} | – | 13 | – | ms | $C_D = 100\text{ nF}$ | P_4.0.19 |
| Reset reaction time | t_{rr} | – | – | 3 | μs | $C_D = 100\text{ nF}$ | P_4.0.20 |

Overvoltage protection

| | | | | | | | |
|------------------|------------|----|----|----|---|---|----------|
| Turn-off voltage | $V_{I,ov}$ | 42 | 44 | 46 | V | – | P_4.0.21 |
|------------------|------------|----|----|----|---|---|----------|

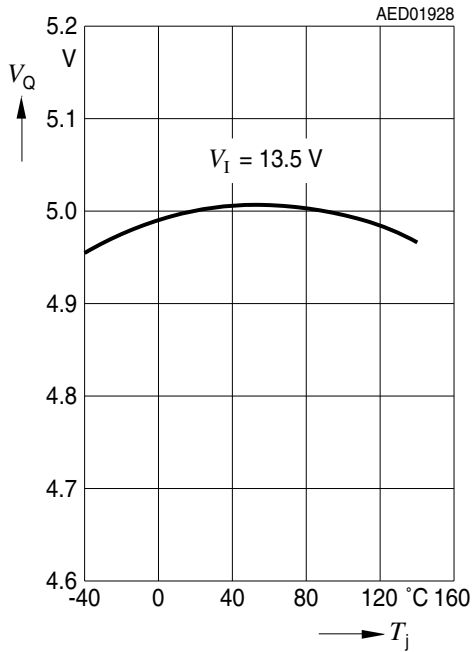
- 1) Drop voltage = $V_I - V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input).
- 2) Reset peak is always lower than 1.0 V.

Functional description

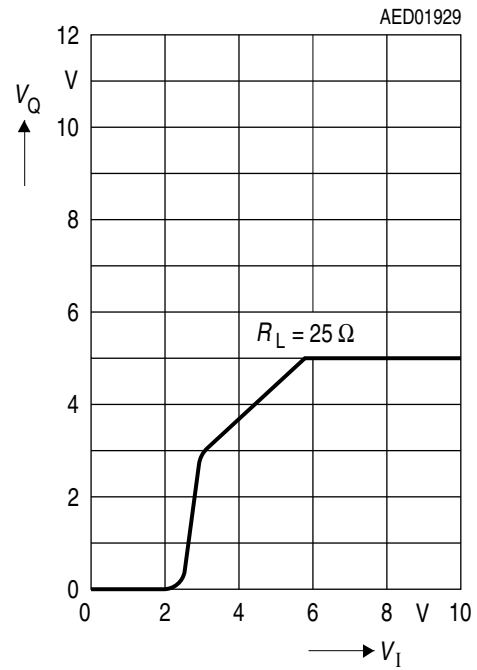
4.3 Typical performance graphs

Typical performance characteristics

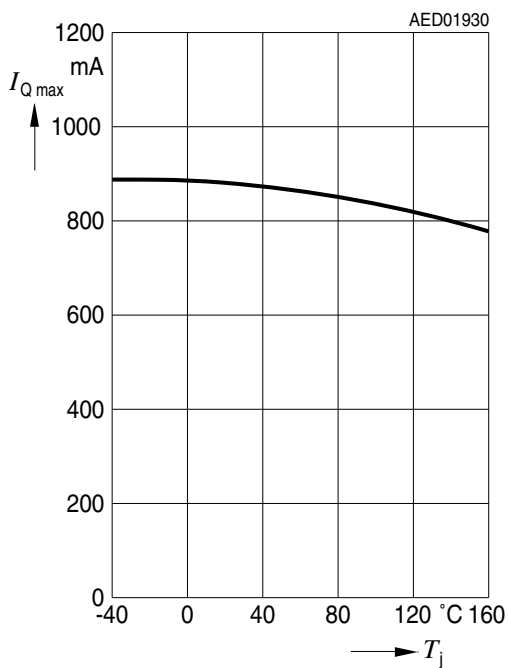
Output voltage V_Q vs. junction temperature T_j



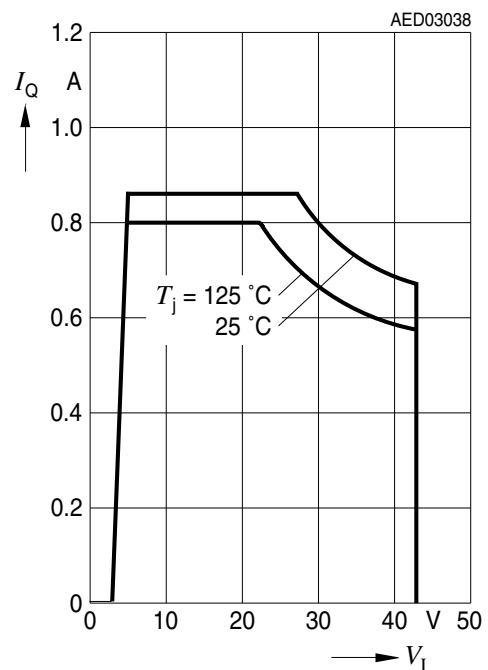
Output voltage V_Q vs. input voltage V_I



Output current I_Q vs. junction temperature T_j

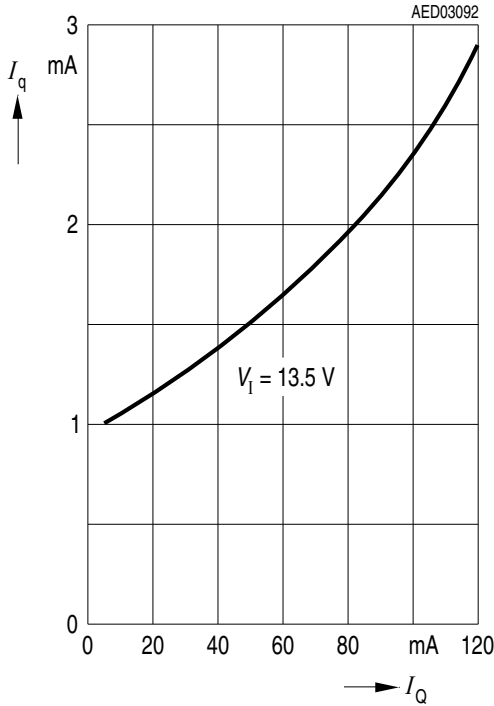


Output current I_Q vs. input voltage V_I

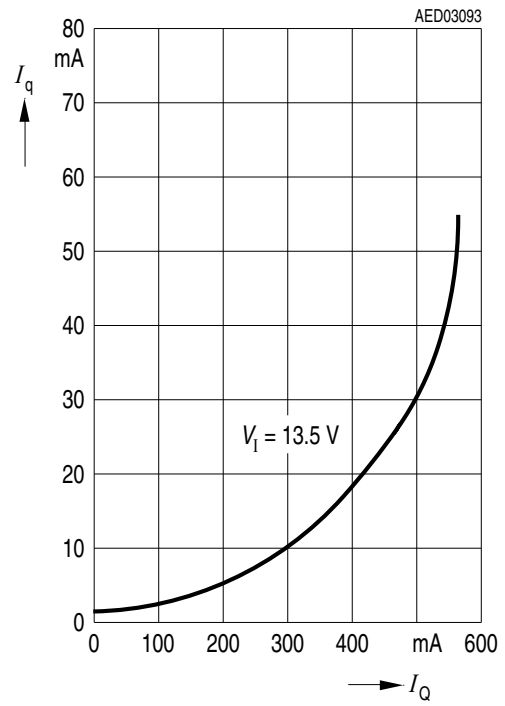


Functional description

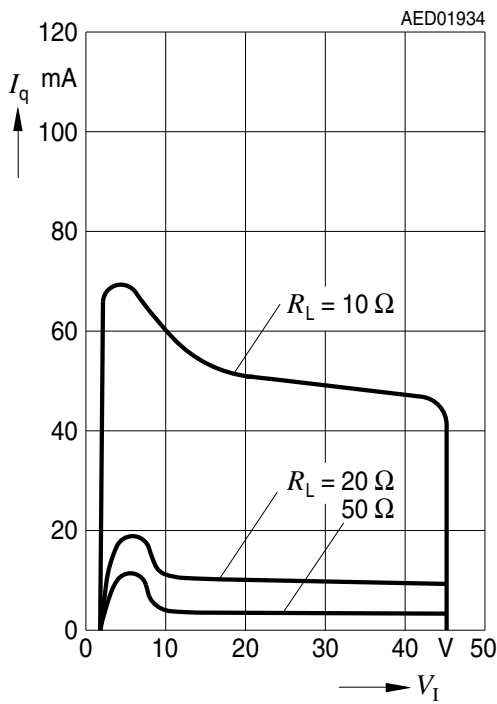
Current consumption I_q vs. output current I_Q



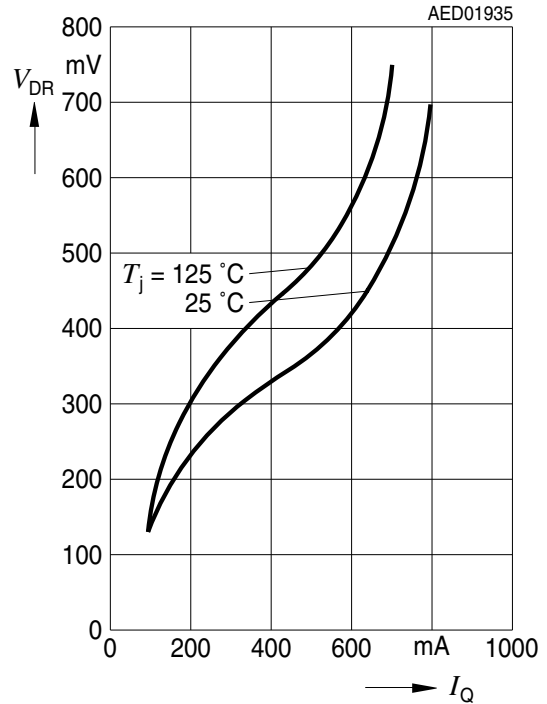
Current consumption I_q vs. output current I_Q



Current consumption I_q vs. input voltage V_1



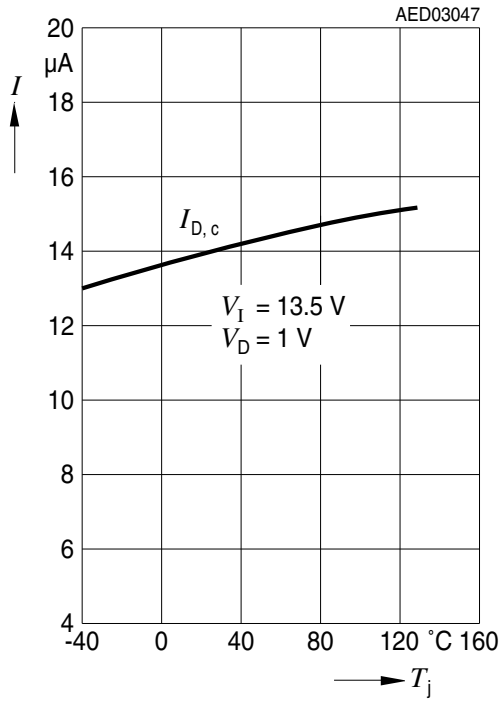
Drop voltage V_{DR} vs. output current I_Q



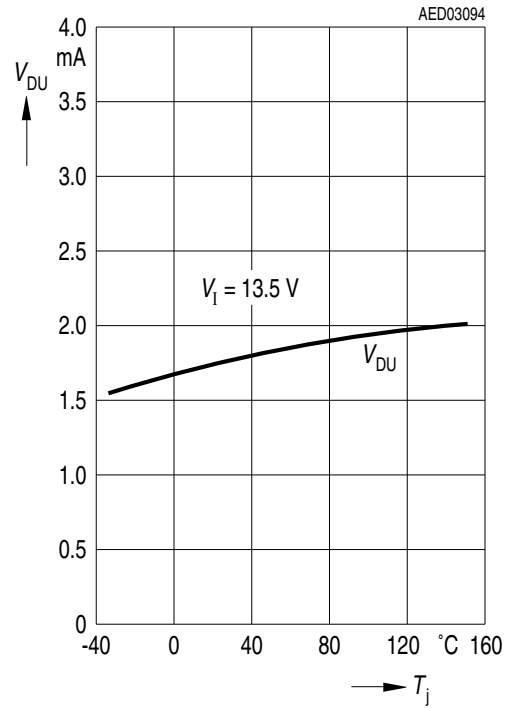
Functional description

Typical performance characteristics

Charge current $I_{D,c}$ vs. junction temperature T_j



Upper reset timing threshold V_{DU} vs. junction temperature T_j



Application information

5.2 Reset circuitry

If the output voltage decreases below 4.5 V, an external capacitor C_D on pin 4 (D) will be discharged by the reset generator. If the voltage on this capacitor drops below V_{DL} , a reset signal is generated on pin 2 (RO), i.e. reset output is set low. If the output voltage rises above the reset threshold, C_D will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches V_{DU} and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of C_D .

5.3 Reset timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$$C_D = (\Delta t \times I_{D,c}) / \Delta V \tag{5.1}$$

Definitions:

- C_D = delay capacitors
- Δt = reset delay time t_{rd}
- $I_{D,c}$ = charge current, typical 14 μ A
- $\Delta V = V_{DU}$, typical 1.8 V

V_{DU} = upper reset timing threshold at C_D for reset delay time

$$t_{rd} = \Delta V \times C_D / I_{D,c} \tag{5.2}$$

The reset reaction time t_{rr} is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1 μ s for delay capacitor of 47 nF. For other values for C_D the reaction time can be estimated using the following equation:

$$t_{rr} \approx 20 \text{ s/F} \times C_D \tag{5.3}$$

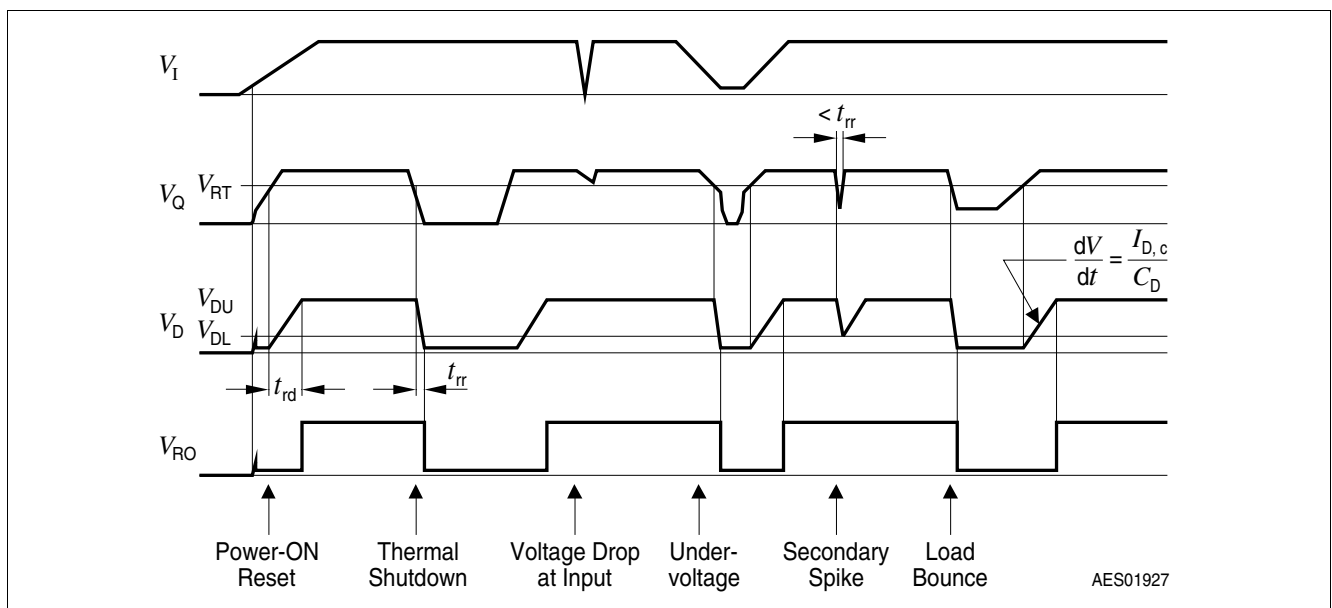


Figure 5 Reset time response

Package information

6 Package information

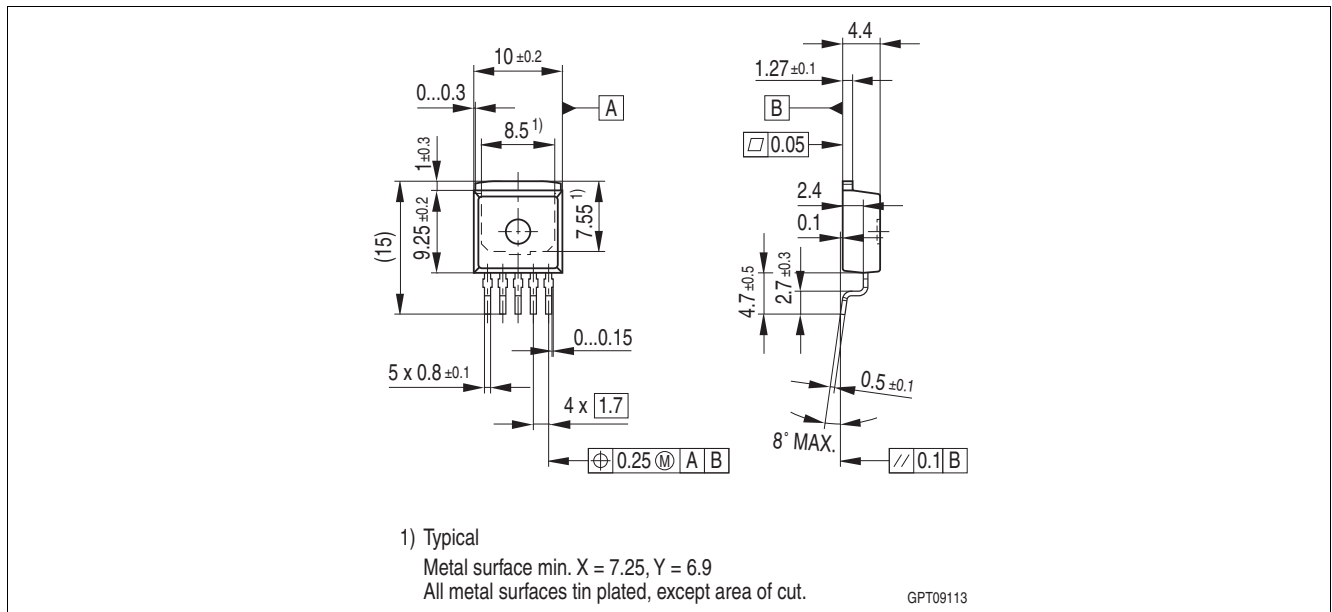


Figure 6 P-TO263-5 (plastic transistor single outline)¹⁾

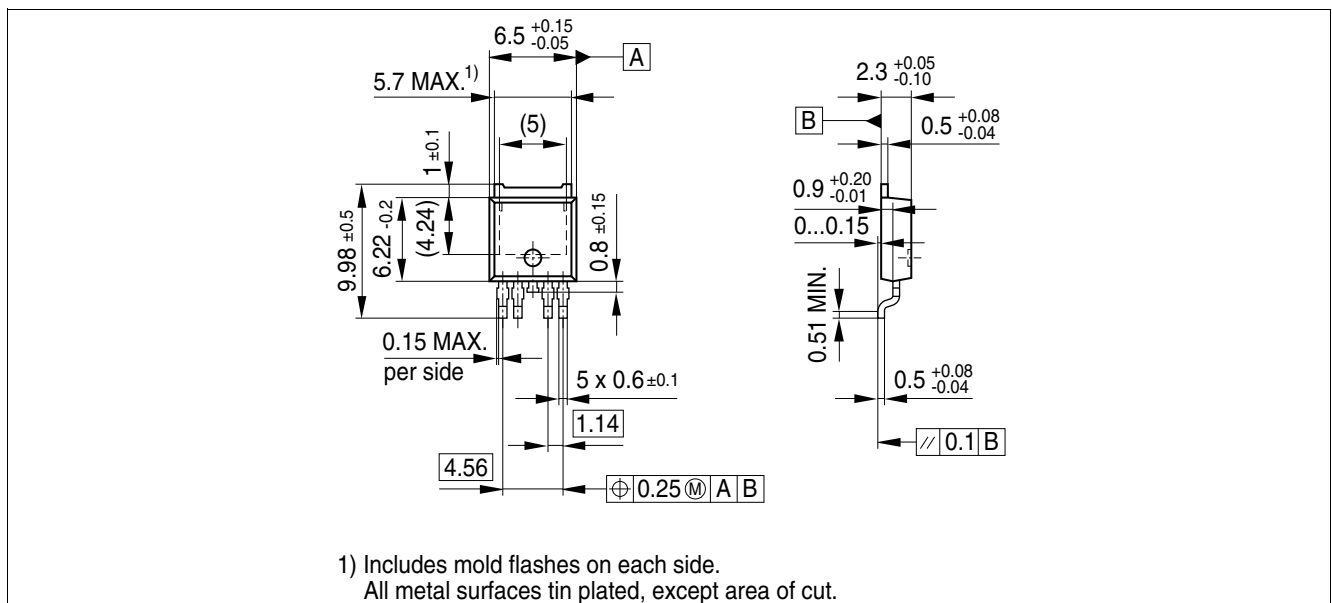


Figure 7 P-TO252-5 (plastic transistor single outline)¹⁾

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm.

Revision history

7 Revision history

| Version | Date | Changes |
|----------------|-------------|---|
| 1.9 | 2020-02-25 | Editorial changes, including rearranged content. |
| 1.8 | 2007-11-09 | Page 1: Changed ESD specification from “>4000V” to “±2 kV HBM” according to PCN No. 2007-08 |
| 1.7 | 2007-03-20 | Initial version of RoHS-compliant derivate of TLE 4270. Change of product name to TLE4270-2 due to modified chip layout and size. Page 1: AEC certified statement added Page 1 and Page 15: RoHS compliance statement and Green product feature added Page 1 and Page 15: Package changed to RoHS compliant version Legal Disclaimer updated |

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