

Linear RF Power FET

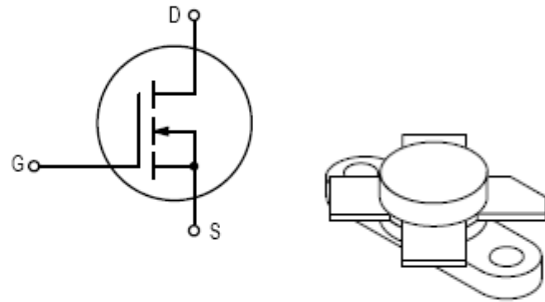
30 W, 175 MHz, 50 V



MRF148A
Rev. V2

Features

- Superior High Order IMD
IMD(d3) (30 W PEP): -35 dB
IMD(d11) (30 W PEP): -60 dB
- Specified 50 V, 30 MHz Characteristics:
Output Power: 30 W
Gain: 18 dB
Efficiency: 40%
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Lower Reverse Transfer Capacitance: 3 pF



Applications

- Industrial, Commercial & Amateur Radio Equipment to 175 MHz.

CASE 211-07, STYLE 2

Description

The MRF148B is a linear RF Power FET designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175 MHz.

Electrical Specifications: $T_A = +25^\circ\text{C}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Off Characteristics					
Drain Source Breakdown Voltage	$V_{GS} = 0, I_D = 10 \text{ mA}$	Vdc	120	—	—
Zero Gate Voltage Drain Current	$V_{DS} = 50 \text{ V}, V_{GS} = 0$	mAdc	—	—	1
Gate Body Leakage Current	$V_{GS} = 20 \text{ V}, V_{DS} = 0$	nAdc	—	—	100
On Characteristics					
Gate Threshold Voltage	$V_{DS} = 10 \text{ V}, I_D = 10 \text{ mA}$	Vdc	0.8	2.5	5.0
Drain Source On-Voltage	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$	Vdc	1.0	3.0	5.0
Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 2.5 \text{ A}$	Mhos	0.8	1.2	—
Dynamic Characteristics					
Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	pF	—	62	—
Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	pF	—	35	—
Reverse Transfer Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	pF	—	3	—

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DC-0007552

Electrical Specifications: $T_A = +25^\circ\text{C}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Functional Tests (SSB)					
Common Source Amplifier Power Gain	$V_{DD} = 50\text{ V}$, $P_{OUT} = 30\text{ W (PEP)}$, $I_{DQ} = 100\text{ mA}$ 30 MHz 175 MHz	dB	—	18 15	—
Drain Efficiency	$V_{DD} = 50\text{ V}$, $f = 30\text{ MHz}$, $I_{DQ} = 100\text{ mA}$ 30 W PEP 30 W CW	%	—	40 50	—
Intermodulation Distortion	$V_{DD} = 50\text{ V}$, $P_{OUT} = 30\text{ W (PEP)}$, $f = 30; 30.001\text{ MHz}$, $I_{DQ} = 100\text{ mA}$	dB	—	-35 -60	—
Load Mismatch	$V_{DD} = 50\text{ V}$, $P_{OUT} = 30\text{ W (PEP)}$, $f = 30; 30.001\text{ MHz}$, $I_{DQ} = 100\text{ mA}$, VSWR 30:1 at all phase angles	No Degradation in Output Power			
Class A Performance					
Power Gain	$V_{DD} = 50\text{ V}$, $P_{OUT} = 10\text{ W (PEP)}$, $f_1 = 30\text{ MHz}$, $f_2 = 30.001\text{ MHz}$, $I_{DQ} = 1\text{ A}$	dB	—	20	—
Intermodulation Distortion ¹	$V_{DD} = 50\text{ V}$, $P_{OUT} = 10\text{ W (PEP)}$, $f_1 = 30\text{ MHz}$, $f_2 = 30.001\text{ MHz}$, $I_{DQ} = 1\text{ A}$	dB	—	-50 -70	—

1. To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

Absolute Maximum Ratings^{5,6}

Parameter	Absolute Maximum
Drain-Source Voltage	120 Vdc
Drain-Gate Voltage	120 Vdc
Gate-Source Voltage	$\pm 40\text{ Vdc}$
Drain Current—Continuous	6 Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$. Derate above 25°C	115 W
Junction Temperature	$+200^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$

Handling Procedures

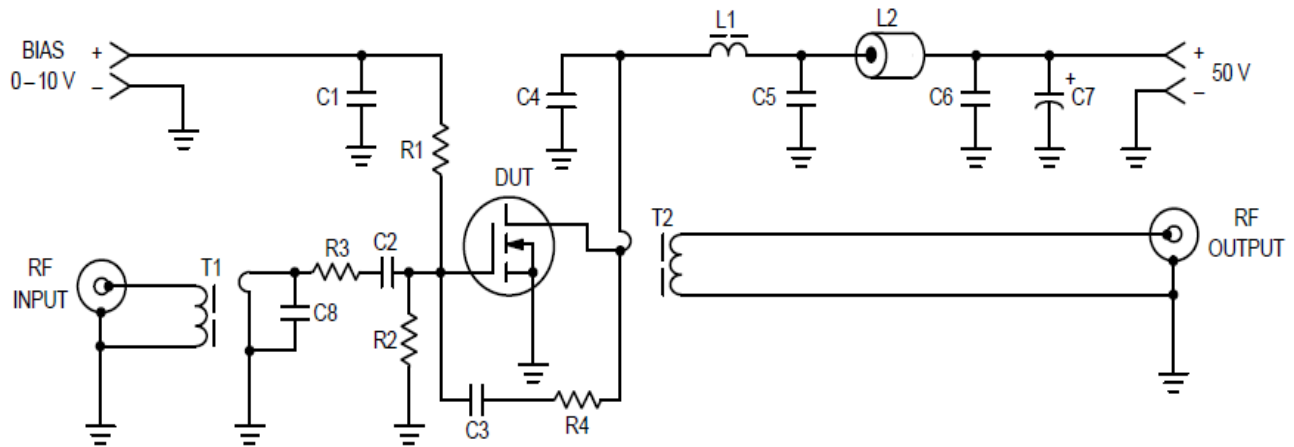
Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Thermal Characteristics

Parameter	Absolute Maximum
Thermal Resistance, Junction to Case	1.52°C/W



- | | |
|---|--------------------------------------|
| C1, C2, C3, C4, C5, C6 — 0.1 μ F Ceramic Chip or Equivalent | R1, R2 — 200 Ω , 1/2 W Carbon |
| C7 — 10 μ F, 100 V Electrolytic | R3 — 4.7 Ω , 1/2 W Carbon |
| C8 — 100 pF Dipped Mica | R4 — 470 Ω , 1.0 W Carbon |
| L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 μ H) | T1 — 4:1 Impedance Transformer |
| L2 — Ferrite Bead(s), 2.0 μ H | T2 — 1:2 Impedance Transformer |

Figure 1. 2.0 to 50 MHz Broadband Test Circuit

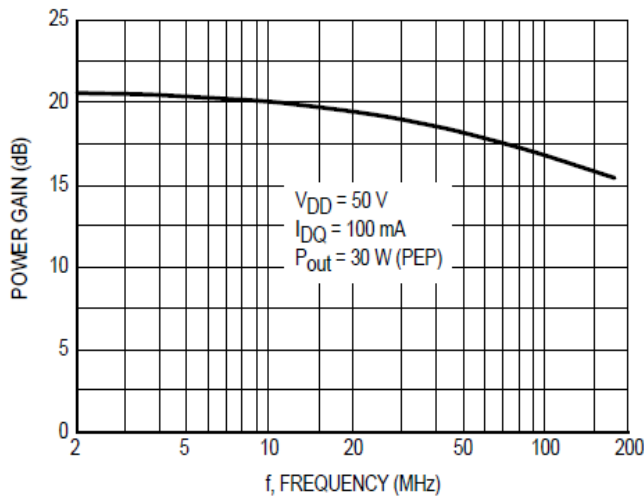


Figure 2. Power Gain versus Frequency

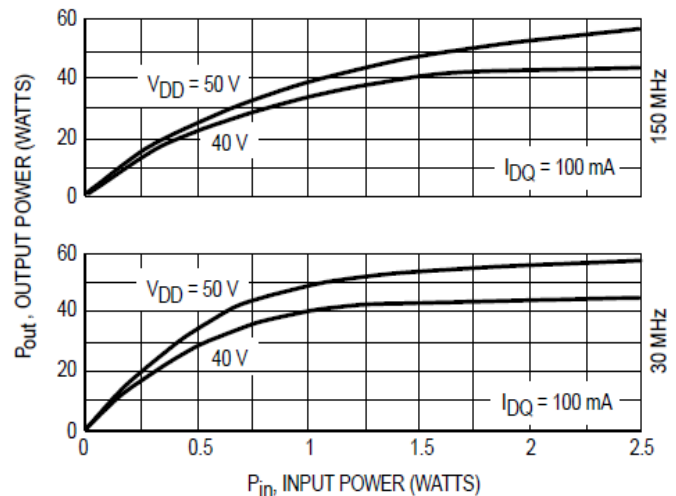


Figure 3. Output Power versus Input Power

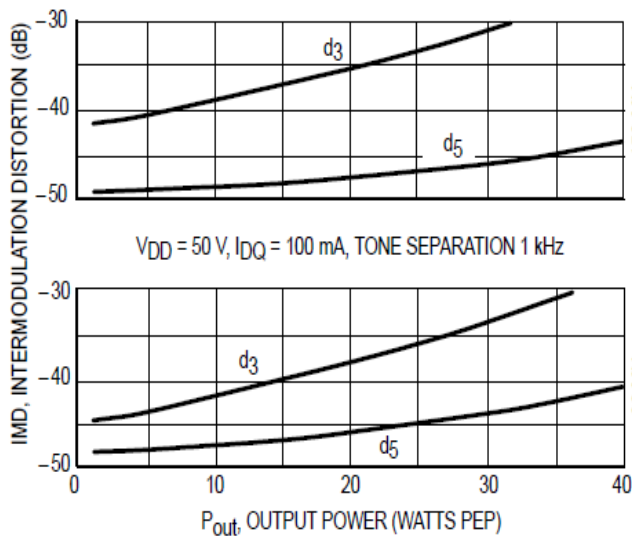


Figure 4. IMD versus P_{out}

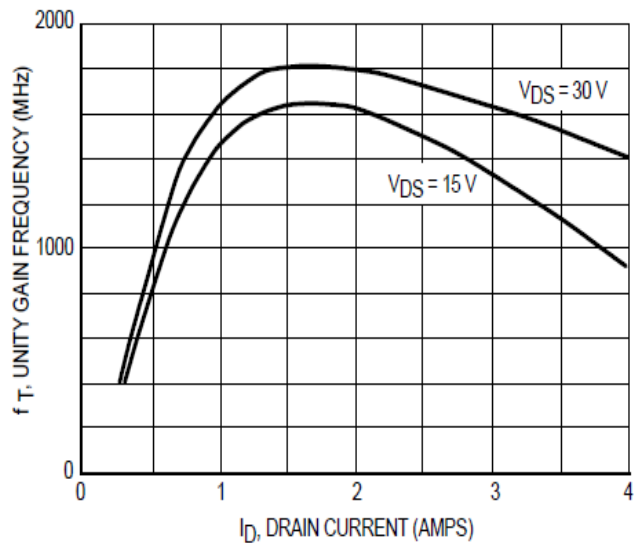


Figure 5. Common Source Unity Gain Frequency versus Drain Current

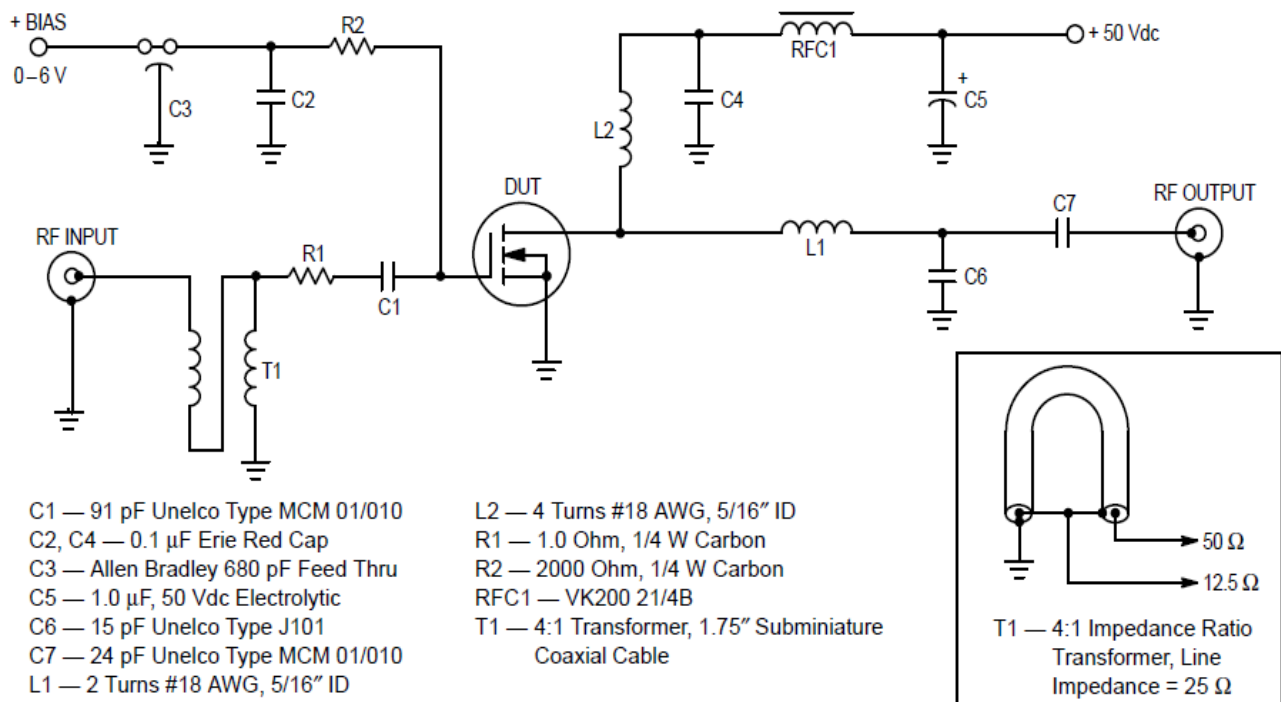


Figure 6. 150 MHz Test Circuit

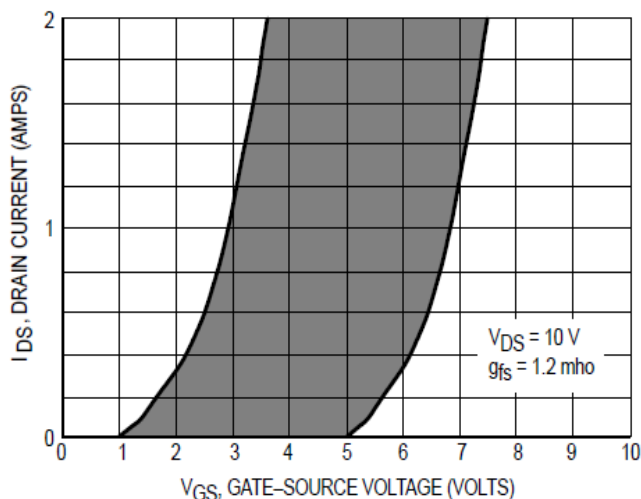


Figure 7. Gate Voltage versus Drain Current

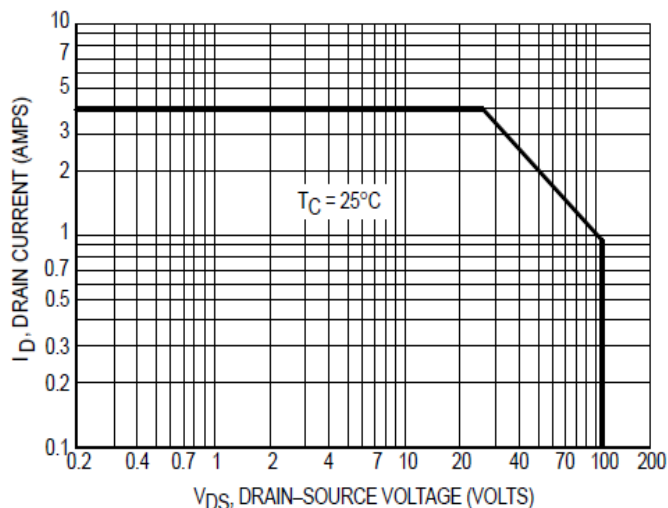
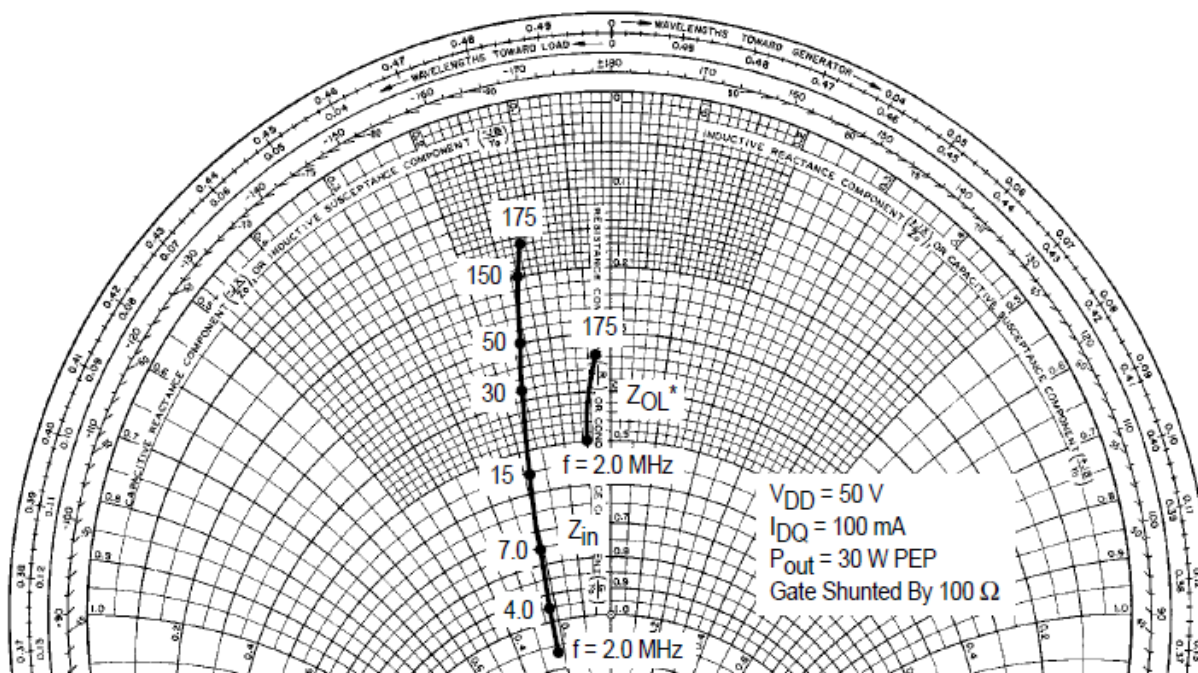


Figure 8. DC Safe Operating Area (SOA)



Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Impedance Coordinates — 50 Ohm Characteristic Impedance

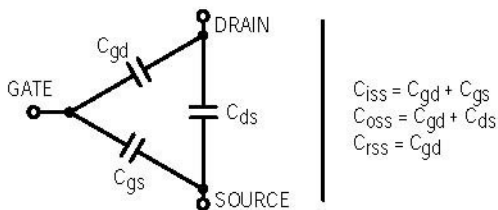
RF Power MOSFET Considerations

MOSFET Capacitances

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}), and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



Linearity & Gain Characteristics

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors.

Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

Drain Characteristics

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

Gate Characteristics

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high on the order of $10^9 \Omega$ resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}

$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$
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Package Dimensions

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.370	0.390	9.40	9.90
C	0.229	0.281	5.82	7.13
D	0.215	0.235	5.47	5.96
E	0.085	0.105	2.16	2.66
H	0.150	0.108	3.81	4.57
J	0.004	0.006	0.11	0.15
K	0.395	0.405	10.04	10.28
M	40°	50°	40°	50°
Q	0.113	0.130	2.88	3.30
R	0.245	0.255	6.23	6.47
S	0.790	0.810	20.07	20.57
U	0.720	0.730	18.29	18.54

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

**CASE 211-07
ISSUE N**

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