



**THE DATASHEET OF  
SN74LVC540AQPWREP**



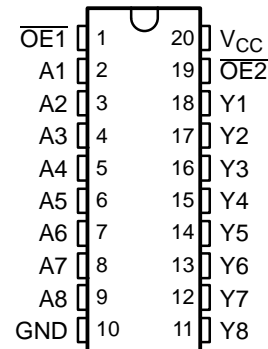
## FEATURES

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree <sup>(1)</sup>
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.3 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}\text{C}$

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation

DW OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN74LVC540A-EP octal buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

This device is ideal for driving bus lines or buffer-memory address registers. This device features inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOIC – DW	Reel of 2000	SN74LVC540AQDWREP	C540AEP
	TSSOP – PW	Reel of 2000	SN74LVC540AQPWREP	C540AEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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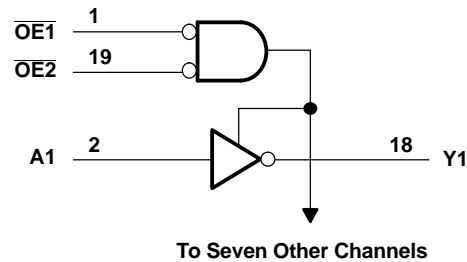
# SN74LVC540A-EP OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS747A–DECEMBER 2003–REVISED AUGUST 2005

**FUNCTION TABLE**

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DW package	58	°C/W
		PW package	83	
$T_{stg}$	Storage temperature range <sup>(5)</sup>	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

**Recommended Operating Conditions<sup>(1)</sup>**

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	V
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V		-12	mA
		V <sub>CC</sub> = 3 V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		12	mA
		V <sub>CC</sub> = 3 V		24	
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	2.7 V to 3.6 V	V <sub>CC</sub> - 0.2		V	
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I <sub>OH</sub> = -24 mA	3 V	2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V	0.2		V	
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			
	I <sub>OL</sub> = 24 mA	3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V	±5		μA	
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V	±15		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	10		μA	
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>		10			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	4		pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	5.5		pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

**SN74LVC540A-EP**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

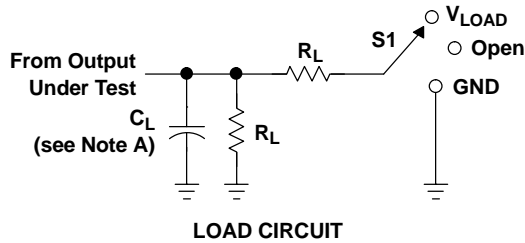
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	7.1		1	5.3	ns
t <sub>en</sub>	$\overline{OE}$	Y	8		1	6.6	ns
t <sub>dis</sub>	$\overline{OE}$	Y	8.2		1	7.4	ns

**Operating Characteristics**

T<sub>A</sub> = 25°C

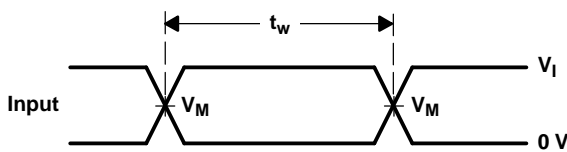
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	f = 10 MHz	56	31	pF
			Outputs enabled	3	
			Outputs disabled		

PARAMETER MEASUREMENT INFORMATION

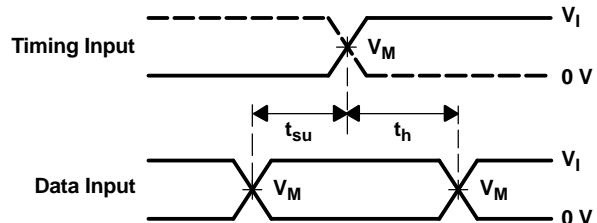


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

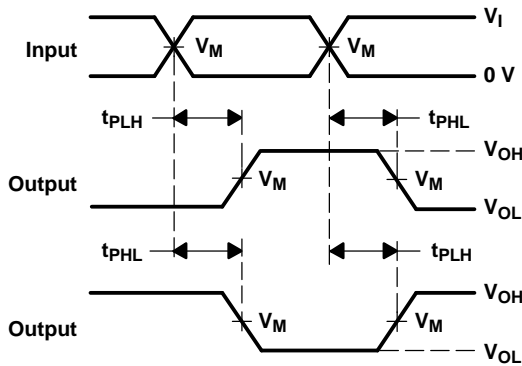
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



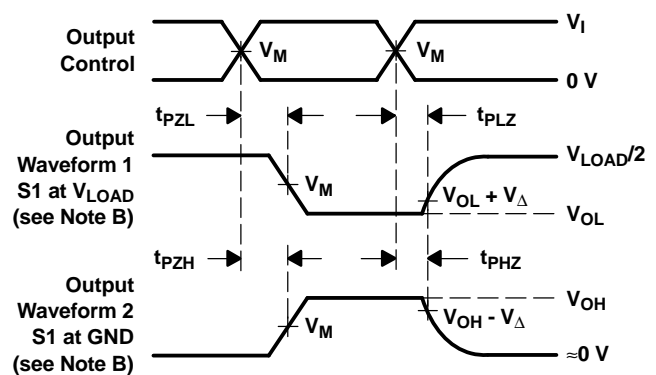
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC540AQDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C540AEP	<a href="#">Samples</a>
SN74LVC540AQPWREP	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C540AEP	<a href="#">Samples</a>
V62/04665-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C540AEP	<a href="#">Samples</a>
V62/04665-01YE	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C540AEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC540A-EP :**

- Catalog: [SN74LVC540A](#)
- Automotive: [SN74LVC540A-Q1](#)
- Military: [SN54LVC540A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC540AQDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC540AQPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC540AQDWREP	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVC540AQPWREP	TSSOP	PW	20	2000	367.0	367.0	38.0

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