ispClock™5500 Family

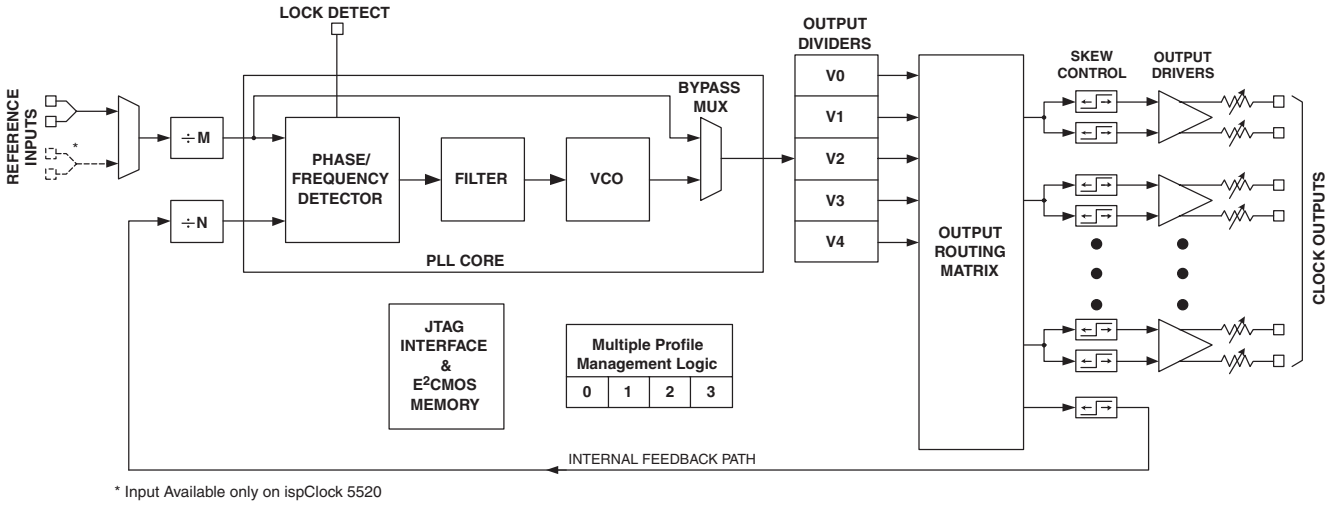
In-System Programmable Clock Generator with Universal Fan-Out Buffer

March 2005 **Data Sheet**

Features

- **10MHz to 320MHz Input/Output Operation**
- **Low Output to Output Skew (<50ps)**
- **Low Jitter Peak-to-Peak(<70ps)**
- **Up to 20 Programmable Fan-out Buffers**
  - Programmable output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, SSTL, LVDS, LVPECL
  - Programmable output impedance
    - 40 to 70Ω in 5Ω increments
  - Programmable slew rate
  - Up to 10 banks with individual V_{CCO} and GND
    - 1.5V, 1.8V, 2.5V, 3.3V
- **Fully Integrated High-Performance PLL**
  - Programmable lock detect
  - Multiply and divide ratio controlled by
    - Input divider (5 bits)
    - Internal feedback divider (5 bits)
    - Five output dividers (5 bits)
  - Programmable On-chip Loop Filter
- **Precision Programmable Phase Adjustment (Skew) Per Output**
  - 16 settings; minimum step size 195ps
    - Locked to VCO frequency
  - Up to +/- 12ns skew range
  - Coarse and fine adjustment modes
- **Up to Five Clock Frequency Domains**
- **Flexible Clock Reference Inputs**
  - Programmable input standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL
  - Clock A/B selection multiplexer
  - Programmable precision termination
- **Four User-programmable Profiles Stored in E²CMOS® Memory**
  - Supports both test and multiple operating configurations
- **Full JTAG Boundary Scan Test In-System Programming Support**
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges**
- **100-pin and 48-pin TQFP Packages**
- **Applications**
  - Circuit board common clock generation and distribution
  - PLL-based frequency generation
  - High fan-out clock buffer

Product Family Block Diagram



* Input Available only on ispClock 5520

General Description and Overview

The ispClock5510 and ispClock5520 are in-system-programmable high-fanout PLL-based clock drivers designed for use in high performance communications and computing applications. The ispClock5510 provides up to 10 single-ended or five differential clock outputs, while the ispClock5520 provides up to 20 single-ended or 10 differential clock outputs. Each pair of outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, LVTTL, LVCMOS, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile E^2CMOS memory.

The ispClock5500's PLL and divider systems supports the synthesis of clock frequencies differing from that of the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken from the output of any of the five V-dividers.

The core functions of all members of the ispClock5500 family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5510 and ispClock5520.

Table 1. ispClock5500 Family Members

Device	Ref. Input Pairs	Clock Outputs
ispClock5510	1	10
ispClock5520	2	20

Figure 1. ispClock5510 Functional Block Diagram

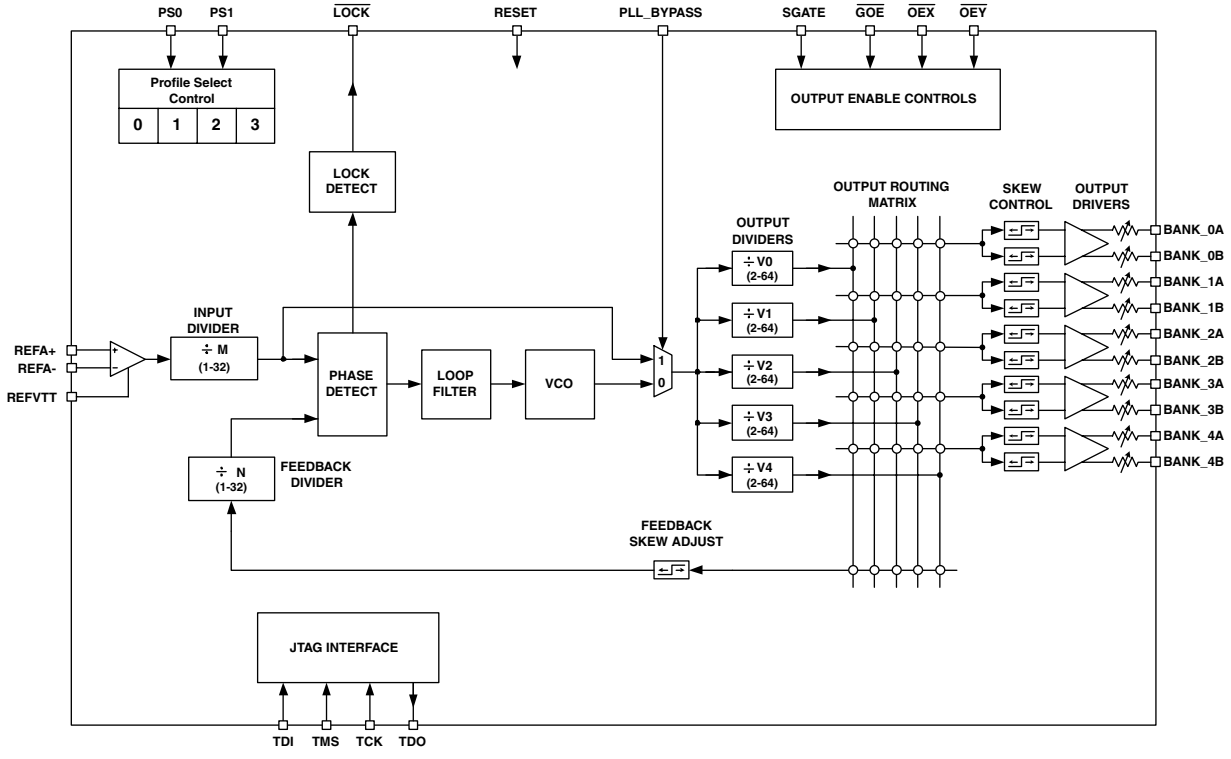
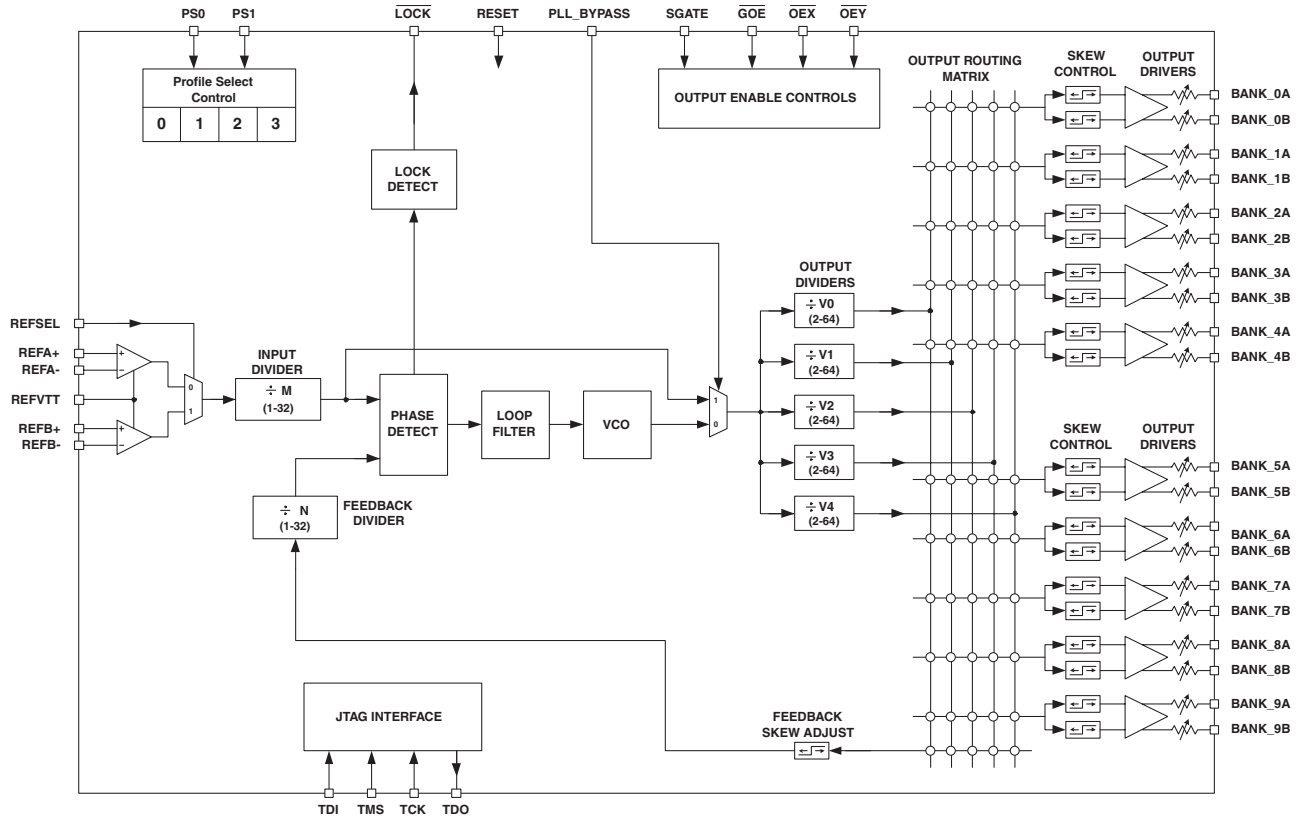


Figure 2. ispClock5520 Functional Block Diagram



Absolute Maximum Ratings

	ispClock5500V
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 130°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	ispClock5500V		Units
			Min.	Max.	
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		1.62	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCASLEW}$	V_{CCA} Turn-on Ramp Rate		—	0.033	V/µs
T_{JOP}	Operating Junction Temperature	Commercial	0	100	°C
		Industrial	-40	115	
T_A	Ambient Operating Temperature	Commercial	0	70[1]	°C
		Industrial	-40	85[1]	

1. Device power dissipation may also limit maximum ambient operating temperature.

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard		V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL		3.0	3.3	3.6	—	—	—	—	—	—
LVCMOS 1.8V		1.71	1.8	1.89	—	—	—	—	—	—
LVCMOS 2.5V		2.375	2.5	2.625	—	—	—	—	—	—
LVCMOS 3.3V		3.0	3.3	3.6	—	—	—	—	—	—
SSTL2 Class 1		2.375	2.5	2.625	1.15	1.25	1.35	V_{REF} - 0.04	—	V_{REF} + 0.04
SSTL3 Class 1		3.0	3.3	3.6	1.30	1.50	1.70	V_{REF} - 0.05	V_{REF}	V_{REF} + 0.05
HSTL Class 1		1.425	1.5	1.575	0.68	0.75	0.90	—	0.5 x V_{CCO}	—
LVPECL (Differential)		3.0V	3.3V	3.6V	—	—	—	—	—	—
LVDS	V_{CCO} = 2.5V	2.375	2.5V	2.625	—	—	—	—	—	—
	V_{CCO} = 3.3V	3.0	3.3	3.6	—	—	—	—	—	—

Note: '—' denotes V_{REF} or V_{TT} not applicable to this logic standard

E^2CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max.	Units
I_{CCD}	Core Supply Current	ispClock5510, f_{VCO} = 640MHz	100	110	mA
		ispClock5520, f_{VCO} = 640MHz	130	150	mA
I_{CCA}	Analog Supply Current	f_{VCO} = 640MHz	5.5	7	mA
I_{CCO}	Output Driver Supply Current (per Bank)	V_{CCO} = 1.8V[1], LVCMOS V_{CCO} = 2.5V[1], LVCMOS V_{CCO} = 3.3V[1], LVCMOS V_{CCO} = 3.3V[2], LVDS	13 18 24 7.5	15 24 35 8	mA
I_{CCJ}	JTAG I/O Supply Current (static)	V_{CCJ} = 1.8V V_{CCJ} = 2.5V V_{CCJ} = 3.3V	200 300 300	300 400 400	µA

1. Supply current consumed by each bank, both outputs active, 18pF load, 320MHz output frequency.
2. Supply current consumed by each bank, 100Ω/5pF differential load, 320MHz output frequency.

DC Electrical Characteristics – Single-ended Logic

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	4[1]	-4[1]
LVCMOS 1.8V	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	4[1]	-4[1]
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	4[1]	-4[1]
SSTL2 Class 1	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54[2]	V_{CCO} - 0.81[2]	7.6	-7.6
SSTL3 Class 1	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.9[2]	V_{CCO} - 1.3[2]	8	-8
HSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[3]	V_{CCO} - 0.4[3]	8	-8

1. Specified for 50Ω internal series output termination.
2. Specified for 40Ω internal series output termination.
3. Specified for ≈20Ω internal series output termination.

DC Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage	V_{THD} ≤ 100mV	V_{THD}/2	—	2.0	V
		V_{THD} ≤ 150mV	V_{THD}/2		2.325	V
V_{THD}	Differential Input Threshold		±100	—	—	mV
V_{IN}	Input Voltage		0	—	2.4	V
V_{OH}	Output High Voltage	R_T = 100Ω	—	1.375	1.60	V
V_{OL}	Output Low Voltage	R_T = 100Ω	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	R_T = 100Ω	250	400	480	mV
ΔV_{OD}	Change in V_{OD} between H and L		—	—	50	mV
V_{OS}	Output Voltage Offset	Common Mode Output Voltage	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to GND	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to Each Other	—	—	12	mA

DC Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input Voltage High	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.17	—	V_{CCD} - 0.88	V
		V_{CCD} = 3.3V	2.14	—	2.42	
V_{IL}	Input Voltage Low	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.81	—	V_{CCD} - 1.48	V
		V_{CCD} = 3.3V	1.49	—	1.83	
V_{OH}	Output High Voltage[1]	V_{CCO} = 3.0 to 3.6V	V_{CCO} - 1.07	—	V_{CCO} - 0.88	V
		V_{CCO} = 3.3V	2.23	—	2.42	
V_{OL}	Output Low Voltage[1]	V_{CCO} = 3.0 to 3.6V	V_{CCO} - 1.81	—	V_{CCO} - 1.62	V
		V_{CCO} = 3.3V	1.49	—	1.68	

1. 100Ω differential termination.

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	Note 3	—	120	150	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	8	10	pF
		Note 6	—	13.5	15	pF

1. Applies to clock reference inputs when termination ‘open’.
2. Applies to TDI, TMS inputs.
3. Applies to REFSEL, PS0, PS1, $\overline{GOE}$, SGATE, PLL_BYPASS, $\overline{OEX}$ and $\overline{OEY}$.
4. Applies to all logic types when in tristated mode.
5. Applies to $\overline{OEX}$, $\overline{OEY}$, TCK, RESET inputs.
6. Applies to REFA+, REFA-, REFB+, REFB-.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Base Parameter(s)	Description	Min.	Typ.	Max.	Units
t_{IOI} Input Adders[2]						
LVTTL_in		Using LVTTL Standard	—	0	—	ns
LVCMOS18_in		Using LVCMOS 1.8V Standard	—	0	—	ns
LVCMOS25_in		Using LVCMOS 2.5V Standard	—	0	—	ns
LVCMOS33_in		Using LVCMOS 3.3V Standard	—	0	—	ns
SSTL2_in		Using SSTL2 Standard	—	0.4	—	ns
SSTL3_in		Using SSTL3 Standard	—	0.4	—	ns
HSTL_in		Using HSTL Standard	—	0.4	—	ns
LVDS_in		Using LVDS Standard	—	1.8	—	ns
LVPECL_in		Using LVPECL Standard	—	1.8	—	ns
t_{IOO} Output Adders[1, 3]						
LVTTL_out		Output Configured as LVTTL Buffer	—	0.1	—	ns
LVCMOS18_out		Output Configured as LVCMOS 1.8V Buffer	—	0.1	—	ns
LVCMOS25_out		Output Configured as LVCMOS 2.5V Buffer	—	0.1	—	ns
LVCMOS33_out		Output Configured as LVCMOS 3.3V Buffer	—	0.1	—	ns
SSTL2_out		Output Configured as SSTL2 Buffer	—	0.1	—	ns
SSTL3_out		Output Configured as SSTL3 Buffer	—	0.1	—	ns
HSTL_out		Output Configured as HSTL Buffer	—	0.1	—	ns
LVDS_out		Output Configured as LVDS Buffer	—	0.1	—	ns
LVPECL_out		Output Configured as LVPECL Buffer	—	0	—	ns
t_{IOS} Output Slew Rate Adders[1]						
Slew_1		Output Slew_1 (Fastest)	—	0	—	ps
Slew_2		Output Slew_2	—	330	—	ps
Slew_3		Output Slew_3	—	660	—	ps
Slew_4		Output Slew_4 (Slowest)	—	1320	—	ps

1. Measured under standard output load conditions – see Figures 3-5.
2. All input adders referenced to LVTTL.
3. All output adders referenced to LVPECL.

Output Rise and Fall Times – Typical Values[1, 2]

Output Type	Slew 1 (Fastest)		Slew 2		Slew 3		Slew 4 (Slowest)		Units
	t_R	t_F	t_R	t_F	t_R	t_F	t_R	t_F	
LVTTL	0.65	0.45	0.85	0.60	1.20	0.90	1.75	1.30	ns
LVCMOS 1.8V	0.90	0.40	1.05	0.50	1.40	0.80	2.00	1.20	ns
LVCMOS 2.5V	0.70	0.40	0.90	0.55	1.20	0.85	1.80	1.20	ns
LVCMOS 3.3V	0.65	0.45	0.85	0.60	1.20	0.90	1.75	1.30	ns
SSTL2	0.65	0.40	0.90	0.60	1.35	0.85	2.30	1.40	ns
SSTL3	0.65	0.40	0.90	0.60	1.35	0.85	2.30	1.40	ns
HSTL	0.85	0.30	1.00	0.50	1.50	0.70	2.55	1.10	ns
LVDS[3]	0.25	0.20	—	—	—	—	—	—	ns
LVPECL[3]	0.20	0.20	—	—	—	—	—	—	ns

1. See Figures 3-5 for test conditions.
2. Measured between 20% and 80% points.
3. Only the 'fastest' slew rate is available in LVDS and LVPECL modes.

Output Test Loads

Figures 3-5 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 3. CMOS Termination Load

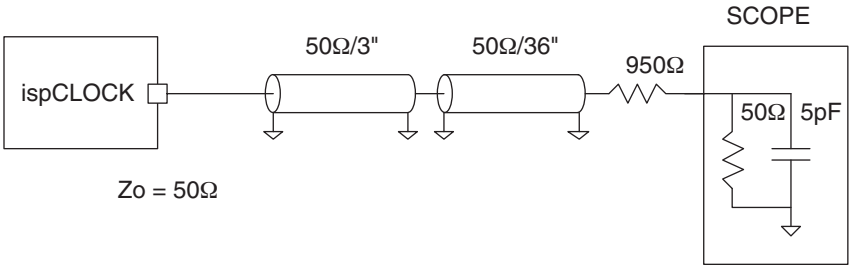


Figure 4. HSTL/SSTL Termination Load

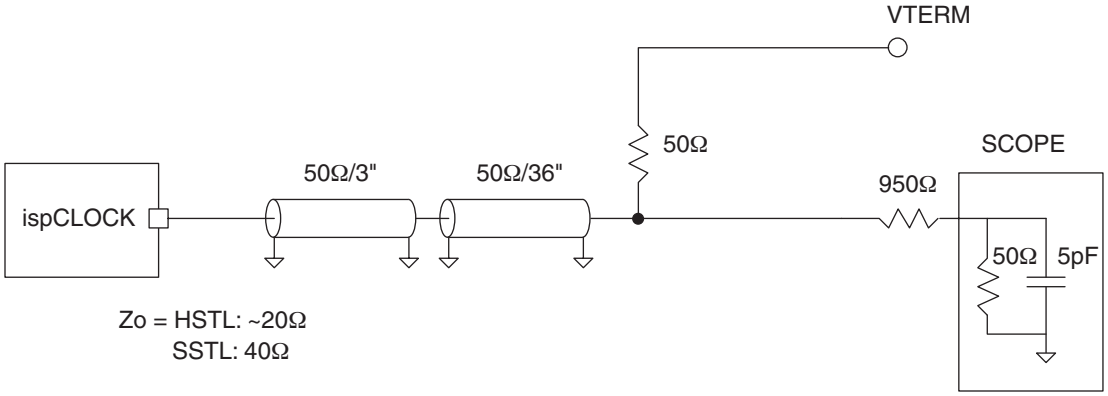
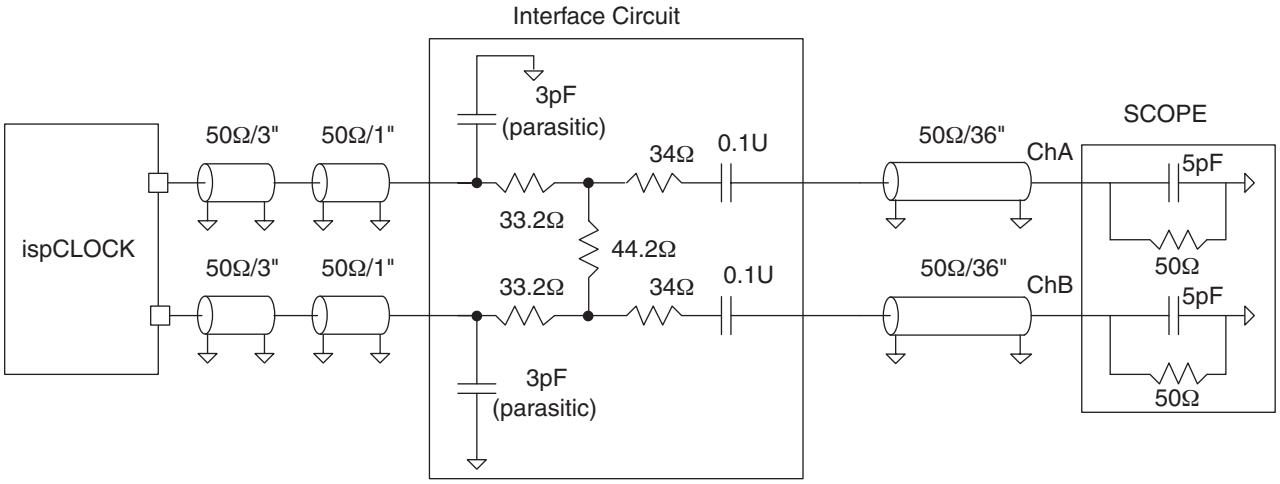


Figure 5. LVDS/LVPECL Termination Load



Programmable Input and Output Termination Characteristics

Symbol	Parameter	Conditions	V_{CCO} Voltage	Min.	Typ.	Max.	Units
R_{IN}	Input Resistance	Rin=40Ω setting		36	—	44	Ω
		Rin=45Ω setting		40.5	—	49.5	
		Rin=50Ω setting		45	—	55	
		Rin=55Ω setting		49.5	—	60.5	
		Rin=60Ω setting		54	—	66	
		Rin=65Ω setting		59	—	71.5	
		Rin=70Ω setting		61	—	77	
R_{OUT}	Output Resistance[1]	Rout≈20Ω setting	VCCO=3.3V	—	14	—	Ω
			VCCO=2.5V	—	14	—	
			VCCO=1.8V	—	14	—	
			VCCO=1.5V	—	14	—	
		Rout≈40Ω setting	VCCO=3.3V	-9%	38	9%	
			VCCO=2.5V	-11%	40	11%	
			VCCO=1.8V	-13%	40	13%	
		Rout≈45Ω setting	VCCO=3.3V	-10%	45	10%	
			VCCO=2.5V	-12%	45	12%	
			VCCO=1.8V	-14%	44	14%	
		Rout≈50Ω setting	VCCO=3.3V	-8%	50	8%	
			VCCO=2.5V	-9%	49	9%	
			VCCO=1.8V	-13%	49	13%	
		Rout≈55Ω setting	VCCO=3.3V	-9%	55	9%	
			VCCO=2.5V	-11%	55	11%	
			VCCO=1.8V	-13%	55	13%	
		Rout≈60Ω setting	VCCO=3.3V	-8%	59	8%	
			VCCO=2.5V	-9%	59	9%	
			VCCO=1.8V	-14%	59	14%	
		Rout≈65Ω setting	VCCO=3.3V	-8%	65	8%	
			VCCO=2.5V	-9%	64	9%	
			VCCO=1.8V	-13%	64	13%	
		Rout≈70Ω setting	VCCO=3.3V	-9%	72	9%	
			VCCO=2.5V	-10%	70	10%	
			VCCO=1.8V	-12%	69	12%	

1. Guaranteed by characterization.

Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{REF}	Reference input frequency range		10	—	320	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference input clock HIGH and LOW times		1.25	—	—	ns
t_{RINP}, t_{FINP}	Input rise and fall times	Measured between 20% and 80% levels	—	—	5	ns
M_{DIV}	M-divider range		1	—	32	
N_{DIV}	N-Divider range		1	—	32	
f_{PFD}	Phase detector input frequency range[2]		10	—	320	MHz
f_{VCO}	VCO operating frequency		320	—	640	MHz
V_{DIV}	Output Divider range	Even integer values only	2	—	64	
f_{OUT}	Output frequency range[1]	Fine Skew Mode, f_{VCO} = 640MHz	10	—	320	MHz
		Coarse Skew Mode, f_{VCO} = 640MHz	5	—	160	MHz
t_{JIT} (cc)	Output adjacent-cycle jitter	1000 cycle sample[3]	—	55	70	ps (p-p)
t_{JIT} (per)	Output period jitter	10000 cycle sample[3]	—	11	14	ps (RMS)
$t_{JIT(\phi)}$	Reference clock to output jitter	6000 cycle sample[3]	—	170	—	ps (RMS)
$t\phi$	Static phase offset	PFD input frequency ≥ 100MHz[5]	—	-500	—	ps
DC_{ERR}	Output duty cycle error (see Table 3 for nominal values)[4]	Output type LVDS, V_{CCO} = 3.3V[6]	—	—	260	ps
		Output type LVCMOS 3.3V[6] f_{OUT} > 100 MHz	—	—	300	ps
t_{CO_BYPASS}	Reference clock to output delay, PLL bypass mode	Inputs and Outputs configured to LVCMOS 3.3V standard	—	5	—	ns
t_L	PLL Lock time	From Power-up event	—	150	500	µs
		From Reset event	—	15	50	µs
PSR	Power supply rejection, period jitter vs. power supply noise	$f_{IN} = f_{OUT}$ = 100MHz VCCA = VCCD = VCCO modulated with 100kHz sinusoidal stimulus	—	0.05	—	$\frac{ps(RMS)}{mV(p\text{-}p)}$

1. In PLL Bypass mode (PLL_BYPASS = HIGH), output will support frequencies down to 0Hz (divider chain is a fully static design).
2. Dividers should be set so that they provide the phase detector with signals of 10MHz or greater for loop stability.
3. $f_{IN} = f_{OUT}$ = 100 MHz, M = N = 1, V = 6, output type LVPECL.
4. Variation in duty cycle expressed in ps. To obtain duty cycle percentage error ($\%_{ERR}$) for a given output frequency (f_{OUT}), $\%_{ERR} = 100 \times f_{OUT} \times DC_{ERR}$.
5. Input and outputs LVPECL mode.
6. See Figures 3-5 for output loads.

Timing Specifications

Skew Matching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-output Skew	Between any two identically configured and loaded outputs regardless of bank.	—	—	50	ps

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKRANGE}$	Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 320 MHz	—	5.86	—	ns
		Fine Skew Mode, f_{VCO} = 640 MHz	—	2.93	—	
		Coarse Skew Mode, f_{VCO} = 320 MHz	—	11.72	—	
		Coarse Skew Mode, f_{VCO} = 640 MHz	—	5.86	—	
SK_{STEPS}	Skew Steps per range		—	16	—	
t_{SKSTEP}	Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 320 MHz	—	390	—	ps
		Fine Skew Mode, f_{VCO} = 640 MHz	—	195	—	
		Coarse Skew Mode, f_{VCO} = 320 MHz	—	780	—	
		Coarse Skew Mode, f_{VCO} = 640 MHz	—	390	—	
t_{SKERR}	Skew Time Accuracy[3]	Fine skew mode	—	30	—	ps
		Coarse skew mode	—	50	—	

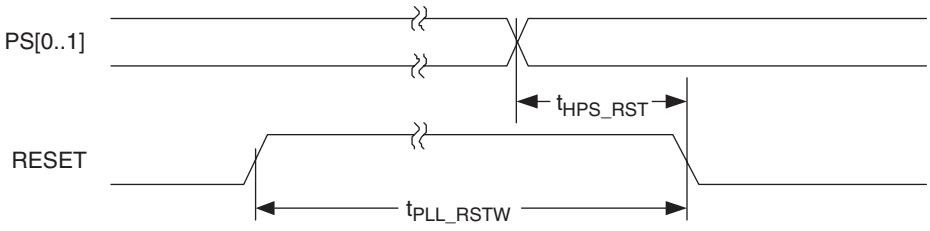
1. Skew control range is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 15/(8 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 15/(4 \times f_{VCO})$.
2. Skew step size is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(4 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, $\overline{OEX}$ or $\overline{OEY}$ to Output Disabled/ Enabled		—	10	20	ns
$t_{DIS/GOE}$	Delay Time, $\overline{GOE}$ to Output Disabled/Enabled		—	10	20	ns
$t_{SUSGATE}$	Setup Time, SGATE to Output Clock Start/ Stop		3	—	—	cycles[1]
t_{PLL_RSTW}	PLL Reset Pulse Width		15	—	—	µs
t_{HPS_RST}	Hold time for RESET past change in PS[0..1]		20	—	—	ns

1. Output clock cycles for the particular output being controlled.

Figure 6. RESET and Profile Select Timing



Timing Specifications (Cont.)

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_{H}	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

Timing Diagrams

Figure 7. Erase (User Erase or Erase All) Timing Diagram

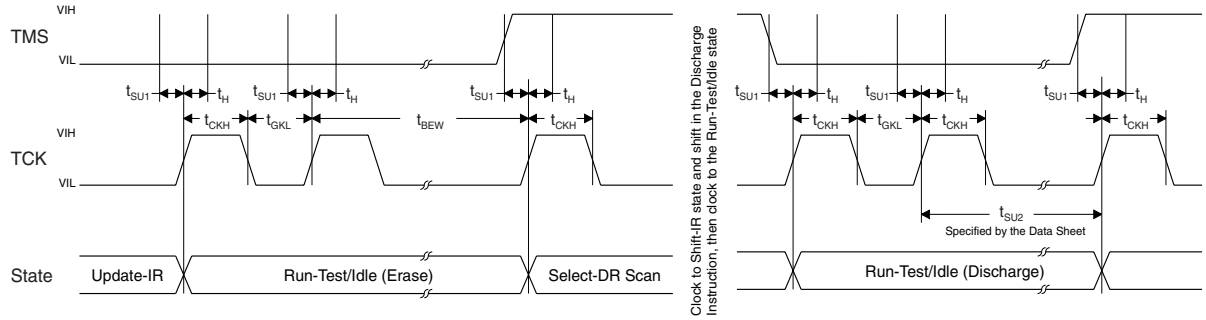


Figure 8. Programming Timing Diagram

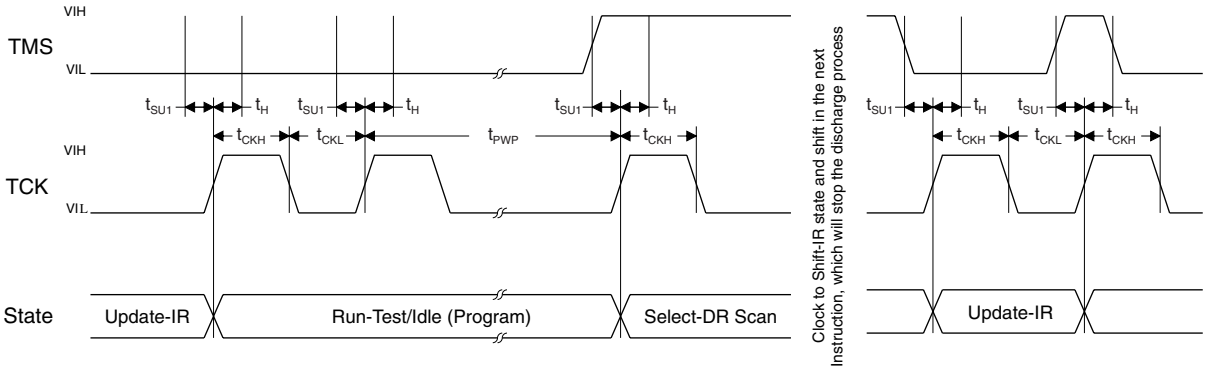


Figure 9. Verify Timing Diagram

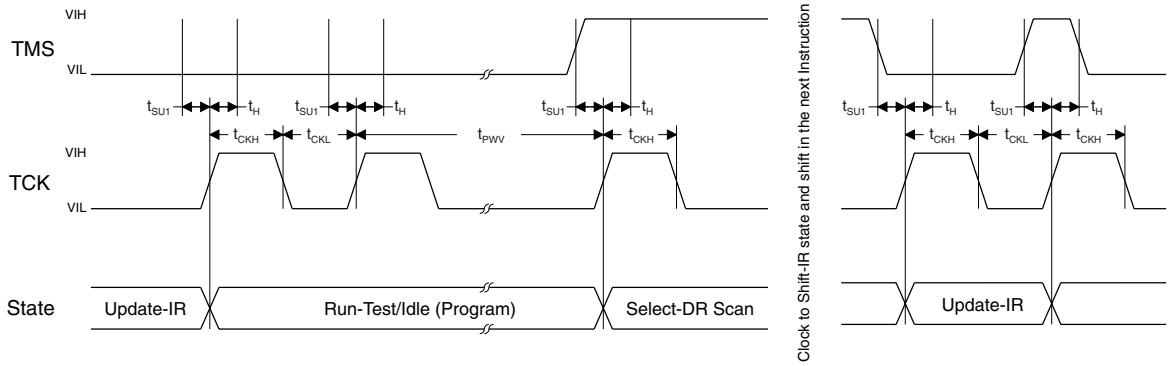
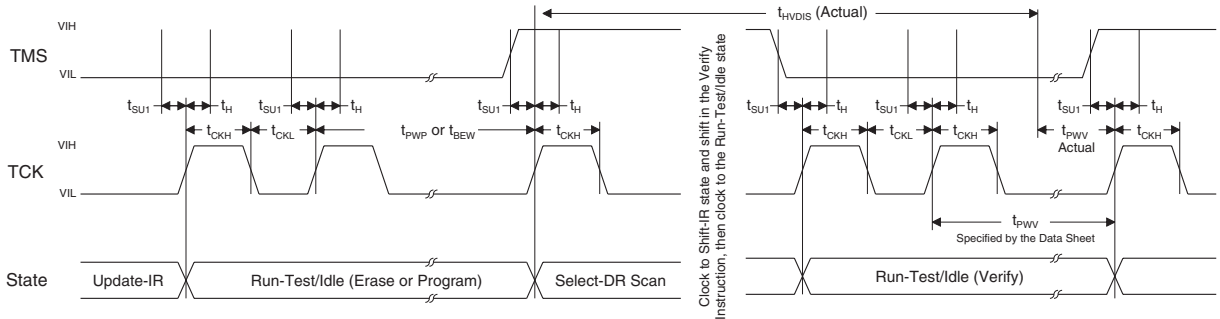
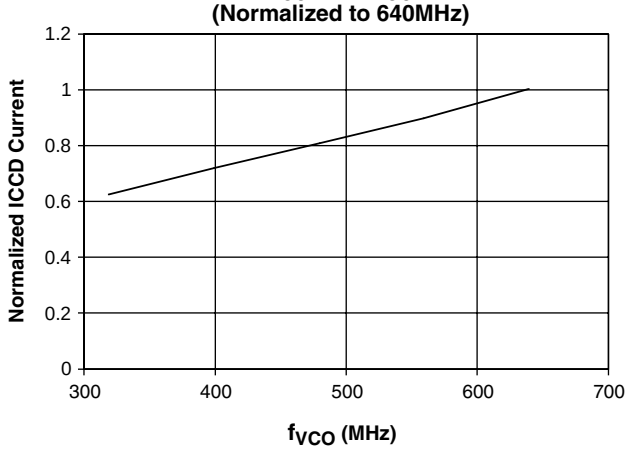


Figure 10. Discharge Timing Diagram

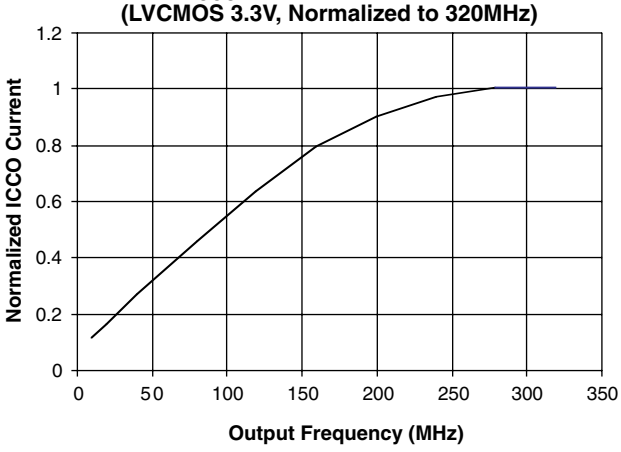


Typical Performance Characteristics

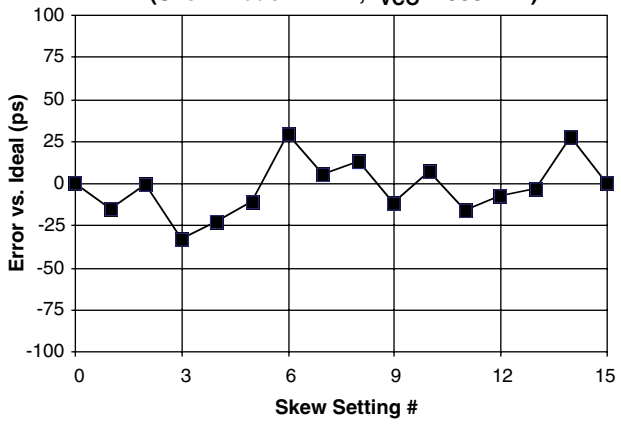
I_{CCD} vs. f_{VCO} (Normalized to 640MHz)



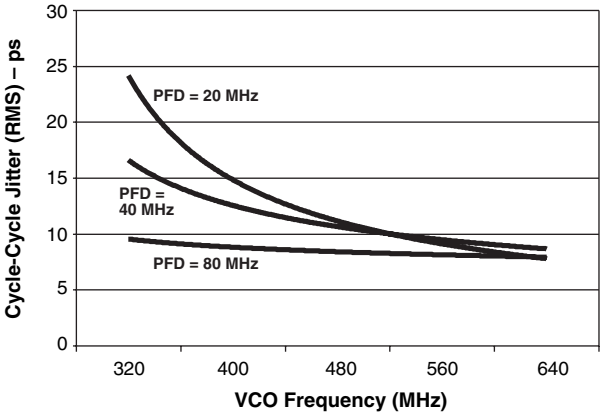
I_{CCO} vs. Output Frequency (LVCMOS 3.3V, Normalized to 320MHz)



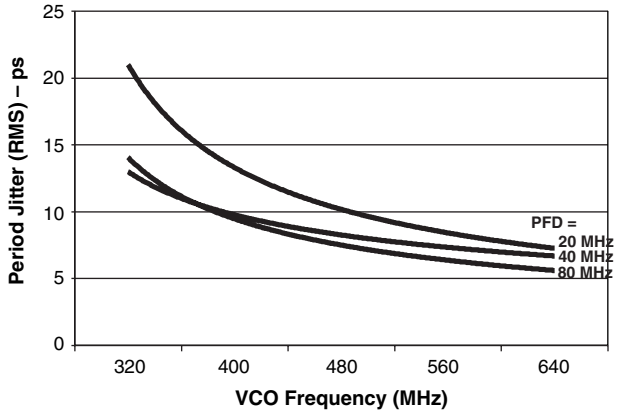
Typical Skew Error vs. Setting (Skew Mode = FINE, f_{VCO} = 600MHz)



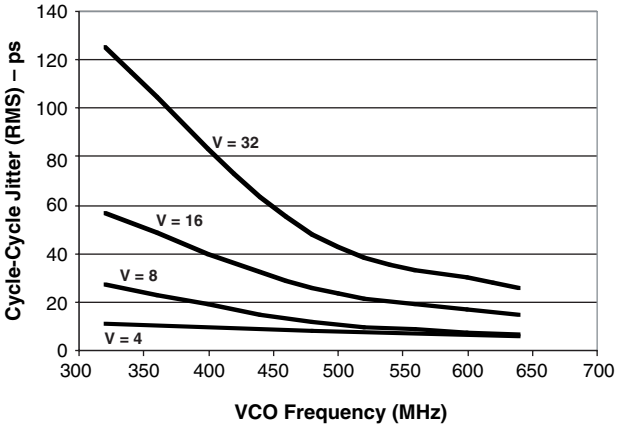
Cycle-Cycle Jitter vs. VCO Frequency V=4



Period Jitter vs. VCO Frequency V=4

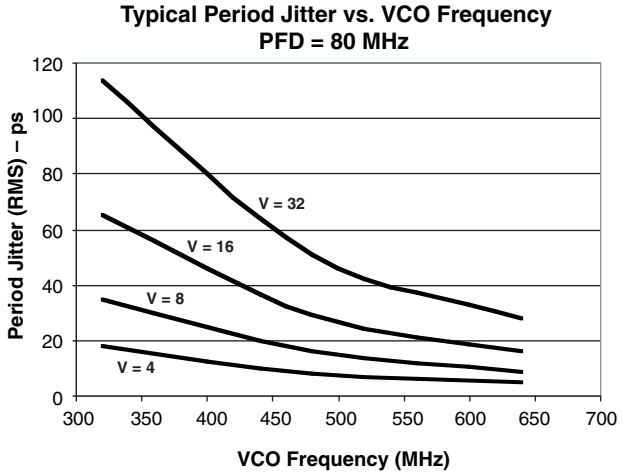


Typical Cycle-Cycle Jitter vs. VCO Frequency PFD = 80 MHz



*PFD = Phase/Frequency Detector

Typical Performance Characteristics (Cont.)



Detailed Description

PLL Subsystem

The ispClock5500 provides an integrated phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Additionally, a set of programmable input, output and feedback dividers (M, N, V[1..5]) are provided to support the synthesis of different output frequencies.

Phase/Frequency Detector

The ispClock5500 provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI}$, $t_{CLOCKLO}$) for it to properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter.

A lock-detection feature is also associated with the PFD. When the ispClock5500 is in a LOCKED state, the $\overline{LOCK}$ output pin goes LOW. The lock detector has two operating modes; phase lock mode and frequency lock mode. In phase-lock mode, the $\overline{LOCK}$ signal is asserted if the phases of the reference and internal feedback signals match, whereas in frequency-lock mode the $\overline{LOCK}$ signal is asserted when the frequencies of the internal feedback and reference signals match. The option of which mode to use is programmable and may be set using PAC-Designer software (available from Lattice's web site at www.latticesemi.com).

In phase-lock mode the lock detector asserts the $\overline{LOCK}$ signal as soon as a lock condition is determined. In frequency-lock mode, however, the PLL must be in a locked condition for a set number of phase detector cycles before the $\overline{LOCK}$ signal will be asserted. The number of cycles required before asserting the $\overline{LOCK}$ signal in frequency-lock mode can be set from 16 through 256, in increments of 16.

The $\overline{LOCK}$ signal is generated in response to certain phase or frequency matches being detected at the input of the phase-frequency detector. Therefore it is possible that the $\overline{LOCK}$ signal may be asserted before the PLL has completely stabilized, and may change state while the PLL is in the process of stabilizing. Additionally, the output dividers are resynchronized in response to the frequency lock detector detecting a lock condition, even when the lock detector is set to phase mode. The frequency lock detector and phase lock detector are completely independent circuits.

Because the frequency lock detector requires a user-selectable number of cycles (16-256) to determine a lock condition, it is possible for the dividers to experience a resynchronization event a short time after a phase lock condition is detected. This may result in an glitch or missing clock cycle on one or more of the outputs. For all of the

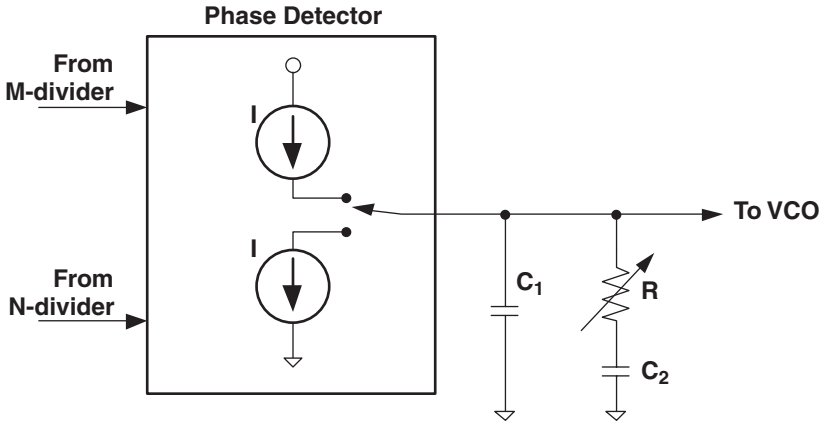
above reasons, it is recommended that when using phase-detect mode, the user wait a small amount of time (~25µs) between the time the $\overline{LOCK}$ signal is first asserted and the time at which the output clock signals are assumed to be completely stable.

When the lock condition is lost the $\overline{LOCK}$ signal will be de-asserted immediately in both phase-lock and frequency-lock detection modes. In frequency-lock mode, however, if the input reference signal is stopped, the $\overline{LOCK}$ output may continue to be asserted. In phase-lock mode, a loss of the input reference signal will always result in de-assertion of the $\overline{LOCK}$ output.

Loop Filter

A simplified schematic for the ispClock5500 loop filter is shown in Figure 11. The filter's capacitors are fixed, and the response is controlled by setting the value of the phase-detector's output current source's and the value of the variable resistor. The phase detector output current has 14 possible settings, ranging from 3µA to 55µA, while the resistor may be set to any one of six values ranging from 2.3K to 9.3K. This provides a total of 84 unique I-R combinations which may be selected.

Figure 11. ispClock5500 Loop Filter (Simplified)



Because the selection of an optimal PLL loop filter can be a daunting task, PAC-Designer offers a set of default filter settings which will provide acceptable performance for most applications. The primary criterion for selecting one of these settings is the total division factor used in the feedback path. This factor is the ratio between the VCO output frequency and the feedback V-divider output frequency which is the product of the N-divider and $V_{feedback}$-divider (N x $V_{feedback}$). Table 2 lists these default settings and conditions under which they should be used.

Table 2. PAC-Designer Recommended Loop Filter Settings

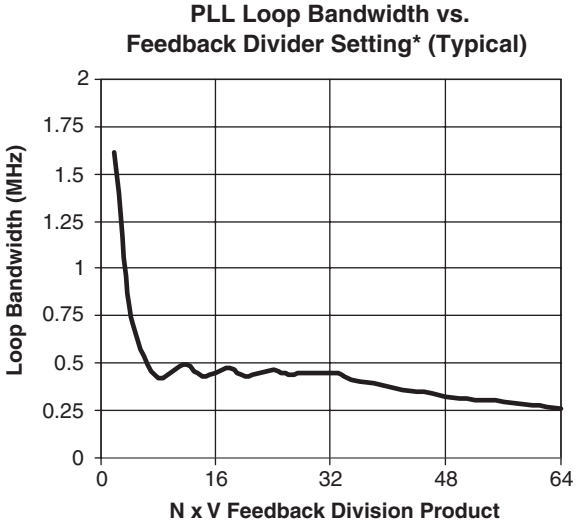
N x V_{FBK}	I (µA)	R (kΩ)
2 to 8	5	2.3
10	7	2.3
12 to 14	9	2.3
16	11	2.3
18 to 20	13	2.3
22	15	2.3
24 to 26	17	2.3
28	19	2.3
30	21	2.3
32 to 64	22	2.3

The choice of loop filter parameters can have significant effects on settling time, output jitter, and whether the PLL will be fundamentally stable and be able to lock to an incoming signal. The values recommended in Table 2 were

chosen to provide maximum loop stability while still providing exceptional jitter performance. Please note that when the skew mode is set to 'coarse', the effective value of NxV must be doubled. Refer to the section titled 'Coarse Skew Mode' on page 30 for more details.

The PLL's loop bandwidth is a function of both the divider configuration and the loop filter settings. Figure 12 shows the loop bandwidth as a function of the total feedback division ratio (N x V_{FBK}). For each NxV feedback divider point in this plot, the PLL loop filter was set to the corresponding value recommended in Table 2. The use of non-recommended loop filter settings may result in significantly different bandwidths for a given NxV divider setting.

Figure 12. PLL Loop Bandwidth vs. Feedback Divider Setting (nominal)



*loop filter configured to recommended setting

VCO

The ispClock5500 provides an internal VCO which provides an output frequency ranging from 320MHz to 640MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to generate skews as a function of the total VCO period. Using the VCO as the basis for controlling output skew allows for highly precise and consistent skew generation, both from device-to-device, as well as channel-to-channel within the same device.

M, N, and V Dividers

The ispClock5500 incorporates a set of programmable dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input.

The input, or M, divider prescales the input reference frequency, and can be programmed with integer values over the range of 1 to 32. To achieve low levels of output jitter, it is best to use the smallest M divider value possible.

The feedback, or N, divider prescales the feedback frequency and like the M divider, can also be programmed with integer values ranging from 1 to 32.

Each one of the five output, or V, dividers can be independently programmed to provide even division ratios ranging from 2 to 64.

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{N \times V_{fbk}}{M \times V_k} \quad (1)$$

where

f_k is the frequency of V divider k
f_{ref} is the input reference frequency
M and N are the input and feedback divider settings
V_{fbk} is the setting of the V divider used to close the PLL feedback path
V_k is the setting of the V divider used to provide output k

Note that because the feedback may be taken from any V divider, V_k and V_{fbk} may refer to the same divider.

Because the VCO has an operating frequency range spanning 320 MHz to 640 MHz, and the V dividers provide division ratios from 2 to 64, the ispClock5500 can generate output signals ranging from 5MHz to 320 MHz. For performance and stability reasons, however, there are several constraints which should be followed when selecting divider values:

- Use the smallest feasible value for the M divider
- The output frequency from the M (and N) divider should be greater or equal to 10 MHz.
- The product of the N divider and the V divider used to close the PLL's feedback loop should be less than or equal to 64 ($N \times V_{fbk} \leq 64$)

Output Duty Cycle

The ispClock5500's output duty cycle varies as a function of the V divider used to generate that output. If the V-divider setting is either 2 or a multiple of 4, the nominal output duty cycle will be exactly 50%. All other V divider settings will result in non-50% output duty cycles. Table 3 summarizes the nominal output duty cycle as a function of the V divider setting. Note that if the output is inverted, the duty cycle will be equal to 100%-DC%, where DC% is the duty cycle indicated in the table. For example, with a V divider of 14, the non-inverted duty cycle from Table 3 will be 43%. For an inverted output, the duty cycle will be 100%-43% or 57%.

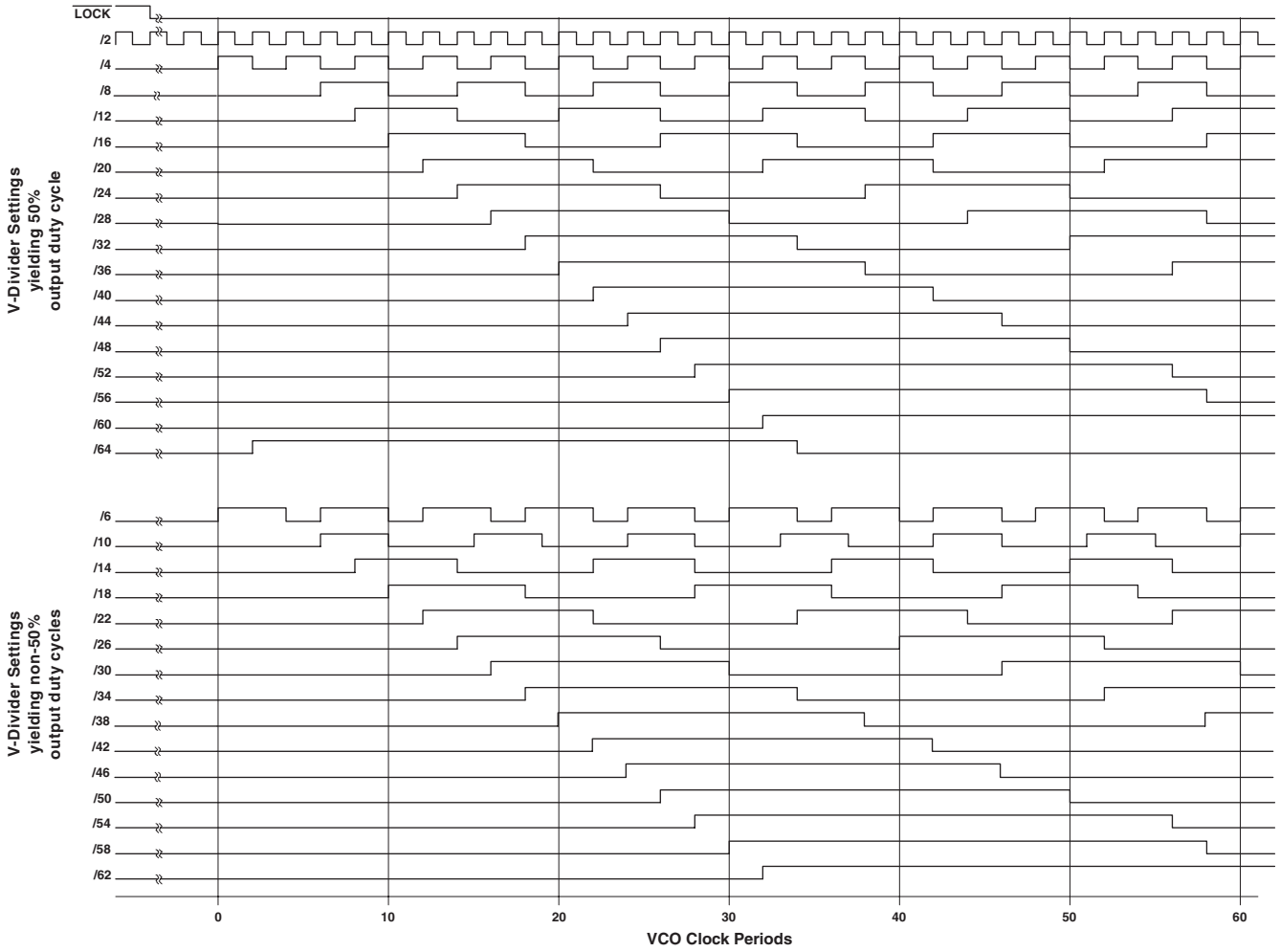
Table 3. Nominal Output Duty Cycle vs. V-Divider Setting

Divider Settings with 50% Output Duty Cycle	
V	**DC%**
2	50
4	
8	
12	
16	
20	
24	
28	
32	
36	
40	
44	
48	
52	
56	
60	
64	

Divider Settings with Non-50% Output Duty Cycles	
V	**DC%**
6	33
10	40
14	43
18	44
22	45
26	46
30	47
34	47
38	47
42	48
46	48
50	48
54	48
58	48
62	48

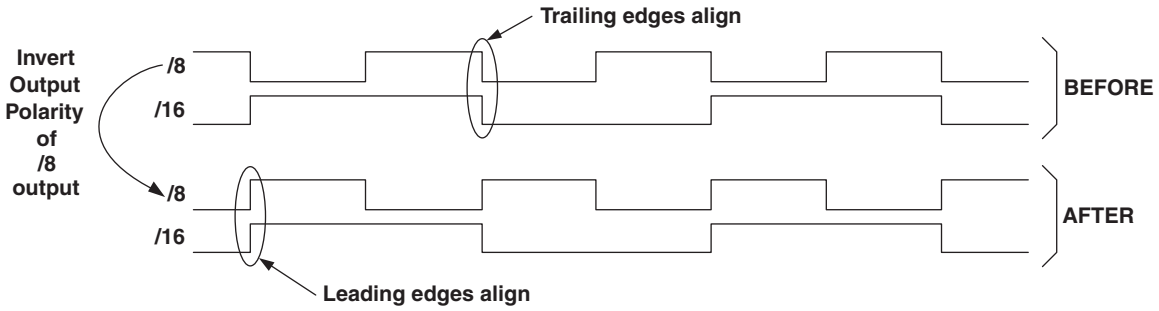
Figure 13 shows the relative timing for a V-divider as a function of its 32 possible divisor settings (2-64) as the PLL locks. If two V-dividers are configured with the same divisor, their outputs will be synchronized. If these two V-dividers are fed to separate outputs, and the skew settings for these two outputs are identical, then the corresponding rising and falling edges for the two outputs will occur simultaneously.

Figure 13. ispClock5500 Output Divider Timing Relationships Among Various Divisors



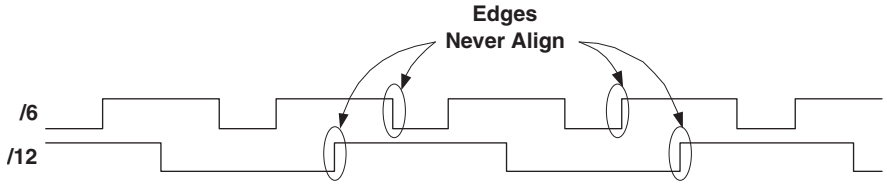
If two V-dividers are configured with different divisors, however, their outputs may not necessarily have aligned edges, even in cases where one divisor is an integer multiple of the other (e.g. 6 and 12). In cases where the divisor is set to either 2 or a multiple of 4, the output duty cycle will be 50% (top set of waveforms in Figure 13), and the rising edges (or falling edges) of outputs driven from different divisors may be aligned by inverting one or more of the outputs as shown in Figure 14.

Figure 14. Flipping Polarity to Edge Align Two Outputs



For V-divider combinations in which one or more of the V-dividers is configured to a value that is not divisible by 4 (e.g. 6), there exists the possibility that neither rising nor falling edges may align. For example, when V-divider values of 6 and 12 are chosen, the two resulting outputs will have no edge alignment, as shown in Figure 15. Note that because the offset is 2 VCO periods in this case, it is not possible to use the skew adjustment feature to force any of the edges into perfect alignment as the skew control units provide a maximum delay of 1.875 VCO periods.

Figure 15. Timing Relationship Between V-divider Values of 6 and 12



PLL_BYPASS Mode

The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the output of the M divider is routed directly to the inputs of the V dividers. In PLL_BYPASS mode, the nominal values of the V dividers are halved, so that they provide division ratios ranging from 1 to 32. The divide-by-1 setting, however, is invalid and will produce undefined results. The output frequency for a given V divider (f_k) will be determined by

$$f_k = \frac{f_{ref} \times 2}{M \times V_k} \quad (2)$$

Please note that PLL_BYPASS mode is provided primarily for testing purposes. When PLL_BYPASS mode is enabled, features such as lock detect and skew generation are unavailable.

Reference Inputs

The ispClock5500 provides sets of configurable, internally-terminated inputs for clock reference signals. In normal operation, the clock reference input (REFB) is connected to the system clock from which the output signals are to be derived.

The ispClock5510 provides one input signal pair for reference input, while the ispClock5520 provides two input pairs for reference signals. To select between reference inputs, the ispClock5520 provides a CMOS-compatible digital input called REFSEL. Table 4 shows the behavior of this control input:

Table 4. REFSEL Operation for ispClock5520

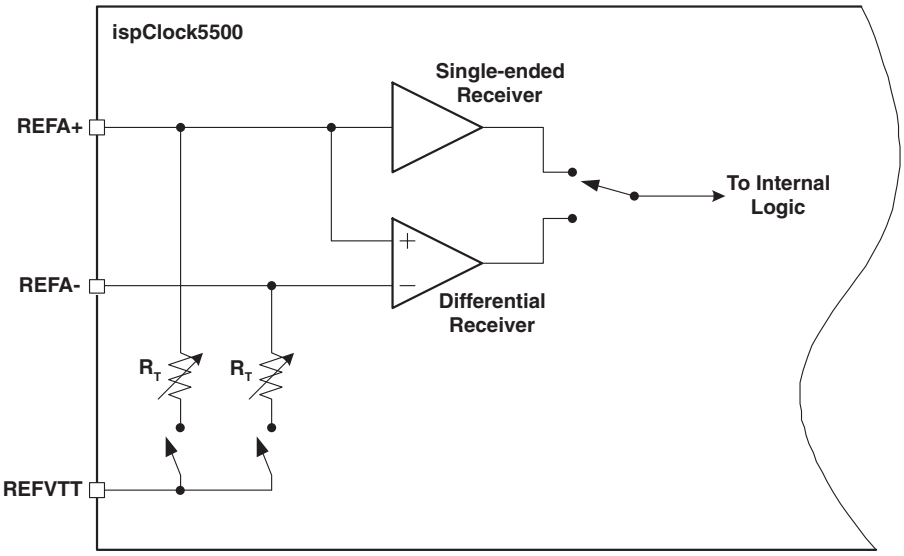
REFSEL	Selected Input Pair
0	REFA+/-
1	REFB+/-

Clock reference inputs may be configured to interface to signals from the following logic families with little or no external support circuitry:

- LVTTL (3.3V)
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- LVDS
- LVPECL (differential, 3.3V)

Each input also features internal programmable termination resistors, as shown in Figure 16.

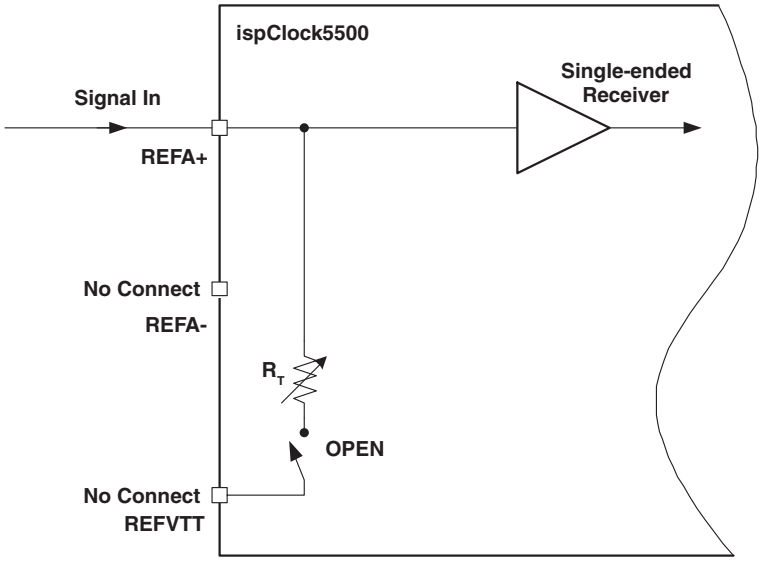
Figure 16. ispClock5500 Clock Reference Input Structure (REFA+/- Pair Shown)



The following usage guidelines are suggested for interfacing to supported logic families.

LVTTL (3.3V), LVCMOS (1.8V, 2.5V, 3.3V)
The receiver should be set to LVCMOS or LVTTL mode, and the input signal should be connected to the '+' terminal of the input pair (e.g. REFA+). The '-' input terminal should be left floating. CMOS transmission lines are generally source terminated, so all termination resistors should be set to the OPEN state. Figure 17 shows the proper configuration. Please note that because switching thresholds are different for LVCMOS running at 1.8V, there is a separate configuration setting for this particular standard.

Figure 17. LVCMOS/LVTTL Input Receiver Configuration

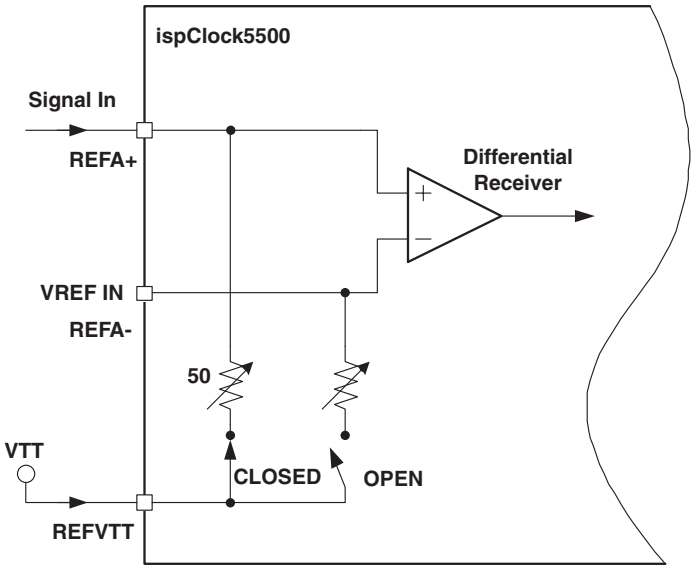


HSTL, SSTL2, SSTL3

The receiver should be set to HSTL/SSTL mode, and the input signal should be fed into the '+' terminal of the input pair. The '-' input terminal should be tied to the appropriate V_{ref} value, and the REFVTT terminal should be tied to a V_{TT} termination supply. The positive input's terminating resistor should be engaged and set to 50Ω. Figure 18 shows an appropriate configuration. Refer to the "Recommended Operating Conditions - Supported Logic Standards" table in this data sheet for suitable values of V_{REF} and $V_{TT.}$

One important point to note is that the termination supplies must have low impedance and be able to both source and sink current without experiencing fluctuations. These requirements generally preclude the use of a resistive divider network, which has an impedance comparable to the resistors used, or of commodity-type linear voltage regulators, which can only source current. The best way to develop the necessary termination voltages is with a regulator specifically designed for this purpose. Because SSTL and HSTL logic is commonly used for high-performance memory busses, a suitable termination voltage supply is often already available in the system.

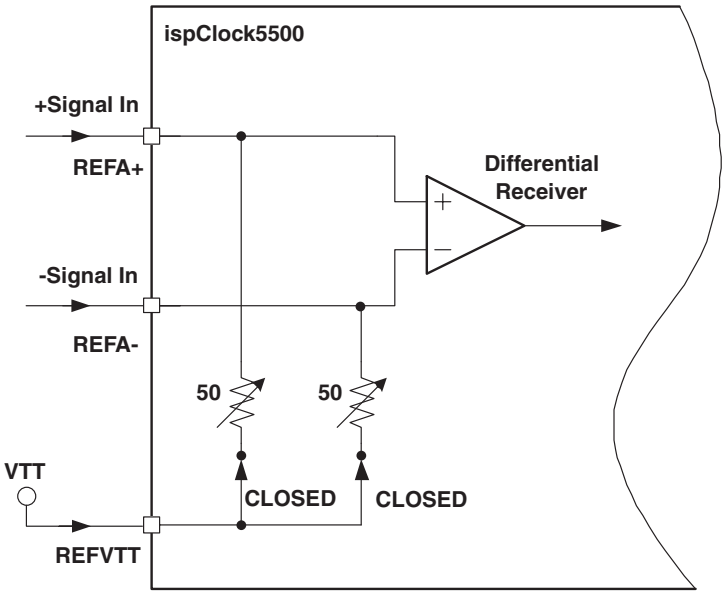
Figure 18. SSTL2, SSTL3, HSTL Receiver Configuration



Differential HSTL and SSTL

HSTL and SSTL are sometimes used in a differential form, especially for distributing clocks in high-speed memory systems. Figure 19 shows how ispClock5500 reference input should be configured for accepting these standards. The major difference between the differential and single-ended forms of these logic standards is that in the differential cases, the REFA- input is used as a signal input, not a reference level, and that both terminating resistors are engaged and set to 50Ω.

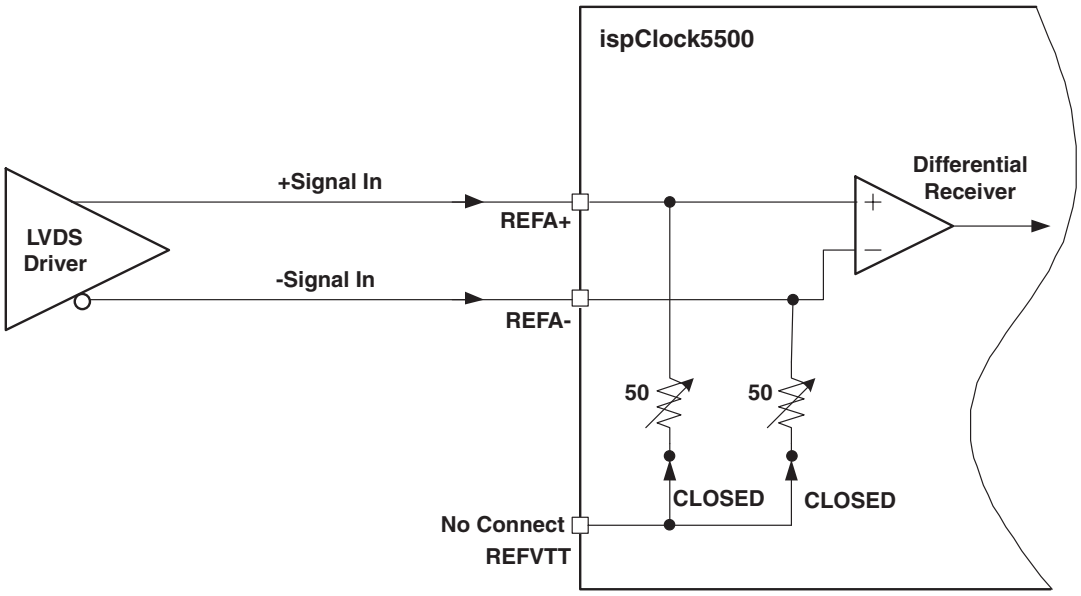
Figure 19. Differential HSTL/SSTL Receiver Configuration



LVDS/Differential LVPECL

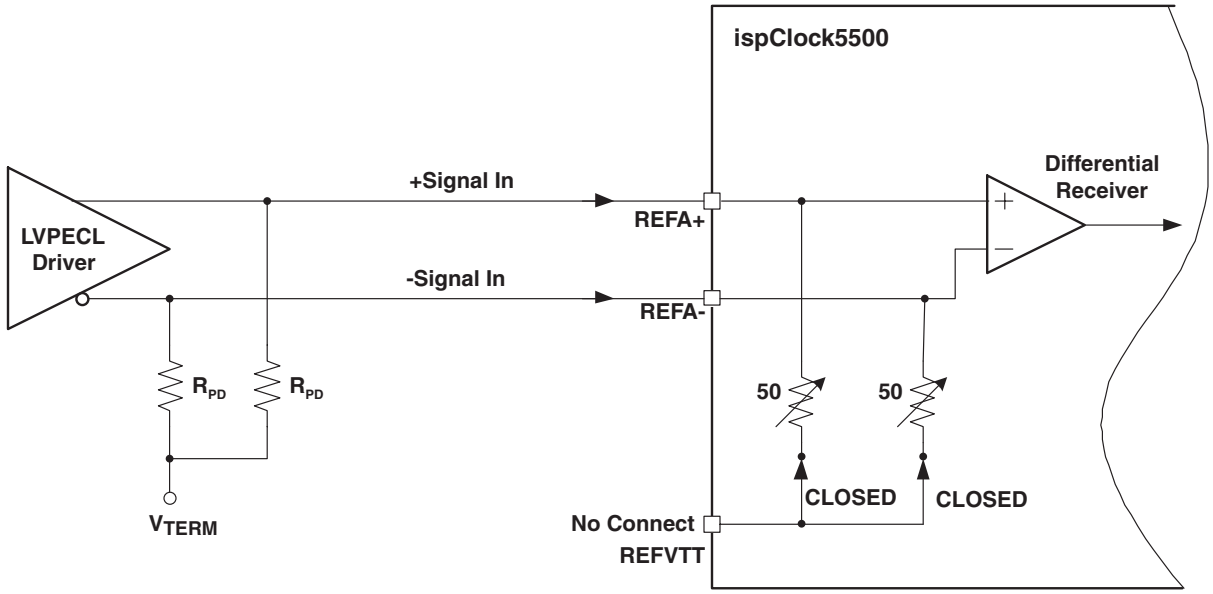
The receiver should be set to LVDS or LVPECL mode as required and both termination resistors should be engaged and set to 50Ω. The REFVTT pin, however, should be left unconnected. This creates a floating 100Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 20.

Figure 20. LVDS Input Receiver Configuration



Note that while a floating 100Ω resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. When interfacing to an LVPECL input signal, the ispClock5500's internal termination resistors should not be used for this pull-down function, as they may be damaged from excessive current. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 21)

Figure 21. LVPECL Input Receiver Configuration



Please note that while the above discussions specify using 50Ω termination impedances, the actual impedance required to properly terminate the transmission line and maintain good signal integrity may vary from this ideal. The actual impedance required will be a function of the driver used to generate the signal and the transmission medium used (PCB traces, connectors and cabling). The ispClock5500's ability to adjust input impedance over a range of 40Ω to 70Ω allows the user to adapt his circuit to non-ideal behaviors from the rest of the system without having to swap out components.

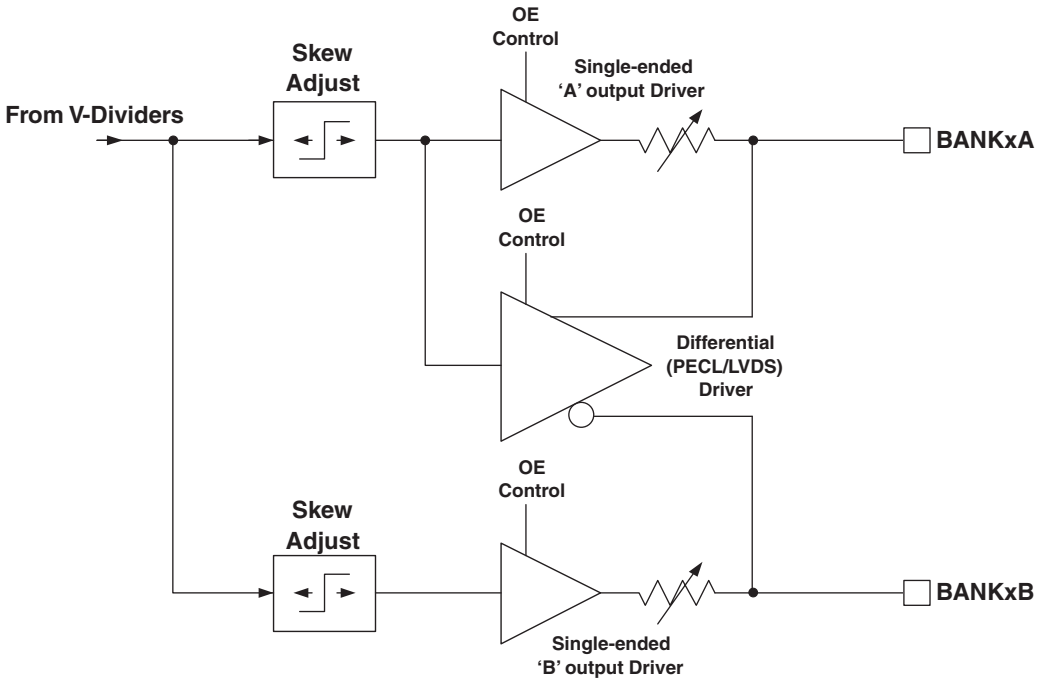
Output Drivers

The ispClock5500 provide banks of configurable, internally-terminated high-speed dual-output line drivers. The ispClock5510 provides five driver banks, while the ispClock5520 provides ten. Each of these driver banks may be configured to provide either a single differential output signal, or a pair of single-ended output signals. Programmable internal source-series termination allows the ispClock5500 to be matched to transmission lines with impedances ranging from 40 to 70 Ohms. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by external control lines. Additionally, each can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 22 shows a block diagram of a typical ispClock5500 output driver bank and associated skew control.

Because of the high edge rates which can be generated by the ispClock5500's clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respective output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GNDD pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 22. ispClock5500 Output Driver and Skew Control



Each of the ispClock5500's output driver banks can be configured to support the following logic outputs:

- LVTTL
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- LVDS
- Differential LVPECL (3.3V)

To provide LVTTL, LVCMOS, SSTL2, SSTL3, and HSTL outputs, the CMOS output drivers in each bank are enabled. These circuits provide logic outputs which swing from ground to the VCCO supply rail. The choice of VCCO to be supplied to a given bank is determined by the logic standard to which that bank is configured. Because each pair of outputs has its own VCCO supply pin, each bank can be independently configured to support a different logic standard. Note that the two outputs associated with a bank must necessarily be configured to the same logic standard. The source impedance of each of the two outputs in each bank may be independently set over a range of 40Ω to 70Ω in 5Ω steps. A low impedance option (≈20Ω) is also provided for cases where low source termination is desired on a given output, such as when using HSTL output mode.

Control of output slew rate is also provided in LVTTL, LVCMOS, SSTL2, SSTL3, and HSTL output modes. Four output slew-rate settings are provided, as specified in the "Output Rise Times" and "Output Fall Times" tables in this data sheet.

To provide LVDS and differential LVPECL outputs, a separate driver is used which provides the correct LVDS or LVPECL logic levels when operating from a 3.3V VCCO. Because both LVDS and differential LVPECL transmission lines are normally terminated with a single 100Ω resistor between the '+' and '-' signal lines at the far end, the

ispClock5500's internal termination resistors are not available in these modes. Also note that output slew-rate control is not available in LVDS or LVPECL mode, and that these drivers always operate at a fixed slew-rate.

Polarity control (true/inverted) is available for all output drivers. In the case of single-ended output standards, the polarity of each of the two output signals from each bank may be controlled independently. In the case of differential output standards, the polarity of the differential pair may be selected.

Suggested Usage

Figure 23 shows a typical configuration for the ispClock5500's output driver when configured to drive an LVTTL or LVCMOS load. The ispClock5500's output impedance should be set to match the characteristic impedance of the transmission line being driven. The far end of the transmission line should be left open, with no termination resistors.

Figure 23. Configuration for LVTTL/LVCMOS Output Modes

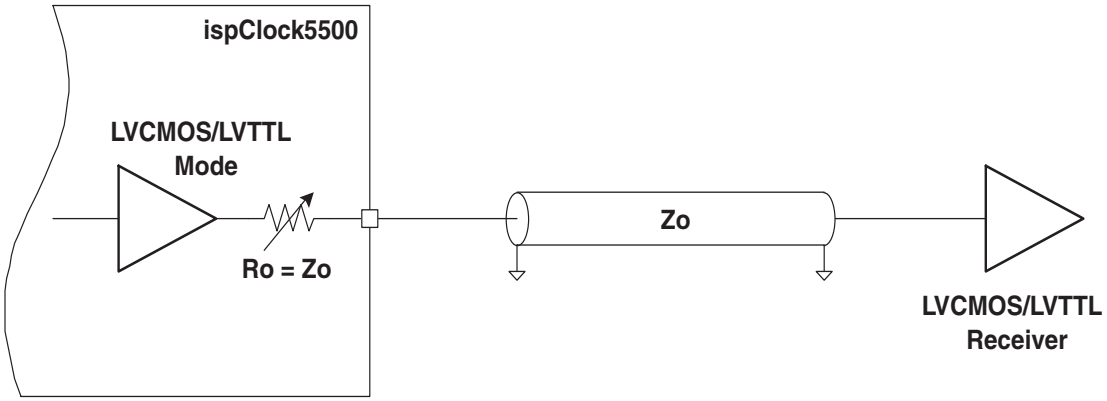
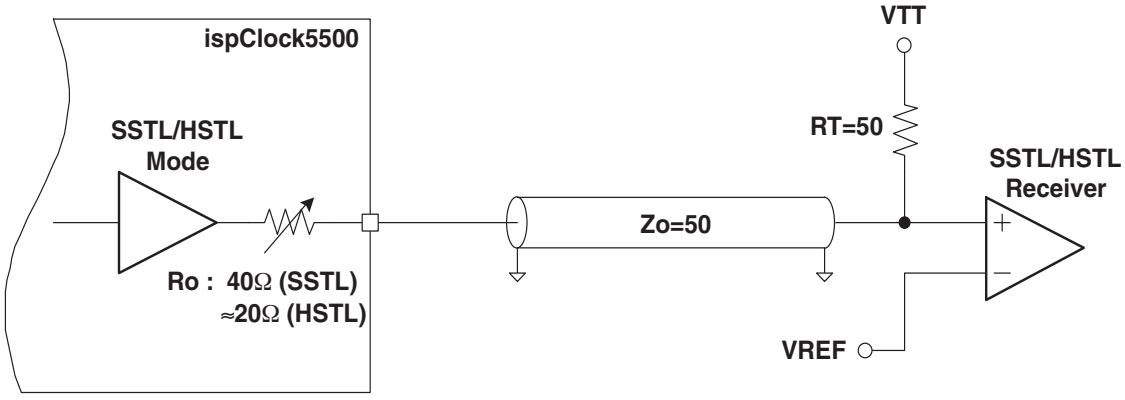


Figure 24 shows a typical configuration for the ispClock5500's output driver when configured to drive SSTL2, SSTL3, or HSTL loads. The ispClock5500's output impedance should be set to 40Ω for driving SSTL2 or SSTL3 loads and to the ≈20Ω setting for driving HSTL. The far end of the transmission line must be terminated to an appropriate VTT voltage through a 50Ω resistor.

Figure 24. Configuration for SSTL2, SSTL3, and HSTL Output Modes

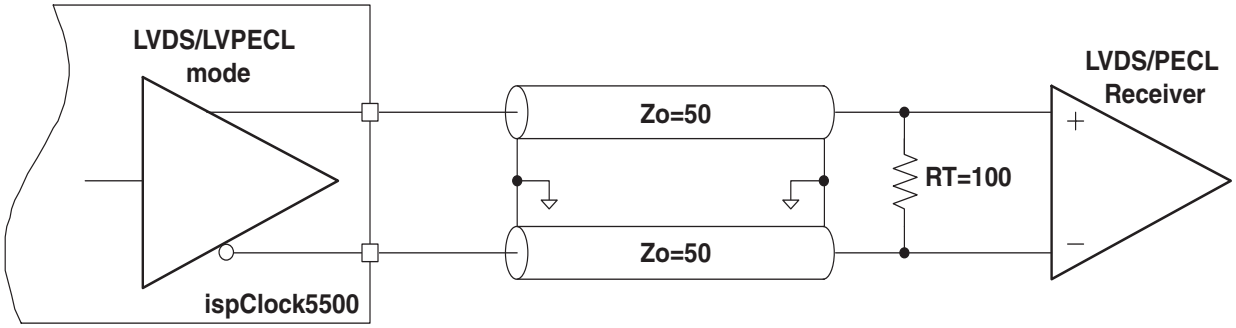


While supporting single-ended HSTL and SSTL outputs, the ispClock5500 does not support differential HSTL or SSTL. Although complementary HSTL and SSTL signals may be generated by using both an inverted output and a non-inverted output similarly configured, the resulting signal pair may not meet the JEDEC differential HSTL specifications for common mode voltage or crossover voltage.

Figure 25 shows a typical configuration for the ispClock5500's output driver when configured to drive LVDS or differential LVPECL loads. The ispClock5500's output impedance is disengaged when the driver is set to LVDS or

LVPECL mode. The far end of the transmission line must be terminated with a 100Ω resistor across the two signal lines.

Figure 25. Configuration for LVDS and LVPECL Output Modes



Note that when in LVPECL output mode, the ispClock5500's output driver provides an internal pull-down, unlike a typical bipolar LVPECL driver. For this reason no external pull-down resistors are necessary and the driver may be terminated with a single 100Ω resistor across the signal lines. For proper operation, pull-down resistors should NOT be used with the ispClock5500's LVPECL output mode.

Thermal Management

In applications where a majority of the ispClock5510 or ispClock5520's outputs are active and operating at or near maximum output frequency (320 MHz), package thermal limitations may need to be considered to ensure a successful design. Thermal characteristics of the packages employed by Lattice Semiconductor may be found in the document *Thermal Management* which may be obtained at www.latticesemi.com.

The maximum current consumption of the digital and analog core circuitry is approximately 157mA worst case (I_{CCD} + I_{CCA}), and each of the output banks may draw up to 35mA worst case (LVCMOS 3.3V, CL=18pF, f_{OUT}=320 MHz, both outputs in each bank enabled). This results in a total device dissipation:

$$P_{DMAX} = 3.3V \times (10 \times 35mA + 157mA) = 1.67W \quad (3)$$

With a maximum recommended operating junction temperature (T_{JOP}) of 115°C for an industrial grade device, the maximum allowable ambient temperature (T_{AMAX}) can be estimated as

$$T_{AMAX} = T_{JOP} - PD_{MAX} \times \Theta_{JA} = 115°C - 1.67W \times 35°C/W = 56°C \quad (4)$$

where Θ_{JA} = 35 °C/W for the 100 TQFP package and Θ_{JA} = 48 °C/W for the 48 TQFP package in still air.

The above analysis represents the worst-case scenario. Significant improvement in maximum ambient operating temperature can be realized with additional cooling. Providing a 200 LFM (Linear Feet per Minute) airflow reduces Θ_{JA} to 29°C/W, which results in a maximum ambient operating temperature of 66°C.

In practice, however, the absolute worst-case situation will be relatively rare, as not all outputs may be running at maximum output frequency in a given application. Additionally, if the internal VCO is operating at less than its maximum frequency (640MHz), it requires less current on the VCCD pin. In these situations, one can estimate the effective I_{CCO} for each bank and the effective I_{CCD} for the digital core functions based on output frequency and VCO frequency. Normalized curves relating current to operating frequency for these parameters may be found in the Typical Performance Characteristics section.

While it is possible to perform detailed calculations to estimate the maximum ambient operating temperature from operating conditions, some simpler rule-of-thumb guidance can also be obtained through the derating curves shown in Figure 26. The curves in Figure 26a show the maximum ambient operating temperature permitted when operating a given number of output banks at the maximum output frequency (320MHz). Note that it is assumed that both outputs in each bank are active.

Figure 26. Maximum Ambient Temperature vs. Number of Active Output Banks

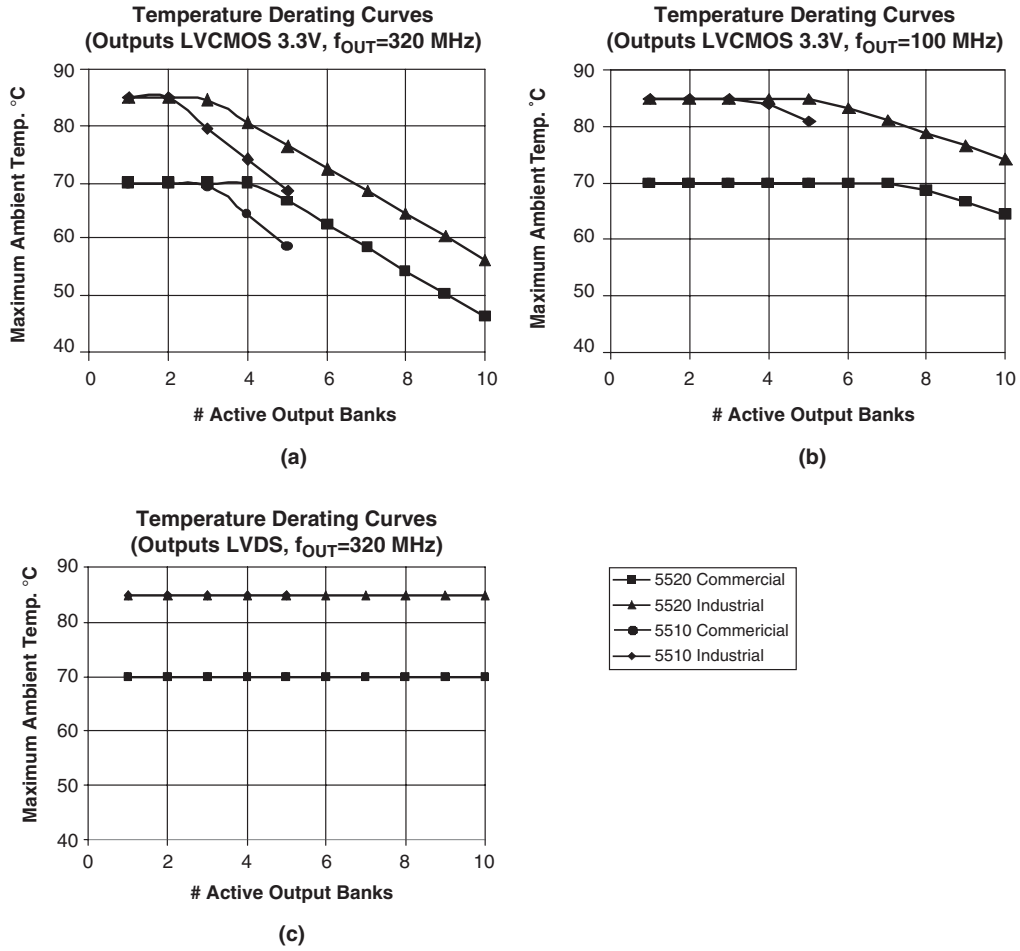


Figure 26b shows another derating curve, derived under the assumption that the output frequency is 100MHz. For many applications, 100MHz outputs will be a more realistic scenario. Comparing the maximum temperature limits of Figure 26b with Figure 26a, one can see that significantly higher operating temperatures are possible in LVCMOS 3.3V output mode with more outputs at 100MHz than at 320MHz.

The examples above described examples using LVCMOS 3.3V logic, which represents the maximum power dissipation case at higher frequencies. For optimal operation at very high frequencies (> 150 MHz) LVDS will often be the best choice from a signal integrity standpoint. For LVDS-configured outputs, the maximum ICCO current consumption per bank is low enough that both the ispClock5510 and ispClock5520 can operate all outputs at maximum frequency over their complete rated temperature range, as shown in Figure 26c.

Note that because of variations in circuit board mounting, construction, and layout, as well as convective and forced airflow present in a given design, actual die operating temperature is subject to considerable variation from that which may be theoretically predicted from package characteristics and device power dissipation.

Output Enable Controls

The ispClock5500 family provides the user with several options for enabling and disabling output pins, as well as suspending the output clock. In addition to providing the user with the ability to reduce the device's power consumption by turning off unused drivers, these features can also be used for functional testing purposes. The following inputs pins are used for output enable functions:

- $\overline{GOE}$ – global output enable
- $\overline{OEX}$, $\overline{OEY}$ – secondary output enable controls
- SGATE – synchronous output control

Additionally, internal E^2CMOS configuration bits are provided for the purpose of modifying the effects of these external control pins.

When $\overline{GOE}$ is HIGH, all output drivers are forced into a high-Z state, regardless of any internal configuration. When $\overline{GOE}$ is LOW, the output drivers may also be enabled or disabled on an individual basis, and optionally controlled by the $\overline{OEX}$ and $\overline{OEY}$ pins. Internal E^2CMOS configuration is used to establish whether the output driver is always enabled (when $\overline{GOE}$ pin is LOW), never enabled (permanently off), or selectively enabled by the state of either $\overline{OEX}$ or $\overline{OEY}$. Bringing $\overline{GOE}$ high will also disable the internal feedback driver and will result in a loss of lock.

Synchronous output gating is provided by ispClock5500 devices through the use of the SGATE pin. The SGATE pin does not disable the output driver, but merely forces the output to either a high or low state, depending on the output driver's polarity setting. If the output driver polarity is true, the output will be forced LOW when SGATE is brought LOW, while if it is inverted, the output will be forced HIGH. A primary feature of the SGATE function is that the clock output is enabled and disabled synchronous to the selected internal clock source. This prevents the generation of partial, 'runt', output clock pulses, which would otherwise occur with simple combinatorial gating schemes. The SGATE is available to all clock outputs and is selectable on a bank-by-bank basis.

Table 5 shows the behavior of the outputs for various combinations of the output enables, SGATE input, and E^2CMOS configuration.

Table 5. Clock Output Enable Functions

$\overline{GOE}$	$\overline{OEX}$	$\overline{OEY}$	E^2 Configuration	Output
X	X	X	Always OFF	High-Z
0	X	X	Always ON	Clock Out
0	0	X	Enable on OEX	Clock Out
0	1	X	Enable on OEX	High-Z
0	X	0	Enable on OEY	Clock Out
0	X	1	Enable on OEY	High-Z
1	X	X	n/a	High-Z

Table 6. SGATE Function

SGATE	Bank Controlled by SGATE?	Output Polarity	Output
X	NO	True	Clock
X	NO	Inverted	Inverted Clock
0	YES	True	LOW
0	YES	Inverted	HIGH
1	YES	True	Clock
1	YES	Inverted	Inverted Clock

Skew Control Units

Each of the ispClock5500's clock outputs is supported by a skew control unit which allows the user to insert an individually programmable delay into each output signal. This feature is useful when it is necessary to de-skew clock signals to compensate for physical length variations among different PCB clock paths.

Unlike the skew adjustment features provided in many competing products, the ispClock5500's skew adjustment feature provides exact and repeatable delays which exhibit extremely low channel-to-channel and device-to-device variation. This is achieved by deriving all skew timing from the VCO, which results in the skew increment being a linear function of the VCO period. For this reason, skews are defined in terms of 'time units' (TUs), which may be pro-

grammed by the user over a range of 0 to 15. The ispClock5500 family also supports both 'fine' and 'coarse' skew modes. In fine skew mode, the unit skew ranges from 195ps to 390 ps, while in the coarse skew mode unit skew varies from 390ps to 780ps. The value of one TU may be calculated from the VCO frequency (f_{vco}) by using the following expressions:

For fine skew mode, For coarse skew mode,

$$TU = \frac{1}{8f_{vco}} \qquad TU = \frac{1}{4f_{vco}} \tag{5}$$

When an output driver is programmed to support a differential output mode, a single skew setting is applied to both the BANKxA+ and BANKxB- signals. When the output driver is configured to support a single-ended output standard, each of the two single-ended outputs may be assigned independent skews.

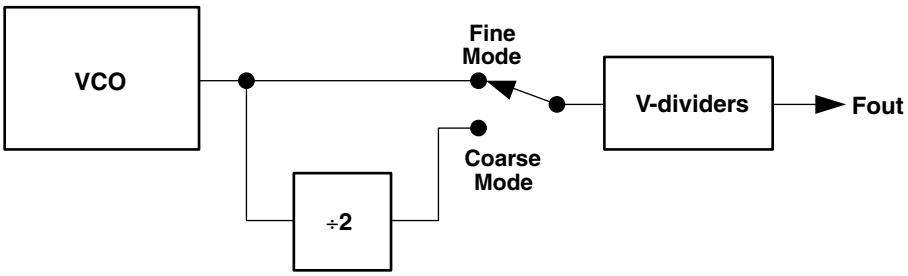
By using the internal feedback path, and programming a skew into the feedback skew control, it is possible to implement negative timing skews, in which the clock edge of interest appears at the ispClock5500's output before the corresponding edge is presented at the reference input. When the feedback skew unit is used in this way, the resulting negative skew is added to whatever skew is specified for each output. For example, if the feedback skew is set to 6TU, BANK1's skew is 8TU and BANK2's skew is 3TU, then BANK1's effective output skew will be 2TU (8TU-6TU), while BANK2's effective skew will be -3TU (3TU-6TU). This negative skew will manifest itself as BANK2's outputs appearing to lead the input reference clock, appearing as a negative propagation delay.

Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Coarse Skew Mode

The ispClock5500 family provides the user with the option of obtaining longer skew delays at the cost of reduced time resolution through the use of coarse skew mode. Coarse skew mode provides TU values ranging from 390ps (f_{VCO} = 640MHz) to 780ps (f_{VCO} = 320MHz), which is twice as long as those provided in fine skew mode. When coarse skew mode is selected, an additional divide-by-2 stage is effectively inserted between the VCO and the V-divider bank, as shown in Figure 27. When assigning divider settings in coarse skew mode, one must account for this additional divide-by-two so that the VCO still operates within its specified range (320-640MHz).

Figure 27. Additional Factor-of-2 Division in Coarse Mode



When one moves from fine skew mode to coarse skew mode with a given divider configuration, the VCO frequency will attempt to double to compensate for the additional divide-by-2 stage. Because the f_{VCO} range is not increased, however, one must modify the feedback path V-divider settings to bring f_{VCO} back into its specified operating range (320MHz to 640MHz). This can be accomplished by dividing all V-divider settings by two. All output frequencies will remain unchanged from what they were in fine mode. One drawback of moving from fine skew mode into coarse skew mode is that it may not be possible to maintain consistent output frequencies, as only those V-divider settings which are multiples of four (in fine mode) may be divided by two. For example, a V-divider setting of 24 will divide down to 12, which is also a legal V-divider setting, whereas an initial setting of 26 would divide down to 13, which is not a valid setting.

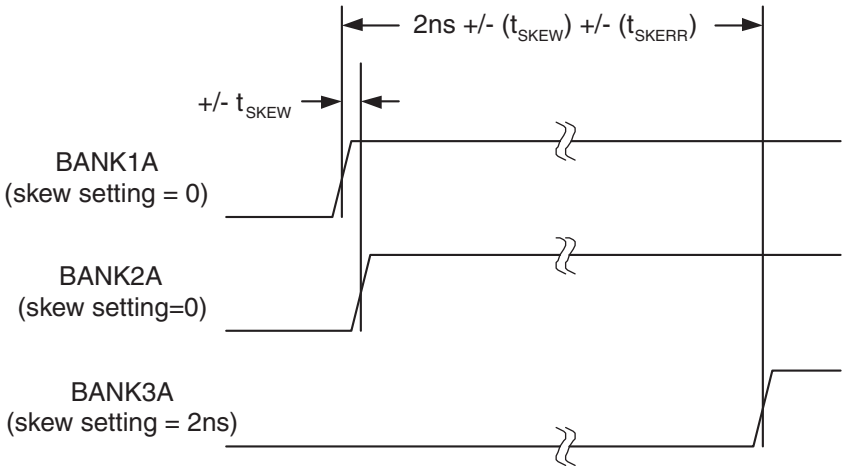
When one moves from coarse skew mode to fine skew mode, the extra divide-by-two factor is removed from between the VCO and the V-divider bank, halving the VCO's effective operating frequency. To compensate for this change, all of the V-dividers must be doubled to move the VCO back into its specified operating range and maintain consistent output frequencies. The only situation in which this may be a problem is when a V-divider initially in coarse mode has a value greater than 32, as the corresponding fine skew mode setting would be greater than 64, which is not supported.

Skew Matching and Accuracy

Understanding the various factors which relate to output skew is essential for realizing optimal skew performance in the ispClock5500 family of devices.

In the case where two outputs are identically configured, and driving identical loads, the maximum skew is defined by $t_{SKEW,}$ which is specified as a maximum of 50ps. In Figure 28 the Bank1A and BANK2A outputs show the skew error between two matched outputs.

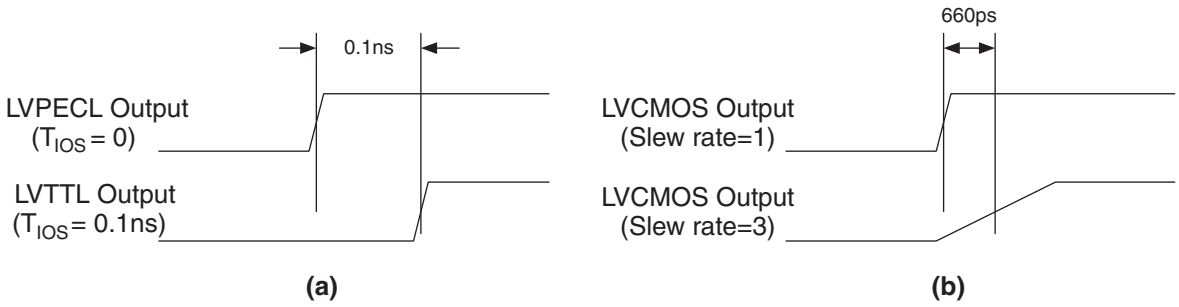
Figure 28. Skew Matching Error Sources



One can also program a user-defined skew between two outputs using the skew control units. Because the programmable skew is derived from the VCO frequency, as described in the previous section, the absolute skew is very accurate. The typical error for any non-zero skew setting is given by the t_{SKERR} specification. For example, if one is in fine skew mode with a VCO frequency of 500MHz, and selects a skew of 8TU, the realized skew will be 2ns, which will typically be accurate to within +/-30 ps. An example of error vs. skew setting can be found in the chart 'Typical Skew Error vs. Setting' in the typical performance characteristics section. Note that this parameter adds to output-to-output skew error only if the two outputs have *different* skew settings. The Bank1A and Bank3A outputs in Figure 28 show how the various sources of skew error stack up in this case. Note that if two or more outputs are programmed to the same skew setting, then the contribution of the t_{SKERR} skew error term does not apply.

When outputs are configured or loaded differently, this also has an effect on skew matching. If an output is set to support a different logic type, this can be accounted for by using the t_{IOO} output adders specified in the Table 'Switching Characteristics'. That table specifies the additional skew added to an output using LVPECL as a baseline. For instance, if one output is specified as LVTTL (t_{IOO} = 0.1ns), and another output is specified as LVPECL (t_{IOO} = 0ns), then one could expect 0.1ns of additional skew between the two outputs. This timing relationship is shown in Figure 29a.

Figure 29. Output Timing Adders for Logic Type (a) and Output Slew Rate (b)



Similarly, when one changes the slew rate of an output, the output slew rate adders (t_{IOS}) can be used to predict the resulting skew. In this case, the fastest slew setting (1) is used as the baseline against which other slews are measured. For example, in the case of outputs configured to the same logic type (e.g. LVCMOS 1.8V), if one output is set to the fastest slew rate (1, t_{IOS} = 0ps), and another set to slew rate 3 (t_{IOS} = 660ps), then one could expect 660ps of skew between the two outputs, as shown in Figure 29b.

Other Features

Profile Select

The ispClock5500 stores all internal configuration data in on-board E^2CMOS memory. Up to four independent configuration profiles may be stored in each device. The choice of which configuration profile is to be active is specified thought the profile select inputs PS0 and PS1, as shown in Table 7.

Table 7. Profile Select Function

PS1	PS0	Active Profile
0	0	Profile 0
0	1	Profile 1
1	0	Profile 2
1	1	Profile 3

Each profile controls the following internal configuration items:

- M divider setting
- N divider setting
- V divider settings
- PLL Loop filter settings
- Output Skew settings
- Internal feedback delay compensation

The following settings are independent of the selection of active profile and will apply regardless of which profile is selected:

- Input logic configuration
  - – Logic family
  - – Input impedance
- Output bank logic configuration
  - – Logic family
  - – V-Divider signal source
  - – Enable/SGATE control options
  - – Output Impedance
  - – Slew rate

– Signal Inversion

- V-Divider to be used as feedback source
- Internal feedback delay compensation
- Fine/Coarse skew mode selection
- UES string

If any of the above items are modified, the change will apply across all profiles. In some cases this may cause unanticipated behavior. If multiple profiles are used in a design, the suitability of the profile independent settings must be considered with respect to each of the individual profiles.

When a profile is changed by modifying the values of the PS0 and PS1 inputs, it is necessary to assert a RESET signal to the ispClock5500 to restart the PLL and resynchronize all the internal dividers.

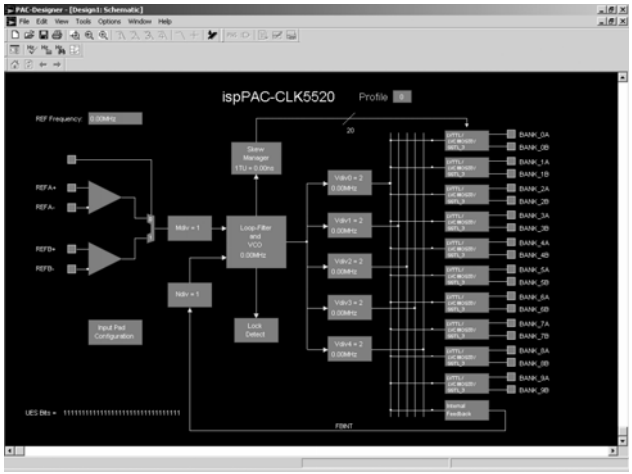
RESET and Power-up Functions
To ensure proper PLL startup and synchronization of outputs, the ispClock5500 provides both internally generated and user-controllable external reset signals. An internal reset is generated whenever the device is powered up. An external reset may be applied by asserting a logic HIGH at the RESET pin. Please note that the RESET pin does not have an internal pull-up or pull-down resistor associated with it and should be tied LOW if not used. Asserting RESET resets all internal dividers, and will cause the PLL to lose lock. On losing lock, the VCO frequency will begin dropping. The length of time required to regain lock is related to the length of time for which RESET was asserted. Output phase relationships among the outputs may not be valid until the ispClock5500 asserts its LOCK output.

When the ispClock5500 begins operating from initial power-on, the VCO starts running at a very low frequency (<100 MHz) which gradually increases as it approaches a locked condition. To prevent invalid outputs from being applied to the rest of the system, it is recommended that either the SGATE, $\overline{OEX}$, or $\overline{OEY}$ pins be used to control the outputs based on the status of the LOCK pin. Holding the SGATE pin LOW during power-up will result in the BANK outputs being asserted HIGH or LOW (depending on inversion status) until SGATE is brought HIGH. Asserting $\overline{OEX}$ or $\overline{OEY}$ high will result in the BANK outputs being held in a high-impedance state until the $\overline{OEX}$ or $\overline{OEY}$ pin is pulled LOW. One should not use the $\overline{GOE}$ pin to control the outputs in anticipation of LOCK status, as holding $\overline{GOE}$ HIGH also disables internal feedback and will prevent the device from ever achieving lock.

Software-Based Design Environment

Designers can configure the ispClock5500 using Lattice's PAC-Designer software, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispClock5500. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available on the Lattice web site at www.latticesemi.com. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation. The PAC-Designer schematic window, shown in Figure 30 provides access to all configurable ispClock5500 elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved and downloaded to devices.

Figure 30. PAC-Designer Design Entry Screen (ispClock5520)



In-System Programming

The ispClock5500 is an In-System Programmable (ISP™) device. This is accomplished by integrating all E^{2}CMOS configuration control logic on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^{2}CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispClock5500 instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

A user electronic signature (UES) feature is included in the E^{2}CMOS memory of the ispClock5500. This consists of 32 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Electronic Security

An electronic security “fuse” (ESF) bit is provided in every ispClock5500 device to prevent unauthorized readout of the E^{2}CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can not be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Production Programming Support

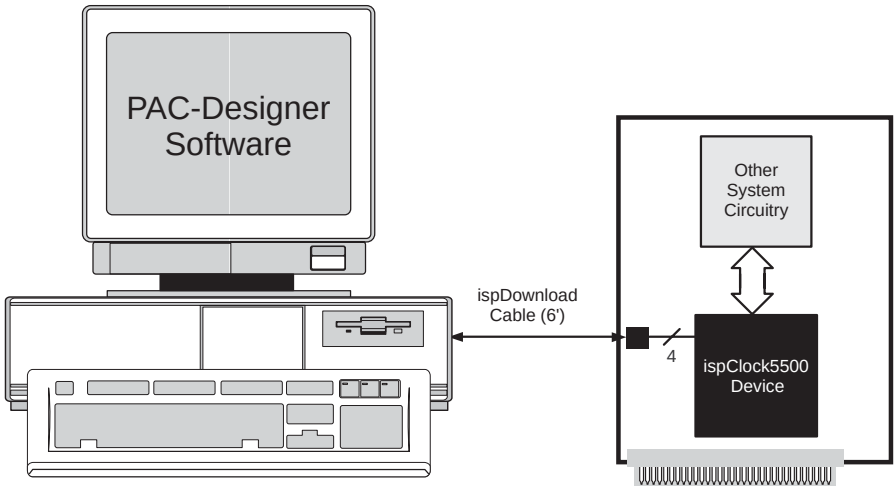
Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user’s specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

Evaluation Fixture

Included in the basic ispClock5500 Design Kit is an engineering prototype board that can be connected to the parallel port of a PC using a Lattice ispDOWNLOAD® cable. It demonstrates proper layout techniques for the ispClock5500 and can be used in real time to check circuit operation as part of the design process. Input and output connections (SMA connectors for all RF signals) are provided to aid in the evaluation of the ispClock5500 for a given application. (Figure 31).

Part Number	Description
PAC-SYSTEMCLK5520	Complete system kit, evaluation board, ispDOWNLOAD cable and software.
PACCLK5520-EV	Evaluation board only, with components, fully assembled.

Figure 31. Download from a PC



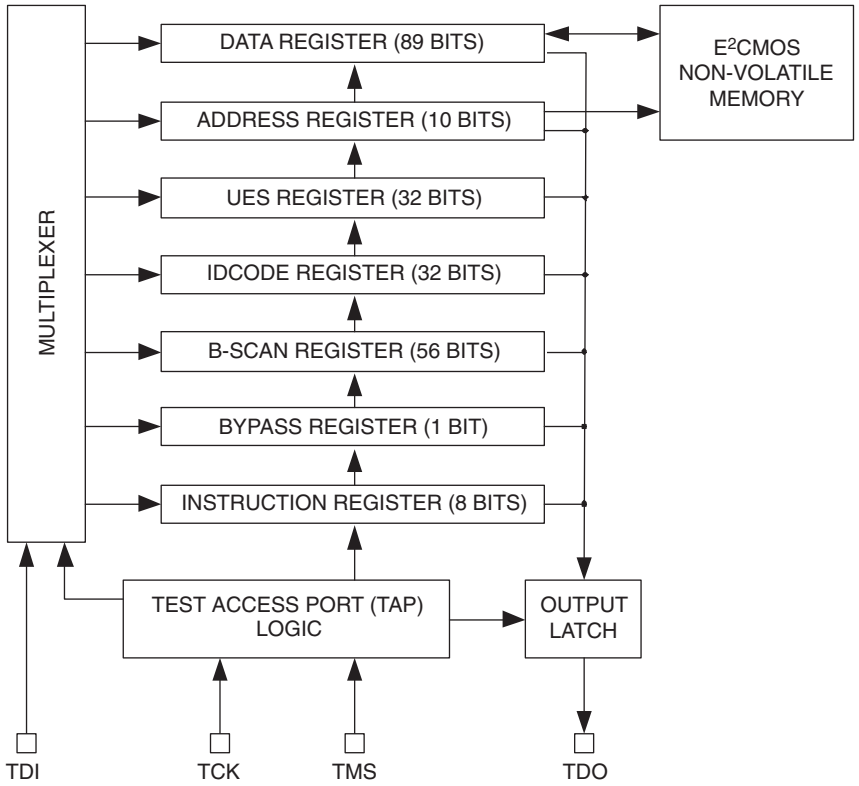
IEEE Standard 1149.1 Interface (JTAG)

Serial Port Programming Interface Communication with the ispClock5500 is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispClock5500 both as a serial programming interface, and for boundary scan test purposes. A brief description of the ispClock5500 JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990 (which now includes IEEE Std. 1149.1a-1993).

Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispClock5500. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E^2CMOS cells. It is these non-volatile cells that store the configuration or the ispClock5500. A set of instructions are defined that access all data registers and perform other internal control operations. For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. Figure 32 shows how the instruction and various data registers are organized in an ispClock5500.

Figure 32. ispClock5500 TAP Registers

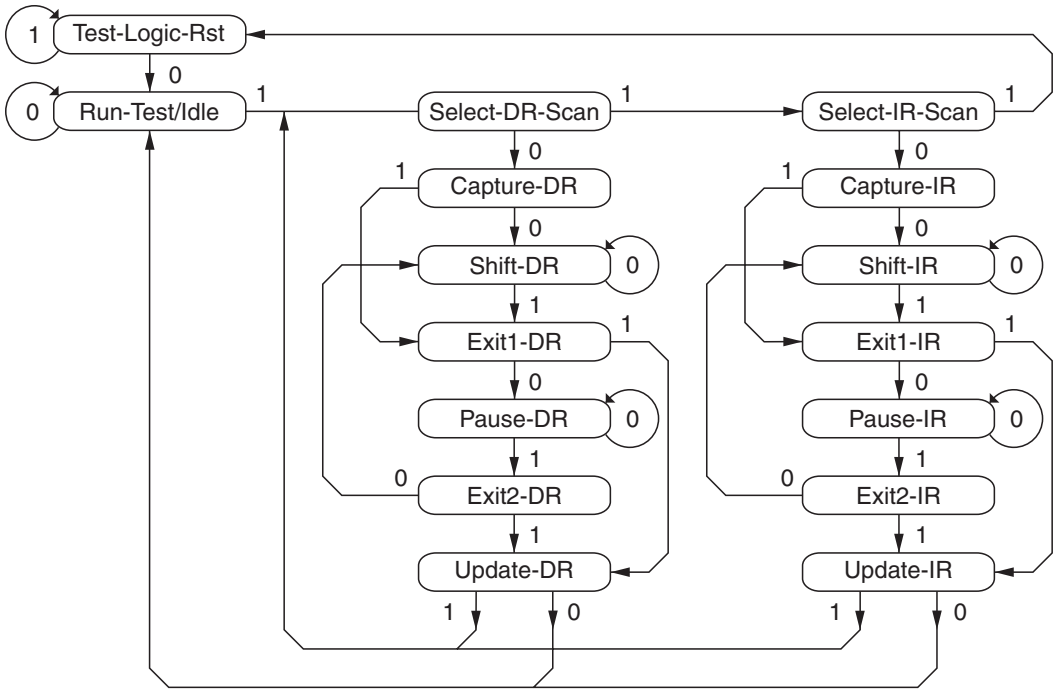


TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the TMS input as shown in Figure 33. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run-

Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

Figure 33. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain. From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manu-

facturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispClock5000 contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified. For ispClock5000, the instruction word length is eight bits. All ispClock5000 instructions available to users are shown in Table 8.

The following table lists the instructions supported by the ispClock5500 JTAG Test Access Port (TAP) controller:

Table 8. ispClock5500 TAP Instruction Table

Instruction	Code	Description
EXTEST	0000 0000	External Test.
ADDRESS_SHIFT	0000 0001	Address register (10 bits)
DATA_SHIFT	0000 0010	Address column data register (89 bits)
BULK_ERASE	0000 0011	Bulk Erase
PROGRAM	0000 0111	Program column data register to E^2
PROGRAM_SECURITY	0000 1001	Program Electronic Security Fuse
VERIFY	0000 1010	Verify column
DISCHARGE	0001 0100	Fast VPP Discharge
PROGRAM_ENABLE	0001 0101	Enable Program Mode
IDCODE	0001 0110	Address Manufacturer ID code register (32 bits)
USERCODE	0001 0111	Read UES data from E^2 and addresses UES register (32 bits)
PROGRAM_USERCODE	0001 1010	Program UES register into E^2
PROGRAM_DISABLE	0001 1110	Disable Program Mode
HIGHZ	0001 1000	Force all outputs to High-Z state
SAMPLE/PRELOAD	0001 1100	Capture current state of pins to boundary scan register
CLAMP	0010 0000	Drive I/Os with boundary scan register
USER_LOGIC_RESET	0010 0010	Resets User Logic
INTEST	0010 1100	Performs in-circuit functional testing of device.
ERASE DONE	0010 0100	Erases the ‘Done’ bit only
PROG_INCR	0010 0111	Program column data register to E^2 and auto-increment address register
VERIFY_INCR	0010 1010	Load column data register from E^2 and auto-increment address register
PROGRAM_DONE	0010 1111	Programs the ‘Done’ Bit
NOOP	0011 0000	Functions Similarly to CLAMP instruction
BYPASS	1xxx xxxx	Bypass - Connect TDO to TDI

BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispClock5500. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (111111).

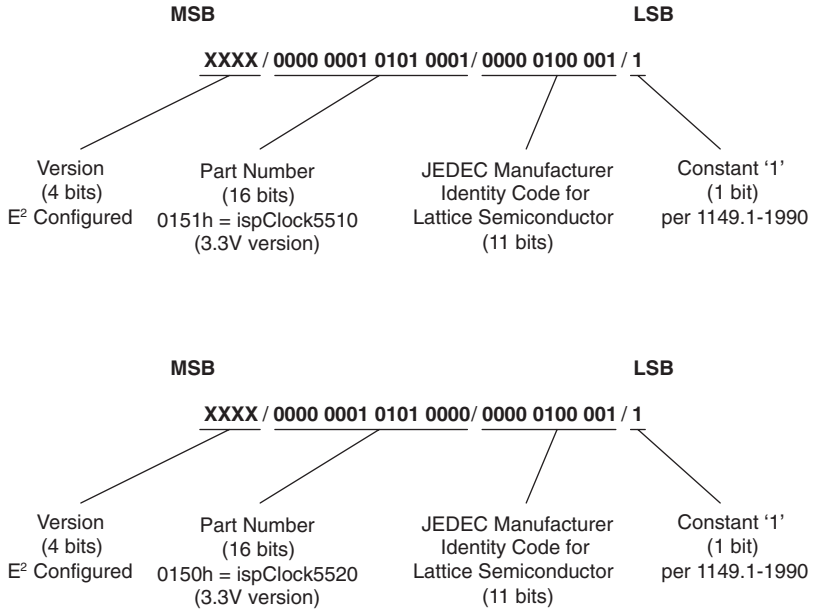
The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The bit code for this instruction is defined by Lattice as shown in Table 8.

The **EXTEST** (external test) instruction is required and will place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispClock5500 and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device

type and version code (Figure 34). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 8.

Figure 34. ispClock5500 Family ID Codes



In addition to the four instructions described above, there are 20 unique instructions specified by Lattice for the ispClock5520. These instructions are primarily used to interface to the various user registers and the E^2CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device, including boundary scan operations. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 8.

PROGRAM_ENABLE – This instruction enables the ispClock5500's programming mode.

PROGRAM_DISABLE – This instruction disables the ispClock5500's programming mode.

BULK_ERASE – This instruction will erase all E^2CMOS bits in the device, including the UES data and electronic security fuse (ESF). A bulk erase instruction must be issued before reprogramming a device. The device must already be in programming mode for this instruction to execute.

ADDRESS_SHIFT – This instruction shifts address data into the address register (10 bits) in preparation for either a PROGRAM or VERIFY instruction.

DATA_SHIFT – This instruction shifts data into or out of the data register (90 bits), and is used with both the PROGRAM and VERIFY instructions.

PROGRAM – This instruction programs the contents of the data register to the E^2CMOS memory column pointed to by the address register. The device must already be in programming mode for this instruction to execute.

PROG_INCR – This instruction first programs the contents of the data register into E^2CMOS memory column pointed to by the address register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

PROGRAM_SECURITY – This instruction programs the electronic security fuse (ESF). This prevents data other than the ID code and UES strings from being read from the device. The electronic security fuse may only be reset by issuing a BULK_ERASE command. The device must already be in programming mode for this instruction to execute.

VERIFY – This instruction loads data from the E^2CMOS array into the column register. The data may then be shifted out. The device must already be in programming mode for this instruction to execute.

VERIFY_INCR – This instruction copies the E^2CMOS column pointed to by the address register into the data column register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispClock5500 for a read cycle.

PROGRAM_USERCODE – This instruction writes the contents of the UES register (32 bits) into E^2CMOS memory. The device must already be in programming mode for this instruction to execute.

USERCODE – This instruction both reads the UES string (32 bits) from E^2CMOS memory into the UES register and addresses the UES register so that this data may be shifted in and out.

HIGHZ – This instruction forces all outputs into a High-Z state.

CLAMP – This instruction drives I/O pins with the contents of the boundary scan register.

USER_LOGIC_RESET – This instruction resets all user-accessible logic, similar to asserting a HIGH on the RESET pin.

INTEST – This instruction performs in-circuit functional testing of the device.

ERASE_DONE – This instruction erases the 'DONE' bit only. This instruction is used to disable normal operation of the device while in programming mode until a valid configuration pattern has been programmed.

PROGRAM_DONE – This instruction programs the 'DONE' bit only. This instruction is used to enable normal device operation after programming is complete.

NOOP – This instruction behaves similarly to the CLAMP instruction.

Pin Descriptions

Pin Name	Description	Pin Type	Pin Number	
			ispClock5510 48 TQFP	ispClock5520 100 TQFP
VCCO_0	Output Driver '0' VCC	Power	1	3
VCCO_1	Output Driver '1' VCC	Power	5	7
VCCO_2	Output Driver '2' VCC	Power	9	11
VCCO_3	Output Driver '3' VCC	Power	25	15
VCCO_4	Output Driver '4' VCC	Power	29	19
VCCO_5	Output Driver '5' VCC	Power	—	51
VCCO_6	Output Driver '6' VCC	Power	—	55
VCCO_7	Output Driver '7' VCC	Power	—	59
VCCO_8	Output Driver '8' VCC	Power	—	63
VCCO_9	Output Driver '9' VCC	Power	—	67
GNDO_0	Output Driver '0' Ground	GND	4	6
GNDO_1	Output Driver '1' Ground	GND	8	10
GNDO_2	Output Driver '2' Ground	GND	12	14
GNDO_3	Output Driver '3' Ground	GND	28	18
GNDO_4	Output Driver '4' Ground	GND	32	22
GNDO_5	Output Driver '5' Ground	GND	—	54
GNDO_6	Output Driver '6' Ground	GND	—	58
GNDO_7	Output Driver '7' Ground	GND	—	62
GNDO_8	Output Driver '8' Ground	GND	—	66
GNDO_9	Output Driver '9' Ground	GND	—	70
BANK_0A	Clock Output driver 0, 'A' output	Output	3	5
BANK_0B	Clock Output driver 0, 'B' output	Output	2	4
BANK_1A	Clock Output driver 1, 'A' output	Output	7	9
BANK_1B	Clock Output driver 1, 'B' output	Output	6	8
BANK_2A	Clock Output driver 2, 'A' output	Output	11	13
BANK_2B	Clock Output driver 2, 'B' output	Output	10	12
BANK_3A	Clock Output driver 3, 'A' output	Output	27	17
BANK_3B	Clock Output driver 3, 'B' output	Output	26	16
BANK_4A	Clock Output driver 4, 'A' output	Output	31	21
BANK_4B	Clock Output driver 4, 'B' output	Output	30	20
BANK_5A	Clock Output driver 5, 'A' output	Output	—	53
BANK_5B	Clock Output driver 5, 'B' output	Output	—	52
BANK_6A	Clock Output driver 6, 'A' output	Output	—	57
BANK_6B	Clock Output driver 6, 'B' output	Output	—	56
BANK_7A	Clock Output driver 7, 'A' output	Output	—	61
BANK_7B	Clock Output driver 7, 'B' output	Output	—	60
BANK_8A	Clock Output driver 8, 'A' output	Output	—	65
BANK_8B	Clock Output driver 8, 'B' output	Output	—	64
BANK_9A	Clock Output driver 9, 'A' output	Output	—	69
BANK_9B	Clock Output driver 9, 'B' output	Output	—	68
VCCA	Analog VCC for PLL circuitry	Power	13	30
GNDA	Analog Ground for PLL circuitry	GND	14	31

Pin Descriptions (Continued)

Pin Name	Description	Pin Type	Pin Number	
			ispClock5510 48 TQFP	ispClock5520 100 TQFP
VCCD	Digital Core VCC	Power	24, 33	47, 71
GNDD	Digital GND	GND	15, 16, 17, 23, 48	32, 33, 34, 35, 36, 37, 46, 93
VCCJ	JTAG interface VCC	Power	36	74
REFA+	Clock Reference A positive input	Input	18	38
REFA-	Clock Reference A negative input	Input	19	39
REFB+	Clock Reference B positive input	Input	—	42
REFB-	Clock Reference B negative input	Input	—	41
REFSEL	Clock Reference Select input (LVCMOS)	Input[1]	—	43
REFVTT	Termination voltage for reference inputs	Power	20	40
TDO	JTAG TDO Output line	Output	35	73
TDI	JTAG TDI Input line	Input[2]	39	84
TCK	JTAG Clock Input	Input	38	83
TMS	JTAG Mode Select	Input[2]	37	82
$\overline{LOCK}$	PLL Lock indicator, LOW indicates PLL lock	Output	34	72
SGATE	Synchronous output gate	Input[1]	40	85
$\overline{GOE}$	Global Output Enable	Input[1]	42	87
$\overline{OEX}$	Output Enable 1	Input	21	44
$\overline{OEY}$	Output Enable 2	Input	22	45
PS0	Profile Select 0	Input[1]	44	89
PS1	Profile Select 1	Input[1]	43	88
PLL_BYPASS	PLL Bypass	Input[1]	47	92
RESET	Reset PLL	Input	41	86
TEST1	Test Input 1 - connect to GNDD	Input	46	91
TEST2	Test Input 2 - connect to GNDD	Input	45	90
n/c	No internal connection	n/a	—	1, 2, 23, 24, 25, 26, 27, 28, 29, 48, 49, 50, 75, 76, 77, 78, 79, 94, 97, 98, 99, 100
Reserved	Factory use only - Do not connect	n/a	—	80, 81, 95, 96

1. Internal pull-down resistor.
2. Internal pull-up resistor.

Detailed Pin Descriptions

VCCO_[0..9], GNDO_[0..9] – These pins provide power and ground for each of the output banks. In the case when an output bank is unused, its corresponding VCCO pin may be left unconnected or preferably should be tied to ground. ALL GNDO pins should be tied to ground regardless of whether the associated bank is used or not. When a bank is used, it should be individually bypassed with a capacitor in the range of 0.01 to 0.1uF as close to its VCCO and GNDO pins as is practical.

BANK_[0..9]A, BANK_[0..9]B – These pins provide clock output signals. The choice of output divider (V0-V4) and output driver type (CMOS, LVDS, SSTL, etc.) may be selected on a bank-by-bank basis. When the outputs are configured as pairs of single-ended outputs, output impedance and slew rate may be selected on an output-by-output basis.

VCCA, GNDA – These pins provide analog supply and ground for the ispClock5500 family's internal analog circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity, it is suggested that the supply to the VCCA pin be isolated from other circuitry with a ferrite bead.

VCCD, GNDD – These pins provide digital supply and ground for the ispClock5500 family's internal digital circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. to improve noise immunity it is suggested that the supply to the VCCD pins be isolated with ferrite beads.

VCCJ – This pin provides power and a reference voltage for use by the JTAG interface circuitry. It may be set to allow the ispClock5500 family devices to function in JTAG chains operating at voltages differing from VCCD.

REFA+, REFA-, REFB+, REFB- – These input pins provide the inputs for clock signals, and can accommodate either single ended or differential signal protocols by using either just the '+' pins, or both the '+' and '-' pins. Two sets of inputs are provided to accommodate the use of different signal sources and redundant clock sources.

REFSEL – This input pin is used to select which clock input pair (REFA+/- or REB+/-) is selected for use as the reference input. When REFSEL=0, REFA+/- is used, and when REFSEL=1, REFB+/- is used.

REFVTT – This pin is used to provide a termination voltage for the reference inputs when they are configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases.

TDO, TDI, TCK, TMS – These pins comprise the ispClock5500 device's JTAG interface. The signal levels for these pins are determined by the selection of the VCCJ voltage.

$\overline{\text{LOCK}}$ – This open drain output pin indicates that the device's PLL is in a locked condition when it goes low.

SGATE – This input pin provides a synchronous gating function for the outputs, which may be enabled on a bank-by-bank basis. When the synchronous gating function is enabled for a given bank, that bank's outputs will output a clock signal when the SGATE pin is HIGH, and will drive a constant HIGH or LOW when the SGATE pin is LOW. Synchronous gating ensures that when the state of SGATE is changed, no partial clock pulses will appear at the outputs.

$\overline{\text{OEX}}$, $\overline{\text{OEY}}$ – These pins are used to enable the outputs or put them into a high-impedance condition. Each output may be set so that it is always on, always off, enabled by $\overline{\text{OEX}}$ or enabled by $\overline{\text{OEY}}$.

$\overline{\text{GOE}}$ – Global output enable. This pin drives all outputs to a high-impedance state when it is pulled HIGH. $\overline{\text{GOE}}$ also controls the internal feedback buffer, so that bringing $\overline{\text{GOE}}$ high will cause the PLL to lose lock.

PS0, PS1 – These input pins are used to select one of four user-defined configuration profiles for the device.

PLL_BYPASS – When this pin is pulled LOW, the V-dividers are driven from the output of the device's VCO, and the device behaves as a phase-locked loop. When this pin is pulled HIGH, the V-dividers are driven directly from the output of the M-divider, and the PLL functions are effectively bypassed.

RESET – When this pin is pulled HIGH, all on-board counters are reset, and lock is lost.

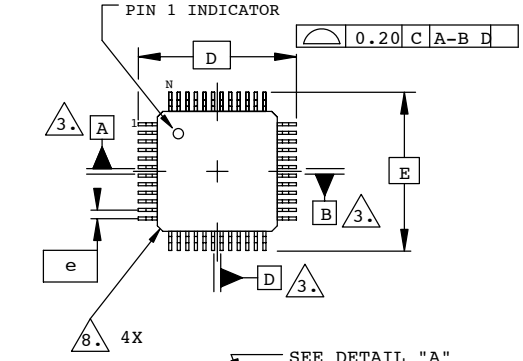
TEST1,TEST2 – These pins are used for factory test functions, and should always be tied to ground.

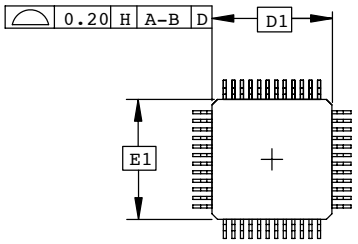
n/c – These pins have no internal connection. We recommend that they be left unconnected.

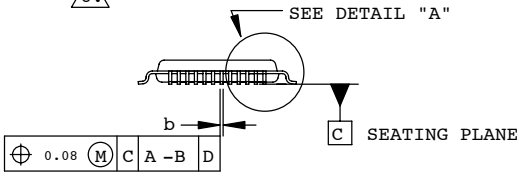
RESERVED – These pins are reserved for factory use and should be left unconnected.

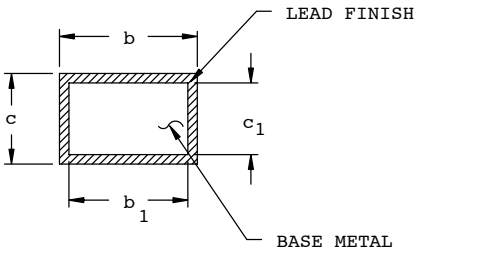
Package Diagrams

48-Pin TQFP (Dimensions in Millimeters)

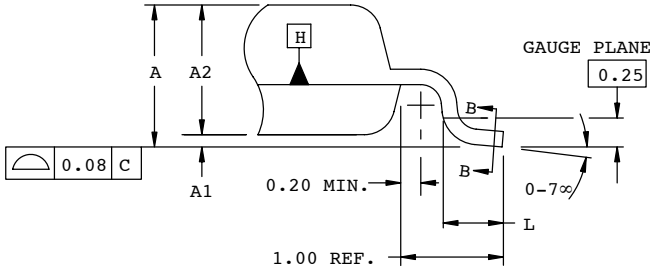








SECTION B - B



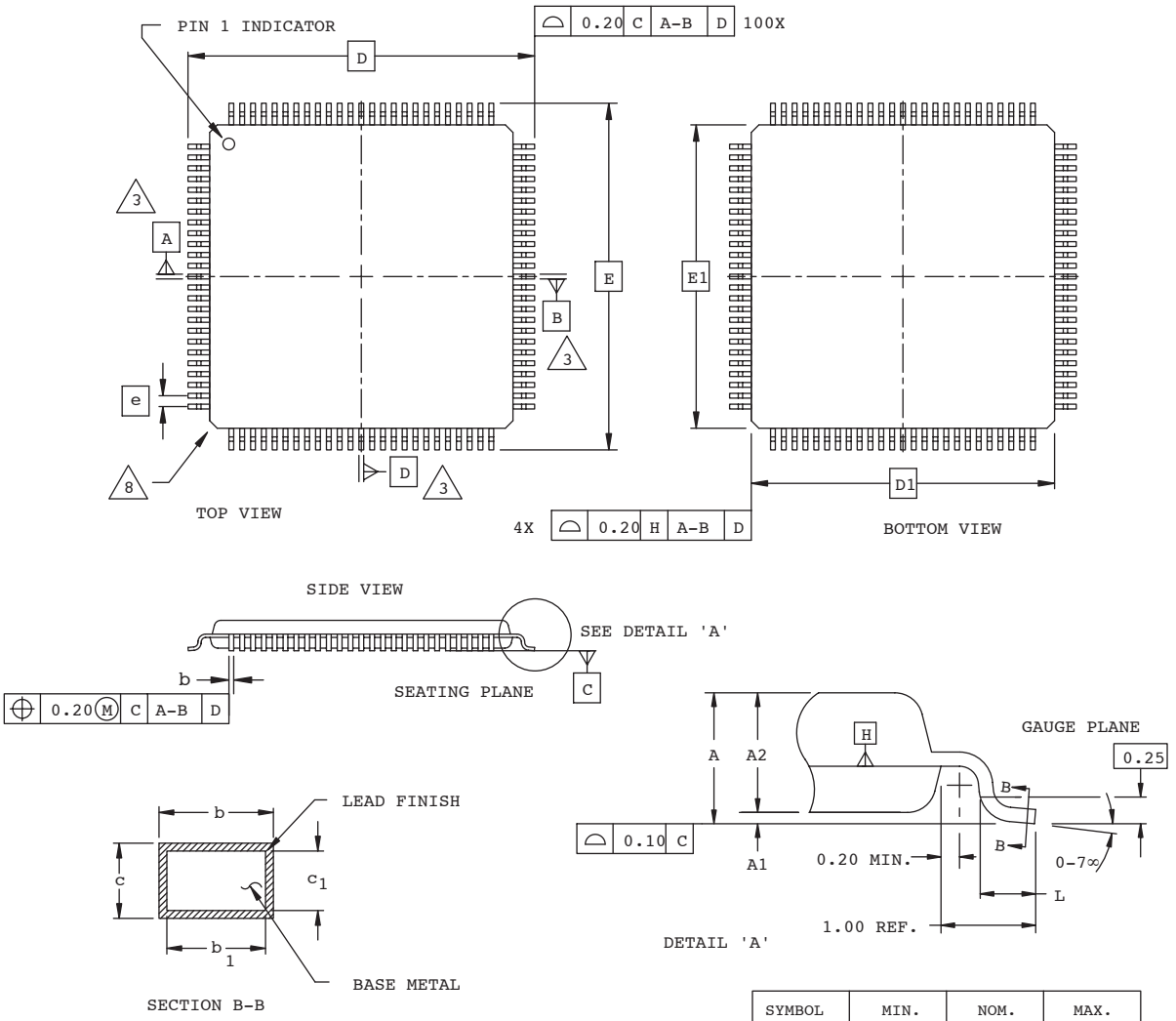
DETAIL "A"

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
5. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MM.
6. SECTION B-B:
   THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.
7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
N	48		
e	0.50 BSC		
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.13	0.16

100-Pin TQFP (Dimensions in Millimeters)



SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		16.00 BSC	
D1		14.00 BSC	
E		16.00 BSC	
E1		14.00 BSC	
L	0.45	0.60	0.75
N		100	
e		0.50 BSC	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.13	0.16

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
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7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
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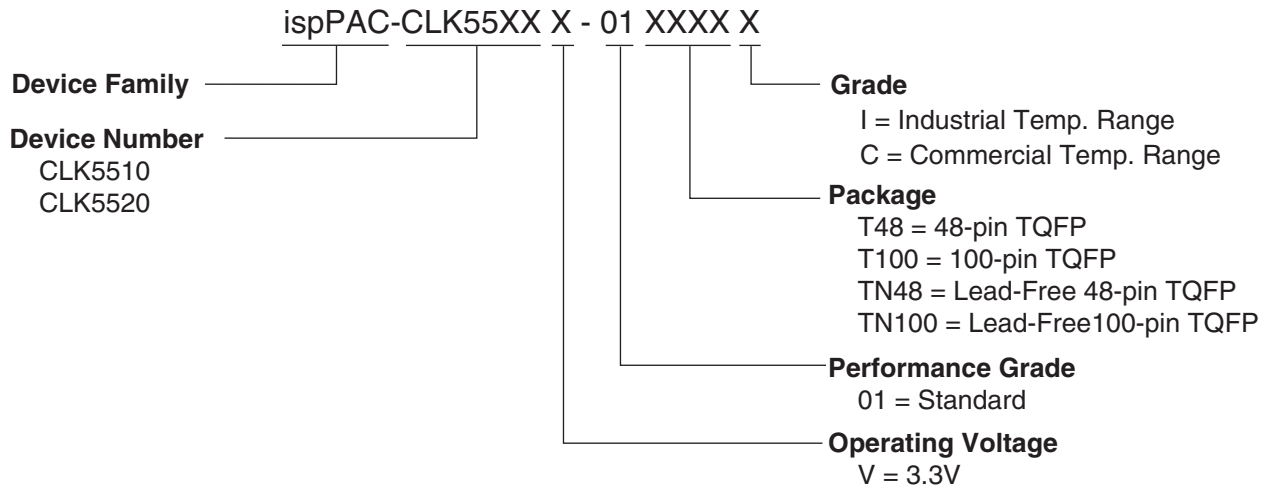
Part Number Description



Ordering Information

Conventional Packaging

Commercial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5510V-01T48C	10	3.3V	TQFP	48
ispPAC-CLK5520V-01T100C	20	3.3V	TQFP	100

Industrial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5510V-01T48I	10	3.3V	TQFP	48
ispPAC-CLK5520V-01T100I	20	3.3V	TQFP	100

Lead-Free Packaging

Commercial

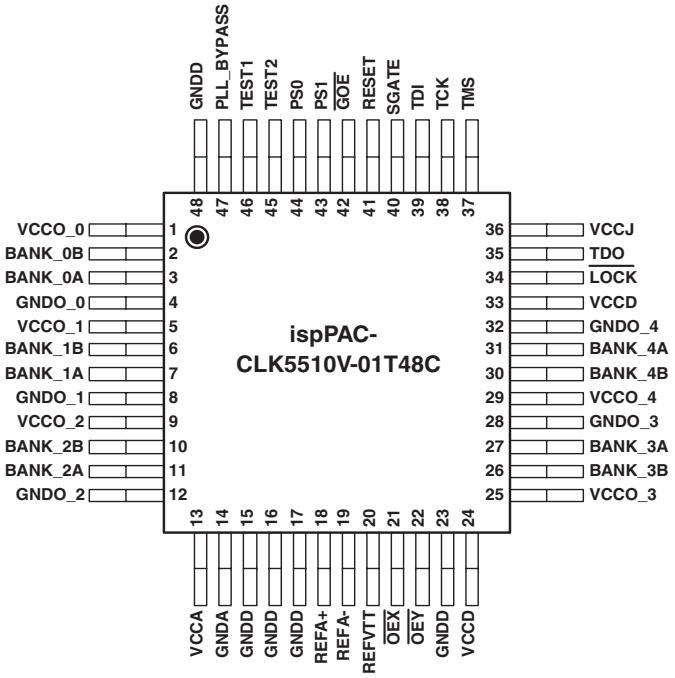
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5510V-01TN48C	10	3.3V	Lead-Free TQFP	48
ispPAC-CLK5520V-01TN100C	20	3.3V	Lead-Free TQFP	100

Industrial

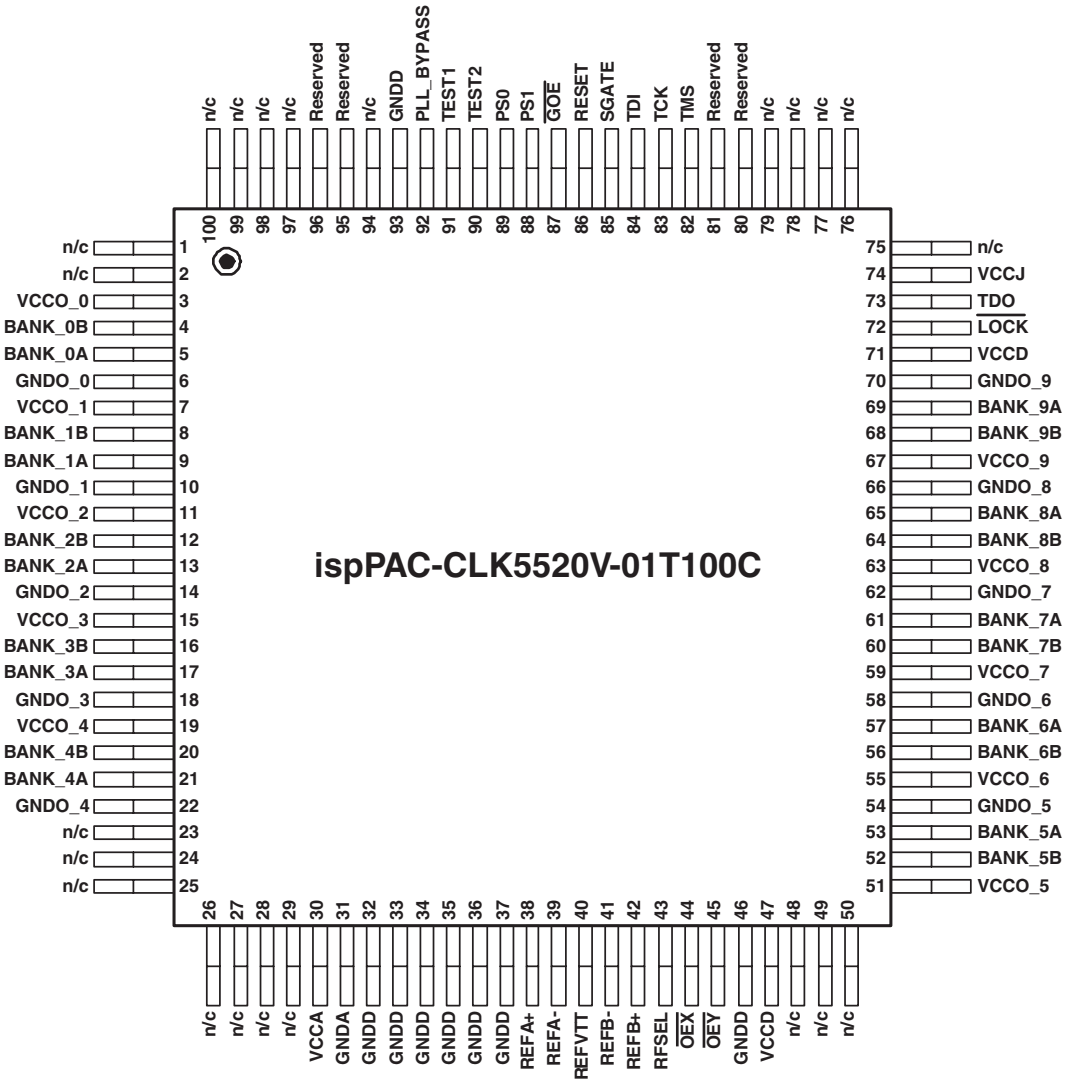
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5510V-01TN48I	10	3.3V	Lead-Free TQFP	48
ispPAC-CLK5520V-01TN100I	20	3.3V	Lead-Free TQFP	100

Package Options

ispClock5510: 48-pin TQFP



ispClock5520: 100-pin TQFP



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