THE DATASHEET OF

LM97937RMER

LM97937 Dual 370 MSPS Receiver and Feedback IC With SNRBoost, Bit-Burst, and JESD204B Outputs

Check for Samples: LM97937

FEATURES

- **Conversion Rate: 370 MSPS**
- **1.7 V_{P-P} Input Full Scale Range**
- **SNRBoost Noise Shaping with 100 MHz Bandpass Bandwidth**
  - **Noise Spectral Density: –152.0 dBFS/Hz**
  - **Programmable Passband Center Frequency**
- **Bit-Burst Resolution Switching**
  - **Resolutions: 9-bit (Low-Res), 14-bit (Hi-Res)**
  - **Hi-Res Noise Density: –152.7 dBFS/Hz**
  - **Programmable Burst Configurations**
- **Performance**
  - **Input: 150 MHz, –3 dBFS**
    - **SNR (SNRBoost): 71.6 dBFS**
    - **SNR (Bit-Burst): 69.6 dBFS**
    - **SFDR: 88 dBFS**
    - **non-HD2/HD3 SPUR: –90 dBFS**
- **Power Dissipation: 876 mW/channel**
- **Buffered Analog Inputs**
- **On-chip Precision Reference Without External Bypassing**
- **Input Sampling Clock Divider with Phase Synchronization (Divide-by- 1, 2, 4 or 8)**
- **JESD204B Subclass 1 Serial Data Interface**
  - **Lane Rates up to 7.4 Gb/s**
  - **Configurable as 1- or 2-lanes/channel**
- **Fast Over-range Signals**
- **4-wire, 1.2 V, 1.8 V, 2.5V or 3.3V Compatible SPI**
- **56-pin QFN Package, (8 x 8 mm, 0.5mm pin-pitch)**

APPLICATIONS

- **High IF Sampling Receivers**
- **Multi-Carrier Base Station Receivers**
  - **GSM/EDGE, CDMA2000, UMTS, LTE, and WiMax**
- **Diversity, Multi-Mode and Multiband Receivers**
- **Digital Pre-Distortion**

DESCRIPTION

The LM97937 device is a dual-channel 370 MSPS analog-to-digital converter (ADC) with JESD204B interface operating up to 7.4 Gb/s. SNRBoost technology with bandpass spectral shaping improves the noise density at the intermediate frequency and Bit-Burst technology provides temporary and periodic resolution enhancement. The integrated input buffer reduces charge kick-back noise and eases the system level design of the driving amplifier, anti-aliasing filter and impedance matching. An input sampling clock divider provides integer divide ratios with configurable phase selection to simplify system clocking. The device comes in a 56-pin, 8-mm × 8-mm QFN package.

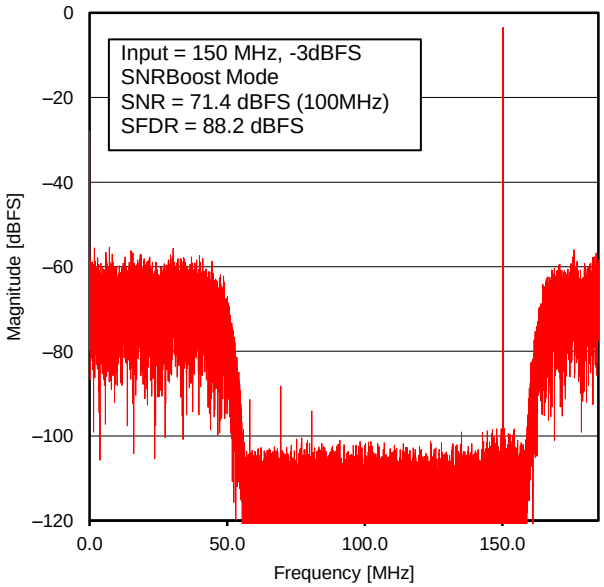


Figure 1. 1-Tone Spectrum, SNRBoost Mode, 150 MHz

Block Diagrams

Figure 2. SNRBoost Mode Top Level Block Diagram

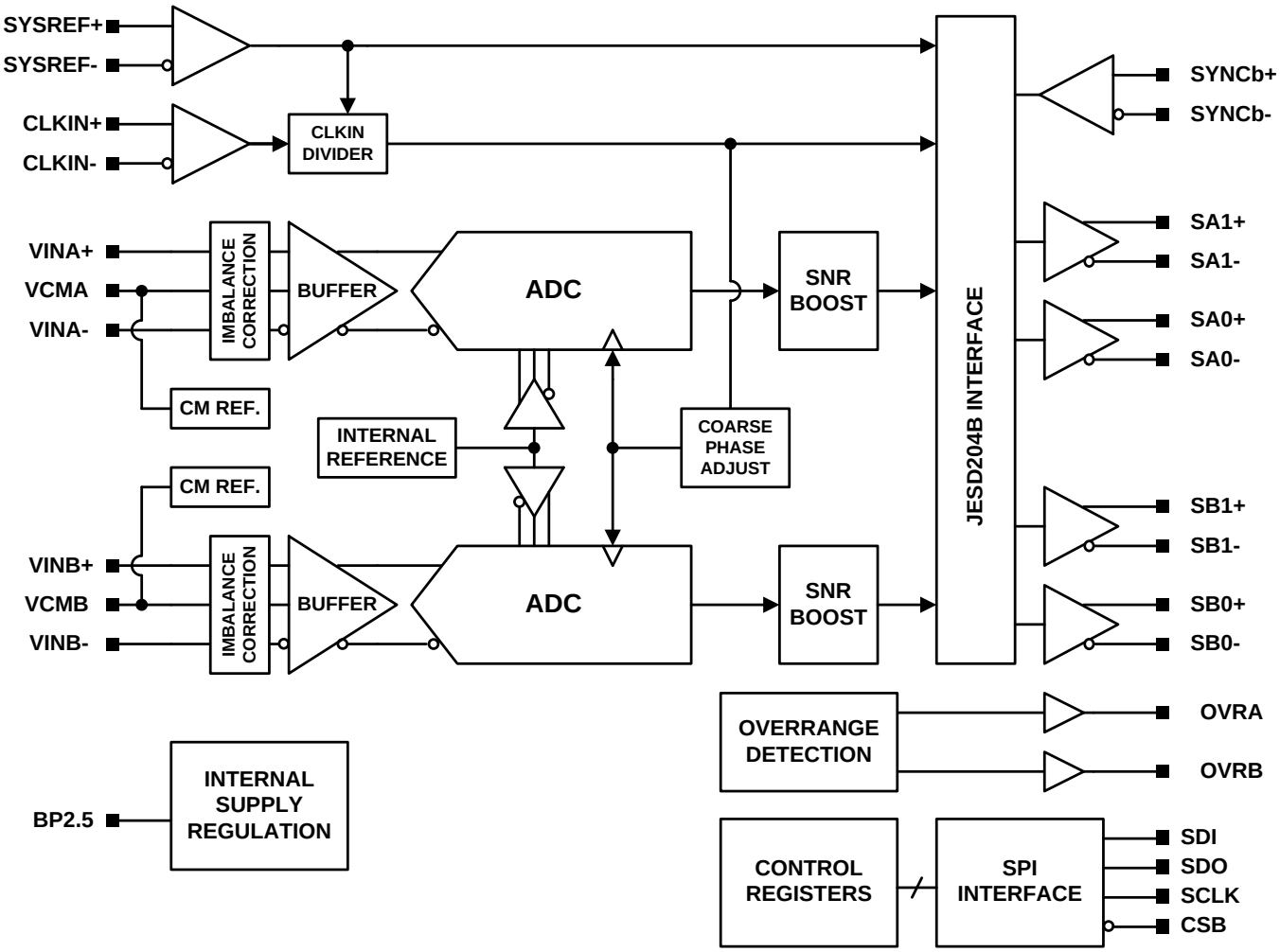
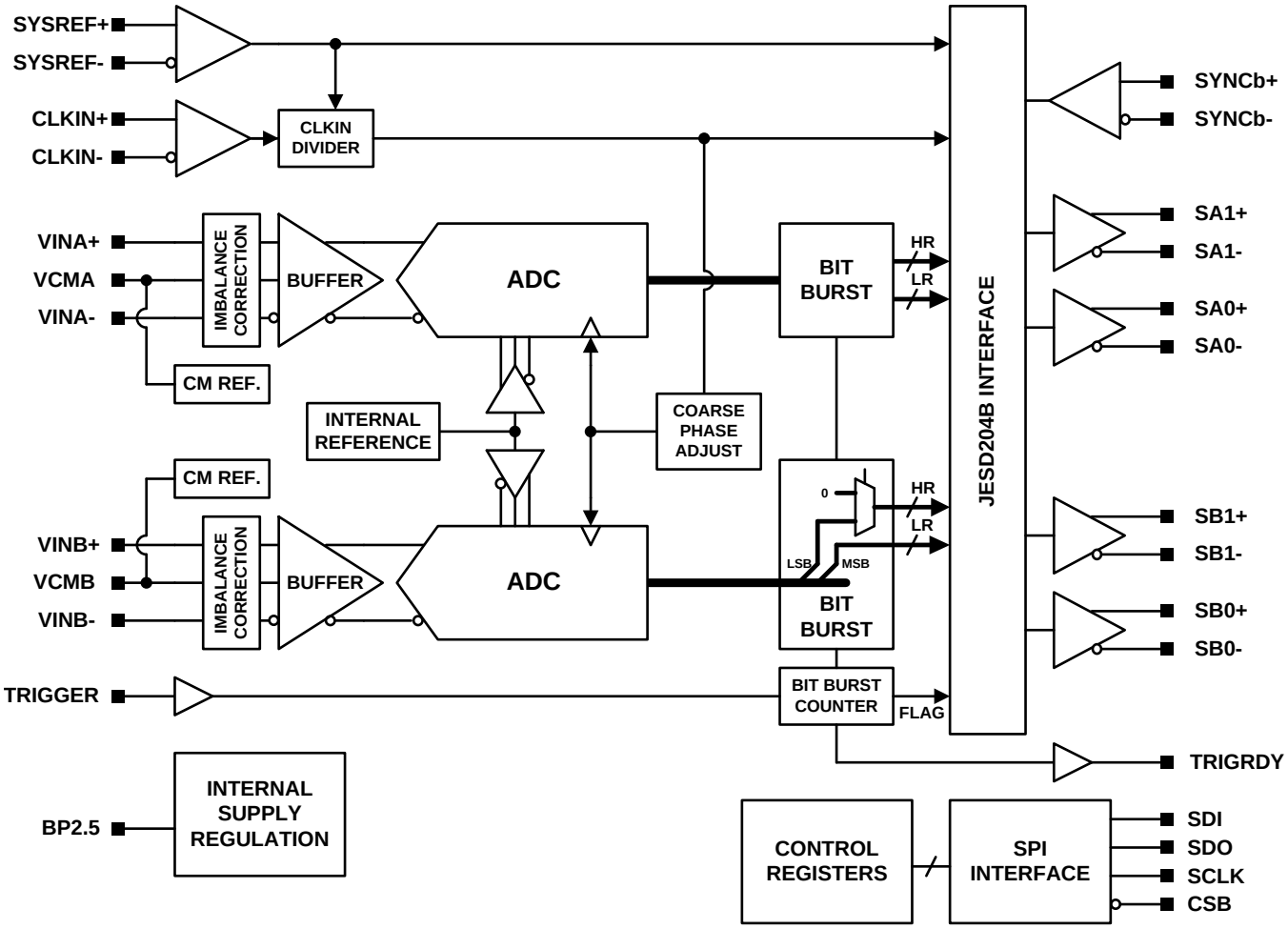
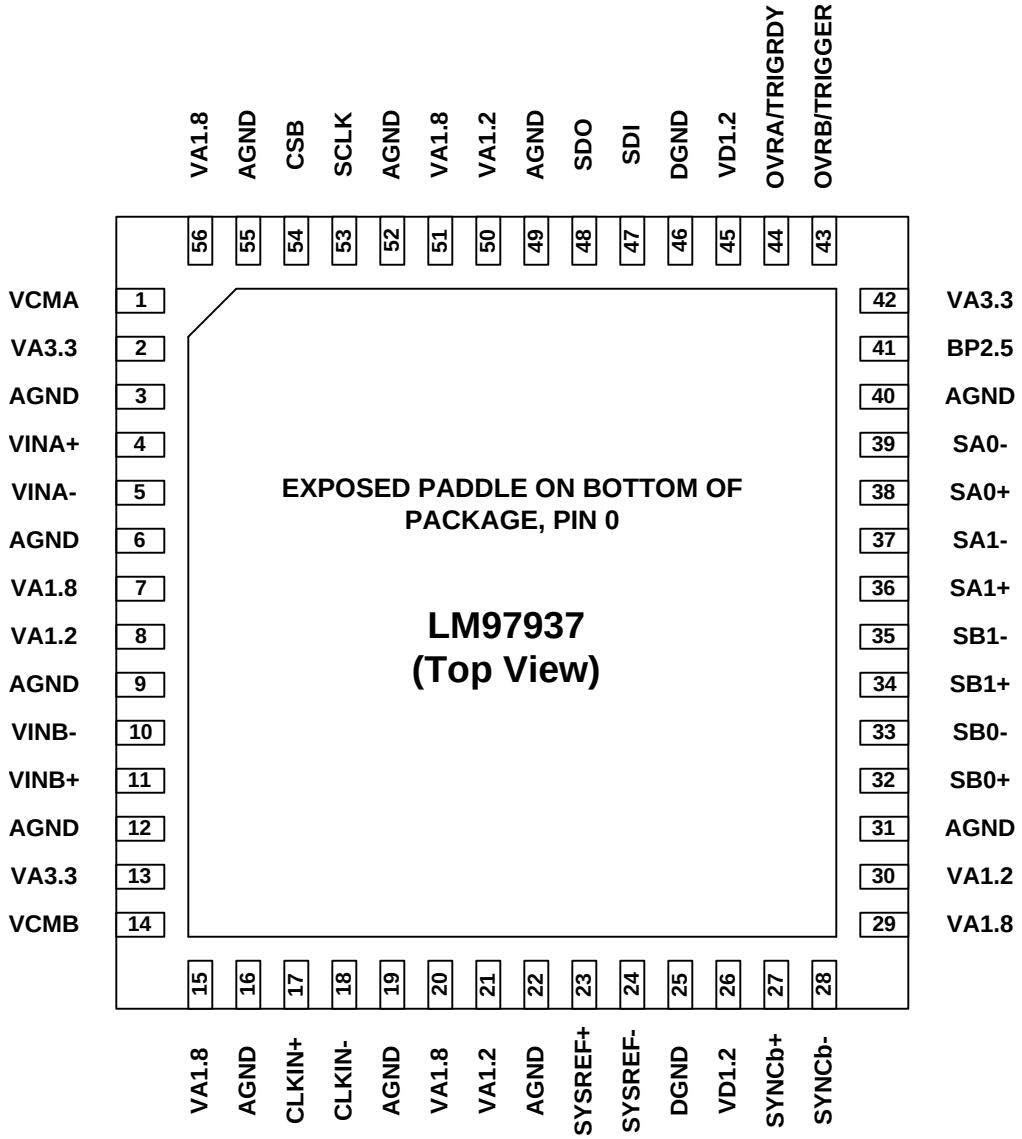


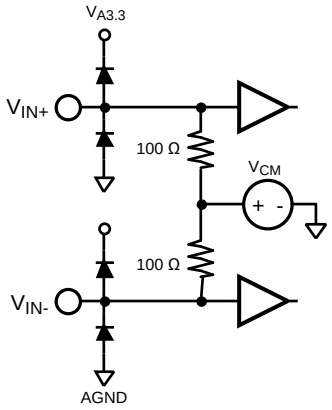
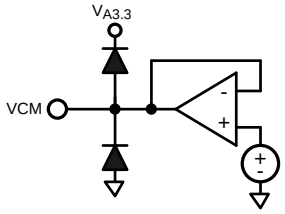
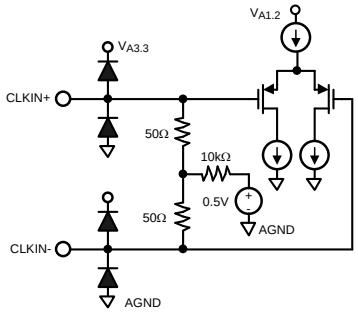
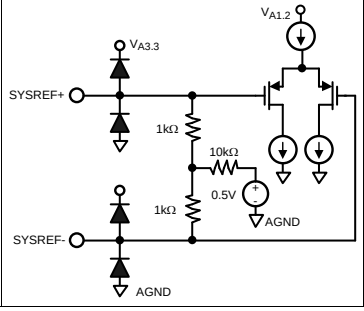
Figure 3. Bit-Burst Mode Top Level Block Diagram

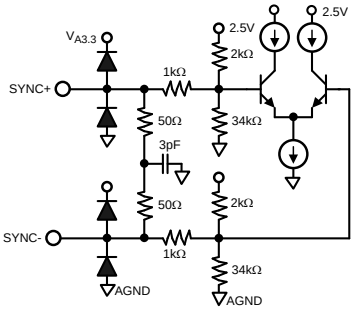
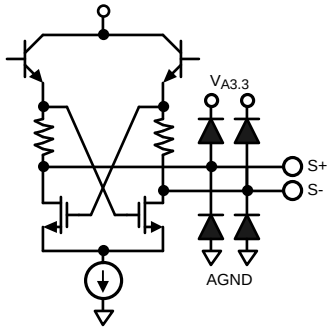
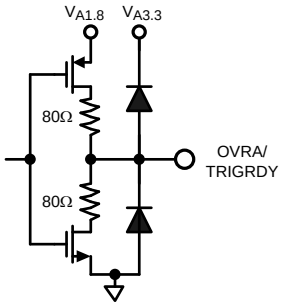
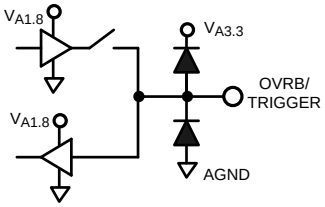


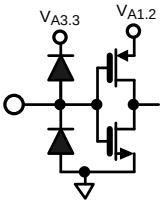
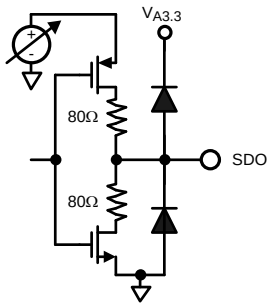
PIN DIAGRAM



PIN DESCRIPTION

PIN	NAME	TYPE/DIAGRAM	DESCRIPTION
4,5	VINA+, VINA–		Differential analog input pins of channel A. Each input pin is terminated to the internal common mode reference with a resistor for an internal differential termination.
11,10	VINB+, VINB–		Differential analog input pins of channel B. Each input pin is terminated to the internal common mode reference with a resistor for an internal differential termination.
1,14	VCMA, VCMB		Input interface common mode voltage for channels A and B. These pins must be bypassed to AGND with low ESL (equivalent series inductance) 0.1 µF capacitors. One should be placed as close to the pin as possible and additional capacitors placed at the bias load points. 10 µF capacitors should also be placed in parallel. It is recommended to use VCMA and VCMB to provide the common mode voltage for the differential analog inputs. The input common mode bias is provided internally for the ADC input, therefore external use of VCMA and VCMB is recommended but not strictly required. The recommended bypass capacitors are always required.
17,18	CLKIN+, CLKIN–		Differential device clock input pins. Each pin is internally terminated to a DC bias with a 50 Ω resistor for a 100 Ω total internal differential termination. AC coupling is required for coupling the clock input to these pins if the clock driver cannot meet the common-mode requirements. Sampling occurs on the rising edge of the differential signal (CLKIN+) − (CLKIN–).
23,24	SYSREF+, SYSREF–		Differential SYSREF signal input pins. Each pin is internally terminated to a DC bias with a 1 kΩ resistor. An external 100 Ω differential termination must always be provided. AC coupling using capacitors is required for coupling the SYSREF signal to these pins if the clock driver cannot meet the common-mode requirements. In the case of AC coupling, the termination must be placed on the source side of the coupling capacitors.

PIN	NAME	TYPE/DIAGRAM	DESCRIPTION
27, 28	SYNCb+, SYNCb–		Differential SYNCb signal input pins. DC coupling is required for coupling the SYNCb signal to these pins. Each pin is internally terminated to the DC bias with a large resistor. An internal 100 Ω differential termination is provided therefore an external termination is not required. Additional resistive components in the input structure give the SYNCb input a wide input common-mode range. The SYNCb signal is active low and is therefore asserted when the voltage at SYNCb+ is less than at SYNCb–.
38, 39, 36, 37	SA0+, SA0–, SA1+, SA1–		Differential high speed serial data lane pins for channel A. These pins must be AC coupled to the receiving device. The differential trace routing from these pins must maintain a 100Ω characteristic impedance. In single-lane mode, SA0 +/– is utilized to transfer data and SA1+/– is undefined and may be left floating.
32, 33, 34, 35	SB0+, SB0–, SB1+, SB1–		Differential high speed serial data lane pins for channel B. These pins must be AC coupled to the receiving device. The differential trace routing from these pins must maintain a 100Ω characteristic impedance. In single-lane mode, SB0+/– is utilized to transfer data and SB1+/– is undefined and may be left floating.
44	OVRA/ TRIGRDY		Dual purpose pin. While in SNRBoost mode, this pin outputs the channel A over-range signal. While in Bit-Burst mode and in Trigger sub-mode, this pin outputs the “trigger ready” signal that indicates when a Bit-Burst cycle has completed and a new trigger edge may be applied. This pin is a 1.8 V CMOS logic level output.
43	OVRB/ TRIGGER		Dual purpose pin. While in SNRBoost mode, this pin outputs the channel B over-range signal. In this mode, the pin is a 1.8 V CMOS logic level output. While in Bit-Burst mode and Trigger sub-mode, this pin is the “trigger” signal that is used to start a new Bit-Burst cycle when a rising edge is applied. In this mode, the pin is a 1.8 V CMOS logic level asynchronous input.

PIN	NAME	TYPE/DIAGRAM	DESCRIPTION
53	SCLK		SPI Interface Serial Clock pin. Serial data is shifted into and out of the device synchronous with this clock signal. Compatible with 1.2 – 3.3 V CMOS logic levels.
54	CSB		SPI Interface Chip Select pin. When this signal is asserted, SCLK is used to clock the input serial data on the SDI pin or output serial data on the SDO pin. When this signal is de-asserted, the SDO pin is high impedance and the input data is ignored. Active low. A 10 kΩ pull-up resistor to the VA1.8 supply is recommended to prevent undesired activation of the SPI bus. Compatible with 1.2 – 3.3 V CMOS logic levels.
47	SDI		SPI Interface Data Input pin. Serial data is shifted into the device on this pin while the CSB signal is asserted. Compatible with 1.2 – 3.3 V CMOS logic levels.
48	SDO		SPI Interface Data Output pin. Serial data is shifted out of the device on this pin during a read command while CSB is asserted. The output logic level is configurable as 1.2 V, 1.8 V, 2.5 V or 3.3 V. The output level MUST be configured after power up and before performing a read command. See the Register Map for configuration details.
2, 13, 42	VA3.3	Supply Input Pin	3.3 V Analog Power Supply pin. This pin must be connected to a quiet source and decoupled to AGND with a 0.1 µF and a 0.01 µF capacitor located close to the pin.
7, 15, 20, 29, 51, 56	VA1.8	Supply Input Pin	1.8 V Analog Power Supply pins. These pins must be connected to a quiet source and decoupled to AGND with a 0.1 µF and a 0.01 µF capacitor located close to each pin.
8, 21, 30, 50	VA1.2	Supply Input Pin	1.2 V Analog Power Supply pins. These pins must be connected to a quiet source and decoupled to AGND with a 0.1 µF and a 0.01 µF capacitor located close to each pin.
26, 45	VD1.2	Supply Input Pin	1.2 V Digital Power Supply pin. This pin must be connected to a quiet source and decoupled to AGND with a 0.1 µF and a 0.01 µF capacitor located close to each pin.
41	BP2.5	Bypass Pins	Capacitive Bypassing pin for internally regulated 2.5 V supply. This pin must be decoupled to AGND with a 0.1 µF and a 10 uF capacitor located close to the pin.
3, 6, 9, 12, 16, 19, 22, 31, 40, 49, 52, 55	AGND	Analog Ground	Analog Ground. Must be connected to a solid ground reference plane under the device.

PIN	NAME	TYPE/DIAGRAM	DESCRIPTION
25, 46	DGND	Digital Ground	Digital Ground. Must be connected to the same solid ground reference plane under the device to which AGND connects. Bypass capacitors connected to the VD1.2 pins must be connected to ground as close to this DGND pins as possible.
0		Exposed Thermal Pad	Exposed Thermal Pad. The exposed pad must be connected to the AGND ground plane electrically and with good thermal dissipation properties to ensure rated performance.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

		VALUE		UNIT
		MIN	MAX	
Supply Voltage: $V_{A3.3}$		–0.3	4.2	V
Supply Voltage: $V_{A1.8}$		–0.3	2.35	V
Supply Voltage: $V_{A1.2}$, $V_{D1.2}$		–0.3	1.55	V
Voltage at VINA+, VINA–		V_{CMA} – 1.0	V_{CMA} + 0.75	V
Voltage at VINB+, VINB-		V_{CMB} – 1.0	V_{CMB} + 0.75	V
Voltage at VCMA, VCMB		–0.3	$V_{A3.3}$ + 0.3, not to exceed 4.2 V	V
Voltage at OVRA /TRIGRDY, ORVB/TRIGGER		–0.3	$V_{A1.8}$ + 0.3	V
Voltage at SCLK, SDI, CSb		–0.3	$V_{A3.3}$ + 0.3, not to exceed 4.2 V	V
Voltage at SDO		–0.3	V_{SPI} + 0.3, not to exceed 4.2 V	V
Voltage at CLKIN+, CLKIN–, SYSREF+, SYSREF–		–0.3	1.55	V
Voltage at SYNC+, SYNC–		–0.3	$V_{BP2.5}$ + 0.3	V
Voltage at BP2.5		–0.3	3.2	V
Voltage at SA0+, SA0–, SA1+, SA1–, SB0+, SB0–, SB1+, SB1–		–0.3	$V_{BP2.5}$ + 0.3	V
Input Current at any Pin(1)			5	mA
Junction Temperature (T_J)	Maximum rated operating junction temperature(2)	+125		°C
	Recommended long-term operating junction temperature		+105	°C
Storage Temperature Range		–65	+150	°C
ESD Rating	Human Body Model		1000	V
	Charged Device Model		250	V

(1) When the input voltage at any pin exceeds the VA3.3 power supply (that is $V_{IN} > V_{A3.3}$ or $V_{IN} < AGND$) the current at that pin should be limited to +/-5mA. The +/-50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of +/-5mA to 10 pins.

(2) Prolonged use at this temperature may increase the device failure-in-time (FIT) rate.

THERMAL INFORMATION

THERMAL METRIC(1)		NOMINAL VALUE	UNIT
θ_{JA}	Thermal Resistance, Junction–Ambient	24.9	°C/W
θ_{JC}–Top	Thermal Resistance, Junction–Package Top	8.6	°C/W
θ_{JB}	Thermal Resistance, Junction–Board	3.0	°C/W
PSI_{JT}	Characterization parameter, Junction-Package Top	0.2	°C/W
PSI_{JB}	Characterization parameter, Junction-Board	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953

RECOMMENDED OPERATING CONDITIONS

Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. Guaranteed specifications and test conditions are specified in the Electrical Characteristics section. Operation of the device beyond the Operating Ratings is not recommended as it may degrade the device lifetime.

	MIN	MAX	UNITS
Specified Temperature Range	–40	85	°C
3.3 V Analog Supply Voltage Range: $V_{A3.3}$	2.85	3.45	V
1.8 V Analog Supply Voltage Range: $V_{A1.8}$	1.7	1.9	V
1.2 V Analog Supply Voltage Range: $V_{A1.2}$	1.15	1.25	V
1.2 V Digital Supply Voltage Range: $V_{D1.2}$	1.15	1.25	V
CLKIN Duty Cycle	30	70	%

Converter Dynamic Performance Characteristics (SNRBoost Mode)

Unless otherwise noted, these specifications apply for $V_{A3.3}$= 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; SNRBoost Mode, F_C=0.25*F_S; external differential resistive termination at ADC input is 66 Ω. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	TYP	LIMIT	UNITS
SNR	Signal to Noise Ratio Noise, integrated across 100 MHz SNRBoost Bandwidth			dBFS
	Input = 46 MHz, –3 dBFS	71.9		
	Input = 150 MHz, –3 dBFS, SNRBoost F_C=0.29*F_S	71.6	**71.3**	
	Input = 231 MHz, –3 dBFS	71.4		
	Input = 325MHz, –3 dBFS	71.0		
	Input = 325MHz, –40 dBFS	72.0		
SINAD	Signal to Noise and Distortion Ratio, integrated across 100 MHz SNRBoost bandwidth			dBFS
	Input = 46 MHz, –3 dBFS	71.7		
	Input = 150 MHz, –3 dBFS, SNRBoost F_C=0.29*F_S	71.2		
	Input = 231 MHz, –3 dBFS	71.0		
	Input = 325MHz, –3 dBFS	70.6		
	Input = 325MHz, –40 dBFS	72.0		
NSD	Noise Spectral Density, average NSD across 100MHz SNRBoost bandwidth			dBFS/Hz
	Input = 46 MHz, –3 dBFS	–151.9		
	Input = 150 MHz, –3 dBFS, SNRBoost F_C=0.29*F_S	–151.6	**–151.3**	
	Input = 231 MHz, –3 dBFS	–151.4		
	Input = 325MHz, –3 dBFS	–151.0		
	Input = 325MHz, –40 dBFS	–152.0		

Converter Dynamic Performance Characteristics (SNRBoost Mode) (continued)

Unless otherwise noted, these specifications apply for $V_{A3.3}$= 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; SNRBoost Mode, F_C=0.25*F_S; external differential resistive termination at ADC input is 66 Ω. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	TYP	LIMIT	UNITS
SFDR	Single-tone Spurious Free Dynamic Range Measured across 100MHz SNRBoost Bandwidth			dBFS
	Input = 46 MHz, –3 dBFS	88.0		
	Input = 150 MHz, –3 dBFS, SNRBoost F_C=0.29*F_S	88.0	**80.0**	
	Input = 231 MHz, –3 dBFS	85.0		
	Input = 325MHz, –3 dBFS	85.0		
HD2	2nd Order Harmonic Distortion			dBFS
	Input = 46 MHz, –3 dBFS	–93.0		
	Input = 150 MHz, –3 dBFS, SNRBoost F_C=0.29*F_S	–89.0	**–80.0**	
	Input = 231 MHz, –3 dBFS	–90.0		
	Input = 325MHz, –3 dBFS	–89.0		
HD3	3rd Order Harmonic Distortion			dBFS
	Input = 46 MHz, –3 dBFS	–88.0		
	Input = 150 MHz, –3 dBFS	–88.0	**–81.0**	
	Input = 231 MHz, –3 dBFS	–85.0		
	Input = 325MHz, –3 dBFS	–85.0		
SPUR	Largest spurious tone, not including DC, HD2 or HD3			dBFS
	Input = 46 MHz, –3 dBFS	–90.0		
	Input = 150 MHz, –3 dBFS	–90.0	**–88.0**	
	Input = 231 MHz, –3 dBFS	–90.0		
	Input = 325MHz, –3 dBFS	–90.0		

Converter Dynamic Performance Characteristics (Bit-Burst Mode)

Unless otherwise noted, these specifications apply for $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; device configured for Bit-Burst Mode, 14-bit High-Resolution; external differential resistive termination at ADC input is 66 Ω. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	TYP	LIMIT	UNITS
SNR	Signal to Noise Ratio, integrated across entire Nyquist bandwidth, Low Resolution Bit-Burst phase			dBFS
	Input = 325 MHz, Ain = –3 dBFS	58.4		
	Signal to Noise Ratio, integrated across entire Nyquist Bandwidth, High Resolution Bit-Burst phase			
	Input = 46 MHz, –3 dBFS	69.8		
	Input = 150 MHz, –3 dBFS	69.6		
	Input = 231 MHz, –3 dBFS	69.4		
	Input = 325 MHz, Ain = –3 dBFS	69.0		
	Input = 325MHz, Ain = –40 dBFS	70.0		

Converter Dynamic Performance Characteristics (Bit-Burst Mode) (continued)

Unless otherwise noted, these specifications apply for $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; device configured for Bit-Burst Mode, 14-bit High-Resolution; external differential resistive termination at ADC input is 66 Ω. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	TYP	LIMIT	UNITS
SINAD	Signal to Noise and Distortion Ratio, integrated across entire Nyquist bandwidth, Low Resolution Bit-Burst phase			dBFS
	Input = 325 MHz, Ain = –3 dBFS	54.7		
	Signal to Noise and Distortion Ratio, integrated across Nyquist bandwidth, High Resolution Bit Burst phase			
	Input = 46 MHz, –3 dBFS	69.5		
	Input = 150 MHz, –3 dBFS	69.4		
	Input = 231 MHz, –3 dBFS	69.1		
	Input = 325 MHz, –3 dBFS	68.8		
	Input = 325 MHz, –40 dBFS	70.0		
NSD	Noise Spectral Density, average NSD across entire Nyquist bandwidth, Low Resolution Bit-Burst phase			dBFS/Hz
	Input = 325 MHz, –3 dBFS	–141.1		
	Noise Spectral Density, average NSD across Nyquist bandwidth, High Resolution Bit Burst phase			
	Input = 46 MHz, –3 dBFS	–152.5		
	Input = 150 MHz, –3 dBFS	–152.3		
	Input = 231 MHz, –3 dBFS	–152.1		
	Input = 325 MHz, –3 dBFS	–151.7		
	Input = 325 MHz, –40 dBFS	–152.7		
SFDR	Spurious Free Dynamic Range, Single Tone, High Resolution Bit Burst phase			dBFS
	Input = 46 MHz, –3 dBFS	88		
	Input = 150 MHz, –3 dBFS	88		
	Input = 231 MHz, –3 dBFS	85		
	Input = 325 MHz, –3 dBFS	85		
HD2	2^{nd} Order Harmonic Distortion			dBFS
	Input = 46 MHz, –3 dBFS	–93		
	Input = 150 MHz, –3 dBFS	–89		
	Input = 231 MHz, –3 dBFS	–90		
	Input = 325MHz, –3 dBFS	–89		
HD3	3^{rd} Order Harmonic Distortion			dBFS
	Input = 46 MHz, –3 dBFS	–88		
	Input = 150 MHz, –3 dBFS	–88		
	Input = 231 MHz, –3 dBFS	–85		
	Input = 325MHz, –3 dBFS	–85		
SPUR	Largest spurious tone, not including DC, HD2 or HD3			dBFS
	Input = 46 MHz, –3 dBFS	–90		
	Input = 150 MHz, –3 dBFS	–90		
	Input = 231 MHz, –3 dBFS	–90		
	Input = 325MHz, –3 dBFS	–90		
IMD3	Third-order Intermodulation, Dual Tone, High Resolution Bit Burst phase			dBFS
	Tone 1 = 145 MHz, –10 dBFS Tone 2 = 155 MHz, –10 dBFS	–102		

POWER SUPPLY ELECTRICAL CHARACTERISTICS(1)

Unless otherwise noted, these specifications apply for $V_{A3.3}$ = 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS		TYP	LIMIT	UNIT
$I_{A3.3}$	$V_{A3.3}$ supply current consumption	Normal operation, single data lane per channel	236		mA
		Normal operation, dual data lane per channel	255		
		Power down mode	8.7		
$I_{A1.8}$	$V_{A1.8}$ supply current consumption	Normal operation	383		mA
		Power down mode	3.6		
$I_{A1.2}$	$V_{A1.2}$ supply current consumption	Normal operation	176		mA
		Power down mode	3.3		
$I_{D1.2}$	$V_{D1.2}$ supply current consumption	SNRBoost Mode, F_C=0.25*F_S	141		mA
		Bit-Burst Mode	46		
		Power down mode	3.3		
P_T	Total power consumption of the $V_{A3.3}$ and $V_{A1.8}$ and $V_{A1.2}$ and $V_{D1.2}$ supplies				mW
	SNRBoost Mode, F_C=0.25*F_S, Single Serial Lane per Channel		1,871	1978	
	Bit-Burst Mode, Single Serial Lane per Channel		1,752	1854	
P_{PD}	Power Consumption during Power Down State, external clock active		30		mW
P_{SL}	Power Consumption during Sleep state, external clock active		30		mW
$V_{BP2.5}$	Voltage at the BP2.5 pin		2.65		V
	Supply Sensitivity to Noise Power of spectral spur resulting from a 100mV sinusoidal signal modulating a supply at 500kHz. Analog input is a -3 dBFS 150 MHz single tone. In all cases, the spur appears as part of a pair symmetric about the fundamental that scales proportionally with the fundamental amplitude.				dBFS
	VA3.3		-72.5		
	VA1.8		-58.0		
	VA1.2		-37.7		
	VD1.2		-78.0		

(1) Power values indicate consumption during normal conversion assuming JESD204 link establishment and proper ADC calibration as described in ADC Core Calibration

SNRBoost Mode Functional Characteristics

Unless otherwise noted, these specifications apply for all supply and temperature conditions.

PARAMETER	DESCRIPTION / CONDITIONS	VALUE	UNIT
FSR_{SB}	SNRBoost Mode Digital Full Scale At Clipping Maximum sinusoidal power before 9-bit clipping results in a sample clipping rate of 1e–5	–0.8	dBFS
BW_{SB}	Low-Noise Bandwidth Dependent on sampling rate (F_S)	0.273 * F_S	MHz
FC_{SB}	Noise Shaping Center Frequencies Configurable via SPI, dependent on sampling rate (F_S).	0.21 * F_S 0.25 * F_S 0.29 * F_S	MHz
NQ_{SB}	Total Quantization Noise Power Integrated noise across full Nyquist zone with no input signal.	–31.5	dBFS
OVRTH	Over-range Detection Threshold Configurable via SPI	0 (max) –48.16 (min)	dBFS
OVRTHS	Over-range Detection Threshold Step Expressed as the change in the total code range outside of which an over-range event occurs. Half of the step value is changed at the upper boundary of the code range and half is changed at the lower boundary.	256	Codes

Bit-Burst Mode Functional Characteristics

Unless otherwise noted, these specifications apply for all supply and temperature conditions.

PARAMETER	DESCRIPTION / CONDITIONS	VALUE	UNIT
$R_{LOW-RES}$	Low-Res Phase Resolution Bit resolution of the sampled data during the low-resolution phase of the Bit-Burst cycle.	9	Bits
R_{HI-RES}	High-Res Phase Resolution Bit resolution of the sampled data during the high-resolution phase of the Bit-Burst cycle; Configurable via SPI.	12 or 14	Bits
N_{HI-RES}	High-Res Phase Duration Number of samples output during the High-Resolution phase of the Bit-Burst cycle; Configurable via SPI.	2^10 (min, def) 2^25 (max)	Samples
$N_{LOW-RES}$	Low-Res Phase Duration Number of samples output during the Low-Resolution phase of the Bit-Burst cycle; Depends on R_{HI-RES} and N_{HI-RES}.		Samples
	R_{HI-RES} = 14 bits	3 * N_{HI-RES}	
	R_{HI-RES} = 12 bits	N_{HI-RES}	
DC_{HI-RES}	Bit-Burst Duty Cycle Ratio of N_{HI-RES} to the total number of samples in a full Bit-Burst cycle; Depends on R_{HI-RES}.		
	R_{HI-RES} = 14 bits	1 / 4	
	R_{HI-RES} = 12 bits	1 / 2	
N_{D-BB}	Bit-Burst Mode Start-up Delay Low-Resolution start-up time that must complete before High-Resolution bits appear (Stream sub-mode) or High-Resolution bits may be triggered (Trigger sub-mode)		Samples
	After supply power-up	3 * 2^10	
	After soft power-up via SPI	$N_{LOW-RES}$	
	After changing R_{HI-RES}	$N_{LOW-RES}$	
	After entering Bit-Burst Mode or switching between Trigger and Stream configurations	$N_{LOW-RES}$	

Input Clock Divider and Clock Phase Adjustment Functional Characteristics

Unless otherwise noted, these specifications apply for $V_{A3.3}$ = 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	TYP	LIMIT	UNIT
CLKDIV	Input CLKIN Divider Factor Configurable via SPI	1 (default), 2, 4, or 8		
$N\Phi_C$	Number of Available Coarse Phase Adjustment Steps	2*CLKDIV		
Φ_C	Nominal CLKIN Coarse Phase Adjustment Step Coarse step of CLKIN divider phase adjustment range; Common to both channels; Depends on clock divider factor (CLKDIV) and sampling rate (F_S).	1 / (2*CLKDIV*F_S)		s
$\Delta\Phi_C$	Typical Coarse Phase Adjustment Step Error(1) Percent variation of actual phase adjustment step relative to the nominal step (Φ_C). Assumes ideal 50% CLKIN duty cycle			
	CLKDIV = 8, F_S = 250MSPS	+/- 6		%
	CLKDIV = 4, F_S = 370MSPS	+/- 4		

(1) CLKIN duty cycles that are not 50/50% increase the coarse delay step error

JESD204B Interface Functional Characteristics

Unless otherwise noted, these specifications apply for all supply and temperature conditions.

PARAMETER	DESCRIPTION / CONDITIONS	VALUE
LSF	Supported Configurations L = Number of lanes/converter S = Samples per frame F = Octets per frame	L=1, S=1, F=2 or L=2, S=1, F=1
K	Number of Frames per Multi-Frame Configurable via SPI.	
	L=1, S=1, F=2	9 (min) 32 (max, default)
	L=2, S=1, F=1	17 (min) 32 (max, default)

Analog Interface Electrical Characteristics

Unless otherwise noted, these specifications apply for $V_{A3.3}$ = 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; external differential resistive termination at ADC input is 66 Ω. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	TYP	LIMIT	UNIT
FSR	Full Scale Range Differential peak-to-peak	1.7		Vpp
G_{VAR}	Gain Variation Variation of input voltage to output code gain between different parts, part-to-part or channel-to-channel	± 0.07		dB
BW_{3dB}	3dB Bandwidth Frequency at which the voltage input to digital output response deviates by 3dB compared to low frequencies for a low impedance differential signal applied at the input pins. Includes 0.5 nH parasitic inductance in series with each pin of the differential analog input.	800		MHz
R_{IN}	Input Termination Resistance Differential	200		Ω
C_{IN}	Input Capacitance, Differential	3.7		pF
V_{CMA}, V_{CMB}	Input Common Mode Voltage Reference Voltage at the VCMA or VCMB pins Varies with temperature	1.6		V
I_{VCM}	Input Common Mode Voltage Reference Current Sourcing or Sinking on VCMA or VCMB pins		1	mA
V_{CM-OFF}	Input Common Mode Voltage Offset Range Allowable difference between the common mode applied to the analog input of a particular channel and the bias voltage at the respective common mode VCM bias pin (VCMA or VCMB)		± 50	mV

CLKIN, SYSREF, SYNCb Interface Electrical Characteristics

Unless otherwise noted, these specifications apply for $V_{A3.3}$ = 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT CHARACTERISTICS (CLKIN)					
V_{ID}	Input Differential Voltage(1)(2) Differential peak voltage	250		1000	mV
dV_{SS}/dt	Recommended Minimum Edge Slew Rate at the Zero Crossing(1)	2	5		V/ns
$V_{IS-BIAS}$	Input Offset Voltage Internal Bias (1) Internally biased		0.5		V
V_{IS-IN}	Externally Applied Input Offset Voltage(2) Allowable common mode voltage range for DC coupled interfaces	0.4	0.5	0.6	V

(1) Specification applies to the electrical level diagram of Figure 4
(2) The voltage present at the pins should not exceed Absolute Maximum limits

CLKIN, SYSREF, SYNCb Interface Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{A3.3}$ = 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	MIN	TYP	MAX	UNITS
Zrdiff	Differential Termination Resistance at DC (3)		130		Ω
Ztt	Common-Mode Bias Source Impedance (3)		11		kΩ
C_T	Differential Termination Capacitance		1.5		pF
DIGITAL INPUT CHARACTERISTICS (SYSREF)					
V_{ID}	Input Differential Voltage (1) (2) Differential peak voltage	250		1000	mV
$V_{IS-BIAS}$	Input Offset Voltage Bias (1) Internally biased		0.5		V
V_{IS-IN}	Externally Applied Input Offset Voltage (2) Allowable common mode voltage range for DC coupled interfaces	0.4	0.5	0.6	V
Zrdiff	Differential Termination Resistance at DC (3)		2		kΩ
Ztt	Common-Mode Bias Source Impedance (3)		11		kΩ
C_T	Differential Termination Capacitance (3)		0.8		pF
DIGITAL INPUT CHARACTERISTICS (SYNCb)					
V_{ID}	Input Differential Voltage (1) (2) Differential peak voltage		350		mV
V_{IS-IN}	Externally Applied Input Offset Voltage (4) (5)	0.5	1.2	2.0	V
Zrdiff	Differential Termination Resistance (6)		100		Ω
C_T	Differential Termination Capacitance (6)		1.0		pF

(3) Specification applies to the electrical circuit diagram of Figure 5
(4) Specification applies to the electrical level diagram of Figure 4
(5) The voltage present at the pins should not exceed Absolute Maximum limits
(6) Specification applies to the electrical circuit diagram of Figure 5

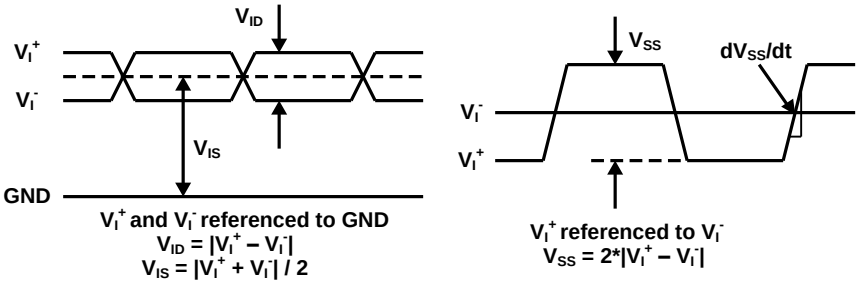


Figure 4. Electrical Level Diagram for Differential Input Signals

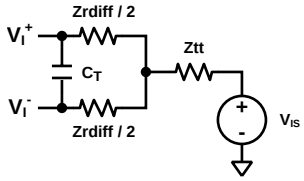


Figure 5. Simplified Electrical Circuit Diagram for Differential Input Signals

Serial Data Output Interface Electrical Characteristics

Unless otherwise noted, these specifications apply for $V_{A3.3}$ = 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL LANE OUTPUT CHARACTERISTICS (SA0, SA1, SB0, SB1)					
V_{OD}	Output Differential Voltage(1) Differential peak-peak values. Assumes ideal 100Ω load. De-emphasis disabled. Configurable via SPI		580 680 760 860 960 1060 1140 1240		mV
Zddiff	Differential Output Impedance at DC(2)		100		Ω
RLddiff	Differential Output Return Loss Magnitude Relative to 100 Ω; For frequencies up to 5.5 GHz		-11		dB
Rdeemp	Transmitter De-Emphasis values V_{OD} configured to default value.		0 0.4 1.2 2.1 2.8 3.8 4.8 6.8		dB

(1) Specification applies to the electrical level diagram of Figure 6
(2) Specification applies to the electrical circuit diagram of Figure 7

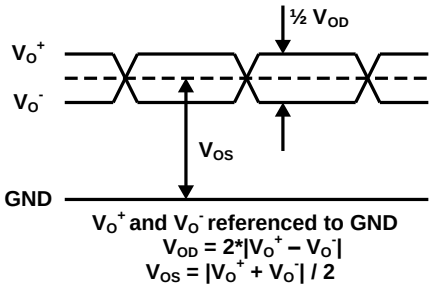


Figure 6. Electrical Level Diagram for Differential Output Signals

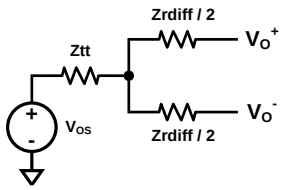


Figure 7. Electrical Circuit Diagram for Differential Output Signals

Digital Input Electrical Interface

Unless otherwise noted, these specifications apply for $V_{A3.3}$= 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT CHARACTERISTICS (SDI, SCLK, CSB)					
V_{IH}	Logical “1” Input Voltage(1) Inputs are compatible with 1.2V or 1.8V logic.	0.9			V
V_{IL}	Logical “0” Input Voltage(1)			0.3	V
I_{IN0}	Logic Low Input Current		0.5		uA
I_{IN1}	Logic High Input Current		0.5		uA
C_{IN}	Input Capacitance		2		pF
DIGITAL OUTPUT CHARACTERISTICS (SDO)					
V_{OH}	Logical “1” Output Voltage(1)(2) V_{SPI} = 1.2, 1.8, 2.5 or 3.3V ; Configurable via SPI	V_{SPI} – 0.3	V_{SPI}(2)		V
V_{OL}	Logical “0” Output Voltage(1)(2)		0.0	0.3	V
$+I_{SC}$	Logic High Short Circuit Current		9		mA
$-I_{SC}$	Logic Low Short Circuit Current		-10		mA
DIGITAL OUTPUT CHARACTERISTICS (OVRA/TRIGRDY, OVRB)					
V_{OH}	Logical “1” Output Voltage(1)	1.5	1.8		V
V_{OL}	Logical “0” Output Voltage(1)		0.0	0.3	V
$+I_{SC}$	Logic High Short Circuit Current		17.7		mA
$-I_{SC}$	Logic Low Short Circuit Current		-15.0		mA
DIGITAL INPUT CHARACTERISTICS (TRIGGER)					
V_{IH}	Logical “1” Input Voltage(1)	1.5			V
V_{IL}	Logical “0” Input Voltage(1)			0.3	V
I_{IN0}	Logic Low Input Current		0.5		uA
I_{IN1}	Logic High Input Current		0.5		uA
C_{IN}	Input Capacitance		3		pF

(1) Specification applies to the electrical level diagram of Figure 8
(2) The SPI_CFG register must be changed to a supported output logic level after power up and before a read command is executed. Until that time, the output voltage on SDO may be as high as 3.3V during a read command. The SDO output is high-Z at all times except during a read command.

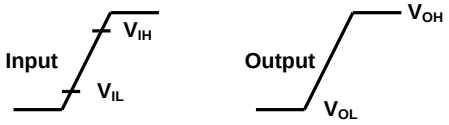


Figure 8. Electrical Level Diagram for Single-Ended Digital Inputs and Outputs

Timing Specifications

Unless otherwise noted, these specifications apply for $V_{A3.3}$= 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	MIN	TYP	MAX	UNITS
ADC SAMPLING INSTANT TIMING CHARACTERISTICS					
F_S	Sampling Rate Equal to F_{CLKIN} / CLKDIV	50		370	MSPS
F_{CLKIN}	Input Clock Frequency at CLKIN Inputs				MHz
	CLKDIV = 1	50		370	
	CLKDIV = 2	100		740	
	CLKDIV = 4	200		1,480	
	CLKDIV = 8	400		2,000	
$t_{LAT-ADC}$	ADC Core Latency Delay from a reference sampling instant to the boundary of the internal LMFC where the reference sample is the first sample of the next transmitted multi-frame. Coarse sampling phase adjust disabled. Includes SNRBoost and Bit-Burst signal processing and applies to both modes.		14.5		Frame Clock Cycles
t_J	Additive Sampling Aperture Jitter Depends on input CLKIN differential edge rate at the zero crossing, dV_{SS}/dt. Tested with 5 V/ns edge rate.				fs
	CLKDIV = 1		70		
	CLKDIV = 2, 4, Coarse Phase disabled		80		
	CLKDIV = 4, Coarse Phase enabled. Typical worst-case value across all coarse phase configuration possibilities.		145		
BIT-BURST INTERFACE TIMING CHARACTERISTICS (Bit-Burst Mode)					
t_{TRH}	TRIGGER Assertion Hold Time Required assertion duration of TRIGGER signal; TRIGGER is an asynchronous signal .	1.5			Frame Clock Cycles
t_{TD}	TRIGGER to Data Delay Delay between TRIGGER assertion detected and start of high-resolution data output on serial lanes; Single lane mode.			13	Frame Clock Cycles
t_{TRDL}	TRIGRDY De-assertion Delay Delay between TRIGGER assertion detected and TRIGRDY de-asserted.			2	Frame Clock Cycles
OVER-RANGE INTERFACE TIMING CHARACTERISTICS (SNRBoost Mode, OVRA, OVRB)					
t_{ODH}	OVR Assertion Delay Delay between an over-range value sampled and OVR asserted; Coarse clock phase adjust disabled.		7.5		Frame Clock Cycles
t_{ODL}	OVR De-assertion Delay Delay between first under-range value sampled until OVR de-assertion; Configurable via SPI.	t_{ODH} + 0		t_{ODH} + 15	Frame Clock Cycles
SYSREF TIMING CHARACTERISTICS					
t_{PH-SYS}	SYSREF Assertion Duration Required duration of SYSREF assertion after rising edge event	2			Frame Clock Cycles
t_{PL-SYS}	SYSREF De-Assertion Duration Required duration of SYSREF de-assertion after falling edge event	2			Frame Clock Cycles
t_{S-SYS}	SYSREF Setup Time Relative to CLKIN rising edge		320		ps
t_{H-SYS}	SYSREF Hold Time Relative to CLKIN rising edge		80		ps

Timing Specifications (continued)

Unless otherwise noted, these specifications apply for $V_{A3.3}$= 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	MIN	TYP	MAX	UNITS
JESD204B INTERFACE LINK TIMING CHARACTERISTICS					
t_{D-LMFC}	SYSREF to LMFC Delay Functional delay between SYSREF assertion latched and LMFC frame boundary. Depends on CLKDIV setting.				CLKIN Cycles (Frame Clock Cycles)
	CLKDIV = 1		3.5 (3.5)		
	CLKDIV = 2		8 (4)		
	CLKDIV = 4		15 (3.75)		
	CLKDIV = 8		29 (3.625)		
t_{D-K28}	LMFC to K28.5 Delay Functional delay between the start of the first K28.5 frame during Code Group Synchronization at the serial output and the preceding LMFC frame boundary.	5	6	7	Frame Clock Cycles
t_{D-ILA}	LMFC to ILA Delay Functional delay between the start of the first ILA frame during Initial Lane Synchronization at the serial output and the preceding LMFC frame boundary	5	6	7	
t_{D-DATA}	LMFC to Valid Data Delay Functional delay between the start of the first valid data frame at the serial output and the preceding LMFC frame boundary.	5	6	7	
$t_{S-SYNCb-F}$	SYNCb Setup Time Required SYNCb setup time relative to the internal LMFC boundary.		3		Frame Clock Cycles
$t_{H-SYNCb-F}$	SYNCb Hold Time Required SYNCb hold time relative to the internal LMFC boundary .		0		
$t_{H-SYNCb}$	SYNCb Assertion Hold Time Required SYNCb hold time after assertion before de-assertion to initiate a link re-synchronization.		4		
t_{ILA}	ILA Duration Duration of the ILA sequence .		4		Multi-Frame Clock Cycles
SERIAL OUTPUT DATA TIMING CHARACTERISTICS					
F_{SR}	Serial Bit Rate Single or Dual lane mode	1.0		7.4	Gb/s
UI	Unit Interval 7.4 Gb/s Data Rate		135.1		ps
DJ	Deterministic Jitter Includes Periodic Jitter (PJ), Data Dependent Jitter (DDJ), Duty Cycle Distortion (DCD) and Inter-Symbol Interference (ISI); 7.4 Gb/s Data Rate.		0.047 (6.33)		p-p UI (p-p ps)
RJ	Random Jitter Assumes BER of 1e-15 (Q=15.88); 7.4 Gb/s Data Rate		0.156 (1.35)		p-p UI (rms ps)
TJ	Total Jitter Sum of DJ and RJ. Assumes BER of 1e-15 (Q=15.88); 7.4 Gb/s Data Rate.		0.206 (27.77)		p-p UI (p-p ps)
SPI BUS TIMING CHARACTERISTICS (1)					
f_{SCLK}	Serial Clock Frequency f_{SCLK} = 1 / t_P			20	MHz
t_{PH}	SCLK Pulse Width – High % of SCLK Period	25		75	%
t_{PL}	SCLK Pulse Width – Low % of SCLK Period	25		75	%
t_{SSU}	SDI Input Data Setup Time	5			ns

(1) All timing specifications for the SPI interface given for V_{SPI}=1.8 V logic levels and a 5pF capacitive load on the SDO pin. Timing specification may require larger margins for V_{SPI}=1.2 V.

Timing Specifications (continued)

Unless otherwise noted, these specifications apply for $V_{A3.3}$= 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS. Typical values are at T_A =+25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply at T_A =+25°C, unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITIONS	MIN	TYP	MAX	UNITS
t_{SH}	SDI Input Data Hold Time	5			ns
t_{ODZ}	SDO Output Data Driven-to-Tri-State Time			25	ns
t_{OZD}	SDO Output Data Tri-State-to-Driven Time			25	ns
t_{OD}	SDO Output Data Delay Time			30	ns
t_{CSS}	CSB Setup Time	5			ns
t_{CSH}	CSB Hold Time	5			ns
t_{IAG}	Inter-Access Gap Minimum time CSB must be de-asserted between accesses	5			ns

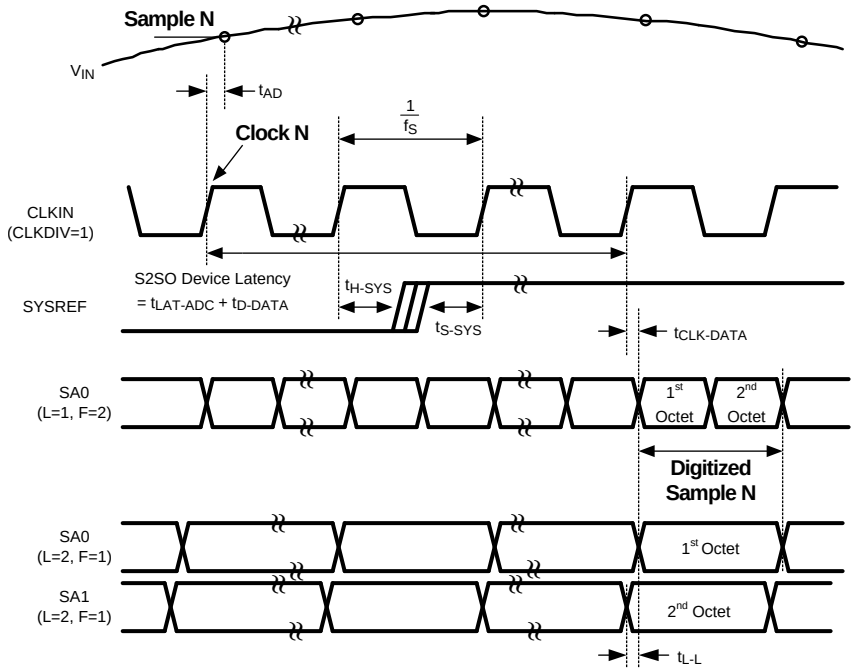


Figure 9. Sample to Data Timing Diagram

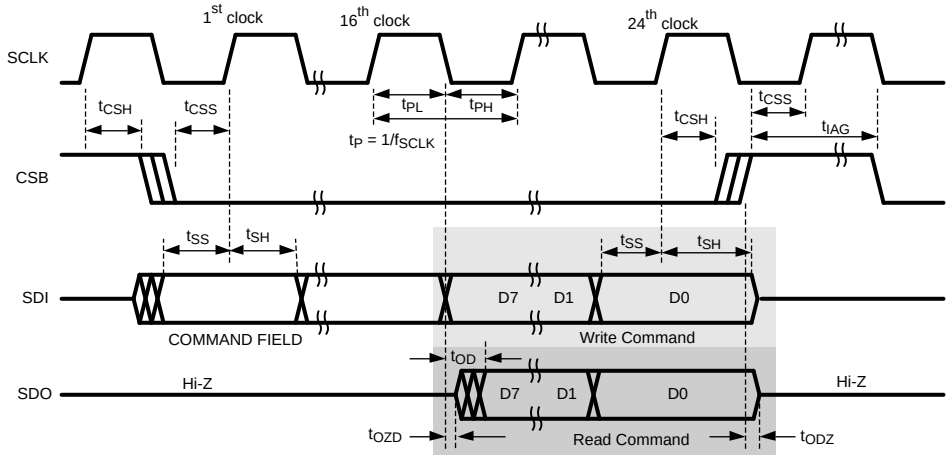


Figure 10. SPI Timing Diagram

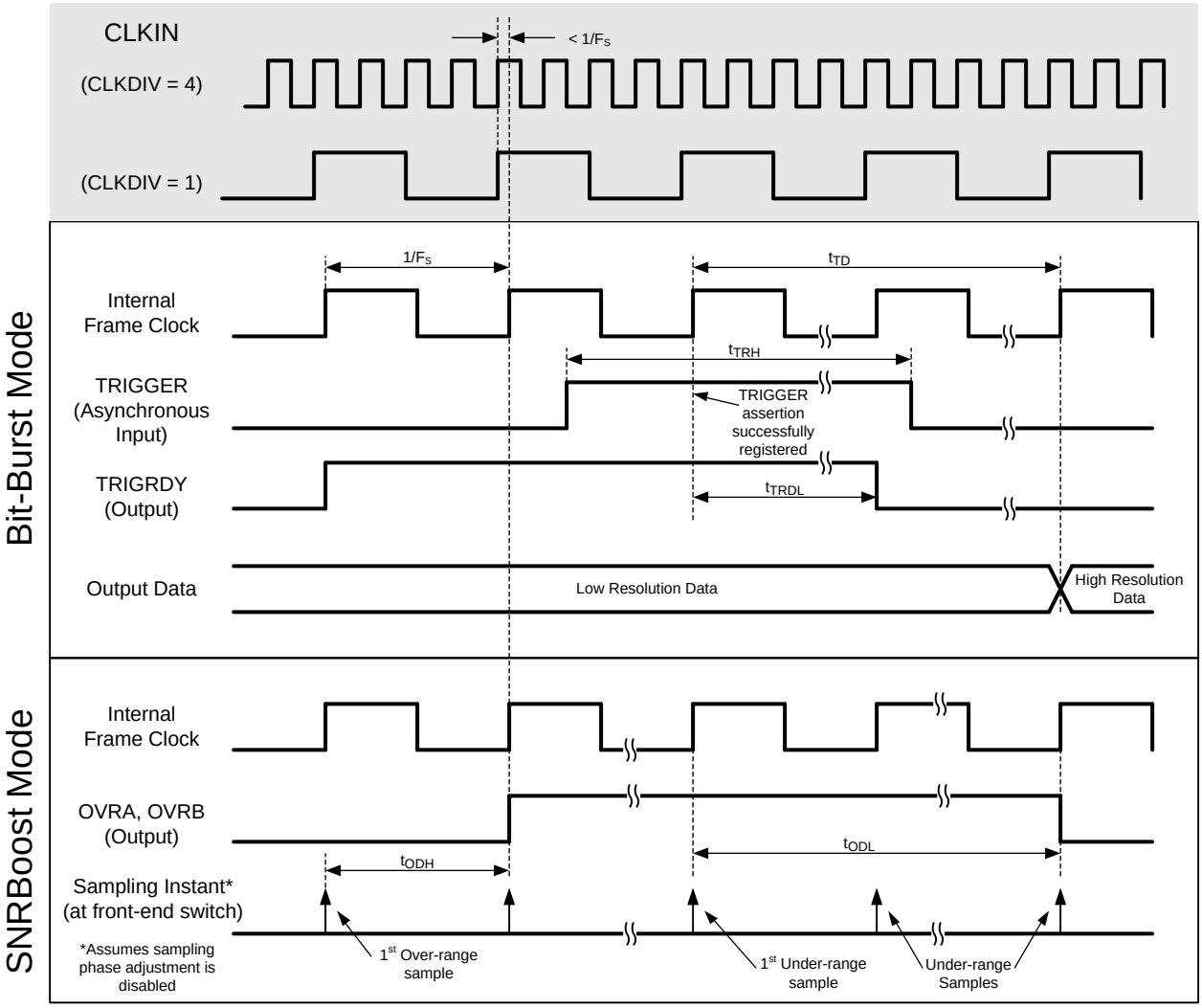


Figure 11. Trigger and Over-Range Timing Diagrams

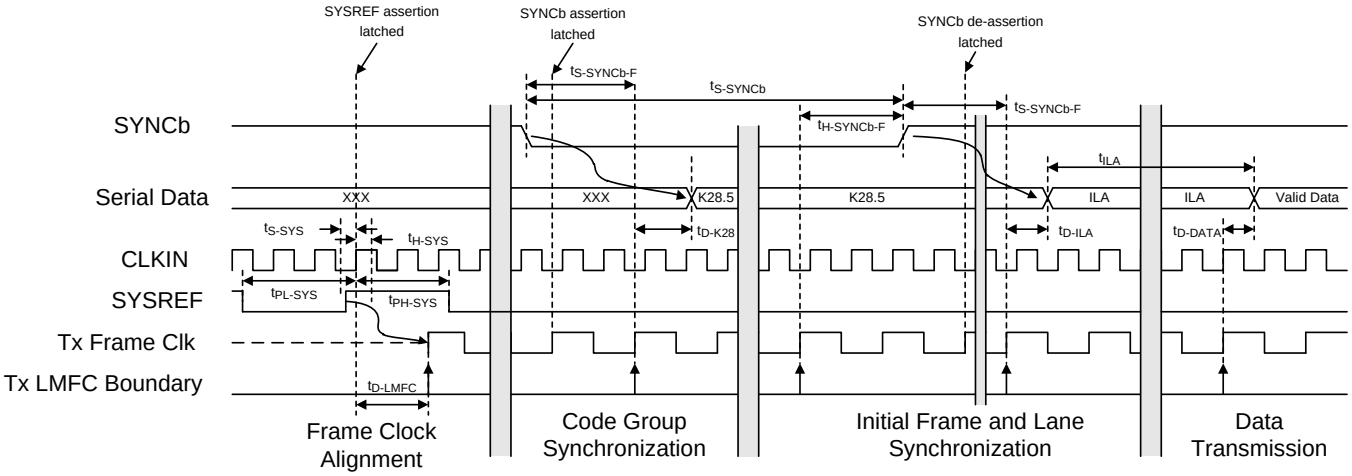


Figure 12. JESD204B Interface Link Initialization Timing Diagram

SPECIFICATION DEFINITIONS

APERTURE DELAY is the time delay between the rising edge of the clock until the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both terminals of the ADC differential input.

COMMON MODE REJECTION RATIO (CMRR) is the ratio of the magnitude of the single-tone spur in the sampled spectrum (referred to the ADC analog input as a peak voltage quantity) to the peak voltage swing of a sinusoid simultaneously incident on both the positive and negative terminals of a differential analog input as a common-mode signal from which the spur generated. CMRR is typically expressed in decibels [dB].

SAMPLE TO SERIAL OUT (S2SO) LATENCY is the number of frame clock cycles between initiation of conversion and the time when the first bit of serial data for that sample is present at the output driver. This latency is not guaranteed to be deterministic.

SAMPLE TO PARALLEL OUT (S2PO) LATENCY is the number of frame clock cycles between initiation of conversion and the time when the parallel sample data is available at the output of the receiver's elastic buffer. This latency is guaranteed to be deterministic if the JESD204B subclass 1 requirements are satisfied.

CROSSTALK is the coupling of energy from one channel into the other channel.

3dB BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental deviates 3 dB from its low frequency value relative to the differential voltage signal applied at the device input pins.

GAIN VARIATION is the expected standard deviation in the gain of the converter from an applied voltage to output codes between parts or between channels.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It quantifies the power of the largest intermodulation product adjacent to the input tones, expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

OFFSET ERROR is the difference between the two input voltages (VIN+ – VIN-) required to cause a transition from code 32767LSB and 32768LSB with offset binary data format.

POWER SUPPLY SENSITIVITY is a measure of the sensitivity of the power supplies to noise. In this specification, a supply is modulated with a 100mV, 500kHz sinusoid and the resulting spurs in the spectrum are measured. The sensitivity is expressed relative to the power of a possible full-scale sinusoid [dBFS].

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the power of the input signal to the total power of all other spectral components, not including harmonics and DC. SNR is usually expressed relative to the power of a possible full-scale sinusoid [dBFS] or relative to the power of the actual input carrier signal [dBc].

SIGNAL TO NOISE AND DISTORTION (SINAD) is the ratio, expressed in dB, of the power of the input signal to the total power of all of the other spectral components, including harmonics but excluding DC. SINAD is usually expressed relative to the power of a possible full-scale sinusoid [dBFS] or relative to the power of the actual input carrier signal [dBc].

SPUR is the ratio, expressed in dB, of the power of the peak spurious signal to the power of the input signal, where a spurious signal is any signal present in the output spectrum that is not present at the input excluding the second and third harmonic distortion. SPUR is usually expressed relative to the power of a possible full-scale sinusoid [dBFS] or relative to the power of the actual input carrier signal [dBc].

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the ratio, expressed in dB, of the input signal power to the peak spurious signal power, where a spurious signal is any signal present in the output spectrum that is not present at the input. SINAD is usually expressed relative to the power of a possible full-scale sinusoid [dBFS] or relative to the power of the actual input carrier signal [dBc].

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the total power of the first eight harmonics (HD2 through HD9) to the input signal power. THD is usually expressed relative to the power of a possible full-scale sinusoid [dBFS] or relative to the power of the actual input carrier signal [dBc].

SECOND HARMONIC DISTORTION (2ND HARM or HD2) is the ratio, expressed in dB, of the power of the input signal's 2nd harmonic to the power of the input signal. HD2 is usually expressed relative to the power of a possible full-scale sinusoid [dBFS] or relative to the power of the actual input carrier signal [dBc].

THIRD HARMONIC DISTORTION (3RD HARM or HD3) is the ratio, expressed in dB, of the power of the input signal's 3rd harmonic to the power of the input signal. HD3 is usually expressed relative to the power of a possible full-scale sinusoid [dBFS] or relative to the power of the actual input carrier signal [dBc].

JESD204B DEFINITIONS

DEVICE CLOCK is a master clock signal from which a device must generate its local frame and local multi-frame clocks. For the LM97937, this refers to the signal at the CLKIN input.

FRAME is a set of consecutive octets in which the position of each octet can be identified by references to a frame alignment signal.

FRAME CLOCK is a signal used for sequencing frames or monitoring their alignment. For the LM97937, this clock is internally generated and is not externally accessible.

SERIAL LANE is a differential signal pair for data transmission in one direction.

LINK (DATA LINK) is an assembly, consisting of parts of two devices and the interconnecting data circuit, that is controlled by a long protocol enabling data to be transferred from a data source to a data sink. The link includes portions of the LM97937 (transmitter), FPGA or ASIC (receiver), and the hardware that connects them.

MULTI-FRAME is a set of consecutive frames in which the position of each frame can be identified by reference to a multi-frame alignment signal.

LOCAL MULTI-FRAME CLOCK (LMFC) is a signal used for sequencing multi-frames or monitoring their alignment. This clock is derived inside the LM97937 from the device clock and used in the implementation of the JESD204B link within the device.

OCTET is a group of eight adjacent binary digits, serving as the input to an 8B/10B encoder or the output of an 8B/10B decoder.

SYSREF is a periodic, one-shot, or "gapped" periodic signal used to align the boundaries of local multi-frame clocks in JESD204B subclass 1 compliant devices. SYSREF must be source synchronous with the device clock.

SCRAMBLING is the randomization of the output data that is used to eliminate long strings of consecutive identical transmitted symbols and avoid the presence of spectral lines in the signal spectrum without changing the signaling rate.

TYPICAL CHARACTERISTICS (SNRBoost Mode)

Unless otherwise noted, these specifications apply for SNRBoost Mode, $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; SNRBoost F_C=0.25*F_S; external differential resistive termination at ADC input is 66 Ω; -3 dBFS input power. Typical values are at T_A =+25°C.

Unless otherwise noted, these specifications apply for SNRBoost Mode, $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; SNRBoost F_C=0.25*F_S; external differential resistive termination at ADC input is 66 Ω; -3 dBFS input power. Typical values are at T_A =+25°C.

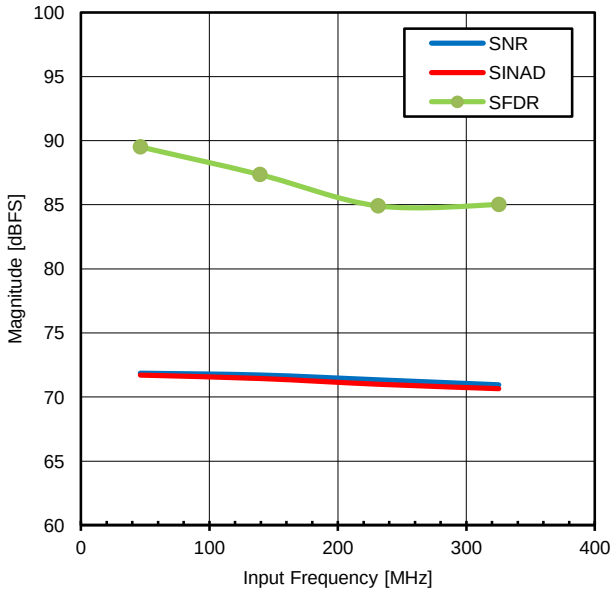


Figure 13. SNR, SINAD, SFDR vs. Input Frequency

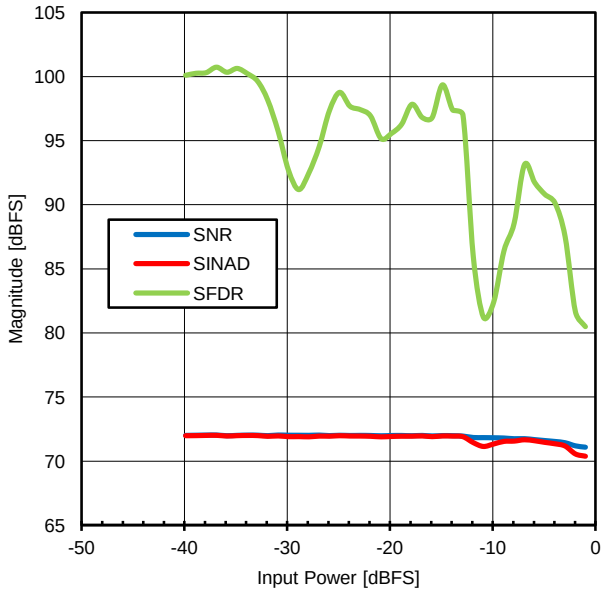


Figure 14. SNR, SINAD, SFDR vs. Input Power (150 MHz, F_C=0.29*F_S)

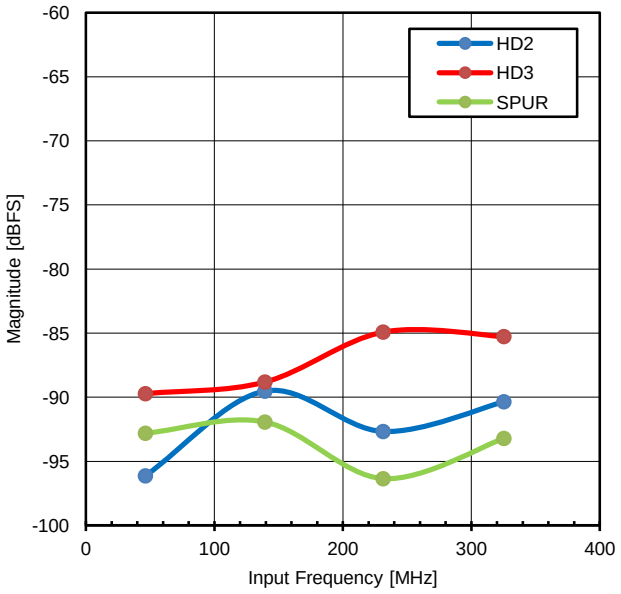


Figure 15. HD2, HD3, SPUR vs. Input Frequency

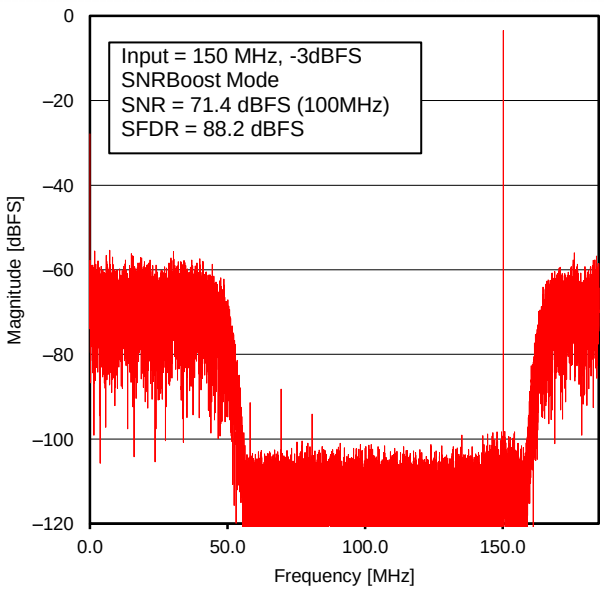


Figure 16. 1-Tone Spectrum (150 MHz, F_C=0.29*F_S)

Unless otherwise noted, these specifications apply for SNRBoost Mode, $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; SNRBoost F_C=0.25*F_S; external differential resistive termination at ADC input is 66 Ω; -3 dBFS input power. Typical values are at T_A =+25°C.

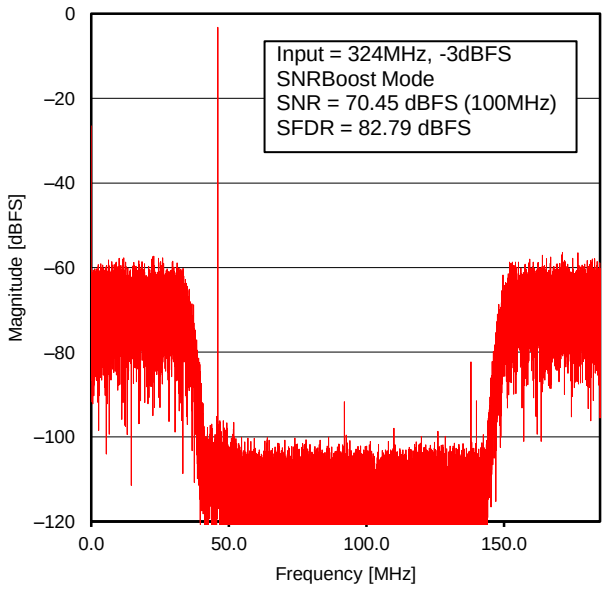


Figure 17. 1-Tone Spectrum (324 MHz)

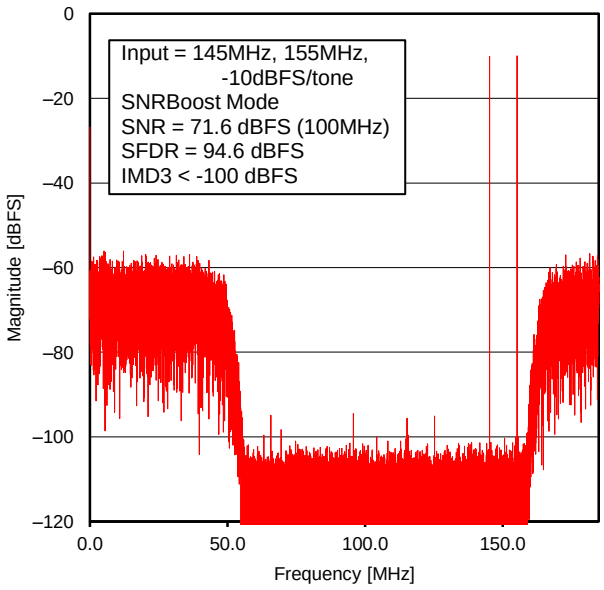


Figure 18. 2-Tone Spectrum (-10dBFS/tone, 145 & 155 MHz, F_C=0.29*F_S)

TYPICAL CHARACTERISTICS (Bit-Burst Mode)

Unless otherwise noted, these specifications apply for Bit-Burst Mode, $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; Bit-Burst data in Hi-Res phase; 150 MHz input frequency; -3 dBFS input power. Typical values are at T_A =+25°C.

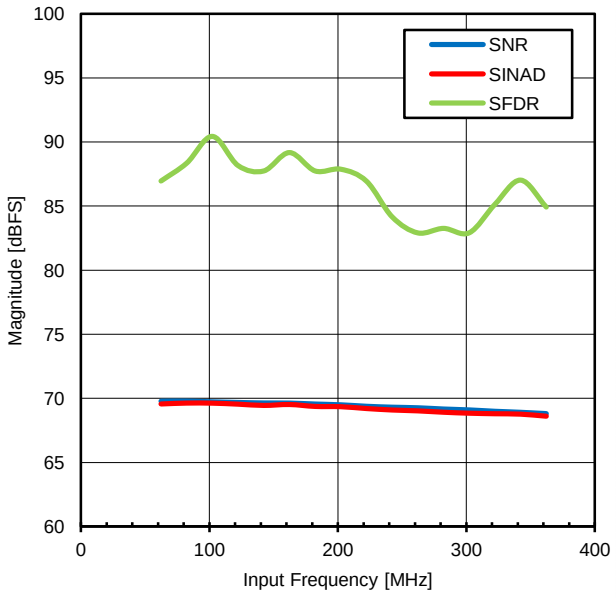


Figure 19. SNR, SINAD, SFDR vs. Input Frequency

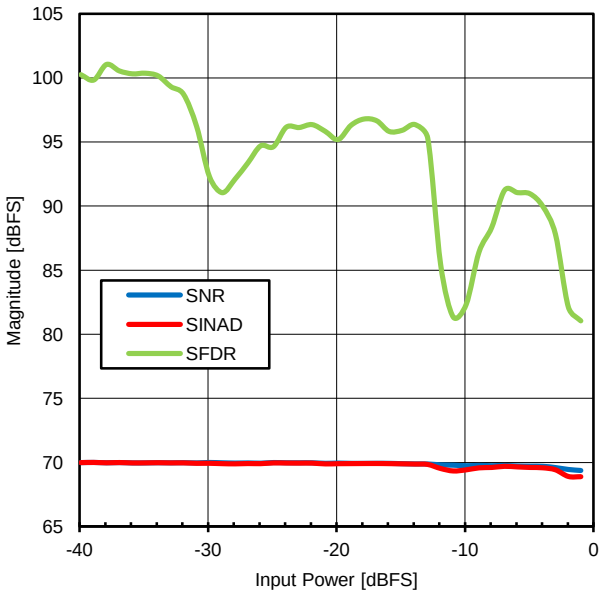


Figure 20. SNR, SINAD, SFDR vs. Input Power

Unless otherwise noted, these specifications apply for Bit-Burst Mode, $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; Bit-Burst data in Hi-Res phase; 150 MHz input frequency; -3 dBFS input power. Typical values are at T_A =+25°C.

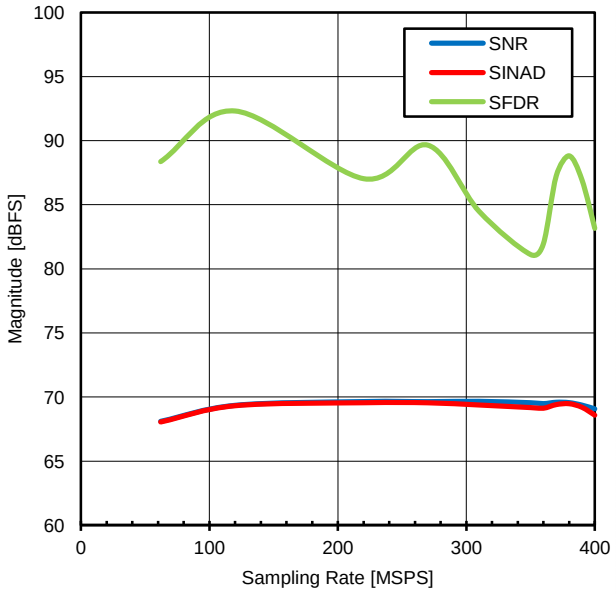


Figure 21. SNR, SINAD, SFDR vs. Sampling Rate

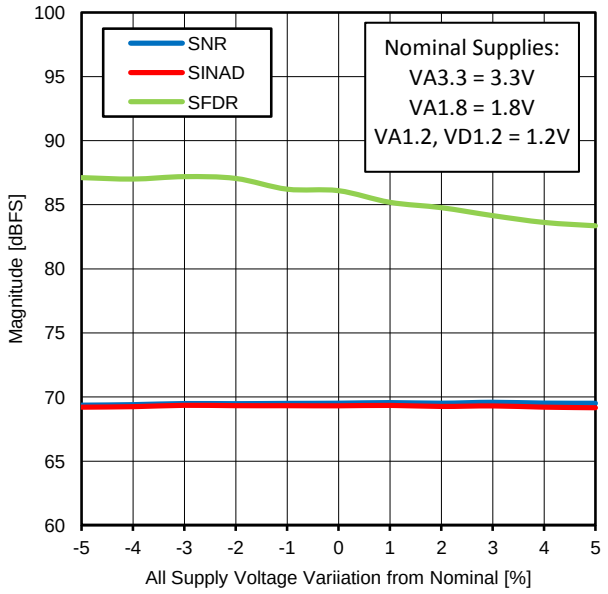


Figure 22. SNR, SINAD, SFDR vs. Supply

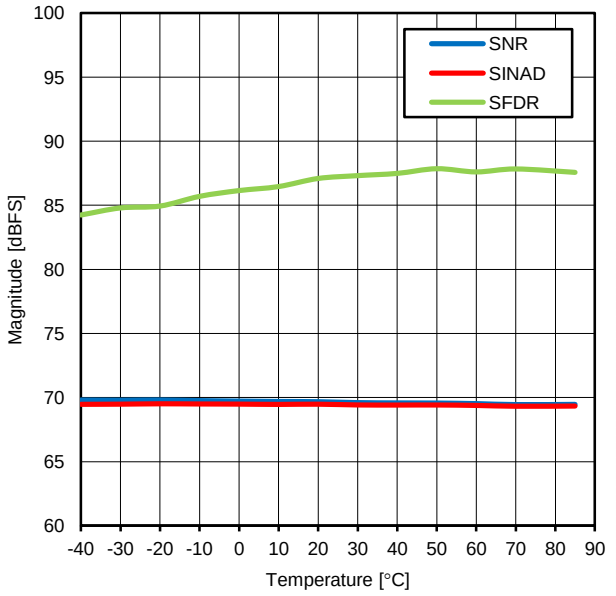


Figure 23. SNR, SINAD, SFDR vs. Temperature (150 MHz)

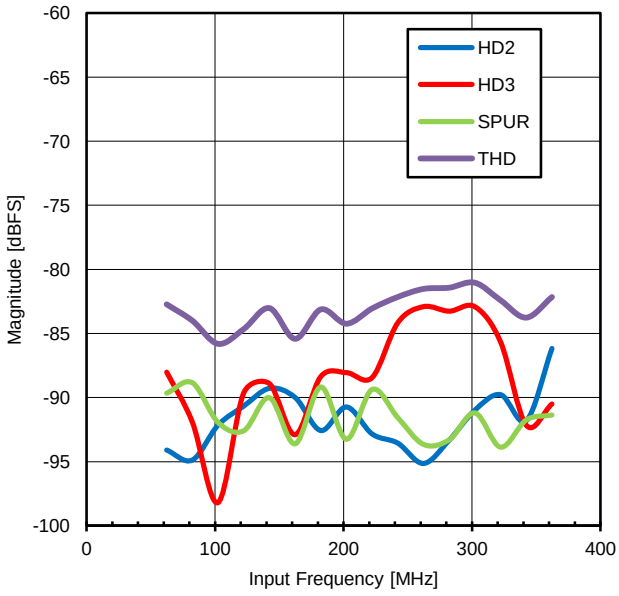


Figure 24. HD2, HD3, SPUR, THD vs. Input Frequency

Unless otherwise noted, these specifications apply for Bit-Burst Mode, $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; Bit-Burst data in Hi-Res phase; 150 MHz input frequency; -3 dBFS input power. Typical values are at T_A =+25°C.

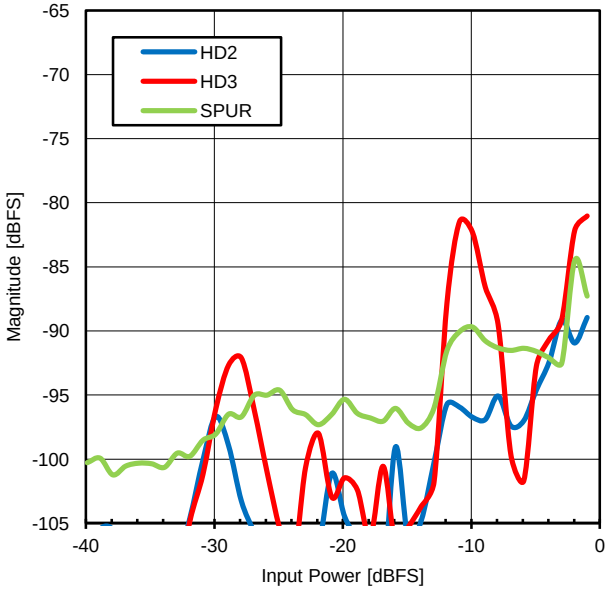


Figure 25. HD2, HD3, SPUR, THD vs. Input Power

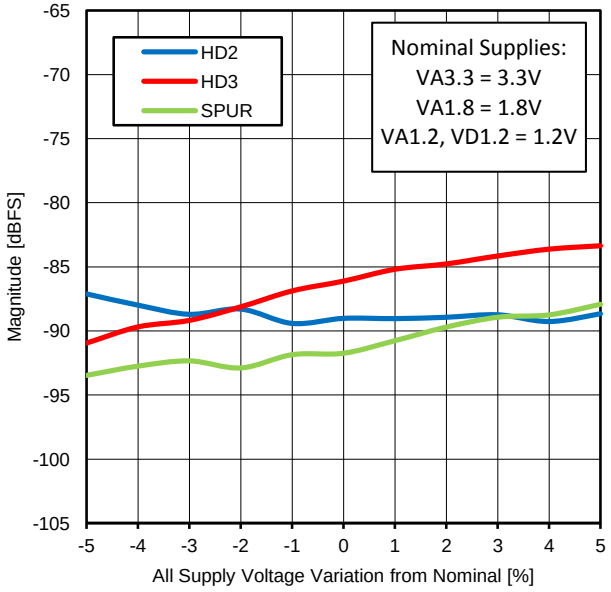


Figure 26. HD2, HD3, and SPUR vs. Supply

Figure 27. HD2, HD3, SPUR, THD vs. Temperature

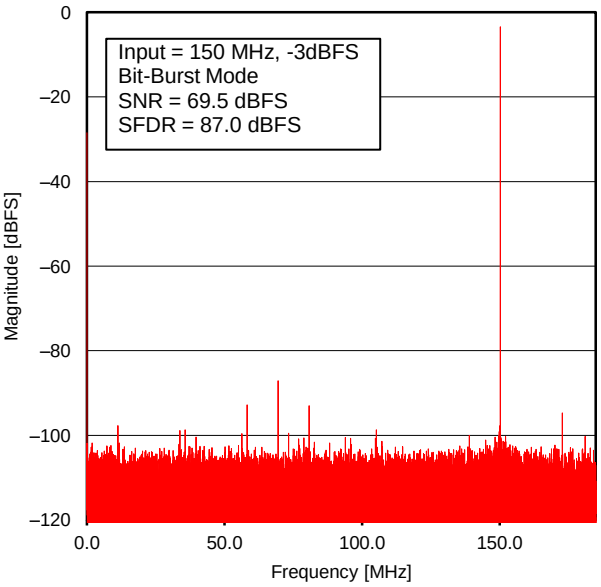


Figure 28. 1-Tone Spectrum, Hi-Res Mode

Unless otherwise noted, these specifications apply for Bit-Burst Mode, $V_{A3.3}$ = 3.1 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; Bit-Burst data in Hi-Res phase; 150 MHz input frequency; -3 dBFS input power. Typical values are at T_A =+25°C.

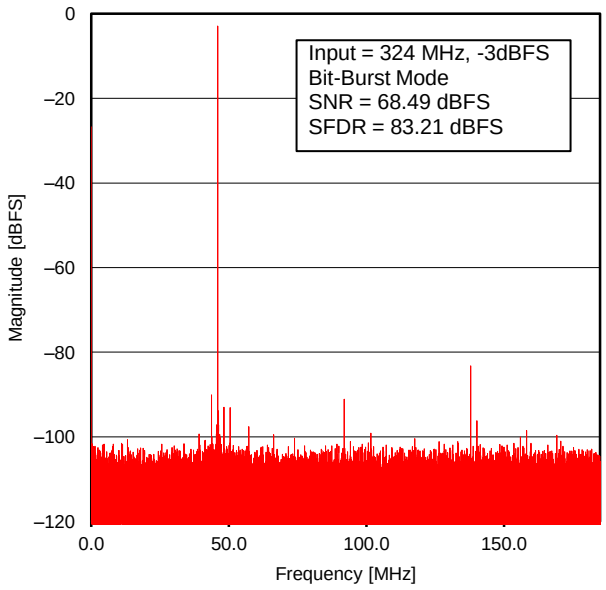


Figure 29. 1-Tone Spectrum, Hi-Res Mode (324 MHz)

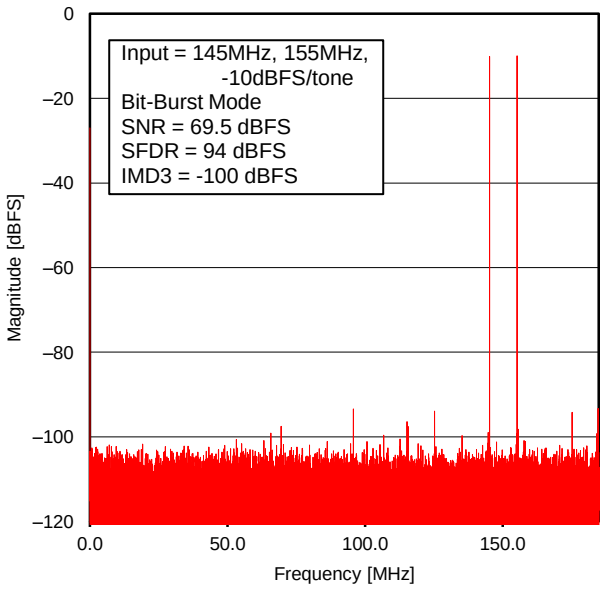


Figure 30. 2-Tone Spectrum (-10dBFS/tone, 145 & 155 MHz)

TYPICAL CHARACTERISTICS (Common)

Unless otherwise noted, these specifications apply for SNRBoost Mode, $V_{A3.3}$ = 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; -3 dBFS input power. Typical values are at T_A =+25°C.

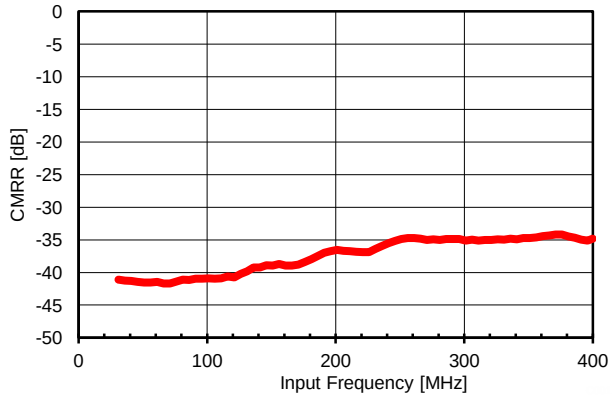


Figure 31. CMRR vs. Input Frequency (small signal, -24dBm input)

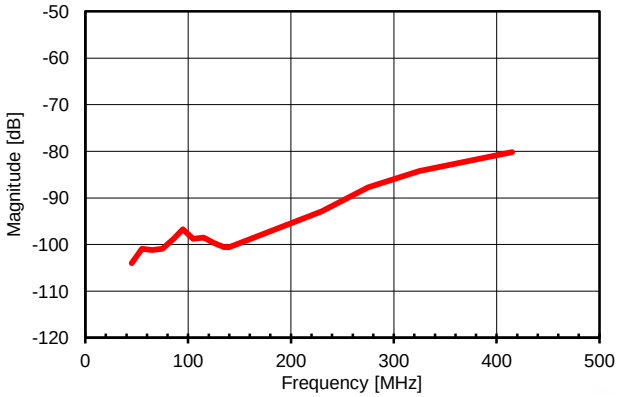


Figure 32. Crosstalk vs. Input Frequency

Unless otherwise noted, these specifications apply for SNRBoost Mode, $V_{A3.3}$ = 3.3 V; $V_{A1.8}$ = 1.8 V; $V_{A1.2}$ = $V_{D1.2}$ = 1.2 V; F_{CLKIN} = F_S = 370 MSPS; -3 dBFS input power. Typical values are at T_A =+25°C.

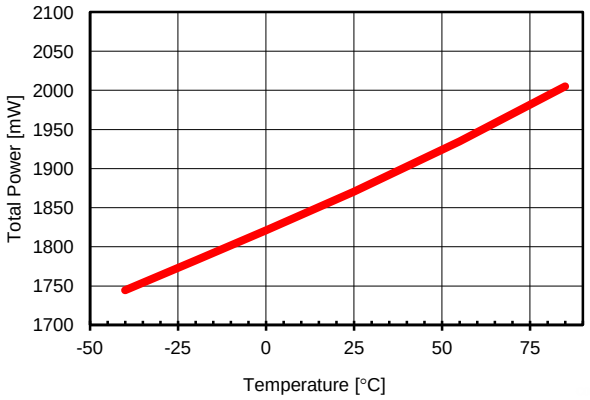


Figure 33. Power vs. Temperature

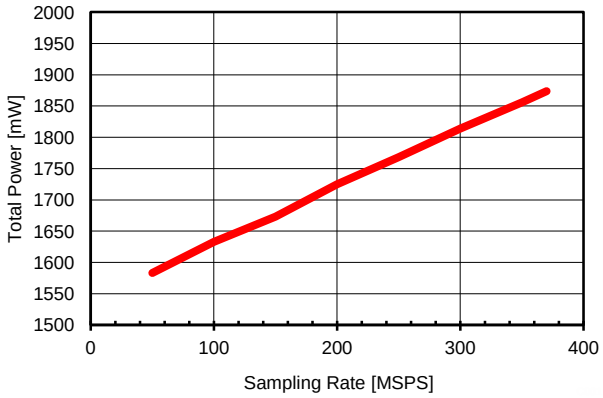


Figure 34. Power vs. Sampling Rate

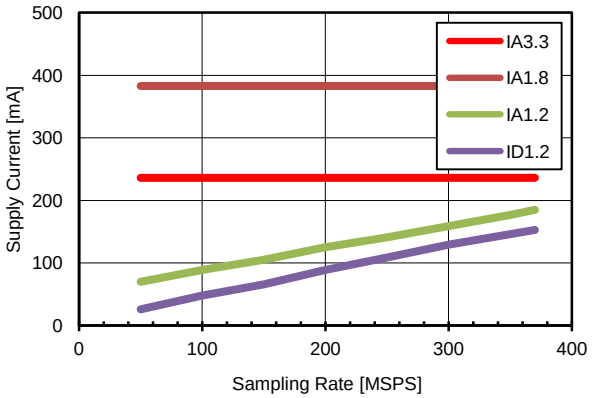


Figure 35. Current vs. Sampling Rate

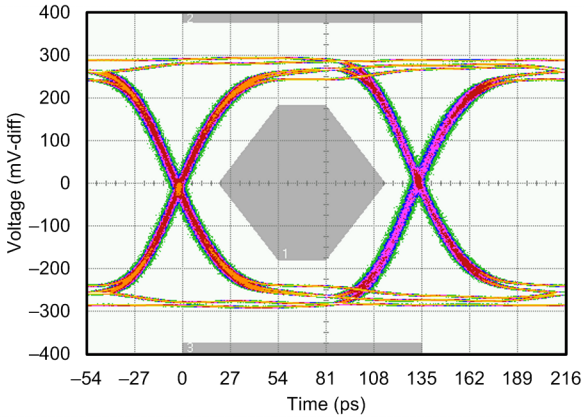


Figure 36. Output Serial Lane Eye Diagram at 7.4Gb/s

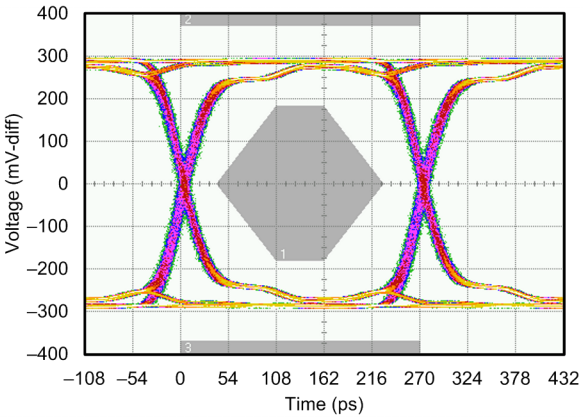


Figure 37. Output Serial Lane Eye Diagram at 3.7Gb/s

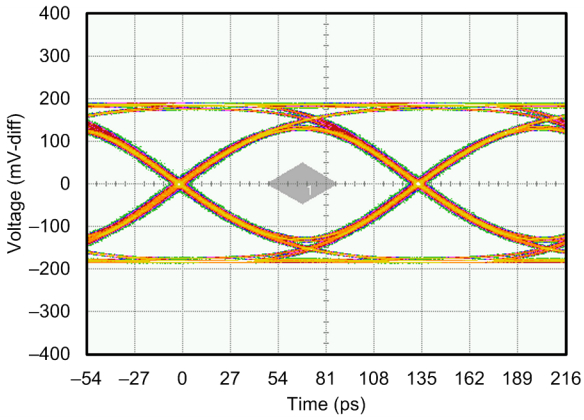


Figure 38. Transmitted Eye at Output of 20in. 5 mil. FR4 Microstrip at 7.4Gb/s with Optimized De-Emphasis

Functional Description

Architecture Summary

The LM97937 is a dual analog signal receiver composed of pipelined ADC cores followed by back-end digital signal processing. Each ADC core is preceded by an input buffer and imbalance correction circuit at the analog input and is provided with the necessary reference voltages with internal drivers that require no external components. The analog input common-mode is also internally regulated.

This multi-purpose device may be configured in one of two basic signal processing modes: SNRBoost or Bit-Burst. SNRBoost places a quantization noise modulator in the signal path and outputs 9-bit data. Bit-Burst mode modulates the output resolution between high-resolution and low-resolution phases. Over-range and Bit-Burst Triggering signals are externally available on pins to monitor and interact with the signal path. A DC Offset Correction block is disabled by default but may be enabled at the ADC core output to remove DC offset. Processed data is passed into the JESD204B interface where the data is framed, encoded, serialized, and output on 1 or 2 lanes per channel. Data is serially transmitted by configurable high-speed voltage mode drivers.

The sampling clock is derived from the CLKIN input via a low-noise receiver and clock divider. A Coarse Phase Adjustment block in the clock signal path controls the phase of the sampling instant. The CLKIN, SYSREF and SYNCb inputs provide the device clock, sysref, and sync~ signals to the JESD204B interface that are used to derive the internal local frame and local multi-frame clocks and establish the serial link.

Features of the LM97937 are configurable via the 4-wire SPI interface.

SNRBoost Mode

The SNRBoost technology overcomes the basic limitations of quantization noise and increases the dynamic range of the output spectrum at the cost of increased noise at the edges of the spectrum that remain unused in many applications. When the device is configured in SNRBoost Mode, 54.6% of the Nyquist band obtains increased dynamic range and gives the spectrum a bandpass noise shaping. This allows up to 101MHz of high dynamic range bandwidth when sampling at 370MSPS. The SNR Boost block may be configured to have the center of the low-noise spectrum located at 0.25*Fs or 0.29*Fs or 0.21*Fs as shown in Figure 39.

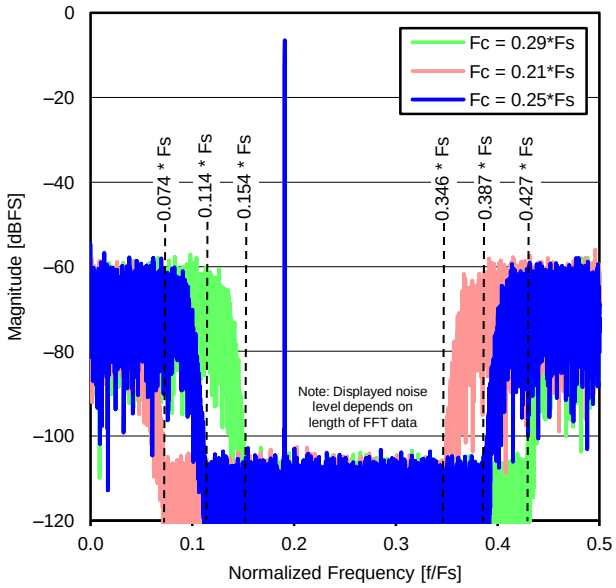


Figure 39. SNRBoost Noise Shaping for the Three Different Center Frequencies

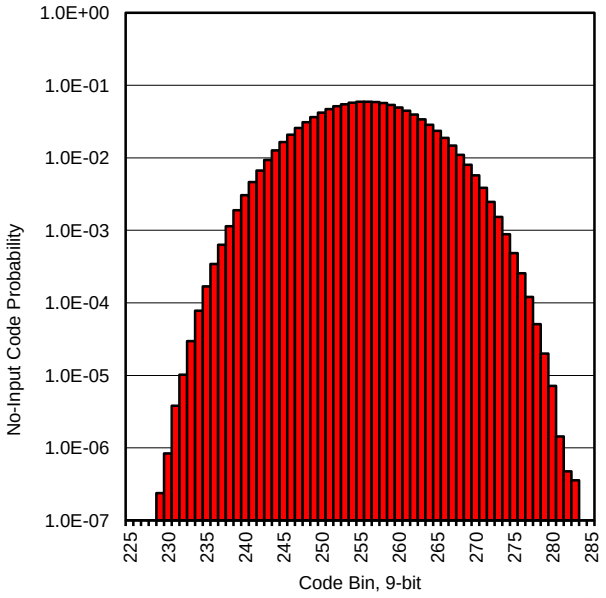


Figure 40. SNRBoost Quantization Noise Code Probability with No Input Signal

Quantization noise shaping also affects other properties of the noise including the peak-to-average ratio (PAR) and total quantization noise. The PAR is the ratio of the peak deviation from the average value to the standard deviation and may be extracted from the Gaussian quantization noise probability density shown in Figure 40. The standard deviation of the probability density is 6.5 codes. The "peak" value is a statistical quantity that must be described as a probability. The probability of a code deviating from the average by 26 LSB is approximately 1 ppm. Therefore, the PAR for an error rate less than 1ppm is 20*log10(26/6.5) = 12dB. The total quantization noise in the signal spectrum is the integration of the noise in the spectrum and is simply another representation of the noise standard deviation, in this case equal to -31.5 dBFS where the noise is given relative to the RMS power of a full scale sinusoid.

The SNRBoost block outputs a 9-bit digital word that can accommodate codes 0 to 511. For large signals, clipping may occur within the 9-bit code range as a result of a large input signal summed together with the large amount of noise generated by the SNRBoost block. For a large sinusoidal signal, clipping events begin to occur near -0.8 dBFS. At this input level, the -31.5dBFS additional quantization noise with a 12 dBFS PAR causes the output data to clip at the bounds of the 9-bit code range. Figure 41 quantifies the increase in the rate of clipped data samples as the amplitude of a near full scale sinusoid is increased when the device is in SNRBoost mode.

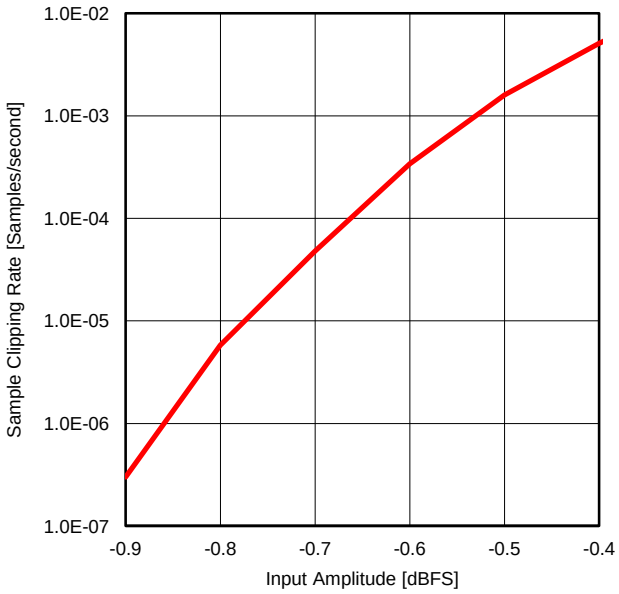


Figure 41. Rate of Clipped Samples in SNRBoost Mode for a Near Full-Scale Sinusoidal Input

Bit-Burst Mode

Bit Burst mode provides a temporary increase in dynamic range by enabling High Resolution ADC bits for a brief period of time before returning to 9-bit resolution. The alternating frequency of the resolution is described by its duty cycle and by the High Resolution burst duration. Configuration of the High Resolution bits and duty cycle is programmable according to Table 1. The duration of the High Resolution phase is equal to 2^N samples where N may be programmed from 10 to 25. The duration of the Low Resolution phase is equal to 2^N*(1/k-1) where k determines the duty cycle. Table 1 summarizes the Bit-Burst functional properties for the two possible configurations.

Table 1. Bit-Burst Configuration

Resolution Configuration	High-Res Resolution	Low-Res Resolution	Duty Cycle	Burst Cycle Period
0 (default)	14-bits	9-bits	¼	= 2^N / k (Stream Mode), > 2^N / k (Trigger Mode)
1	12-bits	9-bits	½	

The Bit-Burst mode of operation has two sub-modes called Trigger Mode and Stream Mode. In the Trigger Mode, the High Resolution bits become active with a low-to-high assertion of the TRIGGER input signal. A short trigger delay exists that lasts from when the trigger signal is latched until high-resolution data is available at the output. After a burst cycle is initiated with a TRIGGER assertion, the TRIGGER signal is ignored until the burst cycle is finished. The TRIGRDY signal de-asserts (low) after a TRIGGER assertion to indicate that a burst cycle is in progress and asserts (high) when the burst cycle is complete and a new cycle may be triggered.

In Stream Mode, the High Resolution bits become active periodically in a constant stream and the TRIGGER signal is ignored. The Flag control bit in the output serial data stream indicates the status of the data in the burst period. When the Flag bit is logic high (1), the ADC is in the High Resolution phase. When Flag is logic low (0), the ADC is in the Low Resolution phase. When in the Stream mode, the duty cycle is equal to k and the High Resolution burst period is equal to 2^N / k.

Both Bit-Burst sub-modes have a mandatory low-resolution phase that occurs after power-up, after a soft reset, or after changing modes. During this phase, low resolution data is output for 2^N*(1/k-1) samples, where N and k are determined by the default register settings (after power-up) or determined by the current state of the registers (after sleep mode or after a soft reset or after changing modes).

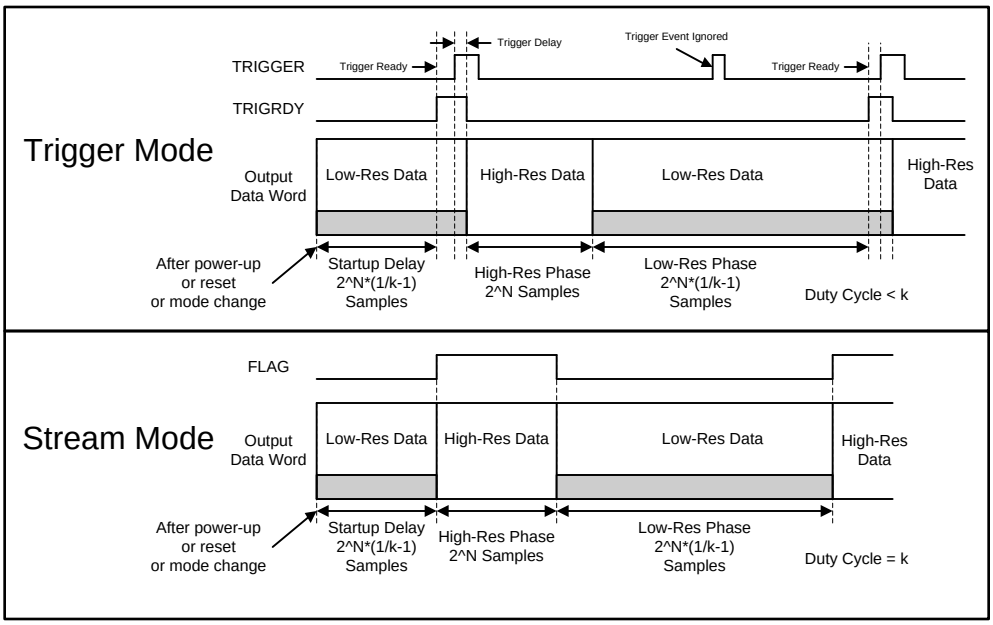


Figure 42. Bit-Burst Timing Diagram for Trigger and Stream Modes

DC Offset Correction

DC offset correction is provided using a digital high-pass IIR filter at the immediate output of the ADC core. The DC offset correction is bypassed by default but may be enabled and configured via the SPI interface. The 3dB bandwidth of the IIR digital correction filter may be set to four different low-frequency values. When DC offset correction is enabled, any signal in the stop-band of the high-pass filter is attenuated. The settling time of the DC offset correction is approximately equal to the inverse of the 3dB bandwidth setting.

Over-Range Detection

Separate over-range detection output signals for channels A and B are dedicated to pins when the device is configured in SNRBoost Mode. The OVRA pin asserts (high) when an over-range signal is detected at the input of channel A. The short delay from when an over-range signal is incident at the input until the OVRA is asserted allows for almost immediate detection of over-range signals without delay from the internal ADC pipeline latency or data serialization latency. OVRB responds similarly when an over-range signal is detected at the input of channel B.

The input power threshold to indicate an over-range event is programmable via the SPI interface from full scale code range down to a +/-128 LSB code range in steps of 128 codes relative to the 16-bit code range of the data at the output of the ADC core before entering the SNRBoost block.

After an over-range event occurs and the signal at the channel input reduces to a level below full-scale, an internal counter begins counting to provide a hold function. When the counter reaches a programmable counter threshold, the OVRA (or OVRB) signal is de-asserted. The duration of the hold counter is programmable via the SPI interface to hold for +3, +7, or +15 frame clock cycles. The counter is disabled (+0 cycles) by default to allow de-assertion without holding. Each channel has an independent hold counter but the hold duration value is common to both channels.

The over-range signals are not available when the device is configured in Bit-Burst Mode.

Amplitude and Phase Imbalance Correction of Differential Analog Input

The ADC performance can be sensitive to amplitude and phase imbalance of the input differential signal and therefore integrates a front-end balance correction circuit to optimize the second-order distortion (HD2) performance of the ADC in the presence of an imbalanced input signal. 4-bit control of the phase mismatch and 3-bit control of the amplitude mismatch corrects the input mismatch before the input buffer. A simplified diagram of the amplitude and phase correction circuit at the ADC input is shown in Figure 43.

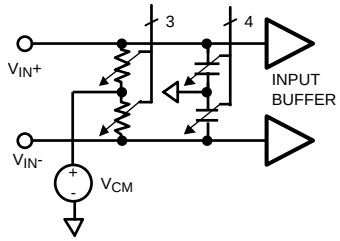


Figure 43. Simplified Input Differential Balance Correction Circuit

The amplitude correction is achieved by varying the single-ended termination resistance of each input while maintaining constant total differential resistance, thereby adjusting the amplitude at each input but leaving the differential swing constant. Phase correction, also considered capacitive balance correction, varies the capacitive load at the ADC input thereby correcting a phase imbalance by creating a bandwidth difference between the analog inputs that minimally affects amplitude. This function is useful for correcting the balance of transformers or filters that drive the ADC analog inputs. Figure 44 shows the measured HD2 resulting from an example 250MHz imbalanced signal input into the LM97937 recorded over the available amplitude and phase correction settings, demonstrating the optimization of HD2. Performance parameters in the Converter Dynamic Performance Characteristics (SNRBoost Mode) are characterized with the amplitude and phase correction settings in the default condition.

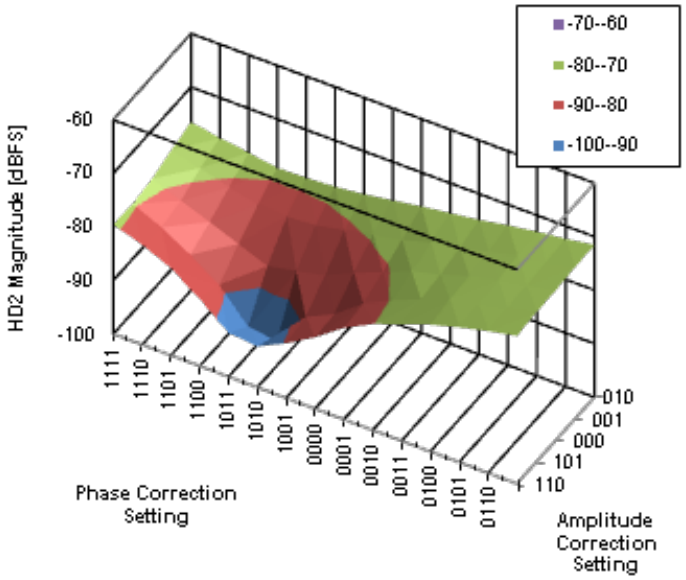


Figure 44. Gain and Phase Imbalance HD2 optimization at 250 MHz

Input Clock Divider

An input clock divider allows a high frequency clock signal to be distributed throughout the system and locally divided down at the ADC device so that coupling of signals at common intermediate frequencies into other parts of the system can be avoided. The frequency at the CLKIN input may be divided down to the sampling rate of the ADC by factors of 1, 2, 4, or 8. Changing the clock divider setting initiates a JESD204 link re-initialization and requires re-calibration of the ADC if the sampling rate is changed from the rate during the previous calibration.

Sampling Instant Phase Adjustment

Adjustment of the ADC sampling instant relative to the CLKIN input clock may be controlled using the coarse phase adjustment feature.

Coarse clock phase adjustment is provided to control the phase of the sampling instant in the ADC cores. The coarse phase steps are equal to 1/(2*CLKDIV*F_S) seconds over a 1/F_S second range where CLKDIV is the clock division factor and F_S is the sampling rate. The coarse phase adjustment setting is common to both channels.

Once the JESD204B serial link is established, the frame and LMFC clocks as well as the internal reference clocks used by the JESD204B serializer are not affected by the clock phase adjustments because the data is re-timed at the ADC core output. Changing the phase setting does not affect the status of the JESD204B link and does not cause glitches in the serial data. Varying the phase does not vary the timing of frames output on the JESD204B link but it does vary the sampling instant relative to the internal frame clock, therefore the total latency from the sampling instant to the beginning of the frame output on the serial link changes equal to the change in the phase adjustment. This latency change is a fraction of a frame clock cycle.

The phase of the internal sampling clock is aligned to SYSREF events. This impacts the phase relationship between the input signal and sampling instant and may affect the latency across the link.

Serial Differential Output Drivers

The differential drivers of the LM97937 that output the serial JESD204B data are voltage mode drivers with amplitude control and de-emphasis features that may be configured via the SPI interface for a variety of different channel applications. Eight amplitude control (VOD) and eight de-emphasis control (DEM) settings are available. Both VOD and DEM must be configured to optimize the noise performance of the serial interface for a particular lossy channel.

The output common-mode of the driver varies with the VOD configuration and temperature, therefore AC coupling is required between the LM97937 and the device receiving the serial data.

De-Emphasis Equalization

De-emphasis of the differential output is provided as a form of continuous-time linear equalization that imposes a high-pass frequency response onto the output signal to compensate for frequency dependent attenuation as the signal propagates through the channel to the receiver. In the time-domain, the de-emphasis appears as the bit transition transient followed by an immediate reduction in the differential amplitude as shown in Figure 45. The characteristic appearance of the waveform changes with differential amplitude and the magnitude of de-emphasis applied. The serial lane rate determines the available period of time during which the de-emphasis transient settles but the lane rate does not affect the settling behavior of the applied de-emphasis.

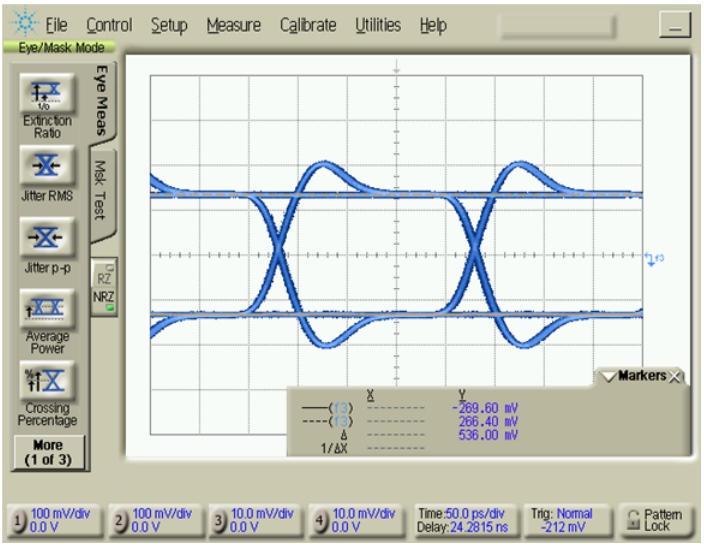


Figure 45. De-Emphasis of the Differential Output Signal

Table 2 indicates the typical measured values for the de-emphasis range, where the de-emphasis value is measured as the ratio (in units of [dB]) between the peak voltage after the signal transition to the settled voltage value in one bit period. The data rate for this measurement is 1.2Gb/s to allow settling of the de-emphasis transient. Table 2 illustrates the actual de-emphasis value in terms of voltage attenuation and shows dependence on the amplitude setting but does not reflect the optimal amplitude setting (VOD) and de-emphasis setting (DEM) for a particular lossy channel. Table 3 shows the amplitude of the differential signal swing during its settled state after the transition transient. The measurement is performed at 1.2Gb/s and the units are in differential peak-peak mV.

Table 2. De-emphasis Values [dB] for All VOD and DEM Configuration Settings

		DEM							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
VOD	**0**	0	–0.4	–1.2	–2.1	–2.8	–3.8	–4.8	–6.8
	1	0	–0.6	–1.7	–2.7	–3.5	–4.6	–5.7	–7.8
	2	0	–0.8	–2.2	–3.3	–4.1	–5.3	–6.4	–8.6
	3	0	–1.0	–2.6	–3.9	–4.7	–5.9	–7.0	–9.4
	4	0	–1.3	–3.0	–4.3	–5.3	–6.5	–7.7	–9.9
	5	0	–1.6	–3.5	–4.9	–5.8	–7.0	–8.3	–10.5
	6	0	–1.9	–3.9	–5.3	–6.2	–7.5	–8.7	–11.0
	7	0	–2.1	–4.2	–5.7	–6.7	–8.0	–9.3	–11.5

Table 3. Settled differential voltage swing values, V_{OD} [mVp-p] for All VOD and DEM Configuration Settings

		DEM							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
VOD	**0**	580	540	500	440	420	380	340	260
	1	680	620	560	500	440	400	340	280
	2	760	700	600	520	480	420	360	280
	3	860	760	640	560	500	440	380	300
	4	960	820	680	580	520	460	400	300
	5	1060	880	700	600	540	460	400	320
	6	1140	920	740	620	560	480	420	320
	7	1240	960	760	640	580	500	420	320

Power Down and Sleep Modes

Power Down and Sleep modes are provided to allow the user to reduce the power consumption of the device without disabling power supplies. Both modes reduce power consumption by the same amount but they differ in the amount of time required to return to normal operation. Upon changing from Power Down back to Normal operation, an ADC calibration routine is performed. Awaking from Sleep mode does not perform ADC calibration. Neither Power Down mode nor Sleep mode resets configuration registers.

The Power Down mode may be used at any time but it must be used as part of the secondary "ADC Core Calibration Procedure" as described in the next section. Exiting the power down mode without following the ADC Core Calibration Procedure results in sub-optimal performance.

ADC Core Calibration

The ADC core of this device requires calibration to be performed after power-up to achieve full performance. After power-up, the LM97937 detects that the supplies and clock are valid, waits for a power-up delay, and then performs a primary calibration of the ADC core. The power-up delay is 8.4e6 sampling clock cycles or 22.7ms at a 370MSPS sampling rate. The primary calibration requires approximately 1.0e6 sampling clock cycles.

A secondary calibration procedure must be followed after the automatic primary calibration step is complete. Figure 46 illustrates the required calibration procedure. During a system start-up, the power supplies are turned on and the device clock is applied to the CLKIN input, and then the SPI logic level must be appropriately configured, and then the system must wait for the device to finish the primary calibration cycle. Monitoring the CAL_DONE bit in the JESD_STATUS register (address 0x006C) indicates the completion of the primary calibration. Once the primary calibration is complete, the secondary ADC core calibration procedure must be performed in the following steps. Some of the steps refer to the "desired" input clock divider factor, CLKDIV. This refers to the clock divide factor value (and not the CLKDIV register field value) that achieves the desired sampling rate during normal operation.

- Set the device into power-down mode by properly programming register address 0x0002.
- Set CLKDIV. If the desired CLKDIV factor is 1, 2, or 4, then the CLKDIV value must be set to twice the desired value for this step in the procedure. For example, if the desired CLKDIV factor is 4 then CLKDIV must be set to 8 at this time. If the desired CLKDIV factor is 8, then CLKDIV must remain at 8 for this step in the procedure.
- Set the values of the registers 0x0016, 0x001E and 0x0028 as indicated in Figure 46. These register writes are required but details of the register functions are not provided. Changing these registers to any other values will result in undesired results.
- Set the device back into Normal Operation by properly configuring register address 0x0002.
- Monitor the JESD_STATUS register until the CAL_DONE bit is asserted to 1. Optionally, the system may wait 10^6 sampling clock cycles before advancing to the next step instead of repetitively querying the JESD_STATUS register. Note that the wait time in seconds depends on the current setting of CLKDIV at this step in the procedure.
- Change the CLKDIV factor back to the desired value by properly programming register address 0x0013. If the desired CLKDIV factor is 8, then nothing is required in this step. After completing of this step, the calibration procedure is complete and the device will automatically advance into JESD204B link initialization.

If an ADC core re-calibration is desired or if the system must place the device in Power Down Mode, then the ADC Core Calibration Procedure must be followed as shown in the Figure 46 to ensure that the device calibrates properly after Power Down Mode exit. Exiting Power Down mode without following the calibration procedure results in sub-optimal performance. When the device exits power-down mode, it waits for a power-down exit delay, then the ADC core is re-calibrated. The power-down exit delay is 262e3 sampling clock cycles and the calibration requires 10^6 sampling clock cycles.

Re-calibration is not required across the supported operating temperature range to maintain functional performance but it is recommended for large changes in ambient temperature to maintain optimal dynamic performance.

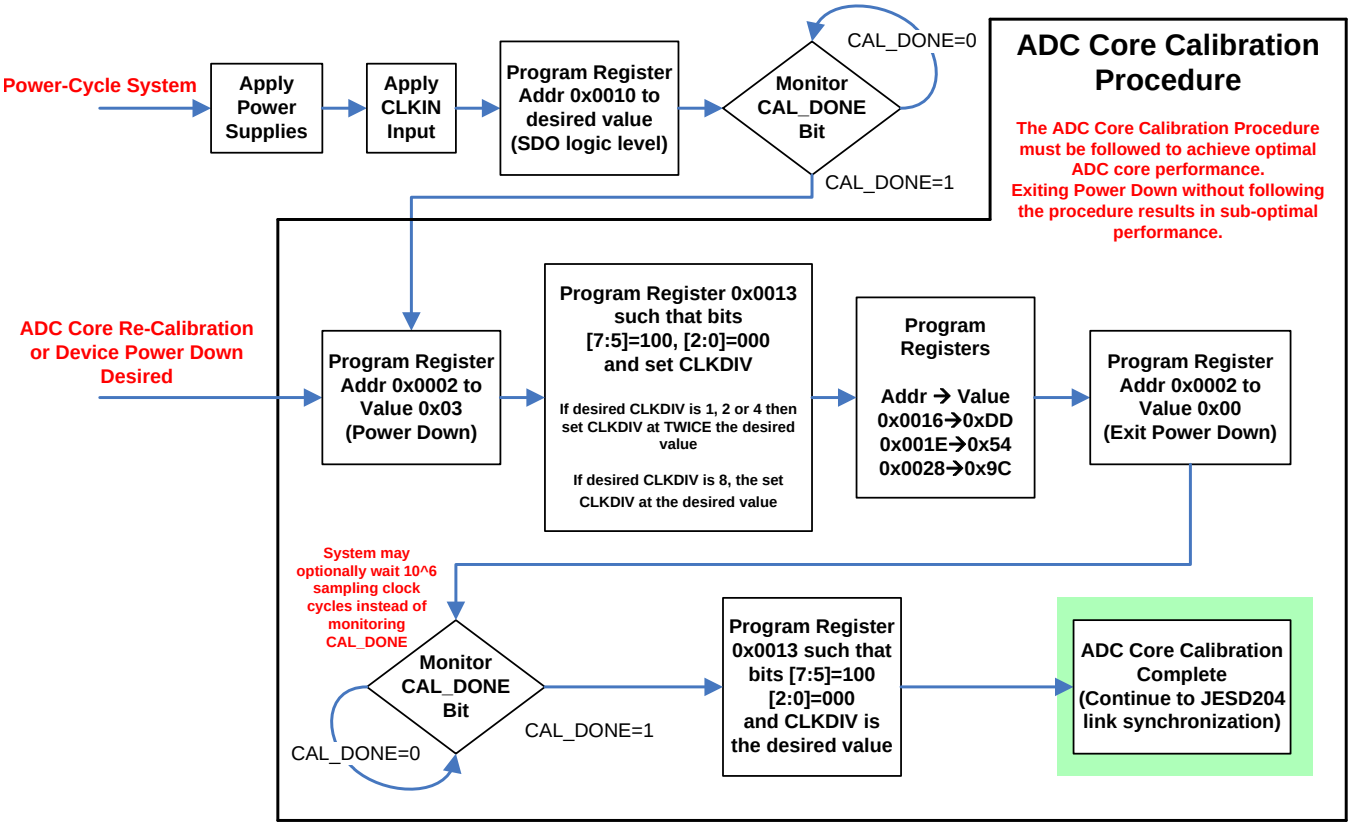


Figure 46. Device Start-Up Flow Chart

Data Format

Data may be output in the serial stream as 2's complement format by default or optionally as offset binary. This formatting is configured via the SPI interface and is performed in the data path prior to JESD204B data framing and 8b/10b encoding.

JESD204B Supported Features

The LM97937 supports a feature set of the JESD204B standard targeted to its intended applications but does not implement all the flexibility of the standard. Table 4 summarizes the level of feature support.

Table 4. LM97937 Feature Support for the JESD204B Serial Interface

Feature	Supported	NOT Supported
Subclass	• Subclass 1, 0 (1)	• Subclass 2
Device Clock (CLKIN) and SYSREF	• AC coupled CLKIN and SYSREF • DC coupled CLKIN and SYSREF (special cases) • Periodic, Pulsed Periodic and One-Shot SYSREF	
Latency	• Deterministic latency supported for subclass 1 implementations using standard SYSREF signal	• Deterministic latency NOT supported for non-standard implementations
Electrical layer features	• LV-OIF-11G-SR interface and performance • AC coupled serial lanes	• TX lane polarity inversion • DC coupled serial lanes

(1) The LM97937 supports most subclass 0 requirements but is not strictly subclass 0 compliant

Table 4. LM97937 Feature Support for the JESD204B Serial Interface (continued)

Feature	Supported	NOT Supported
Transport layer features and configuration	• L=1 or 2 for each channel • K configuration • Scrambling	• F, S and HD configuration depends on L and is not independently configurable • M, N, N', CS, CF configuration • Idle link mode • Short and Long transport layer test patterns
Data link layer features	• 8b/10b encoding • Lane synchronization • D21.5, K28.5, ILA, PRBS7, PRBS23, Ramp test sequences	• RPAT/JSPAT test sequences

Transport Layer Configuration

The transport layer features supported by the LM97937 are a subset of possible features described in the JESD204B standard. The configuration options are intentionally simplified to provide the lowest power and most easy-to-use solution.

Lane Configuration

Each channel outputs its digital data on up to two (2) serial lanes that support JESD204B. The number of transmission lanes per channel (L) is configurable as 1 or 2. Transmitting both channels on the same lane(s) is not supported. When using one (1) serial lane per channel, the serial data lane transmits at twenty (20) times the sampling rate. A 370MSPS sampling rate corresponds to a 7.4Gb/s/lane rate. When using two (2) serial lanes per channel, the serial data rate is ten (10) time the sampling rate. A 370MSPS sampling rate corresponds to a 3.7Gb/s/lane rate.

Frame Format

The format of the data arranged in a frame depends on the L setting and the device mode (SNRBoost or Bit-Burst). The octets per frame (F), samples per frame (S) and high density mode (HD) parameters are not independently configurable. The N, N', CS, CF, M and HD parameters are fixed and not configurable. Figure 47 and Figure 48 below show the data format for L=1 and L=2 when the device is in SNRBoost or Bit-Burst modes. M=1 in this device, indicating one converter per device and each channel is considered as a different device. Therefore, the L value corresponds to the number of lanes used by a channel, not the number of lanes output from the chip.

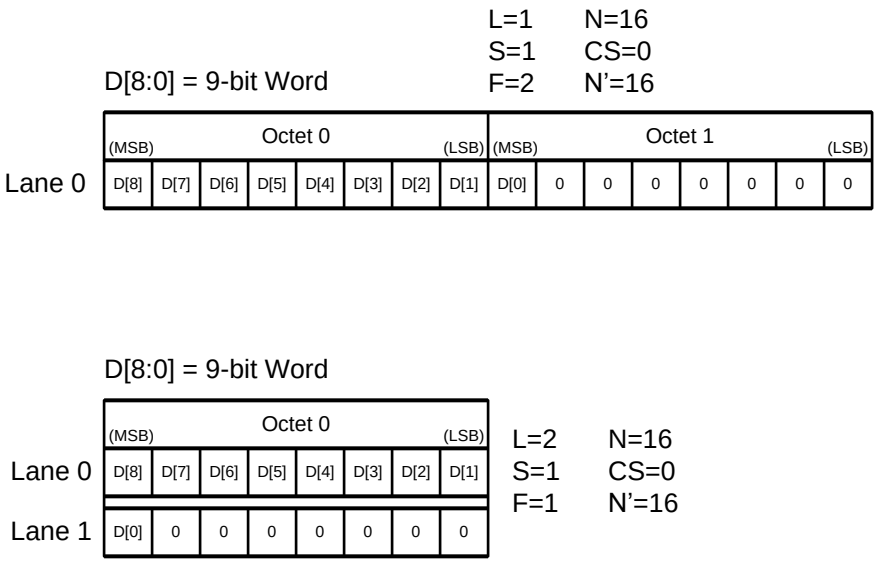


Figure 47. SNRBoost Mode Transport Layer Definitions for the Supported Lane Configurations

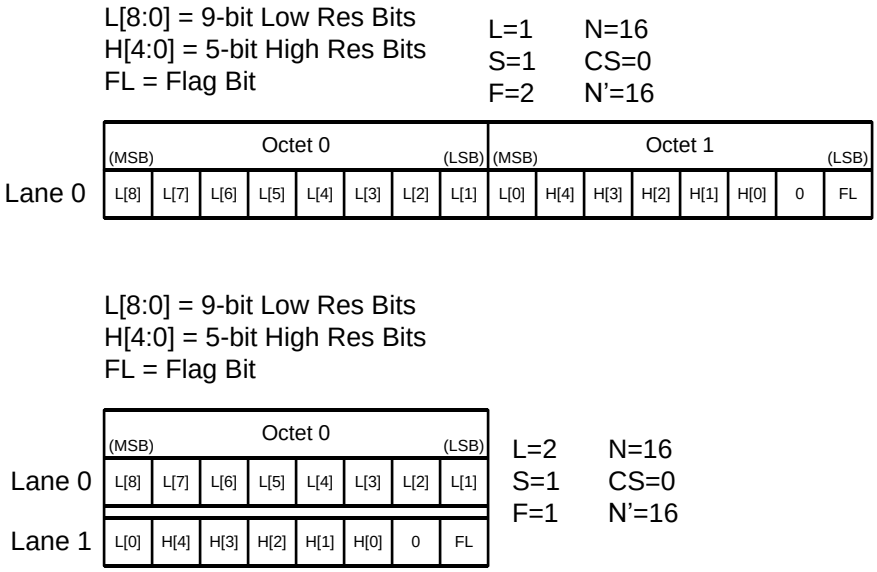


Figure 48. Bit-Burst Mode Transport Layer Definitions for the Supported Lane Configurations

ILA Information

Table 5 summarizes the information transmitted during the initial lane alignment (ILA) sequence. Mapping of these parameters into the data stream is described in the JESD204B standard.

Table 5. Parameters Transmitted in the Initial Lane Alignment (ILA) Sequence

Parameter	Description	Value	
		Single Lane Mode	Dual Lane Mode
ADJCNT	DAC LMFC adjustment	0	0
ADJDIR	DAC LMFC adjustment direction	0	0
BID	Bank ID	0	0
CF	Number of control words per frame clock period per link	0	0
CS	Number of control bits per sample	0	0

Table 5. Parameters Transmitted in the Initial Lane Alignment (ILA) Sequence (continued)

Parameter	Description	Value	
		Single Lane Mode	Dual Lane Mode
DID	Device identification number	0	0
F	Number of octets per frame (per lane)(1)	2	1
HD	High Density Format	0	1
JESDV	JESD204 Version	1	1
K	Number of frames per multi-frame(1)	Set by register as 9 to 32	Set by register as 17 to 32
L	Number of lanes per link(1)	1	2
LID	Lane identification number	0	0 (lane 0), 1 (lane 1)
M	Number of converters per device(1)	1	1
N	Converter Resolution (1)	16	16
N'	Total number of bits per sample(1)	16	16
PHADJ	Phase adjustment request to DAC	0	0
S	Number of samples per converter per frame cycle(1)	1	1
SCR	Scrambling enabled	Set by register as 0 (disabled) or 1	Set by register as 0 (disabled) or 1
SUBCLASSV	Device Subclass Version	1	1
RES1	Reserved field 1	0	0
RES2	Reserved field 2	0	0
FCHK	Checksum	Computed	Computed

(1) These parameters have a "binary value minus 1" encoding applied before being mapped into the link configuration octets. For example, F=2 is encoded as 1, and F=1 is encoded as 0.

Scrambling of the output serial data is supported and conforms to the JESD204B standard. Scrambling is disabled by default but may be enabled via the SPI interface. When scrambling is enabled, the LM97937 supports the early synchronization option by the receiver during the ILA sequence, although the ILA sequence data is never scrambled.

Test Pattern Sequences

The following test pattern sequences are supported and may be enabled via the SPI interface. Short and Long transport layer sequences and RPAT/JSPAT sequences are not supported.

Table 6. Supported Test Pattern Sequences

Test Pattern	Description	Common Purpose
D21.5	Alternating 1 and 0 pattern (101010...)	Jitter or system debug
K28.5	Continuous K28.5 symbols	System debug
Repeated ILA	ILA repeats indefinitely	System debug
Ramp	After ILA, an ascending sample ramp is transmitted with programmable step	System debug and transport layer verification
PRBS	PRBS 7/15/23 Complies with ITU-T O.150 specification and is compatible with J-BERT equipment.	Jitter and bit error rate testing

JESD204B Link Initialization

A JESD204B link is established via link initialization which involves the following steps: Frame alignment, Code Group Synchronization, and Initial Lane Synchronization. These steps are shown in Figure 49. Link initialization must occur between the transmitting device (LM97937) and receiving device before sampled data may be transmitted over the link. The link initialization steps described here are specifically for the LM97937, supporting JESD204B subclass 1.

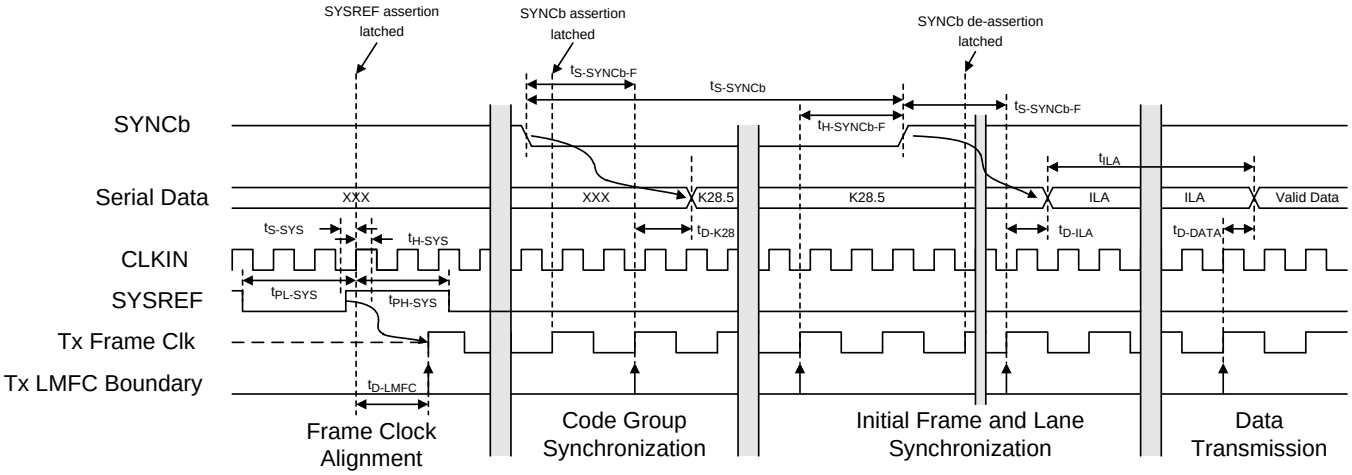


Figure 49. Link Initialization Timing and Flow Diagram

The **Frame Alignment** step requires alignment of the frame and local multi-frame clocks within the LM97937 to an external reference. This is accomplished by providing the device clock and SYSREF clock to the CLKIN and SYSREF inputs, respectively. The LM97937 aligns its frame clock and LMFC to any SYSREF rising edge event, offset by a SYSREF-to-LMFC propagation delay.

The SYSREF signal must be source synchronous to the device clock, therefore the SYSREF rising edge must meet setup and hold requirements relative to the signal at the CLKIN input. If this requirement cannot be met, then the alignment of the internal frame and multi-frame clocks cannot be guaranteed. As a result, a link may still be established, but the latency through the link cannot be deterministic. Frame alignment may occur at any time, although a re-alignment of the internal frame clock and LMFC will break the link. Note that frame alignment is not required for the LM97937 to establish a link because the device automatically generates the clocks on power up with unknown phase alignment.

Code Group Synchronization is initiated when the receiver sends a synchronization request by asserting the SYNCb input of the LM97937 to a logic low state (SYNCb+ < SYNCb–). After the SYNCb assertion is detected, the LM97937 outputs K28.5 symbols on all serial lanes that are used by the receiver to synchronize and time align its clock and data recovery (CDR) block to the known symbols. The SYNCb signal must be asserted for at least 4 frame clock cycles otherwise the event is ignored by the LM97937. Code group synchronization is completed when the receiver de-asserts the SYNCb signal to a logic high state.

After the LM97937 detects a de-assertion of its SYNCb input, the **Initial Lane Synchronization** step begins on the following LMFC boundary. The LM97937 outputs 4 multi-frames of information that compose the Initial Lane Alignment (ILA) sequence. This sequence contains information about the data transmitted on the link. The initial lane synchronization step and link initialization conclude when the ILA is finished and immediately transitions into **Data Transmission**. During data transmission, valid sampled data is transmitted across the link until the link is broken.

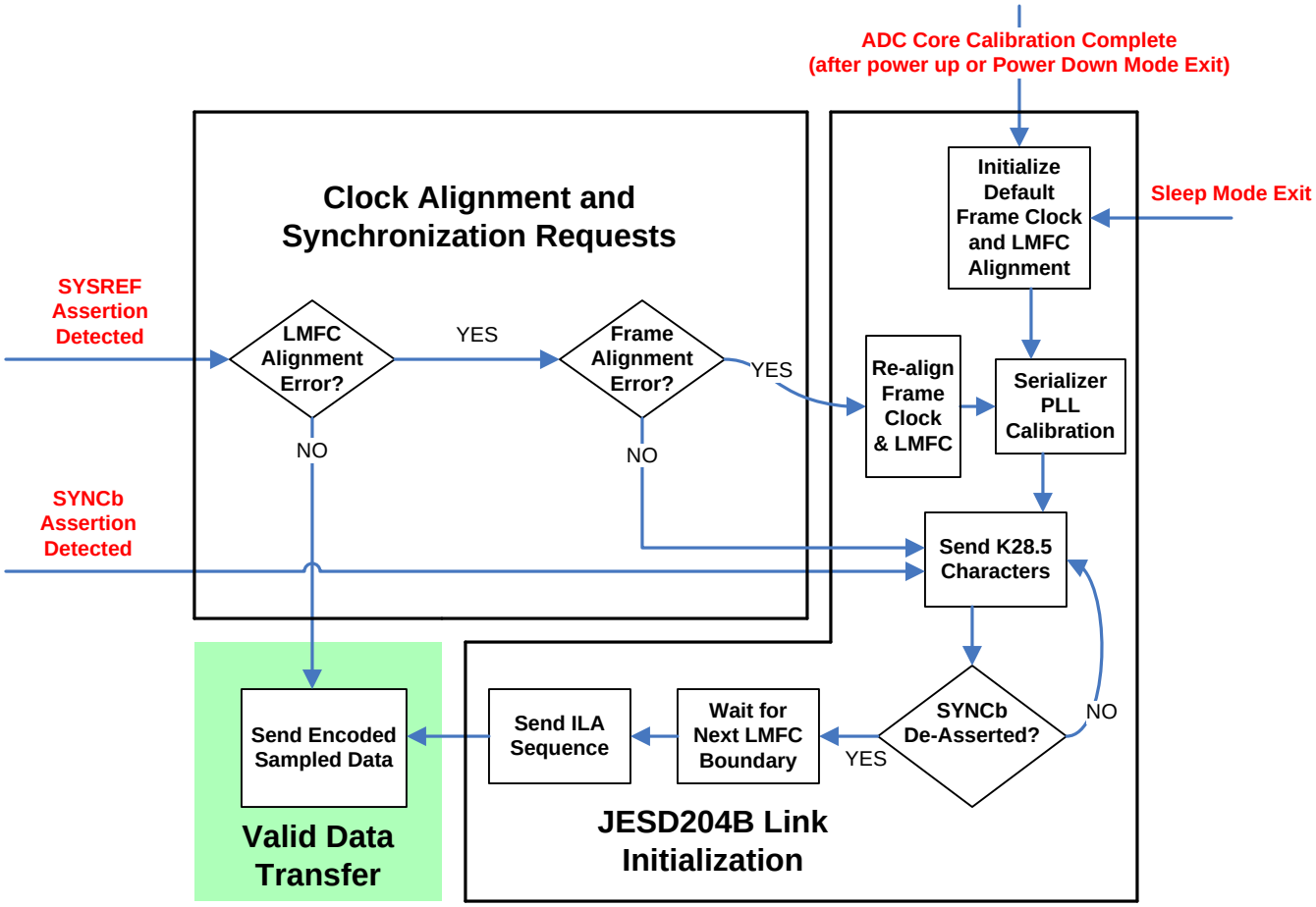


Figure 50. Device Start-Up and JESD204B Link Synchronization Flow Chart

The flowchart in Figure 50 describes how the LM97937 initializes the JESD204B link and reacts to changes in the link. Once the ADC core calibration is finished, the LM97937 begins with PLL calibration and link initialization using a default frame clock and LMFC alignment by sending K28.5 characters. PLL calibration requires approximately 153e3 sampling clock cycles. If SYNCb is not asserted, then the device immediately advances to the ILA sequence at the next LMFC boundary. On the other hand, if SYNCb is asserted, then the device continues to output K28.5 characters until SYNCb is de-asserted.

When a SYSREF rising edge event is detected, then the LM97937 compares the SYSREF event to the current alignment of the LMFC. If the SYSREF event is aligned to the current LMFC alignment, then no action is taken and the device continues to output data. If misalignment is detected, then the SYSREF event is compared to the frame clock. If misalignment of the frame clock is also detected, then the clocks are re-aligned and the link is re-initialized. If the frame clock is not misaligned, then the frame clock alignment is not updated. In the cases that a SYSREF event causes a link re-initialization, the LM97937 will begin sending K28.5 characters without a SYNCb assertion and will immediately transition to the ILA sequence on the next LMFC boundary unless the SYNCb signal is asserted. Any time the frame clock and LMFC are re-aligned, the serializer PLL must calibrate before Code Group Synchronization begins. SYSREF events must not occur during LM97937 power-up, ADC calibration, or PLL calibration. The JESD_STATUS register is available to check the status of the LM97937 and the JESD204B link.

If a SYNCb assertion is detected for at least 4 frame clock cycles, the LM97937 immediately breaks the link and sends K28.5 characters until the SYNCb signal is de-asserted.

When exiting sleep mode, the frame clock and LMFC are started with a default (unknown) phase alignment, PLL calibration is performed, and the device immediately transitions into sending K28.5 characters.

SPI Interface

The SPI interface allows access to the internal configuration registers of the ADC via read and write commands to a specific address. The four-wire interface (SCLK, SDI, SDO, CSb) is compatible with 1.2V, 1.8V, 2.5V, or 3.3V logic. The input pins (SCLK, SDI, CSb) utilize thick-oxide devices to tolerate 3.3V logic although the input threshold levels are relative to 1.2V logic. The SDO output is high impedance at all times other than during the final portion of a read command. During the time that the SDO output is active, the logic level is determined by a configuration register. The SPI output logic level must be properly configured after power up and before making a read command to prevent damaging the receiving device or any other device connected to the SPI bus. Until the SPI_CFG register is properly configured, voltages on the SDO output may be as high as 3.3V during a read command. A low capacitance protection diode may be added with the anode connected to the SDO output and the cathode connected to the desired voltage supply to prevent an accidental pre-configured read command from causing damage. Figure 51 demonstrates a typical circuit to interface the LM97937 to a SPI master using a shared SPI bus.

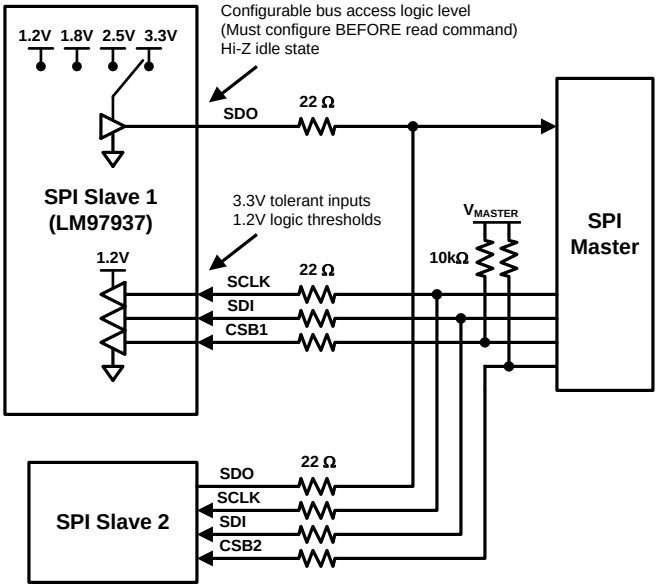


Figure 51. Typical SPI Interface Application

The SPI interface protocol has a 1-bit command, 15-bit address word and 8-bit data word as shown in Figure 52. A read or write command is 24 bits in total, starting with the read/write command bit where 0 indicates a write command and 1 indicates a read command. The read/write command bit is clocked into the device on the first rising edge of SCLK after CSb is asserted to 0. During a write command, the 15-bit address and 8-bit data values follow the read/write bit MSB-first and are latched on the rising edge of SCLK. During a read command, the SDO output is enabled shortly after the 16th rising edge of SCLK and outputs the read value MSB first before the SDO output is returned to a high impedance state. The read or write command is completed on the SCLK rising edge on which the data word's LSB is latched. CSb may be de-asserted to 1 after the LSB is latched into the device.

The SPI interface allows command streaming where multiple commands are made without de-asserting CSb in-between commands. The commands in the stream must be of similar types, either read or write. Each subsequent command applies to the register address adjacent to the register accessed in the previous command. The address order can be configured as either ascending or descending. Command streaming is accomplished by immediately following a completed command with another set of eight (8) rising edges of SCLK without de-asserting CSb. During a write command, an 8 bit data word is input on the SDI input for each subsequent set of SCLK edges. During a read command, data is output from SDO for each subsequent set of SCLK edges. Each subsequent command is considered finished after the 8th rising edge of SCLK. De-asserting CSb aborts an incomplete command.

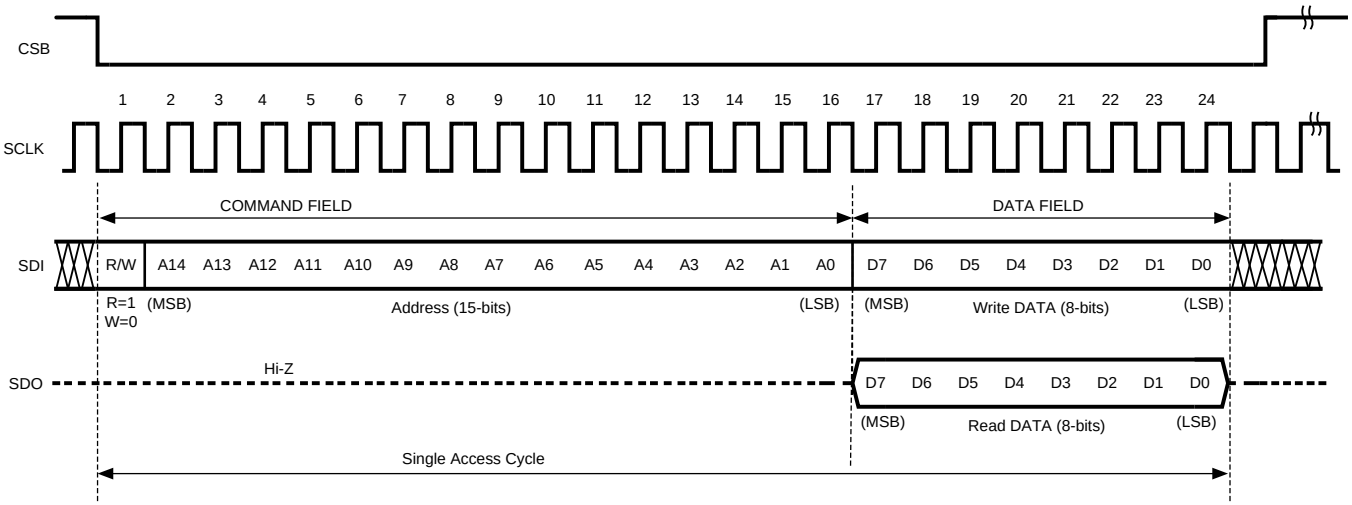


Figure 52. Serial Interface Protocol

APPLICATIONS

Example Circuit Implementation

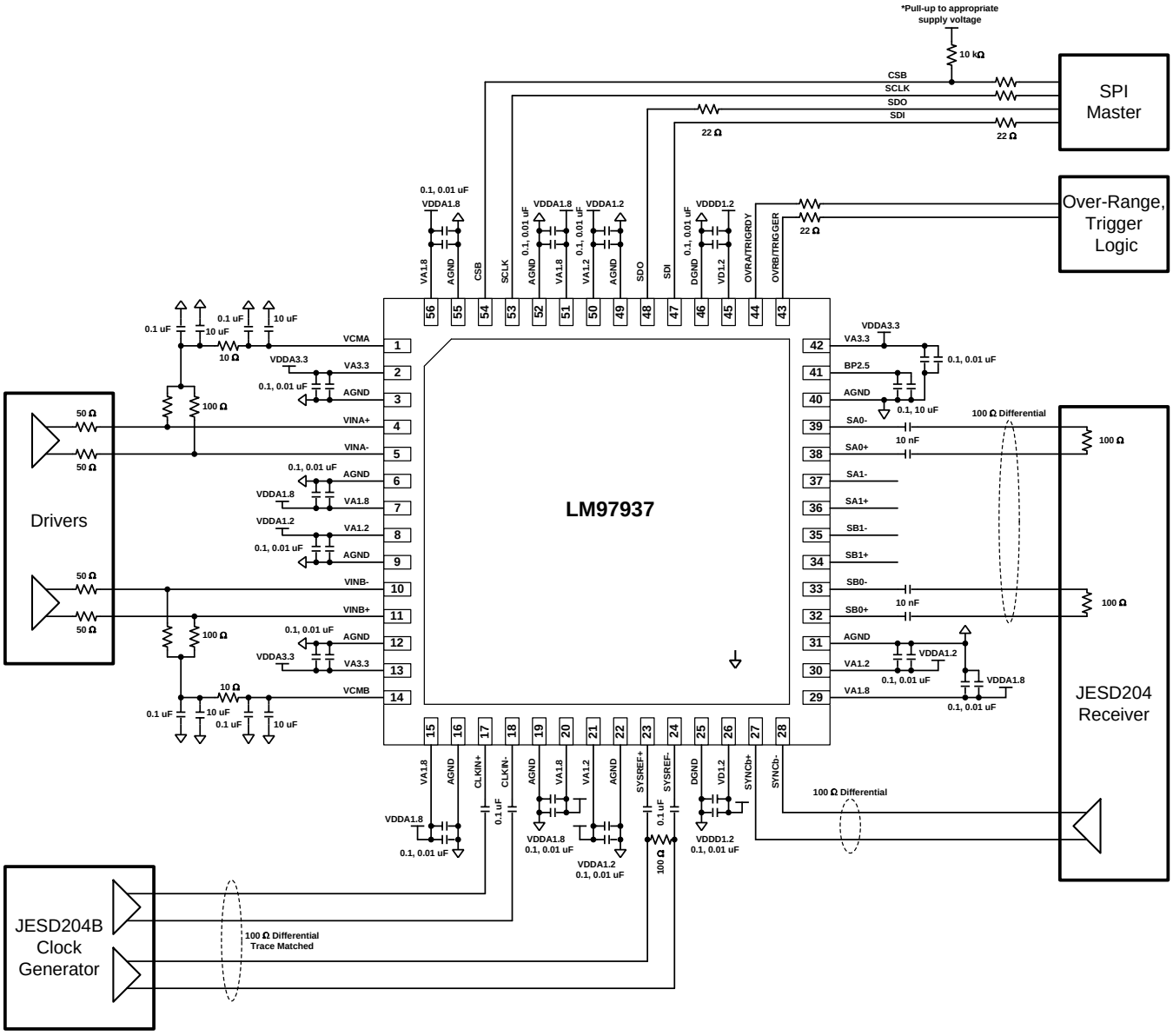


Figure 53. Example Circuit Implementation

Analog Input Considerations

Differential Analog Inputs and Full Scale Range

The LM97937 has two channels, each with a pair of analog signal input pins: VINA+, VINA− for channel A and VINB+, VINB− for channel B. VIN, the input differential signal for a channel, is defined as VIN = (VIN+) – (VIN−). Table 7 shows the expected input signal range when the differential signal swings about the input common mode, VCM. The full-scale differential peak-to-peak input range is equal to twice the internal reference voltage, VREF. Nominally, the full scale range is 1.7Vpp-diff, therefore the maximum peak-to-peak single-ended voltage is 0.85 Vpp at each of the VIN+ and VIN− pins.

The single-ended signals must be opposite in polarity relative to the VCM voltage to provide a purely differential signal, otherwise the common-mode component may be rejected by the ADC input. Table 7 indicates the input to output relationship of the LM97937 where V_{REF} = 0.85 V. Differential signals with amplitude or phase imbalances result in lower system performance compared to perfectly balanced signals. Imbalances in signal path circuits lead to differential-to-common-mode signal conversion and differential signal amplitude loss as shown in Figure 54. This deviation or imbalance directly causes a reduction in the signal amplitude and may also lead to distortion, particularly even order harmonic distortion, as the signal propagates through the signal path. The differential imbalance correction feature of the LM97937 helps to correct amplitude or phase errors in the signal.

Table 7. Mapping of the analog input full scale range to digital codes for Bit-Burst data in 14-bit high resolution

VIN+	VIN-	2's Complement Output	Binary Output	Note
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	10 0000 0000 0000	00 0000 0000 0000	Negative Full-Scale
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	11 0000 0000 0000	01 0000 0000 0000	
V_{CM}	V_{CM}	00 0000 0000 0000	10 0000 0000 0000	Mid-Scale
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	01 0000 0000 0000	11 0000 0000 0000	
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	01 1111 1111 1111	11 1111 1111 1111	Positive Full-Scale

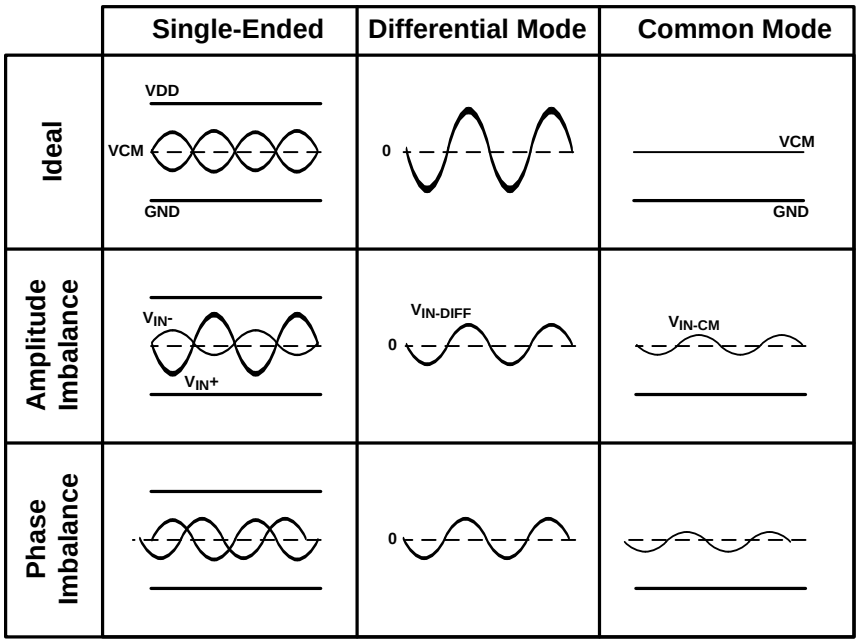


Figure 54. Differential Signal Waveform and Signal Imbalance

Analog Input Network Model

Matching the impedance of the driving circuit to the input impedance of the ADC can be important for low distortion performance and a flat gain response through the network across frequency. In very broadband applications or lowpass applications, the ADC driving network must have very low impedance with a small termination resistor at the ADC input to maximize the bandwidth and minimize the bandwidth limitation posed by the capacitive load of the ADC input. In bandpass applications, a designer may either design the anti-aliasing filter to match to the complex impedance of the ADC input at the desired intermediate frequency, or consider the resistive part of the ADC input to be part of the resistive termination of the filter and the capacitive part of the ADC input to be part of the filter itself. The capacitive load of the ADC input can be easily absorbed into most LC bandpass filter designs with a final shunt LC tank stage.

The analog input circuit of the LM97937 is a buffered input with an internal differential termination. Compared to an ADC with a switched-capacitor input sampling network that has an input impedance that varies with time, the LM97937 provides a constant input impedance that simplifies the interface design joining the ADC and ADC driver. A simplified passive model of the ADC input network is shown in Figure 55 that includes the termination resistance, input capacitance, parasitic bond-wire inductance, and routing parastics.

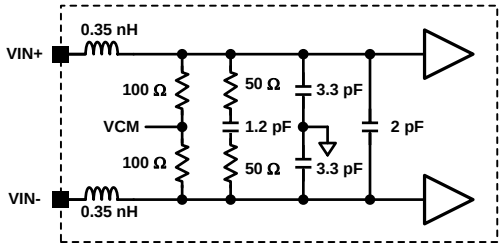


Figure 55. Simplified Analog Input Network Circuit Model

A more accurate load model is described by the measured differential SDD11 (100Ω) parameter model. A plot of the differential impedance derived from the model is shown on the Smith Chart of Figure 56. The model includes the internal resistive termination, the capacitive loading of the input buffer, and stray parasitic impedances like bond wire inductance and signal routing coupling. The SDD11 model may be used to back-calculate the impedance of the ADC input at a frequency of interest.

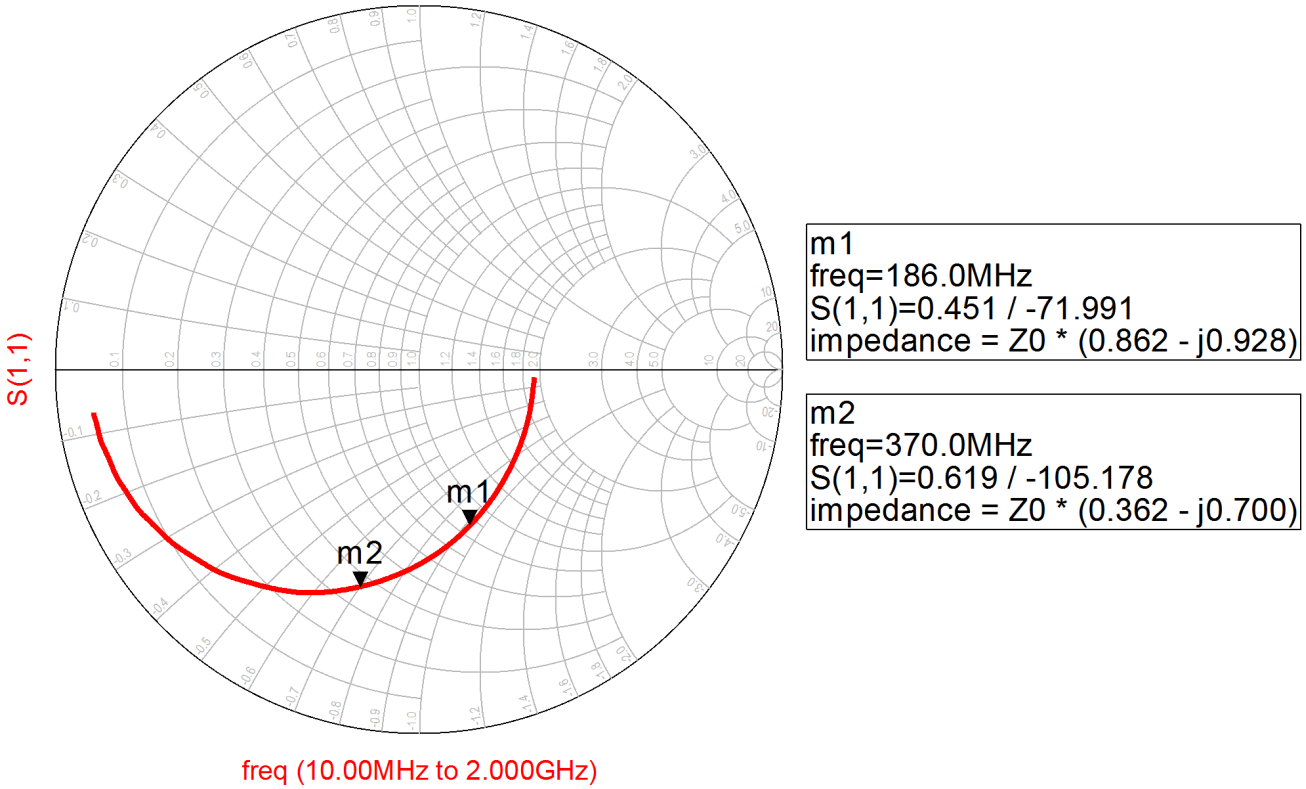


Figure 56. Measured SDD11 Data Showing the Differential Impedance of the Analog Input Network on a Smith Chart (100Ω)

Input Bandwidth

The input bandwidth of the LM97937 is defined here as the frequency at which the fundamental amplitude of the sampled data deviates by 3 dB, compared to the amplitude at low frequencies, for a low impedance input sinusoidal signal with constant voltage amplitude at the VIN+/- input pins. The voltage frequency response is shown in Figure 57.

The peaking in the frequency response is caused by the resonance between the package bond wires and input capacitance as well as a parasitic 0.5nH series trace inductance leading to the device pins. This peaking is typically made insignificant by the stop-band of an anti-aliasing filter that precedes the ADC input. For broadband applications, 10Ω resistors may be put in series with the VIN+ and VIN- input pins. This extra resistance flattens out the frequency response at the cost of adding some attenuation in the signal path. The additional series resistance also accordingly modifies the measured SDD11 looking into the analog input.

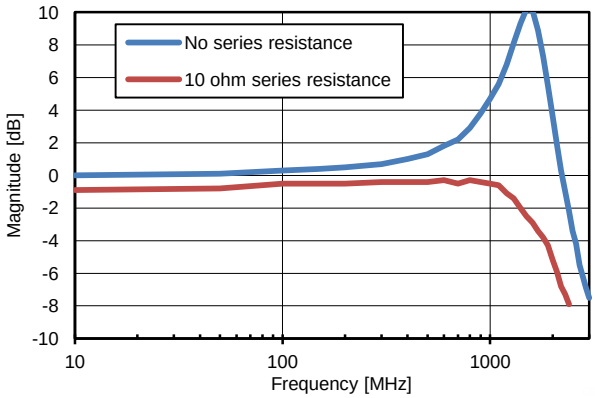


Figure 57. Measured Input Voltage Frequency Response

Driving the Analog Input

The LM97937 analog input may be driven by a number of methods depending on the end application. The most important design aspects to consider when designing the ADC voltage driver network are signal coupling, impedance matching, differential signal balance, anti-alias filtering, and signal level.

An analog signal is AC or DC coupled to the ADC depending on whether signal frequencies near DC must be sampled. DC coupling requires tight control of the output common-mode of the ADC driver to match the input common-mode of the ADC input. In the case of DC coupling, the biases at pins VCMA and VCMB may be used as references to establish the driver output common-mode but the load cannot source/sink more current than what is specified in the electrical parameters. AC coupling does not require strict common-mode control of the driver and is typically achieved using AC coupling capacitors or a flux-coupled transformer. AC coupling capacitors should be chosen to have 0.1Ω impedance or less over the frequency band of interest. LC filter designs may be customized to achieve either AC or DC coupling.

The internal input network of the LM97937 has the common-mode voltage bias provided via internal shunt termination resistors as shown in Figure 55. Providing the common-mode reference externally from the VCMA and VCMB pins, through external termination resistors, is also recommended. VCMA is used exclusively for channel A and is independent from VCMB.

Impedance matching in high speed signal paths using an ADC is dictated by the characteristic impedance of interconnects and by the design of anti-aliasing filters. Matching the source to the load termination is critical to ensure maximum power transfer to the load and to maintain gain flatness across the desired frequency band. In applications with signal transmission lengths greater than 10% of the smallest signal wavelength (0.1λ), matching is also desirable to avoid signal reflections and other transmission line effects. Applications that require high order anti-aliasing filters designs, including LC bandpass filters, require an expected source and load termination to guarantee the passband bandwidth and ripple of the filter design. The recommended range of the ADC driver source termination and ADC load termination is from 50Ω to 200Ω differential. The LM97937 has an internal

differential load termination but additional termination resistance may be added at the ADC input pins to adjust the total termination. The load termination at the ADC input presents a system-level design tradeoff. Better 2nd order distortion performance (HD2, IMD2) is achieved by the ADC using a lower load termination resistance but the ADC driver must have a higher drive strength and linearity to drive the lower impedance. Choosing a 100Ω total load termination is a reasonable balance between these opposing requirements.

Differential signal balance is important to achieve high distortion performance, particularly even order distortion (HD2, HD4). Circuits such as transformers and filters in the signal path between the signal source and ADC can disrupt the amplitude and phase balance of the differential signal before reaching the ADC input due to component tolerances or parasitic mismatches between the two parallel paths of the differential signal. The amplitude mismatch in the differential path should be less than ±0.4 dB and the phase mismatch should be less than ±2° to achieve a high level of HD2 performance. In the case that this imbalance is exceeded, the input balance correction may be used to re-balance the signal and improve the performance. Driving the LM97937 with a single-ended signal is not supported due to the tight restriction on the ADC input common-mode to maintain good distortion performance.

Converting a single-ended signal to a differential signal may be performed by an ADC driver or transformer. The advantages of the ADC driver over a transformer include configurable gain, isolation from previous stages of analog signal processing, and superior differential signal balancing. The advantages of using a transformer include no additional power consumption and little additional noise or distortion.

Figure 58 is an example of driving the ADC input with a cascaded transformer configuration. The cascaded transformer configuration provides a high degree of differential signal balancing, the series 0.1uF capacitors provide AC coupling, and the additional 33Ω termination resistors provide a total differential load termination of 50Ω. When additional termination resistors are added to change the ADC load termination, shunt terminations to the VCM reference are recommended to reduce common-mode fluctuations or sources of common-mode interference. A differential termination may be used if these sources of common-mode interference are minimal. In either case, the additional termination components must be placed as close to the ADC pins as possible. The MABA007159 transmission-line transformer from this example is widely available and results in good differential balance, although improved balance may be achieved using the rarer MABACT0040 transformer. Shunt capacitors at the ADC input, used to suppress the charge kickback of an ADC with switched-capacitor inputs, are not required for this purpose because the buffered input of the LM97937 does not kick back a significant amount of charge.

The insertion loss between an ADC driver and the ADC input is important because the driver must overcome the insertion loss of the connecting network to drive the ADC to full-scale and achieve the best SNR. Minimizing the loss through the network reduces the output swing and distortion requirements of the driver and usually translates to a system-level power savings in the driver. This can be accomplished by selecting transformers or filter designs with low insertion loss. Some filter designs may employ reduced source terminations or impedance conversions to minimize loss. Many designs require the use of high-Q inductors and capacitors to achieve an expected passband flatness and profile.

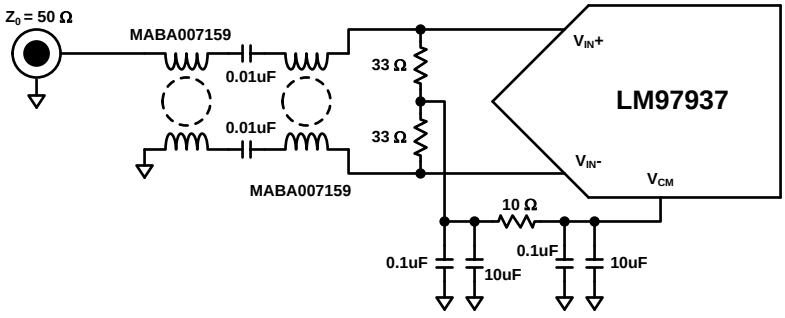


Figure 58. Transformer Input Network

Sampling theory states that if a signal with frequency f_{IN} is sampled at a rate less than $2*f_{IN}$ then it experiences aliasing, causing the signal to fall at a new frequency between 0 and $F_S/2$ and become indistinguishable from other signals at that new frequency.

To prevent out-of-band interference from aliasing onto a desired signal at a particular frequency, an anti-aliasing filter is required at the ADC input to attenuate the interference to a level below the level of the desired signal. This is accomplished by a lowpass filter in systems with desired signals from DC to $F_S/2$ or with a bandpass filter in systems with desired signals greater than $F_S/2$ (under-sampled signals). If an appropriate anti-aliasing filter is not included in the system design, the system may suffer from reduced dynamic range due to additional noise and distortion that aliases into the frequency bandwidth of interest.

An anti-aliasing filter is required in front of the ADC input in most applications to attenuate noise and distortion at frequencies that alias into any important frequency band of interest during the sampling process. An anti-aliasing filter is typically a LC lowpass or bandpass filter with low insertion loss. The bandwidth of the filter is typically designed to be less than $F_S/2$ to allow room for the filter transition band. Figure 59 is an example architecture of a ten (10) pole order LC bandpass anti-aliasing filter with added transmission zeros that can achieve a tight filtering profile for second Nyquist zone under-sampling applications.

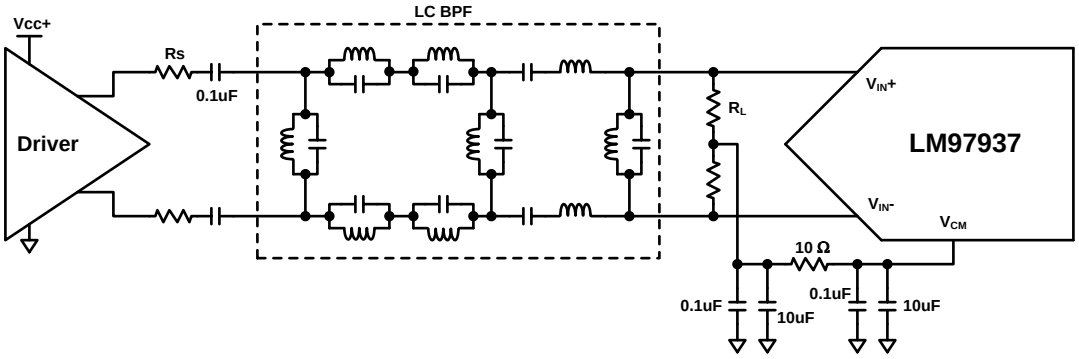


Figure 59. Bandpass Filter Anti-Aliasing Interface

DC Coupling to the analog input is also possible but the input common-mode must be tightly controlled for guaranteed performance. The driver device must have an output common-mode that matches the input common-mode of the LM97937 and the driver must track the VCM output from the LM97937 as shown in the example DC coupled interface of Figure 60 because the input common-mode varies with temperature. The common-mode path from the VCM output, through the driver device, back to the LM97937 input, and through a common-mode detector inside the LM97937 forms a closed tracking loop that will correct common-mode offset contributed by the driver device but the loop must be stable to ensure correct performance. The loop requires the large, 10uF, capacitor at the VCM output to establish the dominant pole for stability and the driver device must reliably track the VCM output voltage bias. The current drive strength and voltage swing of the VCM output bias limits the correctable amount of common-mode offset.

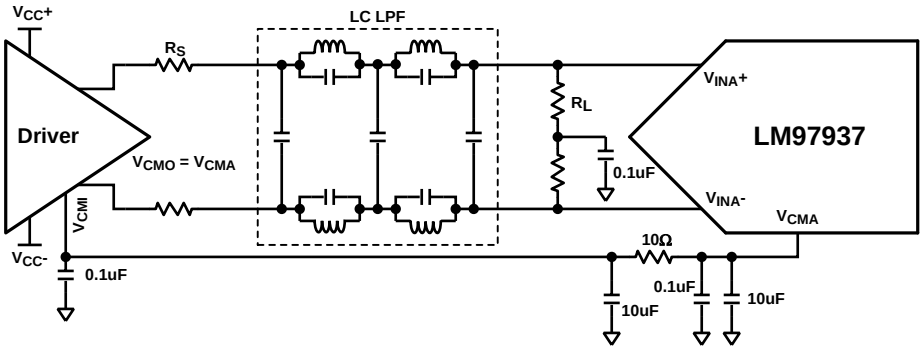


Figure 60. DC Coupled Interface

Clipping and Over-Range

The LM97937 has two regions of signal clipping: code clipping (over-range) and ESD clipping. When the input signal amplitude exceeds the full-scale reference range, code clipping occurs during which the digital output codes saturate. The effect of code clipping on the output digital code is different when the device is configured in Bit-Burst mode compared to SNRBoost mode. If the signal amplitude increases beyond the absolute maximum rating of the analog inputs, ESD clipping occurs due to the activation of ESD diodes.

If the LM97937 is configured for Bit-Burst mode and clipping occurs, the device outputs the maximum code for positive clipping and the minimum code for negative clipping. The maximum and minimum codes depend on the resolution state of the Bit-Burst block. While in the 14-bit high resolution phase, the maximum code is +8,191 (2's complement) and the minimum code is -8,192. When the input signal is reduced to below full scale, the non-clipped samples are available after a short latency time without a recovery transient. Early indication of clipping while in Bit-Burst mode is not provided.

If the LM97937 is configured for SNRBoost mode, the full-scale range without clipping is reduced to -0.8dBFS. When the power of the input signal increases beyond this value, the SNRBoost modulator becomes saturated and the noise level of the spectrum rises. The output data reaches extreme codes, but the clipped data is noisy as a result of passing through the modulator and does not show the flat characteristic at extreme codes similar to Bit-Burst mode. In SNRBoost mode, dedicated over-range indicators are available for each channel at output pins OVRA and OVRB. The thresholds of the indicators are programmable via the SPI interface. An over-range hold feature is also available to extend the time duration of the indicator longer than the over-range event itself to accommodate the case that a device monitoring the OVRA and OVRB outputs cannot process at the rate of the ADC sampling clock.

ESD clipping and activation of the ESD diodes at the analog input is not recommended and may damage or shorten the life of the device. This clipping may be avoided by selecting an ADC driver with an appropriate saturating output voltage, by placing insertion loss between the driver and ADC, by limiting the maximum amplitude earlier in the signal path at the system level, or by using a dedicated differential signal limiting device such as back-to-back diodes. Any signal swing limiting device must be chosen carefully to prevent added distortion to the signal.

CLKIN, SYSREF and SYNCb Input Considerations

Clocking the LM97937 shares many common concepts and system design requirements with previously released ADC products, but the JESD204B supported architecture adds another layer of complexity to clocking at the system level. A SYSREF signal accompanies the device clock to provide phase alignment information for the output data serializer (as well as for the sampling instant when the clock divider is enabled) to ensure that the latency through the JESD204B link is always known and does not vary, a concept called deterministic latency. To ensure deterministic latency, the SYSREF signal must meet setup and hold requirements relative to CLKIN and the design of the clocking interfaces require close attention. As with other ADCs, the quality of the clock signal also influences the noise and spurious performance of the device.

Driving the CLKIN Input

The CLKIN input circuit is composed of a differential receiver and an internal termination to a weakly driven common-mode bias. AC coupling to the CLKIN input with 0.1uF external capacitors is recommended to maintain the optimal common-mode biasing. Figure 61 shows the CLKIN receiver circuit and an example AC coupled interface.

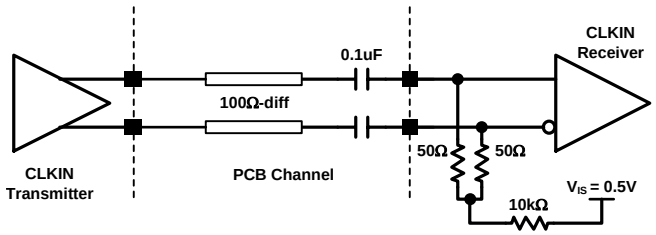


Figure 61. Driving the CLKIN Input with an AC Coupled Interface

DC coupling is allowed as long as the input common-mode range requirements are satisfied. The input common-mode of the CLKIN input is not compatible many common signaling standards like LVDS and LVPECL, therefore the CLKIN signal driver common-mode must be customized at the transmitter or adjusted along the interface. Figure 62 shows an example DC coupled interface that uses a resistor divider network to reduce the common-mode while maintaining a 100Ω total termination at the load. Design equations are provided with example values to determine the resistor values.

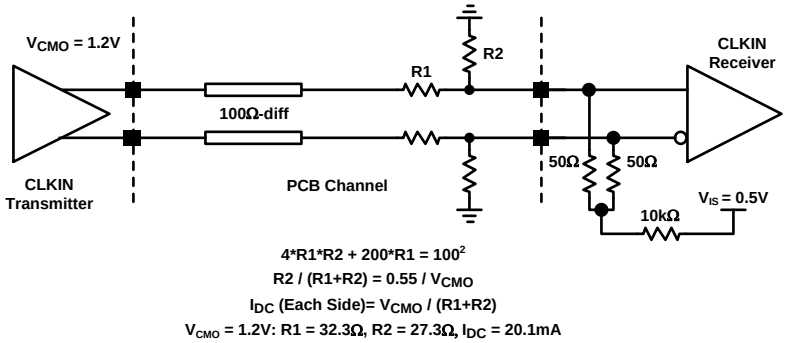


Figure 62. Driving the CLKIN Input with an Example DC Coupled Interface

The CLKIN input supports any type of standard signaling that meets the input signal swing and common-mode range requirements with an appropriate interface. Generic differential sinusoidal or square wave clock signals are both supported. Driving the CLKIN input single-ended is not recommended. The differential lane trace on the PCB should be designed to be a controlled 100Ω and protected from noise sources or other signals.

Clock Noise and Edge Rate

Noise added to the sampling clock path of the ADC degrades the SNR performance of the system. This noise may include broadband noise added by the ADC clock receiver inside the ADC device but may also include broadband and in-close phase noise added by the clock generator and any other devices leading to the CLKIN input. The theoretical SNR performance limit of the LM97937 as a result of clock noise for a given input frequency is shown in Figure 63 for a full scale input signal and different values of total jitter.

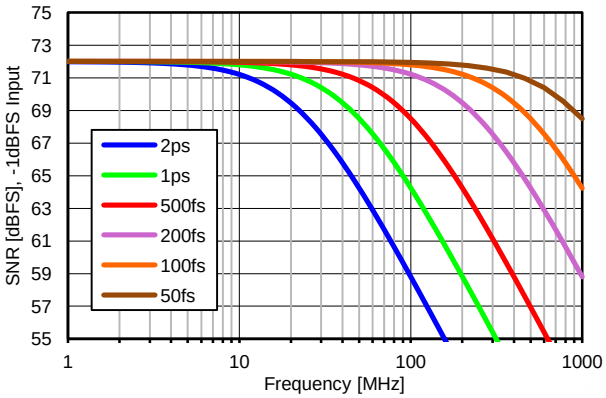


Figure 63. SNR Limit (in 100MHz Band) Due to Jitter of Sampling Clock with a Full Scale Input Signal

The differential clock receiver of the LM97937 has a very low noise floor and wide bandwidth. The wide band clock noise of the receiver, also referred to as the additive jitter, modulates the sampling instant and adds the noise to the signal. At the sampling instant, the added broadband noise appears in the first Nyquist zone at the ADC output to degrade the noise performance. Minimizing the additive jitter requires a sampling clock with a steep edge rate at the zero crossing. Reduced edge rate increases the additive jitter. For clock signals with a differential swing of 100mV or greater, the additive clock Figure 64 shows the SNR performance of the LM97937 for a range of clock transition slopes.

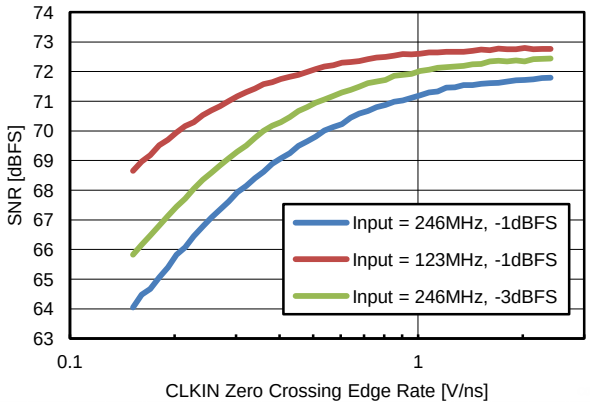


Figure 64. SNR vs. Input Clock Edge Rate

Noise added to the sampling clock by devices leading up to the ADC clock input also directly affects the noise performance of the system. In-close phase noise is typically dominated by the performance of the clock reference and phase-locked loop (PLL) that generates the clock and limits the sensitivity of the sampling system at desired frequencies offset 100Hz - 10MHz away from a large blocking signal. Little can be done to improve the in-close phase noise performance without the use of an additional PLL. Broadband noise added in the clock path limits the sensitivity of the whole spectrum and may be improved by using lower noise devices or by inserting a band-pass filter (BPF) with a narrow pass band and low insertion loss to the clock input signal path. Adding a BPF limits the transition rate of the clock, thereby creating a trade-off between the additive jitter added by the ADC clock receiver and the broadband noise added by the devices that drive the clock input.

Additional noise may couple to the clock path through power supplies. Care must be taken to provide a very low noise power supply and isolated supply return path to minimize noise added to the supply. Spurious noise added to the clock path results in symmetrical, modulated spurs around large input signals. These spurs have a constant magnitude in units of dB relative to the input signal amplitude or carrier, [dBc].

Driving the SYSREF Input

The SYSREF input interface circuit is composed of the differential receiver, internal common-mode bias, SYSREF offset feature, and SYSREF detection feature.

A high impedance (10kΩ) reference biases the input common-mode through internal 1kΩ termination resistors. The bias voltage is similar to the CLKIN input common-mode bias, but the internal differential termination is different. The SYSREF input requires an external 100Ω termination. A network of resistors and switches are included at the input interface to provide a programmable DC offset, referred to as the SYSREF Offset Feature. This feature is configurable via the SPI interface and may be utilized to force a voltage offset at the SYSREF input in the absence of an active SYSREF signal. Following the receiver, an AND gate provides a method for detecting or ignoring incoming SYSREF events.

The timing relationship between the CLKIN and SYSREF signal is very stringent in a JESD204B system, therefore the signal path network of the CLKIN and SYSREF signals must be as similar as possible to ensure that the signal relationship is maintained from the launch of the signal, through their respective channels to the CLKIN and SYSREF input receivers.

AC coupling is recommended for the SYSREF interface as shown in Figure 65. This network closely resembles the AC coupled interface of the CLKIN input shown in Figure 61 with the exception of the 100Ω termination resistor on the source side of the AC coupling capacitors. This resistor is intentionally placed on the source side of the AC coupling capacitors so that the termination does not interfere with the DC biasing capabilities of the SYSREF offset feature. In the case of AC coupling, the coupling capacitors of both the CLKIN and SYSREF interfaces, as well as the SYSREF termination resistor, must be placed as close as possible to the pins of the LM97937.

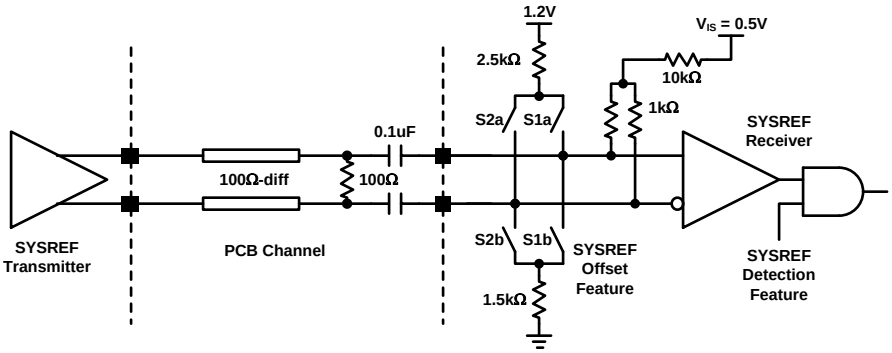


Figure 65. SYSREF Input Receiver and AC Coupled Interface

DC coupling of the SYSREF interface is possible but it is not recommended. DC coupling allows all possible SYSREF signaling types to be used without the use of the SYSREF offset feature, but it has strict common-mode range requirements. The example DC coupled configuration of Figure 66 uses the same technique for the CLKIN example DC coupled interface and also includes the 100Ω external termination. A drawback of the example DC coupled interface is that the resistor divider draws a constant DC current that must be sourced by the SYSREF transmitter.

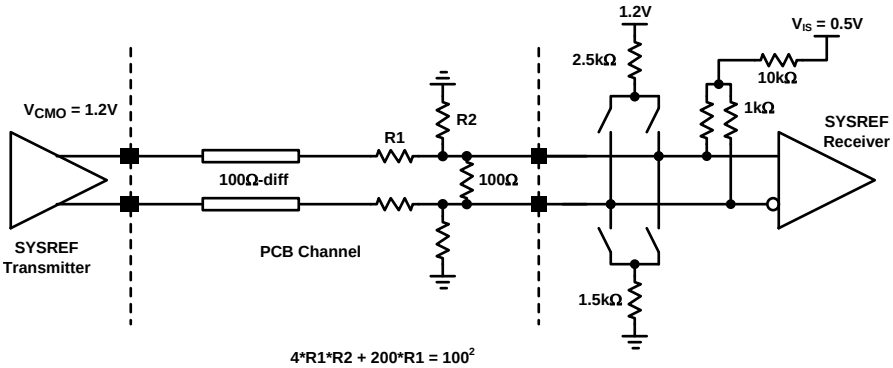


Figure 66. Example DC Coupling to the SYSREF Input

SYSREF Signaling

The SYSREF input may be driven by a number of different types of signals. The supported signal types, shown in Figure 67 (in single-ended form), include periodic, gapped periodic, and one-shot signals. The rising edge of the SYSREF signal is used as a reference to align the internal frame clock and local multi-frame clock (LMFC). To ensure proper alignment of these system clocks, the SYSREF signal must be generated along with the CLKIN signal such that the SYSREF rising edge meets the setup and hold requirements relative to the CLKIN at the LM97937 inputs.

For each rising clock edge that is detected at the SYSREF input, the LM97937 compares the current alignment of the internal frame and LMFC with the SYSREF edge and determines if the internal clocks must be re-aligned. In the case that no alignment is needed, the clocks maintain their current alignment and the JESD204B data link is not broken. In the case that re-alignment is needed, the JESD204B data link is broken and the clocks are re-aligned.

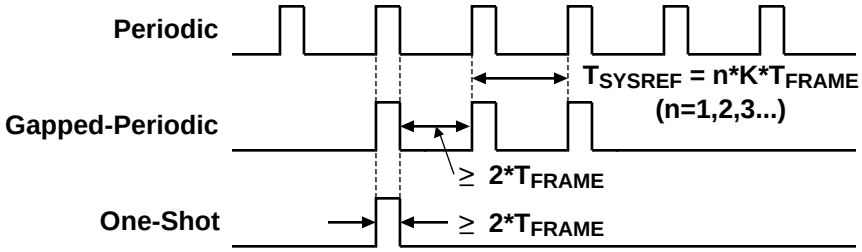


Figure 67. SYSREF Signal Types (Single-Ended Representations)

In the case of a periodic SYSREF signal, the frame and LMFC alignment is established at the first rising edge of SYSREF, and every subsequent rising edge (that properly meets setup and hold requirements) is ignored because the alignment has already been established. A periodic SYSREF must have a period equal to n*K/Fs where 'Fs' is the sampling rate, 'K' is the JESD204B configuration parameter indicating the number of frames per multi-frame, and 'n' is an integer of one or greater. The duty cycle of the SYSREF signal should be greater than 2/K but less than (K-2)/K.

Gapped-period signals contain bursts of pulses. The frame and LMFC alignments are established on the first rising edge of the pulse burst. The rising edges within the pulse burst must be spaced apart by n*K/Fs seconds, similar to the periodic SYSREF signal. Any rising edge that does not abide by this rule or does not meet the setup and hold requirements forces re-alignment of the clocks. The duty cycle requirements are the same as the periodic signal type.

A one-shot signal contains a single rising edge that establishes the frame and LMFC alignment. The single pulse duration must be $2*T_{FRAME}$ or greater.

Gapped-periodic or one-shot signals are recommended for most applications because the SYSREF signal is not active during normal sampling operation. Periodic signals that toggle constantly introduce spurs into the signal spectrum that degrade the sensitivity of the system.

SYSREF Timing

The SYSREF signal must meet setup and hold requirements relative to the CLKIN signal. In the case that the internal CLKIN divider is used and a very high-speed signal is provided to the CLKIN input, the SYSREF signal must meet setup and hold requirements relative to the very high-speed signal at the CLKIN input.

SYSREF Idle, Offset Feature, and Detection Gate Feature

When the signal at the SYSREF input is not actively toggling periodically, the SYSREF signal is considered to be in an "idle" state. The idle state is recommended at any time the LM97937 spurious performance must be maximized. When the SYSREF signal is in the idle state for longer than 1us, an undesirable offset voltage may build up across the AC coupling capacitors between the SYSREF transmitter and the LM97937 input. This offset voltage creates a signal threshold problem, requires a long time to dissipate and therefore prevents quick transition of the SYSREF signal out of the idle state. Two features are provided as a solution and are shown in Figure 65, namely the SYSREF offset feature and SYSREF detection gate.

The SYSREF offset feature is used to intentionally introduce a voltage offset at the SYSREF input pins to prevent voltage built-up across the AC coupling capacitors while the SYSREF signal is in the idle state. The switches shown in Figure 65 are used to apply a +400mV or -400mV or 0mV offset, depending on the voltage of the SYSREF signal at the transmitter in the idle state. Table 8 describes the possible SYSREF idle cases and the corresponding SYSREF offset to apply.

Table 8. SYSREF Offset Feature Usage Cases

SYSREF Signal Type	SYSREF Idle V_{OD} at Tx	SYSREF Idle V_{IS} at Tx	SYSREF offset feature setting
Periodic	N/A	N/A	0mV

Table 8. SYSREF Offset Feature Usage Cases (continued)

SYSREF Signal Type	SYSREF Idle V_{OD} at Tx	SYSREF Idle V_{IS} at Tx	SYSREF offset feature setting
Gapped-Periodic or One-Shot	= 0	V_{CMO} same as non-idle state	0mV
	> 0 (Logic High)	V_{CMO} same as non-idle state	+400mV
	< 0 (Logic Low)	V_{CMO} same as non-idle state	–400mV
Any	0	0	SYSREF offset feature does not support these cases
	Hi-Z	Hi-Z	

In the case that the SYSREF signal idle state has a 0V differential value, or if the LM97937 must be insensitive to noise that may appear on the SYSREF signal, then the SYSREF detection gate may be used. The detection gate is the AND gate shown in Figure 65 that enables or disables propagation of the SYSREF signal through to the internal device logic. If the detection gate is disabled and a false edge appears at the SYSREF input, the signal will not disrupt the internal clock alignment. Note that the SYSREF detection gate is disabled by default therefore the device will not respond to a SYSREF edge until the detection gate is enabled. If the SYSREF detection gate is enabled while the SYSREF input is in a logic high state, a false SYSREF rising edge event is created that temporarily re-aligns the internal frame and LMFC until an actual SYSREF rising edge corrects the clock alignment.

The SYSREF clocking schemes described in Table 9 are highly recommended.

Table 9. Recommended SYSREF Clocking Schemes

Coupling	SYSREF Type	SYSREF Tx Idle State	SYSREF Rx Offset Setting	SYSREF Detection Gate
AC Coupled	One-Shot or Gapped-Periodic(1)	Logic low, Vcm does not change during idle	-400 mV at all times	Disabled during SYSREF idle, enabled during LMFC alignment
DC Coupled	One-Shot or Gapped-Periodic	Logic low or logic high, Vcm does not change during idle	0 mV at all times	Disabled during SYSREF idle, enabled during LMFC alignment

(1) A gapped-periodic signal used in this recommended clocking scheme must have a pulse train duration of less than the RC time constant to prevent voltage offset buildup on the AC coupling capacitors where R=50Ω and C is the value of the AC coupling capacitor. Using a 0.1uF capacitor, the pulse train should be less than 5us.

Driving the SYNCb Input

The SYNCb input is part of the JESD204B interface and is used to send synchronization requests from the serial data receiver to the transmitter, the LM97937. The SYNCb signal, quantified as the (SYNCb+ - SYNCb-), is a differential active low signal. In the case of the LM97937, a JESD204B subclass 1 device, a SYNCb assertion (logic low) indicates a request for synchronization by the receiver.

The SYNCb input is a differential receiver as shown in Figure 68. Resistors provide an internal 100Ω differential termination as well as a voltage divider circuit that gives the SYNCb receiver a wide input common-mode range. The SYNCb signal must be DC coupled from the driver to the SYNCb inputs, therefore the wide common-mode range allows the use of many different logic standards including LVDS and LVPECL. No additional external components are needed for the SYNCb signal path as shown in the interface circuit of Figure 68 but providing an electrical probing site is recommended for system debug.

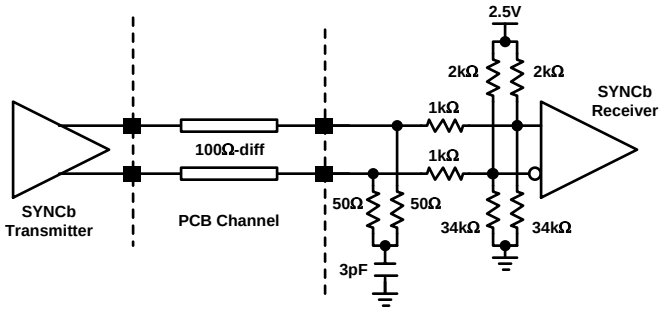


Figure 68. SYNCb Input Receiver and Interface

The SYNCb input is an asynchronous input and does not have sub-clock-cycle setup and hold requirements relative to the CLKIN or any other input to the LM97937. The SYNCb input also does not have setup and hold requirements relative to the frame and LMFC system clocks unless the delay through the JESD204B link is longer than a multi-frame. A design that has link delay greater than a multi-frame does not strictly follow the standard rules for achieving deterministic latency but may be required in many applications and may still achieve deterministic latency. In this case, it is important to de-assert SYNCb within the window of the desired multi-frame period.

Output Serial Interface Considerations

Output Serial Lane Interface

The output high speed serial lanes must be AC coupled to the receiving device with 0.01uF capacitors as shown in Figure 69. DC coupling to the receiving device is not supported. The lane channel on the PCB must be a 100Ω differential transmission line with dominant coupling between the differential traces instead of to adjacent layers. The lane must terminate at a 100Ω termination inside the receiving device. Changing the direction of the channel traces abruptly at angles larger than 45 degrees should be avoided.

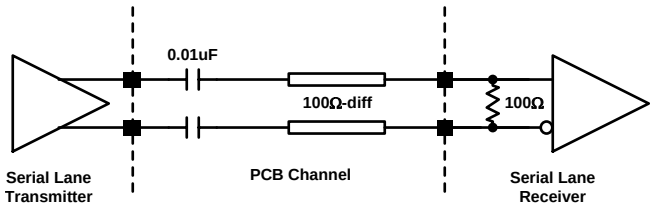


Figure 69. High Speed Serial Lane Interface

The recommended spacing between serial lanes is 3x the differential line spacing or greater. High speed serial lanes should be routed on top of or below adjacent, quiet ground planes to provide shielding. It is recommended that other high speed signal traces do not cross the serial lanes on adjacent PCB layers. If absolutely necessary, crossing should occur at a 90 degree angle with the trajectory of the serial lane to minimize coupling.

The integrity of the data transfer from the transmitter to receiver is limited by the accuracy of the lane impedance and the attenuation as the signal travels down the lane. Inaccurate or varying impedance and frequency dependent attenuation results in increased inter-symbol interference (ISI, part of deterministic jitter) and reduced signal-to-noise ratio which limits the ability of the receiver to accurately recover the data.

Two features are provided in the LM97937 serial transmitters to compensate attenuation and ISI caused by the serial lane: voltage swing control and de-emphasis.

Voltage Swing and De-Emphasis Optimization

Voltage swing control compensates for attenuation across all frequencies through the channel at the expense of power consumption. Increasing the voltage swing increases the power consumption. De-emphasis compensates for the frequency dependent attenuation of the channel but results in attenuation at lower frequencies. The voltage swing control and de-emphasis feature may be used together to optimally compensate for attenuation effects of the channel.

The frequency response of the PCB channel is typically lowpass with more attenuation occurring at higher frequencies. The de-emphasis implemented in the LM97937 is a form of linear, continuous-time equalization that shapes the signal at the transmitter into a high-pass response to counteract the low-pass response of the channel. The de-emphasis setting should be selected such that the equalizer's frequency response is the inverse of the channel's response. Therefore, transferring data at the highest speeds over long channel lengths requires knowledge of the channel characteristics.

Optimization of the de-emphasis and voltage swing settings is only necessary if the ISI caused by the channel is too great for reception at the desired bit rate. Many applications will perform with an adequate BER using the default settings.

Minimizing EMI

High data transfer rates have the potential to emit radiation. EMI may be minimized using the following techniques.

- Use differential stripline channels on inner layers sandwiched between ground planes instead of routing microstrip pairs on the surface layers.
- Avoid routing lanes near the edges of boards.
- Enable data scrambling to spread the frequency content of the transmitted data.
- If the serial lane must travel through an interconnect, choose a connector with good differential pair channels and shielding.
- Ensure lanes are designed with an accurate, 100Ω characteristic impedance and provide accurate 100Ω terminations inside the receiving device.

JESD204B System Considerations

Frame and Local Multi-Frame Clock (LMFC) Alignment

Frame and LMFC clocks are generated inside the LM97937 and are required to properly align the phase of the serial data leaving the device. The phase of the frame and multi-frame clocks is determined by the frame alignment step for JESD204B link initialization as shown in Figure 49. These clocks are not accessible outside the device. The frequencies of the frame and LMFC must be equal to the frame and LMFC of the device receiving the serial data.

Link Interruption

The internal frame and multi-frame clocks must be stable to maintain the JESD204B link. The LM97937 is designed to maintain the JESD204B link in most conditions but some features interrupt the internal clocks and break the link.

The following actions cause a break in the JESD204B link:

- The LM97937 is configured into power-down mode or sleep mode
- The LM97937 CLKIN clock divider setting is changed
- The serial data receiver performs a synchronization request
- The LM97937 detects a SYSREF assertion that is not aligned with the internal frame or multi-frame clocks
- The CLKIN input is interrupted
- Power to the device is interrupted

The following actions DO NOT cause a change in clock alignment nor break the JESD204B link:

- The sampling clock phase adjustment settings of the LM97937 are changed
- The ambient temperature or operating voltages are varied across the ranges specified in the normal operating conditions.

- The LM97937 detects a SYSREF assertion that is aligned with the internal frame and multi-frame clocks

Frame and LMFC Clock Alignment Procedure

When the LM97937 is powered up, the internal frame and local multi-frame clocks initially assume a default phase alignment. To ensure determinist latency through the JESD204B link, the frame and LMFC clocks of the LM97937 must be aligned in the system. Alignment of the LM97937 clocks is performed with the following steps:

1. Enable the SYSREF signal driver. See SYSREF Signaling for more information.
2. Configure the SYSREF Offset feature appropriately based on the SYSREF signal and channel. See SYSREF Idle, Offset Feature, and Detection Gate Feature for more information.
3. Enable detection of the SYSREF signal at the LM97937 by enabling the SYSREF detection gate.
4. Apply the desired SYSREF signal at the LM97937 SYSREF input. The SYSREF signal must meet setup and hold times relative to the CLKIN signal.
5. Disable detection of the SYSREF signal by disabling the SYSREF gate.
6. Configure the SYSREF driver into its idle state.

Synchronization Requests and SYNCb Alignment in Multi-Device Systems

When a JESD204B link must be established, the transmitting and receiving devices must perform the process described in the JESD204B Link Initialization section to establish the link. Part of the process is the synchronization request, performed by asserting the SYNCb signal. The alignment of the SYNCb assertion with respect to other clocks in the system is not important unless the total link delay is greater than a multi-frame period.

Clock Configuration Examples

The features provided in the LM97937 allow for a number of clock and JESD204B link configurations. These examples in Table 10 show some common implementations that may be used as a starting point for a more customized implementation.

Table 10. Example LM97937 Clock Configurations

Parameter	Example #1	Example #2	Example #3
CLKIN Frequency	370 MHz	1,480 MHz	2,000 MHz
CLKIN Divider	1	4	8
Sampling Rate	370 MSPS	370 MSPS	250 MSPS
K (Frame per Multi-frame)	20	32	16
LMFC Frequency	18.5 MHz	11.5625 MHz	15.625 MHz
SYSREF Frequency(1)	18.5 MHz	11.5625 MHz	15.625 MHz
Dual Lane Serial Bit Rate (L=2)	3.7 Gb/s	3.7 Gb/s	L=2 does not support K<17
Single Lane Serial Bit Rate (L=1)	7.4 Gb/s	7.4 Gb/s	5 Gb/s

(1) The SYSREF frequency for a continuous SYSREF signal may be the indicated frequency 'f_{LMFC}' or integer sub-harmonic such as $f_{LMFC}/2$, $f_{LMFC}/3$, etc. Gapped-periodic SYSREF signals should have pulses spaced by the associated periods $1/f_{LMFC}$, $2/f_{LMFC}$, $3/f_{LMFC}$, etc.

Configuring the JESD204B Receiver

The ASIC or FPGA device that receives the JESD204B data from the LM97937 must be configured properly to interpret the serial stream. Table 5 describes the JESD204B parameter information transmitted during the initial Lane Alignment (ILA) sequence and may be used to dynamically configure the receiving device. Due to the various arrangements of output data across different operational modes, some parameters (N, N', CS, CF) do not always reflect the data properties in all modes. Therefore the ILA information does not completely describe the data output from the LM97937 in all modes.

Power Supply Design and Decoupling

The LM97937 is a very high dynamic range device and therefore requires very low noise power supplies. LDO-type regulators, capacitive decoupling, and series isolation devices like ferrite beads are all recommended.

LDO-type low noise regulators should be used to generate the 1.2, 1.8V and 3.3V supplies used by the device. To improve power efficiency, a switching-type regulator may precede the LDO to efficiently drop a supply to an intermediate voltage that satisfies the drop-out requirements of the LDO. Following a switching-type regulator with an LDO is recommended to provide the best filtering of the switching noise. Additional ferrite beads and LC filters may be used to further suppress noise. Supplying power to multiple devices in a system from one regulator may result in noise coupling between the multiple devices, therefore series isolation devices and additional capacitive decoupling is recommended to improve the isolation.

Decoupling capacitors must be used at each supply pin to prevent supply or ground noise from degrading the dynamic performance of the ADC and to provide the ADC with a well of charge to minimize voltage ripple caused by current transients. The recommended supply decoupling scheme is to have a ceramic X7R 0201 0.01µF and a X7R 0402 0.1µF capacitor at each supply pin. The 0201 capacitor must be placed on the same layer as the device as close to the pin as possible to minimize the AC decoupling path length from the supply pin, through the capacitor, to the nearest adjacent ground pin. The 0402 capacitor should also be close to the pins. Placing the capacitor on the opposite board side is not recommended. Each voltage supply should also have a single 10µF decoupling capacitor near the device but the proximity to the supply pins is less critical.

The BP2.5 pin is an external bypass pin used for stabilizing an internal 2.5V regulator and must have a ceramic or tantalum 10µF capacitor and a ceramic 0402 0.1µF capacitor. The 0.1µF capacitor should be placed as close to the BP2.5 pin as possible.

The power supplies must be applied to the LM97937 in this specific order: 1) VA3.3, 2) VA1.8, 3) VA1.2, 4) VD1.2. First, the VA3.3 (+3.3V) must be applied to provide the bias for the ESD diodes. The VA1.8 (+1.8V) supply should be applied next, followed by the VA1.2 (+1.2V) supply, and then followed by the VD1.2 (+1.2V) supply. As a guideline, each supply should stabilize to within 20% of the final value within 10 ms and before enabling the next supply in the sequence. If the stabilization time is longer than 10ms, then the system should perform the calibration procedure after the supplies have stabilized. Turning power supplies off should occur in the reverse order. An alternate power-up sequence is also supported which allows enabling the 1.2V supplies in any order or at the same time. The alternate sequence is 1) VA3.3, 2) VA1.2 / VD1.2, 3) VA1.8.

PCB Design and Thermal Considerations

The design of the PCB is critical to achieve the full performance of the LM97937. Defining the PCB stackup should be the first step in the board design. Experience has shown that at least 6 layers are required to adequately route all required signals to and from the device. Each signal routing layer must have an adjacent solid ground plane to control signal return paths to have minimal loop areas and to achieve controlled impedances for microstrip and stripline routing. Power planes must also have adjacent solid ground planes to control supply return paths. Minimizing the spacing between supply and ground planes improves performance by increasing the distributed decoupling. The recommended stack-up for a 6-layer board design is shown in Figure 70.

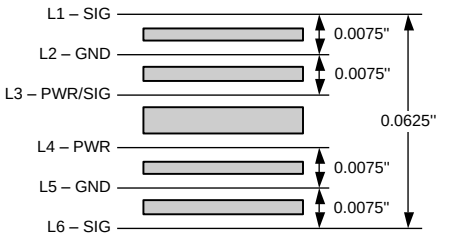


Figure 70. Recommended PCB Layer Stack-Up for a 6–Layer Board

Although the LM97937 consists of both analog and digital circuitry, solid ground planes that encompass the device and its input and output signal paths is highly recommended. Split ground planes that divide the analog and digital portions of the device are not recommended. Split ground planes may improve performance if a nearby, noisy, digital device is corrupting the ground reference of the analog signal path. When split ground planes are employed, one must carefully control the supply return paths and keep the paths on top of their respective ground reference planes.

The exposed thermal pad of the LM97937 draws heat from the silicon down into the PCB to prevent overheating and must attach to the landing pad with a quality solder connection to maximize thermal conductivity. Overly hot operating temperatures may be alleviated further by increasing the PCB size, filling surface layers with ground planes to increase heat radiation, or using a thermally conductive connection between the package top and a heat sink.

Quality analog input signal and clock signal path layout is required for full dynamic performance. Symmetry of the differential signal paths and discrete components in the path is mandatory and symmetrical shunt-oriented components should have a common grounding via. The high frequency requirements of the input and clock signal paths necessitate using differential routing with controlled impedances and minimizing signal path stubs (including vias) when possible.

Coupling onto or between the clock and input signal paths must be avoided using any isolation techniques available including distance isolation, orientation planning to prevent field coupling of components like inductors and transformers, and providing well coupled reference planes. Via stitching around the clock signal path and the input analog signal path provides a quiet ground reference for the critical signal paths and reduces noise coupling onto these paths. Sensitive signal traces MUST NOT cross other signal traces or power routing on adjacent PCB layers, rather a ground plane must separate the traces. If necessary, the traces should cross at 90° angles to minimize crosstalk.

Coupling of ambient signals into the signal path is reduced by providing quiet, close reference planes and by maintaining signal path symmetry to ensure the coupled noise is common-mode. Faraday caging may be used in very noisy environments and high dynamic range applications to isolate the signal path.

Register Map

Register	ADDR	DFLT	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
CONFIG_A	0x0000	0x3C	SR	Res (0)	ASCEND	Res (1)	PAL[3:0]			
DEVICE _CONFIG	0x0002	0x00	Reserved (000000)						PD_MODE[1:0]	
CHIP_TYPE	0x0003	0x03	Reserved (0000)				CHIP_TYPE[3:0]			
CHIP_ID	0x0004	0x03	CHIP_ID[7:0]							
	0x0005	0x00	CHIP_ID[15:8]							
CHIP _VERSION	0x0006	0x00	CHIP_VERSION[7:0]							
VENDOR_ID	0x000C	0x51	VENDOR_ID[7:0]							
	0x000D	0x04	VENDOR_ID[15:8]							
SPI_CFG	0x0010	0x01	Reserved (000000)						VSPI[1:0]	
OM1	0x0012	0x81	DF	Res (00)		IDLE[1:0]		SYS_EN	Res(01)	
OM2	0x0013	0x80	Reserved (010)			CLKDIV		Res (0)	Res(0)	Res (0)
IMB_ADJ_A	0x0014	0x00	Res (0)	AMPADJ_A[2:0]			PHADJ_A[3:0]			
IMB_ADJ_B	0x0015	0x00	Res (0)	AMPADJ_B[2:0]			PHADJ_B[3:0]			
Addr 0x0016-0x0018 Reserved										
CDLY_CTRL	0x0019	0x00	Reserved (000)			CDLY_EN	CRS_DLY[3:0]			
Addr 0x001A-0x003A Reserved										
OVR_HOLD	0x003B	0x00	Reserved (000000)						OVR_HOLD[1:0]	
OVR_TH	0x003C	0x00	OVR_TH[7:0]							
DC_MODE	0x003D	0x00	Reserved (00000)					DC_TC		DC_EN
Addr 0x003E-0x0046 Reserved										
SER_CFG	0x0047	0x00	Res(0)	SEL_VOD[2:0]			Res(0)	SEL_DEM[2:0]		

Register	ADDR	DFLT	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]
Addr 0x0048-0x005F Reserved										
JESD_CTRL1	0x0060	0x7D	SCR_EN	K_M1[4:0]					L_M1	JESD_EN
JESD_CTRL2	0x0061	0x00	Reserved (0000)				JESD_TEST_MODE[3:0]			
JESD_RSTEP	0x0062	0x01	JESD_RSTEP[7:0]							
	0x0063	0x00	JESD_RSTEP[15:8]							
Addr 0x0064-0x006B Reserved										
JESD_STATUS	0x006C	N/A	Res (0)	LINK	SYNC	REALIGN	ALIGN	PLL _LOCK	CAL _DONE	CLK _RDY
Addr 0x006D-0x006F Reserved										
DATA_CTRL	0x0070	0x20	Reserved (00100)					TEST _DATA	Res (0)	DSRC
BITB_CTRL1	0x0071	0x00	Reserved (00000)					HIGH_RES[1:0]		BB _MODE
Addr 0x0072 Reserved										
BITB_CTRL2	0x0073	0x0A	N_LENGTH[7:0]							
Addr 0x0074-0x0077 Reserved										
SNRB_CTRL	0x0078	0x00	Reserved (000000)						SEL_COEF[1:0]	
Addr 0x0079- Reserved										

Register Descriptions

CONFIG_A				Address: 0x0000	Default: 0x3C
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7]	SR	R/W	0	Soft Reset. Setting this bit to 1 causes all registers to be reset to their default state. This bit is self-clearing.	
[6]	Reserved	R/W	0	Reserved. Must be written with 0.	
[5]	ASCEND	R/W	1	Order of address change during streaming reads or writes. 0 : Address is decremented during streaming reads/writes. 1 : Address is incremented during streaming reads/writes (default).	
[4]	Reserved	R	1	Reserved. Must be written with 1.	
[3:0]	PAL[3:0]	R/W	1100	Palindrome Bits. Bits [3:0] must properly match bits [7:4] such that bit 3 = bit 4, bit 2 = bit 5, bit 1 = bit 6, bit 0 = bit 7 or a write command to this address will fail.	

DEVICE CONFIG				Address: 0x0002	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:2]	Reserved	R/W	000000	Reserved. Must be written with 000000.	
[1:0]	PD_MODE [1:0]	R/W	00	Power-Down Mode 00 : Normal operation (default) 01 : Reserved 10 : Sleep operation (faster resume) 11 : Power-Down (slower resume) NOTE: Cycling the device through Power-Down mode and back to Normal Mode performs ADC calibration. This function is mandatory for certain operating conditions as described in ADC Core Calibration. Exiting from power-down mode requires special considerations as described in Power Down and Sleep Modes.	

CHIP_TYPE				Address: 0x0003	Default: 0x03
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:4]	Reserved	R/W	0000	Reserved. Must be written with 0000.	
[3:0]	CHIP_TYPE[3:0]	R	0011	Chip type. Always returns 0x03, indicating that the part is a high speed ADC.	

CHIP_ID				Addresses: [0x0005, 0x0004]	Default: [0x00, 0x03]
Bit	**Bit name**	**R/W**	**Def**	**Description**	
0x0004[7:0]	CHIP_ID[7:0]	R	0x03	Chip ID least significant word.	
0x0005[7:0]	CHIP_ID[15:8]	R	0x00	Chip ID most significant word.	

CHIP_VERSION				Address: 0x0006	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:0]	CHIP_VERSION[7:0]	R	0x00	Chip Version.	

VENDOR_ID				Addresses: [0x000D, 0x000C]	Default: [0x04, 0x51]
Bit	**Bit name**	**R/W**	**Def**	**Description**	
0x000C[7:0]	VENDOR_ID[7:0]	R	0x51	Vendor ID. Texas Instruments vendor ID is 0x0451.	
0x000D[7:0]	VENDOR_ID[15:8]	R	0x04		

SPI_CFG				Address: 0x0010	Default: 0x01
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:2]	Reserved	R/W	000000	Reserved. Must be written with 000000.	
[1:0]	VSPI	R/W	01	SPI Interface Logic Level. Changes the SDO output logic level. 00 : 1.2V 01 : 3.3V (default) 10 : 2.5V 11 : 1.8V CAUTION: This register must be configured (written) before making a read command with the SPI interface to prevent potential damage to other devices connected to the SPI bus. The SPI inputs (SDI, SCLK, CSb) are compatible with 1.2V-3.3V logic levels.	

OM1 (Operational Mode 1)				Address: 0x0012	Default: 0x81
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7]	DF	R/W	1	Output Data Format 0 : Offset Binary 1 : Signed 2's Complement (default)	
[6:5]	Reserved	R/W	00	Reserved. Must be written with 00.	
[4:3]	IDLE[1:0]	R/W	00	SYSREF Idle state offset configuration. 00 : No offset applied (default) 01 : SYSREF idles low (de-asserted) with -400mV offset 10 : SYSREF idles high (asserted) with +400mV offset 11 : Reserved	
[2]	SYS_EN	R/W	0	SYSREF Detection Gate Enable 0 : SYSREF Gate is disabled and input is ignored (default) 1 : SYSREF Gate is enabled	
[1:0]	Reserved[1:0]	R/W	01	Reserved. Must be written with 01.	

OM2 (Operational Mode 2)				Address: 0x0013	Default: 0x80
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:5]	Reserved	R/W	100	Reserved.	
[4:3]	CLKDIV[1:0]	R/W	00	Clock divider ratio. Sets the value of the clock divide factor, CLKDIV 00 : Divide by 1, CLKDIV=1 (default) 01 : Divide by 2, CLKDIV=2 10 : Divide by 4, CLKDIV=4 11 : Divide by 8, CLKDIV=8	
[2:0]	Reserved	R/W	000	Reserved.	

IMB_ADJ_A (Imbalance Adjust, Ch.A)				Address: 0x0014	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7]	Reserved	R/W	0	Reserved. Must be written with 0.	
[6:4]	AMPADJ_A[2:0]	R/W	000	Analog input amplitude imbalance correction for channel A 7 = +30Ω VIN+, -30Ω VIN- 6 = +20Ω VIN+, -20Ω VIN- 5 = +10Ω VIN+, -10Ω VIN- 4 = Reserved 3 = -30Ω VIN+, +30Ω VIN- 2 = -20Ω VIN+, +20Ω VIN- 1 = -10Ω VIN+, +10Ω VIN- 0 = +0Ω VIN+, -0Ω VIN- (default) Resistance changes indicate variation of the internal single-ended termination.	
[3:0]	PHADJ_A[3:0]	R/W	0000	Analog input phase imbalance correction for channel B 15 = +1.68 pF VIN- ... 9 = +0.48 pF VIN- 8 = +0.24 pF VIN- 7 = +1.68 pF VIN+ ... 2 = +0.48 pF VIN+ 1 = +0.24 pF VIN+ 0 = +0 pF VIN+, +0 pF VIN- (default) Capacitance changes indicate the addition of internal capacitive load on the given pin.	

IMB_ADJ_B (Imbalance Adjust, Ch.B)				Address: 0x0015	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7]	Reserved	R/W	0	Reserved. Must be written with 0.	
[6:4]	AMPADJ_B[2:0]	R/W	000	Analog input amplitude imbalance correction for channel B. See description for IMB_ADJ_A	
[3:0]	PHADJ_B[3:0]	R/W	0000	Analog input phase imbalance correction for channel B. See description for IMB_ADJ_A	

CDLY_CTRL (Coarse Delay Control)				Address: 0x0019	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:5]	Reserved	R/W	000	Reserved. Must be written as 000.	
[4]	CDLY_EN	R/W	0	Coarse sampling clock phase delay enable 0 : Coarse clock delay disabled (default) 1 : Coarse clock delay enabled Note: • Coarse delay is not supported when the divide ratio is set to 1 (CLKDIV=00)	

CDLY_CTRL (Coarse Delay Control)				Address: 0x0019				Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**				
[3:0]	CRS_DLY[3:0]	R/W	0000	Coarse sampling clock phase delay adjust. Adjusts the ADC clock delay in coarse increments. The step size is one half of the CLKIN input period.				
				Coarse Clock Delay (in unit of CLKIN periods)				
				CRS_DLY	CLKDIV=11 (divide-by-8)	CLKDIV=10 (divide-by-4)	CLKDIV=01 (divide-by-2)	CLKDIV=00 (divide-by-1)
				0000 (default)	1.0	1.0	1.0	Reserved. Coarse delay disabled for CLKDIV=00 (divide-by-1)
				0001	1.5	1.5	1.5	
				0010	2.0	2.0	0.0	
				0011	2.5	2.5	0.5	
				0100	3.0	3.0	Reserved	
				0101	3.5	3.5		
				0110	4.0	0.0		
				0111	4.5	0.5		
				1000	5.0	Reserved		
				1001	5.5			
				1010	6.0			
				1011	6.5			
				1100	7.0			
				1101	7.5			
				1110	0.0			
				1111	0.5			
				Note: • When (CLKDIV = 01, 10, or 11) and the CRS_DLY setting is 0000, the delay is 1 device clock, not 0. • Any write to this register will restart the Bit-Burst engine. • Do not change the coarse delay when the ADC calibration is running. • The coarse delay adjustment is common to both channel A and B.				

OVR_HOLD (Over-Range Hold)				Address: 0x003B	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:2]	Reserved	R/W	000000	Reserved. Must be written as 000000.	
[1:0]	OVR_HOLD[1:0]	R/W	00	Over-range hold function. In the event of an input signal larger than the full-scale range, an over-range event occurs and the over-range indicators are asserted. OVR_HOLD determines the amount of time the over-range indicators remain asserted after the input signal has reduced below full-scale. 00 : OVR indicator extended by +0 sampling clock cycles (default) 01 : OVR indicator extended by +3 sampling clock cycles 10 : OVR indicator extended by +7 sampling clock cycles 11 : OVR indicator extended by +15 sampling clock cycles Note: • The over-range indicators are only active while the device is in SNRBoost mode. The over-range indicators are not active in Bit-Burst mode.	

OVR_TH (Over-Range Threshold)				Address: 0x003C			Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**			
[7:0]	OVR_TH[7:0]	R/W	00000000	Over-Range Threshold. This field is an unsigned value from 0 to 255. OVR_TH sets the over-range detection thresholds for the ADC. If the 16-bit signed data exceeds the thresholds, then the over-range bit is set. The 16-bit thresholds are ±OVR_TH*128 codes from the low and high full-scale codes (32,767 and -32,768 in signed 2's complement). If OVR_TH is zero, then the default threshold is used (full scale).			
				OVR_TH	16-bit Threshold		Threshold Relative to Peak Full Scale [dB]
					2' Complement	Offset Binary	
				255 (0xFF)	±32640	65,408 / 128	-0.03
				254 (0xFE)	±32512	65,280 / 256	-0.07
				...			
				128 (0x80)	±16384	49,152 / 16,384	-6.02
				...			
				2 (0x02)	±256	33,024 / 32,512	-42.14
				1 (0x01)	±128	32,896 / 32,640	-48.16
				0 (0x00) (default)	+32,767 / -32768	65,535 / 0	–0.0

DC_MODE (DC Offset Correction Mode)				Address: 0x003D			Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**			
[7:3]	Reserved	R/W	000000	Reserved. Must be written as 00000.			
[2:1]	TC_DC	R/W	00	DC offset filter time constant. The time constant determines the filter bandwidth of the DC high-pass filter.			
				TC_DC	Time Constant (F_S = 370MSPS)	3dB Bandwidth (F_S = 370MSPS)	3dB Bandwidth (Normalized)
				00	11 us	14 kHz	37e-6 * Fs
				01	89 us	1.8 kHz	4.9e-6 * Fs
				10	708 us	224 Hz	605e-9 * Fs
				11	5.7 ms	28 Hz	76e-9 * Fs
[0]	DC_EN	R/W	0	DC Offset Correction Enable 0 : Disable DC Offset Correction 1 : Enable DC Offset Correction			

SER_CFG (Serial Lane Transmitter Configuration)				Address: 0x0047	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7]	Reserved	R/W	0	Reserved. Must be written as 0.	
[6:4]	SEL_VOD[2:0]	R/W	000	Serial lane transmitter driver output differential peak-peak voltage amplitude. 000 : 0.580 V (default) 001 : 0.680 V 010 : 0.760 V 011 : 0.860 V 100 : 0.960 V 101 : 1.060 V 110 : 1.140 V 111 : 1.240 V Note: Reported voltage values are nominal values at low lane rates with de-emphasis disabled	
[3]	Reserved	R/W	0	Reserved. Must be written as 0.	

SER_CFG (Serial Lane Transmitter Configuration)				Address: 0x0047	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[2:0]	SEL_DEM[2:0]	R/W	000	Serial lane transmitter de-emphasis.	
				SEL_DEM	De-emphasis [dB]
				000	0.0
				001	0.4
				010	1.2
				011	2.1
				100	2.8
				101	3.8
				110	4.8
				111	6.8

JESD_CTRL1 (JESD Configuration Control 1) **Note: Before altering any parameters in this register, one must set JESD_EN=0. Changing parameters while JESD_EN=1 is not supported.**				Address: 0x0060	Default: 0x7D
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7]	SCR_EN	R/W	0	Scrambler enable. 0 : Disabled (default) 1 : Enabled Note: • JESD_EN must be set to 0 before altering this field.	
[6:2]	K_M1[4:0]	R/W	11111	Number of frames per multi-frame, K, minus 1. The binary values of K_M1 represent the value (K - 1) 00000 : Reserved 00001 : Reserved … 00111 : Reserved 01000 : K = 9 … 11111 : K = 32 (default) Note: • In single-lane mode, K must be in the range 9 to 32. Values outside this range are either reserved or may produce unexpected results. • In dual-lane mode, K must be in the range 17 to 32. Values outside this range are either reserved or may produce unexpected results. • JESD_EN must be set to 0 before altering this field.	
[1]	L_M1	R/W	0	Number of serial lanes used per channel, L, minus 1. The binary value of L_M1 represents the value (L - 1). When L=1, data is transmitted on SA0 and SB0. When L=2, data is transmitted on SA0, SA1, SB0, SB1. 0 : Single-lane mode (L = 1) (default) 1 : Dual-lane mode (L = 2) Note: • If L_M1 is changed then K_M1 must be updated accordingly. • JESD_EN must be set to 0 before altering this field.	
[0]	JESD_EN	R/W	1	JESD204B link enable. When enabled, the JESD204B link synchronizes and transfers data normally. When the link is disabled, the serial transmitters output a repeating, alternating stream or 0's and 1's. The disabled state is not intended for use as a test pattern. 0 : Disabled 1 : Enabled (default)	

JESD_CTRL2 (JESD Configuration Control 2) Note: Before altering any parameters in this register, one must set JESD_EN=0. Changing parameters while JESD_EN=1 is not supported.				Address: 0x0061	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:4]	Reserved	R/W	0000	Reserved. Must be written as 0000.	
[3:0]	JESD_TEST_MODES[3:0]	R/W	0000	JESD204B test modes. 0000 : Test mode disabled. Normal operation (default) 0001 : PRBS7 test mode 0010 : PRBS15 test mode 0011 : PRBS23 test mode 0100 : Reserved 0101 : ILA test mode 0110 : Ramp test mode 0111 : K28.5 test mode 1000 : D21.5 test mode 1001: Logic low test mode (serial outputs held low) 1010: Logic high test mode (serial outputs held high) 1011 – 1111 : Reserved Note: • JESD_EN must be set to 0 before altering this field.	

JESD_RSTEP (JESD Ramp Pattern Step)				Addresses: [0x0063, 0x0062]	Default: [0x00, 0x01]
Bit	**Bit name**	**R/W**	**Def**	**Description**	
0x0062[7:0]	JESD_RSTEP[7:0]	R/W	0x01	JESD204B Ramp Test Mode Step. The binary value JESD_RSTEP[15:0] corresponds to the step of the Ramp Mode step. A value of 0x0000 is not allowed. Note: • JESD_EN must be set to 0 before altering this field.	
0x0063[7:0]	JESD_RSTEP[15:8]	R/W	0x00		

JESD_STATUS (JESD Link Status)				Address: 0x006C	Default: N/A
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7]	Reserved	R	N/A	Reserved.	
[6]	LINK	R	N/A	JESD204B Link status. This bit becomes set when link initialization is finished, transmission of the ILA sequence is complete, and valid data is being transmitted. 0 : Link NOT established 1 : Link established and valid data transmitted	
[5]	SYNC	R	N/A	JESD204B Link synchronization request status. This bit indicates whether a synchronization request is being received at the SYNCb input. 0 : Synchronization request received at the SYNCb input and synchronization is in progress 1 : Synchronization not requested Note: • SYNCb must be asserted for at least 4 local frame clocks before synchronization is initiated. • The SYNC status bit reports the status of link synchronization according to the LM97937 but does not necessarily report the current status of the signal at the SYNCb input.	
[4]	REALIGN	R/W	N/A	SYSREF re-alignment status. This bit becomes set when a SYSREF event causes a shift in the phase of the internal frame or LMFC clocks. Note: • This bit is set upon power-up and should be cleared to use it's function. • Write a 1 to REALIGN to clear the bit field to a 0 state. • SYSREF events that do not cause a frame or LMFC clock phase adjustment do not set this register bit.	

JESD_STATUS (JESD Link Status)				Address: 0x006C	Default: N/A
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[3]	ALIGN	R/W	N/A	SYSREF alignment status. This bit is set when the ADC has processed a SYSREF event and indicates that the local frame and multi-frame clocks are now based on a SYSREF event. Note: • Write a 1 to ALIGN to clear the bit field to a 0 state. • Any rising-edge SYSREF event will set the ALIGN bit.	
[2]	PLL_LOCK	R	N/A	PLL lock status. This bit is set when the serializer's PLL has achieved lock. 0 : PLL unlocked 1 : PLL locked	
[1]	CAL_DONE	R	N/A	ADC calibration status. This bit indicates when the ADC calibration algorithm is processing. 0 : Calibration may be in progress or not yet completed 1 : Calibration is complete Note: • CAL_DONE does not indicate if the ADC calibration procedure has been properly followed • Calibration must complete before SYSREF detection (SYS_EN) may be enabled • Calibration must complete before the any clock phase delay adjustments are made.	
[0]	CLK_RDY	R	N/A	Input clock status. This bit is set when the ADC is powered up and detects an active clock signal at the CLKIN input. 0 : CLKIN not detected 1 : CLKIN detected	

DATA_CTRL (Output Data Source Control)				Address: 0x0070	Default: 0x20
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:3]	Reserved	R/W	00100	Reserved. Must be written as 00100.	
[2]	TEST_DATA	R/W	0	ADC test pattern enable. When enabled, data from the ADC core is replaced by test pattern data before the data is passed to the downstream SNRBoost or Bit-Burst signal processing. The test pattern depends on the DSRC bit. 0 : Disabled ADC test pattern (default) 1 : Enable ADC test pattern DSRC = 0 (SNRBoost) : Test pattern is input into the SNRBoost block. Pattern is a 16-bit repeating [0, 26280, 0, -26328] sequence (signed 16-bit number) that appears in the FFT spectrum as a tone, centered at Fs/4, and just below the clipping level. DSRC = 1 (Bit-Burst) : Test pattern is input into the Bit-Burst block. The test pattern is a 16-bit signed static value of 26328. The value is processed according to whether the Bit-Burst block is in high-resolution (14- or 12-bit) or low-resolution mode (9-bit). Note: • The ADC test pattern function is independent from the test patterns outlined in the JESD_CTRL2 register. The TEST_DATA bit enables a test pattern at the ADC core output, prior to entering the JESD204B core. The JESD_TEST_MODES field enables test patterns within the transport and link layers of the JESD204B core.	
[1]	Reserved	R/W	0	Reserved. Must be written as 0.	

DATA_CTRL (Output Data Source Control)				Address: 0x0070	Default: 0x20
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[0]	DSRC	R/W	0	Data source select. Determines whether the source data that enters the JESD204 core comes from the SNRBoost or Bit-Burst block. Indicates whether the mode of operation is SNRBoost or Bit-Burst mode. 0 : Enable SNRBoost mode (default) 1 : Enable Bit-Burst mode	

BITB_CTRL1 (Bit-Burst Control 1)				Address: 0x0071	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:3]	Reserved	R/W	00000	Reserved. Must be written as 00000.	
[2:1]	HIGH_RES[1:0]	R/W	00	Bit-Burst High Resolution select. Configures the High Resolution Bit-Burst phase to have the indicated bit resolution and duty-cycle 00 : 14-bit output data with 25% duty cycle (default) 01 : 12-bit output data with 50% duty cycle 10 : Reserved 11 : Reserved	
[0]	BB_MODE	R/W	0	Bit-Burst sub-mode select. 0 : Stream sub-mode (default) 1 : Trigger sub-mode	

BITB_CTRL2 (Bit-Burst Control 2)				Address: 0x0073	Default: 0x0A
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:0]	N_LENGTH[7:0]	R/W	00001010	Bit-Burst High Resolution Duration. The binary value of N_LENGTH determines the sample number duration of the high resolution Bit-Burst phase. The high resolution phase duration is calculated as 2^(N_LENGTH). The default value of N_LENGTH = 10 results in a 2^10 sample duration. Valid values of N_LENGTH are from 10 to 25.	

SNRB_CTRL (SNRBoost Control)				Address: 0x0078	Default: 0x00
Bit	**Bit name**	**R/W**	**Def**	**Description**	
[7:2]	Reserved	R/W	000000	Reserved. Must be written as 000000.	
[1:0]	SEL_COEFF[1:0]	R/W	00	SNRBoost Modulator Coefficients. Determines the spectral shape of the quantization noise in the output data spectrum. The SNRBoost modulator has bandpass shaping with a center frequency, F_C, expressed relative to the sampling rate, F_S. 00 : $F_C = 0.25 * F_S$ (default) 01 : $F_C = 0.29 * F_S$ 10 : $F_C = 0.21 * F_S$ 11 : Reserved	

REVISION HISTORY

Changes from Original (December 2013) to Revision A **Page**

- Changed buffer transistors from PNP to NPN 6
- Changed SPI logic compatibility in description for terminal 54 7
- Added the $V_{D1.2}$ supply to the description for total power consumption 12
- Changed DFLT value for CHIP_ID ADDR 0x0004 from 0x07 to 0x03 62
- Added a bit[0] row to the DC_MODE register description table 67

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM97937RMER	ACTIVE	WQFN	RME	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-3-260C-168 HR	-40 to 85	LM97937	Samples
LM97937RMET	ACTIVE	WQFN	RME	56	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-3-260C-168 HR	-40 to 85	LM97937	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

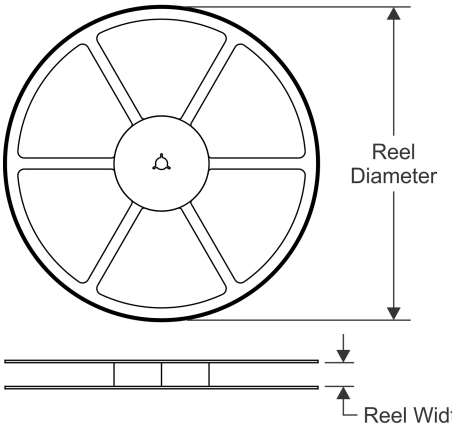
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

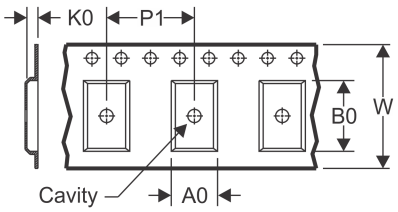
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

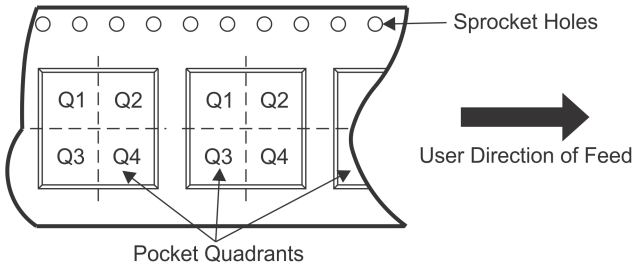


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

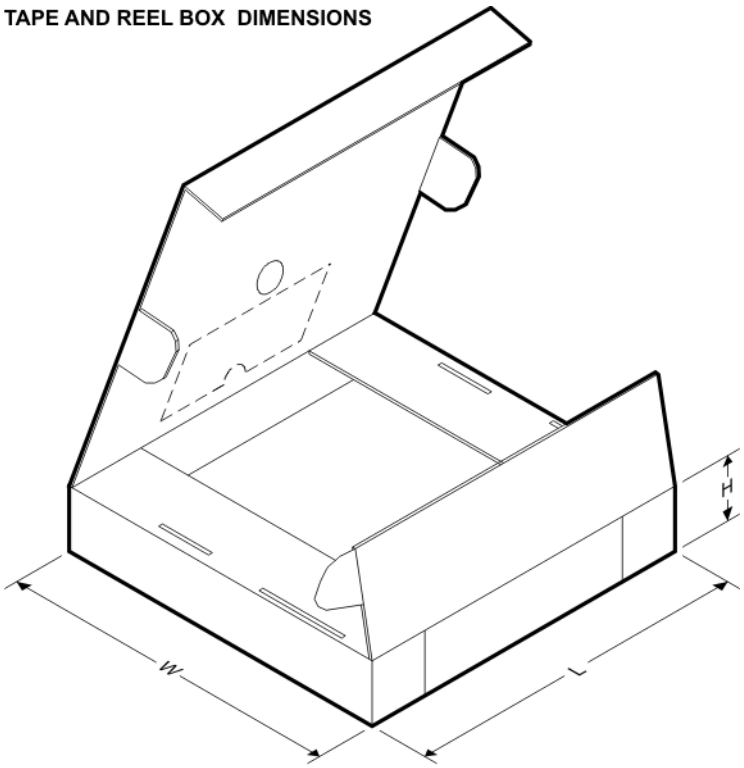
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

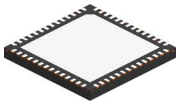
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM97937RMER	WQFN	RME	56	2000	330.0	16.4	8.3	8.3	1.3	12.0	16.0	Q1
LM97937RMET	WQFN	RME	56	250	178.0	16.4	8.3	8.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

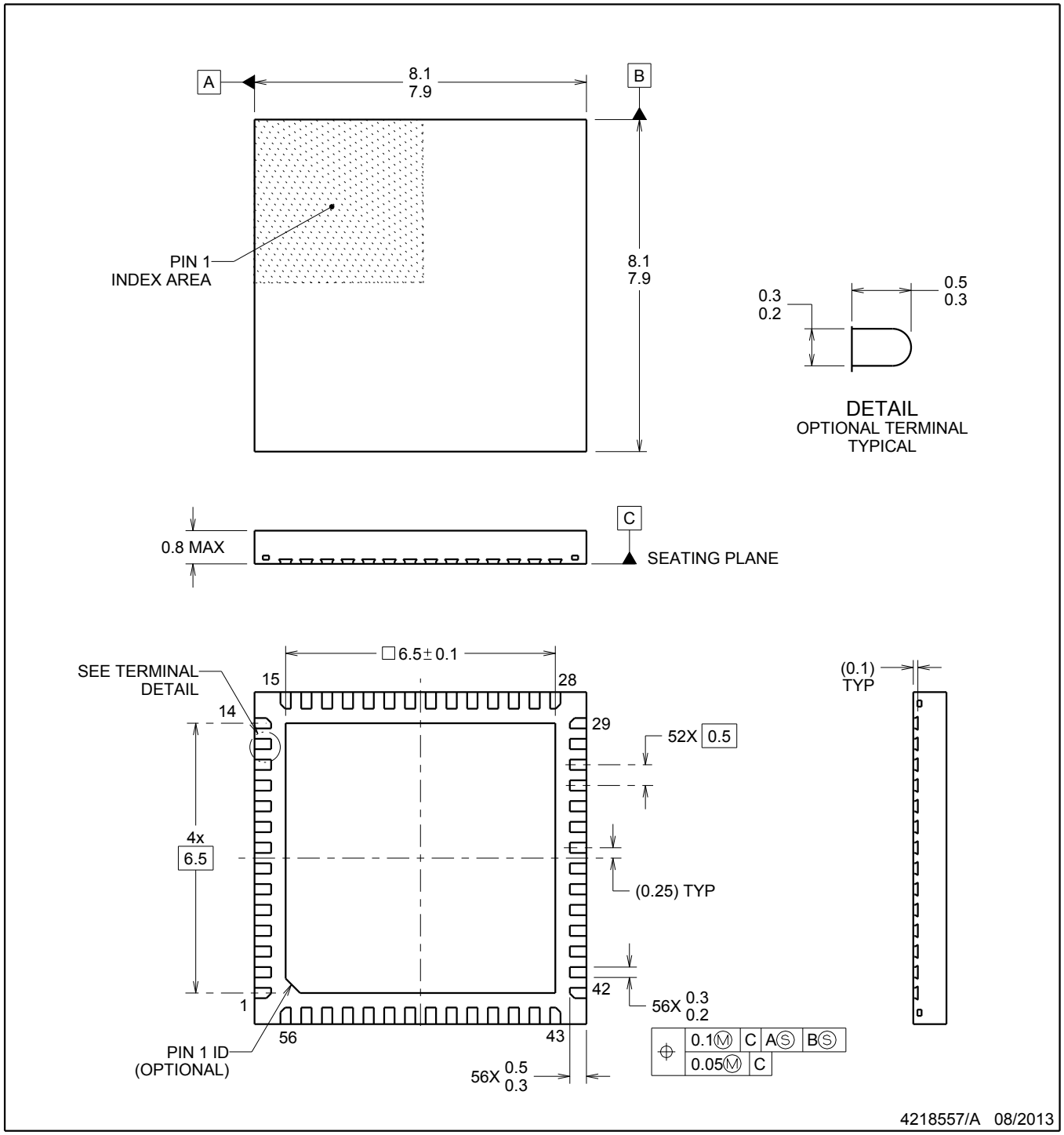
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM97937RMER	WQFN	RME	56	2000	367.0	367.0	38.0
LM97937RMET	WQFN	RME	56	250	210.0	185.0	35.0



RME0056A

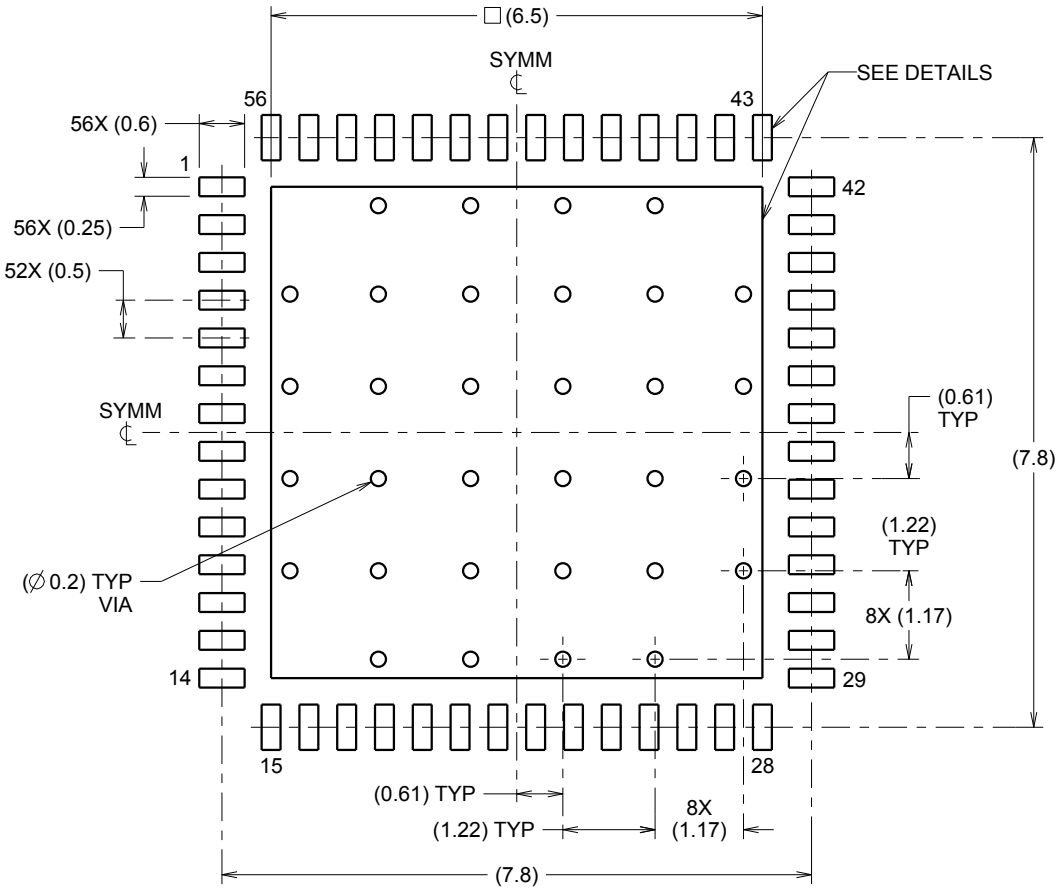
WQFN - 0.8 mm max height

WQFN

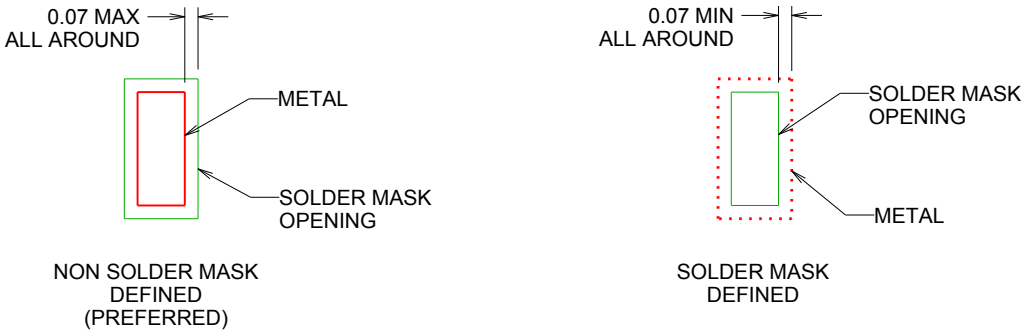


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS

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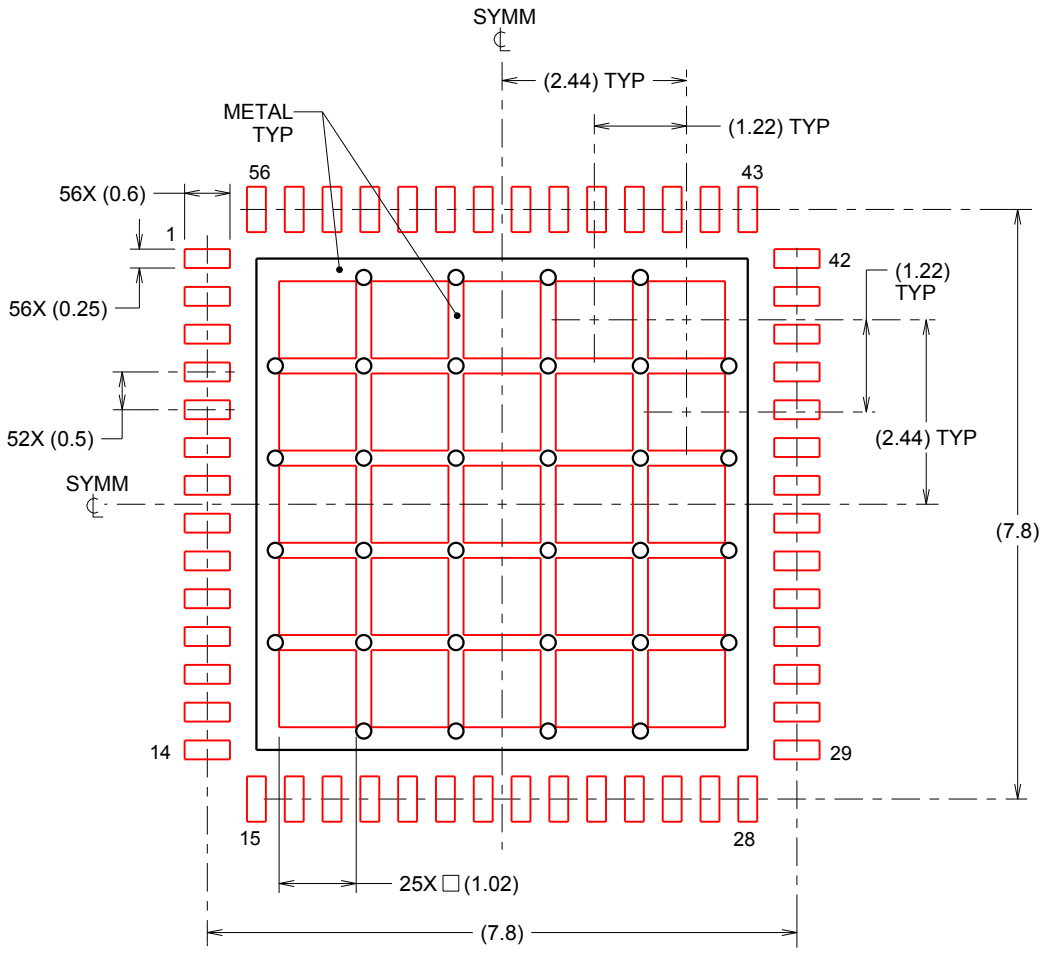
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

RME0056A

WQFN - 0.8 mm max height

WQFN



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4218557/A 08/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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