THE DATASHEET OF

UCC3802DTRG4

UCC1800, UCC1801, UCC1802, UCC1803, UCC1804, UCC1805
UCC2800, UCC2801, UCC2802, UCC2803, UCC2804, UCC2805
UCC3800, UCC3801, UCC3802, UCC3803, UCC3804, UCC3805

SLUS270E – MARCH 1999 – REVISED JUNE 2016

UCC180x, UCC280x, UCC380x Low-Power BiCMOS Current-Mode PWM Controllers

1 Features

- 100-μA Typical Starting Supply Current
- 500-μA Typical Operating Supply Current
- Operation up to 1 MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1-A Totem-Pole Output
- 70-ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UC3842 and UC3842A

2 Applications

- Switch Mode Power Supplies (SMPS)
- DC-to-DC Converters
- Power Modules
- Industrial PSU
- Battery-Operated PSU

3 Description

The UCCx80x family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching mode power supplies with minimal parts count.

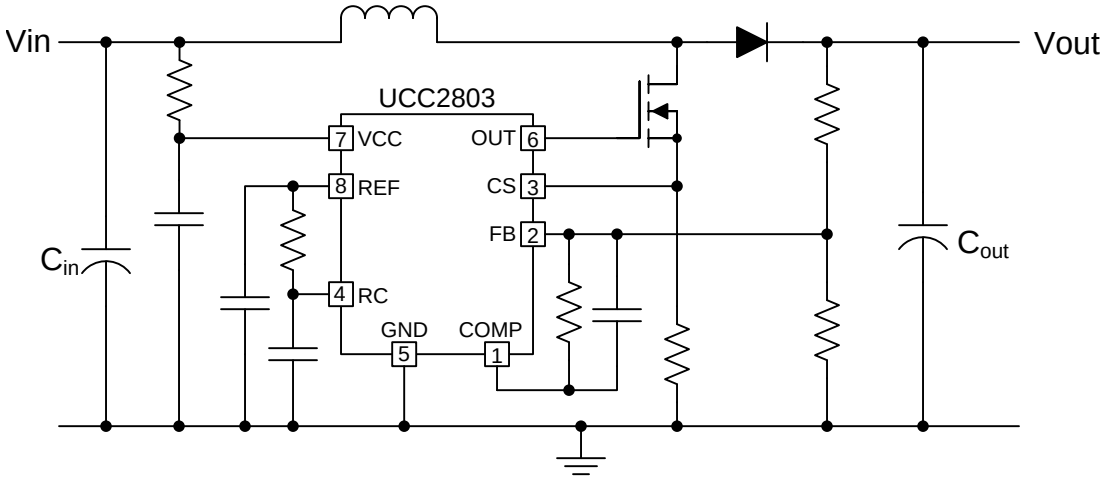
These devices have the same pin configuration as the UCx84x family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC1800	LCC (20)	8.89 mm × 8.89 mm
	CDIP (8)	6.67 mm × 9.60 mm
UCC1801, UCC1802, UCC1803, UCC1804, UCC1805	CDIP (8)	6.67 mm × 9.60 mm
UCC2800, UCC2801, UCC2802, UCC2803, UCC2804, UCC2805, UCC3800, UCC3801, UCC3802, UCC3803, UCC3804, UCC3805	TSSOP (8)	4.40 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

Changes from Revision D (August 2010) to Revision E **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (September 2000) to Revision B **Page**

- Updated Abs Max Table to read: Analog Inputs (FB, CS, RC, COMP)... –0.3V to the lesser of 6.3V or VCC + 0.3V
  From: Analog Inputs (FB, CS)... –0.3V to 6.3V ... 6

5 Description (continued)

The UCCx80x family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC2803 and UCC2805 fit best into battery-operated systems, while the higher reference and higher UVLO hysteresis of the UCC2802 and UCC2804 make these ideal choices for use in off-line power supplies.

The UCC180x series is specified for operation from –55°C to 125°C, the UCC280x series is specified for operation from –40°C to 85°C, and the UCC380x series is specified for operation from 0°C to 70°C.

6 Device Comparison Table

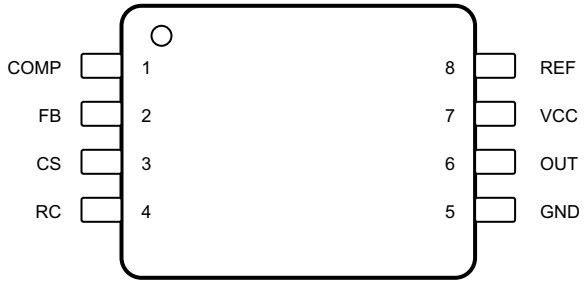
PART NUMBER	MAXIMUM DUTY CYCLE	REFERENCE VOLTAGE	TURNON THRESHOLD	TURNOFF THRESHOLD
UCCx800	100%	5 V	7.2 V	6.9 V
UCCx801	50%	5 V	9.4 V	7.4 V
UCCx802	100%	5 V	12.5 V	8.3 V
UCCx803	100%	4 V	4.1 V	3.6 V
UCCx804	50%	5 V	12.5 V	8.3 V
UCCx805	50%	4 V	4.1 V	3.6 V

Table 1. Temperature and Package Selection

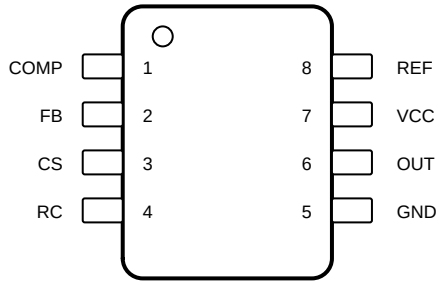
	TEMPERATURE RANGE	AVAILABLE PACKAGES
UCC180x	–55°C to 125°C	J, L
UCC280x	–40°C to 85°C	N, D, PW
UCC380x	0°C to 70°C	N, D, PW

7 Pin Configuration and Functions

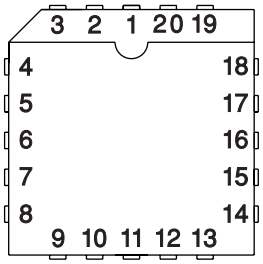
UCC280x and UCC380x PW Package
8-Pin TSSOP
Top View



UCCx80x D, J, or N Package
8-Pin SOIC, CDIP, or PDIP
Top View



UCC1800 L Package
20-Pin LCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TSSOP, SOIC, DIL	LCC		
COMP	1	2	O	COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCCx80x family is a true, low output impedance, 2-MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current-limited, so the user can command zero duty cycle by externally forcing COMP to GND. The UCCx80x family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.
CS	3	7	I	CS is the input to the current sense comparators. The UCCx80x family has two different current sense comparators: the PWM comparator and an overcurrent comparator. The UCCx80x family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100-ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay. The overcurrent comparator is only intended for fault sensing, and exceeding the overcurrent threshold causes a soft-start cycle.
FB	2	5	I	FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.
GND	5	13	—	GND is reference ground and power ground for all functions on this part.
NC	—	1, 3, 4, 6, 8, 9, 11, 14, 16, 18, 19	—	No connection pins

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	TSSOP, SOIC, DIL	LCC		
OUT	6	15	O	OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±750 mA. OUT is actively held low when VCC is below the UVLO threshold. The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to V_{CC}. The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.
PWR GND	—	12	—	Power ground of the IC
RC	4	10	I	RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions. The frequency of oscillation can be estimated with the following equations: $f = \frac{1.5}{R \times C}$ (1) $f = \frac{1.0}{R \times C}$ where • frequency is in Hz • resistance is in Ω • capacitance is in farads (2) The recommended range of timing resistors is between 10 k and 200 k, and timing capacitor is 100 pF to 1000 pF. Never use a timing resistor less than 10 k.
REF	8	20	O	REF is the voltage reference for the error amplifier, and also for many other functions on the IC. REF is also used as the logic power supply for high-speed switching logic on the IC. When VCC is greater than 1 V and less than the UVLO threshold, REF is pulled to ground through a 5-kΩ resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1-μF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5 mA on the reference. To prevent noise problems with high speed switching transients, bypass REF to ground with a ceramic capacitor very close to the IC package.
VCC	7	17	I	VCC is the power input connection for this device. In normal operation, VCC is powered through a current limiting resistor. Although quiescent VCC current is very low, total supply current is higher depending on OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from: $I_{OUT} = Q_g \times f$ (3) To prevent noise problems, bypass VCC to GND with a ceramic capacitor as close to the VCC pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. There must be a minimum of 1 μF in parallel with a 0.1-μF ceramic capacitor from VCC to ground placed close to the device.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC voltage(2)			12	V
VCC current(2)			30	mA
OUT current			±1	A
OUT energy (capacitive load)			20	µJ
Analog inputs (FB, CS, RC, COMP)		–0.3	6.3 or VCC + 0.3(3)	V
Power dissipation at T_A < 25°C	N or J package		1	W
	D package		0.65	
	L package		1.375	
Lead temperature, soldering (10 s)			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In normal operation, VCC is powered through a current-limiting resistor. Absolute maximum of 12 V applies when VCC is driven from a low impedance source, such that ICC does not exceed 30 mA (which includes the gate drive current requirement). The resistor must be sized so that the VCC voltage, under operating conditions, is below 12 V but above the turnoff threshold.
(3) Return the minimum (lesser) value of the two.

8.2 ESD Ratings

			VALUE	UNIT
D, N, OR J PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
L PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VCC}	VCC bias supply voltage from low impedance source		11	V
V_{FB}, V_{CS}, V_{RC}, V_{COMP}	Voltage on analog pins	–0.1	6 or V_{VCC}	V
V_{OUT}	Gate driver output voltage	–0.1	V_{VCC}	V
I_{VCC}	Supply bias current		25	mA
I_{OUT}	Average OUT pin current		20	mA
I_{REF}	REF pin output current		5	mA
f_{OSC}	Oscillator frequency		1	MHz
T_A	Operating free-air temperature	–55	125	°C

8.4 Thermal Information

THERMAL METRIC[1]		UCC180x, UCC280x, UCC380x				UNIT
		PW (TSSOP)	J (CDIP), D (SOIC)	N (PDIP)	L (LCC)	
		8 PINS	8 PINS	8 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	153.8	107.5	50.9	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	49.3	40.3	40.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.8	48.7	28.1	39.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	6.6	17.6	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82	48	28	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

–55°C ≤ T_A ≤ 125°C for UCC180x, –40°C ≤ T_A ≤ 85°C for UCC280x, and 0°C ≤ T_A ≤ 70°C for UCC380x. V_{CC} = 10 V[1], RT = 100 k from REF to RC, CT = 330 pF from RC to GND, 0.1-pF capacitor from V_{CC} to GND, 0.1-pF capacitor from V_{REF} to GND, and T_A= T_J (unless otherwise noted).

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T_J= 25°C, I = 0.2 mA, UCCx800, UCCx801, UCCx802, and UCCx804		4.925	5	5.075	V
	T_J= 25°C, I = 0.2 mA, UCCx803 and UCCx805		3.94	4	4.06	
Load regulation	0.2 mA < I < 5 mA	UCC180x and UCC280x		10	30	mV
		UCC380x			25	
Line regulation	T_J = 25°C, V_{CC} = 10 V to clamp (I_{VCC} = 25 mA)				1.9	mV/V
	T_J = –55°C to 125°C, V_{CC} = 10 V to clamp (I_{VCC} = 25 mA)	UCC180x and UCC280x			2.5	
		UCC380x			2.1	
Total variation	UCCx800, UCCx801, UCCx802, and UCCx804[2]		4.88	5	5.1	V
	UCCx803 and UCCx805[2]		3.9	4	4.08	
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T_J= 25°C[3]			130		µV
Long term stability	T_A = 125°C, 1000 hours[3]			5		mV
Output short circuit			–5		–35	mA
OSCILLATOR						
Oscillator frequency	UCCx800, UCCx801, UCCx802, UCCx804[4]		40	46	52	kHz
	UCCx803 and UCCx805[4]		26	31	36	
Temperature stability[3]				2.5%		
Amplitude peak-to-peak			2.25	2.4	2.55	V
Oscillator peak voltage				2.45		V
ERROR AMPLIFIER						
Input voltage	COMP = 2.5 V, UCCx800, UCCx801, UCCx802, and UCCx804		2.44	2.5	2.56	V
	COMP = 2 V, UCCx803 and UCCx805		1.95	2	2.05	
Input bias current			–1		1	µA
Open loop voltage gain			60	80		dB
COMP sink current	FB = 2.7 V, COMP = 1.1 V	UCC180x and UCC280x	0.3		3.5	mA
		UCC380x	0.4		2.5	
COMP source current	FB = 1.8 V, COMP = REF – 1.2 V		–0.2	–0.5	–0.8	mA
Gain bandwidth product[3]				2		MHz

(1) Adjust VCC above the start threshold before setting at 10 V.
(2) Total variation includes temperature stability and load regulation.
(3) Ensured by design. Not 100% tested in production.
(4) Oscillator frequency for the UCCx800, UCCx802, and UCCx803 is the output frequency. Oscillator frequency for the UCCx801, UCCx804, and UCCx805 is twice the output frequency.

Electrical Characteristics (continued)

–55°C ≤ T_A ≤ 125°C for UCC180x, –40°C ≤ T_A ≤ 85°C for UCC280x, and 0°C ≤ T_A ≤ 70°C for UCC380x. V_{CC} = 10 V(1), RT = 100 k from REF to RC, CT = 330 pF from RC to GND, 0.1-pF capacitor from V_{CC} to GND, 0.1-pF capacitor from V_{REF} to GND, and T_A= T_J (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM					
Maximum duty cycle	UCCx800, UCCx802, and UCCx803	97%	99%	100%	
	UCCx801, UCCx804, and UCCx805	48%	49%	50%	
CURRENT SENSE					
Gain(5)		1.1	1.65	1.8	V/V
Maximum input signal	COMP = 5 V(6)	0.9	1	1.1	V
Input bias current		–200		200	nA
CS blank time		50	100	150	ns
Overcurrent threshold		1.42	1.55	1.68	V
COMP to CS offset	CS = 0 V	0.45	0.9	1.35	V
OUTPUT					
OUT low level	I = 20 mA, all parts		0.1	0.4	V
	I = 200 mA, all parts		0.35	0.9	
	I = 50 mA, VCC = 5 V, UCCx803 and UCCx805		0.15	0.4	
	I = 20 mA, VCC = 0 V, all parts		0.7	1.2	
OUT high V_{SAT} (V_{CC}-OUT)	I = 20 mA, all parts		0.15	0.4	V
	I = 200 mA, all parts		1	1.9	
	I = 50 mA, VCC = 5 V, UCCx803 and UCCx805		0.4	0.9	
Rise time	C_L = 1 nF		41	70	ns
Fall time	C_L = 1 nF		44	75	ns
UNDERVOLTAGE LOCKOUT					
Start threshold(7)	UCCx800	6.6	7.2	7.8	V
	UCCx801	8.6	9.4	10.2	
	UCCx802 and UCCx804	11.5	12.5	13.5	
	UCCx803 and UCCx805	3.7	4.1	4.5	
Stop threshold(7)	UCCx1800	6.3	6.9	7.5	V
	UCCx1801	6.8	7.4	8	
	UCCx802 and UCCx804	7.6	8.3	9	
	UCCx803 and UCCx805	3.2	3.6	4	
Start to stop hysteresis	UCCx800	0.12	0.3	0.48	V
	UCCx801	1.6	2	2.4	
	UCCx802 and UCCx804	3.5	4.2	5.1	
	UCCx803 and UCCx805	0.2	0.5	0.8	
SOFT START					
COMP rise time	FB = 1.8 V, rise from 0.5 V to REF – 1 V		4	10	ms
OVERALL					
Start-up current	V_{CC} < start threshold		0.1	0.2	mA
Operating supply current	FB = 0 V, CS = 0 V		0.5	1	mA
VCC internal Zener voltage	I_{CC} = 10 mA(7)(8)	12	13.5	15	V
VCC internal Zener voltage minus start threshold voltage	UCCx802 and UCCx804(7)	0.5	1		V

(5) Gain is defined by: A = ΔV_{COMP} / Δ V_{CS}. 0 ≤ V_{CS} ≤ 0.8 V
(6) Parameter measured at trip point of latch with Pin 2 at 0 V.
(7) Start threshold, stop threshold, and Zener shunt thresholds track one another.
(8) The device is fully operating in clamp mode, as the forcing current is higher than the normal operating supply current.

8.6 Typical Characteristics

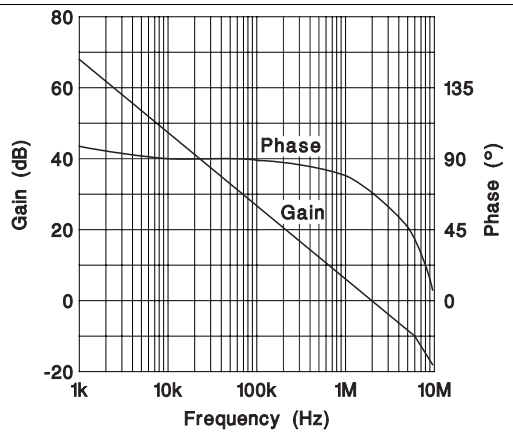


Figure 1. Error Amplifier Gain and Phase Response

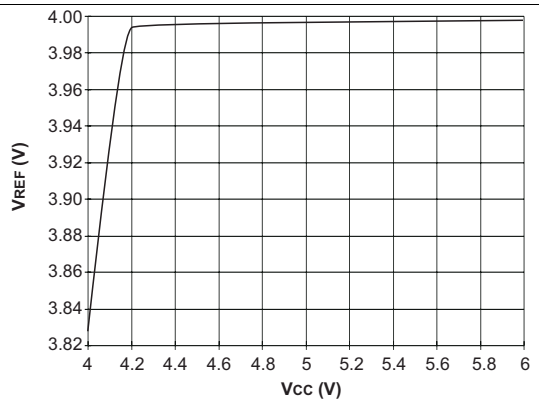


Figure 2. UCC1803 and UCC1805 V_{REF} vs V_{CC}, I_{LOAD} = 0.5 mA

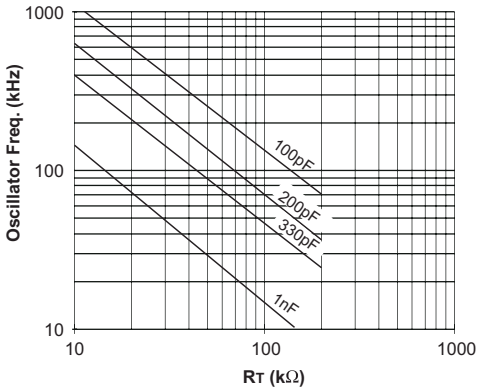


Figure 3. UCC1800, UCC1801, UCC1802, and UCC1804 Oscillator Frequency vs R_T and C_T

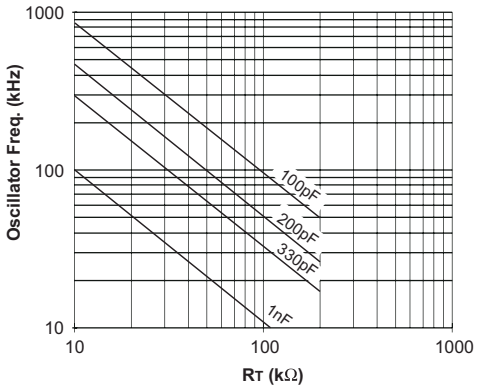


Figure 4. UCC1803 and UCC1805 Oscillator Frequency vs R_T and C_T

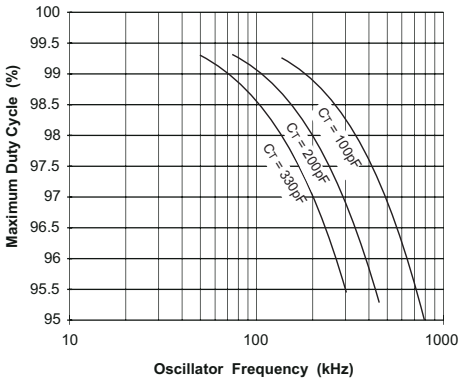


Figure 5. UCC1800, UCC1802, and UCC1803 Maximum Duty Cycle vs Oscillator Frequency

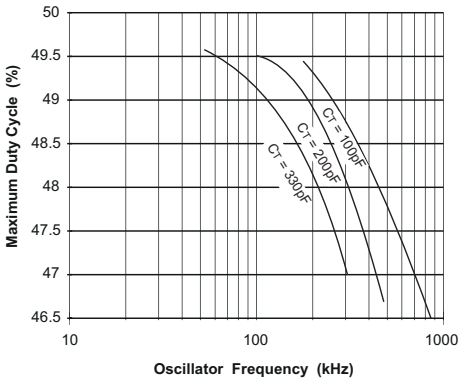


Figure 6. UCC1801, UCC1804, and UCC1805 Maximum Duty Cycle vs Oscillator Frequency

Typical Characteristics (continued)

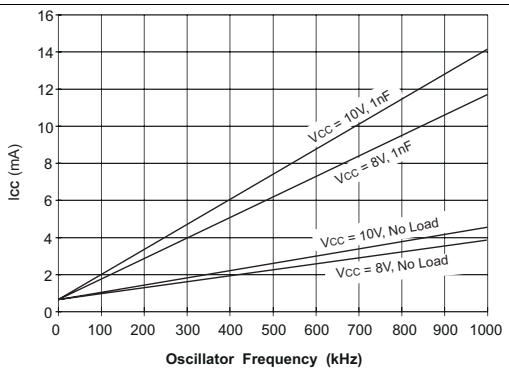


Figure 7. UCC1800 I_{CC} vs Oscillator Frequency

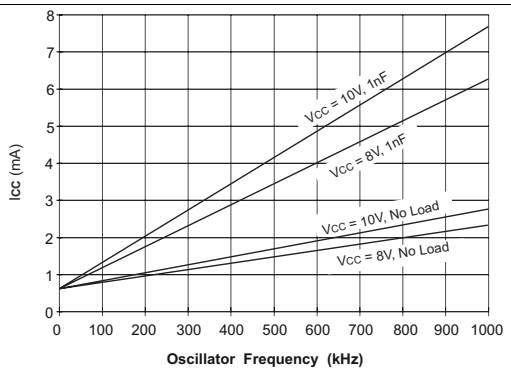


Figure 8. UCC1805 I_{CC} vs Oscillator Frequency

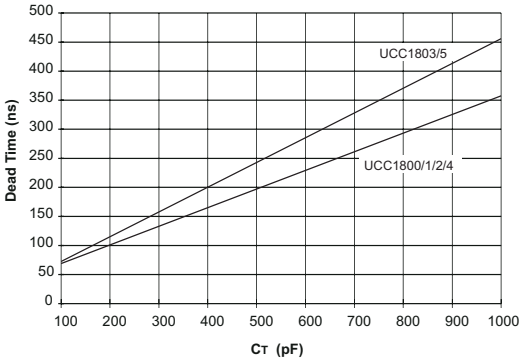


Figure 9. Dead Time vs C_T, R_T = 100 k

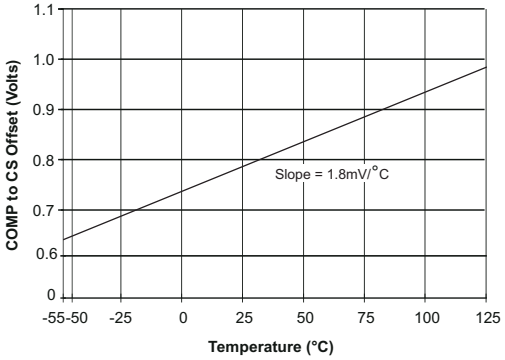


Figure 10. COMP to CS Offset vs Temperature, CS = 0 V

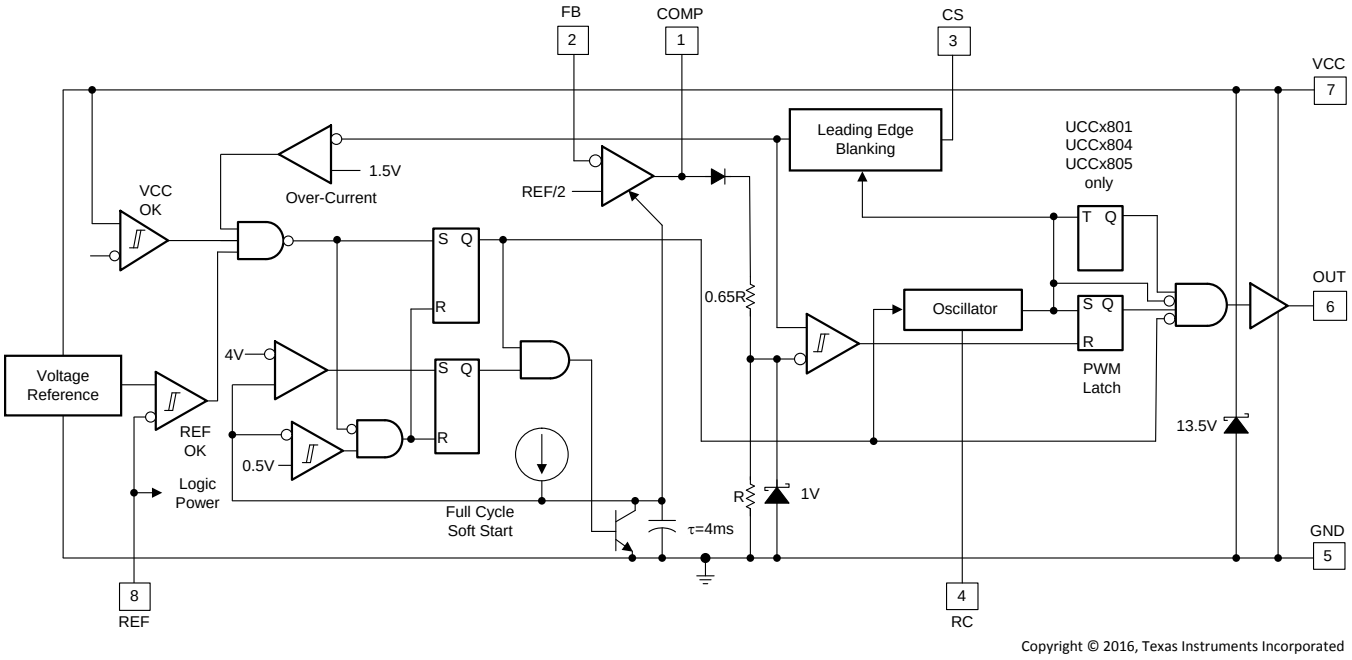
9 Detailed Description

9.1 Overview

The UCCx80x family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed-frequency, current-mode switching mode power supplies with minimal parts count.

These devices have the same pin configuration as the UCx84x family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

9.2 Functional Block Diagram



9.3 Feature Description

The UCCx80x family offers numerous advantages that allow the power supply design engineer to meet these challenging requirements.

Features include:

- Bi-CMOS process
- Low starting supply current: typically 100 μA
- Low operating supply current: typically 500 μA
- Pinout compatible with UC3842 and UC3842A families
- 5-V operation (UCCx803 and UCCx805)
- Leading edge blanking of current sense signal
- On-chip soft start
- Internal full cycle restart delay
- 1.5% voltage reference
- Up to 1-MHz oscillator
- Low self-biasing output during UVLO
- Very few external components required
- 70-ns response from current sense to output
- Available in surface-mount or PDIP package

Feature Description (continued)

The UCCx80x family of devices are pinout compatible with the UCx84x and UCx84xA families. However, they are not plug-in compatible. In general, the UCCx80x requires fewer external components and consumes less operating current.

9.3.1 Detailed Pin Description

9.3.1.1 COMP

Unlike other devices, the error amplifier in the UCCx80x family is a true, low output impedance, 2-MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current-limited, so that one can command zero duty cycle by externally forcing COMP to GND.

The UCCx80x has a true low output impedance error amplifier which both sources and sinks current. The error amplifier associated with the UC3842 family is an open collector in parallel with a current source.

The UCCx80x has power-up soft start and fault soft start built on-chip with a fixed COMP rise time to 5 V in 4 ms. Therefore, no external soft-start circuitry is required, saving 1 resistor, 1 capacitor, and 1 PNP transistor.

9.3.1.2 FB

FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

The UCCx80x features a 2-MHz bandwidth error amplifier versus 1 MHz on the UC3842 family. Feedback techniques are identical to the UC3842 family.

9.3.1.3 CS

CS is the PWM comparator and an overcurrent comparator. The UCCx80x family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100-ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero on-time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay. The overcurrent comparator is only intended for fault sensing, and exceeding the overcurrent threshold causes a soft-start cycle.

The UCCx80x current sense is significantly different from its predecessor. The UC3842 family current sense input connects to only the PWM comparator. The UCCx80x current sense input connects to two comparators: the PWM comparator and the overcurrent comparator. Internal leading edge blanking masks the first 100 ns of the current sense signal. This may eliminate the requirement for an RC current sense filter and prevent false triggering due to leading edge noises. Connect CS directly to MOSFET source current sense resistor. The gain of the current sense amplifier on the UCCx80x family is typically 1.65 V/V versus typically 3 V/V with the UC3842 family.

9.3.1.4 RC

RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting timing capacitor from RC to GND. For the best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The UCCx80x's oscillator allows for operation to 1 MHz versus 500 kHz with the UC3842 family. Both devices make use of an external resistor to set the charging current for the capacitor, which determines the oscillator frequency. For the UCCx802 and UCCx804, use Equation 4.

$$f = \frac{1.5}{R \times C} \tag{4}$$

For the UCCx803 and UCCx805, use Equation 5.

$$f = \frac{1.0}{R \times C} \tag{5}$$

Feature Description (continued)

In these two equations, switching frequency (f) is in Hz, R is in Ω, and C is in farads.

The two equations are different due to different reference voltages. The recommended range of timing resistor values is between 10 kΩ and 200 kΩ; the recommended range of timing capacitor values is between 100 pF and 1000 pF. The peak-to-peak amplitude of the oscillator waveform is 2.45 V versus 1.7 V in UC3842 family. For best performance, keep the timing capacitor lead to GND as short as possible. TI recommends separate ground traces for the timing capacitor and all other pins. The maximum duty cycle for the UCCx802 and UCCx803 is approximately 99%; the maximum duty cycle for the UCCx803 and UCCx804 is approximately 49%. The duty cycle cannot be easily modified by adjusting R_T and C_T, unlike the UC3842A family. The maximum duty cycle limit is set by the ratio of the external oscillator charging resistor R_T and the internal oscillator discharge transistor on-resistance, like the UC3842. However, maximum duty cycle limits less than 90% (for the UCCx802 and UCCx803) and less than 45% (for the UCCx804 and UCCx805) can not reliably be set in this manner. For better control of maximum duty cycle, consider using the UCCx807.

9.3.1.5 GND

GND pin is the signal and power returning ground. TI recommends separating the signal return path and the high current gate driver path so that the signal is not affected by the switching current.

9.3.1.6 OUT

OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding 750 mA. OUT is actively held low when VCC is below the UVLO threshold. The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to VCC. The output stage also provides a low impedance to overshoot and undershoot. This means that in many cases, external Schottky clamp diodes are not required.

The output of the UCCx80x is a CMOS output versus a Bipolar output on the UC3842 family. Peak output current remains the same ±1 A. The CMOS output provides very smooth rising and falling waveforms, with virtually no overshoot or undershoot. Additionally, the CMOS output provides a low resistance to the supply in response to overshoot, and a low resistance to ground in response to undershoot. Because of this, Schottky diodes may not be necessary on the output. Furthermore, the UCCx802 has a self-biasing, active low output during UVLO. This feature eliminates the gate to source *bleeder* resistor associated with the MOSFET gate drive. Finally, no MOSFET gate voltage clamp is necessary with the UCCx80x as the on-chip Zener diode automatically clamps the output to VCC.

9.3.1.7 VCC

VCC is the power input connection for this device. In normal operation, VCC is powered through a current limiting resistor. Although quiescent VCC current is very low, total supply current is higher, depending on the OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from Equation 6.

$$I_{OUT} = Q_g \times f \tag{6}$$

The UCCx80x has a lower VCC (supply voltage) clamp of 13.5 V typical versus 30 V on the UC3842. For applications that require a higher VCC voltage, a resistor must be placed in series with VCC to increase the source impedance. The maximum value of this resistor is calculated with Equation 7.

$$R_{max} = \frac{V_{IN(min)} - V_{VCC(max)}}{I_{VCC} + Q_g \times f} \tag{7}$$

In Equation 7, V_{IN}(min) is the minimum voltage that is used to supply VCC, V_{VCC}(max) is the maximum VCC clamp voltage and I_{VCC} is the IC supply current without considering the gate driver current and Q_g is the external power MOSFET gate charge and f is the switching frequency.

Additionally, the UCCx80x has an on-chip Zener diode to regulate VCC to 13.5 V. The turnon and turnoff thresholds for the UCCx80x family are significantly different: 12.5 V and 8 V for the UCCx802 and UCCx804; 4.1 V and 3.6 V for the UCCx803 and UCCx805. 5-V PWM operation is now possible. To ensure against noise related problems, filter VCC with an electrolytic and bypass with a ceramic capacitor to ground. Keep the capacitors close to the IC pins.

Feature Description (continued)

9.3.1.8 Pin 8 (REF)

REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high-speed switching logic on the IC. When VCC is greater than 1 V and less than the UVLO threshold, REF is pulled to ground through a 5-kΩ resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1-μF ceramic capacitor is required. Additional REF bypassing is required for external loads greater than 2.5 mA on the reference. To prevent noise problems with high-speed switching transients, bypass REF to ground with a ceramic capacitor close to the IC package.

The UCCx802 and UCCx804 have a 5-V reference. The UCCx803 and UCCx805 have a 4-V reference; both ±1.5% versus ±2% on the UC3842 family. The output short-circuit current is lower 5 mA versus 30 mA. REF must be bypassed to ground with a ceramic capacitor to prevent oscillation and noise problems. REF can be used as a logic output; as when VCC is lower than the UVLO threshold, REF is held low.

9.3.2 Undervoltage Lockout (UVLO)

The UCC380x devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Both the supply voltage (VCC) and the reference voltage (Vref) are monitored by the UVLO circuitry. An active low, self-biasing totem pole output during UVLO design is also incorporated for enhanced power switch protection.

Undervoltage lockout thresholds for the UCCx802, UCCx803, UCCx804, and UCCx805 devices are different from the previous generation of UCx842, UCx843, UCx844, and UCx845 PWMs. Basically, the thresholds are optimized for two groups of applications: off-line power supplies and DC-DC converters.

The UCCx802 and UCCx804 feature typical UVLO thresholds of 12.5 V for turnon and 8.3 V for turnoff, providing 4.3 V of hysteresis.

For low voltage inputs, which include battery and 5-V applications, the UCCx803 and UCCx805 turn on at 4.1 V and turn off at 3.6 V with 0.5 V of hysteresis.

The UCCx800 and UCCx801 have UVLO thresholds optimized for automotive and battery applications.

During UVLO the IC draws approximately 100 μA of supply current. Once crossing the turnon threshold the IC supply current increases typically to about 500 μA, over an order of magnitude lower than bipolar counterparts.

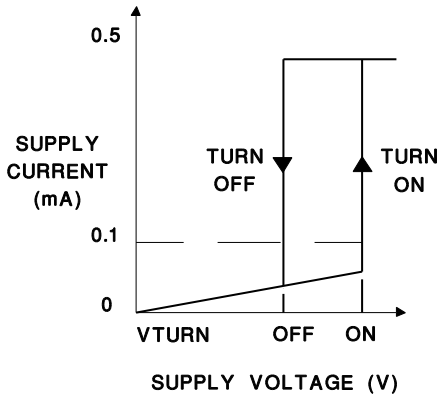


Figure 11. IC Supply Current at UVLO

Table 2. UVLO Level Comparison Table

DEVICE	Vton (V)	Vtoff (V)
UCCx800	7.2	6.9
UCCx801	9.4	7.4
UCCx802, UCCx804	12.5	8.3
UCCx803, UCCx805	4.1	3.6

9.3.3 Self-Biasing, Active Low Output

The self-biasing, active low clamp circuit shown in Figure 12 eliminates the potential for problematic MOSFET turnon. As the PWM output voltage rises while in UVLO, the P device drives the larger N type switch ON, which clamps the output voltage low. Power to this circuit is supplied by the externally rising gate voltage, so full protection is available regardless of the ICs supply voltage during undervoltage lockout.

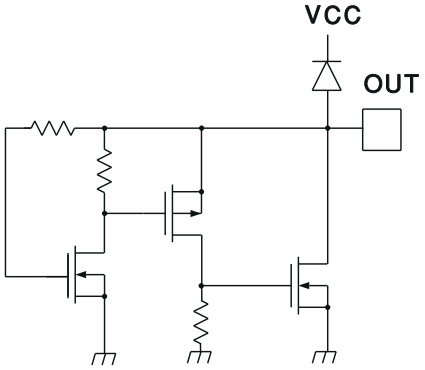


Figure 12. Internal Circuit Holding OUT Low During UVLO

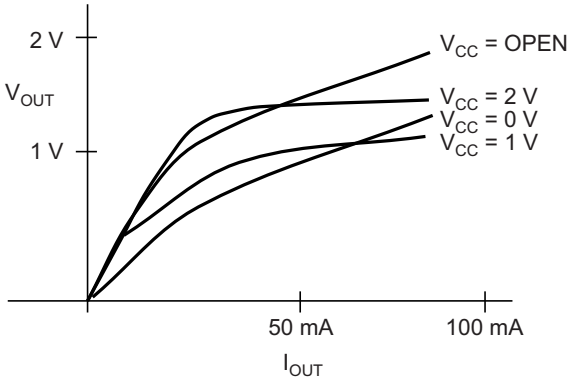


Figure 13. OUT Voltage vs OUT Current During UVLO

9.3.4 Reference Voltage

The traditional 5-V amplitude bandgap reference voltage of the UC3842 family can be also found on the UCCx800, UCCx801, UCCx802, and UCCx804 devices. However, the reference voltage of the UCCx803 and UCCx805 device is 4 V. This change was necessary to facilitate operation with input supply voltages below 5 V. Many of the reference voltage specifications are similar to the UC3842 devices although the test conditions have been changed, indicative of lower-current PWM applications. Similar to their bipolar counterparts, the BiCMOS devices internally pull the reference voltage low during UVLO, which can be used as a UVLO status indication.

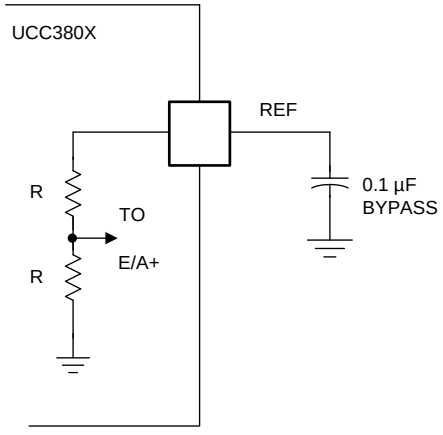


Figure 14. Required Reference Bypass

Note that the 4-V reference voltage on the UCCx803 and UCCx805 is derived from the supply voltage (VCC) and requires about 0.5 V of headroom to maintain regulation. Whenever Vcc is below approximately 4.5 V, the reference voltage also drops outside of its specified range for normal operation. The relationship between VCC and V_{REF} during this excursion is shown in Figure 15.

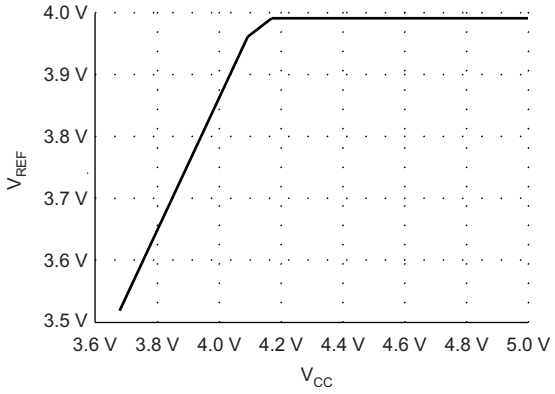


Figure 15. UCC3803 REF Output vs V_{VCC}

The noninverting input to the error amplifier is tied to half of the PWM's reference voltage, V_{REF}. Note that this input is 2 V on the UCC3803 and UCC3805 and 2.5 V on the higher reference voltage parts: the UCC3800, UCC3801, UCC3802, and UCC3804.

9.3.5 Oscillator

The UCC380x oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of R_T and C_T. The fall time is set by C_T and an internal transistor on-resistance of approximately 130 Ω. During the fall time, the output is OFF and the maximum duty cycle is reduced below 50% or 100%, depending on the part number. Larger timing capacitors increase the discharge time and reduce the maximum duty cycle and frequency.

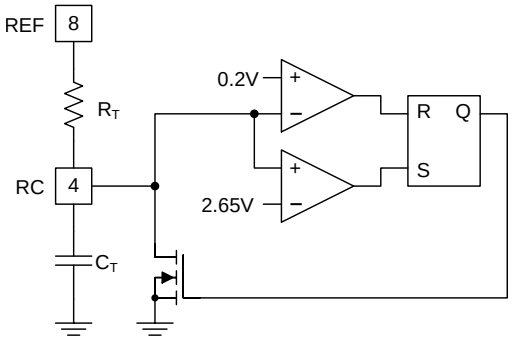


Figure 16. Oscillator Equivalent Circuit

The oscillator section of the UCCx800 through UCCx805 BiCMOS devices has few similarities to the UC3842 type — other than single pin programming. It does still use a resistor to the reference voltage and capacitor to ground to program the oscillator frequency up to 1 MHz. Timing component values must be changed because a much lower charging current is desirable for low-power operation. Several characteristics of the oscillator have been optimized for high-speed, noise-immune operation. The oscillator peak-to-peak amplitude has been increased to 2.45 V typical versus 1.7 V on the UC3842 family. The lower oscillator threshold has been dropped to approximately 0.2 V while the upper threshold remains fairly close to the original 2.8 V at approximately 2.65 V.

Discharge current of the timing capacitor has been increased to nearly 20-mA peak as opposed to roughly 8 mA. This can be represented by approximately 130 Ω in series with the discharge switch to ground. A higher current was necessary to achieve brief dead times and high duty cycles with high-frequency operation. Practical applications can use these new ICs to a 1-MHz switching frequency.

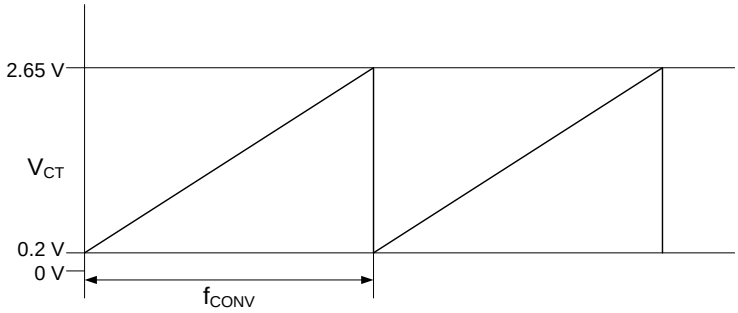


Figure 17. Oscillator Waveform

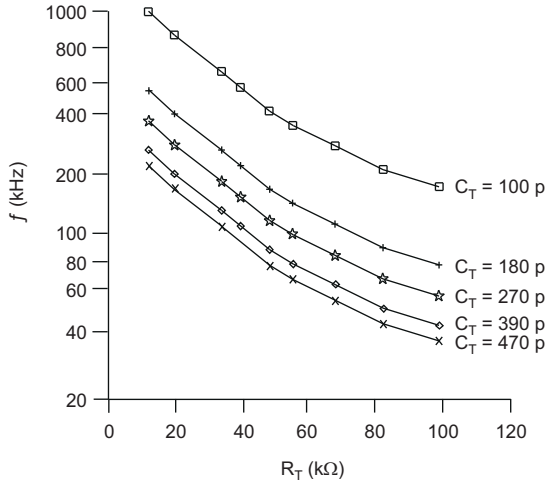


Figure 18. Oscillator Frequency vs R_T For Several C_T

9.3.6 Synchronization

Synchronization of these PWM controllers is best obtained by the universal technique shown in Figure 19. The ICs oscillator is programmed to free run at a frequency about 20% lower than that of the synchronizing frequency. A brief positive pulse is applied across the 50-Ω resistor to force synchronization. Typically, a 1-V amplitude pulse of 100-ns width is sufficient for most applications.

The ICs can also be synchronized to a pulse train input directly to the oscillator RC pin. Note that the IC internally pulls low at this node once the upper oscillator threshold is crossed. This 130-Ω impedance to ground remains active until the pin is lowered to approximately 0.2 V. External synchronization circuits must accommodate these conditions.

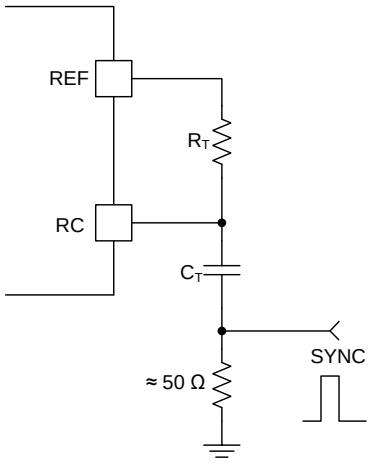


Figure 19. Synchronizing the Oscillator

9.3.7 PWM Generator

Maximum duty cycle is higher for these devices than for their UC3842, UC3843, UC3844, and UC3845 predecessors. This is primarily due to the higher ratio of timing capacitor discharge to charge current, which can exceed one hundred to one in a typical BiCMOS application. Attempts to program the oscillator maximum duty cycle much below the specified range by adjusting the timing component values of R_T and C_T must be avoided. There are two reasons to stay away from this design practice. First, the ICs high discharge current would necessitate higher charging currents than necessary for programming, defeating the purpose of low power operation. Secondly, a low-value timing resistor prevents the capacitor from discharging to the lower threshold and initiating the next switching cycle.

9.3.8 Minimum Off-Time Setting (Dead-Time Control)

Dead time is the term used to describe the ensured OFF time of the PWM output during each oscillator cycle. It is used to ensure that even at maximum duty cycle, there is enough time to reset the magnetic circuit elements, and prevent saturation. The dead time of the UCCx80x PWM family is determined by the internal 130-Ω discharge impedance and the timing capacitor value. Larger capacitance values extend the dead time whereas smaller values results in higher maximum duty cycles for the same operating frequency. A curve for dead time versus timing capacitor values is provided in Figure 20. Increasing the dead time is possible by adding a resistor between the RC pin of the IC and the timing components, as shown in Figure 21. The dead time increases with the discharge resistor value to about 470 Ω as indicated from the curve in Figure 22. Higher resistances must be avoided as they can decrease the dead time and reduce the oscillator peak-to-peak amplitude. Sinking too much current (1 mA) by reducing R_T will *freeze* the oscillator OFF by preventing discharge to the lower comparator threshold voltage of 0.2 V. Adding this discharge control resistor has several impacts on the oscillator programming. First, it introduces a DC offset to the capacitor during the discharge – but not the charging portion of the timing cycle, thus lowering the usable peak-to-peak timing capacitor amplitude. Because of the reduced peak-to-peak amplitude, the exact value of C_T may require adjustment from UC3842 type designs to obtain the correct initial oscillator frequency. One alternative is keep the same value timing capacitor and adjust both the timing and discharge resistor values because these are readily available in finer numerical increments.

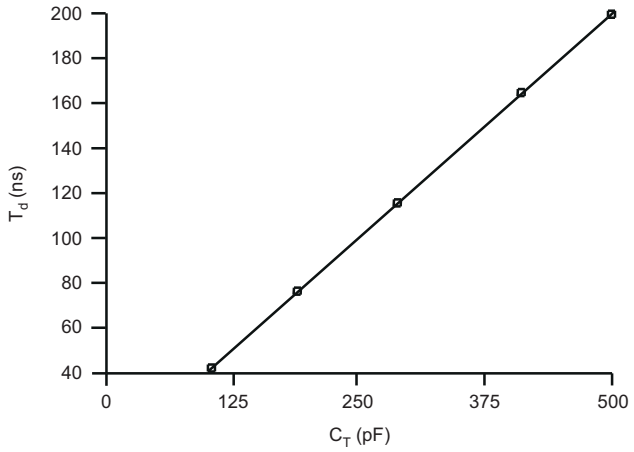


Figure 20. Minimum Dead Time vs C_T

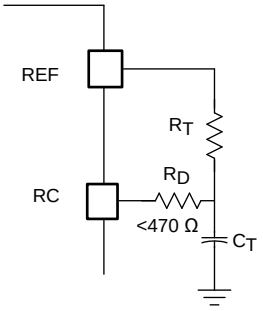


Figure 21. Circuit to Produce Controlled Maximum Duty Cycle

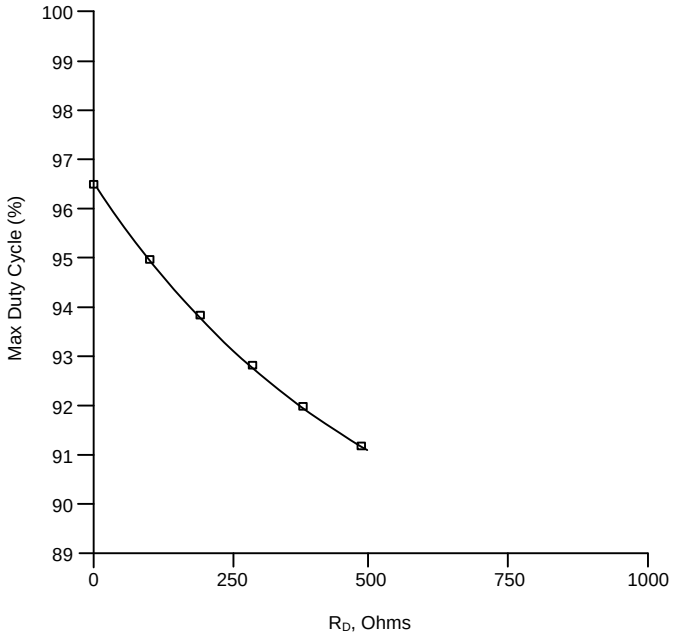


Figure 22. Maximum Duty Cycle vs R_D for R_T = 20 kΩ

9.3.9 Leading Edge Blanking

A 100-ns leading edge blanking interval is applied to the current sense input circuitry of the UCCx80x devices. This internal feature has been incorporated to eliminate the requirement for an external resistor-capacitor filter network to suppress the switching spike associated with turnon of the power MOSFET. This 100-ns period must be adequate for most switch-mode designs but can be lengthened by adding an external R/C filter. Note that the 100-ns leading edge blanking is also applied to the cycle-by-cycle current limiting function in addition to the overcurrent fault comparator.

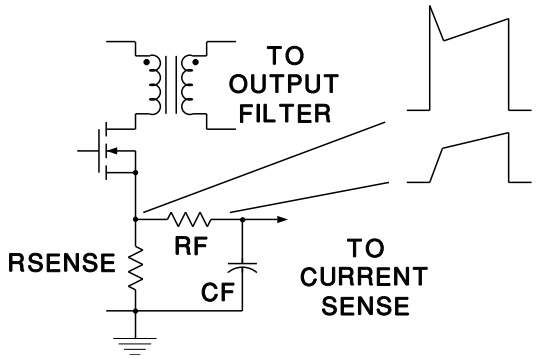


Figure 23. Current Sense Filter Required With Older PWM ICs

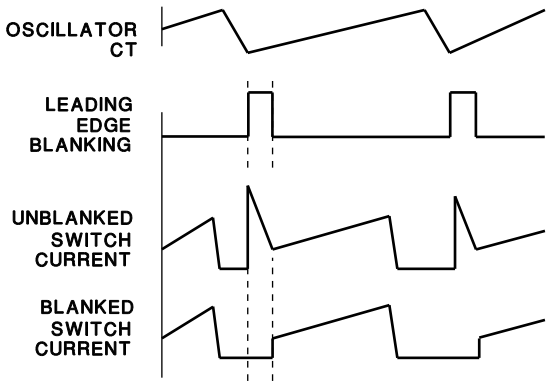


Figure 24. Current Sense Waveforms With Leading Edge Blanking

9.3.10 Minimum Pulse Width

The leading edge blanking circuitry can lead to a minimum pulse width equal to the blanking interval under certain conditions. This occurs when the error amplifier output voltage (minus a diode drop and divided by 1.65) is lower than the current sense input. However, the amplifier output voltage must also be higher than a diode forward voltage drop of about 0.5 V. It is only during these conditions that a minimum output pulse width equal to the blanking duration can be obtained. Note that the PWM comparator has two inputs; one is from the current sense input. The other PWM input is the error amplifier output that has a diode and two resistors in series to ground. The diode in this network is used to ensure that zero duty cycle can be reached. Whenever the E/A output falls below a diode forward voltage drop, no current flows in the resistor divider and the PWM input goes to zero, along with pulse width.

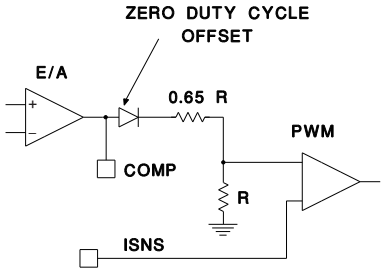


Figure 25. Zero Duty Cycle Offset

9.3.11 Current Limiting

A 1-V (typical) cycle-by-cycle current limit threshold is incorporated into the UCCx80x family. Note that the 100-ns leading edge blanking pulse is applied to this current limiting circuitry. The blanking overrides the current limit comparator output to prevent the leading edge switch noise from triggering a current limit function. Propagation delay from the current limit comparator to the output is typically 70 ns. This high-speed path minimizes power semiconductor dissipation during an overload by abbreviating the ON time.

For increased efficiency in the current sense circuitry, the circuit shown in Figure 26 can be used. Resistors R_A and R_B bias the actual current sense resistor voltage up, allowing a small current sense amplitude to be used. This circuitry provides current limiting protection with lower power loss current sensing.

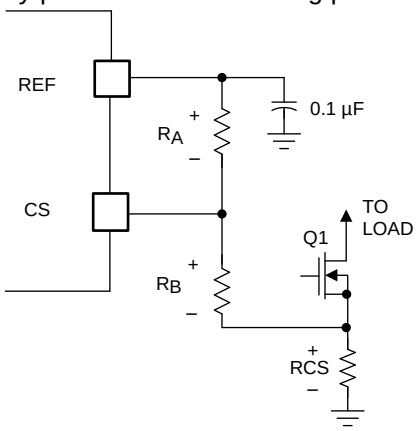


Figure 26. Biasing CS For Lower Current Sense Voltage

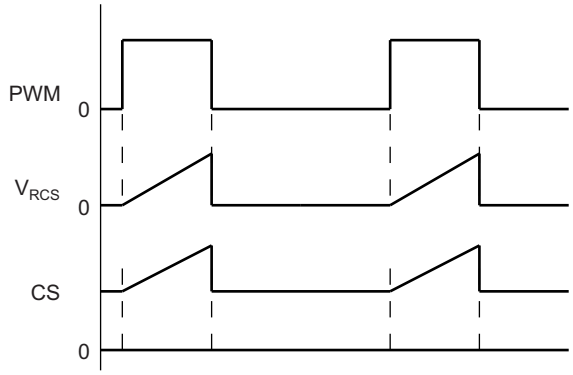


Figure 27. CS Pin Voltage with Biasing

The example shown uses a 200-mV full scale signal at the current sense resistor. Resistor R_B biases this up by approximately 700 mV to mate with the 0.9-V minimum specification of the current limit comparator of the IC. The value of resistor R_A changes with the specific IC used, due to the different reference voltages. The resistor values must be selected for minimal power loss. For example, a 50-µA bias sets R_B = 13 kΩ, R_A = 75 kΩ (UCCx800, UCCx801, UCCx802, and UCCx804), or R_A = 56 kΩ with the UCCx803 and UCCx805 devices.

9.3.12 Overcurrent Protection and Full Cycle Restart

A separate overcurrent comparator within the UCCx80x devices handle operation into a short-circuited or severely overloaded power supply output. This overcurrent comparator has a 1.5-V threshold and is also gated by the leading edge blanking signal to prevent false triggering. Once triggered, the overcurrent comparator uses the internal soft-start capacitor to generate a delay before retry is attempted. Often referred to as *hiccup*, this delay time is used to significantly reduce the input and dissipated power of the main converter and switching components. Full Cycle Soft Start ensures that there is a predictable delay of greater than 3 ms between successive attempts to operate during fault. The circuit shown in Figure 28 and the timing diagram in Figure 29 show how the IC responds to a severe fault, such as a saturated inductor. When the fault is first detected, the internal soft-start capacitor instantly discharges and stays discharged until the fault clears. At the same time, the PWM output is turned off and held off. When the fault clears, the capacitor slowly charges and allows the error

amp output (COMP) to rise. When COMP gets high enough to enable the output, another fault occurs, latching off the PWM output, but the soft-start capacitor still continues to rise to 4 V before being discharged and permitting start of a new cycle. This means that for a severe fault, successive retries is spaced by the time required to fully charge the soft-start capacitor. TI recommends low leakage transformer designs in high-frequency applications to activate the overcurrent protection feature. Otherwise, the switch current may not ramp up sufficiently to trigger the overcurrent comparator within the leading edge blanking duration. This condition would cause continual cyclical triggering of the cycle-by-cycle current limit comparator but not the overcurrent comparator. This would result in brief high power dissipation durations in the main converter at the switching frequency. The intent of the overcurrent comparator is to reduce the effective retry rate under these conditions to a few milliseconds, thus significantly lowering the short-circuit power dissipation of the converter.

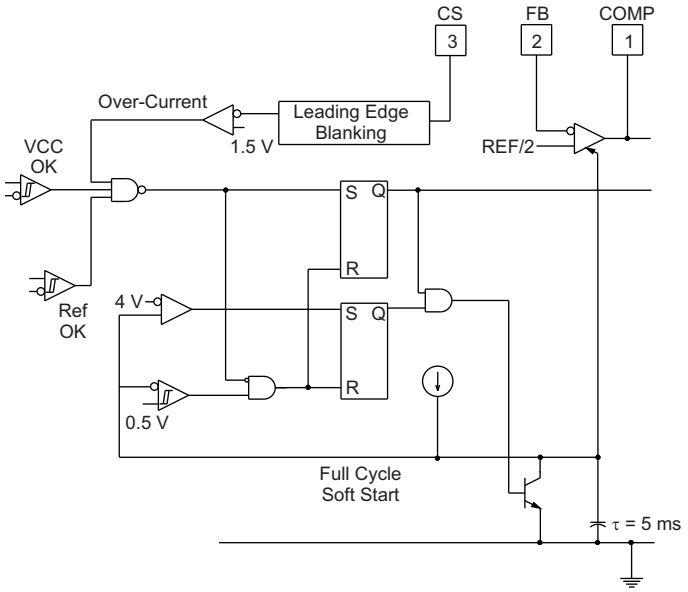


Figure 28. Detailed Block Diagram for Overcurrent Protection

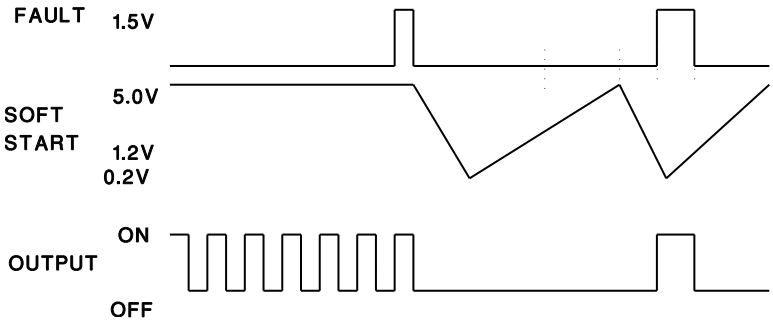


Figure 29. IC Behavior at Repetitive Fault

9.3.13 Soft Start

Internal soft starting of the PWM output is accomplished by gradually increasing error amplifier (E/A) output voltage. When used in current mode control, this implementation slowly raises the peak switch current each PWM cycle in comparison, forcing a controlled start-up. In voltage mode (duty cycle) control, this feature continually widens the pulse width.

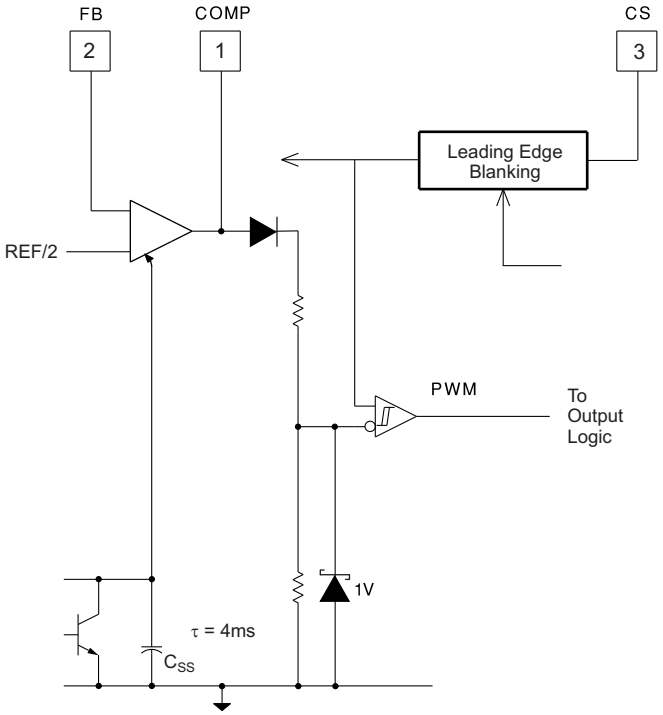


Figure 30. Detailed Block Diagram for Soft-Start

The internal soft-start capacitor (Css) is discharged following an undervoltage lockout transition or if the reference voltage is below a minimum value for normal operation. Additionally, discharge of Css occurs whenever the overcurrent protection comparator is triggered by a fault. Soft start is performed within the UCCx800, UCCx801, UCCx802, UCCx803, UCCx804, and UCCx805 devices by clamping the E/A amplifier output to an internal soft-start capacitor (Css), which is charged by a current source. The soft-start clamp circuitry is overridden once Css charges above the voltage commanded by the error amplifier for normal PWM operation.

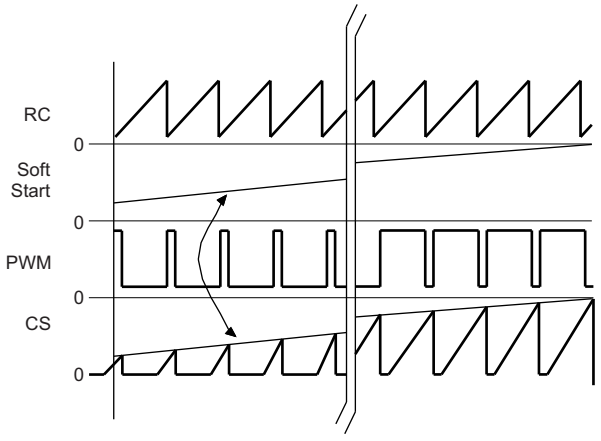


Figure 31. IC Soft-Start Behavior

9.3.14 Slope Compensation

Slope compensation can be added in all current mode control applications to cancel the peak to average current error. Slope compensation is necessary with applications with duty cycles exceeding 50%, but also improves performance in those below 50%. Primary current is sensed using resistor Rcs in series with the converter switch. The timing resistor can be broken up into two series resistors to bias up the NPN follower. This is required to provide ample compliance for slope compensation at the beginning of a switching cycle, especially with continuous current converters. A NPN voltage follower drives the slope compensating programming resistor (Rsc) to provide a slope compensating current into C_F.

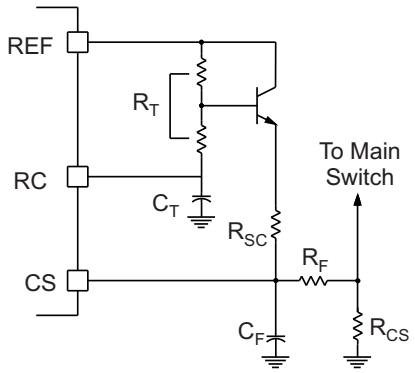


Figure 32. Adding Slope Compensation

9.4 Device Functional Modes

The UCCx80x family of high-speed, low-power integrated circuits has the following function modes.

9.4.1 Normal Operation

During this operation mode, IC controls the power converter into the voltage mode or current mode control, regulate the output voltage or current through the converter duty cycle. The regulation can be achieve through the integrated error amplifier or external feedback circuitry.

9.4.2 UVLO Mode

During the system start-up, VCC voltage starts to rise from 0. Before the VCC voltage reaches its corresponding turn on threshold, the IC is operate under UVLO mode. In this mode, REF pin voltage is not generated. When VCC is above 1 V and below the turn on threshold, the RFE pin is actively pulled low through a 5-kΩ resistor. This way, REF pin can be used as a logic signal to indicate UVLO mode.

9.4.3 Soft Start Mode

Once VCC voltage rises across the UVLO level, or comes out of a fault mode, it enters the soft start mode. During soft start, the internal soft start capacitor C_{SS} clamps the error amplifier output voltage, forces it rise slowly. This in turn controls the power converter peak current rising slowly, reducing the voltage and current stress to the system. The UCCx80x family has a fixed build in soft-start time at 4 ms.

9.4.4 Fault Mode

A separate overcurrent comparator within the UCCx80x devices handles operation into a short-circuited or severely overloaded power supply output. This overcurrent comparator has a 1.5-V threshold and is also gated by the leading edge blanking signal to prevent false triggering. When the fault is first detected, the internal soft-start capacitor instantly discharges and stays discharged until the fault clears. At the same time, the PWM output is turned off and held off. This is often referred to as *hiccup*. This delay time is used to significantly reduce the input and dissipated power of the main converter and switching components. Full cycle soft start insures that there is a predictable delay of greater than 3 milliseconds between successive attempts to operate during fault.

Device Functional Modes (continued)

When the fault clears, the capacitor slowly charges and allows the error amp output (COMP) to rise. When COMP gets high enough to enable the output, another fault occurs, latching off the PWM output, but the soft-start capacitor still continues to rise to 4 V before being discharged and permitting start of a new cycle. This means that for a severe fault, successive retries are spaced by the time required to fully charge the soft-start capacitor.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The UCCx80x controllers are peak current mode (PCM) pulse width modulators (PWM). These controllers have an onboard amplifier and can be used in isolated and non-isolated power supply design. There is an onboard totem-pole gate driver capable of delivering 1 A of peak current. This is a high-speed PWM capable of operating at switching frequencies up to 1 MHz.

10.2 Typical Application

Figure 33 illustrates a typical circuit diagram for an AC-DC converter using the UCC2800 in a peak current mode controlled flyback application.

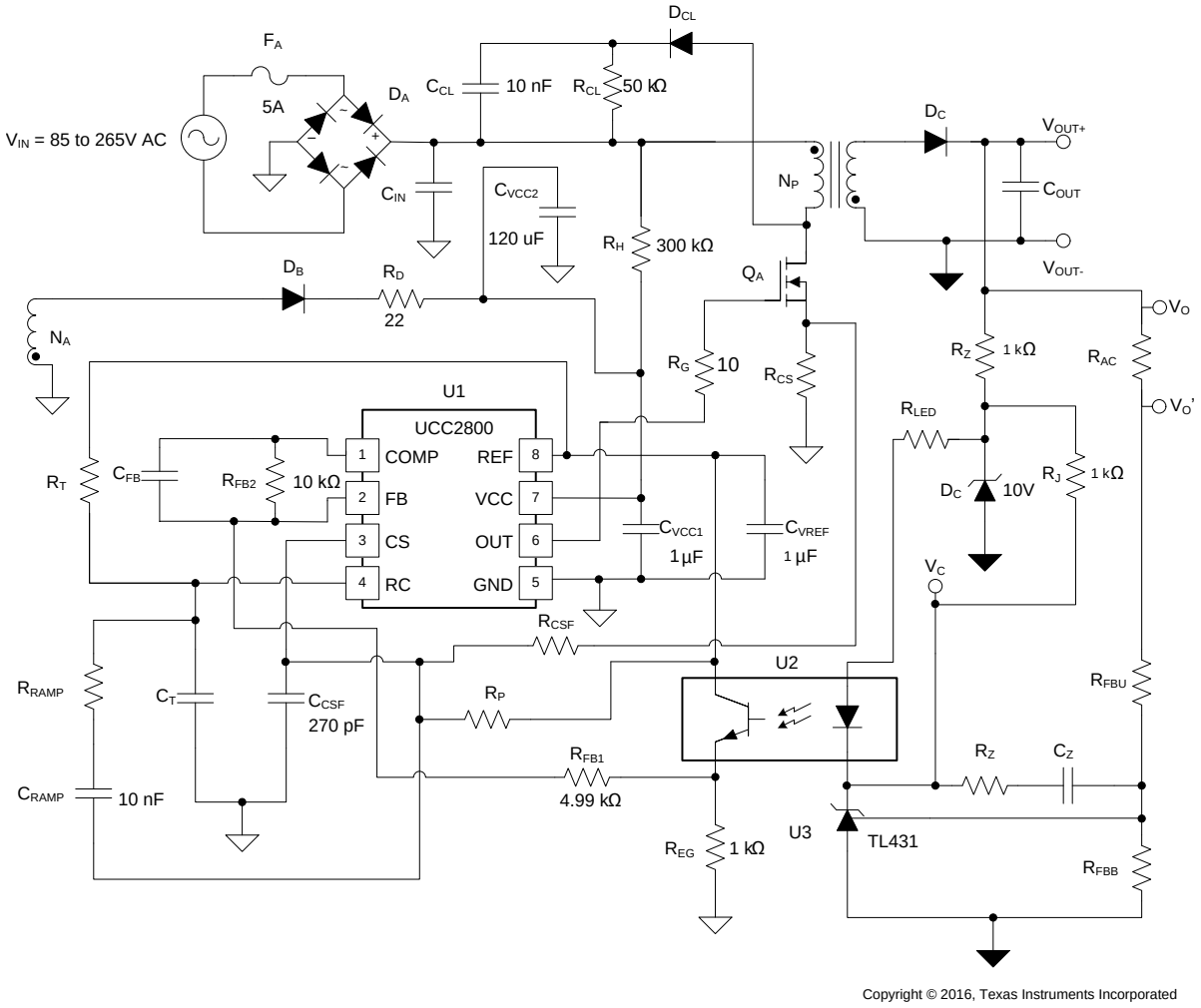


Figure 33. Typical Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

Use the parameters in Table 3 to review the design of a 12-V, 48-W offline flyback converter using UCC2800 PWM controller.

Table 3. Design Specifications

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERSTICS						
V_{IN}	Input voltage (RMS)		85		265	V
f_{LINE}	Line frequency		47		63	Hz
OUTPUT CHARACTRSTICS						
V_{OUT}	Output voltage		11.75	12	12.25	V
V_{ripple}	Output ripple voltage				120	mV_{PP}
I_{OUT}	Output current			4	4.33	A
V_{tran}	Output transient	Output voltage measured under 0-A to 4-A load step	11.75		12.25	V
SYSTEM CHARACTRSTICS						
η	Max load efficiency		85%			

10.2.2 Detailed Design Procedure

The design starts with selecting an appropriate bulk capacitor.

The primary side bulk capacitor is selected based on the power level. Based on the desired minimum bulk voltage level, the bulk capacitor value can be calculated as Equation 8.

$$C_{BULK} = \frac{2P_{IN} \times \left[0.25 + \frac{1}{\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right]}{\left(2V^2_{IN(min)} - V^2_{BULK(min)}\right) \times f_{LINE}} \quad (8)$$

In Equation 8, P_{IN} is the maximum output power divided by target efficiency, $V_{IN(min)}$ is the minimum AC input voltage RMS value. $V_{BULK(min)}$ is the target minimum bulk voltage, and f_{LINE} is the line frequency.

Based on the equation, to achieve 75-V minimum bulk voltage, assuming 85% converter efficiency and 47-Hz minimum line frequency, the bulk capacitor must be larger than 127 µF and 180 µF was chosen in the design, considering the tolerance of the capacitors.

The transformer design starts with selecting a suitable switching frequency. Generally the switching frequency selection is based on the tradeoff between the converter size and efficiency, based on the simple Flyback topology. Normally, higher switching frequency results in smaller transformer size. However, the switching loss is going to be increased and hurts the efficiency. Sometimes, the switching frequency is selected to avoid certain communication band to prevent the noise interference with the communication. The frequency selection is beyond the scope of this data sheet.

The switching frequency is selected as 110 kHz, to minimize the transformer size. At the same time, the regulations start to have limit on EMI noise at 150 kHz, design 110-kHz switching frequency can help to minimize the EMI filter size.

Then the transformer turns ratio can be selected based on the desired MOSFET voltage rating and diode voltage rating. Because maximum input voltage is 265 V AC, the peak voltage can be calculated as Equation 9.

$$V_{BULK(max)} = \sqrt{2} \times V_{IN(max)} \approx 375\ V \quad (9)$$

To minimize the cost of the system, the popular 650-V MOSFET is selected. Considering the design margin and extra voltage ringing on the MOSFET drain, the reflected output voltage must be less than 120 V. The transformer turns ratio can be selected as Equation 10.

$$n_{ps} = \frac{120V}{12V} = 10 \quad (10)$$

The diode voltage stress is the output voltage plus the reflected input voltage. The voltage stress on the diode can be calculated as Equation 11.

$$V_{DIODE} = \frac{V_{BULK(max)}}{n_{ps}} + V_{OUT} = \frac{375V}{10} + 12V \approx 50V \tag{11}$$

Consider the ringing voltage spikes and voltage derating the diode voltage rating must be higher than 50 V.

The transformer inductance selection is based on the CCM condition. Larger inductor would allow the converter stays in CCM longer. However, it tends to increase the transformer size. Normally, the transformer magnetizing inductor is selected so that the converter enters CCM operation at about 50% load at minimum line voltage. This would be a tradeoff between the transformer size and the efficiency. In this particular design, due to the higher output current, it is desired to keep the converter deeper in the CCM and minimize the conduction loss and output ripple. The converter enters CCM operation at about 10% load at minimum bulk voltage.

The inductor can be calculated as Equation 12.

$$L_m = \frac{1}{2} \frac{V^2_{BULK(min)} \times \left(\frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}} \right)^2}{10\,\% \times P_{IN} \times f_{SW}} \tag{12}$$

In this equation, the switching frequency is 110 kHz. Therefore, the transformer inductance must be about 1.7 mH. 1.5 mH is chosen as the magnetizing inductor value.

The auxiliary winding provides the power for UCC2800 normal operation. The auxiliary winding voltage is the output voltage reflected to the primary side. It is desired to have higher reflected voltage so that the IC can quickly get energy from the transformer and make the heavy load startup easier. However, the high the reflect voltage makes the IC consumes more power. Therefore, tradeoff is required.

In this design, the auxiliary winding voltage is selected the same as the output voltage so that it is above the UVLO level and keep the IC and driving loss low. Therefore, the auxiliary winding to the output winding turns ratio is selected as Equation 13.

$$n_{as} = \frac{12\ V}{12\ V} = 1 \tag{13}$$

Based on calculated inductor value and the switching frequency, the current stress of the MOSFET and diode can be calculated.

The peak current of the MOSFET can be calculated as Equation 14.

$$I_{PK_{MOS}} = \frac{P_{IN}}{V_{BULK(min)} \times \frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}}} + \frac{1}{2} \frac{V_{BULK(min)}}{L_m} \times \frac{\frac{n_{PS} V_{OUT}}{V_{BULK(min)} + n_{PS} V_{OUT}}}{f_{sw}} \tag{14}$$

The MOSFET peak current is 1.425 A.

The diode peak current is the reflected MOSFET peak current on the secondary side.

$$I_{PK_{DIODE}} = n_{ps} \times I_{PK_{MOS}} = 14.25\ A \tag{15}$$

The RMS current of the MOSFET can be calculated as Equation 16.

$$I_{RMS_{MOS}} = \sqrt{\frac{1}{3} D^3 \times \left(\frac{V_{BULK(min)}}{L_m \times f_{sw}} \right)^2 - \frac{D^2 I_{PK_{MOS}} V_{BULK(min)}}{L_m \times f_{sw}} + D \times I^2_{PK_{MOS}}} \tag{16}$$

In Equation 16, D is the MOSFET duty cycle at minimum bulk voltage and it can be calculated as Equation 17.

$$D = \frac{n_{ps} V_{OUT}}{V_{BULK(min)} + n_{ps} V_{OUT}} \tag{17}$$

The MOSFET RMS current is 0.75 A. Therefore, IRFB9N65A is selected as primary side MOSFET.

The diode average current is the output current 4 A with 60-V rating and 14.25-A peak current capability, 48CTQ060-1 is selected.

Output capacitor is selected based on the output voltage ripple requirement. In this design, 0.1% voltage ripple is assumed. Based on the 0.1% ripple requirement, the capacitor value can be selected based on Equation 18.

$$C_{OUT} \geq \frac{I_{OUT} \times \frac{n_{ps} V_{OUT}}{V_{BULK(min)} + n_{ps} V_{OUT}}}{0.1\% \times V_{OUT} \times f_{sw}} = 2105\mu F \quad (18)$$

Consider the tolerance and temperature effect, together the ripple current rating of the capacitors, the output capacitor of 3 of 680 µF in parallel was selected.

After the power stage is designed, the surround components can be selected.

10.2.2.1 Current Sensing Network

The current sensing network consists of R_{CS}, R_{CSF}, C_{CSF}, and optional R_P. Typically, the direct current sense signal contains a large amplitude leading edge spike associated with the turnon of the main power MOSFET, reverse recovery of the output rectifier, and other factors including charging and discharging of parasitic capacitances. Therefore, C_{CSF} and R_{CSF} form a low-pass filter that provides additional immunity beyond the internal blanking time to suppress the leading edge spike. For this converter, C_{CSF} is chosen to be 270 pF to provide enough filtering.

Without R_P, R_{CS} sets the maximum peak current in the transformer primary based on the maximum amplitude of CS pin, 1 V. To achieve 1.425-A primary side peak current, a 0.75-Ω resistor is chosen for R_{CS}.

The high current sense threshold help to provide better noise immunity but the current sense loss is increased. The current sense loss can be minimized by injecting offset voltage into the current sense signal. R_P and R_{CS} form a resistor divider network from the current sense signal to the device's reference voltage to offset the current sense voltage. This technique still achieves current mode control with cycle-by-cycle overcurrent protection. To calculate required offset value (Voffset), use Equation 19.

$$V_{offset} = \frac{R_{CSF}}{R_{CSF} + R_P} V_{REF} \quad (19)$$

10.2.2.2 Gate Drive Resistor

R_G is the gate driver resistor for the power switch, Q_A. The selection of this resistor value must be done in conjunction with EMI compliance testing and efficiency testing. Larger R_G slows down the turnon and turnoff of the MOSFET. Slower switching speed reduces EMI but also increases the switching loss. A tradeoff between switching loss and EMI performance must be carefully performed. For this design, 10 Ω was chosen as the gate driver resistor.

10.2.2.3 Vref Capacitor

A precision 5-V reference voltage is designed to perform several important functions. The reference voltage is divided down internally to 2.5 V and connected to the error amplifier's noninverting input for accurate output voltage regulation. Other duties of the reference voltage are to set internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds along with the overcurrent limiting threshold. Therefore, the reference voltage must be bypassed with a ceramic capacitor (C_{VREF}), and 1-µF, 16-V ceramic capacitor was selected for this converter. Placement of this capacitor on the physical printed-circuit board layout must be as close as possible to the respective REF and GND pins as possible

10.2.2.4 $R_T C_T$

The internal oscillator uses a timing capacitor (C_T) and a timing resistor (R_T) to program operating frequency and maximum duty cycle. The operating frequency can be programmed based the curves in Figure 3, where the timing resistor can be found once the timing capacitor is selected. The selection of timing capacitor also affects the maximum duty cycle provided in Figure 5. It is best for the timing capacitor to have a flat temperature coefficient, typical of most COG or NPO type capacitors. For this converter, 13.6 kΩ and 1000 pF were selected for R_T and C_T to operate at 110-kHz switching.

10.2.2.5 Start-Up Circuit

At startup, the IC gets its power directly from the high voltage bulk, through a high voltage resistor R_H. The selection of start-up resistor is the tradeoff between power loss and start-up time. The current flowing through R_H at minimum input voltage must be higher than the VCC current under UVLO condition (0.2 mA at its maximum value). A 150-kΩ resistor is chosen as the result of the tradeoff.

After VCC is charged up above UVLO on threshold, UCC2800 starts to operate and consumes full operating current. At the beginning, because the output voltage is low, VCC cannot get energy from the auxiliary winding. VCC capacitor requires to hold enough energy to prevent its voltage drop below UVLO during start-up time, before output reaches high enough. A larger capacitor holds more energy but slows down the start-up time. In this design, a 120-µF capacitor is chosen to provide enough energy for the start-up purpose.

10.2.2.6 Voltage Feedback Compensation

Feedback compensation, also called closed-loop control, reduces or eliminates steady state error, reduces the sensitivity to parametric changes, changes the gain or phase of a system over some desired frequency range, reduces the effects of small signal load disturbances and noise on system performance, and creates a stable system. The following section describes how to compensate an isolated Flyback converter with the peak current mode control.

10.2.2.6.1 Power Stage Gain, Zeroes, and Poles

The first step in compensating a fixed frequency flyback is to verify if the converter is continuous conduction mode (CCM) or discontinuous conduction mode (DCM). If the primary inductance, L_P, is greater than the inductance for DCM, CCM boundary mode operation, called the critical inductance, or L_{Pcrit}, then the converter operates in CCM calculated with Equation 20.

$$L_{Pcrit} = \frac{R_{OUT} \times N_{PS}^2}{2 \times f_{SW}} \times \left(\frac{V_{IN}}{V_{IN} + V_{OUT} \times N_{PS}} \right)^2 \quad (20)$$

For the entire input voltage range, the selected inductor has value larger than the critical inductor. Therefore, the converter operates in CCM and the compensation loop requires design based on CCM flyback equations.

The current-to-voltage conversion is done externally with the ground-referenced current sense resistor, R_{CS}, and the internal resistor divider sets up the internal current sense gain, A_{CS} = 1.65. The IC technology allows the tight control of the resistor divider ratio, regardless of the actual resistor value variations.

The DC open-loop gain, G_O, of the fixed-frequency voltage control loop of a peak current mode control CCM flyback converter shown in Figure 33 is approximated by first using the output load, R_{OUT}, the primary to secondary turns ratio, N_{PS}, the maximum duty cycle, D, calculated in Equation 21.

$$G_O = \frac{R_{OUT} \times N_{PS}}{R_{CS} \times A_{CS}} \times \frac{1}{\frac{(1-D)^2}{\tau_L} + (2 \times M) + 1} \quad (21)$$

In Equation 21, D is calculated with Equation 22, τ_L is calculated with Equation 23, and M is calculated with Equation 24.

$$D = \frac{N_{PS} \times V_{OUT}}{V_{IN} + (N_{PS} \times V_{OUT})} \quad (22)$$

$$\tau_L = \frac{2 \times L_P \times f_{SW}}{R_{OUT} \times N_{PS}^2} \quad (23)$$

$$M = \frac{V_{OUT} \times N_{PS}}{V_{IN}} \quad (24)$$

For this design, a converter with an output voltage V_{OUT} of 12 V, and 48 W relates to an output load, R_{OUT}, equal to 3 Ω at full load.

At minimum input voltage of 75 V DC, the duty cycle reaches it maximum value of 0.615. The current sense resistance, R_{CS}, is 0.75 Ω, and a primary to secondary turns-ratio, N_{PS} is 10. The open-loop gain calculates to 14.95 dB.

A CCM flyback has two zeroes that are of interest. The ESR and the output capacitance contribute a left-half plane zero to the power stage, and the frequency of this zero, f_{ESRz}, are calculated with Equation 25.

$$\omega_{ESRz} = \frac{1}{R_{ESR} \times C_{OUT}} \tag{25}$$

The f_{ESRz} zero for a capacitance bank of three 680-µF capacitors for a total output capacitance of 2040 µF and a total ESR of 13 mΩ is placed at 6 kHz.

CCM flyback converters have a zero in the right-half plane, RHP, in their transfer function. RHP zero has the same 20 dB/decade rising gain magnitude with increasing frequency just like a left-half plane zero, but it adds phase lag instead of lead. This phase lag tends to limit the overall loop bandwidth. The frequency location, f_{RHPz} in Equation 26, is a function of the output load, the duty cycle, the primary inductance, L_P, and the primary to secondary side turns ratio, N_{PS}.

$$f_{RHPz} = \frac{R_{OUT} \times (1-D)^2 \times N_{PS}^2}{2 \times \pi \times L_P \times D} \tag{26}$$

Right half plane zero frequency increases with higher input voltage and lighter load. Generally, the design requires consideration of the worst case of the lowest right half plane zero frequency and the converter must be compensated at the minimum input and maximum load condition. With a primary inductance of 1.5 mH, at 75-V DC input, the RHP zero frequency, f_{RHPz}, is equal to 7.65 kHz at maximum duty cycle, full load.

The power stage has one dominate pole, ω_{P1}, which is in the region of interest, placed at a lower frequency, f_{P1}, which is related to the duty cycle, D, the output load, and the output capacitance. There is also a double pole placed at half the switching frequency of the converter, f_{P2} calculated with Equation 27 and Equation 28.

$$f_{P1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{2 \times \pi \times R_{OUT} \times C_{OUT}} \tag{27}$$

$$f_{P2} = \frac{f_{SW}}{2} \tag{28}$$

Slope compensation is the large signal sub-harmonic instability that can occur with duty cycles that extends beyond 50%. The subharmonic oscillation increases the output voltage ripple and sometimes it even limits the power handling capability of the converter.

The target of slope compensation is to achieve idea quality coefficient, Q_p , at half of the switching frequency to be 1. The Q_p is calculated with Equation 29.

$$Q_P = \frac{1}{\pi \times \left[M_C \times (1-D) - 0.5\right]} \tag{29}$$

In Equation 29, D is the primary side switch duty cycle and M_C is the slope compensation factor, which is defined with Equation 30.

$$M_C = 1 + \frac{S_e}{S_n} \tag{30}$$

In Equation 30, Se is the compensation ramp slope and the S_n is the inductor rise slope. The optimal goal of the slope compensation is to achieve Q_P equal to 1, which mean M_C must be 2.128 when D reaches it maximum value of 0.615.

The inductor rise slop on CS pin is calculated with Equation 31.

$$S_n = \frac{V_{BULK(min)} \times R_{CS}}{L_P} = \frac{75V \times 0.75\Omega}{1.5mH} = 38mV/\mu s \tag{31}$$

The compensation slope is calculated with Equation 32.

$$S_e = (M_C - 1) \times S_n = (2.128 - 1) \times 38\ mV/\mu s = 46.3\ mV/\mu s \tag{32}$$

The compensation slope is added into the system through R_{RAMP} and R_{CSF}. The C_{RAMP} is selected to approximate high frequency short circuit. Choose C_{RAMP} as 10 nF as the starting point, and make adjustments if required. The R_{RAMP} and R_{CSF} forms a voltage divider from the RC pin ramp voltage and inject the slope compensation into CS pin. Choose R_{RAMP} much larger than the R_T resistor so that it won't affect much the frequency setting. In this design, R_{RAMP} is selected as 24.9 kΩ. The RC pin ramp slope is calculated with Equation 33.

$$S_{RC} = 2.4\ V \times 100\ kHz = 240\ mV / \mu s \tag{33}$$

To achieve 46.3 mV/µs compensation slope, R_{CSF} resistor is calculated with Equation 34.

$$R_{CSF} = \frac{R_{RAMP}}{\frac{S_{RC}}{R_e} - 1} = \frac{24.9\ k\Omega}{\frac{240\ mV / \mu s}{46.3\ mV / \mu s} - 1} = 5.95\ k\Omega \tag{34}$$

The power stage open-loop gain and phase can be plotted as a function of frequency. The total gain, as a function of frequency can be characterized with Equation 35.

$$H_0(S) = G_0 \times \frac{\left(1 + \frac{S}{\omega_{ESRz}}\right) \times \left(1 - \frac{S}{\omega_{RHPz}}\right)}{1 + \frac{s(f)}{\omega_{P1}}} \times \frac{1}{1 + \frac{S}{\omega_{P2} \times Q_P} + \frac{S^2}{\omega_{P2}^2}} \tag{35}$$

The bode is plotted accordingly (see Figure 34 and Figure 35).

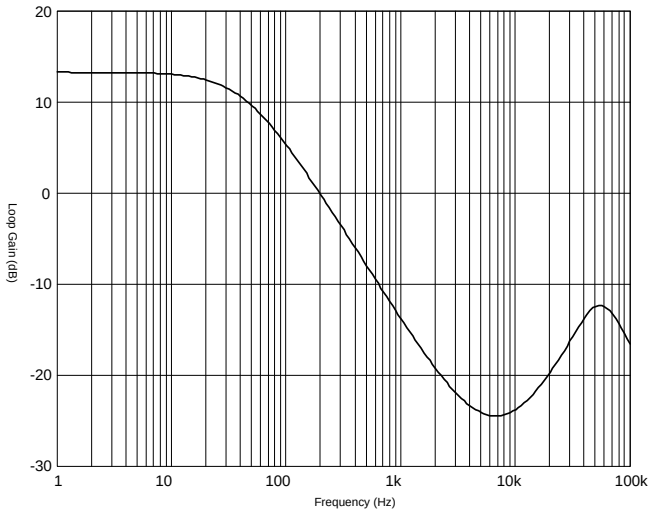


Figure 34. Converter Open Loop Bode Plot - Gain

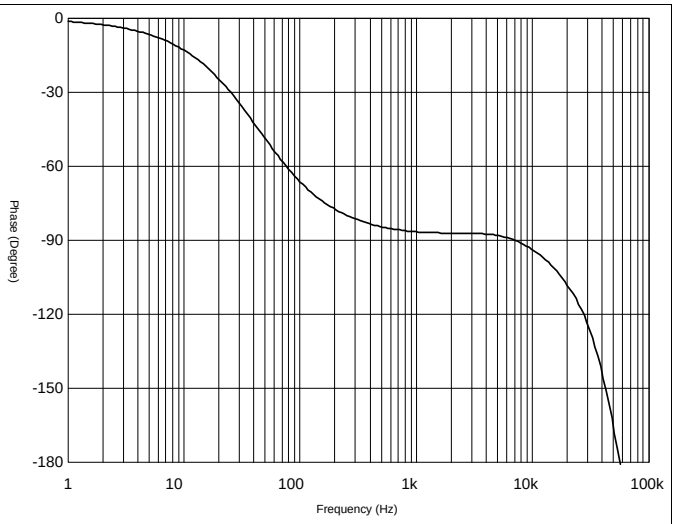


Figure 35. Converter Open Loop Bode Plot - Phase

10.2.2.6.2 Compensation Loop

For good transient response, the bandwidth of the finalized design must be as large as possible. The bandwidth of a CCM flyback, f_{BW}, is limited to ¼ of the RHP zero frequency, or approximately 1.9 kHz using Equation 36.

$$f_{BW} = \frac{f_{RHPz}}{4} \tag{36}$$

The gain of the open-loop power stage at f_{BW} is equal to –22.4 dB and the phase at f_{BW} is equal to –87°. First step is to choose the output voltage sensing resistor values. The output sensing resistors are selected based on the allowed power consumption and in this case, 1 mA of sensing current is assumed.

The TL431 is used as the feedback amplifier. Given its 2.5-V reference voltage, the voltage sensing dividers R_{FBU} and R_{FBB} can be selected with Equation 37 and Equation 38.

$$R_{FBU} = \frac{V_{OUT} - 2.5\ V}{1\ mA} = 9.5\ k\Omega \tag{37}$$

$$R_{FBB} = \frac{2.5\ V}{1\ mA} = 2.5\ k\Omega \tag{38}$$

Next step is to put the compensator zero f_{CZ} at 190 Hz, which is 1/10 of the crossover frequency. Choose C_Z as a fixed value of 10 nF and choose the zero resistor value according to Equation 39.

$$R_Z = \frac{1}{2\pi \times f_{CZ} \times C_Z} = \frac{1}{2\pi \times 190\ Hz \times 10\ nF} = 83.77\ k\Omega \tag{39}$$

Then put a pole at the lower frequency of right half plane zero or the ESR zero. Based previous analysis, the right half plane zero is at 7.65 kHz and the ESR zero is at 6 kHz, the pole of the compensation loop must be put at 6 kHz. This pole can be added through the primary side error amplifier. R_{FB} and C_{FB} provide the necessary pole. Choosing R_{FB} as 10 kΩ and the C_{FB} is selected with Equation 40.

$$C_{FB} = \frac{1}{2\pi \times 10\ k\Omega \times 6\ kHz} = 2.65\ nF \tag{40}$$

Based on the compensation loop structure, the entire compensation loop transfer function is written as Equation 41.

$$G(S) = \frac{1}{R_{FBT} \cdot R_{LED}} \cdot \frac{1 + S \cdot C_Z \cdot R_Z}{S \cdot C_Z} \cdot \frac{R_{FB2}}{R_{FB1}} \cdot \frac{1}{S \cdot C_{FB} \cdot R_{FB2} + 1} \cdot CTR \cdot R_{EG} \tag{41}$$

In this equation, the CTR is the current transfer ratio of the opto-coupler. Choose 1 as the nominal value for CTR. R_{EG} is the opto-pulldown resistor and 1 kΩ is chosen as a default value. The only value required in this equation is R_{LED}. The entire loop gain must be equal to 1 at the crossover frequency. R_{LED} is calculated accordingly as 1.62 kΩ.

The final close loop bode plots are show in Figure 36 and Figure 37. The converter achieves approximately 2-kHz crossover frequency and approximately 70° of phase margin.

TI recommends checking the loop stability across all the corner cases including component tolerances to ensure system stability.

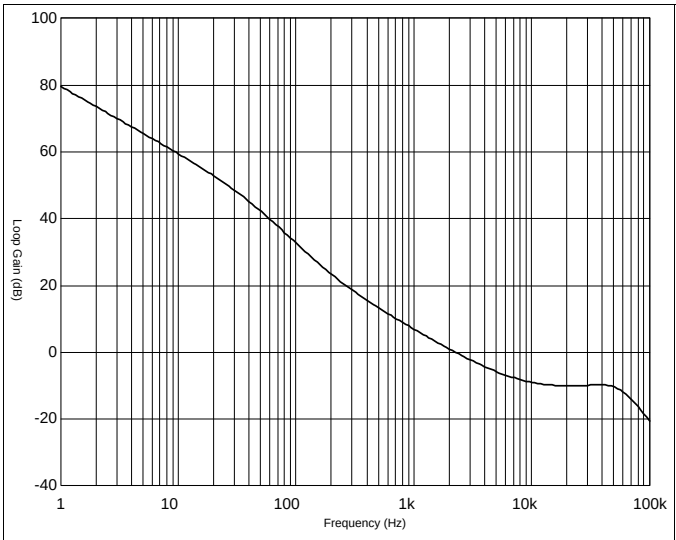


Figure 36. Converter Close Loop Bode Plot – Gain

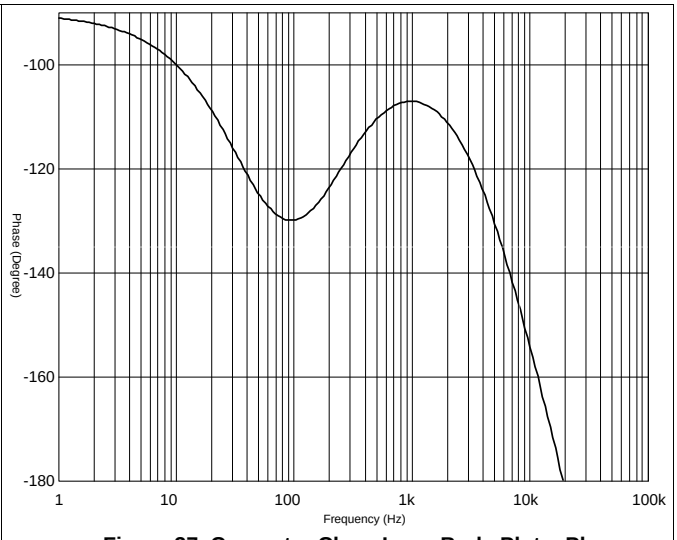


Figure 37. Converter Close Loop Bode Plot – Phase

10.2.3 Application Curves

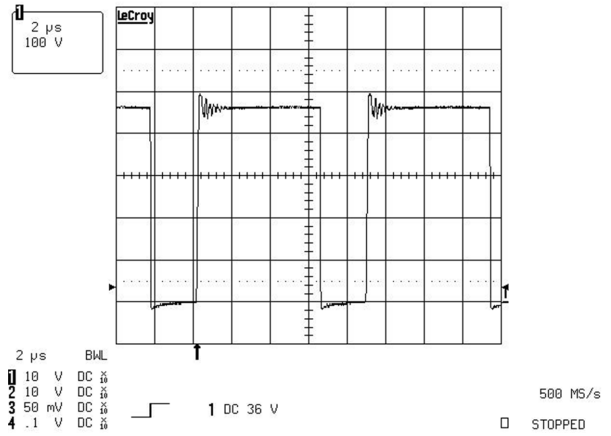


Figure 38. Primary Side MOSFET Drain to Source Voltage at 240-V AC Input (100 V/div)

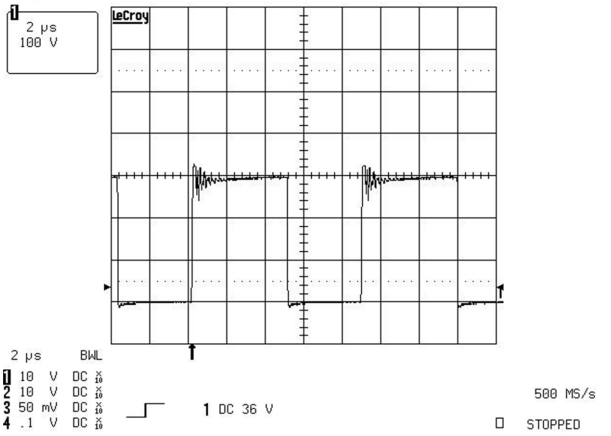


Figure 39. Primary Side MOSFET Drain to Source Voltage at 120-V AC Input (100 V/div)

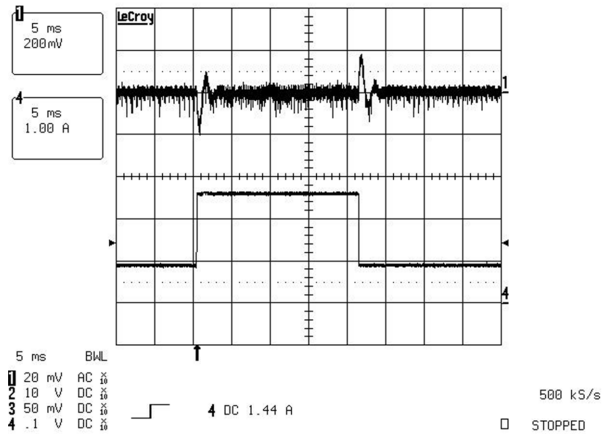


Figure 40. Output Voltage During 0.9-A to 2.7-A Load Transient (CH1: Output Voltage AC Coupled, 200 mV/div; CH4: Output Current, 1 A/div)

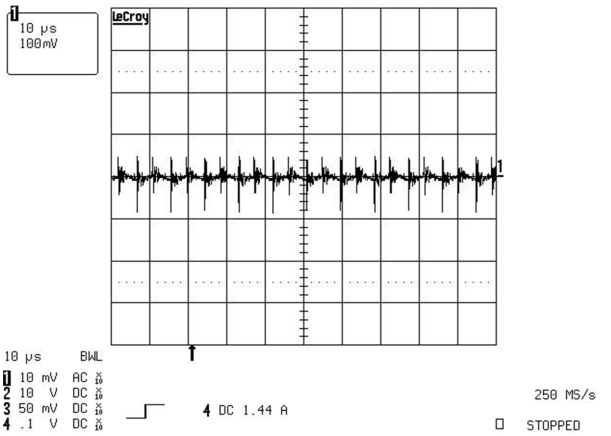


Figure 41. Output Voltage Ripple at Full Load (100 mV/div)

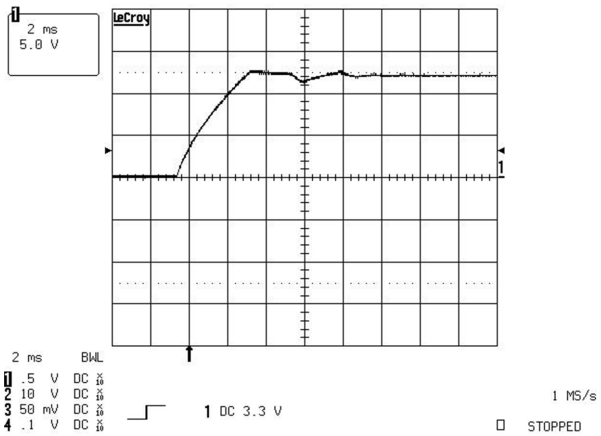


Figure 42. Output Voltage Behavior at Full Load Start-up (5 V/div)

11 Power Supply Recommendations

An internal VCC shunt regulator is incorporated in each member of the UCC380x PWMs to regulate the supply voltage at approximately 13.5 V. A series resistor from VCC to the input supply source is required with inputs above 12 V to limit the shunt regulator current. A maximum of 10 mA can be shunted to ground by the internal regulator. The internal regulator in conjunction with the device's low start-up and operating current can greatly simplify powering the device and may eliminate the requirement for a regulated bootstrap auxiliary supply and winding in many applications. The supply voltage is MOSFET gate level compatible and requires no external Zener diode or regulator protection with a current-limited input supply. The UVLO start-up threshold is 1 V below the shunt regulator level on the UCCx802 and UCCx804 devices to ensure start-up. It is important to bypass the ICs supply (VCC) and reference voltage (REF) pins with a 0.1-µF to 1-µF ceramic capacitor to ground. The capacitors must be placed as close to the actual pin connections as possible for optimal noise filtering. A second, larger filter capacitor may also be required in offline applications to hold the supply voltage (VCC) above the UVLO turnoff threshold during start-up.

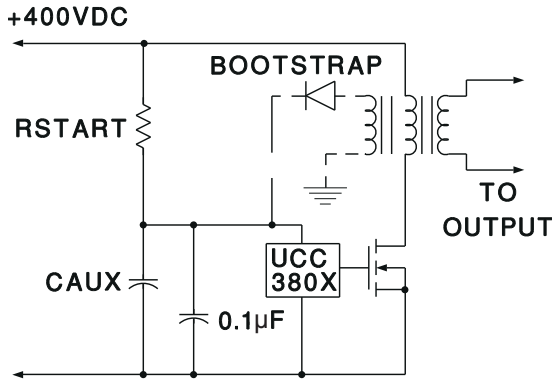


Figure 43. Different Ways of Powering Up the Device

12 Layout

12.1 Layout Guidelines

In addition to following general power management IC layout guidelines (star grounding, minimal current loops, reasonable impedance levels, and so on) layout for the UCCx80x family must consider the following:

- If possible, a ground plane must be used to minimize the voltage drop on the ground circuit and the noise introduced by parasitic inductances in individual traces.
- A decoupling capacitor is required for both the VCC pin and REF pin and both must be returned to GND as close to the IC as possible.
- For the best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.
- The CS pin filter capacitor must be as close to the IC possible and grounded right at the IC ground pin. This ensures the best filtering effect and minimizes the chance of current sense pin malfunction.
- Gate driver loop area must be minimized to reduce the EMI noise because of the high di/dt current in the loop.

12.2 Layout Example

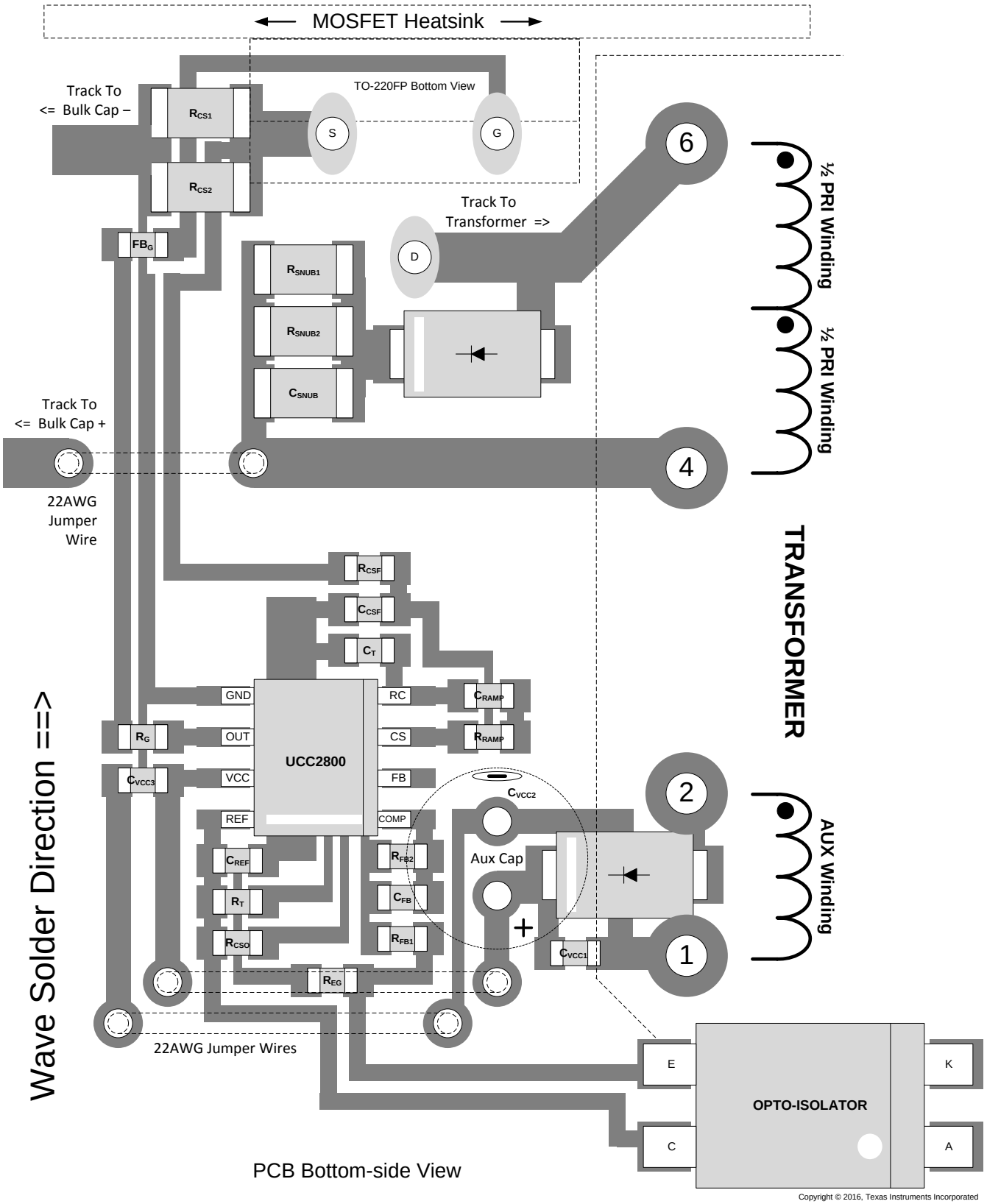


Figure 44. UCC2800 Layout Example

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC1800	Click here	Click here	Click here	Click here	Click here
UCC1801	Click here	Click here	Click here	Click here	Click here
UCC1802	Click here	Click here	Click here	Click here	Click here
UCC1803	Click here	Click here	Click here	Click here	Click here
UCC1804	Click here	Click here	Click here	Click here	Click here
UCC1805	Click here	Click here	Click here	Click here	Click here
UCC2800	Click here	Click here	Click here	Click here	Click here
UCC2801	Click here	Click here	Click here	Click here	Click here
UCC2802	Click here	Click here	Click here	Click here	Click here
UCC2803	Click here	Click here	Click here	Click here	Click here
UCC2804	Click here	Click here	Click here	Click here	Click here
UCC2805	Click here	Click here	Click here	Click here	Click here
UCC3800	Click here	Click here	Click here	Click here	Click here
UCC3801	Click here	Click here	Click here	Click here	Click here
UCC3802	Click here	Click here	Click here	Click here	Click here
UCC3803	Click here	Click here	Click here	Click here	Click here
UCC3804	Click here	Click here	Click here	Click here	Click here
UCC3805	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9451301MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451301MPA UCC1801	Samples
5962-9451302MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451302MPA UCC1802	Samples
5962-9451303MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451303MPA UCC1803	Samples
5962-9451304MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451304MPA UCC1804	Samples
5962-9451305MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451305MPA UCC1805	Samples
UCC1800J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UCC1800J	Samples
UCC1800J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UCC1800J/ 883B	Samples
UCC1800L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UCC1800L/ 883B	Samples
UCC1801J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UCC1801J	Samples
UCC1801J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451301MPA UCC1801	Samples
UCC1802J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UCC1802J	Samples
UCC1802J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451302MPA UCC1802	Samples
UCC1803J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UCC1803J	Samples
UCC1803J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451303MPA UCC1803	Samples
UCC1804J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UCC1804J	Samples
UCC1804J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451304MPA UCC1804	Samples
UCC1805J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UCC1805J	Samples
UCC1805J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9451305MPA UCC1805	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2800D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2800	Samples
UCC2800DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2800	Samples
UCC2800DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2800	Samples
UCC2800DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2800	Samples
UCC2800N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2800N	Samples
UCC2800PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2800	Samples
UCC2801D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2801	Samples
UCC2801DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2801	Samples
UCC2801DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2801	Samples
UCC2801DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2801	Samples
UCC2801N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2801N	Samples
UCC2801PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2801	Samples
UCC2802D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2802	Samples
UCC2802DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2802	Samples
UCC2802DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2802	Samples
UCC2802J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-40 to 85	UCC2802J	Samples
UCC2802N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2802N	Samples
UCC2802NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2802N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2802PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2802	Samples
UCC2803D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2803	Samples
UCC2803DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2803	Samples
UCC2803DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2803	Samples
UCC2803DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2803	Samples
UCC2803N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2803N	Samples
UCC2803PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2803	Samples
UCC2803PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2803	Samples
UCC2804D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2804	Samples
UCC2804DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2804	Samples
UCC2804DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2804	Samples
UCC2804N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2804N	Samples
UCC2804PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2804	Samples
UCC2804PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2804	Samples
UCC2805D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2805	Samples
UCC2805DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2805	Samples
UCC2805DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2805	Samples
UCC2805N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2805N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2805PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2805	Samples
UCC2805PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2805	Samples
UCC2805PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2805	Samples
UCC3800D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3800	Samples
UCC3800DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3800	Samples
UCC3800DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3800	Samples
UCC3800N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3800N	Samples
UCC3800NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3800N	Samples
UCC3800PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3800	Samples
UCC3801D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3801	Samples
UCC3801DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3801	Samples
UCC3801DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3801	Samples
UCC3801N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3801N	Samples
UCC3801NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3801N	Samples
UCC3801PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3801	Samples
UCC3801PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3801	Samples
UCC3802D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3802	Samples
UCC3802DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3802	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3802DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3802	Samples
UCC3802DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3802	Samples
UCC3802N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3802N	Samples
UCC3802PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3802	Samples
UCC3803D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3803	Samples
UCC3803DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3803	Samples
UCC3803DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3803	Samples
UCC3803N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3803N	Samples
UCC3803PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3803	Samples
UCC3803PWTRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3803	Samples
UCC3804D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3804	Samples
UCC3804DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3804	Samples
UCC3804DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3804	Samples
UCC3804DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3804	Samples
UCC3804N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3804N	Samples
UCC3804NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3804N	Samples
UCC3804PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3804	Samples
UCC3804PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3804	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3805D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3805	Samples
UCC3805DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3805	Samples
UCC3805DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3805	Samples
UCC3805DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3805	Samples
UCC3805N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3805N	Samples
UCC3805NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3805N	Samples
UCC3805PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3805	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC1800, UCC1801, UCC1802, UCC1803, UCC1804, UCC1805, UCC2800, UCC2801, UCC2802, UCC2802M, UCC2803, UCC2804, UCC2805, UCC3800, UCC3801, UCC3802, UCC3803, UCC3804, UCC3805 :

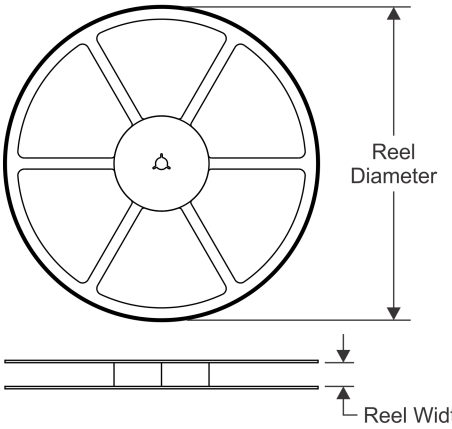
- Catalog: UCC3800, UCC3801, UCC3802, UCC3803, UCC3804, UCC3805, UCC2802
- Automotive: UCC2800-Q1, UCC2801-Q1, UCC2802-Q1, UCC2802-Q1, UCC2803-Q1, UCC2804-Q1, UCC2805-Q1
- Enhanced Product: UCC2800-EP, UCC2801-EP, UCC2802-EP, UCC2802-EP, UCC2803-EP, UCC2804-EP, UCC2805-EP
- Military: UCC2802M, UCC1800, UCC1801, UCC1802, UCC1803, UCC1804, UCC1805

NOTE: Qualified Version Definitions:

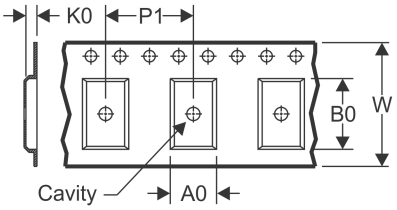
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

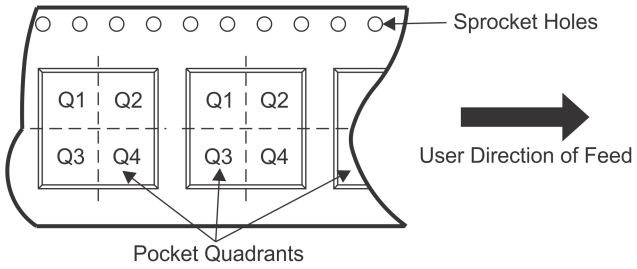


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

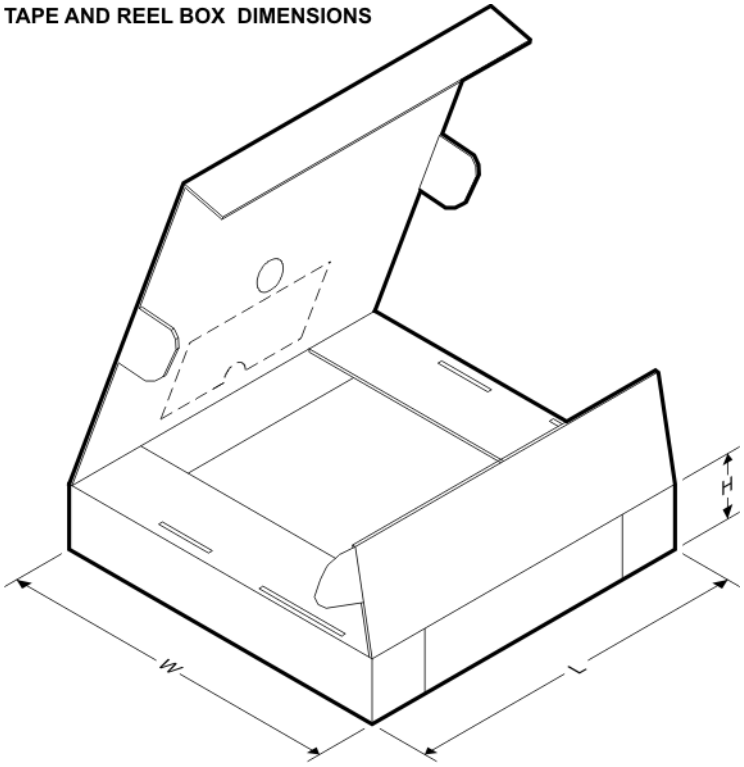
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2800DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2801DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2802DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2803DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2803PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC2804DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2804PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC2805DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2805PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3800DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3801DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3801PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3802DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3803DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3803PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3804DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3804PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3805DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

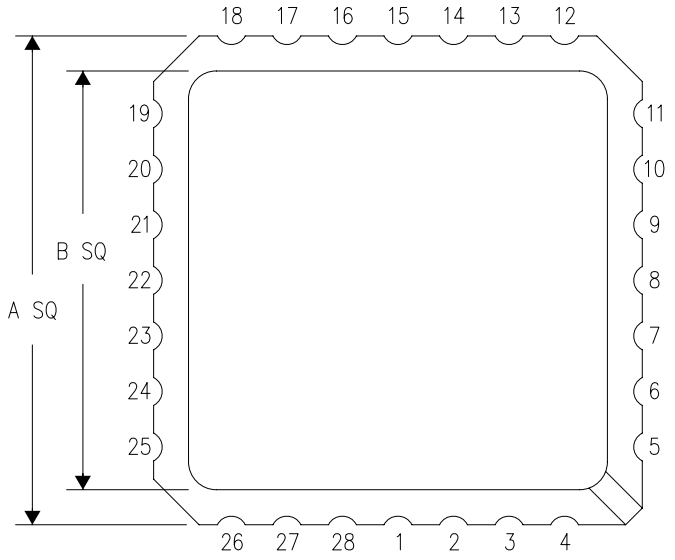


*All dimensions are nominal

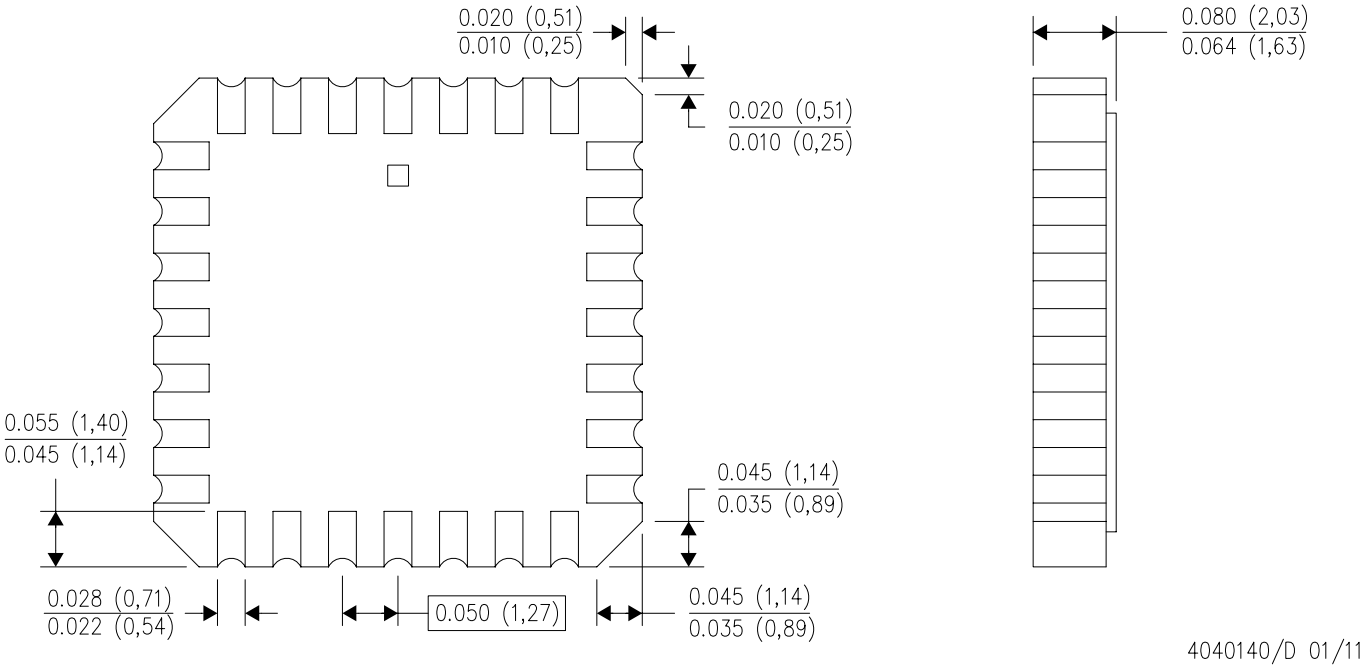
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2800DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2801DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2802DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2803DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2803PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC2804DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2804PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC2805DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2805PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3800DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3801DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3801PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3802DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3803DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3803PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3804DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3804PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3805DTR	SOIC	D	8	2500	340.5	338.1	20.6

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

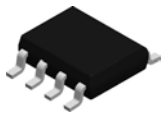


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

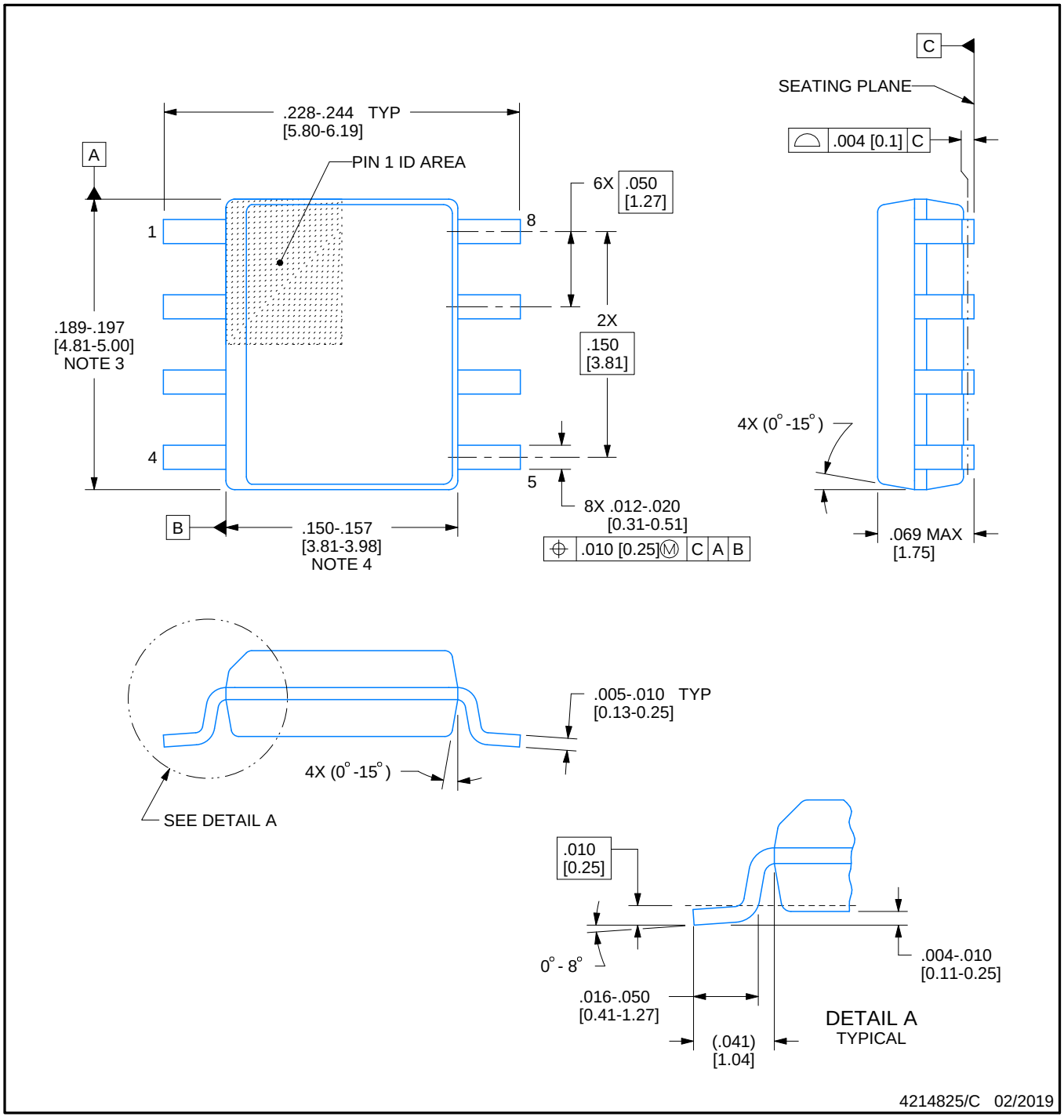


PACKAGE OUTLINE

D0008A

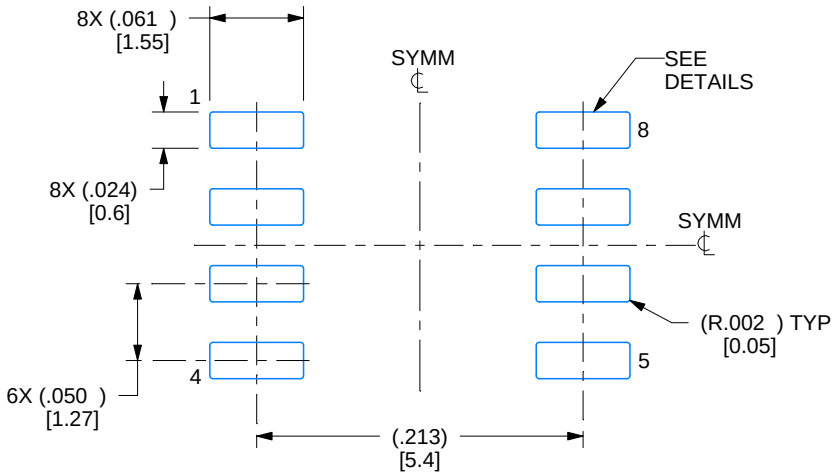
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

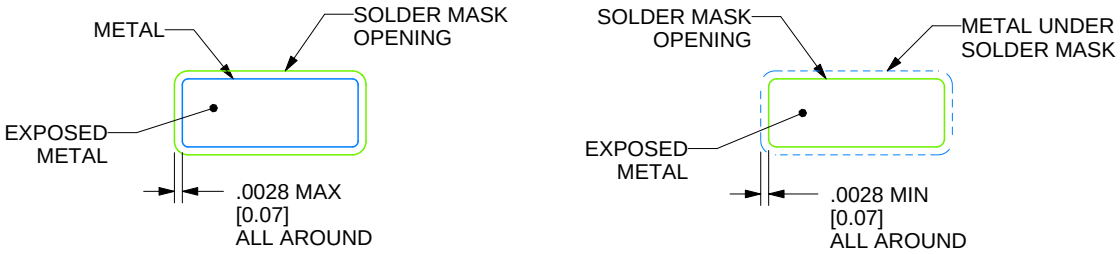


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

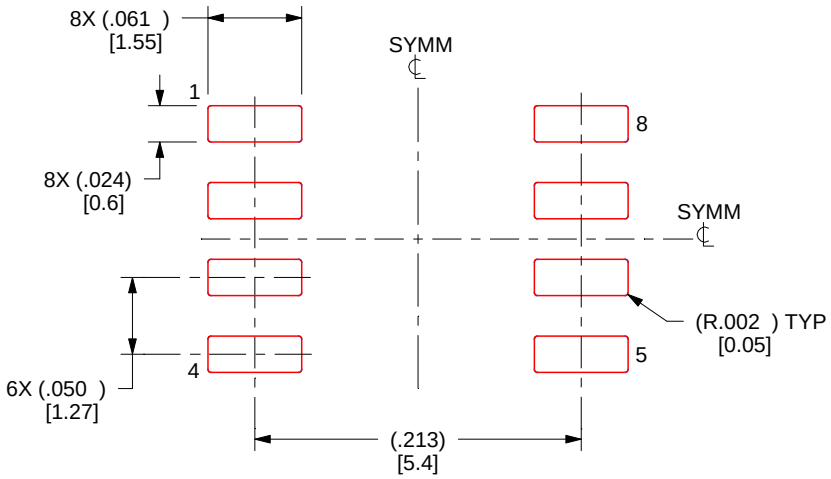
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

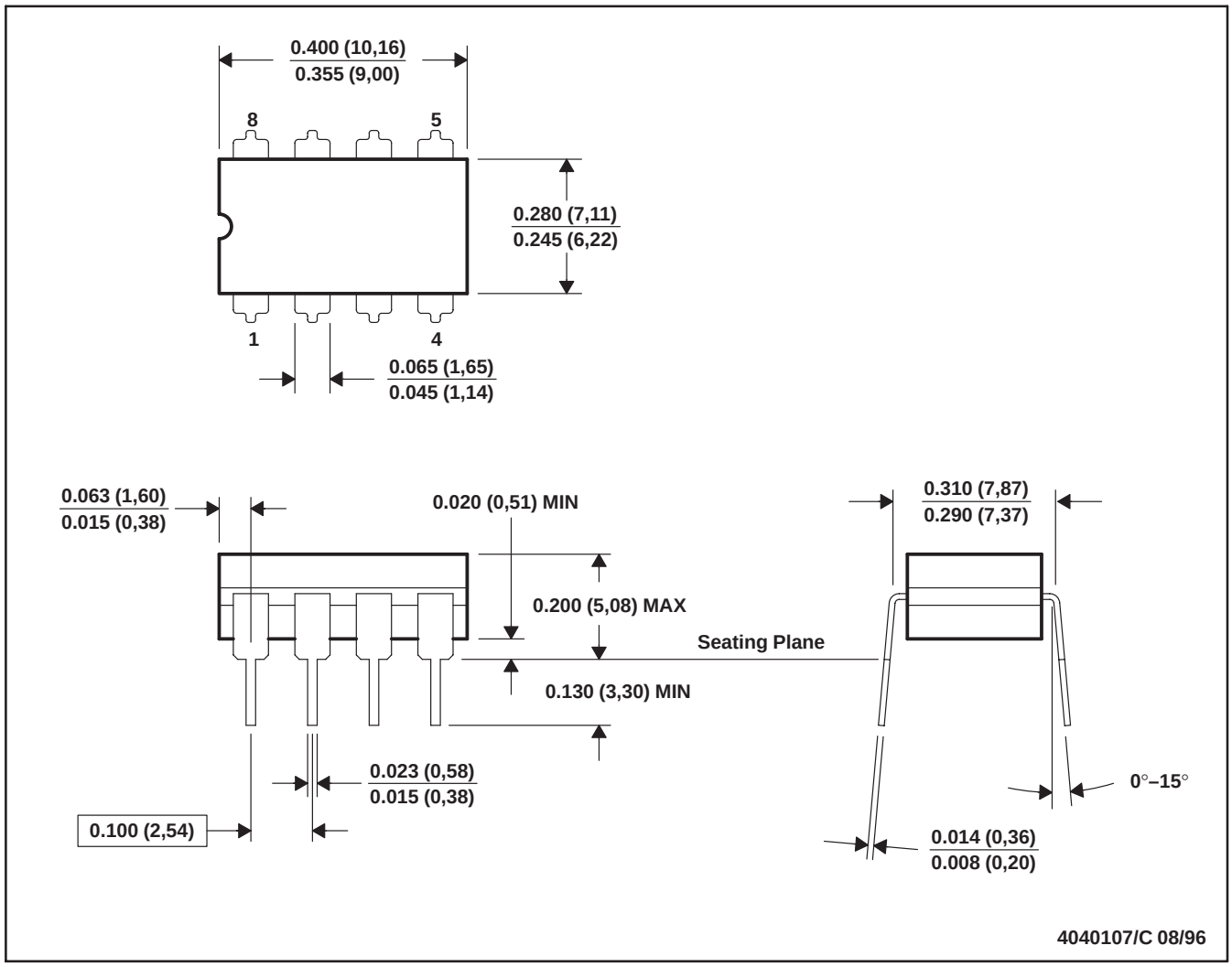
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

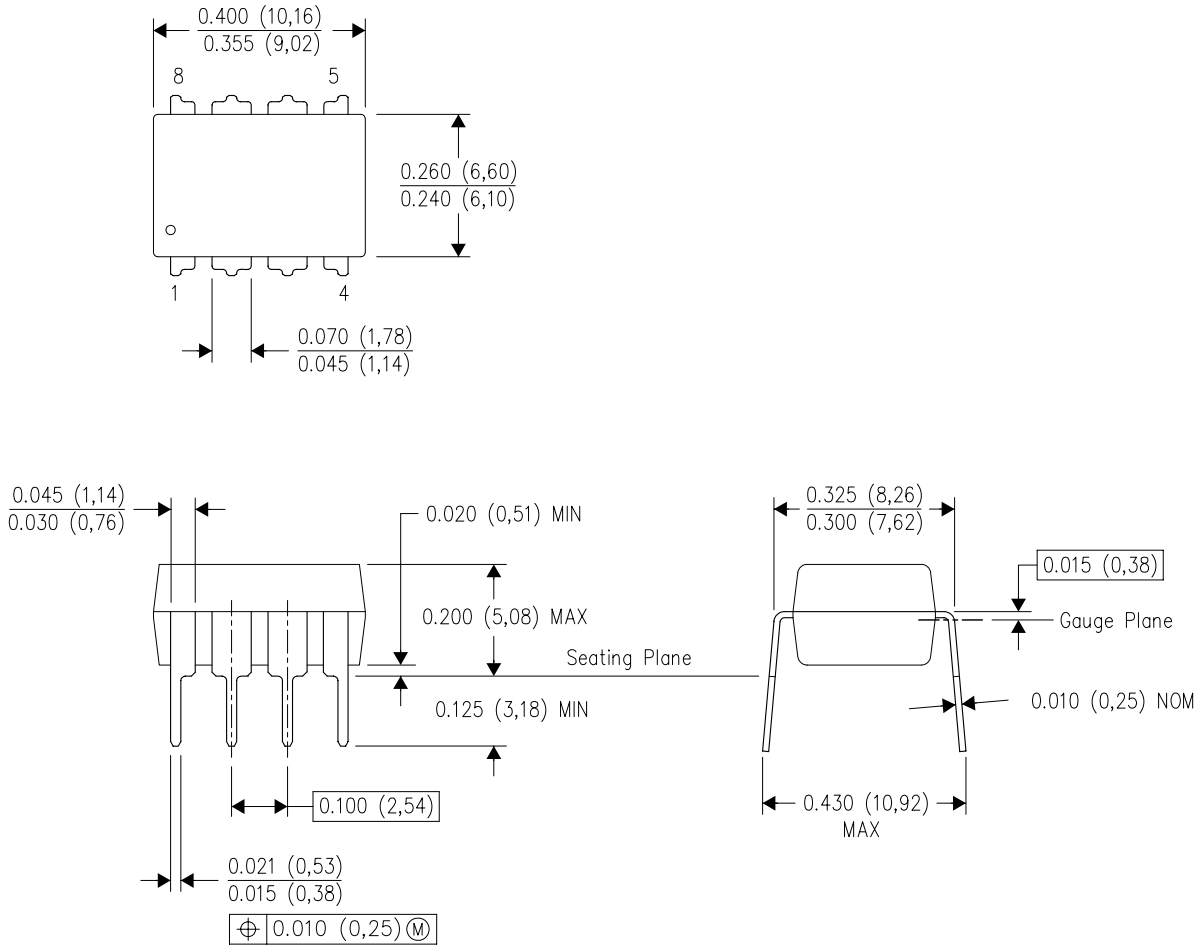
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



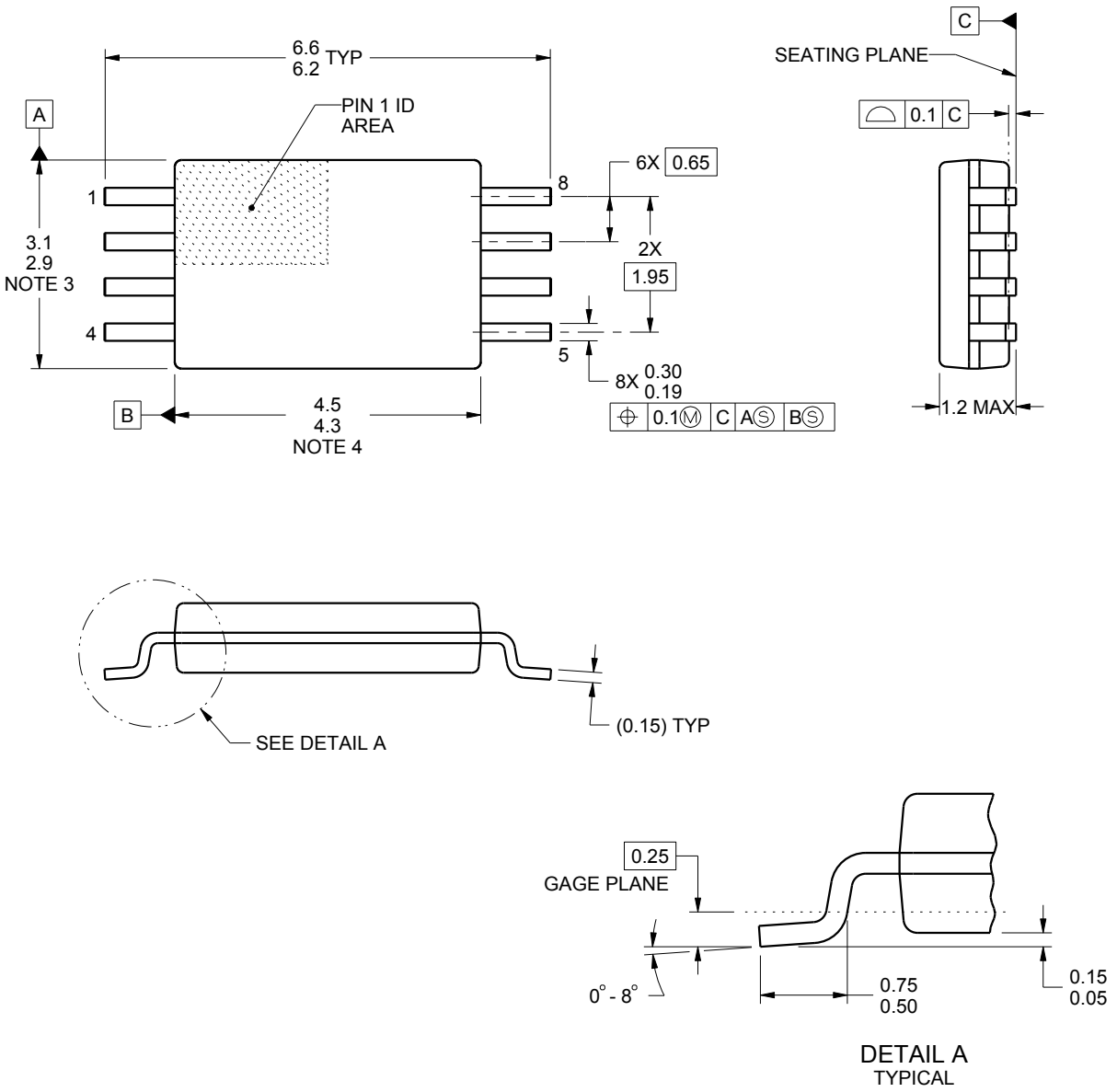
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

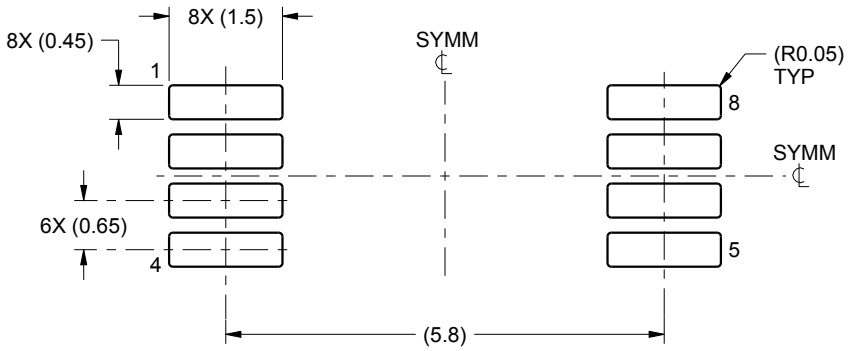
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

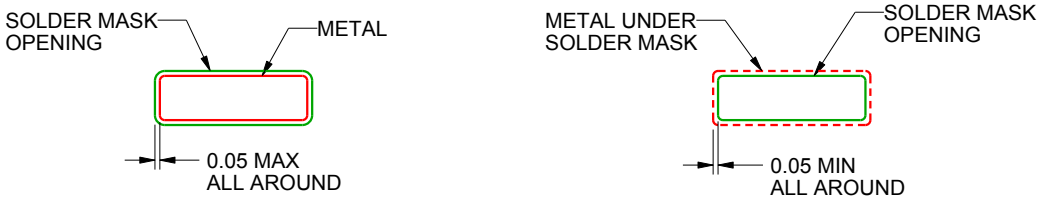


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

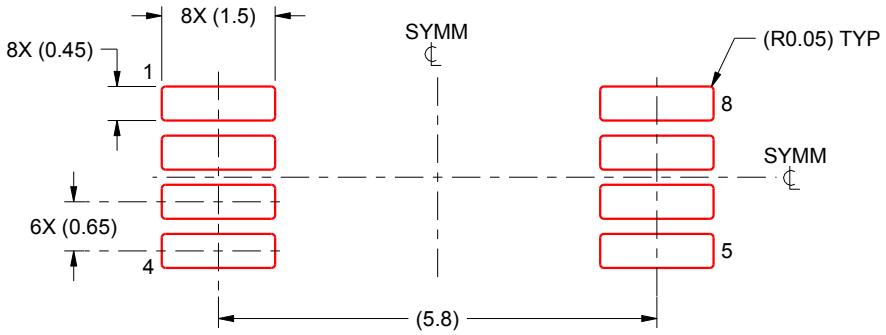


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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