



**THE DATASHEET OF  
MM74HC251N**



## MM74HC251 8-Channel 3-STATE Multiplexer

### General Description

The MM74HC251 8-channel digital multiplexer with 3-STATE outputs utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and 3-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is HIGH, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed

to the Y and W outputs. The 74HC logic family is speed, function, as well as pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### Features

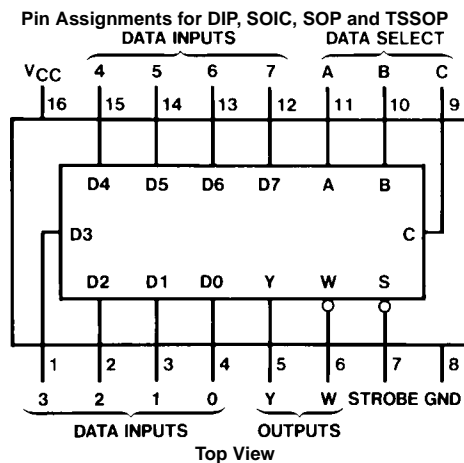
- Typical propagation delay  
Data select to Y: 26 ns
- Wide supply range: 2–6V
- Low power supply quiescent current:  
80  $\mu$ A maximum (74HC)
- 3-STATE outputs for interface to bus oriented systems

### Ordering Code:

Order Number	Package Number	Package Description
MM74HC251M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC251SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC251MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC251N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

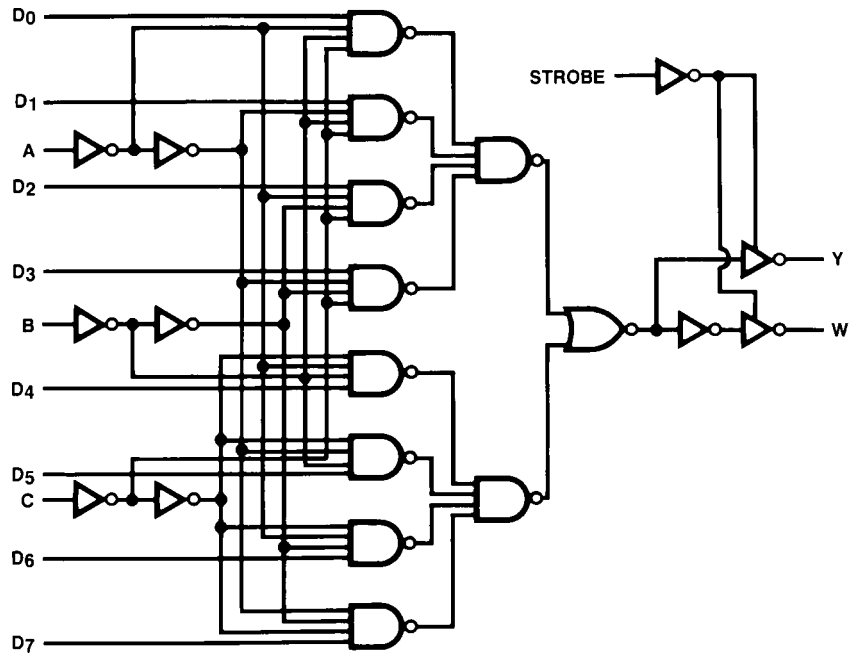


## Truth Table

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = HIGH Logic Level, L = LOW Logic Level  
 X = Irrelevant, Z = High Impedance (off)  
 D0, D1, . . . D7 = The level of the respective D input

## Logic Diagram





## AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15$  pF,  $t_r = t_f = 6$  ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay A, B or C to Y		26	35	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, A, B or C to W		27	35	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Any D to Y		22	29	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Any D to W		24	32	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time, W Output	$R_L = 1$ k $\Omega$ $C_L = 50$ pF	19	27	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time, Y Output	$R_L = 1$ k $\Omega$ $C_L = 50$ pF	19	26	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time W Output	$R_L = 1$ k $\Omega$ $C_L = 5$ pF	26	40	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time Y Output	$R_L = 1$ k $\Omega$ $C_L = 5$ pF	27	35	ns

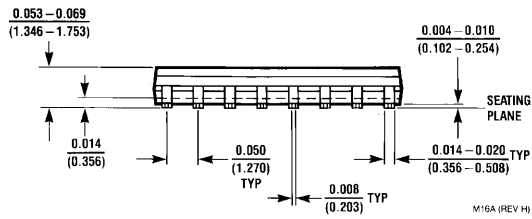
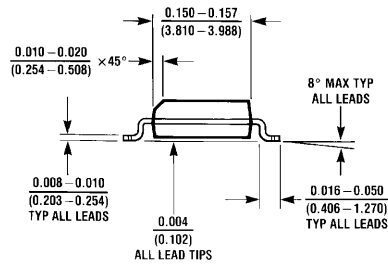
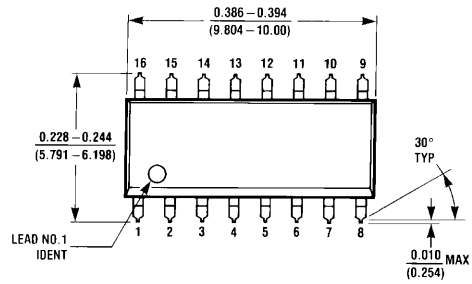
## AC Electrical Characteristics

$C_L = 50$  pF,  $t_r = t_f = 6$  ns (unless otherwise specified)

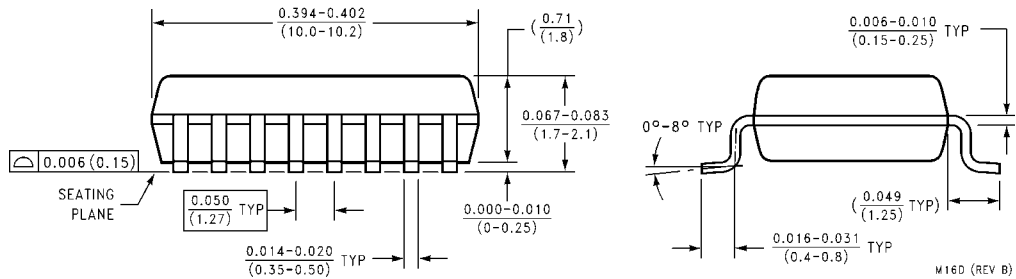
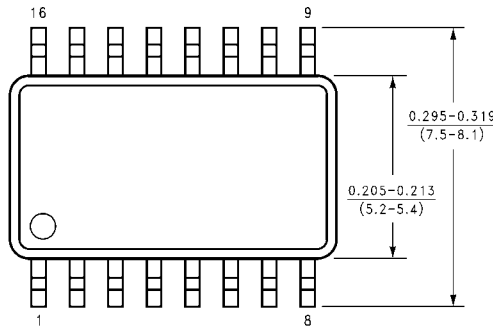
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
				Typ	Guaranteed Limits			
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay A, B or C to Y		2.0V	90	205	256	300	ns
			4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, A, B or C to W		2.0V	95	205	256	300	ns
			4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, any D to Y		2.0V	70	195	244	283	ns
			4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, any D to W		2.0V	75	185	231	268	ns
			4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time W Output	$R_L = 1$ k $\Omega$	2.0V	45	150	188	218	ns
			4.5V	21	30	38	44	ns
			6.0V	18	26	33	38	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time Y Output	$R_L = 1$ k $\Omega$	2.0V	45	145	181	210	ns
			4.5V	21	29	36	42	ns
			6.0V	18	25	31	36	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time W Output	$R_L = 1$ k $\Omega$	2.0V	60	220	275	319	ns
			4.5V	29	44	55	64	ns
			6.0V	25	37	46	54	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time Y Output	$R_L = 1$ k $\Omega$	2.0V	60	195	244	283	ns
			4.5V	30	39	49	57	ns
			6.0V	26	33	41	48	ns
$t_{THL}$ , $t_{TLH}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted

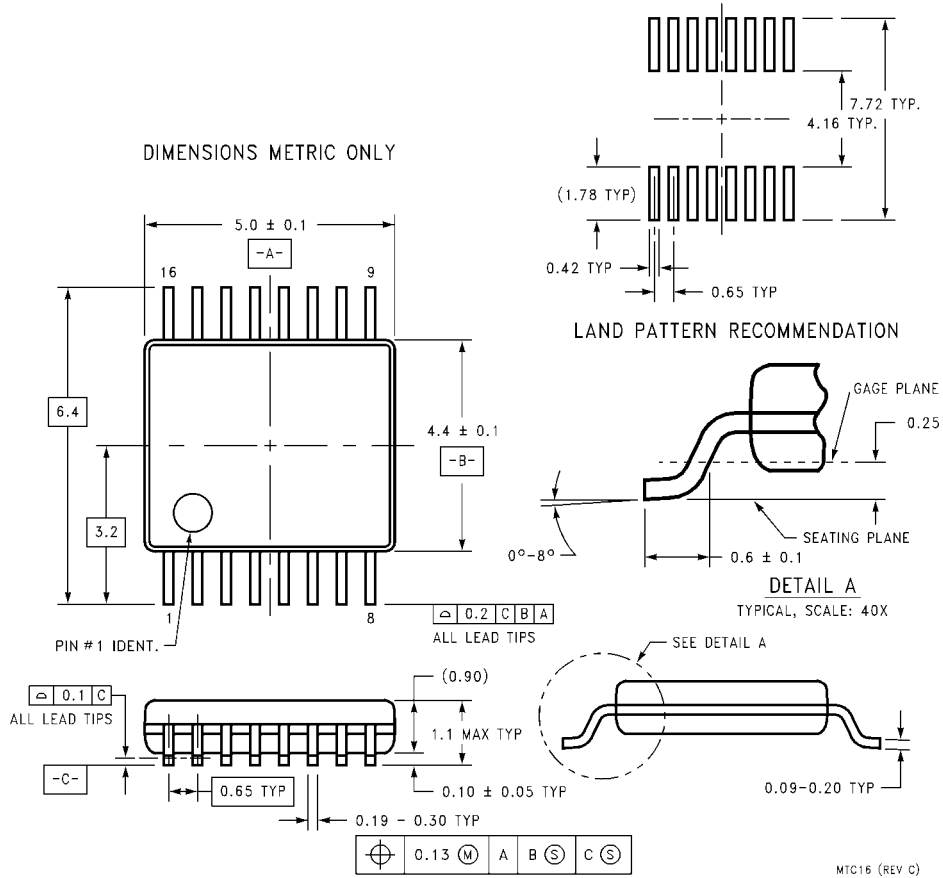


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**



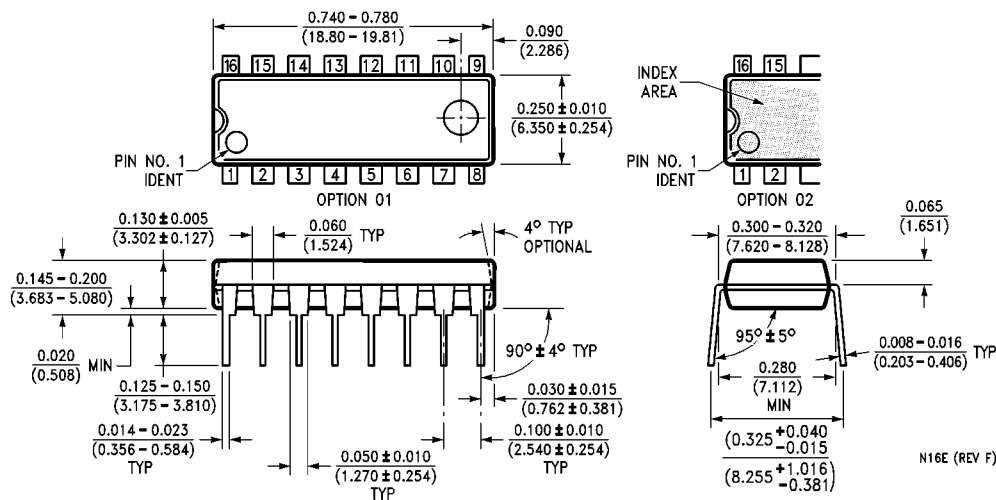
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16A**

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