THE DATASHEET OF

NCP1530DM27R2

www.win-source.net 0086-755-83957316

NCP1530

600 mA PWM/PFM Step-Down Converter with External Synchronization Pin

The NCP1530 is a PWM/PFM non−synchronous step−down (Buck) DC−DC converter for usage in systems supplied from 1−cell Li−ion, or 2 or more cells Alkaline/NiCd/NiMH batteries. It can operate in Constant−Frequency PWM mode or PWM/PFM mode in which the controller will automatically switch to PFM mode operation at low output loads to maintain high efficiency. The switching frequency can also be synchronized to external clock between 600 kHz and 1.2 MHz. The maximum output current is up to 600 mA. Applying an external synchronizing signal to SYN pin can supersede the PFM operation.

The NCP1530 consumes only 47 μA (typ) of supply current (V_{OUT} = 3.0 V, no switching) and can be forced to shutdown mode by bringing the enable input (EN) low. In shutdown mode, the regulator is disabled and the shutdown supply current is reduced to 0.5 μA (typ). Other features include built−in undervoltage lockout, internal thermal shutdown, an externally programmable soft−start time and output current limit protection. The NCP1530 operates from a maximum input voltage of 5.0 V and is available in a space saving, low profile Micro8™ package.

Features

- Pb−Free Package is Available
- High Conversion Efficiency, up to 92% at V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 300 mA
- Current−Mode PWM Control
- Automatic PWM/PFM Mode for Current Saving at Low Output Loads
- Internal Switching Transistor Support 600 mA Output Current (V_{IN} = 5.0 V, V_{OUT} = 3.3 V)
- High Switching Frequency (600 kHz), Support Small Size Inductor and Capacitor, Ceramic Capacitors Can be Used
- Synchronize to External Clock Signal up to 1.2 MHz
- 100% Duty Cycle for Maximum Utilization of the Supply Source
- Programmable Soft−Start Time through External Chip Capacitor
- Externally Accessible Voltage Reference
- Built−In Input Undervoltage Lockout
- Built−In Output Overvoltage Protection
- Power Saving Shutdown Mode
- Space Saving, Low Profile Micro8 Package

Typical Applications

- PDAs
- Digital Still Camera
- Cellular Phone and Radios
- Portable Test Equipment
- Portable Scanners
- Portable Audio Systems

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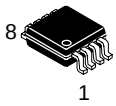
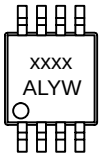
http://onsemi.com

MARKING DIAGRAM

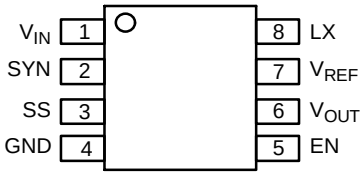


Micro8™
DM SUFFIX
CASE 846A



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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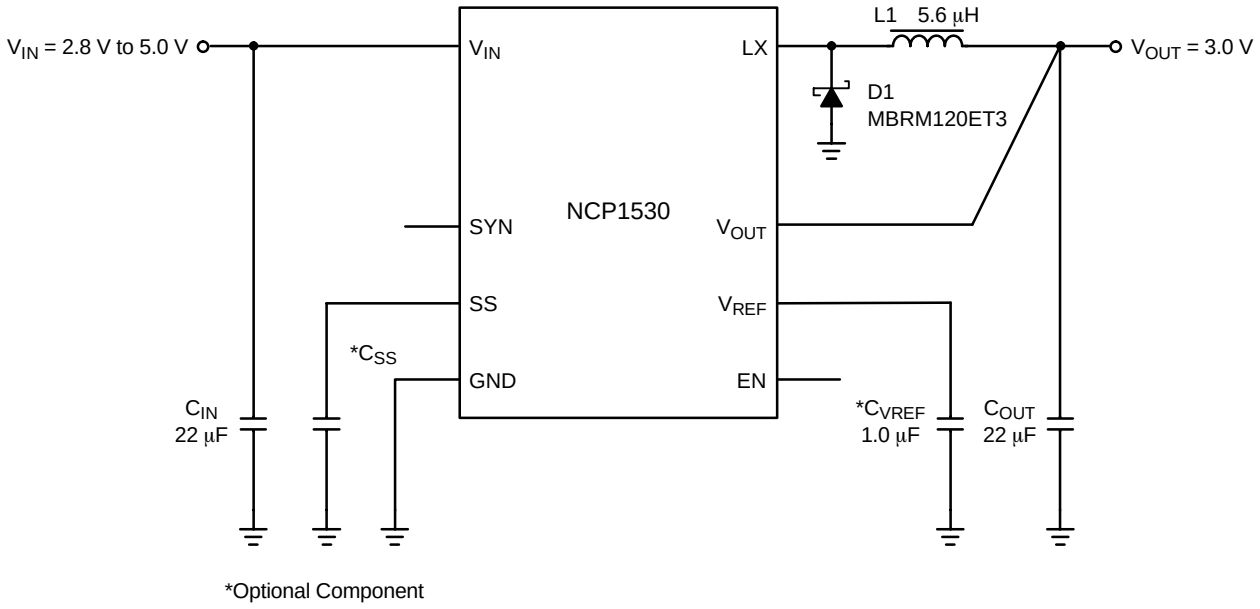


Figure 1. Typical Step−Down Converter Application

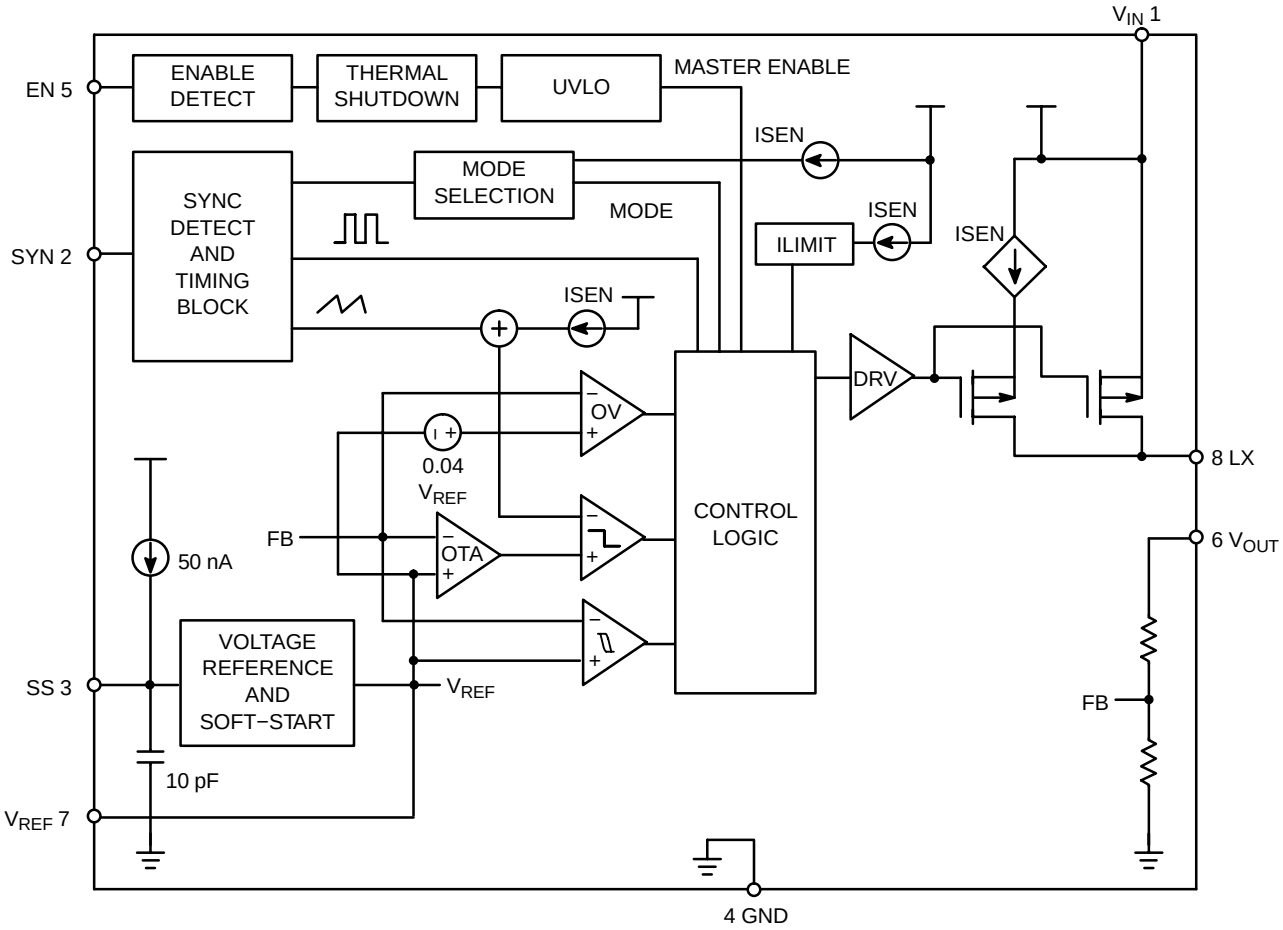


Figure 2. Simplified Functional Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	V_{IN}	Unregulated Supply Input.
2	SYN	Oscillator Synchronization and Mode Selection Input. SYNC = GND (Automatic PWM/PFM mode) The converter operates at 600 kHz fixed−frequency PWM mode primarily, and automatically switches to variable−frequency PFM mode at small output loads for power saving. SYNC = V_{IN} (Constant−Frequency PWM mode) The converter operates at 600 kHz fixed−frequency PWM mode always. SYNC = External clock signal between 600 to 1200 kHz. The converter will be synchronized with the external clock signal. The SYNC pin is internally pulled to GND.
3	SS	Soft−Start Timing control pin. An external soft−start capacitor can be connected to this pin if extended soft−start is required. A 50 nA current will be sourced from this pin to charge up the capacitor during startup and gently ramps the device into service to prevent output voltage overshoot. If this pin is floated, built−in 500 μs (typ.) soft−start will be activated.
4	GND	Ground Terminal.
5	EN	Active−High Enable Input. Active to enable the device. Bring this pin to GND and the quiescent current is reduced to less than 0.5 μA. This pin is internally pulled to V_{IN}.
6	V_{OUT}	Feedback Terminal. The output voltage is sensed by this pin.
7	V_{REF}	Connected to voltage reference decoupling capacitor. For noise non−sensitive applications, the internal voltage reference can operate without decoupling capacitor.
8	LX	Inductor Terminal. This pin is connected to the drains of the internal P−channel switching transistors. The inductor must be connected between this pin and the output terminal.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (Pin 1)	V_{IN}	−0.3 to 6	V
Input/Output Pins (Pins 2−4 & Pins 7−8)	V_{IO}	−0.3 to 6	V
Thermal Characteristics Micro8 Plastic Package Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	240	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
2. Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (V_{IN} = V_R + 1.0 V, test circuit, refer to Figure 1, C_{SS} = NC and C_{VREF} = 1.0 μF, T_A = 25°C for typical value, 0°C ≤ T_A ≤ 85°C for min/max values unless otherwise noted.) *V_R is the factory−programmed output voltage setting.

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{IN}	1.1 V_R	−	5.0	V
Output Voltage (I_{load} = 150 mA, V_R + 1.0 V < V_{IN} < 5.0 V) (Note 4) NCP1530DM25R2 NCP1530DM27R2 NCP1530DM30R2 NCP1530DM33R2	V_{OUT}	 2.425 2.619 2.910 3.201	 2.5 2.7 3.0 3.3	 2.575 2.781 3.090 3.399	V
Maximum Output Current (V_{IN} = 5.0 V, V_{OUT} = 3.0 V) (Note 5)	$I_{OUT(max)}$	600	−	−	mA
Supply Current (V_{IN} = V_R + 1.0 V, No Load, EN and SYN Pins NC)	I_{IN}	−	45	95	μA
Shutdown Supply Current (V_{IN} = 5.0 V, No Load, V_{EN} = 0 V)	I_{SHDN}	−	0.5	1.0	μA
LX Pin Leakage Current (No Load, V_{EN} = 0 V)	I_{LX}	−	−	1.0	μA
Internal P−FET ON Resistance at LX Pin (V_{IN} = V_R + 1.0 V, I_{Load} = 150 mA)	$R_{DS(ON)}$	−	0.3	0.5	Ω
Oscillator Frequency (V_{IN} = V_{EN} = V_R + 1.0 V, I_{Load} = 100 mA, SYN Pin NC)	f_{OSC}	480	600	720	kHz
Maximum PWM Duty Cycle (Note 5)	$D_{MAX−PWM}$	−	−	100	%
PFM to PWM Switch−Over Current Threshold (V_{IN} = 4.5 V, SYN Pin NC, L = 5.6 μH, C_{OUT} = 22 μF) (Note 5) NCP1530DM25R2 NCP1530DM27R2 NCP1530DM30R2 NCP1530DM33R2	$I_{PFM−PWM}$	 − − − −	 83 90 100 102	 − − − −	mA
PWM to PFM Switch−Over Current Threshold (V_{IN} = 4.5 V, SYN Pin NC, L = 5.6 μH, C_{OUT} = 22 μF) (Note 5) NCP1530DM25R2 NCP1530DM27R2 NCP1530DM30R2 NCP1530DM33R2	$I_{PWM−PFM}$	 − − − −	 27 38 39 48	 − − − −	mA
Input Undervoltage Lockout Threshold	V_{UVLO}	−	2.0	2.45	V
Reference Voltage (V_{IN} = V_R + 1.0 V, C_{VREF} = 1.0 μF)	V_{REF}	1.184	1.20	1.216	V
Reference Voltage Temperature Coefficient (V_{IN} = V_R + 1.0 V, C_{VREF} = 1.0 μF) (Note 5)	TC_{VREF}	−	0.03	−	mV/°C
Reference Voltage Load Current (V_{IN} = V_R + 1.0 V, C_{VREF} = 1.0 μF) (Note 6)	I_{VREF}	5.0	−	−	mA
Enable Logic High Threshold Voltage (V_{IN} = V_R + 1.0 V, I_{Load} = 0 mA)	$V_{EN−H}$	−	1.5	1.85	V
Enable Logic Low Threshold Voltage (V_{IN} = V_R + 1.0 V, I_{Load} = 0 mA)	$V_{EN−L}$	0.5	1.2	−	V
PWM Minimum On−Time (Note 5)	$t_{PWM−ON}$	−	100	−	ns
PWM OV Protection Level	$\%V_{OV}$	−	6.0	12	%
PWM Cycle−by−Cycle Current Limit (Note 5)	I_{LIM}	−	1.5	−	A
Built−in Soft−Start Time (V_{OUT} = 3.0 V, SS Pin NC) (Note 5)	t_{SS}	−	500	−	μs
Thermal Shutdown Threshold (V_{IN} = 3.5 V, I_{Load} = 0 mA) (Note 5)	TH_{SHD}	−	145	−	°C
Thermal Shutdown Hysteresis (V_{IN} = 3.5 V, I_{Load} = 0 mA) (Note 5)	TH_{HSYS}	−	15	−	°C

4. Tested at V_{IN} = V_R + 1.0 V in production only. Full V_{IN} range guaranteed by design.
5. Parameter guaranteed by design only, not tested in production.
6. Loading capability decreases with V_{OUT} decreases.

TYPICAL OPERATING CHARACTERISTICS (V_{IN} = V_R + 1.0 V, test circuit, refer to Figure 1, C_{SS} = NC and C_{VREF} = 1.0 μF, T_A = 25°C for typical value, 0°C ≤ T_A ≤ 85°C for min/max values unless otherwise noted.) *V_R is the factory−programmed output voltage setting.

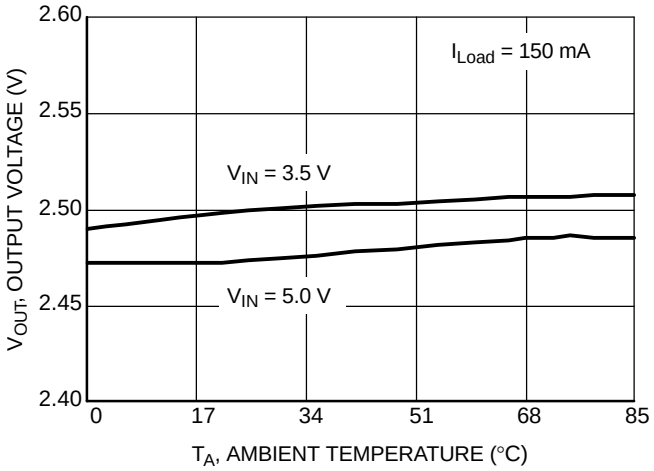


Figure 3. Output Voltage vs. Ambient Temperature (V_{OUT} = 2.5 V)

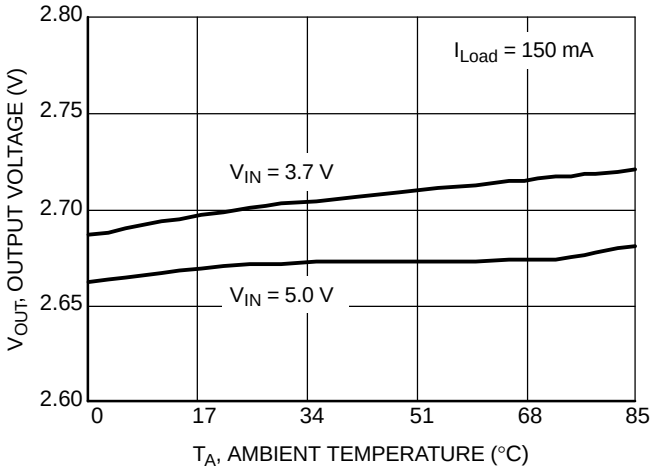


Figure 4. Output Voltage vs. Ambient Temperature (V_{OUT} = 2.7 V)

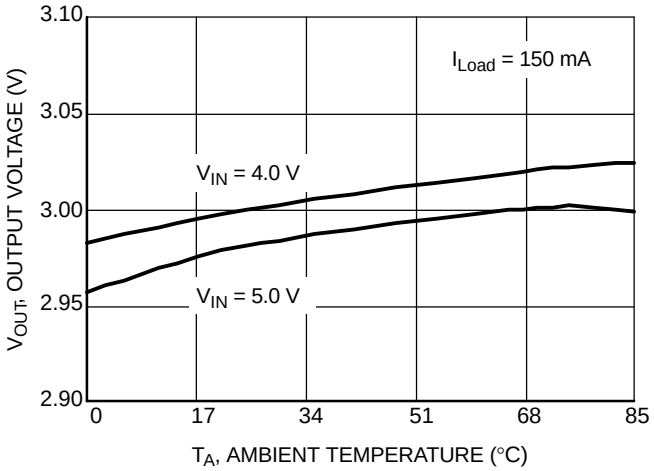


Figure 5. Output Voltage vs. Ambient Temperature (V_{OUT} = 3.0 V)

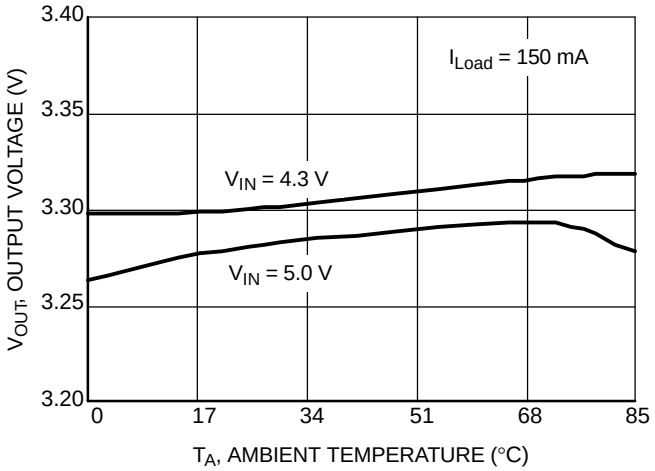


Figure 6. Output Voltage vs. Ambient Temperature (V_{OUT} = 3.3 V)

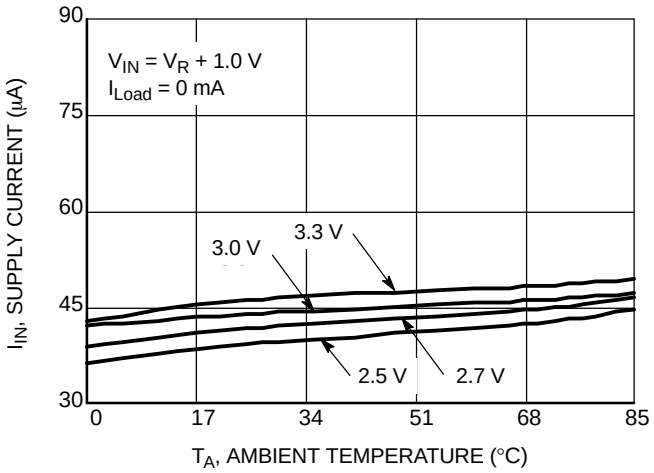


Figure 7. Supply Current vs. Ambient Temperature

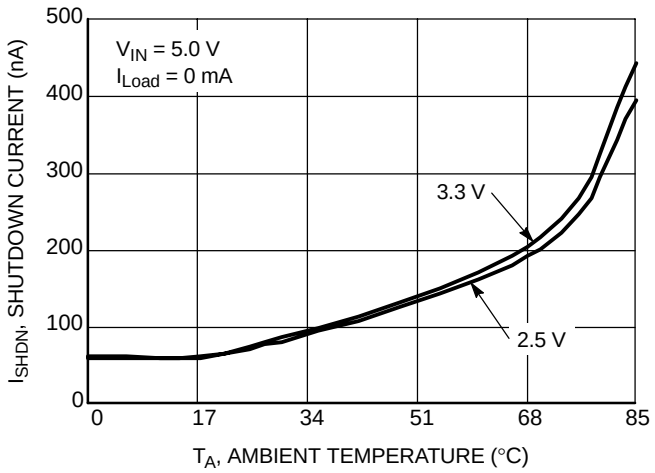


Figure 8. Shutdown Current vs. Ambient Temperature

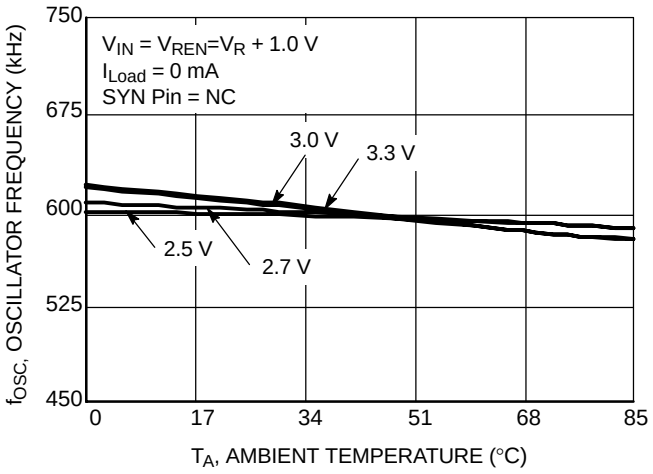


Figure 9. Oscillator Frequency vs. Ambient Temperature

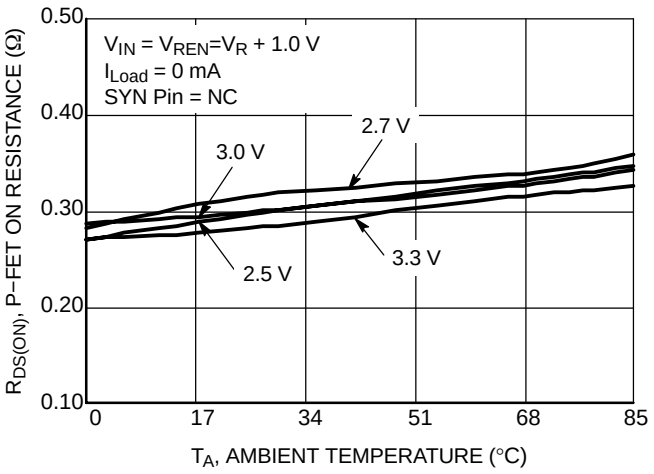


Figure 10. P−FET ON Resistance vs. Ambient Temperature

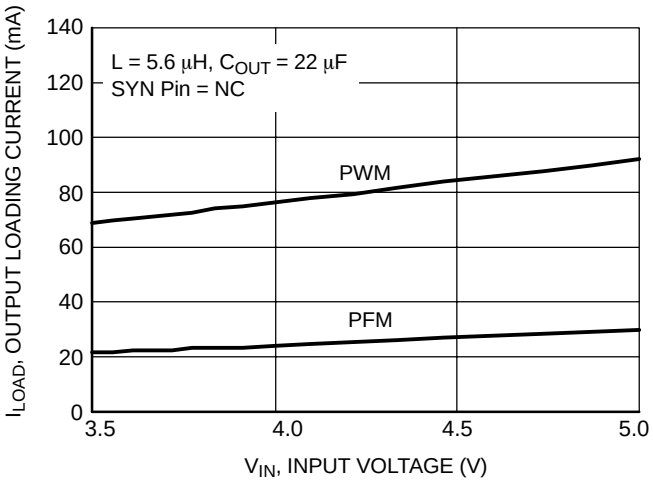


Figure 11. PWM/PFM Switchover Current Thresholds vs. Input Voltage (V_{OUT} = 2.5 V)

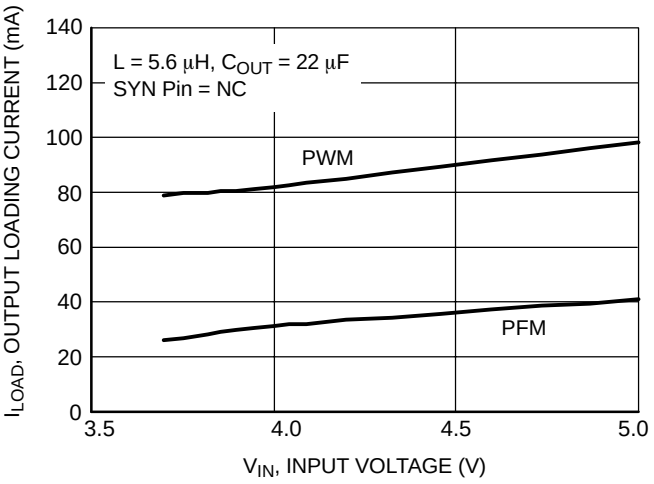


Figure 12. PWM/PFM Switchover Current Thresholds vs. Input Voltage (V_{OUT} = 2.7 V)

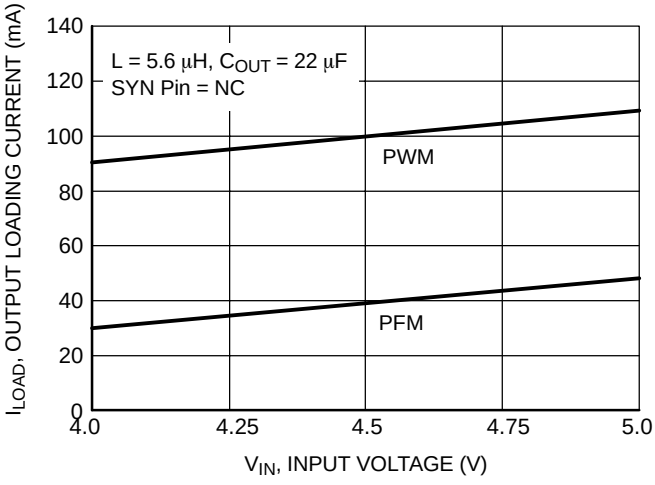


Figure 13. PWM/PFM Switchover Current Thresholds vs. Input Voltage (V_{OUT} = 3.0 V)

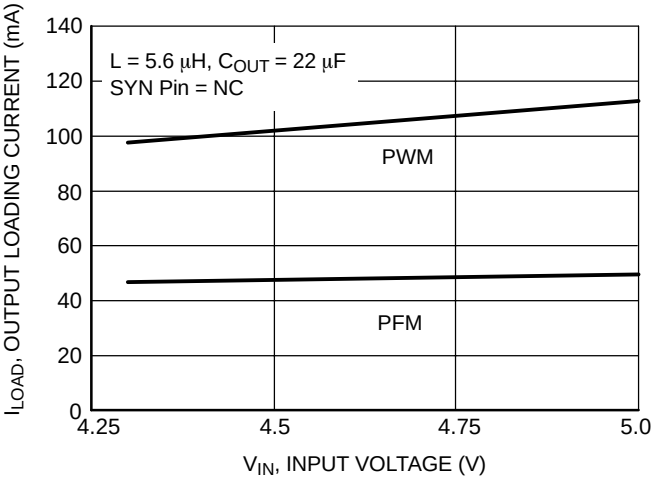


Figure 14. PWM/PFM Switchover Current Thresholds vs. Input Voltage (V_{OUT} = 3.3 V)

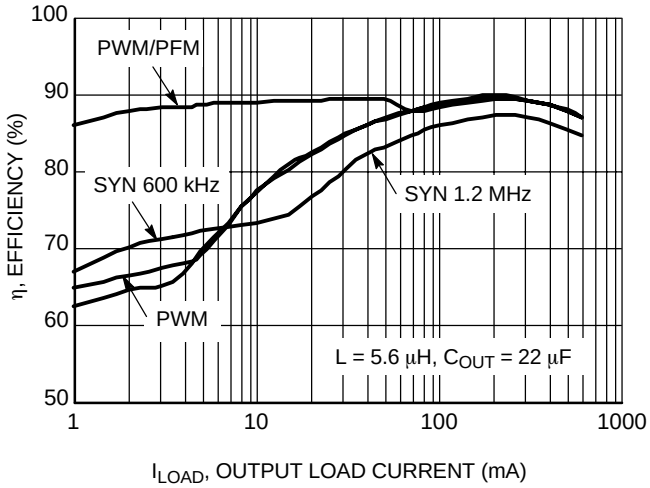


Figure 15. Efficiency vs. Output Load Current (V_{IN} = 3.5 V, V_{OUT} = 2.5 V)

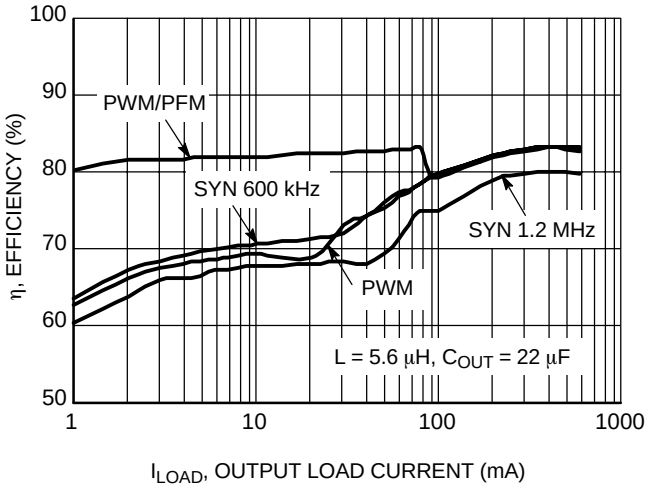


Figure 16. Efficiency vs. Output Load Current (V_{IN} = 5.0 V, V_{OUT} = 2.5 V)

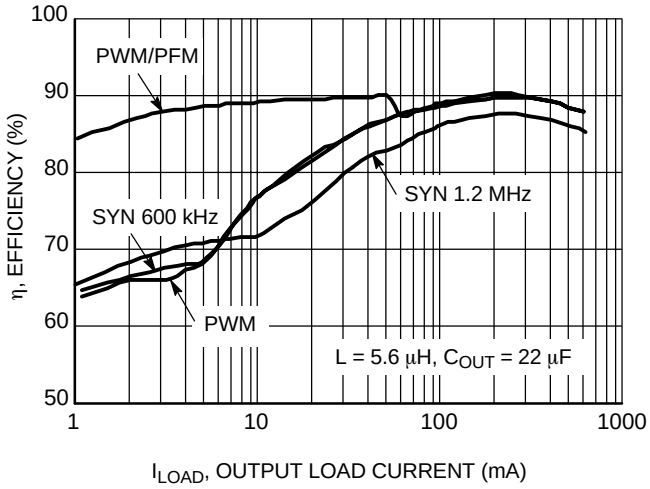


Figure 17. Efficiency vs. Output Load Current (V_{IN} = 3.7 V, V_{OUT} = 2.7 V)

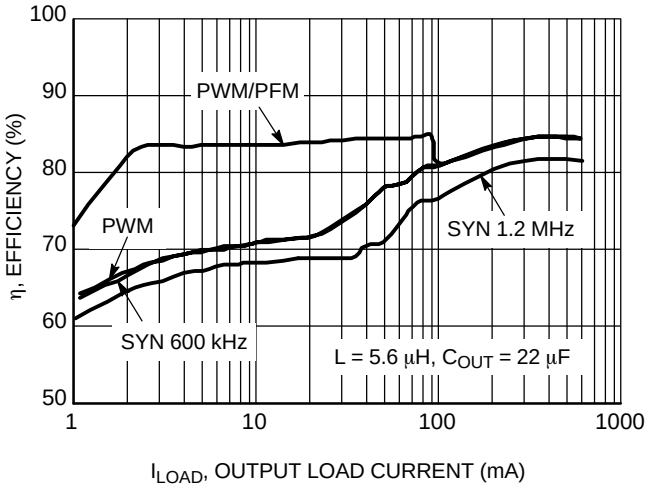


Figure 18. Efficiency vs. Output Load Current (V_{IN} = 5.0 V, V_{OUT} = 2.7 V)

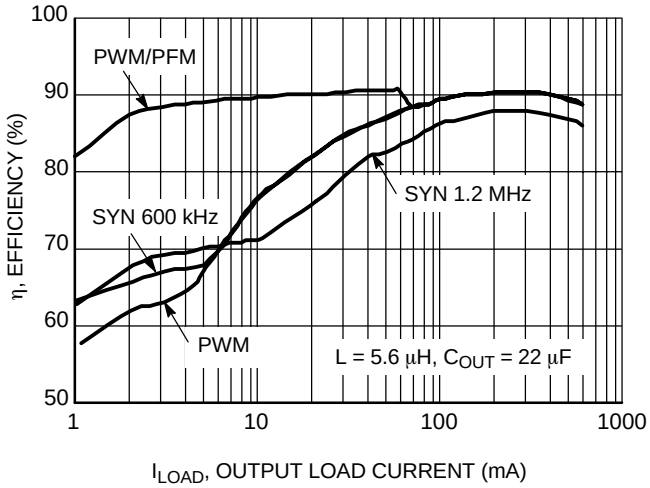


Figure 19. Efficiency vs. Output Load Current (V_{IN} = 4.0 V, V_{OUT} = 3.0 V)

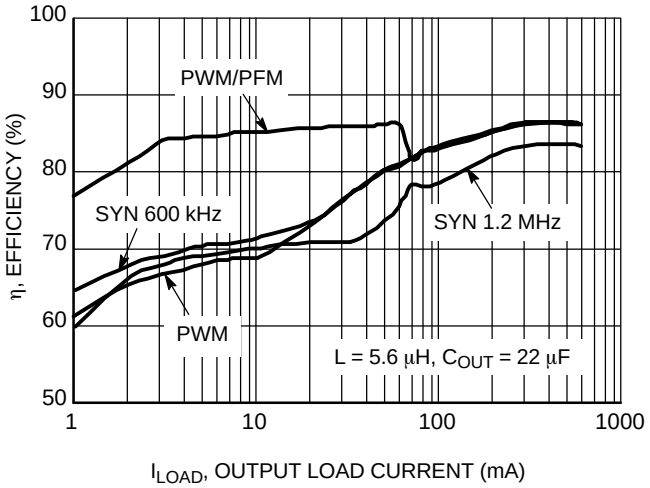


Figure 20. Efficiency vs. Output Load Current (V_{IN} = 5.0 V, V_{OUT} = 3.0 V)

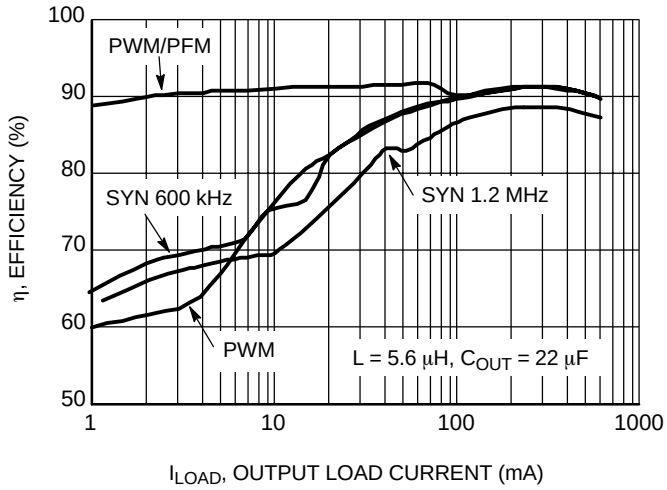


Figure 21. Efficiency vs. Output Load Current (V_{IN} = 4.3 V, V_{OUT} = 3.3 V)

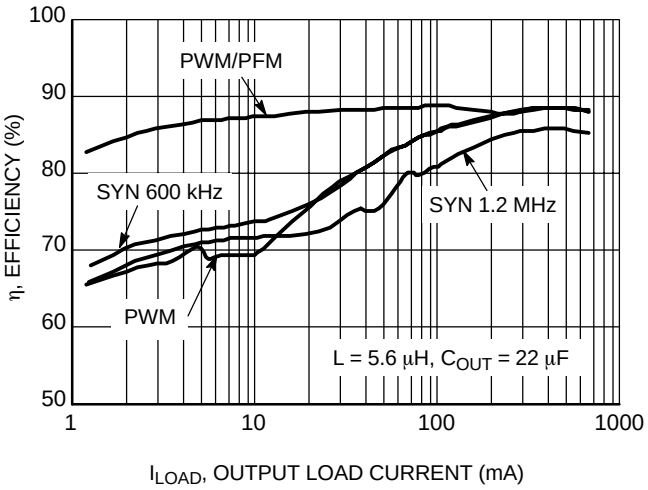


Figure 22. Efficiency vs. Output Load Current (V_{IN} = 5.0 V, V_{OUT} = 3.3 V)

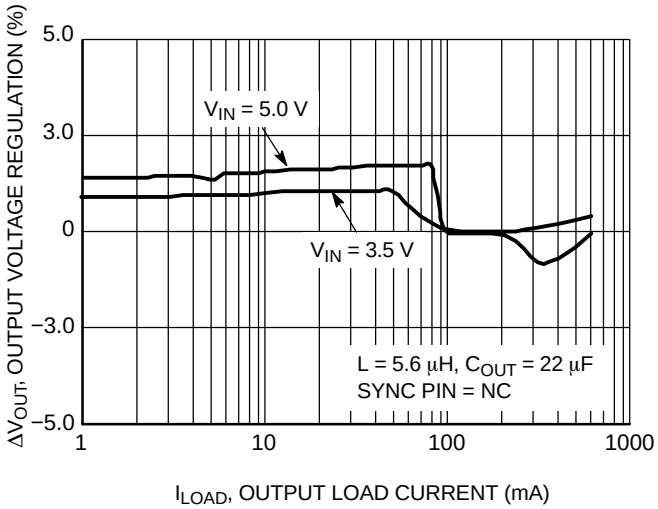


Figure 23. Output Voltage Regulation vs. Output Load Current (V_{OUT} = 2.5 V)

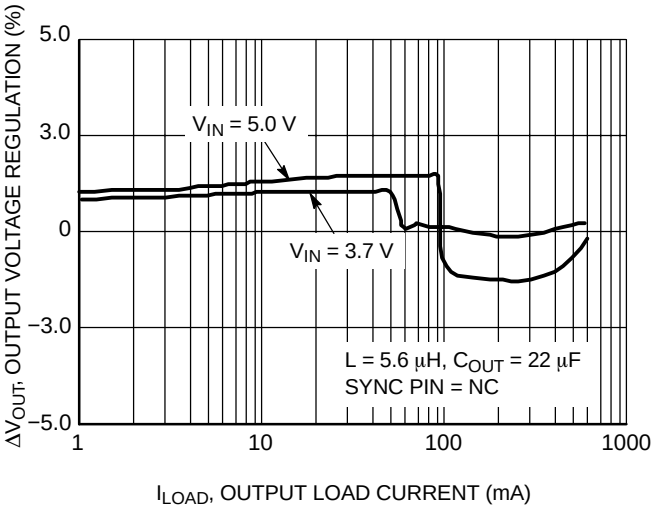


Figure 24. Output Voltage Regulation vs. Output Load Current (V_{OUT} = 2.7 V)

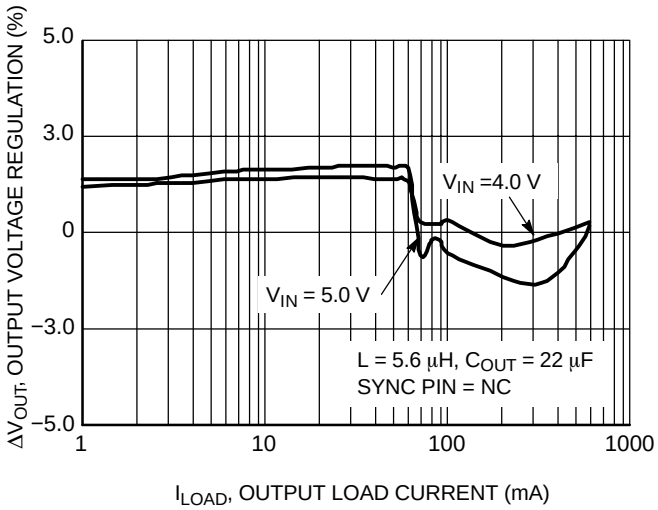


Figure 25. Output Voltage Regulation vs. Output Load Current (V_{OUT} = 3.0 V)

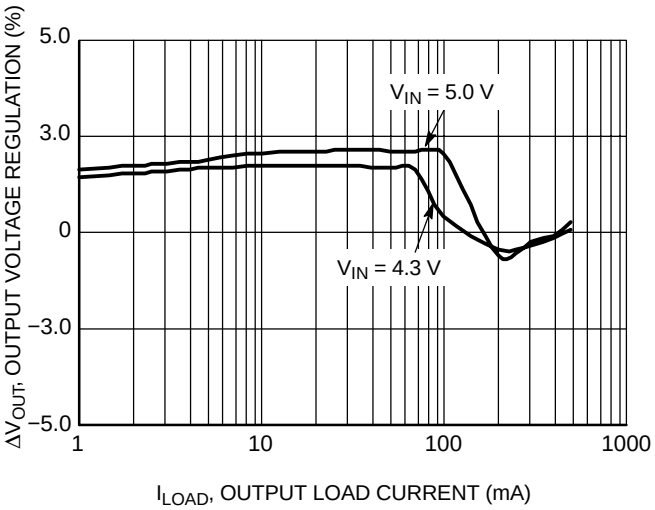
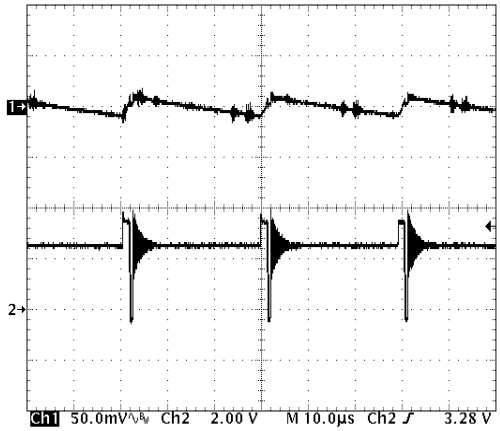
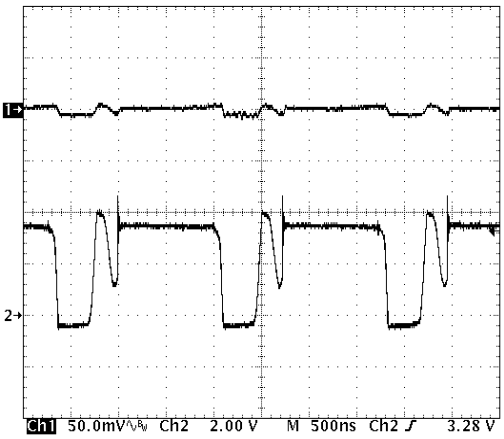


Figure 26. Output Voltage Regulation vs. Output Load Current (V_{OUT} = 3.3 V)



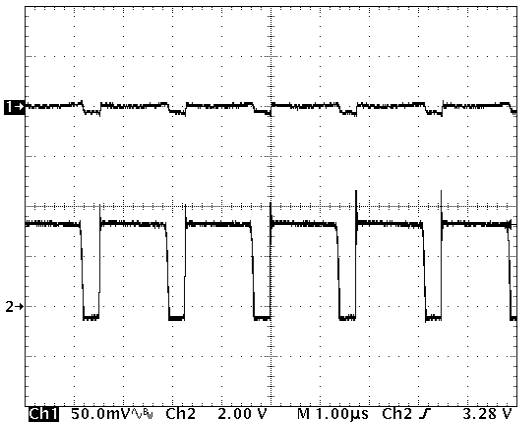
(V_{IN} = 3.5 V, V_{OUT} = 2.5 V, I_{LOAD} = 10 mA)
Upper Trace: Output Voltage Ripple, 50 mVac/Div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/Div.

Figure 27. PFM Switching Waveform and Output Ripple for V_{OUT} = 2.5 V



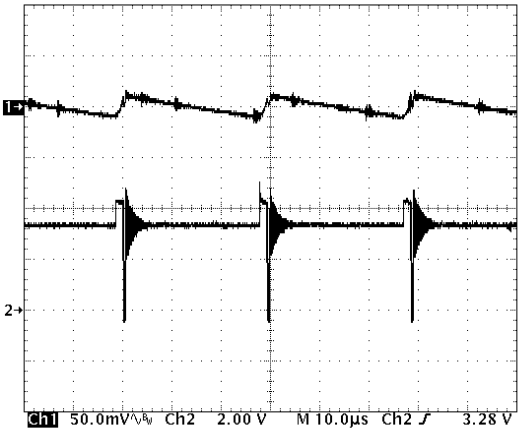
(V_{IN} = 3.5 V, V_{OUT} = 2.5 V, I_{LOAD} = 80 mA)
Upper Trace: Output Voltage Ripple, 50 mVac/Div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/Div.

Figure 28. DCM PWM Switching Waveform and Output Ripple for V_{OUT} = 2.5 V



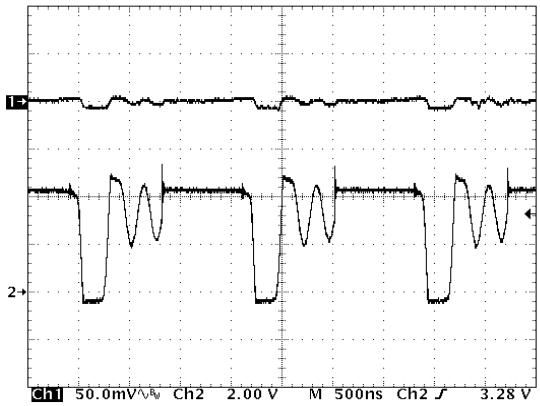
(V_{IN} = 3.5 V, V_{OUT} = 2.5 V, I_{LOAD} = 600 mA)
Upper Trace: Output Voltage Ripple, 50 mVac/Div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/Div.

Figure 29. CCM PWM Switching Waveform and Output Ripple for V_{OUT} = 2.5 V



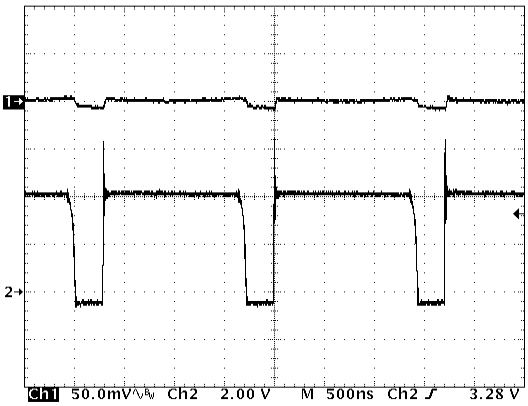
(V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{LOAD} = 10 mA)
Upper Trace: Output Voltage Ripple, 50 mVac/Div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/Div.

Figure 30. PFM Switching Waveform and Output Ripple for V_{OUT} = 3.3 V



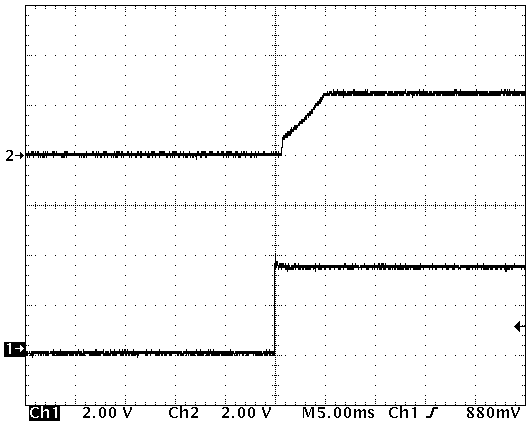
(V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{LOAD} = 50 mA)
Upper Trace: Output Voltage Ripple, 50 mVac/Div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/Div.

Figure 31. DCM PWM Switching Waveform and Output Ripple for V_{OUT} = 3.3 V



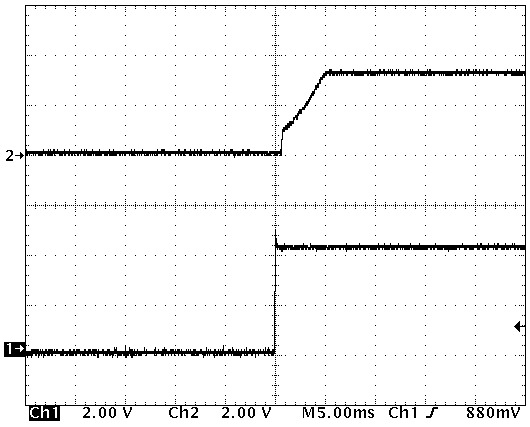
(V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{LOAD} = 600 mA)
Upper Trace: Output Voltage Ripple, 50 mVac/Div.
Lower Trace: LX Pin Switching Waveform, 2.0 V/Div.

Figure 32. CCM PWM Switching Waveform and Output Ripple for V_{OUT} = 3.3 V



(V_{IN} = 3.5 V, V_{OUT} = 2.5 V, C_{SS} = 100 pF, No load)
Upper Trace: Output Voltage, 2.0 V/Div.
Lower Trace: EN Pin Waveform, 2.0 V/Div.
Time Scale: 5.0 ms/Div.

Figure 33. Soft−Start Output Voltage Waveform for V_{OUT} = 2.5 V



(V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{SS} = 100 pF, No load)
Upper Trace: Output Voltage, 2.0 V/Div.
Lower Trace: EN Pin Waveform, 2.0 V/Div.
Time Scale: 5.0 ms/Div.

Figure 34. Soft−Start Output Voltage Waveform for V_{OUT} = 3.3 V

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1530 series are step−down converters with a smart control scheme that operates with 600 kHz fixed Pulse Width Modulation (PWM) at moderate to heavy load currents, so that high efficiency, noise free output voltage can be generated. In order to improve the system efficiency at light loads, this device can be configured to work in auto−mode. In auto−mode operation, the control unit will detect the loading condition and switch to power saving Pulse Frequency Modulation (PFM) control scheme at light load. With these enhanced features, the converter can achieve high operating efficiency for all loading conditions. Additionally, the switching frequency can also be synchronized to external clock signal in between 600 kHz to 1.2 MHz range. The converter uses peak current mode PWM control as a core, with the high switching frequency incorporated. Good line and load regulation can be achieved easily with small value ceramic input and output capacitors. Internal integrated compensation voltage ramp ensures stable operation at all operating modes. NCP1530 series are designed to support up to 600 mA output current with cycle−by−cycle current limit protection.

The Internal Oscillator

The oscillator that governs the switching of the PWM control cycle is self contained and no external timing component is required to setup the switching frequency. For PWM mode and auto−mode operation, all timing signals required for proper operation are derived from the internal oscillator. The internal fix frequency oscillator is trimmed to run at 600 kHz ± 20% over full temperature range. In case the device is forced to operate at Synchronization mode by applying an external clock signal to SYN pin (pin 2), the external clock signal will supersede the internal oscillator and take charge of the switching operation.

Voltage Reference and Soft−Start

An internal high accuracy voltage reference is included in NCP1530. This reference voltage governs all internal reference levels in various functional blocks required for proper operation. This reference voltage is precisely trimmed to 1.2 V ± 1.5% over full temperature range. The reference voltage can be accessed externally at V_{REF} pin (pin 7), with an external capacitor, C_{REF} of 1.0 μF, privding up to 5.0 mA of loading. Additionally, NCP1530 has a Soft−Start circuit built around the voltage reference block that provide limits to the inrush current during start−up by controlling the ramp up of the internal voltage reference. The soft−start time can be user adjusted by an external capacitor, C_{SS}, connecting to the SS pin (pin 3). During converter powerup, a 50 nA current flowing out from the SS pin will charge−up the timing capacitor. The voltage across the SS pin controls the ramp up of the internal reference voltage by slowly releasing it until the nominal value is reached. For an external timing capacitor of value C_{SS} = 100 pF, the soft−start time is about 5.0 ms including the small logic delay time, Figure 33 and 34. In the case where the SS pin is left floating, a small built−in capacitor together with other parasitic capacitance will provide a minimum intrinsic soft−start time of 500 μs. As the soft−start function is implemented by simple circuitry, the final timing depends on non−linear functions, where accurate deterination of the soft−start timing is impossible. However, for simplicity, the empirical formula below can be used to estimate the soft−start time with respect to the value of the external capacitor.

$$t_{SS}\ \text{in}\ \mu s \approx 50 \times C_{SS}\ \text{in}\ pF + 500\ \mu s$$

Current Mode Pulse−Width Modulation (PWM) Control Scheme

With the SYN pin (pin 2) connected to V_{IN}, the converter will set to operate at constant switching frequency PWM mode. NCP1530 uses peak current mode control scheme to achieve good line and load regulation. The high switching frequency, 600 kHz, and a carefully compensated internal control loop, allows the use of low profile small value ceramic type input and output capacitor for stable operation. In current mode operation, the required ramp function is generated by sensing the inductor current (ISEN) and comparing with the voltage loop error amplifier (OTA) output. The OTA output is derived from feedback from the output voltage pin (V_{OUT} − Pin 6) and the internal reference voltage (V_{REF} − Pin 7). See Figure 2. On a cycle−by−cycle basis, the duty cycle is controlled to keep the output voltage within regulation. The current mode approach has outstanding line regulation performance and good overall system stability. Additionally, by monitoring the inductor current, a cycle−by−cycle current limit protection is implemented. Constant Frequency PWM scheme reduces output ripple and noise, which is one of the important characteristics for noise sensitive communication applications. The high switching frequency allows the use of small size surface mount components that saves significant PC board area and improves layout compactness and EMI performance.

Power Saving Pulse−Frequency−Modulation (PFM) Control Scheme

With the SYN pin (pin 2) connected to ground or left open, the converter will operate in PWM/PFM auto mode. Under this operating mode, NCP1530 will stay in constant frequency PWM operation in moderate to heavy load conditions. When the load decreases down to a threshold point, the operation will switch to the power saving PFM operation automatically. The switchover mechanism depends on the input voltage, output voltage and the inductor current level. The mode change circuit will determine whether the converter should be operated in PWM or PFM mode. In order to maintain stable and smooth switching mode transition, a small hysteresis on the load current level for mode transition was implemented. The detailed mode transition characteristics for each voltage option are illustrated in Figures 11 and 14. PFM mode operation provides high conversion efficiency even at very light loading conditions. In PFM mode, most of the circuits inside the device will be turned off and the converter operates just as a simple voltage hysteretic converter. When the load current increases, the converter returns to PWM mode automatically.

External Synchronization Control

The NCP1530 has an internal fixed frequency oscillator of 600 kHz or can be synchronized to an external clock signal at SYN pin (pin 2). Connecting the SYN pin with an external clock signal will force the converter to operate in a pure PWM mode and the switching frequency will be synchronized. The external clock signal should be in the range of 600 kHz to 1.2 MHz and the pulse width should not be less than 300 ns. The detection of the pulse train is edge sensitive and independent of duty ratio. In the case where the external clock frequency is too low, the detection circuit may not be able to follow and will treat it as a disturbance, thus affecting the converters normal operation. The internal control circuit detects the rising edge of the pulse train and the switching frequency synchronized to the external clock signal. If the external clock signal ceases for several clock cycles, the converter will switch back to use the internal oscillator automatically.

Power Saving Shutdown Mode

NCP1530 can be disabled whenever the EN pin (pin 5) is tied to ground. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. With the device put in shutdown mode, the device current consumption will be as low as 0.5 μA (typ).

Input Undervoltage Lockout Protection (UVLO)

To prevent the P−Channel MOSFETs from operating below safe input voltage levels, an Undervoltage Lockout protection is incorporated in NCP1530. Whenever the input voltage, V_{IN} drops below approximately 2.0 V, the protection circuitry will be activated and the converter operation will be stopped.

Output Overvoltage Protection (OVP)

In order to prevent the output voltage from going to high (when the load current is close to zero in a pure PWM mode and other abnormal conditions), an Output Overvoltage protection circuit is included in the NCP1530. In case the output voltage is higher than its nominal level by more than 12% maximum, the protection circuitry will stop the switching immediately.

Internal Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. The protection will be activated at about 145°C with a hysteresis of 15°C. This feature is provided to prevent failures from unexpected overheating.

Input Capacitor Selection

For a PWM converter operating in continuous current mode, the input current of the converter is a square wave with a duty ratio of approximately V_{OUT}/V_{IN}. The pulsating nature of the input current transient can be a source of EMI noise and system instability. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply. For NCP1530, a low ESR, low profile ceramic capacitor of 22 μF can be used for most of the cases. For effective bypass results, the input capacitor should be placed just next to V_{IN} pin (pin 1) whenever it is possible.

Inductor Value Selection

Selecting the proper inductance for the power inductor is a trade−off between inductor's physical sizes, transient response, power delivering capability, output voltage ripple and power conversion efficiency. Low value inductor saves cost, PC board space and provides fast transient response, however suffers high inductor ripple current, core loss and lower overall conversion efficiency. The relationship between the inductance and the inductor ripple current is given by the equation in below.

$$L = \frac{T_{ON}(V_{IN} - R_{DS(ON)} \times I_{OUT} - V_{OUT})}{I_{L_RIPPLE(P-P)}}$$

Where L is the inductance required;

T_{ON} is the nominal ON time within a switching cycle;

$R_{DS(ON)}$ is the ON resistance of the internal MOSFET;

V_{IN} is the worst−case input voltage;

V_{OUT} is the output voltage;

I_{OUT} is the maximum allowed loading current;

$I_{L_RIPPLE(P-P)}$ is the acceptable inductor current ripple level.

For ease of application, the previous equation was plotted in Figure 35 to help end user to select the right inductor for specific application. As a rule of thumb, the user needs to be aware of the maximum peak inductor current and should be designed not to exceed the saturation limit of the inductor selected. Low inductance can supply higher output current, but suffers higher output ripple and reduced efficiency, but it limits the output current capability. On the other hand, high inductance can improve output ripple and efficiency, at the same time, it also limits the output current capability. One other critical parameter of the inductor is its DC resistance. This resistance can introduce unwanted power loss and hence reduce overall efficiency. The basic rule is selecting an inductor with lowest DC resistance within the board space limitation.

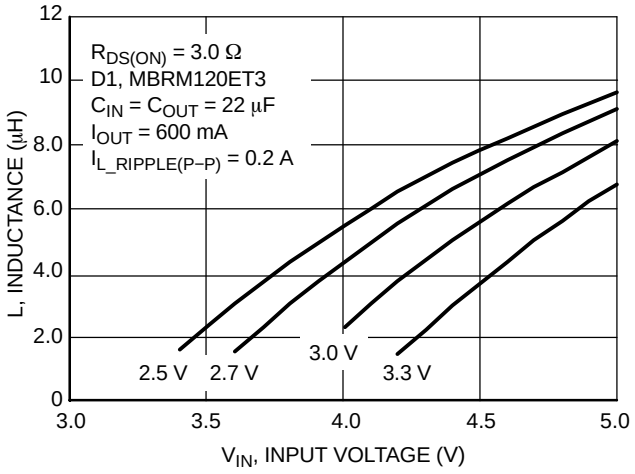


Figure 35. Inductor Selection Chart

Flywheel Diode Selection

The flywheel diode is turned on and carries load current during the off time. At high input voltages, the diode conducts most of the time. In the case where V_{IN} approaches V_{OUT}, the diode conducts only a small fraction of the cycle. While the output terminals are shorted, the diode will be subject to its highest stress. Under this condition, the diode must be able to safely handle the peak current circulating in the loop. So, it is important to select a flywheel diode that can meet the diode peak current and average power dissipation requirements. Under normal conditions, the average current conducted by the flywheel diode is given by,

$$I_D = \frac{V_{IN} - V_{OUT}}{V_{IN} + V_F} \times I_{OUT}$$

Where I_D is the average diode current and V_F is the forward voltage drop of the diode.

A low forward voltage drop and fast switching diode must also be used to optimize converter efficiency. Schottky diodes are a good choice for low forward drop and fast switching times.

Output Capacitor Selection

Selection of the output capacitor, C_{OUT} is primarily governed by the required effective series resistance (ESR) of the capacitor. Typically, once the ESR requirement is met, the capacitance will be adequate for filtering. The output voltage ripple, V_{RIPPLE} is approximated by,

$$V_{RIPPLE} \approx I_{L_RIPPLE(P-P)} \times \left(ESR + \frac{1}{4 \times F_{OSC} C_{OUT}} \right)$$

Where F_{OSC} is the switching frequency and ESR is the effective series resistance of the output capacitor.

From equation in above, it can be noted that the output voltage ripple is contributed to by two parts. For most of the cases, the major contributor is the capacitor's ESR. Ordinary aluminum−electrolytic capacitors have high ESR and should be avoided. High quality Low ESR aluminum−electrolytic capacitors are acceptable and relatively inexpensive. Low ESR tantalum capacitors are another alternative. For even better performance, surface mounted ceramic capacitors can be used. Ceramic capacitors have lowest ESR among all choices. The NCP1530 is internally compensated for stable operation with low ESR ceramic capacitors. However, ordinary multi−layer ceramic capacitors have poor temperature and frequency performance, for switching applications, so only high quality, grade X5R and X7R ceramic capacitors can be used.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedbacks that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

Grounding

Star−ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current flowing through and producing insignificant voltage drop along the path.

Components Placement

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be kept away from the feedback (V_{OUT}, pin 6) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Path

Feedback of the output voltage must be a separate trace separated from the power path. The output voltage sensing trace to the feedback (V_{OUT}, pin 6) pin should be connected to the output voltage directly at the anode of the output capacitor.

ORDERING INFORMATION

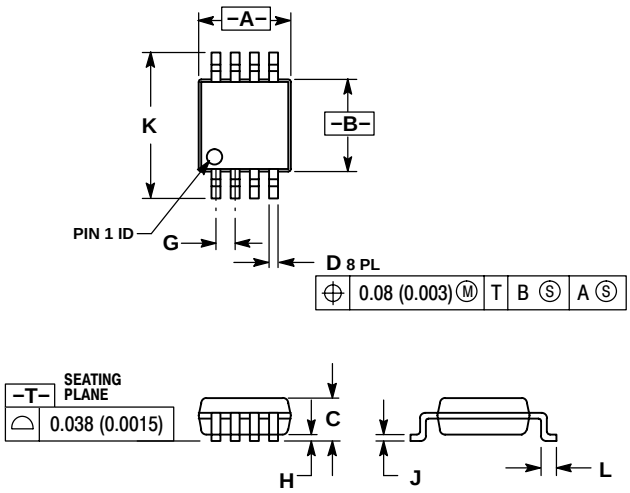
Device	Output Voltage	Device Marking	Package	Shipping†
NCP1530DM25R2	2.5 V	DAAA	Micro8	4000 Units Per 7 Inch Reel
NCP1530DM27R2	2.7 V	DAAB		
NCP1530DM30R2	3.0 V	DAAC		
NCP1530DM30R2G	3.0 V	DAAC	Micro8 (Pb−Free)	
NCP1530DM33R2	3.3 V	DAAD	Micro8	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: The ordering information lists four standard output voltage device options. Additional device with output voltage ranging from 2.5 V to 3.5 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

PACKAGE DIMENSIONS

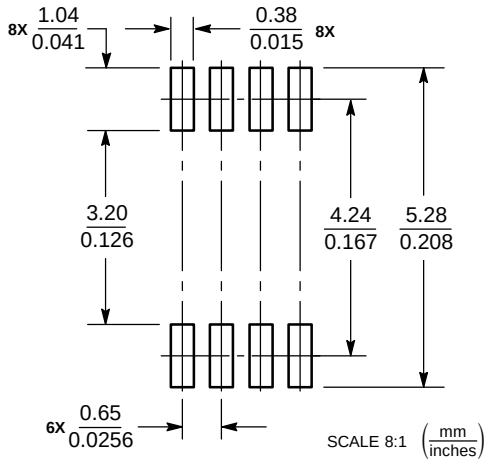
Micro8
DM SUFFIX
CASE 846A−02
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NCP1530/D

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