



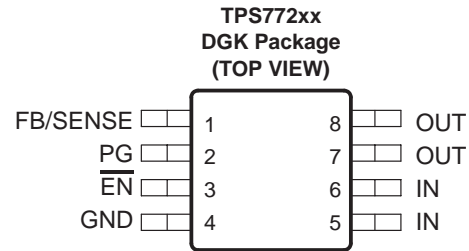
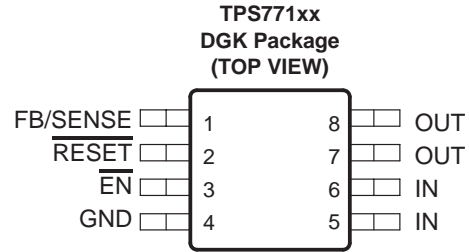
**THE DATASHEET OF
TPS77101QDGKRQ1**



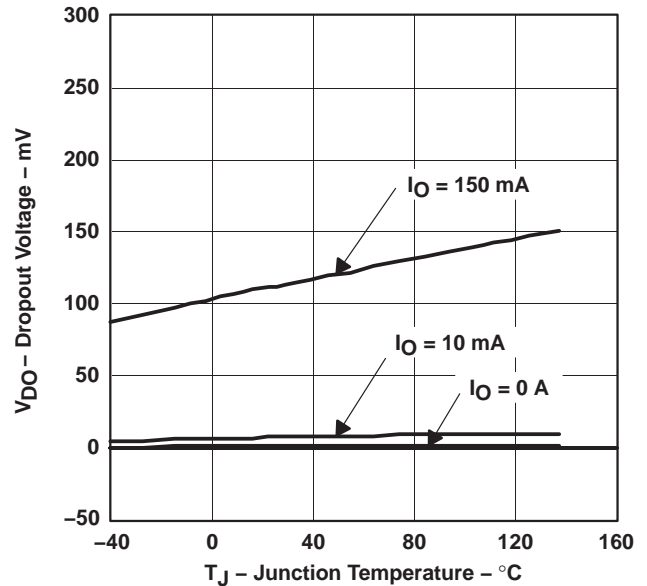
TPS771xx-Q1 WITH RESET OUTPUT TPS772xx-Q1 WITH POWER GOOD OUTPUT 150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

- Qualified for Automotive Applications
- Open Drain Power-On Reset With 220-ms Delay (TPS771xx)
- Open Drain Power-Good (PG) Status Output (TPS772xx)
- 150-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.7-V, 2.8-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage Typically 115 mV at 150 mA (TPS77133, TPS77233)
- Ultralow 92- μ A Quiescent Current (Typ)
- 8-Pin MSOP (DGK) Package
- Low Noise (55 μ V_{rms}) Without External Filter (Bypass) Capacitor (TPS77118, TPS77218)
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Fast Transient Response
- Thermal Shutdown Protection



TPS77x33
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE



description

The TPS771xx and TPS772xx are low-dropout regulators with integrated power-on reset and power good (PG) function respectively. These devices are capable of supplying 150 mA of output current with a dropout of 115 mV (TPS77133, TPS77233). Quiescent current is 92 μ A at full load dropping down to 1 μ A when device is disabled. These devices are optimized to be stable with a wide range of output capacitors including low ESR ceramic (10 μ F) or low capacitance (1 μ F) tantalum capacitors. These devices have extremely low noise output performance (55 μ V_{rms}) without using any added filter capacitors. TPS771xx and TPS772xx are designed to have fast transient response for larger load current changes.

The TPS771xx or TPS772xx is offered in 1.5 V, 1.8-V, 2.7-V, 2.8-V, 3.3-V, and 5 V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is 2% over line, load, and temperature ranges. The TPS771xx and TPS772xx families are available in 8-pin MSOP (DGK) packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2008, Texas Instruments Incorporated

TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is low (typically 115 mV at an output current of 150 mA for 3.3-V option) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is low and independent of output loading (typically 92 μ A over the full range of output current, 0 mA to 150 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The device is enabled when the \overline{EN} pin is connected to a low-level input voltage. This LDO family also features a sleep mode; applying a TTL high signal to \overline{EN} (enable) shuts down the regulator, reducing the quiescent current to less than 1 μ A at $T_J = 25^\circ\text{C}$.

The TPS771xx features an integrated power-on reset, commonly used as a supply voltage supervisor (SVS) or reset output voltage. The \overline{RESET} output of the TPS771xx initiates a reset in DSP, microcomputer or microprocessor systems at power up and in the event of an undervoltage condition. An internal comparator in the TPS771xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT reaches 95% of its regulated voltage, \overline{RESET} goes to a high-impedance state after a 220 ms delay. \overline{RESET} goes to low-impedance state when OUT is pulled below 95% (i.e., over load condition) of its regulated voltage.

For the TPS772xx, the power good terminal (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator. An internal comparator in the TPS772xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT falls below 82% of its regulated voltage, PG goes to a low-impedance state. PG goes to a high-impedance state when OUT is above 82% of its regulated voltage.

AVAILABLE OPTIONS†‡§

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES‡ MSOP (DGK)			
	TYP		TPS771xx SYMBOL		TPS772xx SYMBOL
-40°C to 125°C	5	TPS77150QDGKQ1§	BMO	TPS77250QDGKQ1§	BMI
	3.3	TPS77133QDGKQ1§	BMN	TPS77233QDGKQ1§	BMH
	2.8	TPS77128QDGKQ1§	BMM	TPS77228QDGKQ1§	BMG
	2.7	TPS77127QDGKQ1§	BML	TPS77227QDGKQ1§	BMF
	1.8	TPS77118QDGKQ1§	BMK	TPS77218QDGKQ1§	BME
	1.5	TPS77115QDGKQ1§	BMJ	TPS77215QDGKQ1§	BMD
	Adjustable 1.5 V to 5.5 V	TPS77101QDGKQ1	ANP	TPS77201QDGKQ1§	BMC

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

§ Product Preview

NOTE: The TPS77101 and TPS77201 are programmable using an external resistor divider (see the application information section). The DGK package is available taped and reeled. Add an R suffix to the device type (e.g., TPS77101QDGKRQ1).



TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

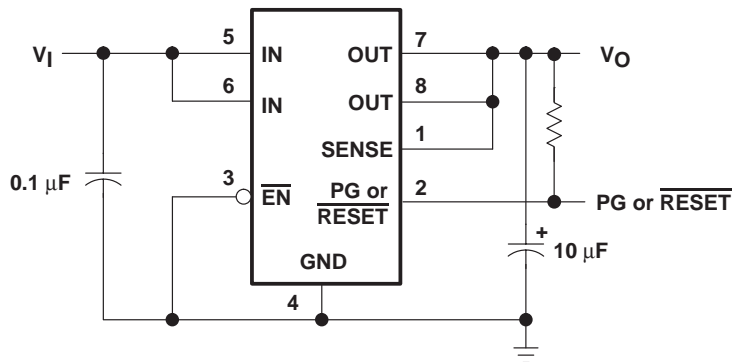
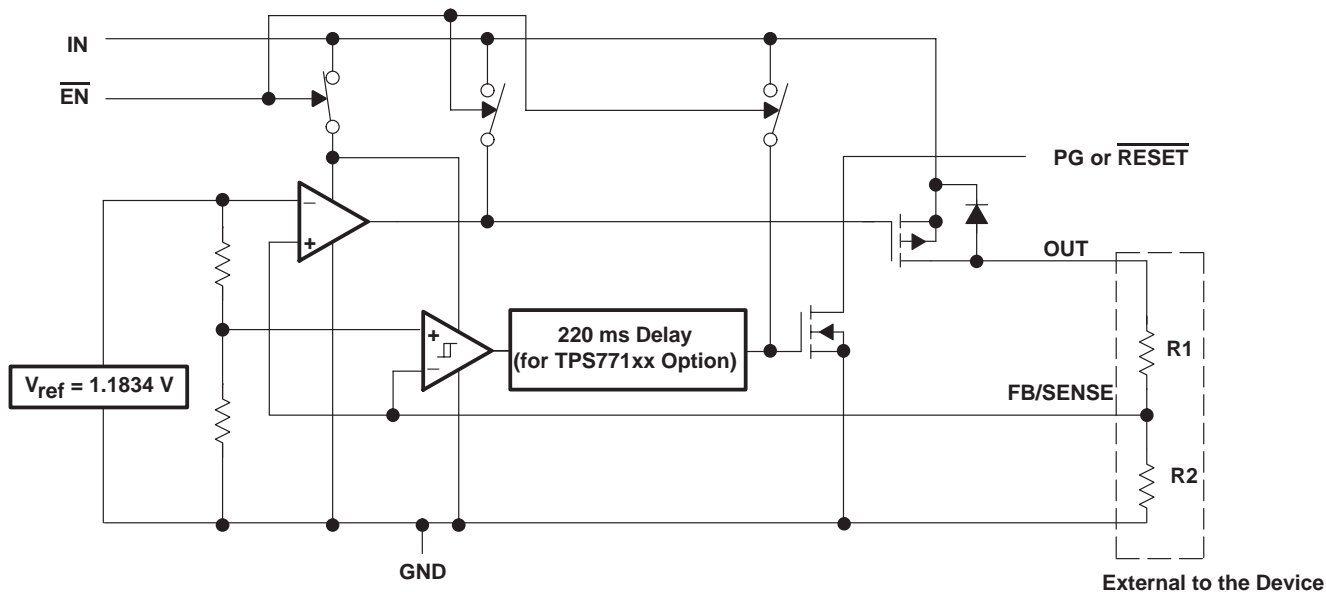


Figure 1. Typical Application Configuration (For Fixed Output Options)

functional block diagrams

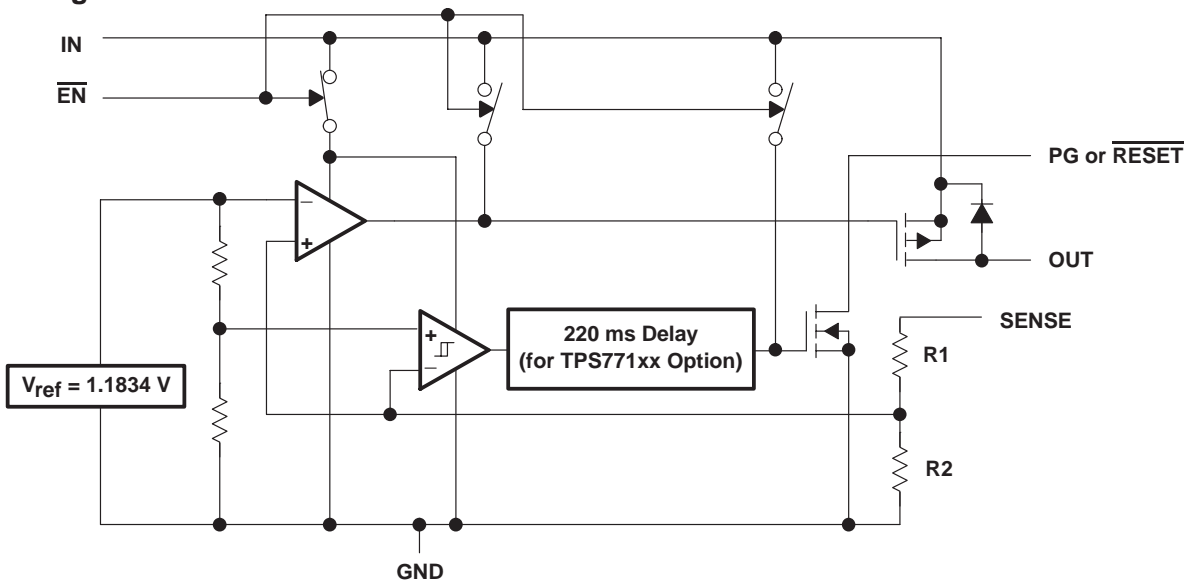
adjustable version



TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

fixed-voltage version



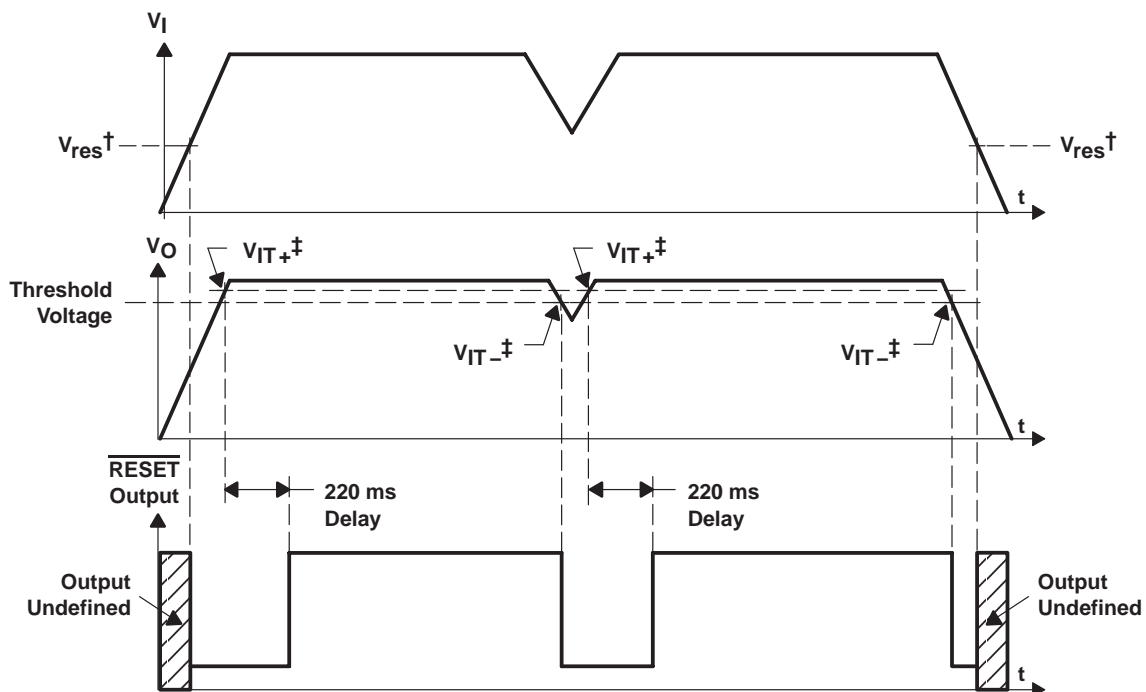
Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
TPS771XX			
FB/SENSE	1	I	Feedback input voltage for adjustable device (sense input for fixed options)
RESET	2	O	Reset output
EN	3	I	Enable input
GND	4		Regulator ground
IN	5, 6	I	Input voltage
OUT	7, 8	O	Regulated output voltage
TPS772XX			
FB/SENSE	1	I	Feedback input voltage for adjustable device (sense input for fixed options)
PG	2	O	Power good
EN	3	I	Enable input
GND	4		Regulator ground
IN	5, 6	I	Input voltage
OUT	7, 8	O	Regulated output voltage

TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

TPS771xx RESET timing diagram



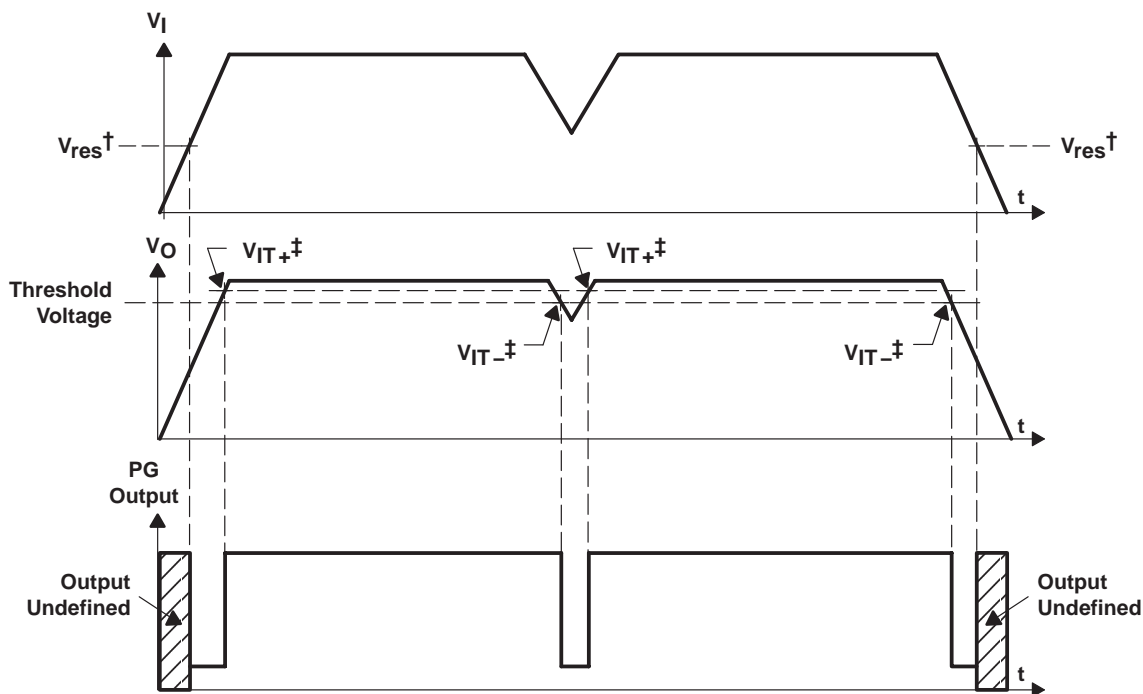
† V_{res} is the minimum input voltage for a valid \overline{RESET} . The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ V_{IT-} – Trip voltage is typically 5% lower than the output voltage ($95\%V_O$) V_{IT-} to V_{IT+} is the hysteresis voltage.

TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

TPS772xx PG timing diagram



† V_{res} is the minimum input voltage for a valid PG. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ V_{IT-} – Trip voltage is typically 18% lower than the output voltage ($82\%V_O$) V_{IT-} to V_{IT+} is the hysteresis voltage.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Input voltage range, V_I , (see Note 1)	–0.3 V to 13.5 V
Voltage range at EN	–0.3 V to 16.5 V
Maximum RESET voltage (TPS771xx)	16.5 V
Maximum PG voltage (TPS772xx)	16.5 V
Peak output current	Internally limited
Continuous total power dissipation	See Dissipation Rating Table
Output voltage, V_O (OUT, FB)	5.5 V
Operating virtual junction temperature range, T_J	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
ESD rating, HBM	2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network terminal ground.



TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

DISSIPATION RATING TABLE – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGK	0	266.2	3.84	376 mW	3.76 mW/°C	207 mW	150 mW
	150	255.2	3.92	392 mW	3.92 mW/°C	216 mW	157 mW
	250	242.8	4.21	412 mW	4.12 mW/°C	227 mW	165 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I †	2.7	10	V
Output voltage range, V_O	1.5	5.5	V
Output current, I_O (see Note 2)	0	150	mA
Operating virtual junction temperature, T_J (see Note 2)	-40	125	°C

† To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.
 NOTE 2: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

electrical characteristics over recommended operating junction temperature range (–40°C to 125°C), $V_I = V_{O(typ)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (see Note 3 and Note 4)	Adjustable voltage	$1.5\text{ V} \leq V_O \leq 5.5\text{ V}$, $T_J = 25^\circ\text{C}$	V_O			V
		$1.5\text{ V} \leq V_O \leq 5.5\text{ V}$	$0.98V_O$	$1.02V_O$		
	1.5-V Output	$T_J = 25^\circ\text{C}$, $2.7\text{ V} < V_{IN} < 10\text{ V}$	1.5			V
		$2.7\text{ V} < V_{IN} < 10\text{ V}$	1.47	1.53		
	1.8-V Output	$T_J = 25^\circ\text{C}$, $2.8\text{ V} < V_{IN} < 10\text{ V}$	1.8			
		$2.8\text{ V} < V_{IN} < 10\text{ V}$	1.764	1.836		
	2.7-V Output	$T_J = 25^\circ\text{C}$, $3.7\text{ V} < V_{IN} < 10\text{ V}$	2.7			
		$3.7\text{ V} < V_{IN} < 10\text{ V}$	2.646	2.754		
	2.8-V Output	$T_J = 25^\circ\text{C}$, $3.8\text{ V} < V_{IN} < 10\text{ V}$	2.8			
		$3.8\text{ V} < V_{IN} < 10\text{ V}$	2.744	2.856		
3.3-V Output	$T_J = 25^\circ\text{C}$, $4.3\text{ V} < V_{IN} < 10\text{ V}$	3.3				
	$4.3\text{ V} < V_{IN} < 10\text{ V}$	3.234	3.366			
5-V Output	$T_J = 25^\circ\text{C}$, $6\text{ V} < V_{IN} < 10\text{ V}$	5			V	
	$6\text{ V} < V_{IN} < 10\text{ V}$	4.9	5.1			
Quiescent current (GND current) (see Note 3 and Note 4)		$T_J = 25^\circ\text{C}$	92			μA
			125			
Output voltage line regulation ($\Delta V_O/V_O$) (see Note 5)		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$, $T_J = 25^\circ\text{C}$	0.005			%/V
		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$			0.05	%/V
Load regulation		$T_J = 25^\circ\text{C}$	1			mV
Output noise voltage		BW = 300 Hz to 100 kHz, $T_J = 25^\circ\text{C}$, TPS77118, TPS77218	55			μVrms
Output current Limit		$V_O = 0\text{ V}$	0.9	1.4		A
Peak output current		2-ms pulse width, 50% duty cycle	400			mA
Thermal shutdown junction temperature			144			$^\circ\text{C}$
Standby current		$\overline{EN} = V_I$, $T_J = 25^\circ\text{C}$			1	μA
		$\overline{EN} = V_I$			3	μA
FB input current	Adjustable voltage	FB = 1.5 V			1	μA
High level enable input voltage			2			V
Low level enable input voltage					0.7	V
Enable input current			-1.5	1.5		μA
Power supply ripple rejection (TPS77118, TPS77218)		f = 1 KHz, $T_J = 25^\circ\text{C}$	55			dB

NOTES: 3. Minimum input operating voltage is 2.7 V or $V_{O(typ)} + 1\text{ V}$, whichever is greater. Maximum input voltage = 10 V, minimum output current 1 mA.

4. If $V_O < 1.8\text{ V}$ then $V_{I(max)} = 10\text{ V}$, $V_{I(min)} = 2.7\text{ V}$:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O(V_{I(max)} - 2.7\text{ V})}{100} \times 1000$$

If $V_O > 2.5\text{ V}$ then $V_{I(max)} = 10\text{ V}$, $V_{I(min)} = V_O + 1\text{ V}$:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O(V_{I(max)} - (V_O + 1))}{100} \times 1000$$

5. $I_O = 1\text{ mA}$ to 150 mA



TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

electrical characteristics over recommended operating junction temperature range (–40°C to 125°C), $V_I = V_O(\text{typ}) + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG (TPS772xx)	Minimum input voltage for valid PG	$I_{(\text{PG})} = 300\mu\text{A}$ $V_{(\text{PG})} \leq 0.8\text{ V}$		1.1		V
	Trip threshold voltage	V_O decreasing	79		85	% V_O
	Hysteresis voltage	Measured at V_O		0.5		% V_O
	Output low voltage	$V_I = 2.7\text{ V}$, $I_{(\text{PG})} = 1\text{ mA}$	0.15		0.4	V
	Leakage current	$V_{(\text{PG})} = 5\text{ V}$			1	μA
Reset (TPS771xx)	Minimum input voltage for valid $\overline{\text{RESET}}$	$I_{(\text{RESET})} = 300\mu\text{A}$		1.1		V
	Trip threshold voltage	V_O decreasing	92		98	% V_O
	Hysteresis voltage	Measured at V_O		0.5		% V_O
	Output low voltage	$V_I = 2.7\text{ V}$, $I_{(\text{RESET})} = 1\text{ mA}$	0.15		0.4	V
	Leakage current	$V_{(\text{RESET})} = 5\text{ V}$			1	μA
	RESET time-out delay			220		ms
V_{DO}	Dropout voltage (see Note 6)	2.8-V Output	$I_O = 150\text{ mA}$, $T_J = 25^\circ\text{C}$		150	mV
			$I_O = 150\text{ mA}$,		265	
		3.3-V Output	$I_O = 150\text{ mA}$, $T_J = 25^\circ\text{C}$		115	
			$I_O = 150\text{ mA}$		200	
		5.0-V Output	$I_O = 150\text{ mA}$, $T_J = 25^\circ\text{C}$		75	
			$I_O = 150\text{ mA}$		115	

NOTE 6: I_N voltage equals $V_O(\text{typ}) - 100\text{ mV}$; 1.5 V, 1.8 V, and 2.7 V dropout voltage limited by input voltage range limitations (i.e., 3.3-V input voltage needs to drop to 3.2 V for purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
V_O	Output voltage	vs Output current
		vs Junction temperature
	Ground current	vs Junction temperature
	Power supply rejection ratio	vs Frequency
	Output spectral noise density	vs Frequency
Z_o	Output impedance	vs Frequency
V_{DO}	Dropout voltage	vs Input voltage
		vs Junction temperature
	Line transient response	12, 14
	Load transient response	13, 15
	Output voltage and enable pulse	vs Time
	Equivalent series resistance (ESR)	vs Output current

TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

TPS77x33
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

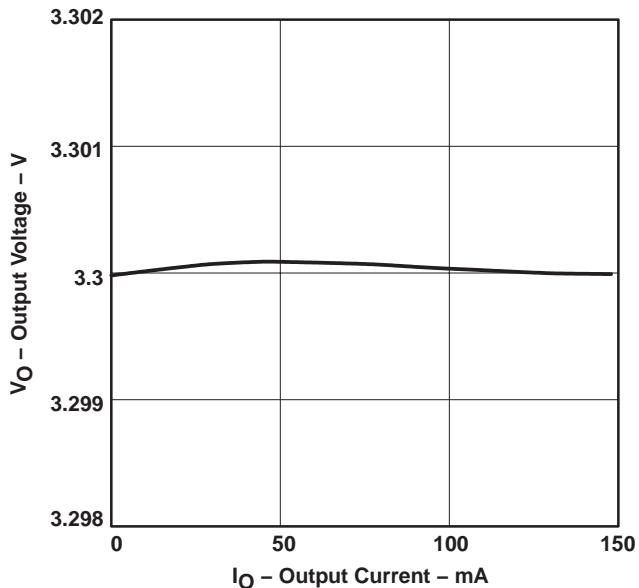


Figure 2

TPS77x18
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

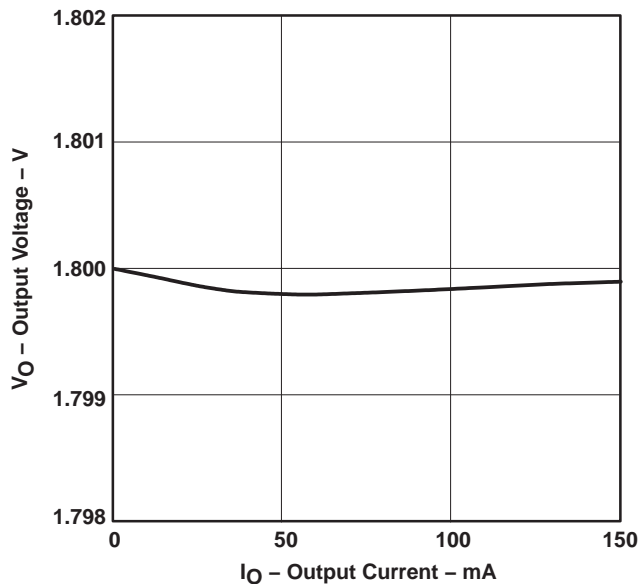


Figure 3

TPS77x33
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

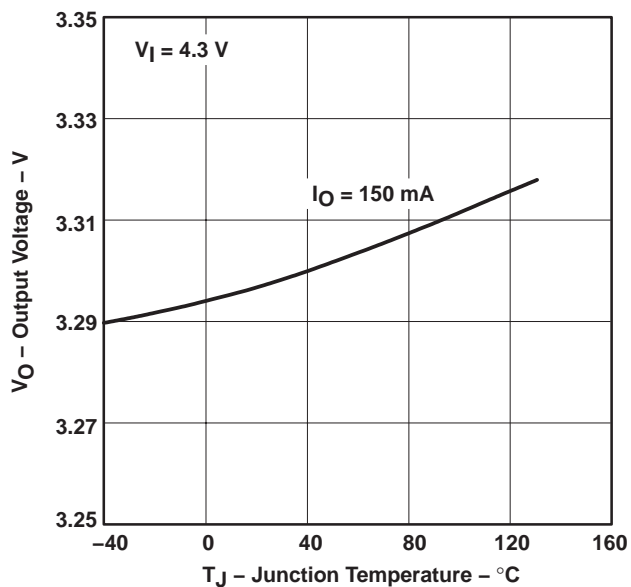


Figure 4

TPS77x18
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

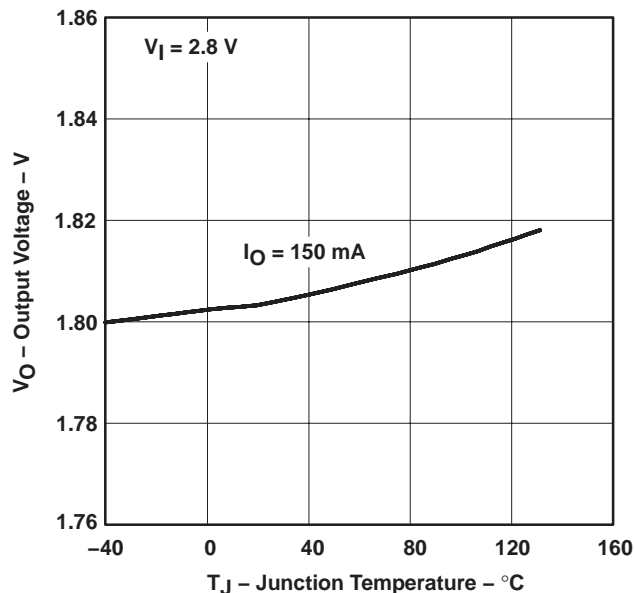


Figure 5



TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

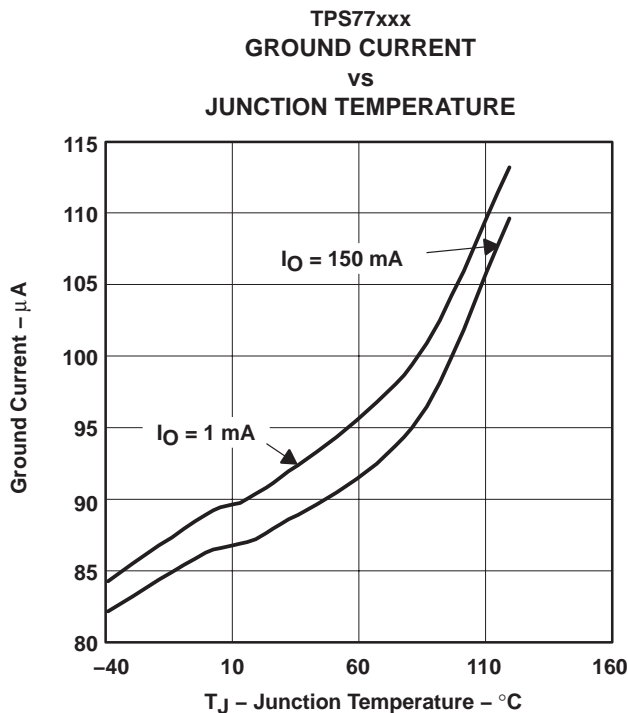


Figure 6

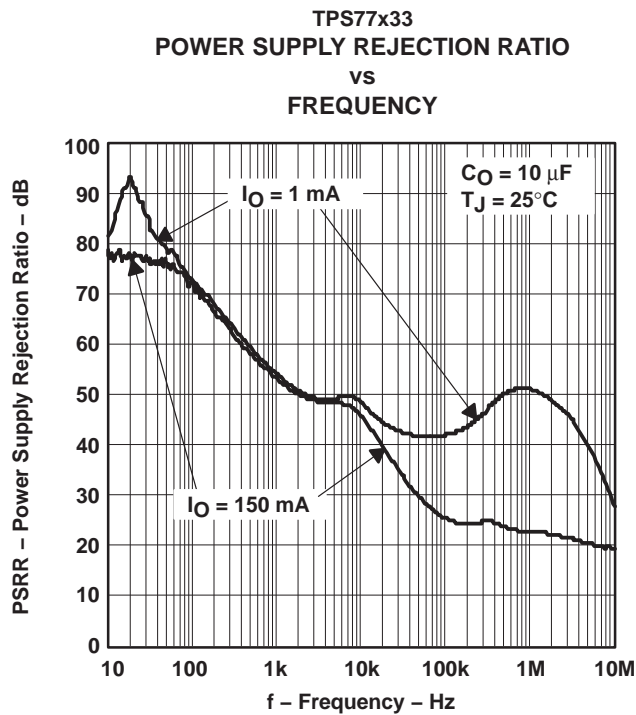


Figure 7

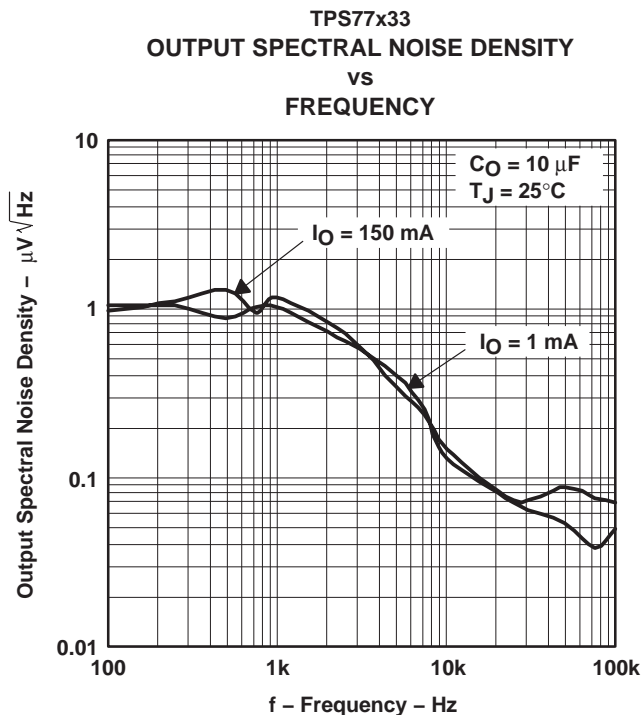


Figure 8

TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

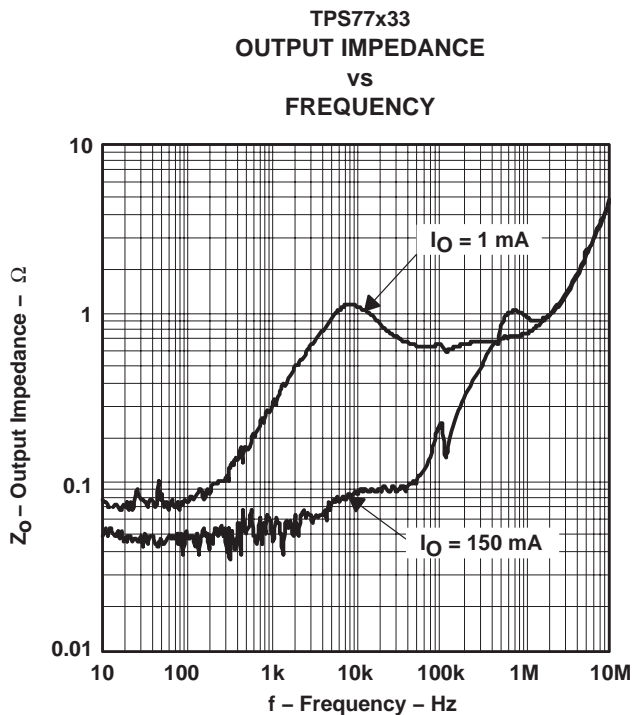


Figure 9

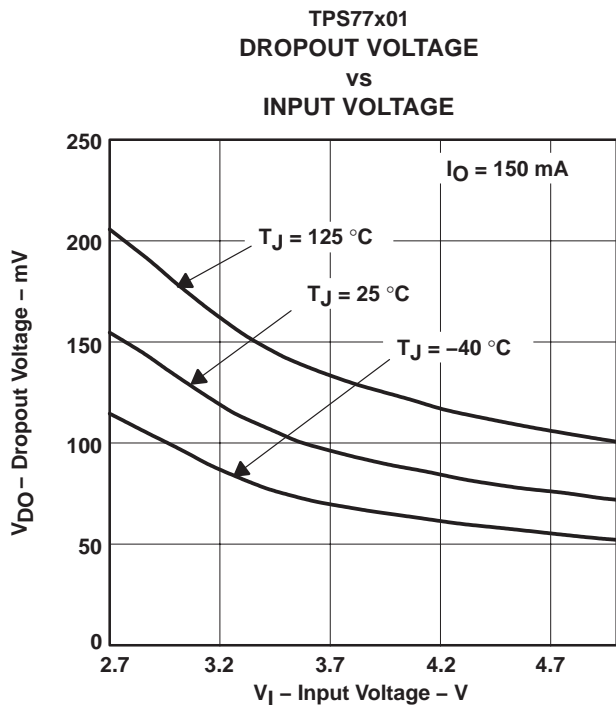


Figure 10

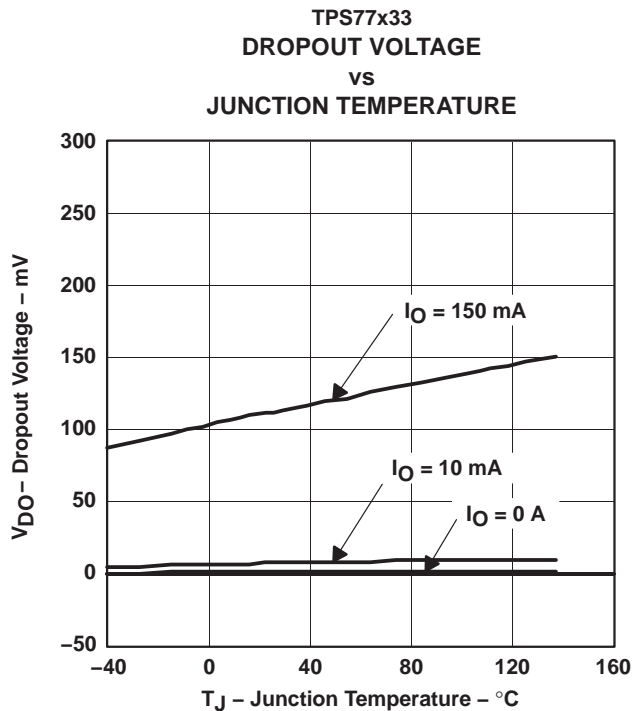


Figure 11



TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

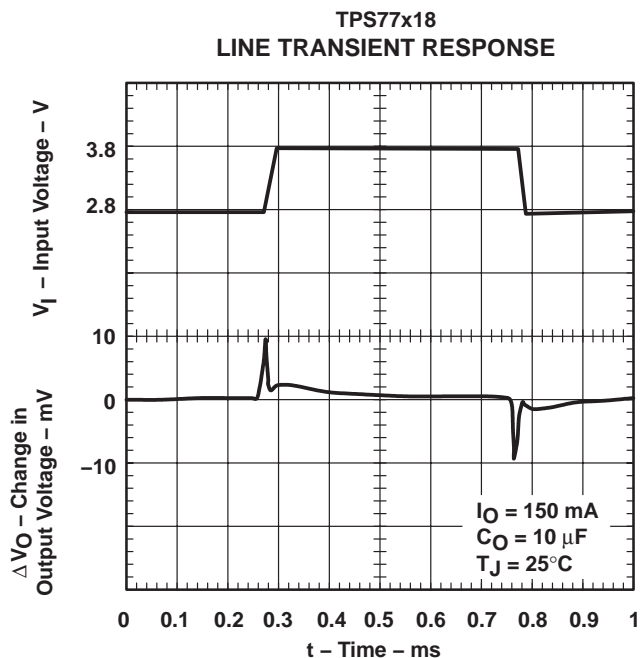


Figure 12

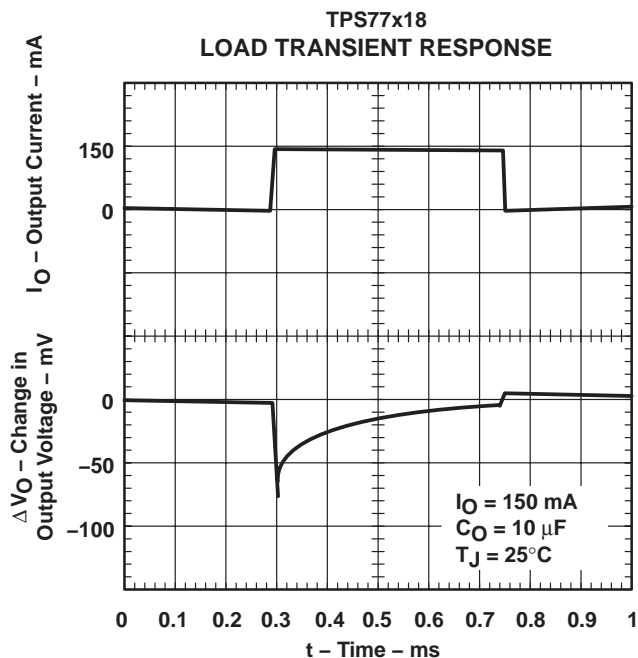


Figure 13

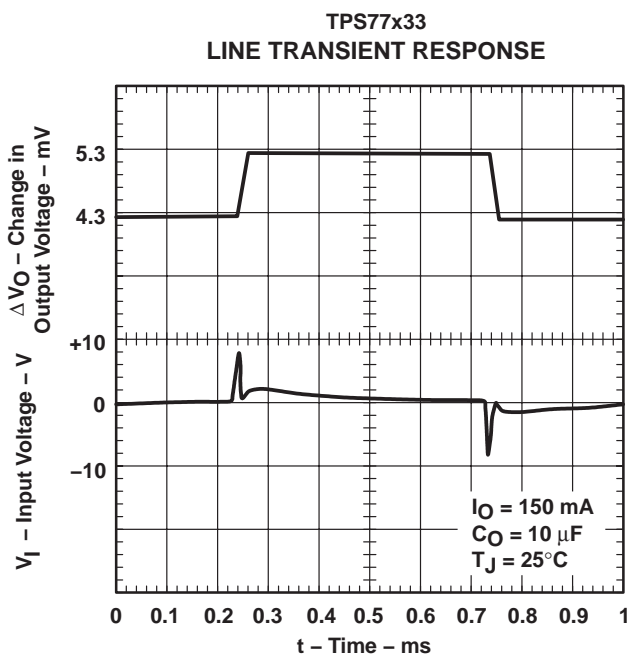


Figure 14

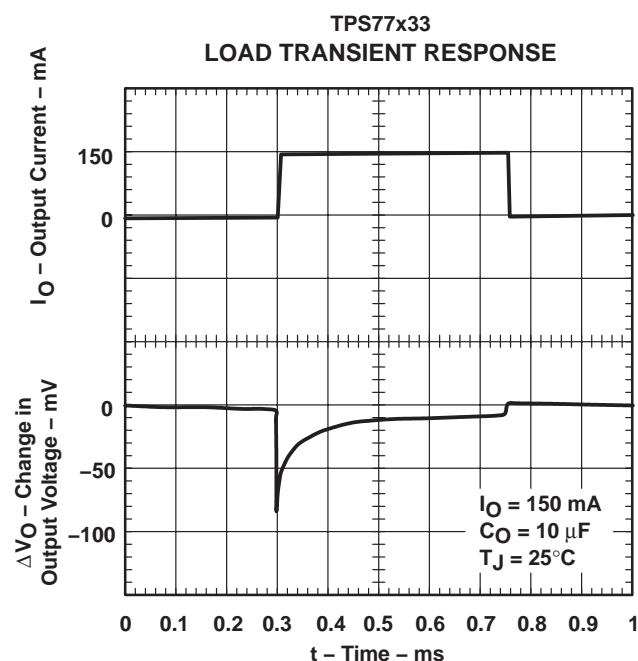


Figure 15

TYPICAL CHARACTERISTICS

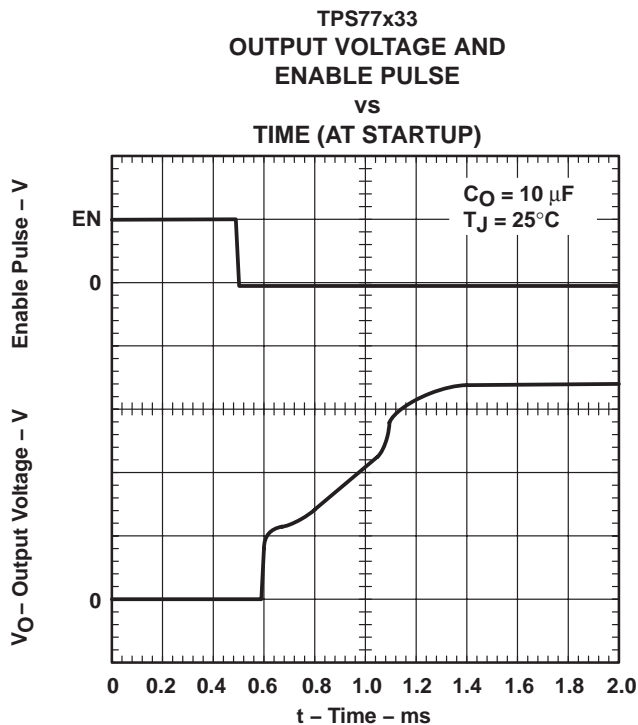


Figure 16

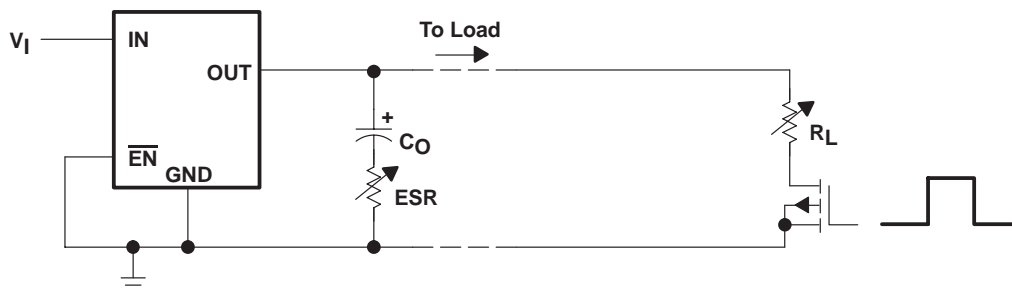
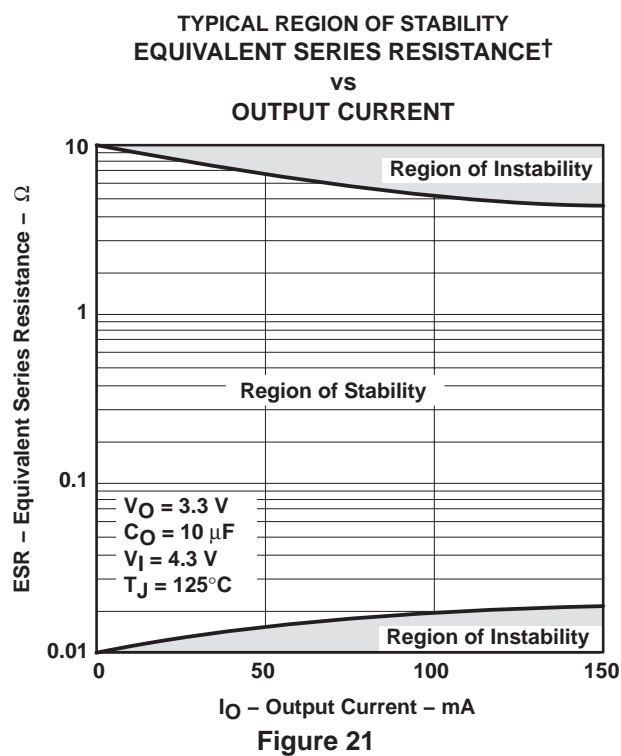
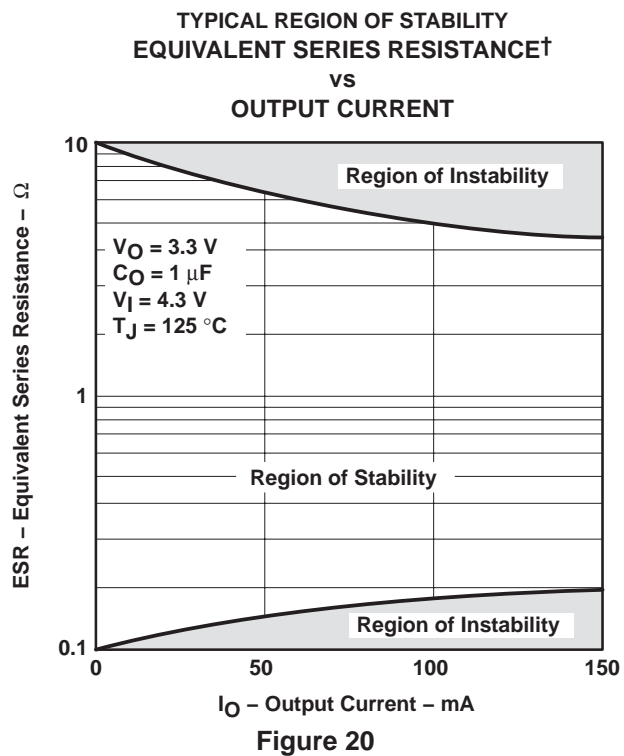
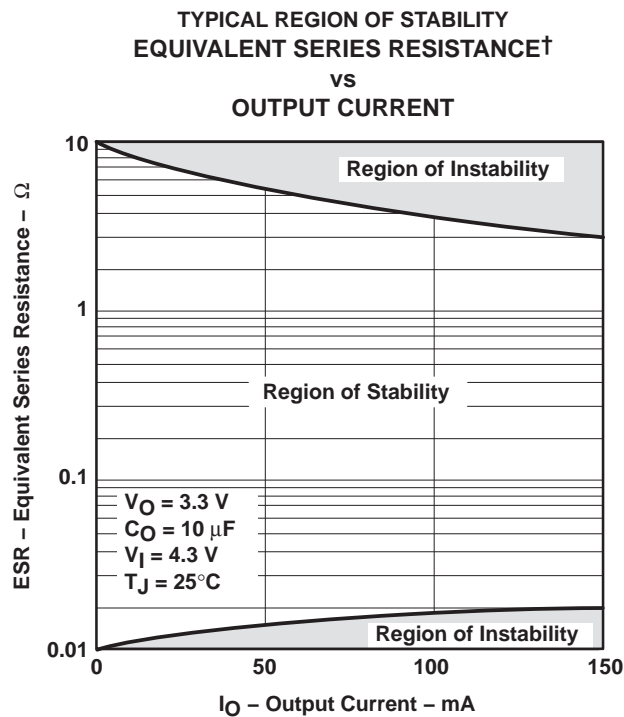
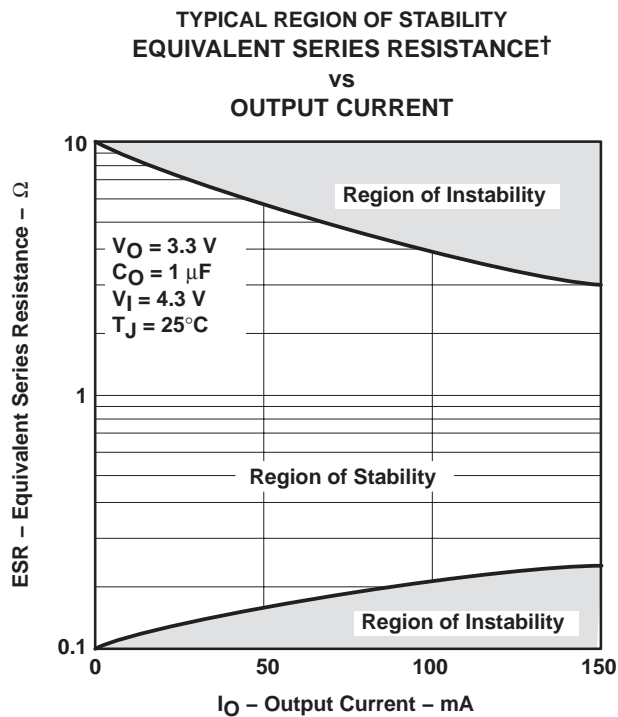


Figure 17. Test Circuit for Typical Regions of Stability (Figures 18 through 21) (Fixed Output Options)

TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS



† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

TPS771xx-Q1 WITH RESET OUTPUT TPS772xx-Q1 WITH POWER GOOD OUTPUT 150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

APPLICATION INFORMATION

pin functions

enable (\overline{EN})

The \overline{EN} terminal is an input which enables or shuts down the device. If \overline{EN} is a logic high, the device will be in shutdown mode. When \overline{EN} goes to logic low, then the device will be enabled.

power good (PG) (TPS772xx)

The PG terminal is an open drain, active high output that indicates the status of V_{out} (output of the LDO). When V_{out} reaches 82% of the regulated voltage, PG goes to a high-impedance state. It goes to a low-impedance state when V_{out} falls below 82% (i.e., over load condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.

sense (SENSE)

The SENSE terminal of the fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between the SENSE terminal and V_{out} to filter noise is not recommended because it may cause the regulator to oscillate.

feedback (FB)

FB is an input terminal used for the adjustable-output options and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and V_{out} to filter noise is not recommended because it may cause the regulator to oscillate.

reset (\overline{RESET}) (TPS771xx)

The \overline{RESET} terminal is an open drain, active low output that indicates the status of V_{out} . When V_{out} reaches 95% of the regulated voltage, \overline{RESET} goes to a high-impedance state after a 220-ms delay. \overline{RESET} goes to a low-impedance state when V_{out} is below 95% of the regulated voltage. The open-drain output of the \overline{RESET} terminal requires a pullup resistor.



APPLICATION INFORMATION

external capacitor requirements

An input capacitor is not usually required; however, a bypass capacitor (0.047 μF or larger) improves load transient response and noise rejection if the TPS771xx or TPS772xx is located more than a few inches from the power supply. A higher-capacitance capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Most low noise LDOs require an external capacitor to further reduce noise. This impacts the cost and board space. The TPS771xx and TPS772xx have low noise specification requirements without using any external components.

Like all low dropout regulators, the TPS771xx or TPS772xx requires an output capacitor connected between OUT (output of the LDO) and GND (signal ground) to stabilize the internal control loop. The minimum recommended capacitance value is 1 μF provided the ESR meets the requirement in Figure 19 and Figure 21. In addition, a low-ESR capacitor can be used if the capacitance is at least 10 μF and the ESR meets the requirements in Figure 18 and Figure 20. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

Ceramic capacitors have different types of dielectric material with each exhibiting different temperature and voltage variation. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO type ceramic type capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are therefore acceptable to use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature; therefore, the Y5U and Z5U are not generally recommended for use on this LDO. Independent of which type of capacitor is used, you must make certain that at the worst case condition the capacitance/ESR meets the requirement specified in Figure 18 through Figure 21.

APPLICATION INFORMATION

Figure 22 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

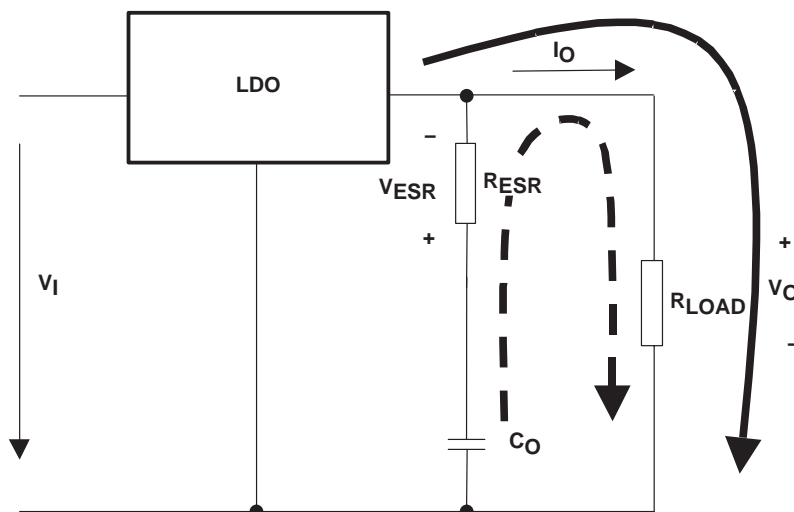


Figure 22. LDO Output Stage With Parasitic Resistances ESR and ESL

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V_{C_{out}} = V_{out}$). This means no current is flowing into the C_{out} branch. If I_{out} suddenly increases (transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 23). Therefore, capacitor C_{out} provides the current for the new load condition (dashed arrow). C_{out} now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop will occur at R_{ESR} . This voltage is shown as V_{ESR} in Figure 22.
- When C_{out} is conducting current to the load, initial voltage at the load will be $V_{out} = V_{C_{out}} - V_{ESR}$. Due to the discharge of C_{out} , the output voltage V_{out} drops continuously until the response time t_1 of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 23.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

APPLICATION INFORMATION

conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

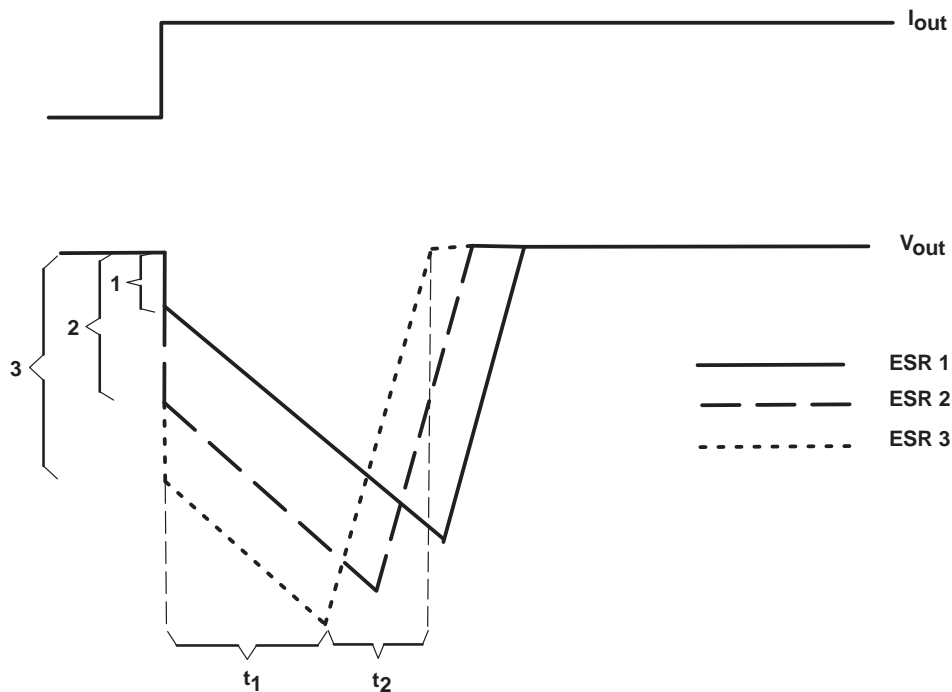


Figure 23. Correlation of Different ESRs and Their Influence to the Regulation of V_{out} at a Load Step From Low-to-High Output Current

TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

APPLICATION INFORMATION

programming the TPS77x01 adjustable LDO regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 24. The output voltage is calculated using:

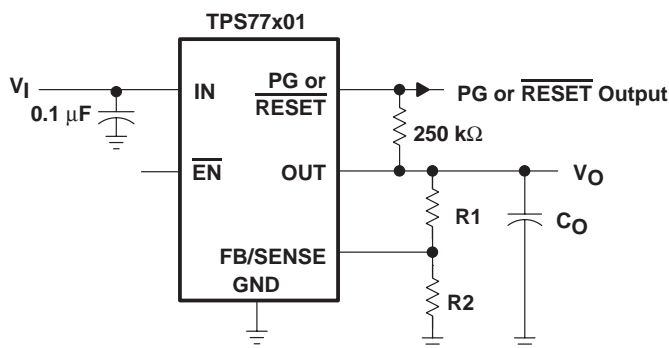
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided, as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.5	30.1	kΩ
3.3 V	53.8	30.1	kΩ
3.6 V	61.5	30.1	kΩ

NOTE: To reduce noise and prevent oscillation, R1 and R2 need to be as close as possible to the FB/SENSE terminal.

Figure 24. TPS77x01 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

regulator protection

The TPS771xx or TPS772xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS771xx or TPS772xx also features internal current limiting and thermal protection. During normal operation, the TPS771xx or TPS772xx limits output current to approximately 0.9 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

T_{Jmax} is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 266.2°C/W for the 8-terminal MSOP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

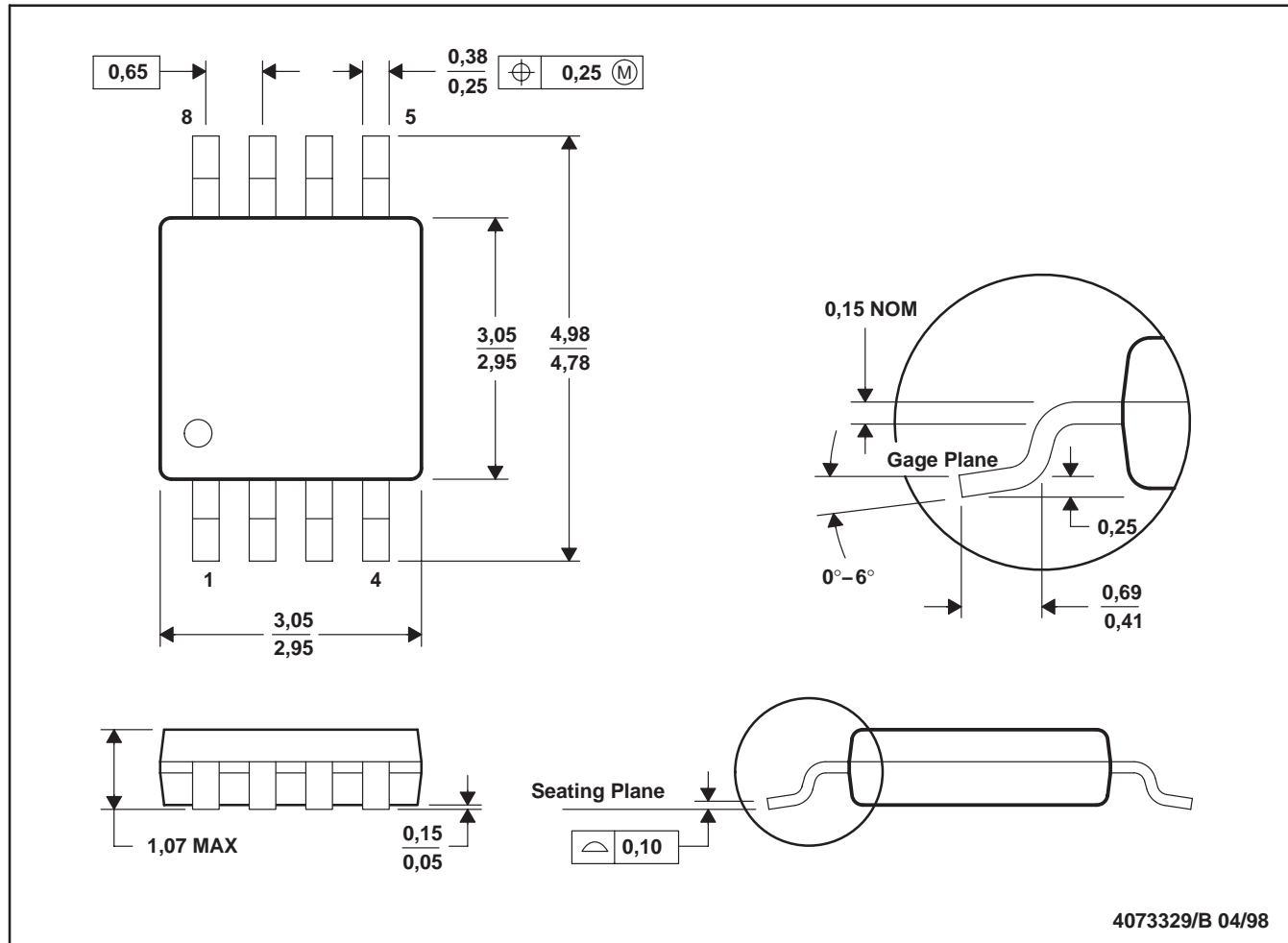
TPS771xx-Q1 WITH RESET OUTPUT
TPS772xx-Q1 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SGLS295A – FEBRUARY 2005 – REVISED APRIL 2008

MECHANICAL DATA

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-187

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS77101QDGKRG4Q1	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS77101QDGKRQ1	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS77101-Q1 :

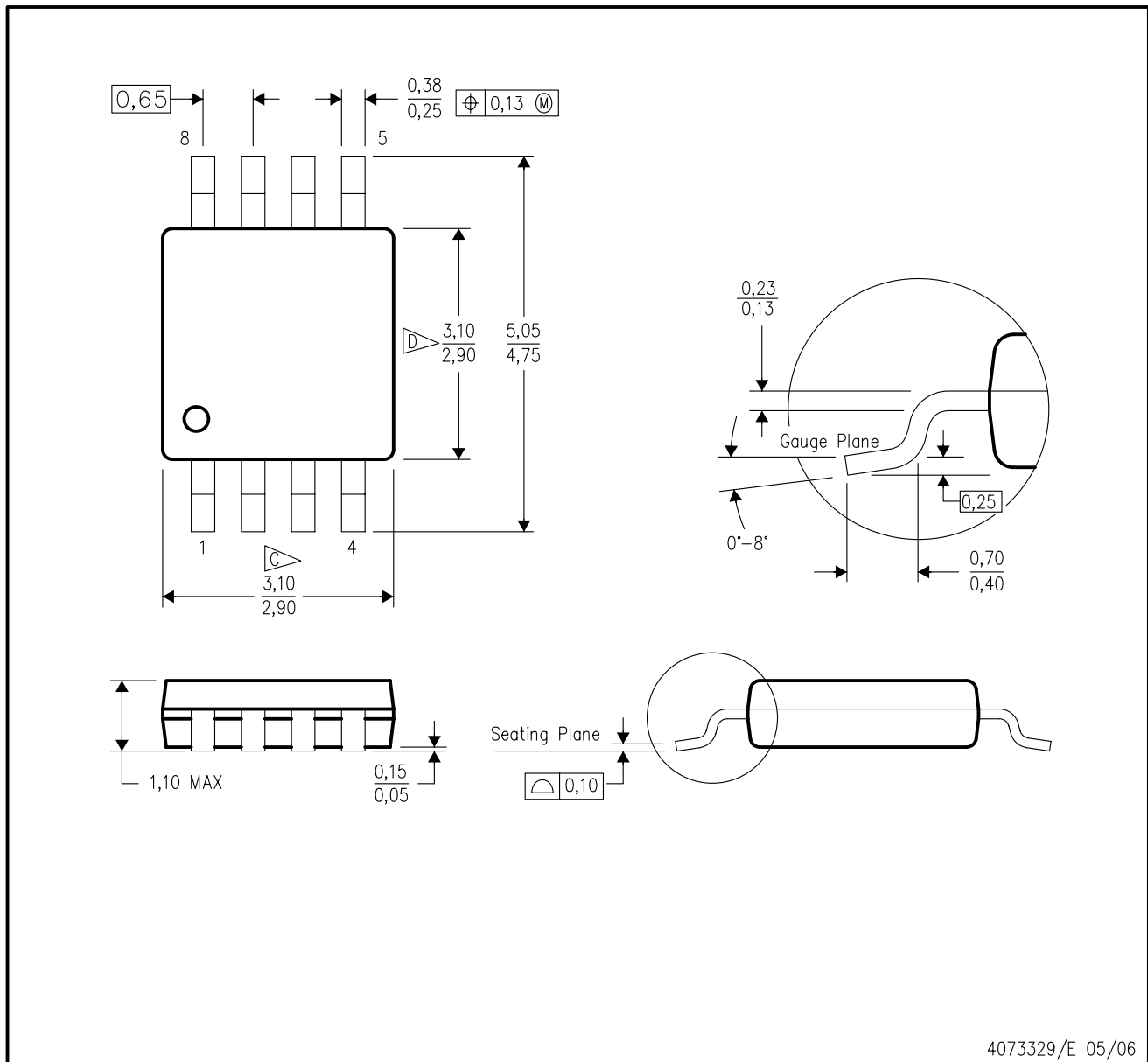
- Catalog: [TPS77101](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TPS77101QDGKRQ1 on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management