Panasonic

AN32055A

http://www.semicon.panasonic.co.jp/en/

7 x 7 Dots Matrix LED Driver LSI with Step-up DC/DC Converter for White LED

FEATURES

- 7 x 7 LED Matrix Driver
  (Total LED that can be driven = 49)
- Built-in memory (ROM and RAM)
- Step-up DC/DC converter
- LDO : 2-ch
- GPIO : 2-ch
- GPI : 3-ch (3pins from GPI1 to GPI3 are in common with SPI2)
- GPO : 2-ch
- SPI Interface : 2-ch (SPI2 is only receiving. It is possible to control only address 05h by SPI2.)
- Driver for LED (Main LED : 4-ch, Sub LED : 2-ch, LED for Photo flash : 2-ch, RGB color unit : 1-ch)
- 80 pin Wafer level chip size package (WLCSP)

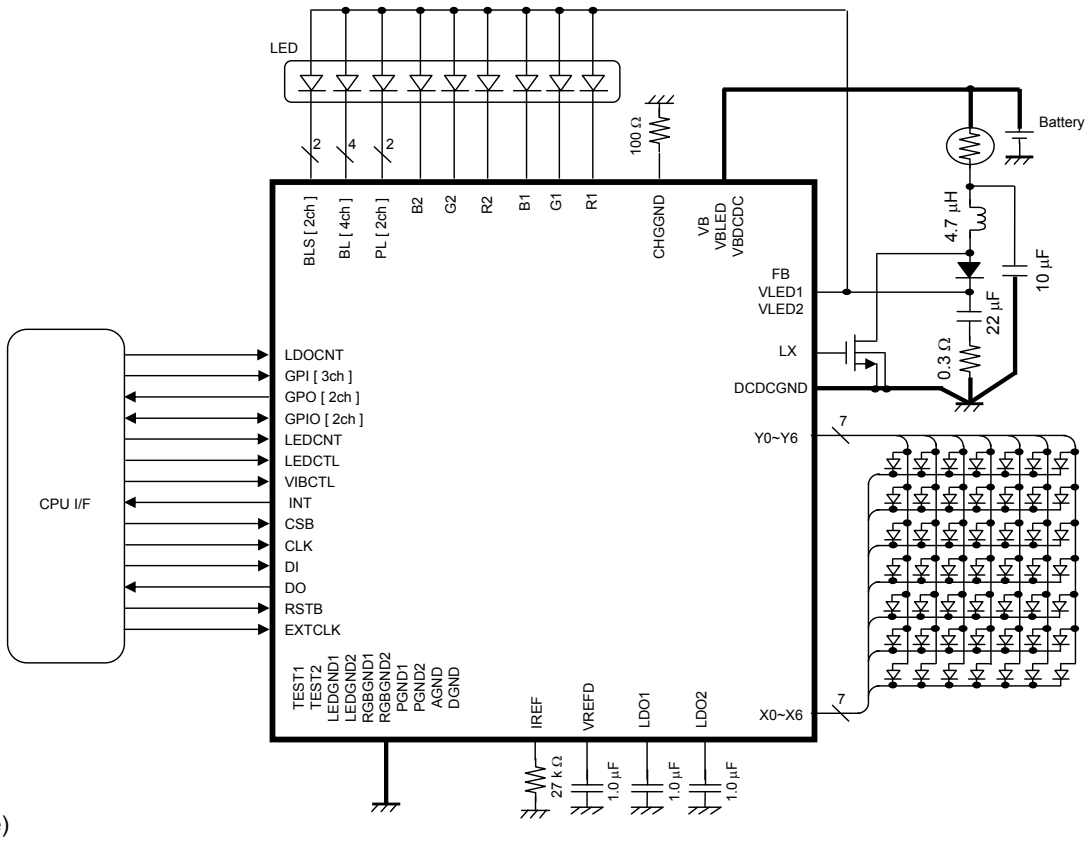
DESCRIPTION

AN32055A is a 6-ch LED driver for LCD backlights, and a driver for LED matrix.
They supply voltage by step-up DC/DC converter.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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CONTENTS

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VB_{MAX}	6.0	V	*1
	$VLED_{MAX}$	6.5	V	*1
Operating ambience temperature	T_{opr}	–30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	LEDCTL, RSTB, CSB, CLK, DI, EXTCLK, VIBCTL, GPI1, GPI2, GPI3, GPIO1, GPIO2	– 0.3 to 3.4	V	—
	LEDCNT, LDOCNT, FB	– 0.3 to 6.0	V	—
Output Voltage Range	GPO1, GPO2, INT, DO	– 0.3 to 3.4	V	—
	LDO1, LDO2	– 0.3 to 6.0	V	—
	BL1, BL2, BL3, BL4, BLS1, BLS2, PL1, PL2, R1, G1, B1, R2, G2, B2, LDO1, LDO2, LX, X0, X1, X2, X3, X4, X5, X6, Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3 to 6.5	V	—
ESD	HBM	1.0 to 1.5	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1: VB_{MAX} = VBDCDC = VBLED = VB, $VLED_{MAX}$ = VLED1 = VLED2. The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
80 pin Wafer level chip size package (WLCSP)	119.4 °C /W	0.837 W	0.335 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value. This value is based on the data LSI mount on PCB Grass Epoxy : 50 X 50 X 0.8 t (mm).

CAUTION

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VB	3.1	3.7	4.6	V	*1
	VLED	3.1	5.0	5.6	V	*1
Input Voltage Range	LEDCTL, RSTB, CSB, CLK, DI, EXTCLK, VIBCTL, GPI1, GPI2, GPI3, GPIO1, GPIO2	– 0.3	—	3.0	V	—
	LEDCNT, LDOCNT, FB	– 0.3	—	VB + 0.3	V	*2
Output Voltage Range	GPO1, GPO2, INT, DO	– 0.3	—	3.0	V	—
	BL1, BL2, BL3, BL4, BLS1, BLS2, PL1, PL2, R1, G1, B1, R2, G2, B2, LDO1, LDO2, LX, X0, X1, X2, X3, X4, X5, X6, Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3	—	VLED + 0.3	V	*2

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, DGND, LEDGND1, LEDGND2, RGBGND1, RGBGND2, DCDCGND, PGND1 and PGND2.
VB is voltage for VBDCDC, VBLED and VB. VLED is voltage for VLED1 and VLED2.
*2: (VB + 0.3) V must not exceed 6 V. (VLED + 0.3) V must not exceed 6.5 V.

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ELECTRICAL CHARACTERISTICS

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (1)	ICC1	At OFF mode LDOCNT = Low	—	0	1	μA	—
Current consumption (2)	ICC2	At Standby mode LDOCNT = Low LDO2 is active.	—	8	12	μA	—
Current consumption (3)	ICC3	LDOCNT = High LDO1 and LDO2 are active.	—	18	24	μA	—
Reference voltage							
Output voltage	VREF	I_{VREF} = 0 μA	1.21	1.24	1.27	V	—
Reference current							
Output voltage	VIREF	I_{IREF} = 0 μA	0.44	0.54	0.64	V	—
Voltage regulator (LDO1)							
Output voltage	VL1	I_{LDO1} = – 30 mA	1.79	1.85	1.91	V	—
Leakage Current when LDO1 turns off	IOFF1	LDOCNT = High REG18 = Low V_{LDO1} = 0 V, IOFF1 = I_{LDO1}	—	—	1	μA	—
Short circuit protection current	IPT1	LDOCNT = High REG18 = High V_{LDO1} = 0 V, IPT1 = I_{LDO1}	50	100	200	mA	—
Ripple rejection (1)	PSL11	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO1} = – 15 mA PSL11 = 20log(acV_{LDO1} / 0.2)	—	– 45	– 40	dB	—
Ripple rejection (2)	PSL12	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO1} = – 15 mA PSL12 = 20log(acV_{LDO1} / 0.2)	—	– 35	– 25	dB	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Voltage regulator (LDO2)							
Output voltage	VL2	I_{LDO2} = – 30 mA	2.76	2.85	2.94	V	—
Leakage Current when LDO2 turns off	IOFF2	LDOCNT = Low REG28 = Low V_{LDO2} = 0 V IOFF2 = I_{LDO2}	—	—	1	μA	—
Short circuit protection current	IPT2	LDOCNT = High V_{LDO2} = 0V IPT2 = I_{LDO2}	50	100	300	mA	—
Ripple rejection (1)	PSL21	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO2} = – 15 mA PSL21 = 20log(acV_{LDO2} / 0.2)	—	– 35	– 30	dB	—
Ripple rejection (2)	PSL22	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO2} = – 15 mA PSL22 = 20log(acV_{LDO2} / 0.2)	—	– 25	– 15	dB	—
Step-up DC/DC converter							
Output voltage (1)	VDC1	Mode 1 Iout = – 400 mA	4.62	4.89	5.16	V	—
Output voltage (2)	VDC2	Mode 2 Iout = – 400 mA	5.03	5.3	5.57	V	—
Oscillation frequency	FDC	OSCEN = [1] , DDSW = [1]	0.96	1.20	1.44	MHz	*1
Short detection delay time	TSCP	Time when INT is set to High from Low, after short detection.	3	13	30	ms	—
SCAN Switch							
Resistance at the Switch ON	RSCAN	$I_{Y0, Y1, Y2, Y3, Y4, Y5, Y6}$ = – 5 mA RSCAN = $V_{Y0, Y1, Y2, Y3, Y4, Y5, Y6}$ / 5 mA	—	2	4.8	Ω	—

*1: Make sure to set both bits of OSCEN and DDSW to [1].
During OSCEN = [1] , DDSW must be set to [1].

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For backlights)							
Output current (1)	IBL1	At 1mA setup $V_{BL1, BL2, BL3, BL4}$ = 1 V IBLS1 = $I_{BL1, BL2, BL3, BL4}$	0.945	1.027	1.109	mA	*2
Output current (2)	IBL2	At 2 mA setup $V_{BL1, BL2, BL3, BL4}$ = 1 V IBLS2 = $I_{BL1, BL2, BL3, BL4}$	1.894	2.058	2.223	mA	*2
Output current (3)	IBL4	At 4 mA setup $V_{BL1, BL2, BL3, BL4}$ = 1 V IBLS4 = $I_{BL1, BL2, BL3, BL4}$	3.808	4.139	4.470	mA	*2
Output current (4)	IBL8	At 8 mA setup $V_{BL1, BL2, BL3, BL4}$ = 1 V IBLS8 = $I_{BL1, BL2, BL3, BL4}$	7.630	8.294	8.957	mA	*2
Output current (5)	IBL16	At 16 mA setup $V_{BL1, BL2, BL3, BL4}$ = 1 V IBLS16 = $I_{BL1, BL2, BL3, BL4}$	15.516	16.865	18.214	mA	*2
Leakage Current when BL1 ~ BL4 turn off	IBLOFF	At current OFF setup $V_{BL1, BL2, BL3, BL4}$ = 4.75 V IBLSOFF = $I_{BL1, BL2, BL3, BL4}$	—	—	1	μA	—
The error between channels	IBLCH	At 15 mA setup The average value of all channels, and the current error of each channel	– 5	—	5	%	—

*2: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For sub backlights)							
Output current (1)	IBLS1	At 1mA setup $V_{BLS1, BLS2}$ = 1 V IBLS1 = $I_{BLS1, BLS2}$	0.949	1.032	1.114	mA	*2
Output current (2)	IBLS2	At 2 mA setup $V_{BLS1, BLS2}$ = 1 V IBLS2 = $I_{BLS1, BLS2}$	1.912	2.078	2.244	mA	*2
Output current (3)	IBLS4	At 4 mA setup $V_{BLS1, BLS2}$ = 1 V IBLS4 = $I_{BLS1, BLS2}$	3.818	4.149	4.480	mA	*2
Output current (4)	IBLS8	At 8 mA setup $V_{BLS1, BLS2}$ = 1 V IBLS8 = $I_{BLS1, BLS2}$	7.677	8.344	9.011	mA	*2
Output current (5)	IBLS16	At 16 mA setup $V_{BLS1, BLS2}$ = 1 V IBLS16 = $I_{BLS1, BLS2}$	15.331	16.665	17.998	mA	*2
Leak current at the time of OFF	IBLSOFF	At current OFF setup $V_{BLS1, BLS2}$ = 4.75 V IBLSOFF = $I_{BLS1, BLS2}$	—	—	1	μA	—
The error between channels	IBLSCH	At 15 mA setup The average value of all channels, and the current error of each channel	– 5	—	5	%	—

*2: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For photo flashes)							
Output current (1)	IPL1	At 1mA setup $V_{PL1, PL2}$ = 1 V IPL1 = $I_{PL1, PL2}$	0.942	1.024	1.105	mA	*2
Output current (2)	IPL2	At 2 mA setup $V_{PL1, PL2}$ = 1 V IPL2 = $I_{PL1, PL2}$	1.887	2.051	2.215	mA	*2
Output current (3)	IPL4	At 4 mA setup $V_{PL1, PL2}$ = 1 V IPL4 = $I_{PL1, PL2}$	3.757	4.083	4.410	mA	*2
Output current (4)	IPL8	At 8 mA setup $V_{PL1, PL2}$ = 1 V IPL8 = $I_{PL1, PL2}$	7.526	8.180	8.835	mA	*2
Output current (5)	IPL16	At 16 mA setup $V_{PL1, PL2}$ = 1 V IPL16 = $I_{PL1, PL2}$	15.215	16.538	17.861	mA	*2
Output current (6)	IPL30	At 30mA setup $V_{PL1, PL2}$ = 1 V IPL30 = $I_{PL1, PL2}$	28.244	30.700	33.156	mA	*2
Leak current at the time of OFF	IPLOFF	At current OFF setup $V_{PL1, PL2}$ = 4.75 V IPLOFF = $I_{PL1, PL2}$	—	—	1	μA	—
The error between channels	IPLCH	At 15 mA setup The average value of all channels, and the current error of each channel	– 5	—	5	%	—

*2: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For 7*7 dots matrix LED)							
Output current (1)	IMX1	At 1mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX1 = $I_{X0, X1, X2, X3, X4, X5, X6}$	0.920	1.000	1.080	mA	*2
Output current (2)	IMX2	At 2 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX2 = $I_{X0, X1, X2, X3, X4, X5, X6}$	1.858	2.019	2.181	mA	*2
Output current (3)	IMX4	At 4 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX4 = $I_{X0, X1, X2, X3, X4, X5, X6}$	3.742	4.068	4.393	mA	*2
Output current (4)	IMX8	At 8 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX8 = $I_{X0, X1, X2, X3, X4, X5, X6}$	7.480	8.131	8.781	mA	*2
Output current (5)	IMX15	At 15 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX15 = $I_{X0, X1, X2, X3, X4, X5, X6}$	14.220	15.456	16.693	mA	*2
Leak current at the time of OFF	IMXOFF	Current OFF setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 4.75 V IMXOFF = $I_{X0, X1, X2, X3, X4, X5, X6}$	—	—	1	μA	—
The error between channels	IMXCH	The average value of all channels, and the current error of each channel	– 5	—	5	%	—

*2: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal. The other current settings are combination of above items.

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For RGB color unit)							
Output current (1)	IRGB1	At 1mA setup $V_{R1, G1, B1}$ = 1 V	0.950	1.032	1.115	mA	*2
Output current (2)	IRGB2	At 2 mA setup $V_{R1, G1, B1}$ = 1 V	1.903	2.068	2.234	mA	*2
Output current (3)	IRGB4	At 4 mA setup $V_{R1, G1, B1}$ = 1 V	3.777	4.105	4.434	mA	*2
Output current (4)	IRGB8	At 8 mA setup $V_{R1, G1, B1}$ = 1 V	7.566	8.223	8.881	mA	*2
Leak current at the time of OFF	IRGBOFF	Current OFF setup $V_{R1, G1, B1, R2, G2, B2}$ = 4.75 V IRGBOFF = $I_{R1, G1, B1, R2, G2, B2}$	—	—	1	μA	—
The error between channels	IRGBCH	The average value of all channels, and the current error of each channel	– 5	—	5	%	—
Switch of Pch-MOS (VLED1)							
VBLED – VLED output impedance	RVLED	VBLED = 2.2 V V_{CHGGND} = 0 V I_{LED1} = – 10 mA RVLED = (2.2 V – V_{LED1}) / 10 mA	—	5	20	Ω	—
Switch of Nch-MOS (R1, R2, G2, B2)							
R1 output impedance	RR1	VB = 2.2 V V_{CHGGND} = 0 V I_{R1} = 5 mA RR1 = V_{R1} / 5 mA	—	10	50	Ω	—
R2 output impedance	RR2	Register : 19hD4 = High I_{R2} = 5 mA RR2 = V_{R2} / 5 mA	—	10	30	Ω	—
G2 output impedance	RG2	Register : 19hD3 = High I_{G2} = 5 mA RG2 = V_{G2} / 5 mA	—	10	30	Ω	—
B2 output impedance	RB2	Register : 19hD2 = High I_{B2} = 5 mA RB2 = V_{B2} / 5 mA	—	10	30	Ω	—

*2: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

Established : 2006-08-29
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI I/F, LEDCTL, RSTB							
Input voltage range of High-level	VIH	High-level recognition voltage	1.4	—	LDO1 + 0.3	V	—
Input voltage range of Low-level	VIL	Low-level recognition voltage	– 0.3	—	0.4	V	—
Input current of High-level	IIH	$V_{LEDCTL, RSTB, CSB, CLK, DI}$ = 1.85 V IIH = $I_{LEDCTL, RSTB, CSB, CLK, DI}$	—	0	1	µA	—
Input current of Low-level	IIL	$V_{LEDCTL, RSTB, CSB, CLK, DI}$ = 0 V IIL = $I_{LEDCTL, RSTB, CSB, CLK, DI}$	—	0	1	µA	—
GPIO I/F, GPI I/F							
Input voltage range of High-level 1	VIH1	High-level recognition voltage (LDO1 mode)	1.4	—	LDO1 + 0.3	V	—
Input voltage range of High-level 1	VIH2	High-level recognition voltage (LDO2 mode)	2.1	—	LDO2 + 0.3	V	—
Input voltage range of Low-level	VIL	Low-level recognition voltage	– 0.3	—	0.4	V	—
Input current of High-level	IIH	$V_{GPI1, GPI2, GPI3, GPIO1, GPIO2}$ = 2.85 V IIH = $I_{GPI1, GPI2, GPI3, GPIO1, GPIO2}$	—	0	1	µA	—
Input current of Low-level	IIL	$V_{GPI1, GPI2, GPI3, GPIO1, GPIO2}$ = 0 V IIL = $I_{GPI1, GPI2, GPI3, GPIO1, GPIO2}$	—	0	1	µA	—
GPIO I/F, GPO I/F, INT							
Output voltage of High-level (1)	VOH1	$I_{GPO1, GPO2, GPIO1, GPIO2, INT}$ = – 2 mA VDDSEL = LDO2	LDO2 × 0.8	—	—	V	—
Output voltage of Low-level (1)	VOL1	$I_{GPO1, GPO2, GPIO1, GPIO2, INT}$ = 2 mA VDDSEL = LDO2 ($I_{GPO1, GPO2, GPIO1, GPIO2, INT}$ = 0.5 mA)	—	—	LDO2 ×0.2 (0.15)	V	—
Output voltage of High-level (2)	VOL2	$I_{GPO1, GPO2, GPIO1, GPIO2, INT}$ = – 2 mA VDDSEL = LDO1	LDO1 × 0.8	—	—	V	—
Output voltage of Low-level (2)	VOL2	$I_{GPO1, GPO2, GPIO1, GPIO2, INT}$ = 2 mA VDDSEL = LDO1 ($I_{GPO1, GPO2, GPIO1, GPIO2, INT}$ = 0.5 mA)	—	—	LDO1 ×0.3 (0.15)	V	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LDOCNT, LEDCNT							
Input voltage range of High-level	VIH	High-level recognition voltage	VB × 0.7	—	VB + 0.3	V	—
Input voltage range of Low-level	VIL	Low-level recognition voltage	– 0.3	—	0.4	V	—
Input current of High-level	IIH	$V_{LDOCNT, LEDCNT}$ = 3.6 V IIH = $I_{LDOCNT, LEDCNT}$	—	0	1	µA	—
Input current of Low-level	IIL	$V_{LDOCNT, LEDCNT}$ = 0 V IIL = $I_{LDOCNT, LEDCNT}$	—	0	1	µA	—
VIBCTL							
Input voltage range of High-level	VIH	High-level recognition voltage	2.1	—	3.3	V	—
Input voltage range of Low-level	VIL	Low-level recognition voltage	– 0.3	—	0.4	V	—
Input current of High-level	IIH	V_{VIBCTL} = 3.0 V IIH = I_{VIBCTL}	—	0	1	V	—
Input current of Low-level	IIL	V_{VIBCTL} = 0 V IIL = I_{VIBCTL}	—	0	1	µA	—
DO							
Output voltage of High-level	VOH3	I_{DO} = – 2 mA	LDO1 × 0.8	—	—	V	—
Output voltage of Low-level	VOL3	I_{DO} = 2 mA	—	—	LDO1 × 0.2	V	—
TEST1, TEST2, GPI1, GPI2, GPI3							
Pull-down resistance	RPD	$I_{TEST1, TEST2, GPI1, GPI2, GPI3}$ = 5 µA RPD = $V_{TEST1, TEST2, GPI1, GPI2, GPI3}$ / 5 µA	70k	100k	130k	Ω	—
GPIO1, GPIO2							
Pull-up resistance	RPU	$I_{GPIO1, GPIO2}$ = 0 µA RPU1 = $V_{GPIO1, GPIO2}$ $I_{GPIO1, GPIO2}$ = – 5 µA RPU = (RPU1 – $V_{GPIO1, GPIO2}$) / 5 µA	70k	100k	130k	Ω	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC/DC converter automatic control part							
Detection voltage	VMON	Voltage which DC/DC converter turns on when the voltage of BL1, BL2, BL3, BL4, BLS1, and BLS2 terminal falls	0.36	0.40	0.44	V	—
Current consumption of DC/DC converter part							
DC/DC control current (1)	IDC1	Current when DC/DC converter is active.	—	1.2	3.0	mA	—
DC/DC control current (2)	IDC2	Current when DC/DC converter is inactive and the automatic control circuit is operating	—	0.7	1.4	mA	—

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Revised : 2013-04-01

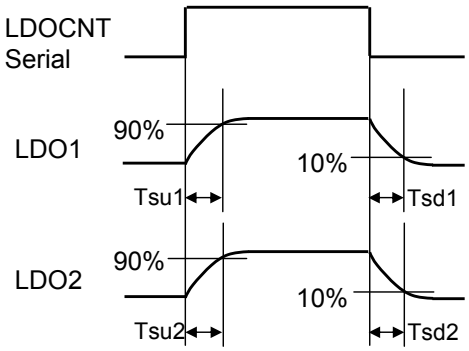
ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Voltage regulator (LDO1)							
Rise time	Tsu1	Time until output voltage reaches to 0 V to 90 %	—	250	—	µs	*3 *4
Fall time	Tsd1	Time until output voltage reaches to 10 %	—	5	—	ms	*3 *4
Load transient response (1)	Vtr11	I_{LDO1} = – 50 µA → – 15 mA (1 µs)	—	70	—	mV	*4
Load transient response (2)	Vtr12	I_{LDO1} = – 15 mA → – 50 µA (1 µs)	—	70	—	mV	*4
Output capacity range	Cldo1	—	—	1.0	—	µF	*4
Output capacity ESR tolerance level	Resr1	—	—	0.05	—	Ω	*4
Maximum output current	Imax1	—	—	15	—	mA	*5
Voltage regulator (LDO2)							
Rise time	Tsu2	Time until output voltage reaches to 0 V to 90 %	—	250	—	µs	*3 *4
Fall time	Tsd2	Time until output voltage reaches to 10 %	—	5	—	ms	*3 *4
Load transient response (1)	Vtr21	I_{LDO2} = – 50 µA → – 15 mA (1 µs)	—	70	—	mV	*4
Load transient response (2)	Vtr22	I_{LDO2} = – 15 mA → – 50 µA (1 µs)	—	70	—	mV	*4
Output capacity range	Cldo2	—	—	1.0	—	µF	*4
Output capacity ESR tolerance level	Resr2	—	—	0.05	—	Ω	*4
Maximum output current	Imax2	—	—	15	—	mA	*5

Note) *3 : Rise time and Fall time are defined as below.
*4 : Typical Design Value



*5 : This IC consumes each 5mA maximum from LDO1 and LDO2 for the internal circuit.
When it is used to supply external components, it must be used within 25mA load current.

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Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Step-up DC/DC converter							
Rise time	Tsu11	Time until output voltage reaches to 90 % from battery voltage	—	1	—	ms	*4 *6
Fall time	Tsd11	Time until output voltage reaches to 3.8 V from 4.9 V $I_{DCDCOUT}$ = 0 mA	—	1	—	s	*4 *6
Load transient response (1)	Vtrdc1	$I_{DCDCOUT}$ = – 50 μA → – 400 mA (1 μs)	—	1	—	V	*4
Load transient response (2)	Vtrdc2	$I_{DCDCOUT}$ = – 400 mA → – 50 μA (1 μs)	—	1	—	V	*4
Output capacity range	Cdc1	—	—	22	—	μF	*4
Output capacity ESR tolerance level	Resr1	—	—	0.30	—	Ω	*4
Excess voltage detection voltage	VOVP	VLED voltage which detects excess voltage	—	6.2	—	V	*4
Delay time of Excess voltage detection voltage	TOVP	Time after excess voltage is detected until INT is set to High from Low	—	12.75	—	ms	*4
Delay time of Constant voltage circuit monitor	TMON	Time after the voltage of BL1 to 4 / BLS1 to 2 goes under 0.4 V until it detects coincidence 3 times and DC/DC converter operates.	—	2.0	—	ms	*4
TSD (Thermal shutdown circuit)							
Detection temperature	Tdet	Temperature which LDO1, LDO2, DC/DC, Constant current circuit, Matrix SW and RGB turns off.	—	160	—	°C	*4 *7
Return temperature	Tsd11	Returning temperature	—	110	—	°C	*4 *8

Note) *4 : Typical Design Value
*6, *7, *8 : Refer to the next page

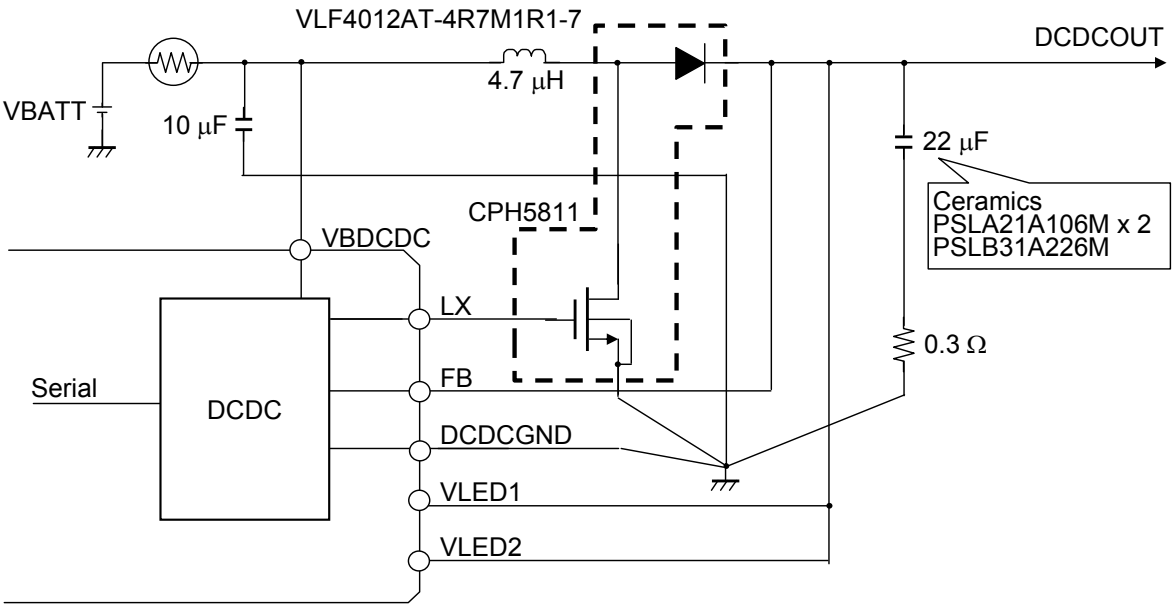
Established : 2006-08-29
Revised : 2013-04-01

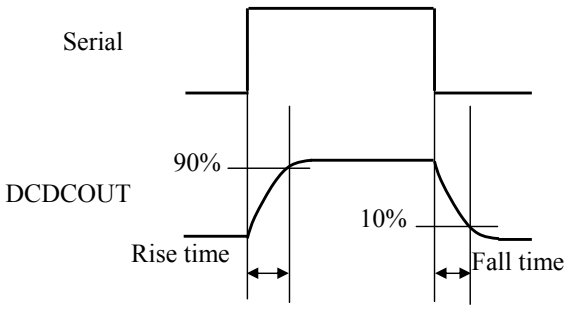
ELECTRICAL CHARACTERISTICS (continued)

VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Note) *6 :





*7: LDO1, LDO2, DC/DC converter, Constant current circuit, and Matrix SW and RGB are turned off when TSD is High. When TSD is High, the register is set as 14hD 1 = 1. However, data can be read only when the register is read immediately after INT occurs since internal regulator is turned off.

*8: Only LDO1 and LDO2 return after ON state of TSD. A logic part will be in Reset state.

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Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

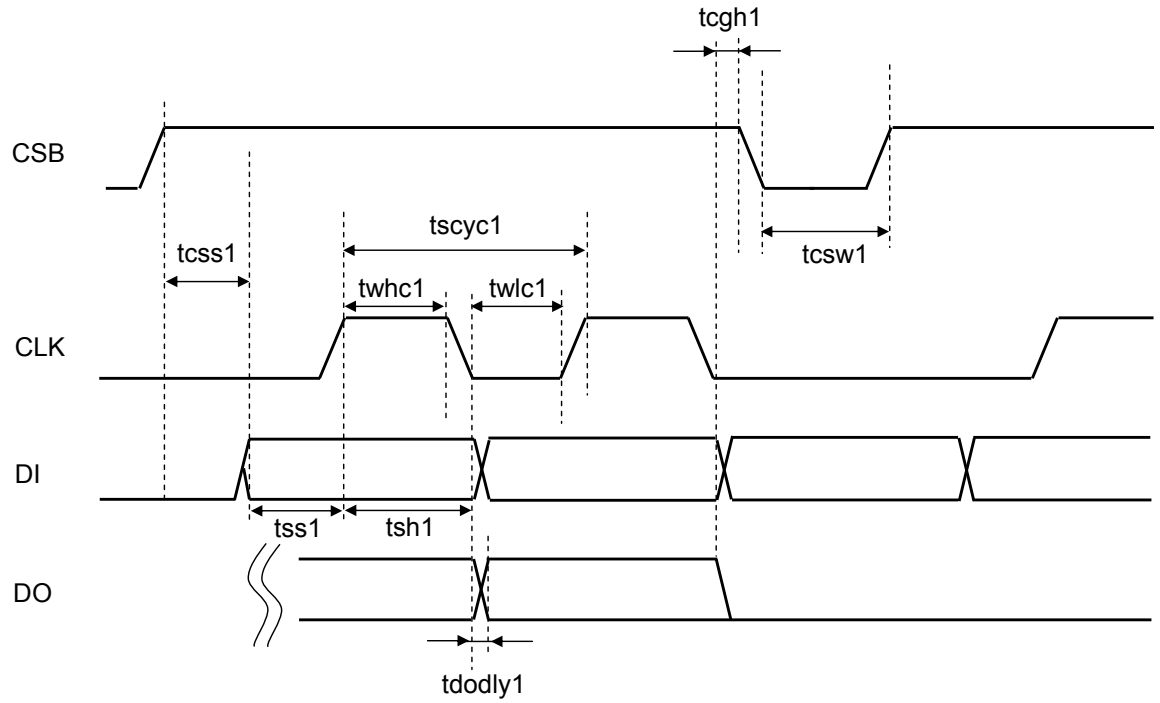
VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Microcomputer interface characteristic (Vdd = 1.85 V ± 3%)							
CLK cycle time	tscyc1	—	—	125	—	ns	*4
CLK cycle time High period	twhc1	—	—	60	—	ns	*4
CLK cycle time Low period	twlc1	—	—	60	—	ns	*4
Serial-data setup time	tss1	—	—	62	—	ns	*4
Serial-data hold time	tsh1	—	—	62	—	ns	*4
Transceiver interval	tcsw1	—	—	62	—	ns	*4
Chip enable setup time	tcss1	—	—	5	—	ns	*4
Chip enable hold time	tcgh1	—	—	5	—	ns	*4
DC delay time	tdodly1	Only READ	—	25	—	ns	*4

Note) *4 : Typical Design Value

Microcomputer interface Timing chart



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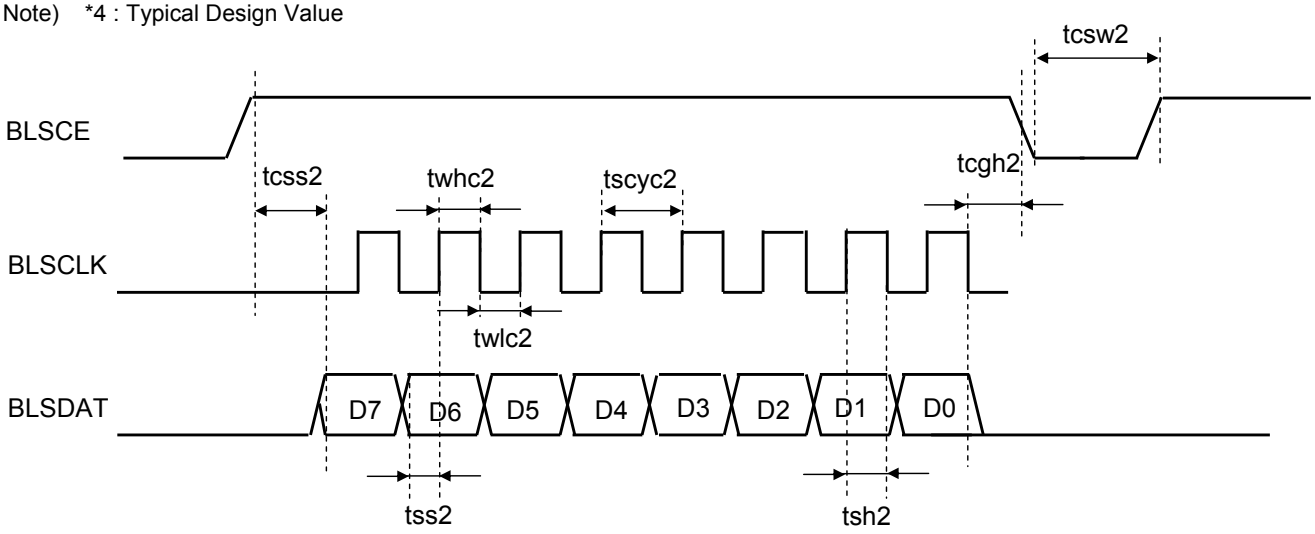
ELECTRICAL CHARACTERISTICS (continued)

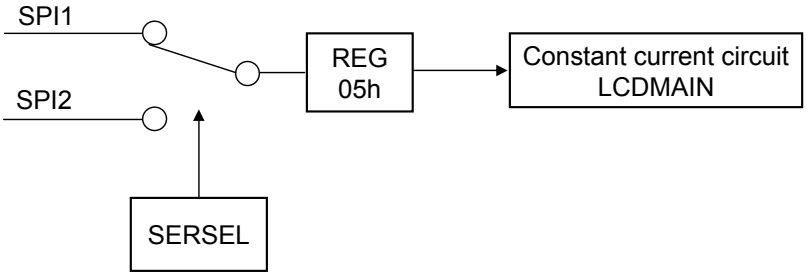
VB = VBDCDC = VBLED = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI2 format Microcomputer interface characteristic (Vdd = 1.85 V ± 3%)							
BLSCLK cycle time	tscyc2	—	—	125	—	ns	*4
BLSCLK cycle time High period	twhc2	—	—	60	—	ns	*4
BLSCLK cycle time Low period	Twlc2	—	—	60	—	ns	*4
Serial-data setup time	tss2	—	—	62	—	ns	*4
Serial-data hold time	tsh2	—	—	62	—	ns	*4
Transceiver interval	tcsw2	—	—	62	—	ns	*4
BLSCE setup time	tcss2	—	—	5	—	ns	*4
BLSCE hold time	tcgh2	—	—	5	—	ns	*4

Note) *4 : Typical Design Value



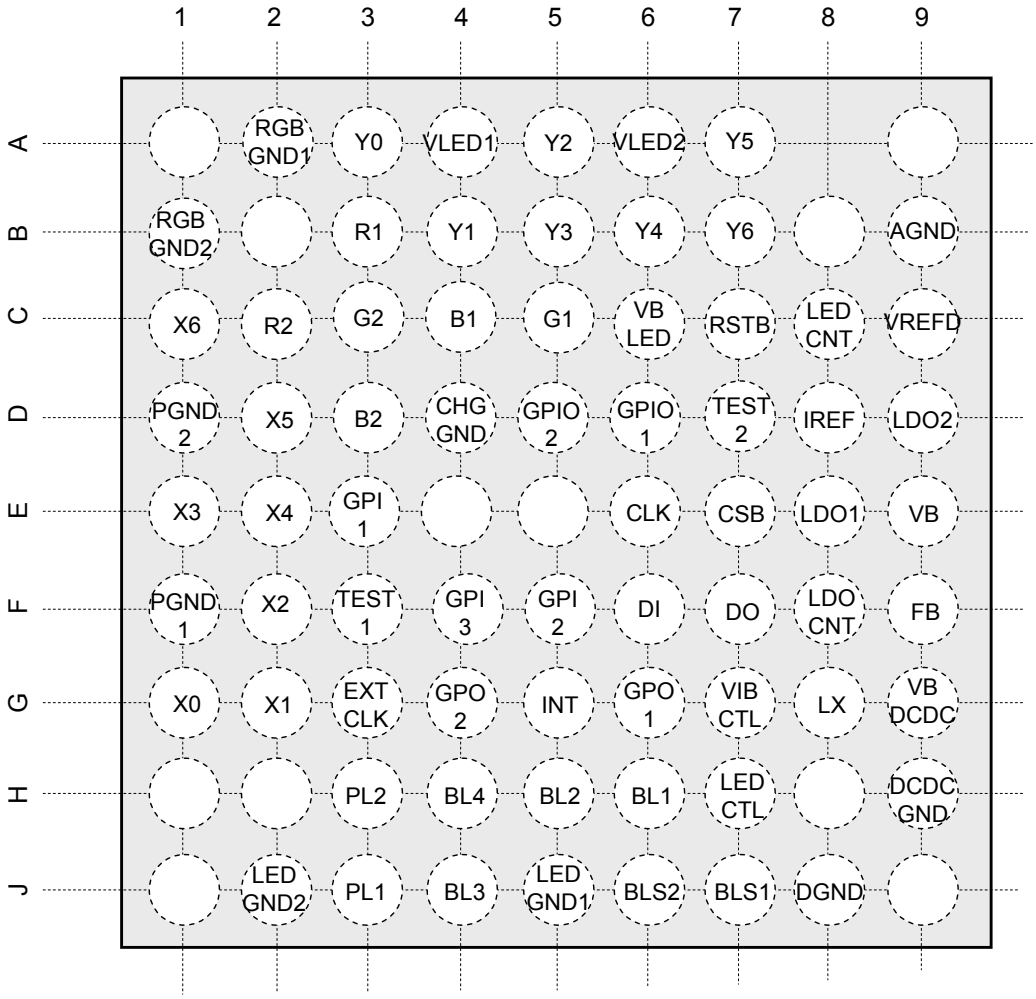


SERSEL	GPI1 terminal	GPI2 terminal	GPI3 terminal	Operation
0	GPI1 operation	GPI2 operation	GPI3 operation	GPIO operation
1	BLSCE operation	BLSCLK operation	BLSDAT operation	SPI2 operation

Established : 2006-08-29
Revised : 2013-04-01

PIN CONFIGURATION

Top View



Established : 2006-08-29
Revised : 2013-04-01

PIN FUNCTIONS

Pin No.	Pin name	Type	Description
G1(1)	X0	Output	Constant current circuit. The output terminal of PWM control. It connects with the 1st Row of matrix LED.
G2(2)	X1	Output	Constant current circuit. The output terminal of PWM control. It connects with the 2nd Row of matrix LED.
F2(3)	X2	Output	Constant current circuit. The output terminal of PWM control. It connects with the 3rd Row of matrix LED.
E1(4)	X3	Output	Constant current circuit. The output terminal of PWM control. It connects with the 4th Row of matrix LED.
F1(5) D1(6)	PGND1 PGND2	Ground	The GND terminal for matrix LED
E2(7)	X4	Output	Constant current circuit. The output terminal of PWM control. It connects with the 5th Row of matrix LED.
D2(8)	X5	Output	Constant current circuit. The output terminal of PWM control. It connects with the 6th Row of matrix LED.
C1(9)	X6	Output	Constant current circuit. The output terminal of PWM control. It connects with the 7th Row of matrix LED.
A3(10)	Y0	Output	Constant current circuit. The output terminal of PWM control. It connects with the A Column of matrix LED.
B4(11)	Y1	Output	Constant current circuit. The output terminal of PWM control. It connects with the B Column of matrix LED.
A5(12)	Y2	Output	Constant current circuit. The output terminal of PWM control. It connects with the C Column of matrix LED.
B5(13)	Y3	Output	Constant current circuit. The output terminal of PWM control. It connects with the D Column of matrix LED.
A4(14) A6(15)	VLED1 VLED2	Power supply	The power supply's connect terminal for matrix LED. Connect with the output of battery or step-up DC/DC converter.
B6(16)	Y4	Output	Constant current circuit. The output terminal of PWM control. It connects with the E Column of matrix LED.
A7(17)	Y5	Output	Constant current circuit. The output terminal of PWM control. It connects with the F Column of matrix LED.
B7(18)	Y6	Output	Constant current circuit. The output terminal of PWM control. It connects with the G Column of matrix LED.

PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
F9(19)	FB	Input	The feedback terminal for step-up DC/DC converter.
H9(20)	DCDCGND	Ground	The GND terminal for step-up DC/DC converter.
G8(21)	LX	Output	The terminal for External Nch-type MOS-Tr Gate driver.
G9(22)	VBDCDC	Power supply	The power supply's connect terminal for step-up DC/DC converter.
B3(23)	R1	Output	LED contact terminal. Control by LEDCNT terminal is also possible.
C5(24)	G1	Output	LED contact terminal.
C4(25)	B1	Output	LED contact terminal.
A2(26) B1(27)	RGBGND1 RGBGND2	Ground	The GND terminal for RGB terminal.
C2(28)	R2	Output	General-purpose output terminal.(Nch-MOS Open Drain)
C3(29)	G2	Output	General-purpose output terminal.(Nch-MOS Open Drain)
D3(30)	B2	Output	General-purpose output terminal.(Nch-MOS Open Drain)
D4(31)	CHGGND	Output	The resistance contact terminal for charge LED.(Connect current restriction resistance between this terminal and GND terminal.)
C6(32)	VBLED	Power supply	Battery voltage's connect terminal. This terminal supplies Power supply to R1 terminal and R2 terminal.
C8(33)	LEDCNT	Input	ON/OFF control terminal of LED connected to R1 terminal and R2 terminal.
D9(34)	LDO2	Output	LDO2 (2.85 V) output terminal.
E9(35)	VB	Power supply	The power supply's connect terminal for BGR circuit and LDO circuit.
E8(36)	LDO1	Output	LDO1 (1.85 V) output terminal.
F8(37)	LDOCNT	Input	ON/OFF control terminal of LDO1 and LDO2.
C9(38)	VREFD	Output	BGR circuit output terminal.
D8(39)	IREF	Output	The resistance connect terminal for constant current value setup.

Established : 2006-08-29
Revised : 2013-04-01

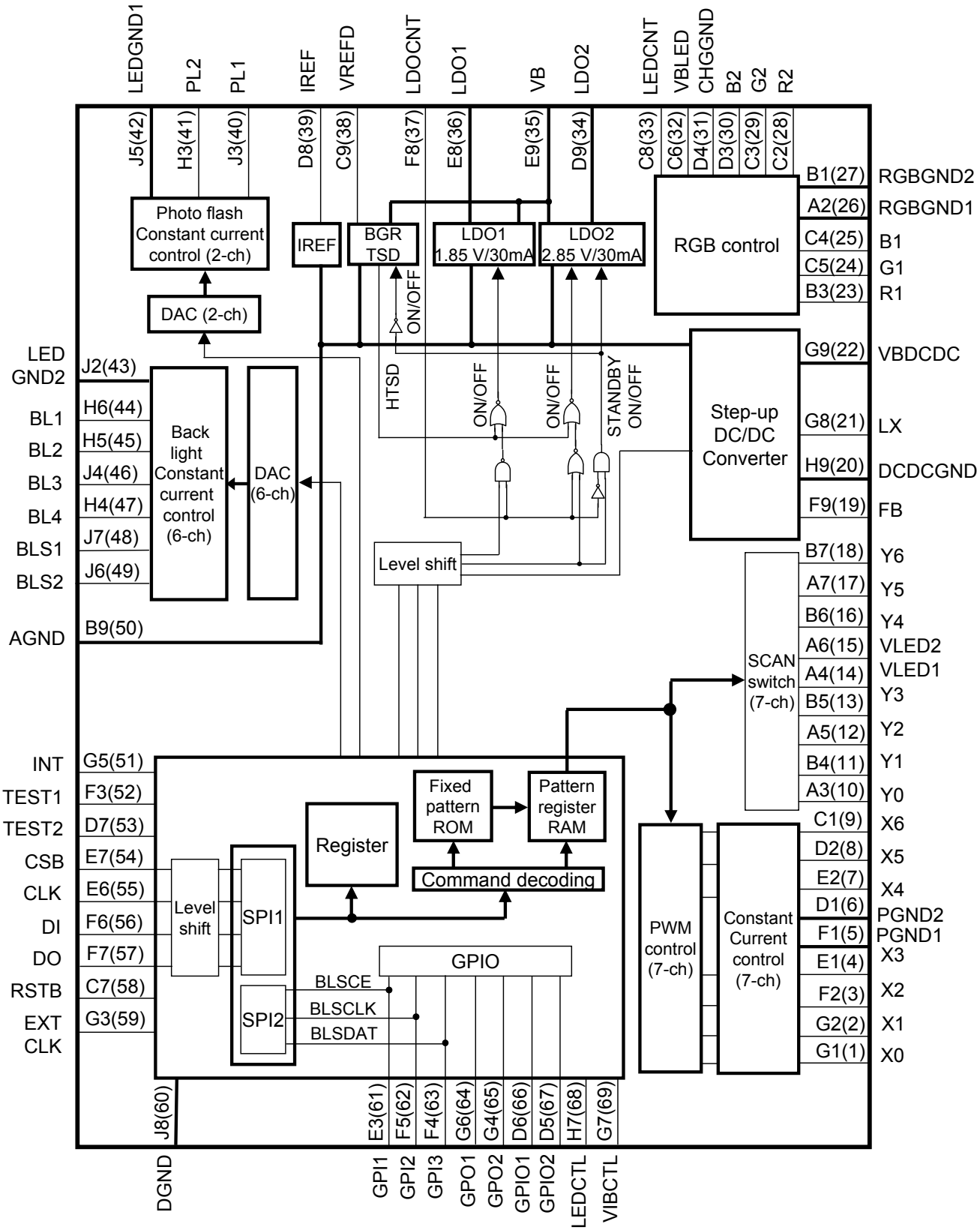
PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
J3(40)	PL1	Output	The constant current output terminal for LED driver. (0 to 61 mA) This terminal is driven with the same current value as PL2 terminal.
H3(41)	PL2	Output	The constant current output terminal for LED driver. (0 to 61 mA) This terminal is driven with the same current value as PL1 terminal.
J5(42) J2(43)	LEDGND1 LEDGND2	Ground	The GND terminal for constant current circuits for LED driver.
H6(44)	BL1	Output	The constant current output terminal for LED driver. (0 to 31 mA) This terminal is driven with the same current value as BL2, BL3 and BL4 terminal.
H5(45)	BL2	Output	The constant current output terminal for LED driver. (0 to 31 mA) This terminal is driven with the same current value as BL1, BL3 and BL4 terminal.
J4(46)	BL3	Output	The constant current output terminal for LED driver. (0 to 31 mA) This terminal is driven with the same current value as BL1, BL2 and BL4 terminal.
H4(47)	BL4	Output	The constant current output terminal for LED driver. (0 to 31 mA) This terminal is driven with the same current value as BL1, BL2 and BL3 terminal.
J7(48)	BLS1	Output	The constant current output terminal for LED driver. (0 to 31 mA) This terminal is driven with the same current value as BLS2 terminal.
J6(49)	BLS2	Output	The constant current output terminal for LED driver. (0 to 31 mA) This terminal is driven with the same current value as BLS1 terminal.
B9(50)	AGND	Ground	The GND terminal for Analog circuitry.
G5(51)	INT	Output	Interrupt output terminal.
F3(52)	TEST1	Input	Test terminal.
D7(53)	TEST2	Input	Test terminal.
E7(54)	CSB	Input	Chip-enable terminal for SPI1 interface.
E6(55)	CLK	Input	Clock input terminal for SPI1 interface.
F6(56)	DI	Input	Data input terminal for SPI1 interface.
F7(57)	DO	Output	Data output terminal for SPI1 interface.
C7(58)	RSTB	Input	Reset input terminal

PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
G3(59)	EXTCLK	Input	External clock input terminal. (It can operate by the clock frequency of a maximum of 1.44 MHz.)
J8(60)	DGND	Ground	The GND terminal for Logic circuitry.
E3(61)	GPI1	Input	GPI input port terminal. (Chip-enable terminal for SPI2 interface.)
F5(62)	GPI2	Input	GPI input port terminal. (Clock input terminal for SPI2 interface.)
F4(63)	GPI3	Input	GPI input port terminal. (Data input terminal for SPI2 interface.)
G6(64)	GPO1	Output	GPO output port terminal.
G4(65)	GPO2	Output	GPO output port terminal.
D6(66)	GPIO1	Input / Output	GPIO input/output port terminal.
D5(67)	GPIO2	Input / Output	GPIO input/output port terminal.
H7(68)	LEDCTL	Input	LED's lighting ON/OFF control terminal. (It is based on register 0Ah.)
G7(69)	VIBCTL	Input	LED's lighting ON/OFF control terminal. (It is based on register 09h.)

FUNCTIONAL BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Explanation of each mode (Power supply startup sequence)

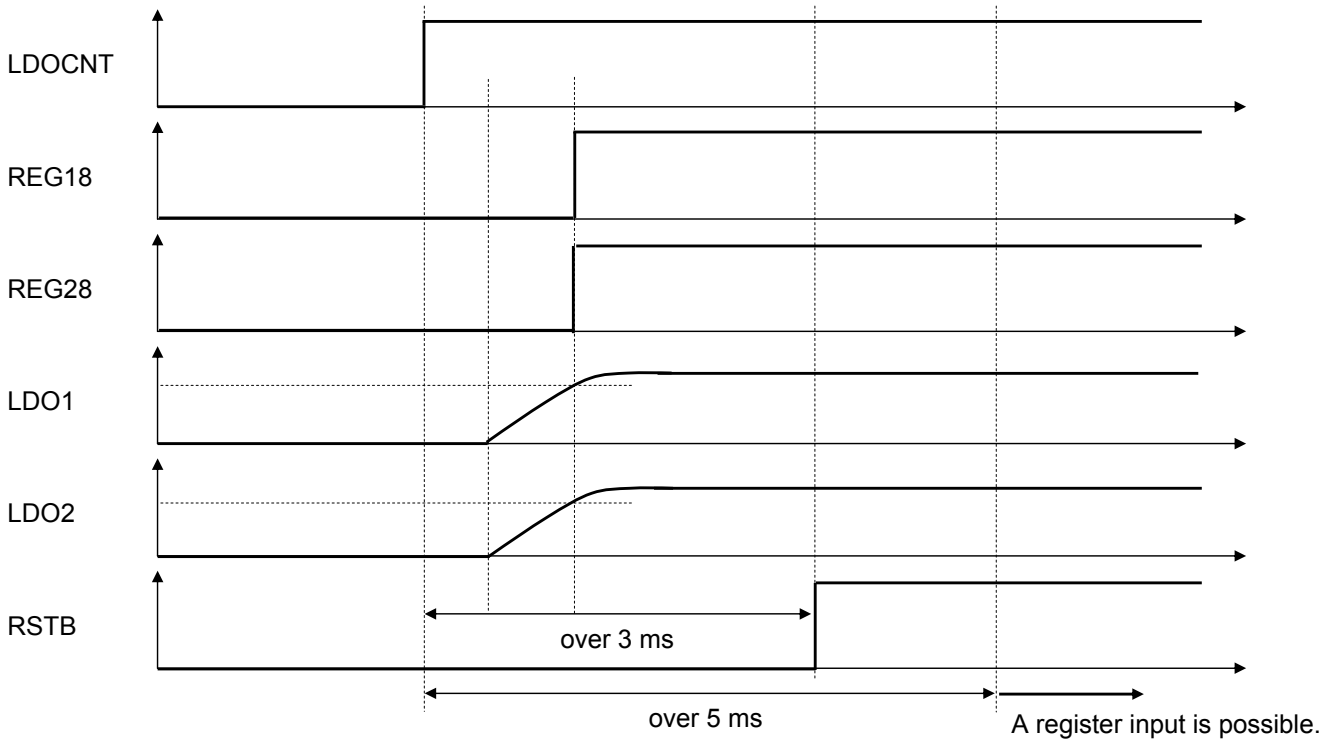
LDOCNT	REG18	REG28	Itotal typ (μA)	Notes
Low (Initial condition)	OFF	OFF	< 1	• It is necessary to make it LDOCNT = High for the return from OFF-mode. • RSTB = Low is forbidden at OFF-mode. (An internal circuit becomes unfixed.) • Do not impress voltage to GPI1, GPI2, GPI3, GPIO1, and GPIO2 terminal at OFF-mode.
Low → High	N.C. (ON)	N.C. (ON)	18	—
High	N.C. (ON)	N.C. (ON)	18	• The signal from serial interface is not received in LDOCNT = Low and the state of REG28 = Low or REG18 = Low. • It shifts to standby mode with LDOCNT = Low and REG28 = High. • The signal from serial interface is not received at Standby-mode. (Power supply for Logic is LDO1 and LDO2.) Therefore, standby release by the signal from serial interface cannot be performed. • In Standby-mode, if LDOCNT is switched to High from Low, it will return to the normal mode. • It cannot shift to OFF-mode from Standby-mode. Once returning to the normal mode, please shift to OFF-mode. • RSTB = Low is prohibited in Standby-mode. (An internal circuit becomes unfixed.) • Do not impress voltage to GPI1, GPI2, GPI3, GPIO1, and GPIO2 terminal in Standby-mode.
High → Low	N.C. (OFF)	Low : OFF At OFF mode	< 1 (OFF mode) or 8 (Standby mode)	• Regardless of the value of REG18, LDO1 turns on at LDOCNT = High. • Regardless of the value of REG28, LDO2 turns on at LDOCNT = High. • Serial interface signal is not received at RSTB = Low • 5 ms after being set to LDOCNT = High, the receptionist of serial interface signal is attained. • To activate RSTB, RSTB should be kept low for more than one internal clock period. • RSTB terminal prohibits the input signal of those other than a rectangle wave.
	Low : OFF High : ON	High : ON At Standby mode		

Established : 2006-08-29
Revised : 2013-04-01

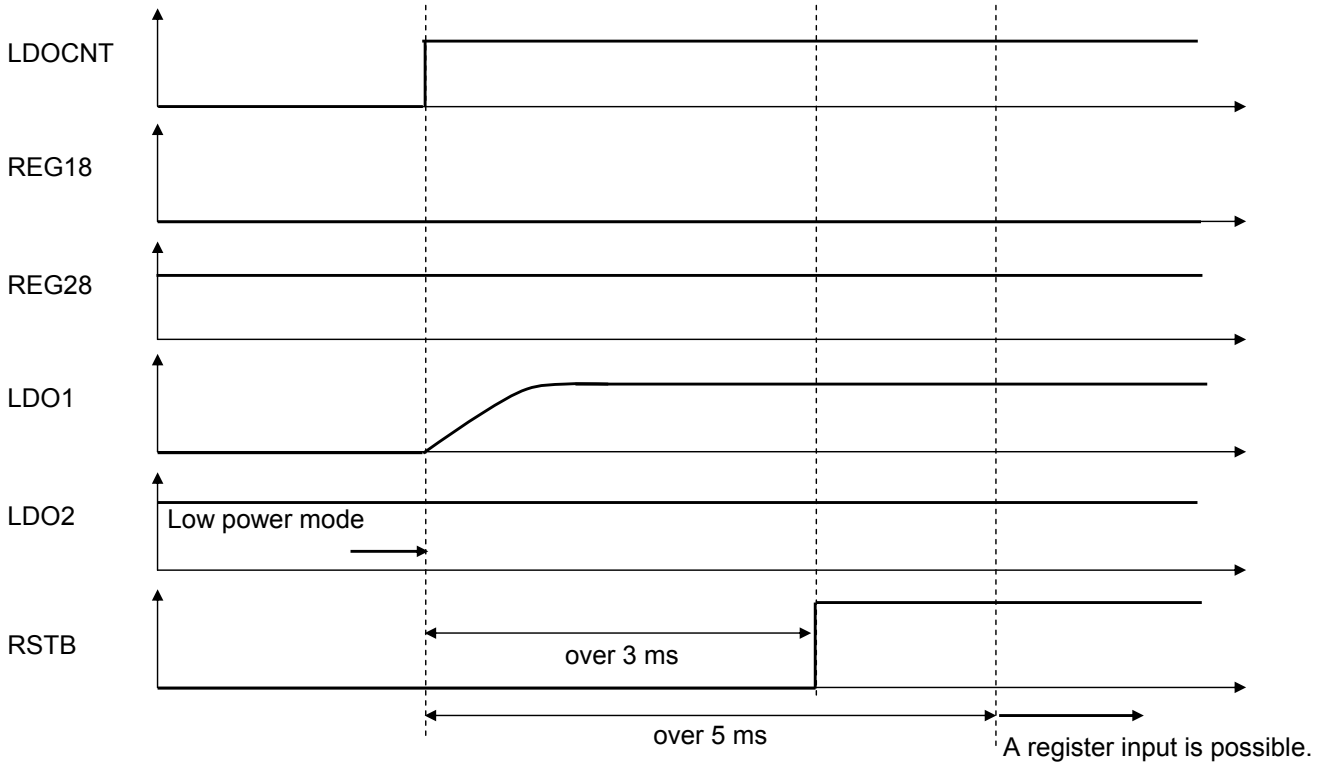
OPERATION (continued)

1. Explanation of each mode (Power supply startup sequence) (continued)

- Shift to the Normal mode from OFF-mode



- Shift to the Normal mode from Standby mode



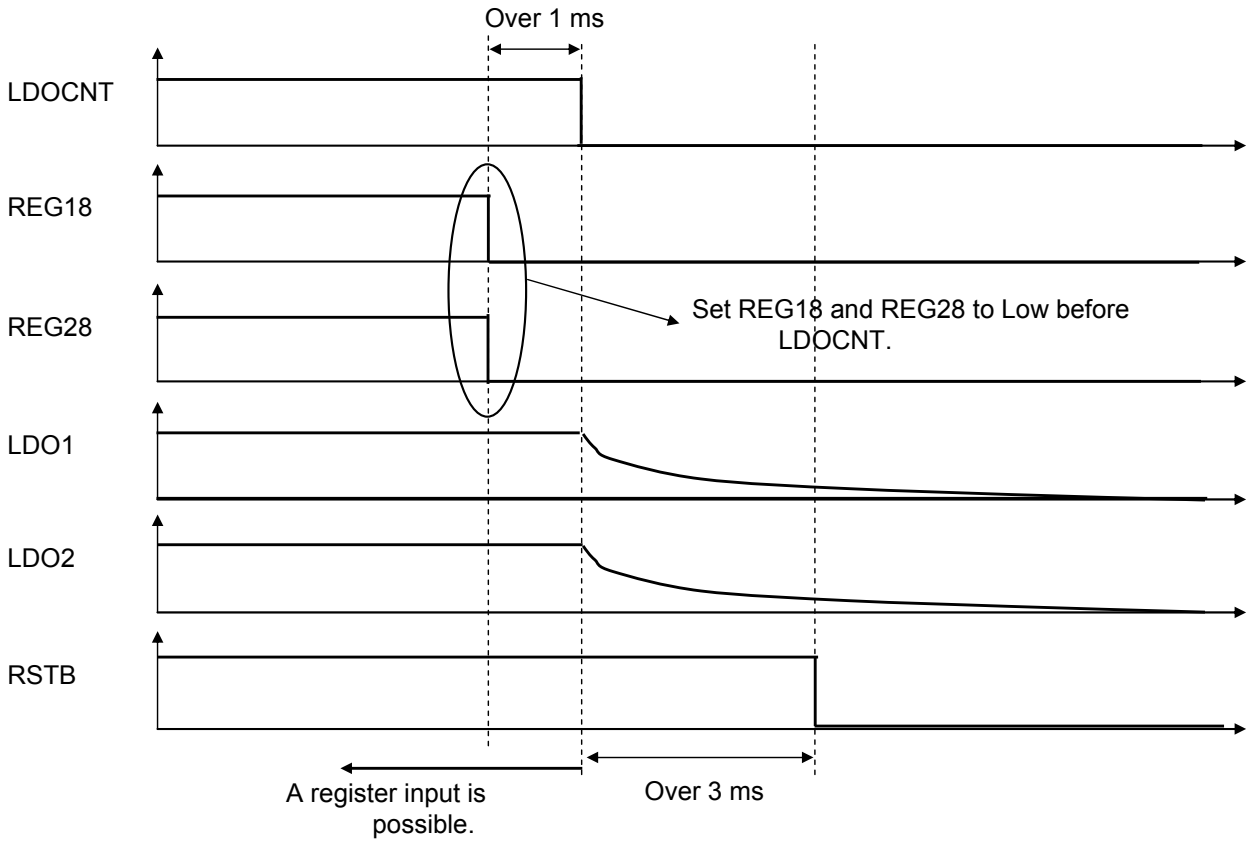
* This is the waveform in the case of applying reset to register setup at Standby mode.
* Maintain the state of RSTB = High to hold the register setup.

Established : 2006-08-29
Revised : 2013-04-01

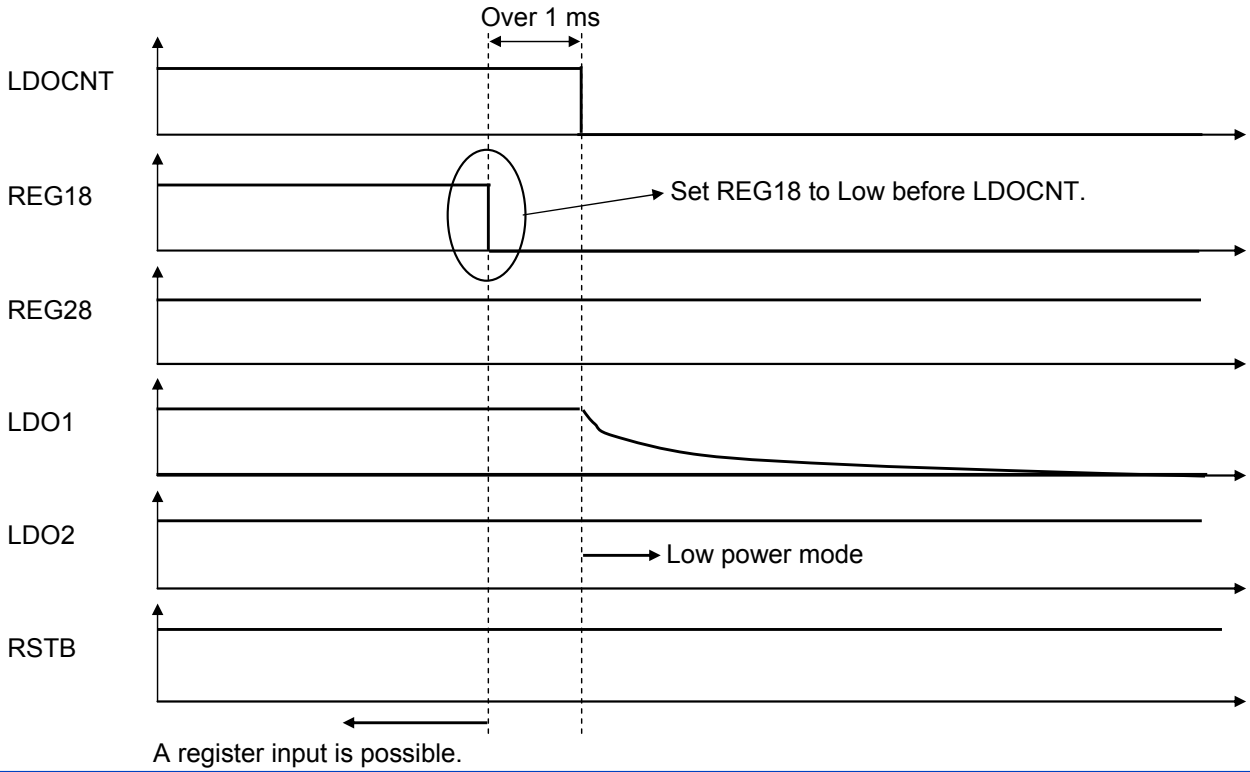
OPERATION (continued)

1. Explanation of each mode (Power supply startup sequence) (continued)

• Shift to the OFF-mode from Normal mode



• Shift to the Standby mode from Normal mode



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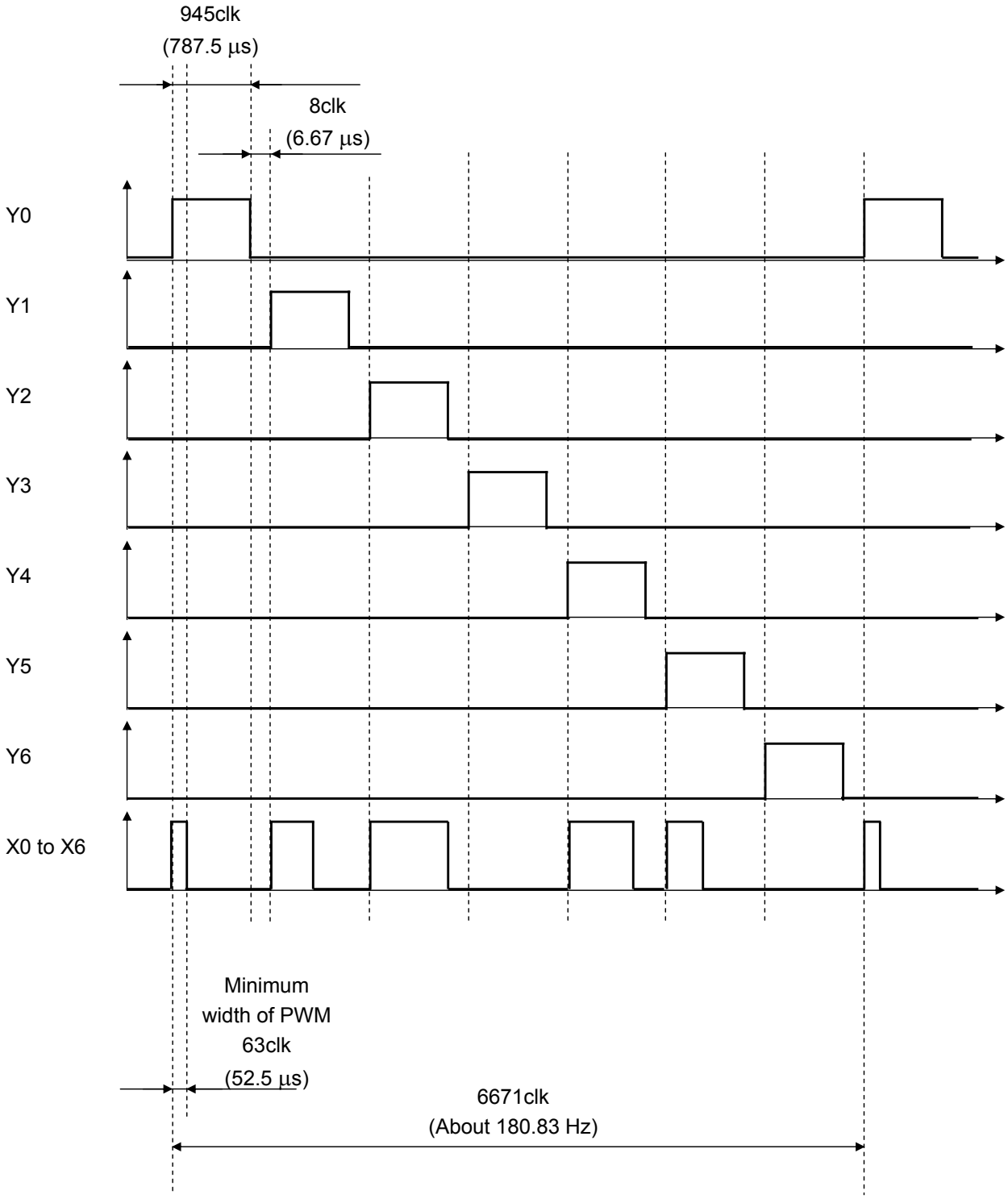
Revised : 2013-04-01

OPERATION (continued)

2. Explanation of operation

Matrix part operation waveform

The following waveform is an internal signal.
In following Yx = Xx = Low, the waveform of actual Yx terminal is set to Hi-Z.



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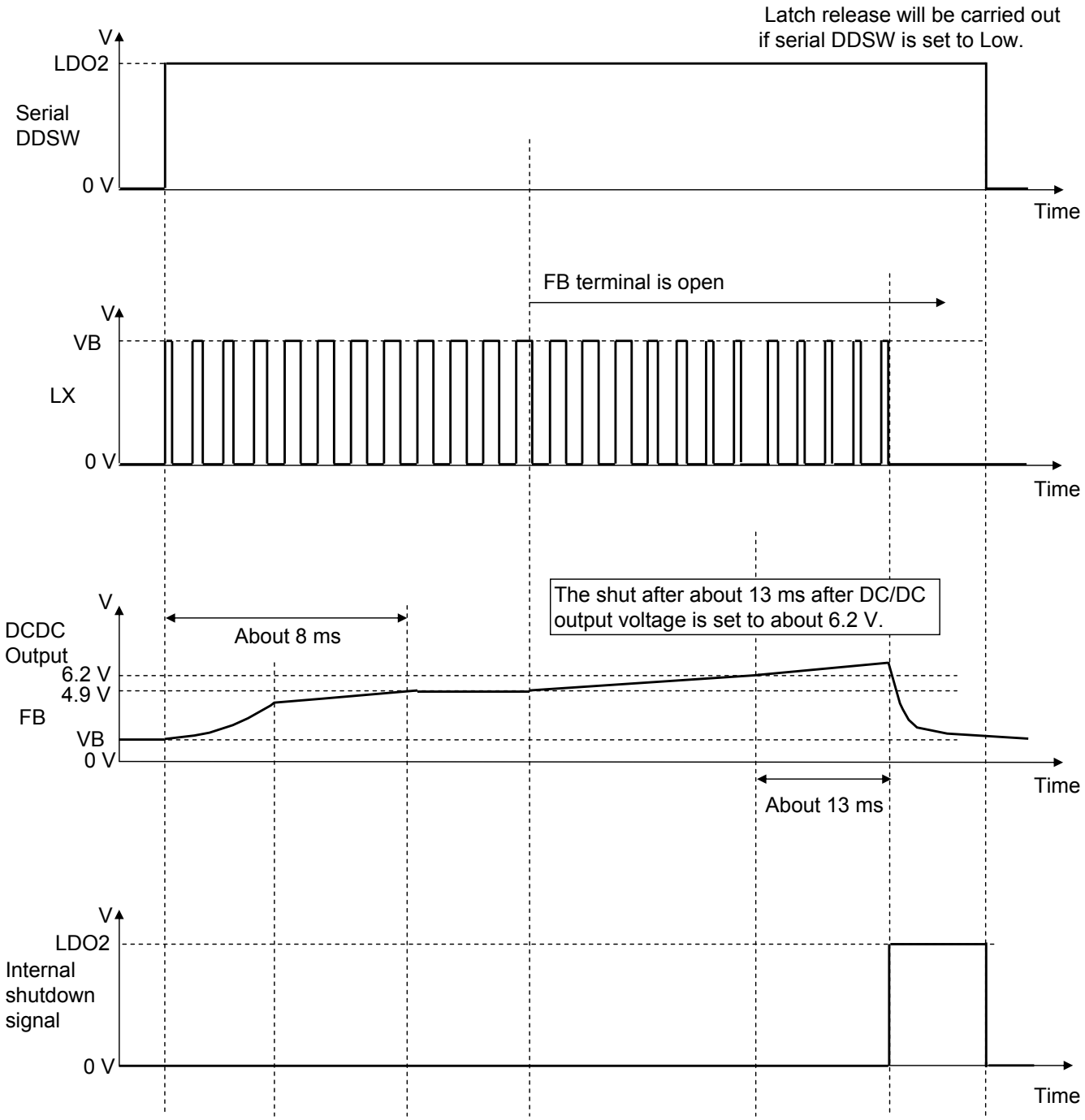
OPERATION (continued)

2. Explanation of operation (continued)

Explanation of excess voltage protection circuit of operation



Established : 2006-08-29
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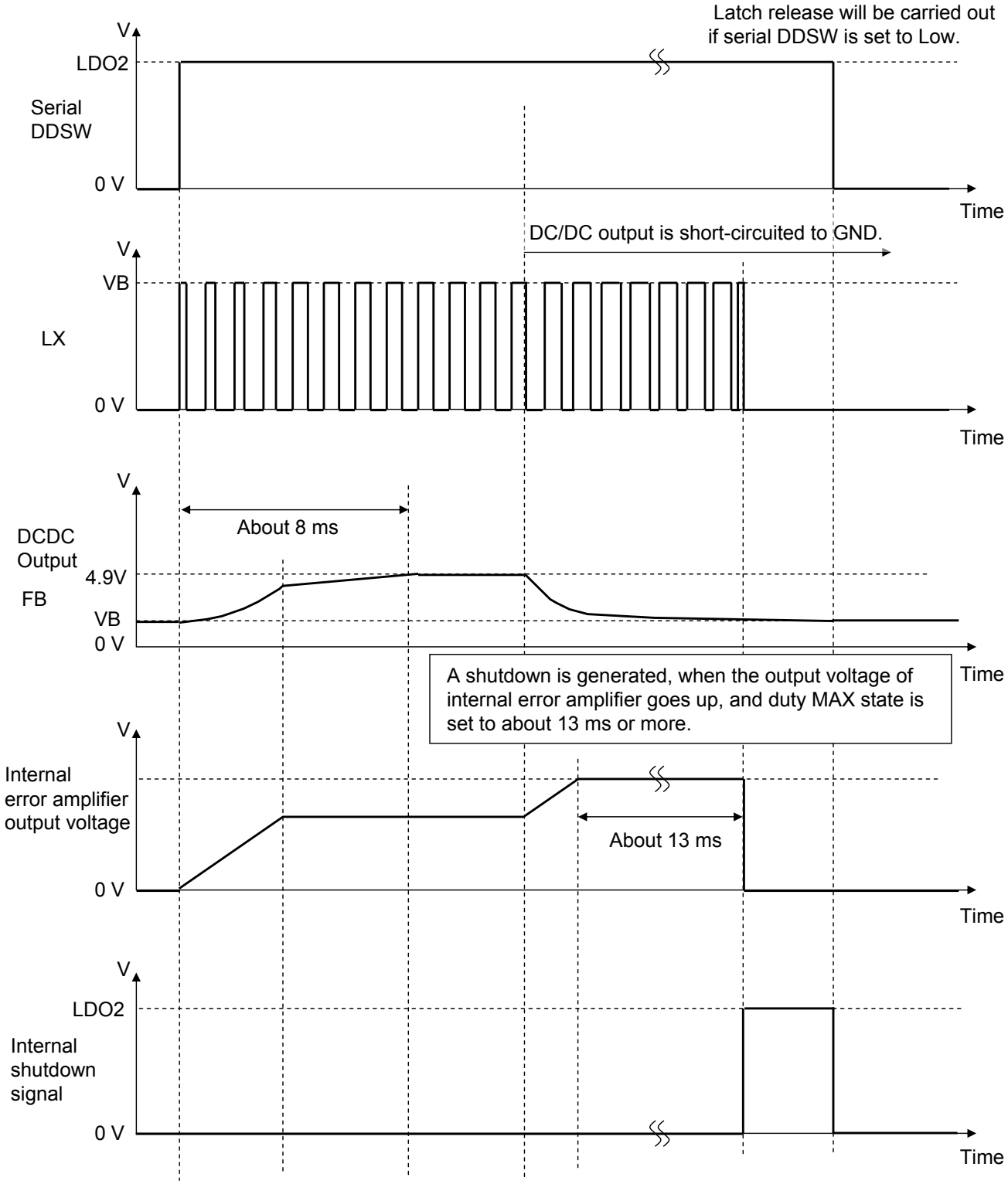
OPERATION (continued)

2. Explanation of operation (continued)

Explanation of over-current protection circuit of operation

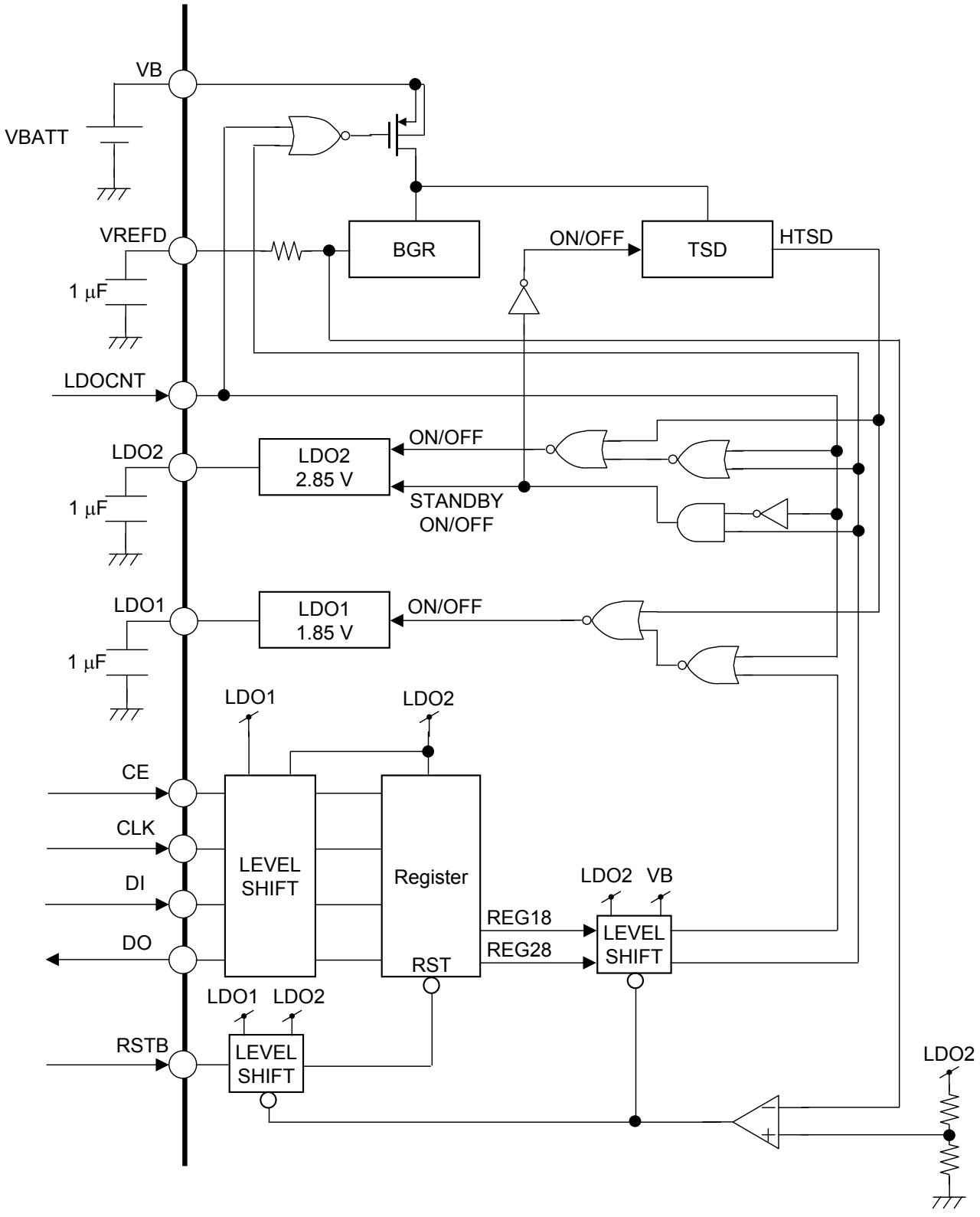


Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

3. Block configuration

RESET part block configuration



All the logic portions to which the power supply is not connected are connected to VB as power supplies.

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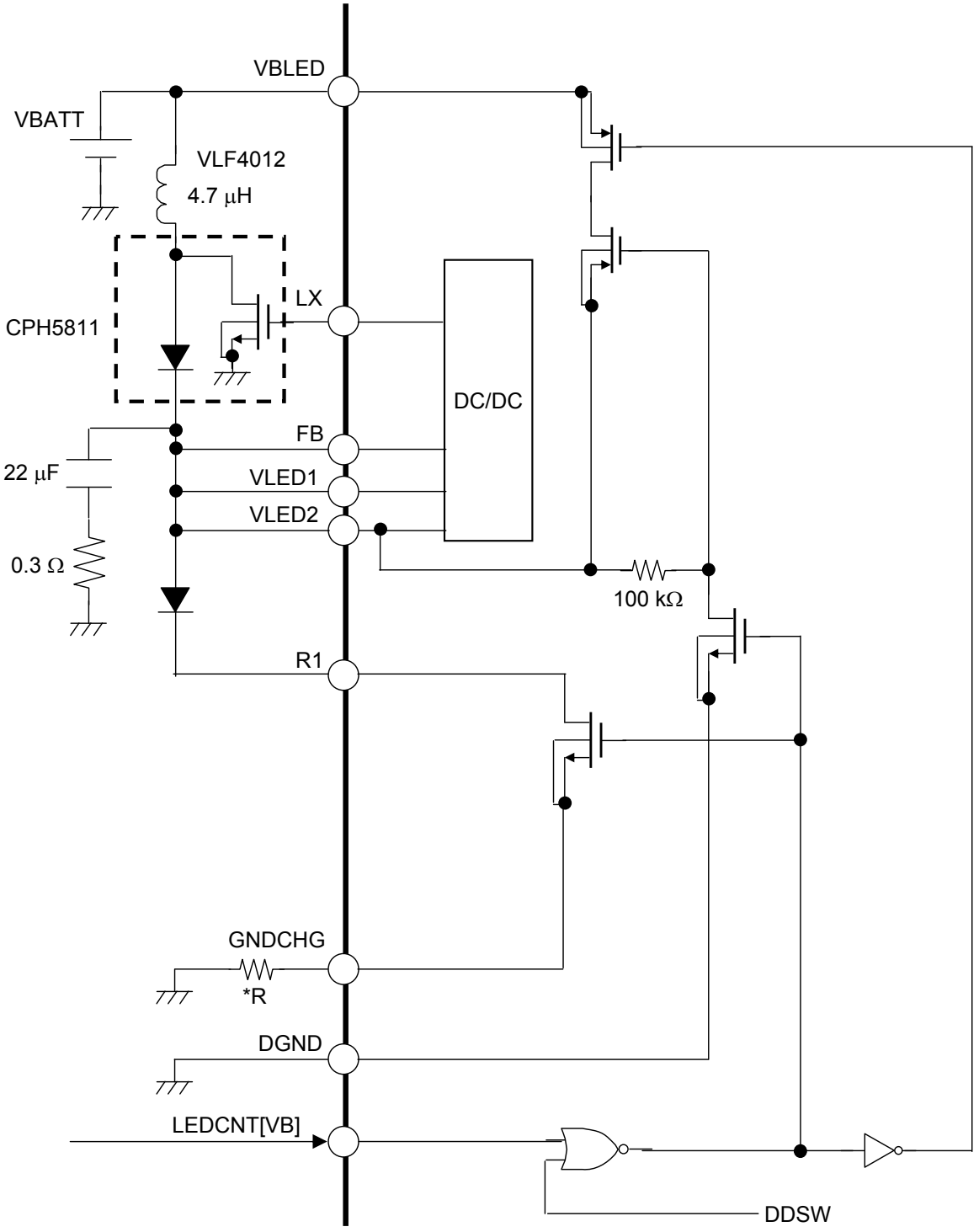
Revised : 2013-04-01

OPERATION (continued)

3. Block configuration (continued)

The LED part for charge block configuration



This function cannot be used when DC/DC converter is active.

All the logic portions to which the power supply is not connected are connected to VB as power supplies.
Adjust R value with the LED and current you use.

Established : 2006-08-29
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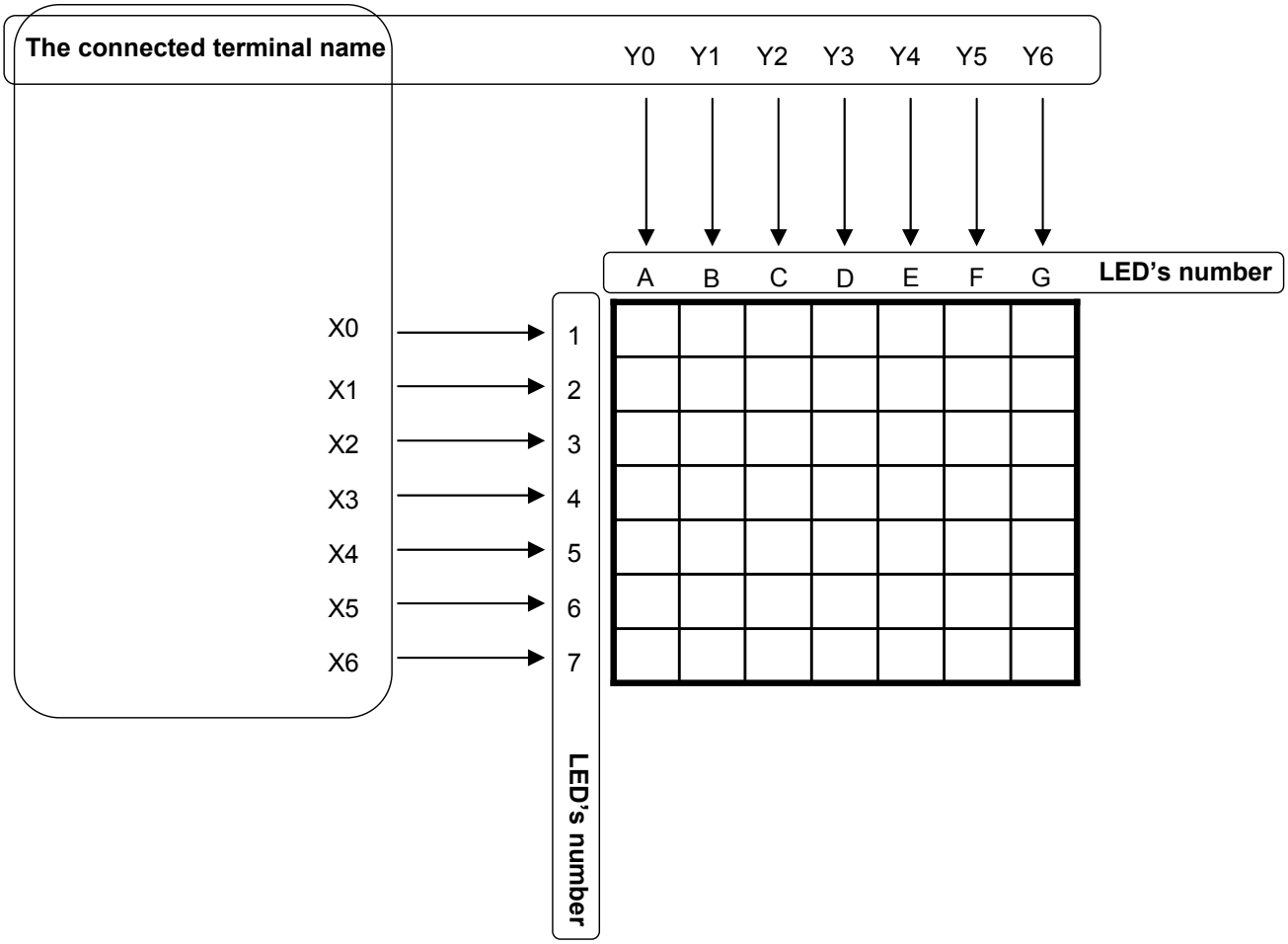
OPERATION (continued)

3. Block configuration (continued)

Explanation of matrix LED part, matrix LED's number



Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address

Register Map

Sub Address	R/W	Data Name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	W	POWERCNT	—	—	—	—	VFOFF	OSCEN	DCOSEL	DDSW
02h	W	LDOCNT	—	—	—	—	—	—	REG18	REG28
03h	W	SERSEL	—	—	—	—	—	—	—	SERSEL
04h	R	LSIVER	LSIVER[7:0]							
05h	W	LCDMAIN	—	—	—	LCDMAIN[4:0]				
06h	W	LCDSUB	—	—	—	LCDSUB[4:0]				
07h	W	PLCNT	—	—	HIEN	PLCNT[4:0]				
08h	W	PWMCNT	—	BL1M	BL2M	BL3M	BL4M	BLS1M	BLS2M	PWMCLK
09h	W	VIBCTL	VIBACT	VIBPL1	VIBPL2	VIBSUB1	VIBSUB2	VIBMTX	VIBRGB1	—
0Ah	W	LEDCTL	LEDACT	DISPL1	DISPL2	DISSUB1	DISSUB2	DISMTX	DISRGB1	—
10h	W/R	GPIOCNT	—	—	—	—	—	—	—	GPIOCLK
11h	W/R	IOSEL	—	—	—	—	—	—	IOSEL1	IOSEL2
12h	W/R	IOMSK	—	—	—	IMSK1	IMSK2	IMSK3	IOMSK1	IMSK2
13h	W/R	IOOUT	—	—	—	—	OOUT1	OOUT2	IOOUT1	IOOUT2
14h	R	IOFACTOR	FACGD1	ERR2EH	—	—	RAMACT	FRMINT	CPUWRER	TSD
15h	R	IOSTATE	STAGD	—	—	ISTA1	ISTA2	ISTA3	IOSTA1	IOSTA2
16h	W/R	ICHAT	—	—	ICHAT1[1:0]		ICHAT2[1:0]		ICHAT3[1:0]	
17h	W/R	IOCHAT	—	—	—	—	IOCHAT1[1:0]		IOCHAT2[1:0]	
18h	W/R	IODET	—	—	—	—	IDET[1:0]		IODET[1:0]	
19h	W/R	IOPLUD	—	—	—	R2ON	G2ON	B2ON	IOPLUD1	IOPLUD2
1Ah	W/R	VDDSEL	INTVSEL	—	—	—	OVSEL1	OVSEI2	IOVSEL1	IOVSEL2

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OPERATION (continued)

4. Register and Address (continued)

Register Map (continued)

Sub Address	R/W	Data Name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	MTXON	—	—	—	—	—	—	—	MTXON
21h	R/W	MTXDATA	MTXDATA[7:0]							
22h	R/W	FFROM	—	—	—	—	—	—	ROM77[1:0]	
23h	R/W	ROMSEL	SELROM[7:0]							
24h	R/W	RAMCOPY	—	—	—	—	—	—	SELRAM	COPYSTART
25h	R/W	SETFROM	SETFROM[7:0]							
26h	R/W	SETTO	SETTO[7:0]							
27h	R/W	REPON	—	—	—	—	—	—	—	REPON
28h	R/W	SETTIME	—	—	—	—	—	—	SETTIME[1:0]	
29h	R/W	RAMRST	—	—	—	—	—	—	RAM1	RAM2
2Ah	R/W	SCROLL	—	—	—	—	—	—	—	SCLON
2Bh	R/W	SCLTIME	—	—	—	—	—	—	SCLTIME[1:0]	
2Ch	R/W	RGBON	—	—	—	—	—	—	—	RGBON
2Dh	R/W	RGBDATA	—	—	RGBDATA[5:0]					
2Eh	R	ERROR	FACGD2	SCP	OVP	IFAC1	IFAC2	IFAC3	IOFAC1	IOFAC2
30h	R/W	RAMNUM	—	—	—	—	—	—	—	RAMNUM
6Bh	R/W	PROT1	—	—	—	—	—	—	—	PROT1
6Dh	R/W	PROT2	—	—	—	PROT2	—	—	—	—
6Fh	R/W	PROT3	PROT3	—	—	—	—	—	—	—
70h	R/W	TEST1	TEST1							
71h	R/W	TEST2	TEST2							
72h	R/W	TEST3	TEST3							
73h	R/W	TEST4	TEST4							
74h	R/W	TEST5	TEST5							
75h	R/W	TEST6	TEST6							
76h	R/W	TEST7	TEST6							
77h	R/W	TEST8	TEST7							

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OPERATION (continued)

4. Register and Address (continued)

RAM Address Map

Sub Address	Data Name	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	A1	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
32h	A2	BLA2[3:0]				FRA2[1:0]		DLA2[1:0]	
33h	A3	BLA3[3:0]				FRA3[1:0]		DLA3[1:0]	
34h	A4	BLA4[3:0]				FRA4[1:0]		DLA4[1:0]	
35h	A5	BLA5[3:0]				FRA5[1:0]		DLA5[1:0]	
36h	A6	BLA6[3:0]				FRA6[1:0]		DLA6[1:0]	
37h	A7	BLA7[3:0]				FRA7[1:0]		DLA7[1:0]	
38h	B1	BLB1[3:0]				FRB1[1:0]		DLB1[1:0]	
39h	B2	BLB2[3:0]				FRB2[1:0]		DLB2[1:0]	
3Ah	B3	BLB3[3:0]				FRB3[1:0]		DLB3[1:0]	
3Bh	B4	BLB4[3:0]				FRB4[1:0]		DLB4[1:0]	
3Ch	B5	BLB5[3:0]				FRB5[1:0]		DLB5[1:0]	
3Dh	B6	BLB6[3:0]				FRB6[1:0]		DLB6[1:0]	
3Eh	B7	BLB7[3:0]				FRB7[1:0]		DLB7[1:0]	
3Fh	C1	BLC1[3:0]				FRC1[1:0]		DLC1[1:0]	
40h	C2	BLC2[3:0]				FRC2[1:0]		DLC2[1:0]	
41h	C3	BLC3[3:0]				FRC3[1:0]		DLC3[1:0]	
42h	C4	BLC4[3:0]				FRC4[1:0]		DLC4[1:0]	
43h	C5	BLC5[3:0]				FRC5[1:0]		DLC5[1:0]	
44h	C6	BLC6[3:0]				FRC6[1:0]		DLC6[1:0]	
45h	C7	BLC7[3:0]				FRC7[1:0]		DLC7[1:0]	
46h	D1	BLD1[3:0]				FRD1[1:0]		DLD1[1:0]	
47h	D2	BLD2[3:0]				FRD2[1:0]		DLD2[1:0]	
48h	D3	BLD3[3:0]				FRD3[1:0]		DLD3[1:0]	
49h	D4	BLD4[3:0]				FRD4[1:0]		DLD4[1:0]	
4Ah	D5	BLD5[3:0]				FRD5[1:0]		DLD5[1:0]	
4Bh	D6	BLD6[3:0]				FRD6[1:0]		DLD6[1:0]	
4Ch	D7	BLD7[3:0]				FRD7[1:0]		DLD7[1:0]	

OPERATION (continued)

4. Register and Address (continued)

RAM Address Map (continued)

Sub Address	Data Name	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
4Dh	E1	BLE1[3:0]				FRE1[1:0]		DLE1[1:0]	
4Eh	E2	BLE2[3:0]				FRE2[1:0]		DLE2[1:0]	
4Fh	E3	BLE3[3:0]				FRE3[1:0]		DLE3[1:0]	
50h	E4	BLE4[3:0]				FRE4[1:0]		DLE4[1:0]	
51h	E5	BLE5[3:0]				FRE5[1:0]		DLE5[1:0]	
52h	E6	BLE6[3:0]				FRE6[1:0]		DLE6[1:0]	
53h	E7	BLE7[3:0]				FRE7[1:0]		DLE7[1:0]	
54h	F1	BLF1[3:0]				FRF1[1:0]		DLF1[1:0]	
55h	F2	BLF2[3:0]				FRF2[1:0]		DLF2[1:0]	
56h	F3	BLF3[3:0]				FRF3[1:0]		DLF3[1:0]	
57h	F4	BLF4[3:0]				FRF4[1:0]		DLF4[1:0]	
58h	F5	BLF5[3:0]				FRF5[1:0]		DLF5[1:0]	
59h	F6	BLF6[3:0]				FRF6[1:0]		DLF6[1:0]	
5Ah	F7	BLF7[3:0]				FRF7[1:0]		DLF7[1:0]	
5Bh	G1	BLG1[3:0]				FRG1[1:0]		DLG1[1:0]	
5Ch	G2	BLG2[3:0]				FRG2[1:0]		DLG2[1:0]	
5Dh	G3	BLG3[3:0]				FRG3[1:0]		DLG3[1:0]	
5Eh	G4	BLG4[3:0]				FRG4[1:0]		DLG4[1:0]	
5Fh	G5	BLG5[3:0]				FRG5[1:0]		DLG5[1:0]	
60h	G6	BLG6[3:0]				FRG6[1:0]		DLG6[1:0]	
61h	G7	BLG7[3:0]				FRG7[1:0]		DLG7[1:0]	
62h	LEDR1	BLLEDR1[3:0]				FRLEDR1[1:0]		DLLEDR1[1:0]	
63h	LEDG1	BLLEDG1[3:0]				FRLEDG1[1:0]		DLLEDG1[1:0]	
64h	LEDB1	BLLEDB1[3:0]				FRLEDB1[1:0]		DLLEDB1[1:0]	

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OPERATION (continued)

4. Register and Address (continued)

ROM Address Map

[00000000] - [10010101] : ROM(Only luminosity) 7 × 7 Pattern No.0 (default) to Pattern No.149

Pattern No.	Contents of the pattern	Display
0	All putting out lights	Nothing
1	Number	0
2	Number	1
3	Number	2
4	Number	3
5	Number	4
6	Number	5
7	Number	6
8	Number	7
9	Number	8
10	Number	9
11	Alphabetic character	A
12	Alphabetic character	B
13	Alphabetic character	C
14	Alphabetic character	D
15	Alphabetic character	E
16	Alphabetic character	F
17	Alphabetic character	G
18	Alphabetic character	H
19	Alphabetic character	I
20	Alphabetic character	J
21	Alphabetic character	K
22	Alphabetic character	L
23	Alphabetic character	M
24	Alphabetic character	N
25	Alphabetic character	O
26	Alphabetic character	P
27	Alphabetic character	Q
28	Alphabetic character	R
29	Alphabetic character	S
30	Alphabetic character	T

Pattern No.	Contents of the pattern	Display
31	Alphabetic character	U
32	Alphabetic character	V
33	Alphabetic character	W
34	Alphabetic character	X
35	Alphabetic character	Y
36	Alphabetic character	Z
37	Alphabetic character	a
38	Alphabetic character	b
39	Alphabetic character	c
40	Alphabetic character	d
41	Alphabetic character	e
42	Alphabetic character	f
43	Alphabetic character	g
44	Alphabetic character	h
45	Alphabetic character	i
46	Alphabetic character	j
47	Alphabetic character	k
48	Alphabetic character	l
49	Alphabetic character	m
50	Alphabetic character	n
51	Alphabetic character	o
52	Alphabetic character	p
53	Alphabetic character	q
54	Alphabetic character	r
55	Alphabetic character	s
56	Alphabetic character	t
57	Alphabetic character	u
58	Alphabetic character	v
59	Alphabetic character	w
60	Alphabetic character	x
61	Alphabetic character	y

Established : 2006-08-29
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OPERATION (continued)

4. Register and Address (continued)

ROM Address Map (continued)

[00000000] - [10010101] : ROM(Only luminosity) 7 × 7 Pattern No.0 (default) to Pattern No.149

Pattern No.	Contents of the pattern	Display
62	Alphabetic character	z
63	Katakana	ア
64	Katakana	ァ
65	Katakana	イ
66	Katakana	ィ
67	Katakana	ウ
68	Katakana	ゥ
69	Katakana	エ
70	Katakana	ェ
71	Katakana	オ
72	Katakana	ォ
73	Katakana	カ
74	Katakana	キ
75	Katakana	ク
76	Katakana	ケ
77	Katakana	コ
78	Katakana	サ
79	Katakana	シ
80	Katakana	ス
81	Katakana	セ
82	Katakana	ソ
83	Katakana	タ
84	Katakana	チ
85	Katakana	ツ
86	Katakana	ッ
87	Katakana	テ
88	Katakana	ト
89	Katakana	ナ
90	Katakana	ニ
91	Katakana	ヌ
92	Katakana	ネ

Pattern No.	Contents of the pattern	Display
93	Katakana	ノ
94	Katakana	ハ
95	Katakana	ヒ
96	Katakana	フ
97	Katakana	ヘ
98	Katakana	ホ
99	Katakana	マ
100	Katakana	ミ
101	Katakana	ム
102	Katakana	メ
103	Katakana	モ
104	Katakana	ヤ
105	Katakana	ャ
106	Katakana	ユ
107	Katakana	ュ
108	Katakana	ヨ
109	Katakana	ョ
110	Katakana	ラ
111	Katakana	リ
112	Katakana	ル
113	Katakana	レ
114	Katakana	ロ
115	Katakana	ワ
116	Katakana	ヲ
117	Katakana	ン
118	Symbol	゛
119	Symbol	゜
120	Symbol	ー
121	Symbol	Heart
122	Symbol	Mail
123	Symbol	Telephone

Established : 2006-08-29
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OPERATION (continued)

4. Register and Address (continued)

ROM Address Map (continued)

[00000000] - [10010101] : ROM(Only luminosity) 7 × 7 Pattern No.0 (default) to Pattern No.149

Pattern No.	Contents of the pattern	Display
124	Symbol	Zero antenna
125	Symbol	One antenna
126	Symbol	Two antenna
127	Symbol	Three antenna
128	Symbol	+
129	Symbol	–
130	Symbol	×
131	Symbol	÷
132	Symbol	=
133	Symbol	:
134	Symbol	!
135	Symbol	?
136	Symbol	↑
137	Symbol	↓
138	Symbol	←
139	Symbol	→
140	Symbol	〒
141	Symbol	Clock mark
142	Symbol	♪
143	Symbol	○

Pattern No.	Contents of the pattern	Display
144	Symbol	×
145	Symbol	△
146	Symbol	□
147	Symbol	◇
148	Symbol	▽
149	Symbol	¥

Established : 2006-08-29
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OPERATION (continued)

4. Register and Address (continued)

ROM Address Map (continued)

[10010110] - [11010000] : ROM(Luminosity + Cycle + Delay) 7 × 7 Pattern No.150 to Pattern No.208

Pattern No.	Contents of the pattern	Display
150	Gradation	Square out 1 s
151	Gradation	Square out 2 s
152	Gradation	Square out 3 s
153	Gradation	Square in 1 s
154	Gradation	Square in 2 s
155	Gradation	Square in 3 s
156	Gradation	Slant right down 1 s
157	Gradation	Slant right down 2 s
158	Gradation	Slant right down 3 s
159	Gradation	Slant left down 1 s
160	Gradation	Slant left down 2 s
161	Gradation	Slant left down 3 s
162	Gradation	Slant right up 1 s
163	Gradation	Slant right up 2 s
164	Gradation	Slant right up 3 s
165	Gradation	Slant left up 1 s
166	Gradation	Slant left up 2 s
167	Gradation	Slant left up 3 s
168	Gradation	Down 1 s
169	Gradation	Down 2 s
170	Gradation	Down 3 s
171	Gradation	Up 1 s
172	Gradation	Up 2 s
173	Gradation	Up 3 s

Pattern No.	Contents of the pattern	Display
174	Gradation	Right 1 s
175	Gradation	Right 2 s
176	Gradation	Right 3 s
177	Gradation	Left 1 s
178	Gradation	Left 2 s
179	Gradation	Left 3 s
180	Gradation	Slant right center 1 s
181	Gradation	Slant right center 2 s
182	Gradation	Slant right center 3 s
183	Gradation	Slant left center 1 s
184	Gradation	Slant left center 2 s
185	Gradation	Slant left center 3 s
186	Gradation	Vertical center 1 s
187	Gradation	Vertical center 2 s
188	Gradation	Vertical center 3 s
189	Gradation	Side center 1 s
190	Gradation	Side center 2 s
191	Gradation	Side center 3 s
192	Gradation	Square right down 1 s
193	Gradation	Square right down 2 s
194	Gradation	Square right down 3 s

Established : 2006-08-29
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OPERATION (continued)

4. Register and Address (continued)

ROM Address Map (continued)

[10010110] - [11010000] : ROM(Luminosity + Cycle + Delay) 7 × 7 Pattern No.150 to Pattern No.208

Pattern No.	Contents of the pattern	Display
195	Gradation	Square left down 1 s
196	Gradation	Square left down 2 s
197	Gradation	Square left down 3 s
198	Gradation	Square right up 1 s
199	Gradation	Square right up 2 s
200	Gradation	Square right up 3 s
201	Gradation	Square left up 1 s
202	Gradation	Square left up2 s
203	Gradation	Square left up 3 s
204	Gradation	Square crossing in 1 s
205	Gradation	Square crossing in 2 s
206	Gradation	Square crossing in 3 s
207	Gradation	Square crossing out1 s
208	Gradation	Square crossing out2 s

OPERATION (continued)

4. Register and Address (continued)

ROM Address Map (continued)

[000001] - [101010] : ROM(RGB pattern, Luminosity + Cycle + Delay)RGB pattern No.1 to No.42

Pattern No.	Contents of the pattern	Display
1	Color 1	Turn on : Blue
2	Color 2	Turn on : Between 1 and 3
3	Color 3	Turn on : Green + Blue
4	Color 4	Turn on : Between 3 and 5
5	Color 5	Turn on : Green
6	Color 6	Turn on : Between 5 and 7
7	Color 7	Turn on : Red + Green
8	Color 8	Turn on : Between 7 and 9
9	Color 9	Turn on : Red
10	Color 10	Turn on : Red + Blue
11	Color 11	Turn on : Between 9 and 10
12	Color 12	Turn on : Red + Blue + Green
13	Color 1 Firefly 1 s	Firefly 1 s : Color 1
14	Color 2 Firefly 1 s	Firefly 1 s : Color 2
15	Color 3 Firefly 1 s	Firefly 1 s : Color 3
16	Color 4 Firefly 1 s	Firefly 1 s : Color 4
17	Color 5 Firefly 1 s	Firefly 1 s : Color 5
18	Color 6 Firefly 1 s	Firefly 1 s : Color 6
19	Color 7 Firefly 1 s	Firefly 1 s : Color 7
20	Color 8 Firefly 1 s	Firefly 1 s : Color 8
21	Color 9 Firefly 1 s	Firefly 1 s : Color 9
22	Color 10 Firefly 1 s	Firefly 1 s : Color 10
23	Color 11 Firefly 1 s	Firefly 1 s : Color 11
24	Color 12 Firefly 1 s	Firefly 1 s : Color 12

Pattern No.	Contents of the pattern	Display
25	Color 1 Firefly 2 s	Firefly 2 s : Color 1
26	Color 2 Firefly 2 s	Firefly 2 s : Color 2
27	Color 3 Firefly 2 s	Firefly 2 s : Color 3
28	Color 4 Firefly 2 s	Firefly 2 s : Color 4
29	Color 5 Firefly 2 s	Firefly 2 s : Color 5
30	Color 6 Firefly 2 s	Firefly 2 s : Color 6
31	Color 7 Firefly 2 s	Firefly 2 s : Color 7
32	Color 8 Firefly 2 s	Firefly 2 s : Color 8
33	Color 9 Firefly 2 s	Firefly 2 s : Color 9
34	Color 10 Firefly 2 s	Firefly 2 s : Color 10
35	Color 11 Firefly 2 s	Firefly 2 s : Color 11
36	Color 12 Firefly 2 s	Firefly 2 s : Color 12
37	Gradation 1	Gradation 1
38	Gradation 2	Gradation 2
39	Gradation 3	Gradation 3
40	Gradation 4	Gradation 4
41	Gradation 5	Gradation 5
42	Gradation 6	Gradation 6

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OPERATION (continued)

4. Register and Address (continued)

Register table which needs a clock

About the following addresses, even if an internal clock or an external clock does not exist,
Read / Write is possible in the data to register. However, it cannot be given to operation finally needed.

Sub Address	R/W	Data Name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	W	POWERCNT	—	—	—	—	VF OFF	OSC EN	DCO SEL	DDS W
05h	W	LCDMAIN	—	—	—	LCDMAIN[4:0]				
06h	W	LCDSUB	—	—	—	LCDSUB[4:0]				
07h	W	PLCNT	—	—	HIEN	PLCNT[4:0]				
12h	W/R	IOMSK	—	—	—	IMSK1	IMSK 2	IMSK 3	IOMSK1	IMSK 2
14h	R	IOFACTOR	FACGD 1	ERR2EH	—	—	RAM ACT	FRM INT	CPU WRER	TSD
15h	R	IOSTATE	STAGD	—	—	ISTA1	ISTA 2	ISTA3	IOSTA1	IOST A2
16h	W/R	ICHAT	—	—	ICHAT1[1:0]		ICHAT2[1:0]		ICHAT3[1:0]	
17h	W/R	IOCHAT	—	—	—	—	IOCHAT1[1:0]		IOCHAT2[1:0]	
18h	W/R	IODET	—	—	—	—	IDET[1:0]		IODET[1:0]	

Established : 2006-08-29
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OPERATION (continued)

4. Register and Address (continued)

Register table which needs a clock (continued)

About the following addresses, even if an internal clock or an external clock does not exist,
Read / Write is possible in the data to register. However, it cannot be given to operation finally needed.

Sub Address	R/W	Data Name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	MTXON	—	—	—	—	—	—	—	MTXON
21h	R/W	MTXDATA	MTXDATA[7:0]							
22h	R/W	FFROM	—	—	—	—	—	—	ROM77[1:0]	
23h	R/W	ROMSEL	SELROM[7:0]							
24h	R/W	RAMCOPY	—	—	—	—	—	—	SEL RAM	COPY START
25h	R/W	SETFROM	SETFROM[7:0]							
26h	R/W	SETTO	SETTO[7:0]							
27h	R/W	REPON	—	—	—	—	—	—	—	REPON
28h	R/W	SETTIME	—	—	—	—	—	—	SETTIME[1:0]	
29h	R/W	RAMRST	—	—	—	—	—	—	RAM1	RAM2
2Ah	R/W	SCROLL	—	—	—	—	—	—	—	SCLON
2Bh	R/W	SCLTIME	—	—	—	—	—	—	SCLTIME[1:0]	
2Ch	R/W	RGBON	—	—	—	—	—	—	—	RGBON
2Dh	R/W	RGBDATA	—	—	RGBDATA[5:0]					
2Eh	R	ERROR	FACGD2	SCP	OVP	IFAC1	IFAC2	IFAC3	IOFAC 1	IOFAC2
30h	R/W	RAMNUM	—	—	—	—	—	—	—	RAMNUM

Established : 2006-08-29
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OPERATION (continued)

4. Register and Address (continued)

Register table which needs a clock (continued)

About the following addresses, when an internal clock or an external clock does not exist, data cannot be Read / Write in at register.

Sub Address	Data Name	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	A1	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
32h	A2	BLA2[3:0]				FRA2[1:0]		DLA2[1:0]	
33h	A3	BLA3[3:0]				FRA3[1:0]		DLA3[1:0]	
34h	A4	BLA4[3:0]				FRA4[1:0]		DLA4[1:0]	
35h	A5	BLA5[3:0]				FRA5[1:0]		DLA5[1:0]	
36h	A6	BLA6[3:0]				FRA6[1:0]		DLA6[1:0]	
37h	A7	BLA7[3:0]				FRA7[1:0]		DLA7[1:0]	
38h	B1	BLB1[3:0]				FRB1[1:0]		DLB1[1:0]	
39h	B2	BLB2[3:0]				FRB2[1:0]		DLB2[1:0]	
3Ah	B3	BLB3[3:0]				FRB3[1:0]		DLB3[1:0]	
3Bh	B4	BLB4[3:0]				FRB4[1:0]		DLB4[1:0]	
3Ch	B5	BLB5[3:0]				FRB5[1:0]		DLB5[1:0]	
3Dh	B6	BLB6[3:0]				FRB6[1:0]		DLB6[1:0]	
3Eh	B7	BLB7[3:0]				FRB7[1:0]		DLB7[1:0]	
3Fh	C1	BLC1[3:0]				FRC1[1:0]		DLC1[1:0]	
40h	C2	BLC2[3:0]				FRC2[1:0]		DLC2[1:0]	
41h	C3	BLC3[3:0]				FRC3[1:0]		DLC3[1:0]	
42h	C4	BLC4[3:0]				FRC4[1:0]		DLC4[1:0]	
43h	C5	BLC5[3:0]				FRC5[1:0]		DLC5[1:0]	
44h	C6	BLC6[3:0]				FRC6[1:0]		DLC6[1:0]	
45h	C7	BLC7[3:0]				FRC7[1:0]		DLC7[1:0]	
46h	D1	BLD1[3:0]				FRD1[1:0]		DLD1[1:0]	
47h	D2	BLD2[3:0]				FRD2[1:0]		DLD2[1:0]	
48h	D3	BLD3[3:0]				FRD3[1:0]		DLD3[1:0]	
49h	D4	BLD4[3:0]				FRD4[1:0]		DLD4[1:0]	
4Ah	D5	BLD5[3:0]				FRD5[1:0]		DLD5[1:0]	
4Bh	D6	BLD6[3:0]				FRD6[1:0]		DLD6[1:0]	
4Ch	D7	BLD7[3:0]				FRD7[1:0]		DLD7[1:0]	

OPERATION (continued)

4. Register and Address (continued)

Register table which needs a clock (continued)

About the following addresses, when an internal clock or an external clock does not exist, data cannot be Read / Write in at register.

Sub Address	Data Name	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
4Dh	E1	BLE1[3:0]				FRE1[1:0]		DLE1[1:0]	
4Eh	E2	BLE2[3:0]				FRE2[1:0]		DLE2[1:0]	
4Fh	E3	BLE3[3:0]				FRE3[1:0]		DLE3[1:0]	
50h	E4	BLE4[3:0]				FRE4[1:0]		DLE4[1:0]	
51h	E5	BLE5[3:0]				FRE5[1:0]		DLE5[1:0]	
52h	E6	BLE6[3:0]				FRE6[1:0]		DLE6[1:0]	
53h	E7	BLE7[3:0]				FRE7[1:0]		DLE7[1:0]	
54h	F1	BLF1[3:0]				FRF1[1:0]		DLF1[1:0]	
55h	F2	BLF2[3:0]				FRF2[1:0]		DLF2[1:0]	
56h	F3	BLF3[3:0]				FRF3[1:0]		DLF3[1:0]	
57h	F4	BLF4[3:0]				FRF4[1:0]		DLF4[1:0]	
58h	F5	BLF5[3:0]				FRF5[1:0]		DLF5[1:0]	
59h	F6	BLF6[3:0]				FRF6[1:0]		DLF6[1:0]	
5Ah	F7	BLF7[3:0]				FRF7[1:0]		DLF7[1:0]	
5Bh	G1	BLG1[3:0]				FRG1[1:0]		DLG1[1:0]	
5Ch	G2	BLG2[3:0]				FRG2[1:0]		DLG2[1:0]	
5Dh	G3	BLG3[3:0]				FRG3[1:0]		DLG3[1:0]	
5Eh	G4	BLG4[3:0]				FRG4[1:0]		DLG4[1:0]	
5Fh	G5	BLG5[3:0]				FRG5[1:0]		DLG5[1:0]	
60h	G6	BLG6[3:0]				FRG6[1:0]		DLG6[1:0]	
61h	G7	BLG7[3:0]				FRG7[1:0]		DLG7[1:0]	
62h	LEDR1	BLLEDR1[3:0]				FRLEDR1[1:0]		DLLEDR1[1:0]	
63h	LEDG1	BLLEDG1[3:0]				FRLEDG1[1:0]		DLLEDG1[1:0]	
64h	LEDB1	BLLEDB1[3:0]				FRLEDB1[1:0]		DLLEDB1[1:0]	

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Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
01h	Data Name	—	—	—	—	VFOFF	OSCEN	DCOSEL	DDSW
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D3 : VFOFF DC/DC converter automatic control selection bit
[0] : The automatic control of DC/DC converter is possible. (default)
[1] : The automatic control of DC/DC converter is impossible.

* The constant current terminal which acts as a monitor is chosen by BL1M, BL2M, BL3M, BL4M, BLS1M, and BLS2M bit of address 08h at VFOFF = Low. And if it is less than 0.4 V, DC/DC converter will be activated.

D2 : OSCEN The ON/OFF bit for internal oscillators
[0] : Internal oscillating circuit is OFF (default)
[1] : Internal oscillating circuit is ON

* The variation width of an internal oscillator is set to 0.96MHz - 1.44 MHz.
* The variation width of an internal clock is set to 694.4 ns – 1042 ns.

D1 : DCOSEL DC/DC converter output voltage setup
[0] : Output voltage set to 4.9 V (default)
[1] : Output voltage set to 5.3 V

D0 : DDSW The ON/OFF bit for DC/DC converter
[0] : DC/DC converter is OFF (default)
[1] : DC/DC converter is ON

* Set both bits of DDSW and OSCEN to [1] to operate DC/DC converter.
* Make sure to set both bits of OSCEN and DDSW to [1].
* During OSCEN = [1] , DDSW must be set to [1].

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
02h	Data Name	—	—	—	—	—	—	REG18	REG28
	Default	0	0	0	0	0	0	1	1
	mode	W	W	W	W	W	W	W	W

D1 : REG18 The ON/OFF control for LDO1(When LDOCNT terminal is Low)
[0] : LDO1 OFF
[1] : LDO1 ON (default)

D0 : REG28 The ON/OFF control for LDO2(When LDOCNT terminal is Low)
[0] : LDO2 OFF
[1] : LDO2 ON (default)

* When LDOCNT terminal is High, regardless of the state of REG18, LDO1 will be activated.
* When LDOCNT terminal is High, regardless of the state of REG28, LDO2 will be activated.
* Set LDOCNT to Low after setting REG28 to Low to put into OFF mode.

LDOCNT	REG18	REG28	Itotal typ(mA)	Note
Low (Initial condition)	OFF	OFF	<1	*
Low → High	N.C. (ON)	N.C. (ON)	18	—
High	N.C. (ON)	N.C. (ON)	18	*
High → Low	N.C. (OFF)	Low : OFF At OFF mode	<1 (OFF mode) or 8 (Standby mode)	*
	Low : OFF High : ON	High : ON At Standby mode		

Note) * : Explanation in each mode (Power supply starting sequence) of Page 26. Refer to the note.

Established : 2006-08-29
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OPERATION (continued)

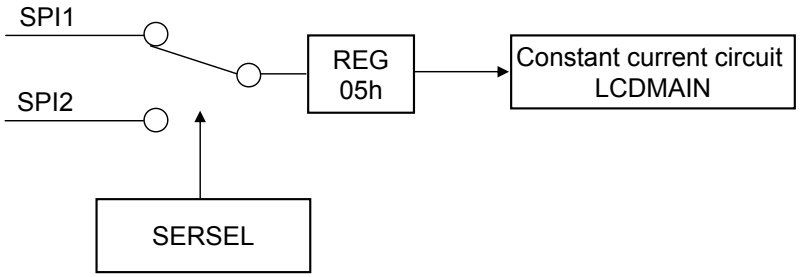
4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
03h	Data Name	—	—	—	—	—	—	—	SERSEL
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D0 : SERSEL The serial interface change which controls LCDMAIN luminosity control.
[0] : GPIO operation (default)
[1] : Serial control of address 05h (LCDMAIN) by SPI2

* GPI1 to GPI3 terminals serve as an input setup and an interruption mask compulsorily at SERSEL = High setup.



SERSEL	GPI1 terminal	GPI2 terminal	GPI3 terminal	Operation
0	GPI1 operation	GPI2 operation	GPI3 operation	GPIO operation
1	BLSCE operation	BLSCLK operation	BLSDAT operation	SPI2 operation

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
04h	Data Name	LSIVER[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	R	R	R	R	R	R	R	R

D7-0 : LSIVER[7:0] The register showing the version of LSI
[00000000] : ES1
[00000001] : ES2
:
:

OPERATION (continued)

4. Register and Address (continued)

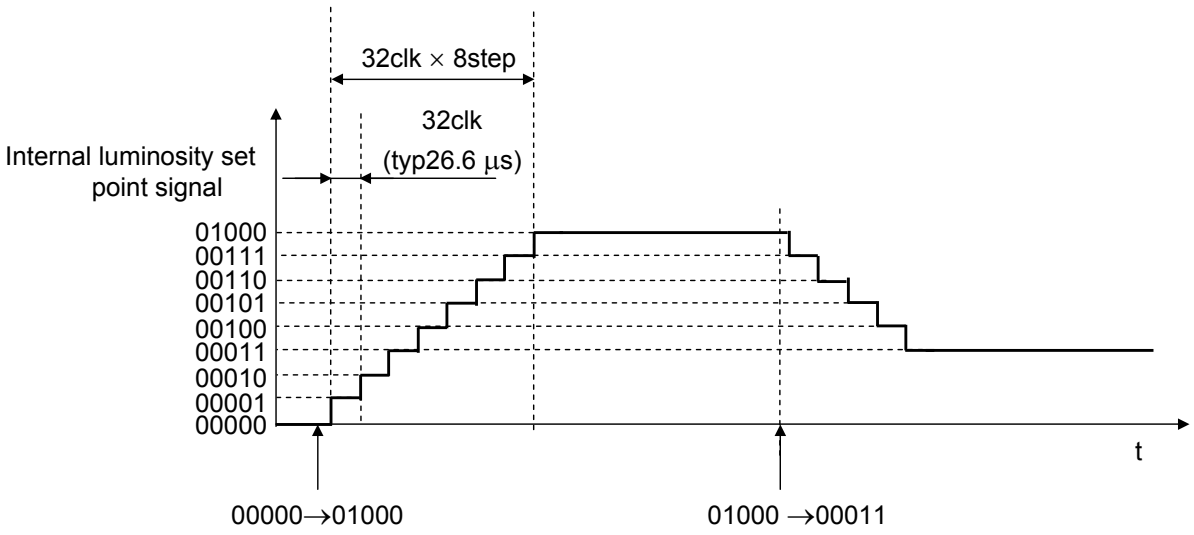
Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
05h	Data Name	—	—	—	LCDMAIN[4:0]				
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D4-0 : LCDMAIN[4:0] Output current setup of BL1-BL4 terminal
[00000] : 0 mA (default)
[00001] : 1 mA
[00010] : 2 mA
:
:
[11110] : 30 mA
[11111] : 31 mA

The waveform of main LCD backlights current of operation

* As for main LCD backlights part, output current changes stepwise for noise reduction.
* By the time it reaches current setup value, there will be delay of setup value × internal 32clk.
* When internal CLK stops during state transition, the state at that time is held.
* The following waveform is internal signal.



Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

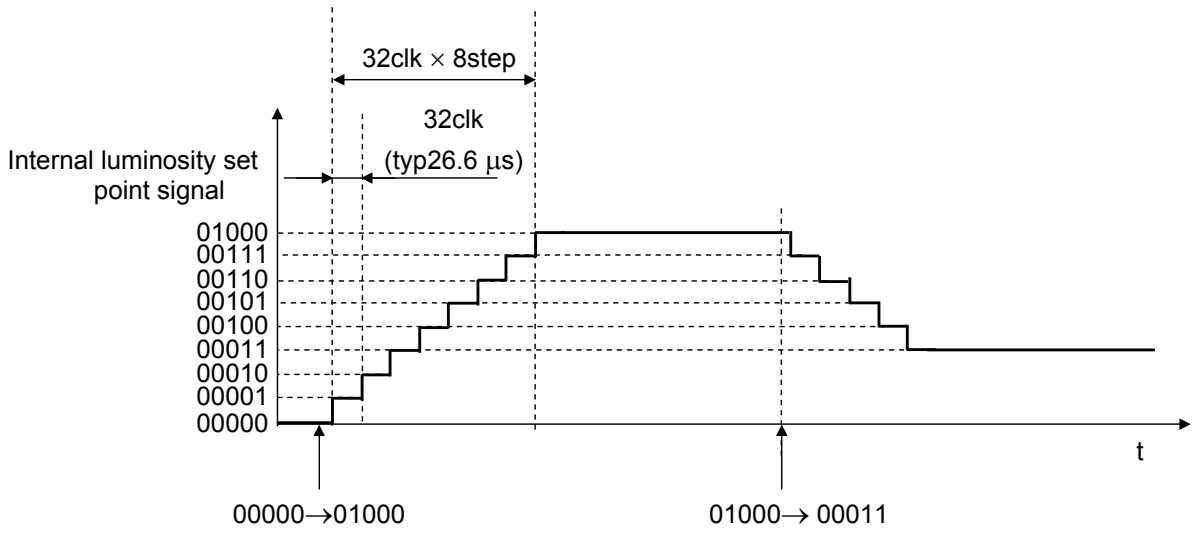
Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
06h	Data Name	—	—	—	LCDSUB[4:0]				
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D4-0 : LCDSUB[4:0] Output current setup of BLS1 - BLS2 terminal.
[00000] : 0 mA (default)
[00001] : 1 mA
[00010] : 2 mA
:
:
[11110] : 30 mA
[11111] : 31 mA

* D7, D6, and D5 must not be written.

The waveform of sub LCD backlights current of operation

* As for sub LCD backlights part, output current changes stepwise for noise reduction.
* By the time it reaches current setup value, there will be delay of setup value × internal 32clk.
* When internal CLK stops during state transition, the state at that time is held.
* The following waveform is internal signal.



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OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

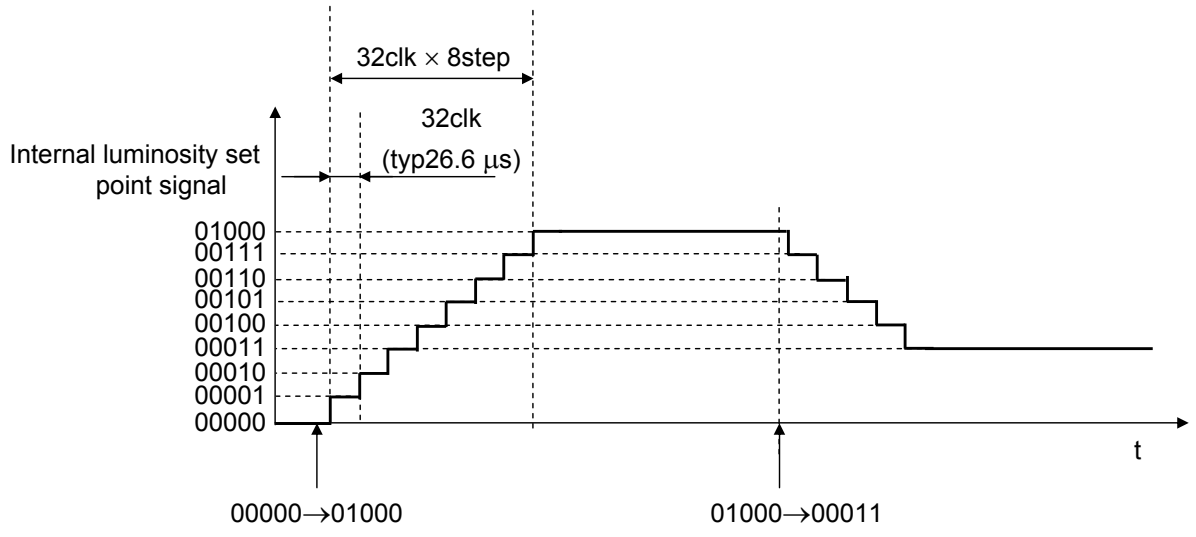
Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
07h	Data Name	—	—	HIEN	PLCNT[4:0]				
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D5 : HIEN Current large mode ON/OFF control of PL1 - PL2 terminal.
[0] : OFF (default)
[1] : ON (+30 mA)

D4-0 : PLCNT[4:0] Output current setup of PL1 - PL2 terminal.
[00000] : 0 mA (default)
[00001] : 1 mA
[00010] : 2 mA
:
:
[11110] : 30 mA
[11111] : 31 mA

The waveform of Photo flashes current of operation

* As for Photo flashes part, output current changes stepwise for noise reduction.
* By the time it reaches current setup value, there will be delay of setup value × internal 32clk.
* When internal CLK stops during state transition, the state at that time is held.
* The following waveform is internal signal.



Established : 2006-08-29
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OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
08h	Data Name	—	BL1M	BL2M	BL3M	BL4M	BLS1M	BLS2M	PWMCLK
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D6 : BL1M The automatic ON control monitor selection bit of DC/DC converter. (BL1 terminal)
[0] : Monitor of BL1 terminal is possible.(default)
[1] : Monitor of BL1 terminal is impossible.

D5 : BL2M The automatic ON control monitor selection bit of DC/DC converter. (BL2 terminal)
[0] : Monitor of BL2 terminal is possible.(default)
[1] : Monitor of BL2 terminal is impossible.

D4 : BL3M The automatic ON control monitor selection bit of DC/DC converter. (BL3 terminal)
[0] : Monitor of BL3 terminal is possible.(default)
[1] : Monitor of BL3 terminal is impossible.

D3 : BL4M The automatic ON control monitor selection bit of DC/DC converter. (BL4 terminal)
[0] : Monitor of BL4 terminal is possible.(default)
[1] : Monitor of BL4 terminal is impossible.

D2 : BLS1M The automatic ON control monitor selection bit of DC/DC converter. (BLS1 terminal)
[0] : Monitor of BLS1 terminal is possible.(default)
[1] : Monitor of BLS1 terminal is impossible.

D1 : BLS2M The automatic ON control monitor selection bit of DC/DC converter. (BLS2 terminal)
[0] : Monitor of BLS2 terminal is possible.(default)
[1] : Monitor of BLS2 terminal is impossible.

D0 : PWMCLK The PWM operation clock selection bit.
[0] : It operates by an internal clock. (default)
[1] : It operates by an EXTCLK clock.

* Interruption of address 14h is generated only in the OSCEN = High state at PWMCLK = Low.
* Interruption of address 14h is generated only in the state where a clock is input into EXTCLK terminal, at PWMCLK = High

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
09h	Data Name	VIBACT	VIBPL1	VIBPL2	VIBSUB1	VIBSUB2	VIBMTX	VIBRGB1	VIBRGB2
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D7 : VIBACT A putting-out-lights setup of LED by VIBCTL terminal.
[0] : The light is switched on at VIBCTL = Low.(default)
[1] : The light is switched on at VIBCTL = High.

D6 : VIBPL1 A putting-out-lights ON/OFF setup of PL1 terminal by VIBCTL terminal.
[0] : Putting-out-lights control OFF by VIBCTL terminal. (default)
[1] : Putting-out-lights control ON by VIBCTL terminal.

D5 : VIBPL2 A putting-out-lights ON/OFF setup of PL2 terminal by VIBCTL terminal.
[0] : Putting-out-lights control OFF by VIBCTL terminal. (default)
[1] : Putting-out-lights control ON by VIBCTL terminal.

D4 : VIBSUB1 A putting-out-lights ON/OFF setup of BLS1 terminal by VIBCTL terminal.
[0] : Putting-out-lights control OFF by VIBCTL terminal. (default)
[1] : Putting-out-lights control ON by VIBCTL terminal.

D3 : VIBSUB2 A putting-out-lights ON/OFF setup of BLS2 terminal by VIBCTL terminal.
[0] : Putting-out-lights control OFF by VIBCTL terminal. (default)
[1] : Putting-out-lights control ON by VIBCTL terminal.

D2 : VIBMTX A putting-out-lights ON/OFF setup of 7*7 dots matrix LED by VIBCTL terminal.
[0] : Putting-out-lights control OFF by VIBCTL terminal. (default)
[1] : Putting-out-lights control ON by VIBCTL terminal.

D1 : VIBRGB1 A putting-out-lights ON/OFF setup of R1, G1 and B1 terminal by VIBCTL terminal.
[0] : Putting-out-lights control OFF by VIBCTL terminal. (default)
[1] : Putting-out-lights control ON by VIBCTL terminal.

D0 : VIBRGB2 A putting-out-lights ON/OFF setup of R2, G2 and B2 terminal by VIBCTL terminal.
[0] : Putting-out-lights control OFF by VIBCTL terminal. (default)
[1] : Putting-out-lights control ON by VIBCTL terminal.

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Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
0Ah	Data Name	LEDACT	DISPL1	DISPL2	DISSUB1	DISSUB2	DISMTX	DISRGB1	DISRGB2
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D7 : LEDACT A putting-out-lights setup of LED by LEDCTL terminal.
[0] : The light is switched on at LEDCTL = Low(default)
[1] : The light is switched on at LEDCTL = High

D6 : DISPL1 A putting-out-lights ON/OFF setup of PL1 terminal by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

D5 : DISPL2 A putting-out-lights ON/OFF setup of PL2 terminal by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

D4 : DISSUB1 A putting-out-lights ON/OFF setup of BLS1 terminal by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

D3 : DISSUB2 A putting-out-lights ON/OFF setup of BLS2 terminal by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

D2 : DISMTX A putting-out-lights ON/OFF setup of 7*7 dots matrix LED by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

D1 : DISRGB1 A putting-out-lights ON/OFF setup of R1, G1 and B1 terminal by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

D0 : DISRGB2 A putting-out-lights ON/OFF setup of R2, G2 and B2 terminal by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Ex.)In the case of PL1 terminal

VIBCTL	VIBACT	VIBPL1	PL1 control signal	Current value
0	0	0	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
0	1	0	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
1	0	0	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
1	1	0	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
0	0	1	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
0	1	1	OFF	0mA
1	0	1	OFF	0mA
1	1	1	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]

LEDCTL	LEDACT	DISPL1	PL1 control signal	Current value
0	0	0	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
0	1	0	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
1	0	0	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
1	1	0	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
0	0	1	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]
0	1	1	OFF	0mA
1	0	1	OFF	0mA
1	1	1	ON	OFF is PLCNT[4:0] = [00000] by PLCNT[4:0]

* When control signal is input from both VIBCTL terminal and LEDCTL terminal, the OFF state of each PL1 terminal control signal is processed in OR logic.
* Same control for VIBPL2 and PL2 terminal
* Same control for VIBSUB1 and BLS1 terminal
* Same control for VIBSUB2 and BLS2 terminal
* Same control for VIBMTX and X0 - X6 terminal
* Same control for VIBRGB1 and R1, G1 and B1 terminal
* Same control for VIBRGB2 and R2, G2 and B2 terminal
* Same control for DISPL2 and PL2 terminal
* Same control for DISSUB1 and BLS1 terminal
* Same control for DISSUB2 and BLS2 terminal
* Same control for DISMTX and X0 - X6 terminal
* Same control for DISRGB1 and R1, G1 and B1 terminal
* Same control for DISRGB2 and R2, G2 and B2 terminal

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
10h	Data Name	—	—	—	—	—	—	—	GPIOCLK
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : GPIOCLK Change of the clock for GPIO control.
[0] : It operates by an internal clock. (default)
[1] : It operates by an EXTCLK clock.

* At GPIOCLK = Low, register (IOFACTOR, IOSTATE, ICHAT, IOCHAT), interruption of address 2Eh, and INT terminal operate in the state of OSCEN = High.
* At GPIOCLK = High, register (IOFACTOR, IOSTATE, ICHAT, IOCHAT), interruption of address 2Eh, and INT terminal operate, where clock is input into EXTCLK terminal.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
11h	Data Name	—	—	—	—	—	—	IOSEL1	IOSEL2
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1 : IOSEL1 An input/output setup of GPIO1 terminal
[0] : Input (default)
[1] : Output

D0 : IOSEL2 An input/output setup of GPIO2 terminal
[0] : Input (default)
[1] : Output

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
12h	Data Name	—	—	—	IMSK1	IMSK2	IMSK3	IOMSK1	IOMSK2
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D4 : IMSK1 GPI1 terminal change-of-state detection mask setup.
[0] : Interruption output mask (default)
[1] : Interruption output enable
* The mask of the interruption detection output ISTA1 by change-of-state detection of GPI1 terminal is carried out.

D3 : IMSK2 GPI2 terminal change-of-state detection mask setup.
[0] : Interruption output mask (default)
[1] : Interruption output enable
* The mask of the interruption detection output ISTA2 by change-of-state detection of GPI2 terminal is carried out.

D2 : IMSK3 GPI3 terminal change-of-state detection mask setup.
[0] : Interruption output mask (default)
[1] : Interruption output enable
* The mask of the interruption detection output ISTA3 by change-of-state detection of GPI3 terminal is carried out.

D1 : IOMSK1 GPIO1 terminal change-of-state detection mask setup.
[0] : Interruption output mask (default)
[1] : Interruption output enable
* The mask of the interruption detection output IOSTA1 by change-of-state detection of GPIO1 terminal is carried out.

D0 : IOMSK2 GPIO2 terminal change-of-state detection mask setup.
[0] : Interruption output mask (default)
[1] : Interruption output enable
* The mask of the interruption detection output IOSTA2 by change-of-state detection of GPIO2 terminal is carried out.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
13h	Data Name	—	—	—	—	OOUT1	OOUT2	IOOUT1	IOOUT2
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D3 : OOUT1 An output logic setup of GPO1 terminal
[0] : Output is Low (default)
[1] : Output is High

D2 : OOUT2 An output logic setup of GPO2 terminal
[0] : Output is Low (default)
[1] : Output is High

D1 : IOOUT1 An output logic setup of GPIO1 terminal
[0] : Output is Low (default)
[1] : Output is High
* Effective only at IOSEL1 = High (output mode).

D0 : IOOUT2 An output logic setup of GPIO2 terminal
[0] : Output is Low (default)
[1] : Output is High
* Effective only at IOSEL2 = High (output mode).

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OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
14h	Data Name	FACGD1	ERR2EH	—	—	RAMACT	FRMINT	CPUWRER	TSD
	Default	0	0	0	0	0	0	0	0
	mode	R	R	R	R	R	R	R	R

D7 : FACGD1
[0] : Normal operation (default)
[1] : No Read clearance

D6 : ERR2EH Unusual detection of address 2Eh
0 : It is NOT unusual detection to address 2Eh. (default)
1 : It is unusual detection to address 2Eh. Read to address 2Eh.

D3 : RAMACT Internal RAM access judgment
0 : RAM is NOT accessed. (default)
1 : RAM is accessed.

D2 : FRMINT An one-frame display end judging scroll on display.
0 : Under a frame display (default)
1 : Frame display end

D1 : CPUWRER CPU access error judgment
0 : CPU access error does NOT occur. (default)
1 : CPU access error occurs.

D0 : TSD Unusual detection of TSD error.
0 : TSD unusual detection does NOT occur. (default)
1 : TSD unusual detection occurs.

* The WRITE contents from CPU are not reflected in this IC at CPUWRER = High. Write from CPU again.
* The interval of FACGD1 = High is maximum 1.93 μs (at the internal clock operation) from the renewal time of data.
* At FACGD1 = Low, if address 14h data is read, data of D0 - D6 are cleared.
* RAM access from CPU cannot be performed at RAMACT = High .
* When each address 14h register is set to High, the pulse in a cycle of 4 ms is output from INT.
* The pulse output from INT continues an output until address 14h is read.
* The pulse output from INT continues an output until address 2Eh is also read in ERR2EH = High .
* The states for RAMACT = High are shown below.
  1. While copying to RAM from ROM.
  2. While clearing RAM

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
15h	Data Name	STAGD	—	—	ISTA1	ISTA2	ISTA3	IOSTA1	IOSTA2
	Default	0	0	0	0	0	0	0	0
	mode	R	R	R	R	R	R	R	R

D7 : STAGD
[0] : Normal operation (default)
[1] : Data interruption disregard

D4 : ISTA1 The state after chattering removal of GPI1 terminal.
[0] : The terminal state after chattering is 0. (default)
[1] : The terminal state after chattering is 1.

D3 : ISTA2 The state after chattering removal of GPI2 terminal.
[0] : The terminal state after chattering is 0. (default)
[1] : The terminal state after chattering is 1.

D2 : ISTA3 The state after chattering removal of GPI3 terminal.
[0] : The terminal state after chattering is 0. (default)
[1] : The terminal state after chattering is 1.

D1 : IOSTA1 The state after chattering removal of GPIO1 terminal.
[0] : The terminal state after chattering is 0. (default)
[1] : The terminal state after chattering is 1.

D0 : IOSTA2 The state after chattering removal of GPIO2 terminal.
[0] : The terminal state after chattering is 0. (default)
[1] : The terminal state after chattering is 1.

* The interval of STAGD = High is maximum 1.93 μs (at internal clock operation) from the time at which data was updated.
* At IOSEL1 = High or IOSEL2 = High, the data of IOOUT1 or IOOUT2 is stored.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
16h	Data Name	—	—	ICHAT1[1:0]		ICHAT2[1:0]		ICHAT3[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D5-4 : ICHAT1[1:0] An interruption chattering processing time setup of GPI1 terminal.
[00] : 4800CLK × 0 No chattering processing time (default)
[01] : 4800CLK × (4-1) Chattering processing time is 10.58 ms to 18.47 ms
[10] : 4800CLK × (9-1) Chattering processing time is 28.23 ms to 41.54 ms
[11] : 4800CLK × (16-1) Chattering processing time is 52.94 ms to 73.85 ms

D3-2 : ICHAT2[1:0] An interruption chattering processing time setup of GPI2 terminal.
[00] : 4800CLK × 0 No chattering processing time (default)
[01] : 4800CLK × (4-1) Chattering processing time is 10.58 ms to 18.47 ms
[10] : 4800CLK × (9-1) Chattering processing time is 28.23 ms to 41.54 ms
[11] : 4800CLK × (16-1) Chattering processing time is 52.94 ms to 73.85 ms

D1-0 : ICHAT3[1:0] An interruption chattering processing time setup of GPI3 terminal.
[00] : 4800CLK × 0 No chattering processing time (default)
[01] : 4800CLK × (4-1) Chattering processing time is 10.58 ms to 18.47 ms
[10] : 4800CLK × (9-1) Chattering processing time is 28.23 ms to 41.54 ms
[11] : 4800CLK × (16-1) Chattering processing time is 52.94 ms to 73.85 ms

*The times shown above are for when the internal clock operates.

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
17h	Data Name	—	—	—	—	IOCHAT1[1:0]		IOCHAT2[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D3-2 : IOCHAT1[1:0] An interruption chattering processing time setup of GPIO1 terminal.
[00] : 4800CLK × 0 No chattering processing time (default)
[01] : 4800CLK × (4-1) Chattering processing time is 10.58 ms to 18.47 ms
[10] : 4800CLK × (9-1) Chattering processing time is 28.23 ms to 41.54 ms
[11] : 4800CLK × (16-1) Chattering processing time is 52.94 ms to 73.85 ms

D1-0 : IOCHAT2[1:0] An interruption chattering processing time setup of GPIO2 terminal.
[00] : 4800CLK × 0 No chattering processing time (default)
[01] : 4800CLK × (4-1) Chattering processing time is 10.58 ms to 18.47 ms
[10] : 4800CLK × (9-1) Chattering processing time is 28.23 ms to 41.54 ms
[11] : 4800CLK × (16-1) Chattering processing time is 52.94 ms to 73.85 ms

*The times shown above are for when the internal clock operates.

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
18h	Data Name	—	—	—	—	IDET[1:0]		IODET[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D3-2 : IDET[1:0] The interruption detection method setup of GPI1, GPI2 and GPI3 terminal.
[00] : Change-of-state detection is impossible. (default)
[01] : Change of the terminal state from Low to High is detected.
[10] : Change of the terminal state from High to Low is detected.
[11] : Both the edge of change of a terminal state is detected. (Low → High and High → Low)

D1-0 : IODET[1:0] The interruption detection method setup of GPIO1 and GPIO2 terminal.
[00] : Change-of-state detection is impossible. (default)
[01] : Change of the terminal state from Low to High is detected.
[10] : Change of the terminal state from High to Low is detected.
[11] : Both the edge of change of a terminal state is detected. (Low → High and High → Low)

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
19h	Data Name	—	—	—	R2ON	G2ON	B2ON	IOPLUD1	IOPLUD2
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D4 : R2ON ON/OFF control of R2 terminal
[0] : OFF (default)
[1] : ON

D3 : G2ON ON/OFF control of G2 terminal
[0] : OFF (default)
[1] : ON

D2 : B2ON ON/OFF control of B2 terminal
[0] : OFF (default)
[1] : ON

D1 : IOPLUD1 A terminal processing setup of GPIO1 terminal
[0] : PULL-UP processing (default)
[1] : NOT PULL-UP processing

D0 : IOPLUD2 A terminal processing setup of GPIO2 terminal
[0] : PULL-UP processing (default)
[1] : NOT PULL-UP processing

* IOPLUD1 and IOPLUD2 are effective only when IOSEL1 and IOSEL2 are input modes.
* In the case of the state of IOPLUD1 = Low and IOVSEL1 = High, the power of 2.85 V cannot be applied to GPIO1.
* In the case of the state of IOPLUD2 = Low and IOVSEL2 = High, the power of 2.85 V cannot be applied to GPIO2.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
1Ah	Data Name	INTVSEL	—	—	—	OVSEL1	OVSEL2	IOVSEL1	IOVSEL2
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7 : INTVSEL A terminal voltage setup of INT terminal
[0] : 1.85 V (default)
[1] : 2.85 V

D3 : OVSEL1 A terminal voltage setup of GPO1 terminal
[0] : 2.85 V (default)
[1] : 1.85 V

D2 : OVSEL2 A terminal voltage setup of GPO2 terminal
[0] : 2.85 V (default)
[1] : 1.85 V

D1 : IOVSEL1 A terminal voltage setup of GPIO1 terminal
[0] : 2.85 V (default)
[1] : 1.85 V

D0 : IOVSEL2 A terminal voltage setup of GPIO2 terminal
[0] : 2.85 V (default)
[1] : 1.85 V

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
20h	Data Name	—	—	—	—	—	—	—	MTXON
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : MTXON An ON/OFF setup of matrix LED
[0] : OFF (default)
[1] : ON

* During MTXON = High, subsequent ROM, RAM, and the control contents to a register are sequentially processed and lit up.
* When address 08h PWMCLK is Low, set MTXON to High 5 ms after setting address 01h OSCEN to High.
* When address 08h PWMCLK is High, set MTXON to High 5 ms after inputting clocks to EXTCLK terminal.
* Set MTXON to High, and then set up other addresses to display the matrix part.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
21h	Data Name	MTXDATA[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : MTXDATA[7:0] An address setup of ROM/RAM of the data to read
[00000000] - [10010101] : ROM (Only luminosity)
7*7 pattern No.0 (default) to No.149
[10010110] - [11010000] : ROM (Luminosity + Cycle + Delay)
7*7 pattern No. 150 to No.208
[11010001] - [11010010] : RAM (Luminosity + Cycle + Delay)
7*7 pattern RAM No.1, 2

* The pattern No.0 of ROM is all 0 data of matrix LED.
* Accessing to 21h is disabled while copying from ROM to RAM (COPYSTART = High of 24h).

OPERATION (continued)

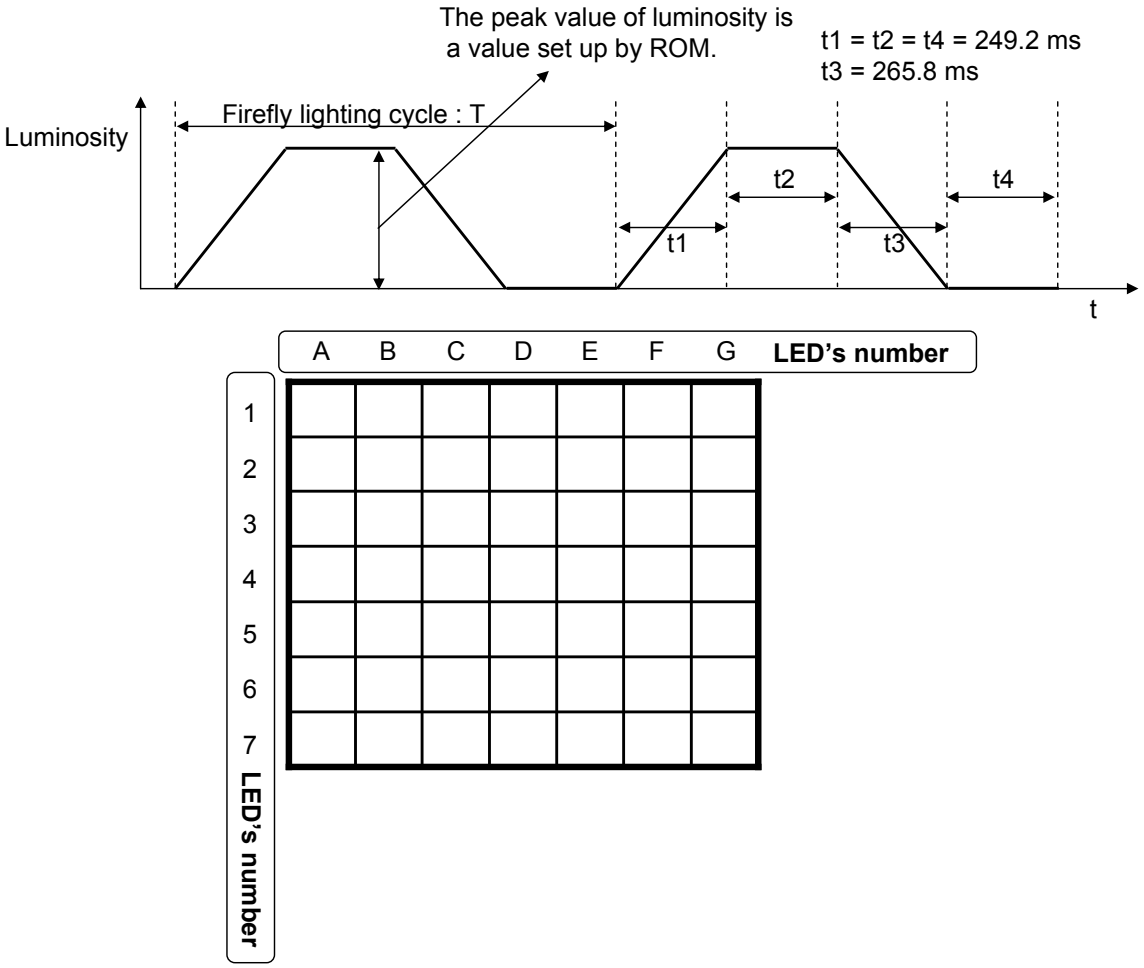
4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
22h	Data Name	—	—	—	—	—	—	ROM77[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : ROM77[1:0] Lighting control of the 7x7 (LED No.A1-G7) fixed pattern of ROM
[00] : ROM data is displayed.
[01] : ROM data is displayed by firefly lighting in 1 s.
[10] : ROM data is displayed by firefly lighting in 2 s.
[11] : ROM data is displayed by firefly lighting in 3 s.

* During display of repetition (REPON = High), ROM77 must not be changed.



Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
23h	Data Name	SELROM[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SELROM[7:0] An address setup of ROM copied to RAM.
[00000000] - [10010101] : ROM (Only luminosity) 7*7 pattern No.0 (default) to No.149
[10010110] - [11010000] : ROM (Luminosity + Cycle + Delay) 7*7 pattern No.150 to No.208

* Accessing to 23h is disabled while copying from ROM to RAM (COPYSTART = High of 24h).

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
24h	Data Name	—	—	—	—	—	—	SELRAM	COPYSTART
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1 : SELRAM A RAM number setup of a copy place.
0 : RAM No.1
1 : RAM No.2

D0 : COPYSTART Copy start ON/OFF control to RAM from ROM
[0] : OFF
[1] : The copy set up by SELROM and SELRAM is started. (It returns to 0 by internal 51 CLK.)

* Address 24h is only for copying data to RAM and never start LED display.
(However, if this RAM is copied when LED display is showing, LED display is updated.)
* Writing in address 21h-MTXDATA, 2Ah-SCLON, and 27h-REPON is disabled while copying.
(RAMACT flag is raised.)
* Accessing to SELRAM is disabled while copying from ROM to RAM (COPYSTART = High of 24h)
* Don't write address 29h (RAM-clear) while copying.
(The waiting time for 1 ms or more is required after COPYSTART.)

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
25h	Data Name	SETFROM[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SETFROM[7:0] An address setup of the ROM frame data at the repetition display start.
[00000000] - [10010101] : ROM (Only luminosity) 7*7 pattern No.0 (default) to No.149
[10010110] - [11010000] : ROM (Luminosity + Cycle + Delay) 7*7 pattern No.150 to No.208

* During display of repetition (REPON = High), Don't change the setting of SETFROM.

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
26h	Data Name	SETTO[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SETTO[7:0] An address setup of the ROM frame data at the repetition display end.
[00000000] - [10010101] : ROM (Only luminosity) 7*7 pattern No.0 (default) to No.149
[10010110] - [11010000] : ROM (Luminosity + Cycle + Delay) 7*7 pattern No.150 to No.208

* During display of repetition (REPON = High), don't change the setting of SETTO.

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
27h	Data Name	—	—	—	—	—	—	—	REPON
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : REPON Repetition display ON/OFF control
0 : Repetition display OFF (default)
1 : Repetition display ON

* During display of repetition, display of set-up ROM is continued.
* A repetition display is started in the state of MTXON = High and REPON = High.
* Accessing to 27h is disabled while copying from ROM to RAM (COPYSTART = High of 24h).
* When the setting of SCLON is changed from Low to High while REPON = High, REPON becomes Low and it shifts to scroll function.
* During display of repetition (REPON = High), don't change the setting of SETFROM and SETTO.

Established : 2006-08-29
Revised : 2013-04-01

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
28h	Data Name	—	—	—	—	—	—	SETTIME[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : SETTIME[1:0] A frame display time setup of repetition display
[00] : 1 s (default)
[01] : 2 s
[10] : 3 s
[11] : 4 s

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
29h	Data Name	—	—	—	—	—	—	RAM1	RAM2
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1 : RAM1 The data in 7*7 RAM1 is cleared.
0 : Overwrite is possible. (default)
1 : The data in 7*7 RAM1 is cleared. (It returns to 0 by internal 2 CLK.)

D0 : RAM2 The data in 7*7 RAM2 is cleared.
0 : Overwrite is possible. (default)
1 : The data in 7*7 RAM2 is cleared. (It returns to 0 by internal 2 CLK.)

* Don't set the RAM-clear operation for RAM1 or RAM2 during display of repetition (SCLON = High).
* Don't set the RAM-clear operation (29h) during the COPY operation (24h).
(The waiting time for 1 ms or more is required after COPYSTART.)

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Ah	Data Name	—	—	—	—	—	—	—	SCLON
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : SCLON ON/OFF setup of scroll display
0 : OFF (default)
1 : ON

* A scroll display displays the data which exists in the RAM No.1-2 of 7*7 in order of A-G column. The display travel time of a column is the preset value of SCLTIME.
* During display of scroll, data can be written to RAM without specifying RAM number.
(Writing is performed to empty RAM.)
* A scroll display is started in the state of MTXON = High and SCLON.
* Accessing to 2Ah is disabled while copying from ROM to RAM (COPYSTART = High of 24h).
* When the setting of REPON is changed from Low to High while SCLON = High, SCLON becomes Low and it shifts to repetition display function.
* During display of scroll (SCLON = High), don’t change the setting of RAM1 and RAM2.

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OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Bh	Data Name	—	—	—	—	—	—	SCLTIME[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : SCLTIME[1:0] A frame display time setup of scroll display
[00] : 0.1 s (default)
[01] : 0.2 s
[10] : 0.4 s
[11] : 0.8 s

* The display travel time of the column is the preset value of SCLTIME.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Ch	Data Name	—	—	—	—	—	—	—	RGBON
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : RGBON ON/OFF setup of RGB lighting
0 : OFF (default)
1 : ON

* When address 08h PWMCLK is Low, set RGBON to High 5 ms after setting address 01h OSCEN to High.
* When address 08h PWMCLK is High, set RGBON to High 5 ms after inputting clocks to EXTCLK terminal.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Dh	Data Name	—	—	RGBDATA					
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : RGBDATA[5:0] An address setup of ROM and register which read RGB data
[000000] : Register is displayed.
[000001] - [101010] : ROM (RGB pattern, Luminosity + Cycle + Delay) pattern No.1 to No.42

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Eh	Data Name	FACGD2	SCP	OVP	IFAC1	IFAC2	IFAC3	IOFAC1	IOFAC2
	Default	0	0	0	0	0	0	0	0
	mode	R	R	R	R	R	R	R	R

D7 : FACGD
[0] : Normal operation (default)
[1] : No read clearance

D6 : SCP An interruption factor register when short comparator operates while the DC/DC converter operated.
[0] : An interrupt does NOT occur. (default)
[1] : An interrupt occurs.

D5 : OVP An interruption factor register when over-voltage detection comparator operates while the DC/DC converter operated.
[0] : An interrupt does NOT occur. (default)
[1] : An interrupt occurs.

D4 : IFAC1 The interruption factor register of GPI1 terminal
[0] : An interrupt does NOT occur. (default)
[1] : An interrupt occurs.

D3 : IFAC2 The interruption factor register of GPI2 terminal
[0] : An interrupt does NOT occur. (default)
[1] : An interrupt occurs.

D2 : IFAC3 The interruption factor register of GPI3 terminal
[0] : An interrupt does NOT occur. (default)
[1] : An interrupt occurs.

D1 : IOFAC1 The interruption factor register of GPIO1 terminal
[0] : An interrupt does NOT occur. (default)
[1] : An interrupt occurs.

D0 : IOFAC2 The interruption factor register of GPIO2 terminal
[0] : An interrupt does NOT occur. (default)
[1] : An interrupt occurs.

* The interval of FACGD2 = High is maximum 1.93 μs (at internal clock operation) from the renewal time of data.
* At FACGD2 = Low, if the data of address 2Eh is read, data of D0 - D6 are cleared.
* Only at IOSEL1 = Low or IOSEL2 = Low, an interruption factor is generated.
* In the case of IOSEL1 = High or IOSEL2 = High, status and register in chattering removal circuit is reset.
* When each address 2Eh register is set to High, the pulse in a cycle of 4 ms is output from INT.
* The pulse output from INT continues an output until address 14h is read.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
30h	Data Name	—	—	—	—	—	—	—	RAMNUM
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : RAMNUM[1:0] A RAM number setup at the CPU access (READ and WRITE).
0 : RAM No.1
1 : RAM No.2

* Accessing to 30h is disabled during display of scroll (2Ah SCLON = High).

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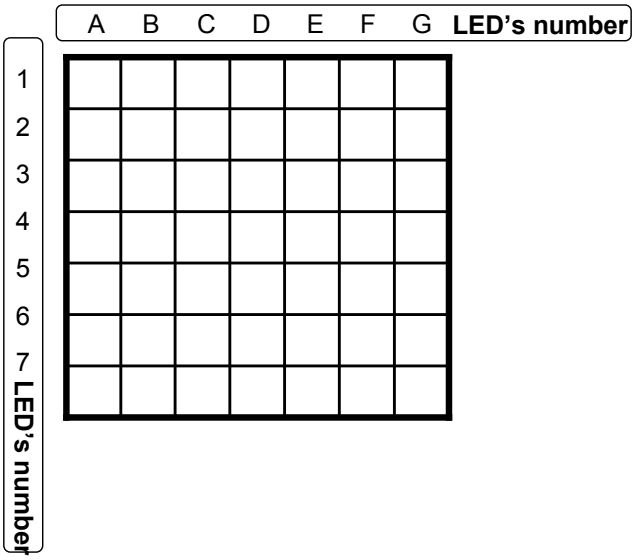
OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	Data Name	BLA1[1:0]				FRA1[1:0]		DLA1[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-4 : BLA1[1:0] Luminosity setup of LED No.A1
[0000] : 0 mA (default)
[0001] : 1 mA
[0010] : 2 mA
[0011] : 3 mA
[0100] : 4 mA
[0101] : 5 mA
[0110] : 8 mA
[0111] : 11 mA
[1000] : 15 mA
[1001] : 17 mA
[1010] : 19 mA
[1011] : 21 mA
[1100] : 24 mA
[1101] : 26 mA
[1110] : 28 mA
[1111] : 30 mA



D3-2 : FRA1[1:0] Firefly operation and cycle setup of the LED No.A1
[00] : Lighting mode (default)
[01] : Firefly lighting cycle 1 s
[10] : Firefly lighting cycle 2 s
[11] : Firefly lighting cycle 3 s

D1-0 : DLA1[1:0] Firefly operation delay setup of the LED No.A1
[00] : No delay (default)
[01] : Delay 25 %
[10] : Delay 50 %
[11] : Delay 75 %

* The operation is the same as above for the addresses to 61h corresponding to each LED number.
* The waiting time for 2 or more internal clocks (2 μs or more) is required after the data from address 31h to 61h is written in. Please input other serial commands after that.

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OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
62h	Data Name	BLLEDR1[1:0]				FRLEDR1[1:0]		DLLEDR1[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-4 : BLLEDR1[1:0] Luminosity setup of R1 terminal
[0000] : 0 mA (default)
[0001] : 1 mA
[0010] : 2 mA
:
:
[1110] : 14 mA
[1111] : 15 mA

D3-2 : FRLEDR1[1:0] Firefly operation and cycle setup of R1 terminal
[00] : Lighting mode (default)
[01] : Firefly lighting cycle 1 s
[10] : Firefly lighting cycle 2 s
[11] : Firefly lighting cycle 3 s

D1-0 : DLLEDR1[1:0] Firefly operation delay setup of R1 terminal
[00] : No delay (default)
[01] : Delay 25 %
[10] : Delay 50 %
[11] : Delay 75 %

* The operation is the same as above for the addresses to 67h corresponding to G1 and B1 terminal.
* The waiting time for 2 or more internal clocks (2 μs or more) is required after the data from address 62h to 64h is written in. Please input other serial commands after that.

OPERATION (continued)

4. Register and Address (continued)

Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
6Bh	Data Name	—	—	—	—	—	—	—	PROT1
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
6Dh	Data Name	—	—	—	PROT2	—	—	—	—
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
6Fh	Data Name	PROT3	—	—	—	—	—	—	—
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

6BhD0(PROT1), 6DhD4(PROT2), 6FhD7(PROT3)

* Please don't access to address 6Bh to 6Fh.
* Addresses to 77h are for test.
* When all the three above bits are set to High, it is allowed to write in Addresses [70h - 77h].
  (For test. Do not setup these addresses.)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
70h	Data Name	TEST1[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : TEST1[7:0] The register for test

* Addresses to 77h are for test.
* Please don't access to address 70h to 77h.

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OPERATION (continued)

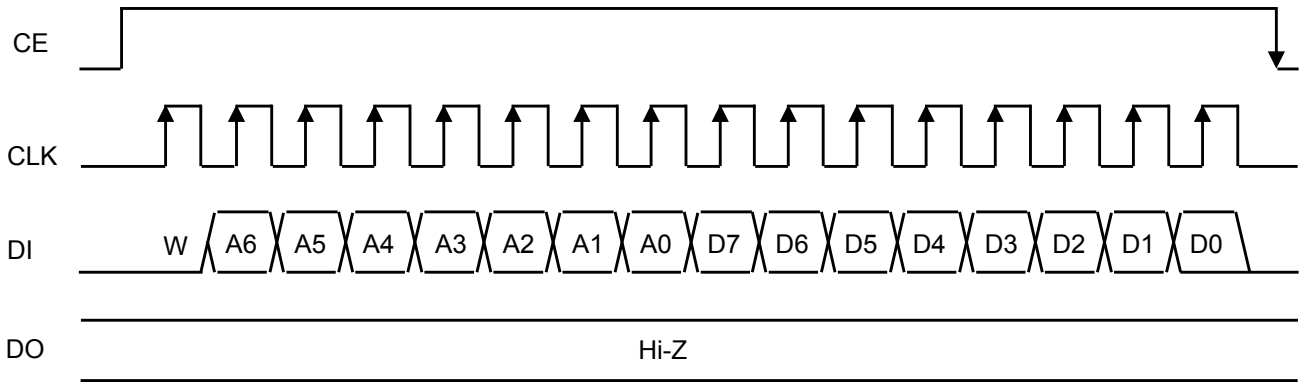
5. Serial interface format

SPI1 format

- The interface with microcomputer consists of 16 bit-serial register (8-bit of command, 8-bit of address), and address decoder and transmitting register (8-bit).
- Serial interface consists of four terminals of serial clock terminal (CLK), serial-data input terminal (DI), serial-data output terminal (DO), and chip enable input terminal (CE).

(1) Reception operation
- Data is taken into internal shift register by the rising edge of CLK. (A maximum of 13 MHz of frequency of CLK can be used)
- In High interval of CE, reception of data becomes ENABLE. (active : High)
- Data is transmitted at MSB first in order of a control register address (8-bit) and control command (8-bit).

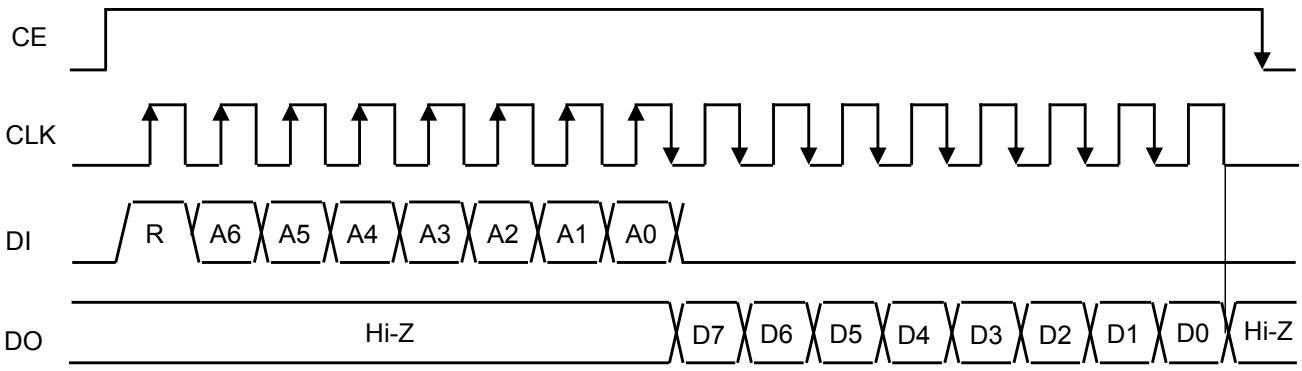
Timing of reception



(2) Transmission operation
- Data is taken into internal shift register by the rising edge of CLK. (A maximum of 6 MHz of frequency of CLK can be used)

* It is not possible to read RAM data.
- In High interval of CE, reception of data becomes ENABLE. (active : High)
- Data is transmitted at MSB first in order of a control register address (8-bit) and control command (max 8-bit).

Timing of transmission



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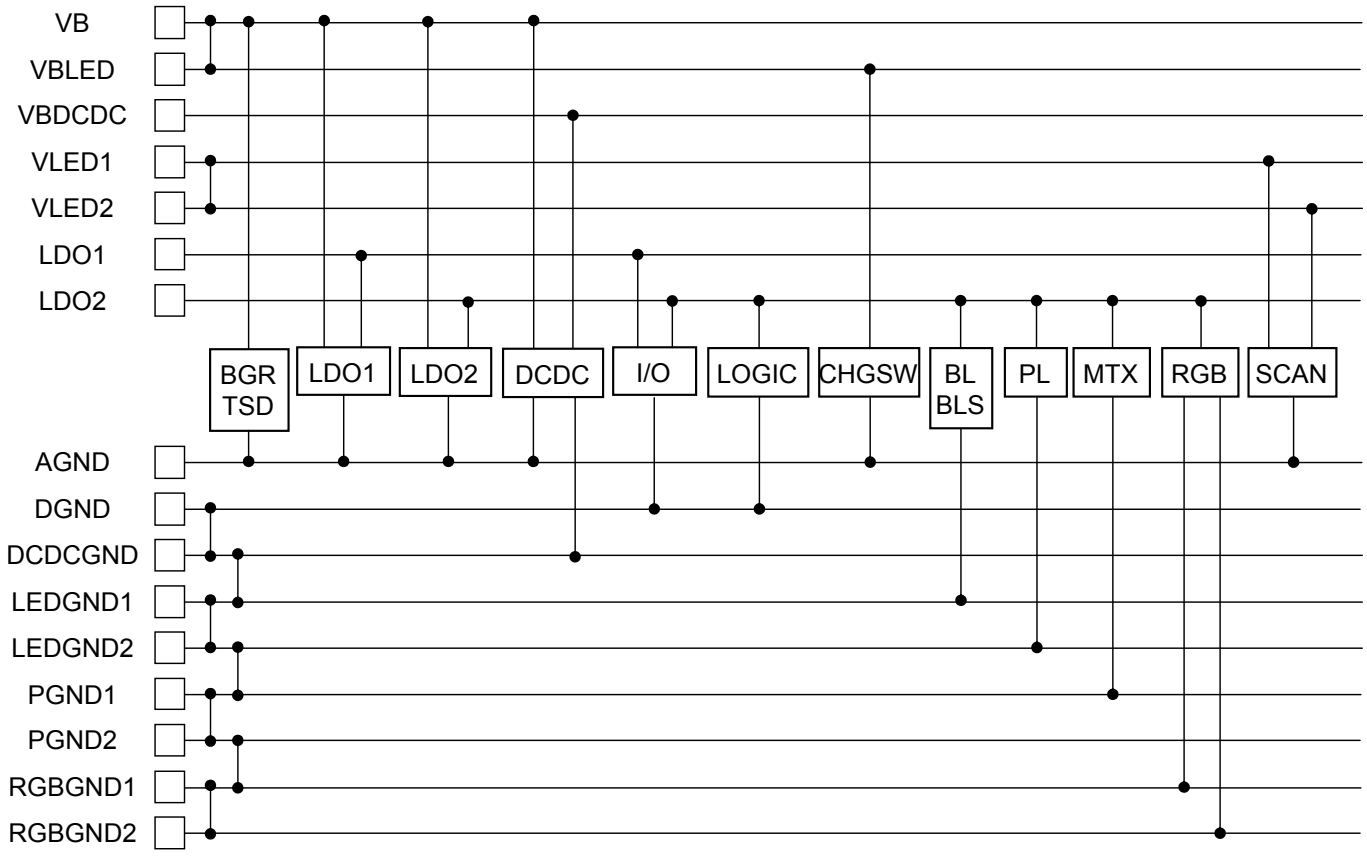
OPERATION (continued)

6. Signal distribution diagram

Power supply distribution diagram



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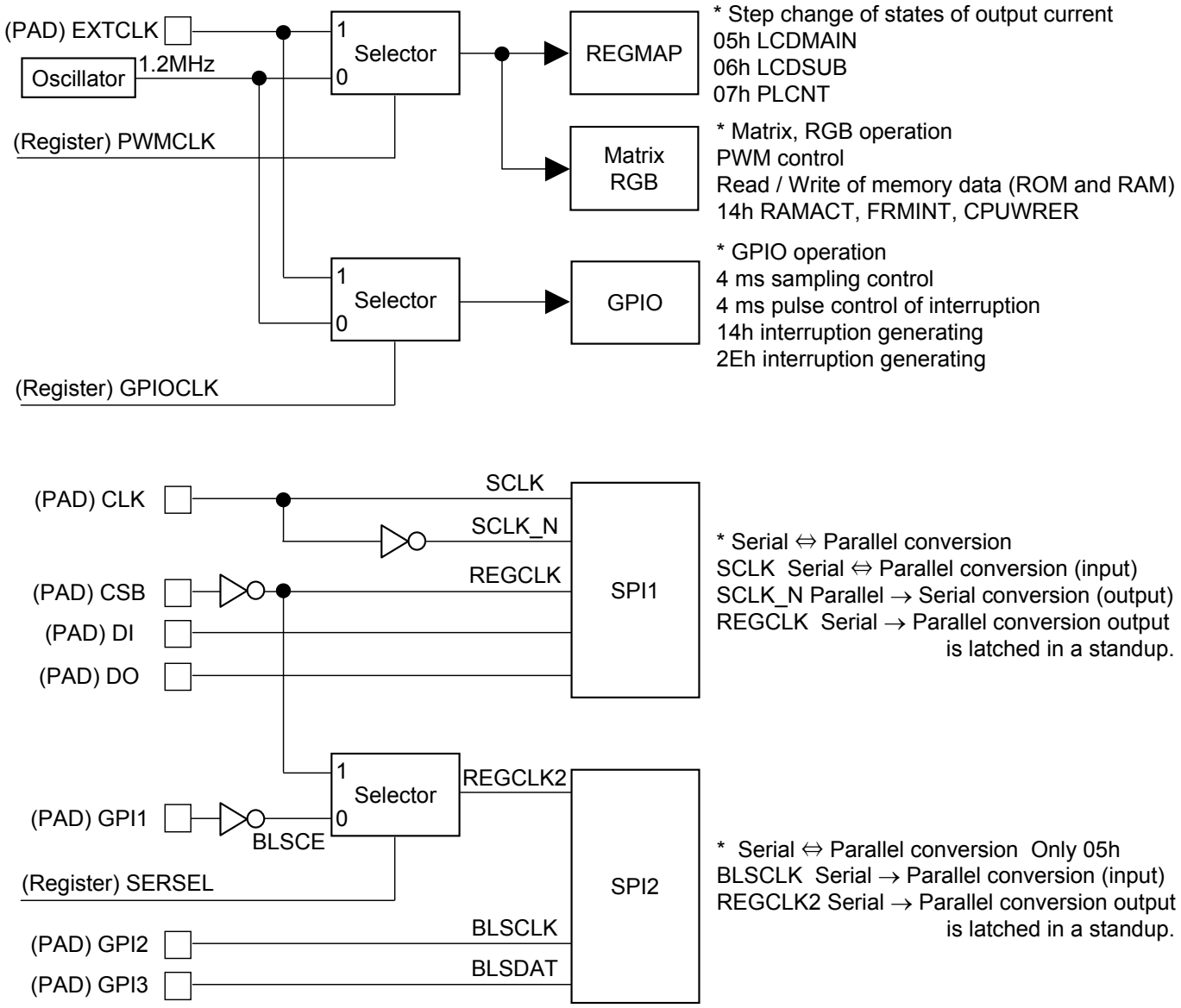
OPERATION (continued)

6. Signal distribution diagram (continued)

Control / Clock distribution diagram



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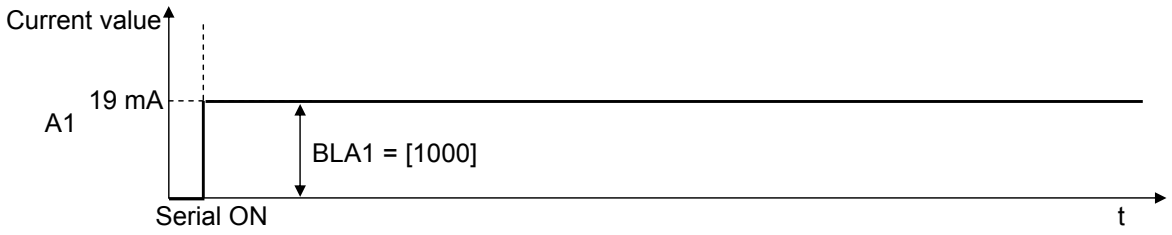
OPERATION (continued)

7. Example of firefly lighting

Example of firefly lighting 1

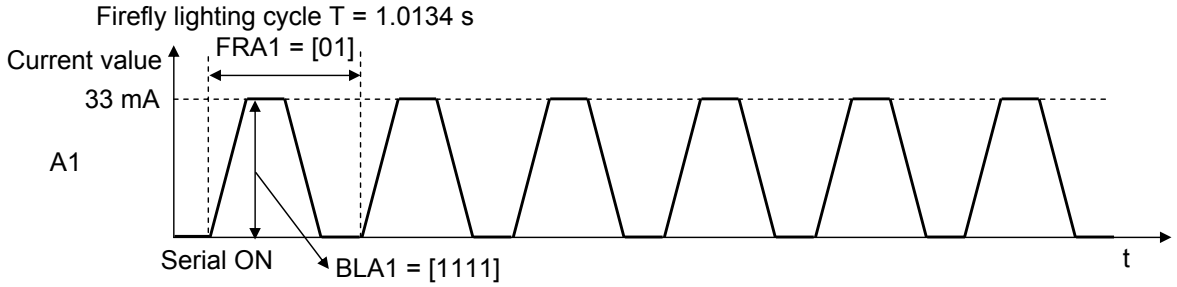
Example of initial setting for lighting

BLA1[1:0]				FRA1[1:0]		DLA1[1:0]	
1	0	0	0	0	0	0	0



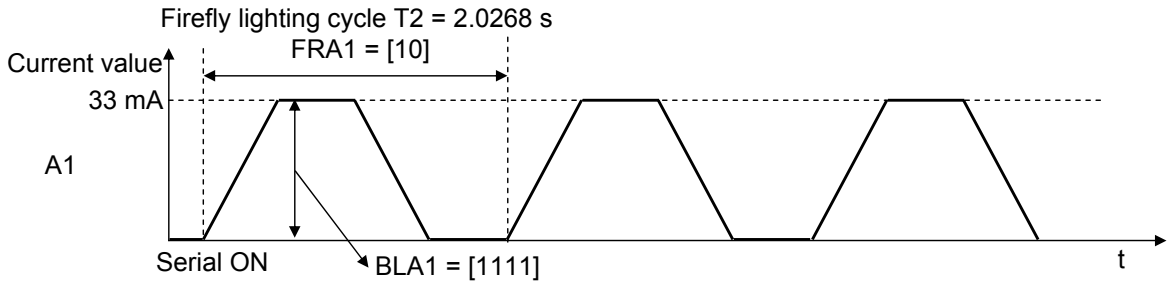
Firefly lighting setup 1 s

BLA1[1:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	0	1	0	0



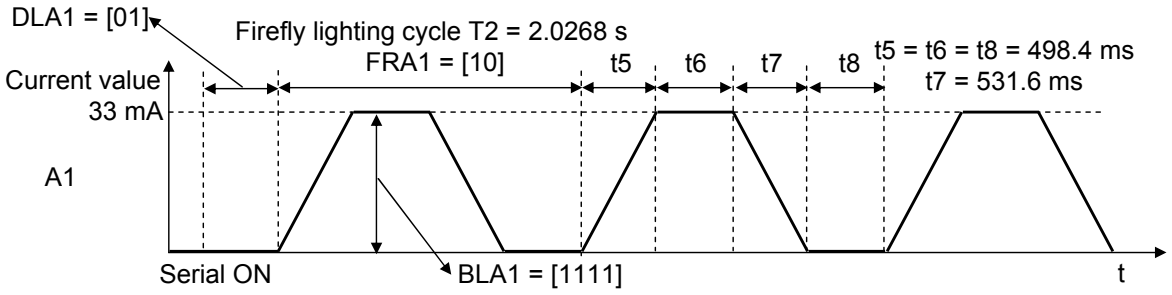
Change to cycle 1 s to 2 s

BLA1[1:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	1	0	0	0



Change to delay 0 → 25 %

BLA1[1:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	1	0	0	1



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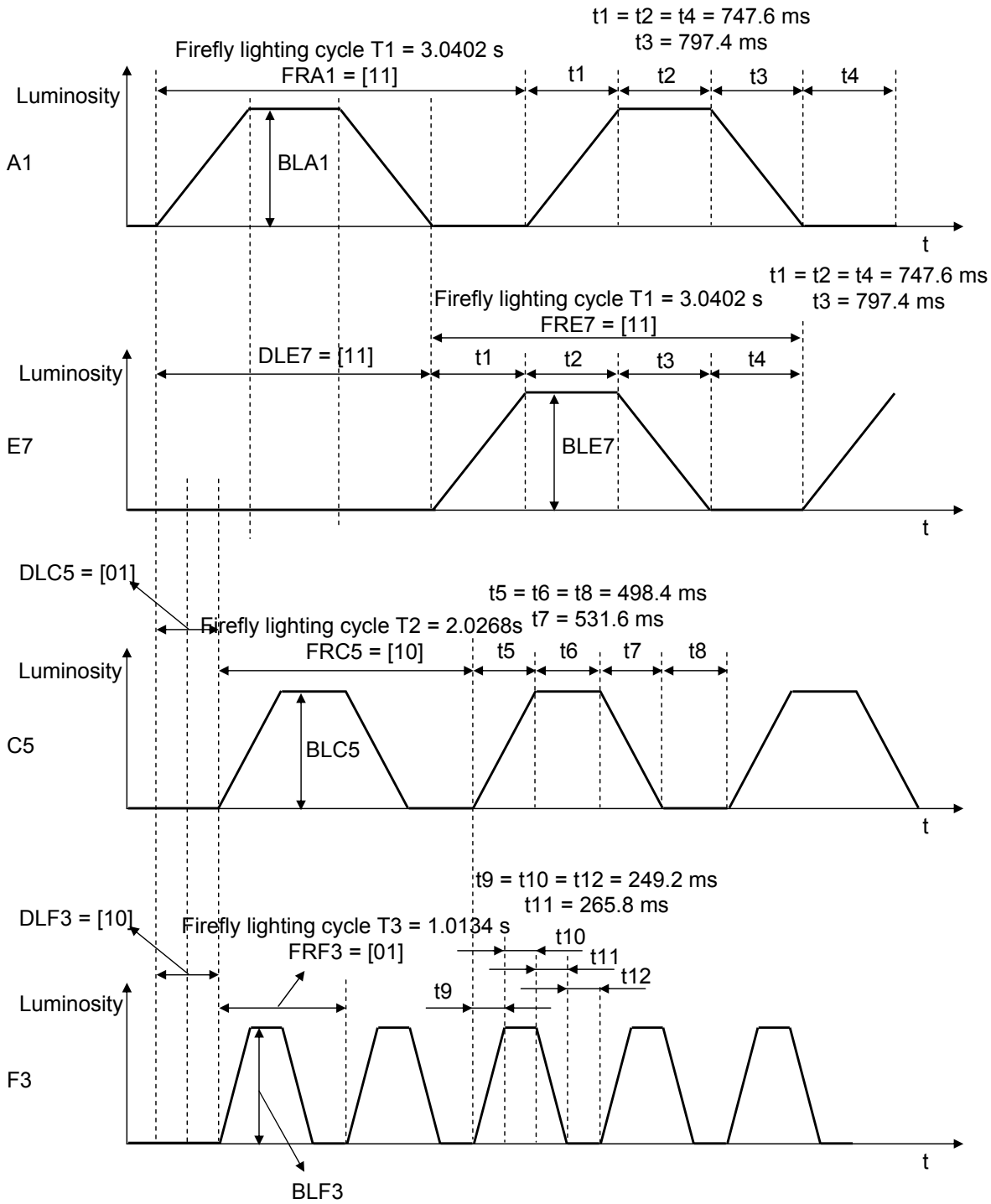
OPERATION (continued)

7. Example of firefly lighting (continued)

Example of firefly lighting 2



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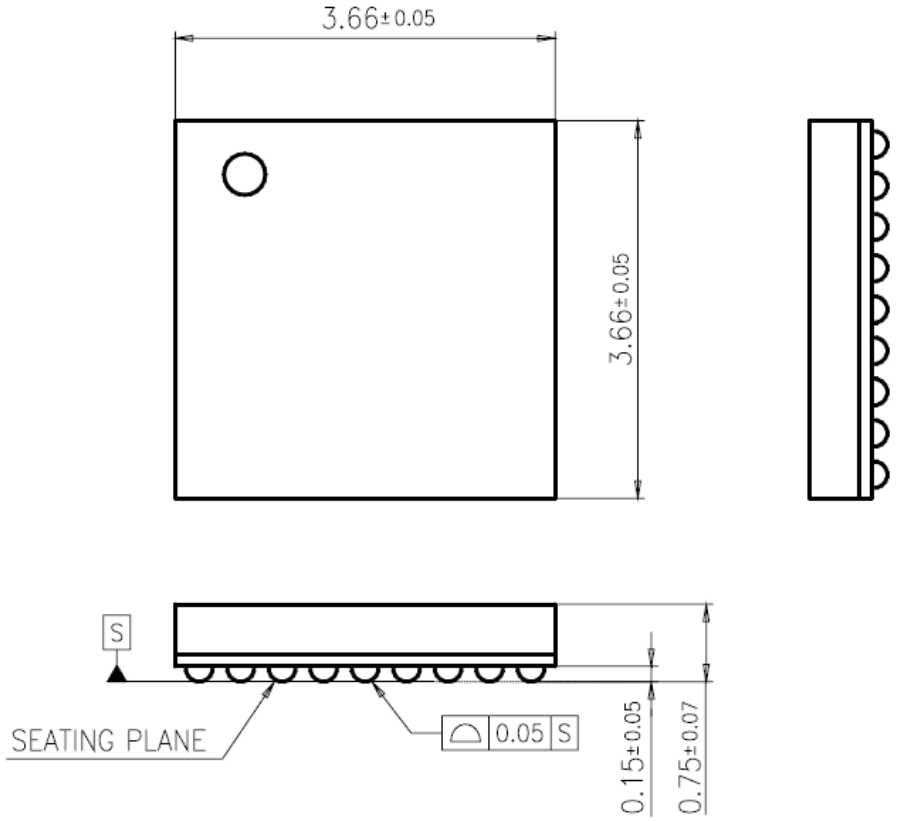
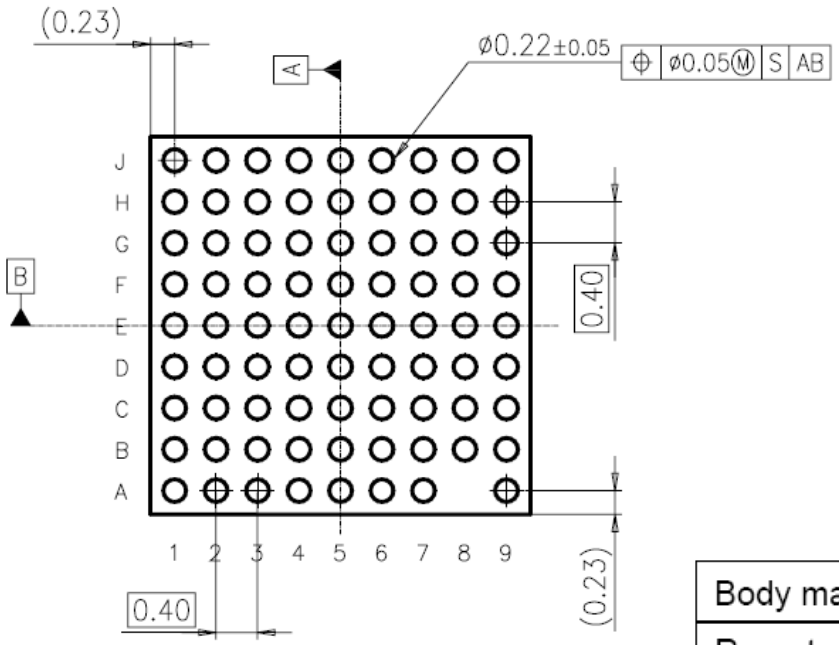
PACKAGE INFORMATION (Reference Data)

XBGA080-W-3737-AN32055A

UNIT : mm





Body material	: Epoxy resin
Reroute material	: Cu
Bump	: SnAgCu

Established : 2006-08-29
Revised : 2013-04-01

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15. Pay attention to the breakdown voltage of this LSI when using.
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