THE DATASHEET OF

74ACTQ16646SSC

FAIRCHILD SEMICONDUCTOR™

June 1991
Revised January 1999

74ACTQ16646
16-Bit Transceiver/Register with 3-STATE Outputs

General Description

The ACTQ16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition. The ACTQ16646 utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector for superior performance.

Features

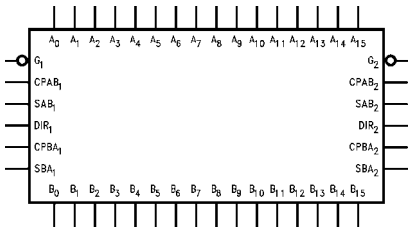
- Utilizes Fairchild FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- Separate control logic for each byte
- 16-bit version of the ACTQ646
- Outputs source/sink 24 mA
- Additional specs for Multiple Output Switching
- Output loading specs for both 50 pF and 250 pF loads

Ordering Code:

Order Number	Package Number	Package Description
74ACTQ16646SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACTQ16646MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

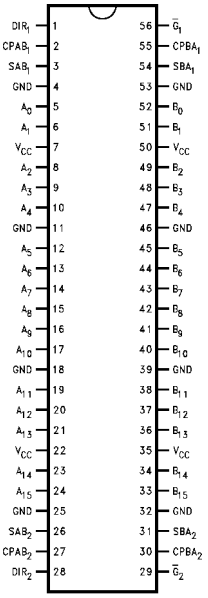
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram

Pin Assignment for SSOP and TSSOP



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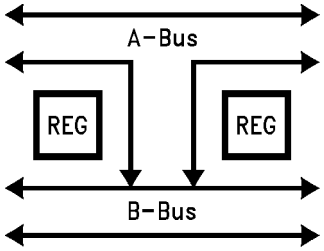
Function Table

Inputs						Data I/O (Note 1)		Output Operation Mode
G_1	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X			Isolation
H	X	↑	X	X	X	Input	Input	Clock An Data into A Register
H	X	X	↑	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X			An to Bn—Real Time (Transparent Mode)
L	H	↑	X	L	X	Input	Output	Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	↑	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L			Bn to An—Real Time (Transparent Mode)
L	L	X	↑	X	L	Output	Input	Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	↑	X	H			Clock Bn into B Register and Output to An

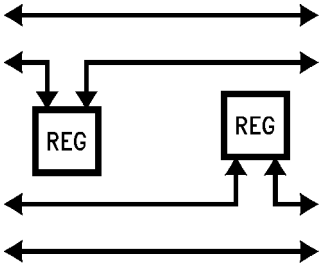
H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level ↑ = LOW-to-HIGH Transition.

Note 1: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

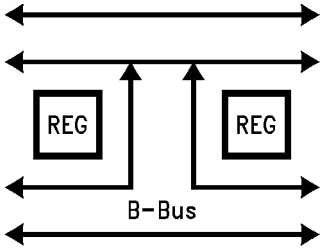
Real Time Transfer A-Bus to B-Bus



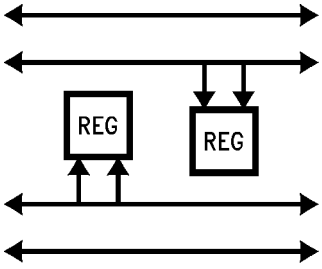
Storage from Bus to Register



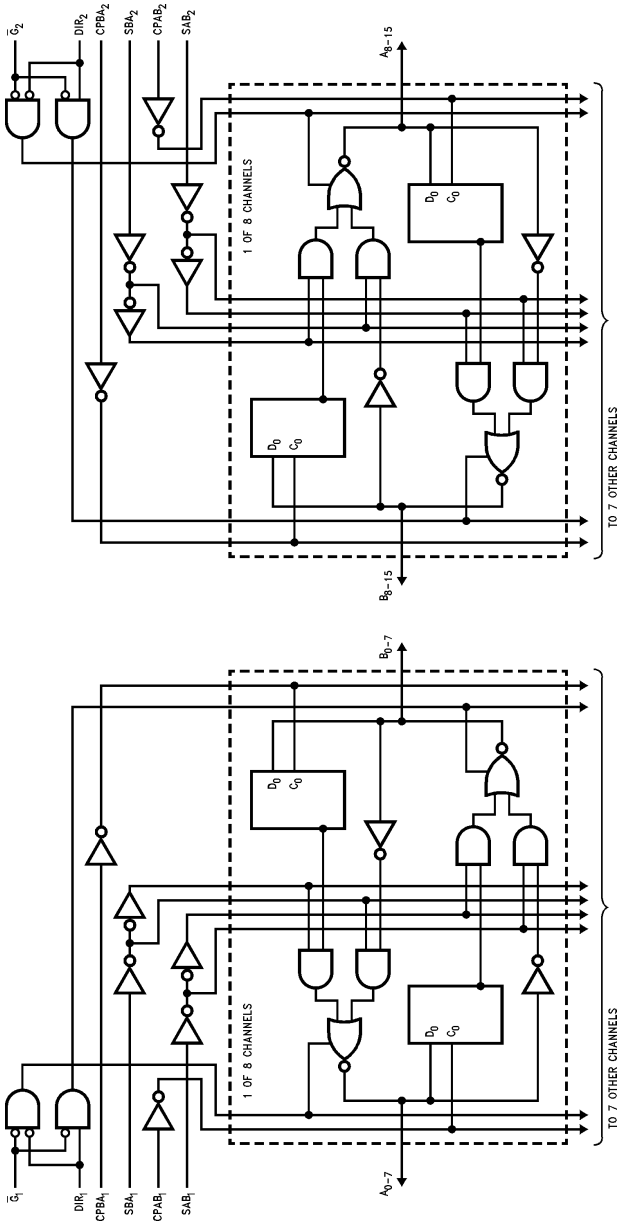
Real Time Transfer B-Bus to A-Bus



Transfer from Register to Bus



Logic Diagram



Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin	±50 mA
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum LOW	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum HIGH	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
	Output Voltage	5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 3)
V_{OL}	Maximum LOW	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
	Output Voltage	5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 3)
I_{OZT}	Maximum I/O	5.5		±0.5	±5.0	μA	V_{IN} = V_{IL}, V_{IH}
	Leakage Current						V_O = V_{CC}, GND
I_{IN}	Maximum Input	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
	Leakage Current						
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1V
I_{CC}	Max Quiescent	5.5		8.0	80.0	μA	V_{IN} = V_{CC} or GND
	Supply Current						
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 4)				−75	mA	V_{OHD} = 3.85V Min
V_{OLP}	Quick Output	5.0	0.5	0.8		V	Figure 1, Figure 2
	Maximum Dynamic V_{OL}						(Note 6)(Note 7)
V_{OLV}	Quick Output	5.0	−0.5	−0.8		V	Figure 1, Figure 2
	Minimum Dynamic V_{OL}						(Note 6)(Note 7)
V_{OHP}	Maximum	5.0	V_{OH} + 1.0	V_{OH} + 1.5		V	Figure 1, Figure 2
	Overshoot						(Note 5)(Note 7)
V_{OHV}	Minimum	5.0	V_{OH} − 1.0	V_{OH} − 1.8		V	Figure 1, Figure 2
	V_{CC} Droop						(Note 5)(Note 7)
V_{IHD}	Minimum HIGH Dynamic	5.0	1.7	2.0		V	(Note 5)(Note 8)
	Input Voltage Level						
V_{ILD}	Maximum LOW Dynamic	5.0	1.2	0.8		V	(Note 5)(Note 8)
	Input Voltage Level						

Note 3: All outputs loaded; thresholds associated with output under test.

Note 4: Maximum test duration 2.0 ms; one output loaded at a time.

Note 5: Worst case package.

DC Electrical Characteristics (Continued)

Note 6: Maximum number of outputs that can switch simultaneously is n. (n – 1) outputs are switched LOW and one output held LOW.

Note 7: Maximum number of outputs that can switch simultaneously is n. (n – 1) outputs are switched HIGH and one output held HIGH.

Note 8: Maximum number of data inputs (n) switching. (n – 1) inputs switching 0V to 3V (ACTQ). Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL}	Propagation Delay	5.0	4.6	6.9	9.4	3.6	10.1	ns
t_{PLH}	Clock to Bus		4.3	6.5	8.9	3.3	9.7	
t_{PHL}	Propagation Delay	5.0	4.0	6.2	8.5	2.9	9.2	ns
t_{PLH}	Bus to Bus		4.1	6.4	8.6	3.2	9.3	
t_{PHL}	Propagation Delay	5.0	4.0	6.4	8.9	3.1	9.6	ns
t_{PLH}	Select to Bus		4.2	6.7	9.5	3.2	10.4	
	(w/An or Bn HIGH or LOW)							
t_{PZL}	Enable Time	5.0	5.3	7.8	10.5	3.8	11.4	ns
t_{PZH}	G to An/Bn		4.6	6.9	9.4	3.3	10.2	
t_{PLZ}	Disable Time	5.0	3.0	5.5	8.1	2.3	8.6	ns
t_{PHZ}	G to An/Bn		3.4	5.7	8.3	2.6	8.6	
t_{PZL}	Enable Time	5.0	5.1	8.2	11.8	4.3	12.7	ns
t_{PZH}	DIR to An/Bn		4.6	7.5	10.8	3.7	11.7	
t_{PLZ}	Disable Time	5.0	2.9	5.8	9.2	2.0	9.8	ns
t_{PHZ}	DIR to An/Bn		3.4	6.1	9.2	2.5	9.7	

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Guaranteed Minimum		
t_S	Setup Time, H or L Bus to Clock	5.0	3.0	3.0	ns
t_H	Hold Time, H or L Bus to Clock	5.0	1.5	1.5	ns
t_W	Clock Pulse Width H or L	5.0	4.0	4.0	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, V_{CC} = Com, C_L = 50 pF, 16 Outputs Switching (Note 12)			$T_A = -40°C$ to $+85°C$, V_{CC} = Com, C_L = 250 pF (Note 13)		Units
		Min	Typ	Max	Min	Max	
t_{PHL}	Propagation Delay	4.1		10.1	6.1	14.5	ns
t_{PLH}	Clock to Bus	4.2		10.1	6.0	14.8	
t_{PHL}	Propagation Delay	4.0		10.0	5.4	13.7	ns
t_{PLH}	Bus to Bus	4.7		10.7	5.9	13.5	
t_{PHL}	Propagation Delay	3.8		9.6	5.7	14.2	ns
t_{PLH}	Select to Bus (w/An or Bn HIGH or LOW)	4.3		10.9	6.1	15.5	
t_{PZL}	Enable Time	5.0		12.7	(Note 14)		ns
t_{PZH}	G to An/Bn	4.1		11.3			
t_{PLZ}	Disable Time	3.2		8.3	(Note 15)		ns
t_{PHZ}	G to An/Bn	3.5		8.6			
t_{PZL}	Enable Time	4.1		11.3	(Note 14)		ns
t_{PZH}	DIR to An/Bn	4.4		13.0			
t_{PLZ}	Disable Time	2.9		9.5	(Note 15)		ns
t_{PHZ}	DIR to An/Bn	3.4		9.7			
t_{OSHL} (Note 11)	Pin-to-Pin Skew Clock to Bus			1.0			ns
t_{OSLH} (Note 11)	Pin-to-Pin Skew Clock to Bus			1.0			ns
t_{OSHL} (Note 11)	Pin-to-Pin Skew Bus to Bus			1.0			ns
t_{OSLH} (Note 11)	Pin-to-Pin Skew Bus to Bus			1.0			ns
t_{OSHL} (Note 11)	Pin-to-Pin Skew Select to Bus (w/An or Bn HIGH or LOW)			1.0			ns
t_{OSLH} (Note 11)	Pin-to-Pin Skew Select to Bus (w/An or Bn HIGH or LOW)			1.2			ns
t_{OST} (Note 11)	Pin-to-Pin Skew Clock to Bus			2.1			ns
t_{OST} (Note 11)	Pin-to-Pin Skew Bus to Bus			1.0			ns
t_{OST} (Note 11)	Pin-to-Pin Skew Select to Bus			2.7			ns

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 12: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 13: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 14: 3-STATE delays are load dominated and have been excluded from the datasheet.

Note 15: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	95	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

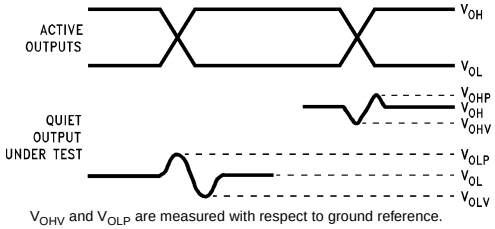
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.



V_{OHV} and V_{OLP} are measured with respect to ground reference.

Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

5. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case transition for active and enable.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

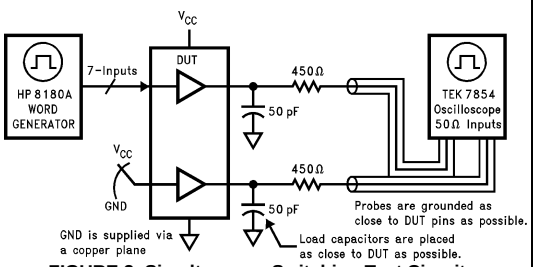
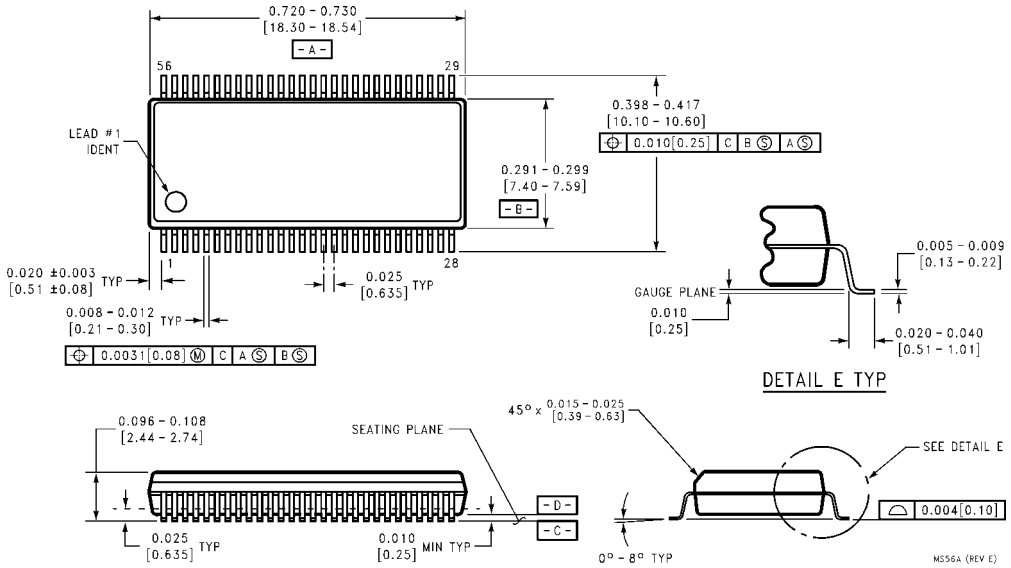


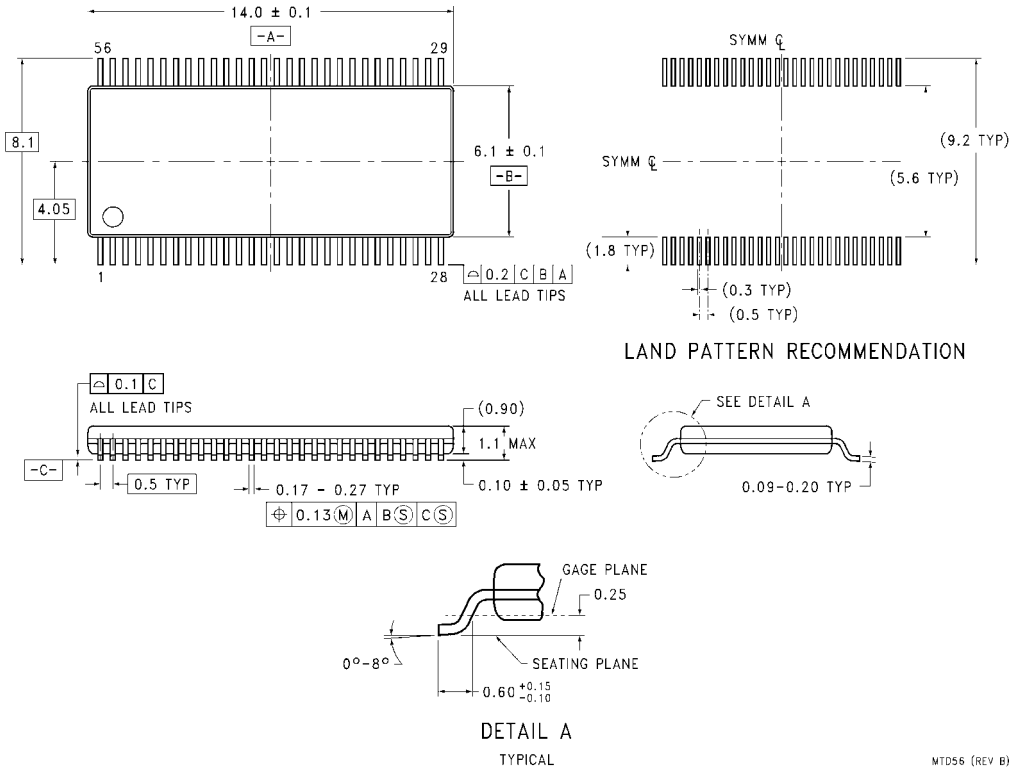
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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